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Development of the Impedance-based Arc-Flash Determination Device (IADD)

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DEVELOPMENT OF THE IMPEDANCE-BASED ARC-FAULT DETERMINATION DEVICE (IADD)

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ABSTRACT

This thesis entitled, "Development of the Impedance based Arc-Fault Determination Device (IADD)" details the development of a testing device that, when attached to an electrical node on the power system and through observations on voltage, current and phase shift with a step load change, determines the effective Thevenin or Norton impedance at the point of test. This thesis includes discussion of the theory and design process that enables the determination of an equivalent circuit, software development using National Instruments' LabView™ software development package and suggestions for future development.

The purpose of this thesis is to produce a device that can accurately and correctly predict the expected bolted fault current at the test location of interest. The importance of accurately measuring phase shift to determine X/R ratio and bolted fault current by the IADD method is examined. Several other factors that effect system impedance, performance of the IADD, and the resultant NFPA arc flash hazard level are explored. The IADD has applications in both industrial/commercial applications and power distribution systems for determining system impedance. These applications are discussed. Several laboratory and field test cases are examined and conclusions are drawn on the performance of the IADD versus other methods of determining fault duty.

DEDICATION

Dedicated to God,

my parents, Lee Allen and Karen Smith,

my siblings, Caitlin and Richard Smith,

my thesis advisor, Dr. Randy Collins,

and his staff, Curtiss Fox and Daniel Fain,

Randy Emanuel and all the folks at Duke Energy that helped make this possible,

and all those who have helped me through the trials of life.

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DEFINITIONS

Arc Fault Incident Exposure Energy: The amount of energy received at a surface, as a direct result of an electrical arc, as measured by the temperature rise on copper calorimeters.

Calorie: An energy measurement used to characterize the amount of arc flash energy which is required to cause a second degree (blister burn) on human skin. Without protection, according to the Stoll Curve, it takes about 1.2 cal/cm^2 to cause a second degree burn.

Bolted Fault Current: The condition that exists when maximum energy transfer occurs between two points of differing voltage, having little or no arcing resistance.

Equivalent Generation: Combining all points of electric generation into one Thevenin voltage source.

Frequency Bin: A band of frequencies of a specific width. This term is most often applied to signals processed by a Fast Fourier Transform (FFT) because frequency bands of equal width are partitioned by the FFT algorithm.

Hall effect: The Hall effect refers to the potential difference (Hall voltage) on opposite sides of a thin sheet of conducting or semi conducting material in the form of a 'Hall bar' (or a van der Pauw element) through which an electric current is flowing, created by a magnetic field applied perpendicular to the Hall element. Edwin Hall discovered this effect in 1879.

In-Test Mode: A mode of operation for the IADD. In-Test Mode refers to the test step in which current is flowing through the load bank and the IADD induced voltage drop and phase angle shift on the measured buss.

Pre-Test Mode: A mode of operation for the IADD. Pre-Test Mode refers to the test step in which the Thevenin voltage value is determined and a reference phase angle is established.

Stoll Curve: This is a standard curve, based on heat and time, used by the American Society for Testing Materials (ASTM) to predict the onset of second-degree burn injury. Energies above the Stoll curve would normally produce a second-degree burn. Those below the Stoll curve would normally not produce a second-degree burn.

Triplen Harmonics: Odd Harmonics divisible by three (e.g., 3, 9, 15, 21, 27, 33 …). These harmonics are particularly troublesome in three phase power systems because they remain in phase with one another in each of the three phases, possibly causing resonant coupling between phases and are additive in the neutral conductor, ground return path or cause circulating currents in the case of a delta configuration.

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CHAPTER 1

INTRODUCTION

Chapter One introduces the background of arc flash assessments and highlights the need for these types of studies, particularly in situations where there is potential for personal injury and damage due to arc flash events. This chapter provides relevance to the applications and shows the need for a device such as the IADD (pronounced "eye-add") in real world conditions.

Between five and ten times a day, an arc flash explosion occurs in electrical equipment in the United States. These arc flash explosions send a burn victim to a special burn center, according to statistics compiled by CapSchell, Inc., a Chicago-based research and consulting firm that specializes in preventing workplace injuries and deaths. That number does not include cases sent to regular hospitals and clinics, or unreported cases and "near misses". Dr. Mary Capelli-Schellpfeffer, principal investigator, noted there are one or two deaths a day from these multi-trauma events. [1]

The costs of these incidents are staggering. According to a 1999 Electric Power Research Institute (EPRI) study cited by CapSchell, a utility company's total spending estimate for electrical incidents over a two-year period was 15.75 million dollars per case when related indirect costs were considered along with the direct expenses. [2]

In response to these statistics and the obvious detrimental affects of arc fault incidents on workers, the Occupational Safety and Health Administration (OSHA) has

begun enforcing recommendations by the National Electric Code (NEC) and National Fire Protection Association (NFPA) regarding employee safety procedures when work on energized systems must be performed. See Appendix A for the current interpretation of OSHA regulations concerning compliance with NFPA 70E. [3] Admittedly, it is preferable and mandated that, when possible and practical, electrical systems are to be worked on in a Zero Energy State (ZES). However, this condition does not exist under all circumstances, and sometimes work on energized systems is necessary.

The 2000 release of the NFPA's 70E document recommended the use of personal protective equipment (PPE) based on the potential for exposure to heat energy radiated by electric arcs. [4] NFPA 70E specifies the need for proper PPE, in all conditions where there is a possibility of harm induced due to electrical arcing. Previously, electric shock had been thought to be the primary and the most frequent type of injury sustained when working with electrical systems. However, according to the National Institute of Occupational Safety and Health, a recent study on injuries sustained during work with electrical components indicates that approximately forty percent of these injuries were due to arc flash. An arc flash exposure may result in severe burns to the skin and, in some cases, death. [5]

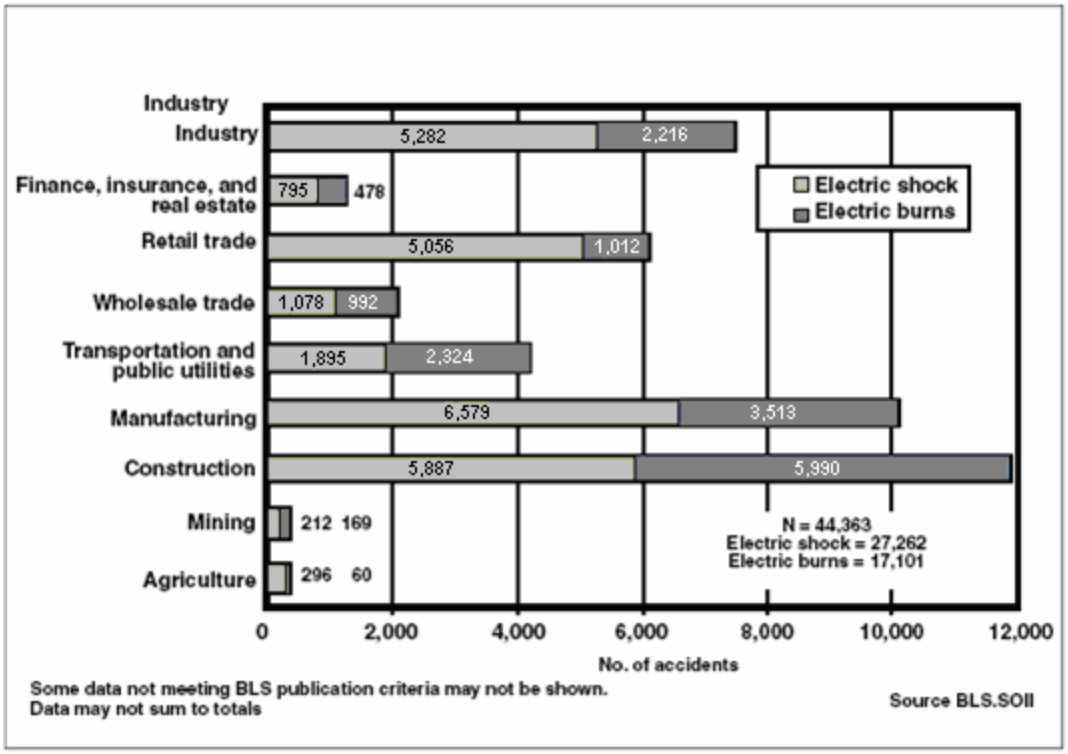

Figure 1.1. Non-fatal electrical accidents involving days away from work, 1992-2001. Source: Journal of Safety Research.

In 2002, the NEC 70-2002 document further expands on this requirement by mandating that all electrical services that can be accessed while energized be labeled with the hazard category as defined by the NFPA. However, neither document has yet to specify the method by which these values are to be calculated.

Category	Cal/cm^2	Clothing
0	1.2	Untreated cotton
1	5	Flame retardant (FR) shirt and FR pants
2	8	Cotton underwear, FR shirt and FR pants
3	25	Cotton underwear, FR shirt, FR pants and FR coveralls
4	40	Cotton underwear, FR shirt, FR pants and double-layer switching coat and pants

Table 1.1. Determining PPE hazard risk category, Source: NFPA 70E.

In response to these considerations, the IEEE, in 2004, issued IEEE 1584. This standard gives the electric power industry a way to gauge arc flash hazards. It lets

designers and facility operators determine arc flash hazard distance, and how much incident energy employees might be exposed to when they work on or near electrical equipment. These calculations form the basis for re-engineering systems to reduce incident energy to manageable levels or to provide guidance for the appropriate level of PPE to be worn while working on or near energized equipment. [6] The goal of this thesis is to produce a device that can accurately and correctly predict the expected bolted fault current at the test location of interest.

CHAPTER 2

DETERMINING ARC FLASH INCIDENT ENERGY

Chapter Two further develops the background for development of the IADD. The IEEE 1584 standard is reviewed for pertinent information, and a survey of comparable devices and literature in this field is presented. This chapter provides additional application related material supporting the merits of the IADD. A review of current techniques used to perform arc flash assessments in the field highlights the potential for reduction in computation and work by using the IADD to conduct arc flash assessments.

As stated previously, the NFPA 70E document requires calculation of arc fault incident energy, but neither provides or specifies any one method of determining this value. As defined by the NFPA, several acceptable methods of determining arc fault incident energy have been proposed. These methods include the IEEE 1584, NFPA 70E, Lee's Calculation [7], ARCPRO by Kinetrics of Toronto [8], and the Duke Heat Flux Calculator, by Duke Energy. The IEEE Standard, Duke Heat Flux, and NFPA 70E use equations developed from empirical testing, while the Lee paper and ARCPRO use equations based on theoretical analysis.

Article 130 of the NFPA 70E document details the requirements for the establishment of boundaries for safe working under live circuit conditions. Portions of this document are included in Appendix B, since NFPA 70E is driving the push for these assessments.

The IEEE 1584 standard is only one of several methods of calculating potential arc fault incident energy, but is widely used in the industry. The variables used in the IEEE calculations can be readily obtained with some knowledge of enclosure geometry, wire spacing, and fault duty. The IEEE standard also has been tested and validated for a wide range of conditions. It specifies that the Lee equations should be used for voltages above 15 kV. The calculations consider three-phase arcs in enclosures and in air. The standard is applicable for input ranges for voltage of 208 to 15,000 volts, bolted fault current of 700 A to 106 kA, equipment enclosures of commonly available sizes, and gaps between conductors of 13mm to 152 mm (0.5 to 6 inches). The equations were developed from curve fitting of results of values measured from testing performed by the standard's working group. Several general conclusions resulting from their testing were found. System X/R ratio, system frequency, and electrode material had little or no effect. Instead, the incident energy depends primarily on arc current. The buss gap (arc length) is only a small factor in the final result.

The IEEE 1584 outlines nine procedural steps in determining arc fault incident energy:

1. Collect the system and installation data
2. Determine the system modes of operation
3. Determine the bolted fault currents
4. Determine the arc fault currents
5. Find the protective device characteristics and duration of the arcs
6. Document the system voltages and classes of equipment
7. Select the working distances
8. Determine the incident energy for all equipment
9. Determine the flash-protection boundary for all equipment

The document states that the majority of the work in completing an arc flash assessment is in the collection of system and installation data (step one). This singular step is expected to account for fully one-half of all the effort in performing such a study. Obtaining the fault duty at a particular electric node can be difficult to determine. Often the wiring diagrams for electrical installations are outdated or lacking necessary information, such as wire size or feeder length. Furthermore, the drawings may be incorrect all together. Rotating loads and varying generation, particularly near the node of interest, can also have major effects on fault duty and are time varying in nature. The majority of remaining analytical work is contained in steps two and three. By effectively skipping steps one through four of the nine step procedure outlined by the IEEE, a significant source of manpower, time and money can be eliminated from an arc flash assessment.

Many entities are currently not compliant with OSHA regulations concerning arc flash assessments and documentation. Previously, OSHA has taken a lenient stand on this issue because methods for determining boundaries as defined in the NFPA have only recently been developed. However, now that the IEEE 1584 standard has been accepted as a viable method of performing these assessments, OSHA has begun vigorously enforcing these requirements to better protect workers from this hazard. [16]

The development of a method to reduce the effort required to reach these end results could radically impact the compliance issues now being faced by most industrial and commercial customers. The prospect of investing large amounts of money into a traditional arc fault assessment when compared to the option of performing this task

quickly and economically makes the development of devices such as the IADD appealing.

2.1. Necessity of Arc Fault Assessments

Burns are sustained due to exposure to a heat source, in this case the heat radiated from an electrical arc. Arcs have temperatures of around 35,000 degrees F (19500 ^{o}C). [9] Distance plays a role in the degree to which injury is sustained. The amount of energy absorbed by the skin at any given time is a function of the temperature of the heat source and the distance from this source to exposed skin. In this case, incident energy is typically calculated in cal/cm^2. An energy density of 1.2 cal/cm^2 is sufficient exposure to result in second degree burns on exposed human skin. [4]

OSHA requires all electrical panels under its jurisdiction to be labeled to indicate the appropriate amount of PPE required while working inside of the panel with it energized. This table defines the PPE required based on arc flash category, which is presented in Table 1.1 of this thesis, and additional detail is included in Appendix B. Currently, OSHA code requires that all employers make an effort to investigate the potential for injury due to arc flash. Noncompliance with this directive may result in monetary penalties and liability in the event of an accident. This new requirement has prompted an influx in awareness to potential damage as a result of arc flash and consequently, is forcing engineers to find ways to determine the appropriate level of protection required in each case. Companies may spend millions of dollars on arc flash assessment surveys, and currently only a very limited number of entities are providing these assessments because of the high cost in manpower and time.

2.2. Review of Present Arc Fault Assessment Techniques

Currently, there exist few methods for establishing the potential for exposure to arc flash energy. The classic method of obtaining fault current is to determine fault current capacity from information based on power system information.

$$I_{Fault-duty} = \frac{V_{Nominal}}{Z_{Service-Impedance}} \tag{2.1}$$

Typically, the electric utility company that supplies a site with electrical power can give service impedance based on fault duty calculations and system models. IEEE 1584 specifies that "available fault data must be realistic; not conservatively high." [6] The document goes further to offer the following reasons for this requirement:

"Available bolted fault currents should be determined at the point of each potential fault. Do not use overly conservative bolted fault current values. A conservatively high value may result in lower calculated incident energy than may actually be possible depending on the protective device's time-current curves. The lower results would be caused by using a faster time-current response value from the protective device's time-current curve." [6]

Overestimating fault current can be dangerous for the simple reason that protective devices often have an inverse or extremely inverse time curve. This is illustrated in Figure 2.1.

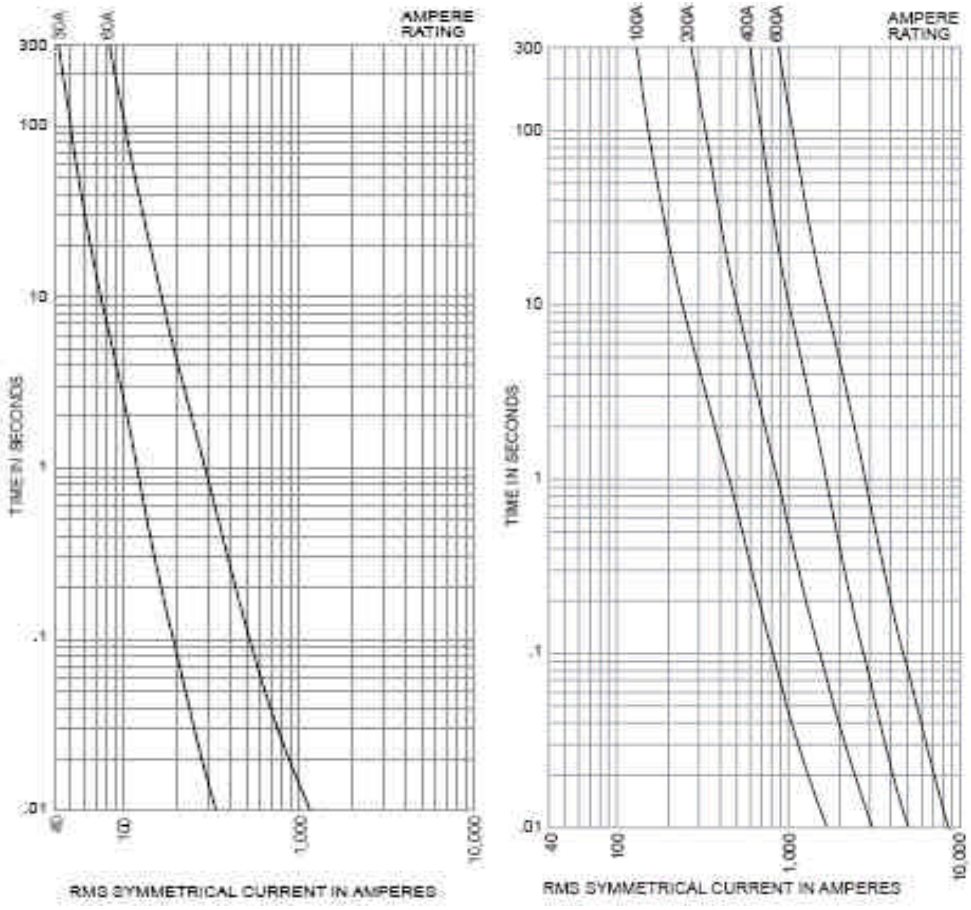

Figure 2.1. Inverse time curves for J type fuses, source: Cooper-Bussmann.

As these curves indicate, the length of time before operation is inversely proportional to the amount of current flowing through the protective device. For example, using the fuse curves presented in Figure 2.1 with a current rating of 200 amperes (amps) and an arc of 1 kA would protect in 0.5 seconds, whereas an arc of 500 A would protect in nine seconds. The first condition results in a delivery of 500 A-s of electric charge, and the second results in an exposure of 4500 A-s of electric charge. Therefore, the likelihood of significant bodily injury due to incident energy exposure may be greater under the lower arc fault condition. Following this reasoning, conservatively high arc fault duty estimations may result in underestimating the potential for exposure to incident energy if protection curves are taken into account.

Protection data is one of the parameters taken into account in the IEEE 1584 calculations.

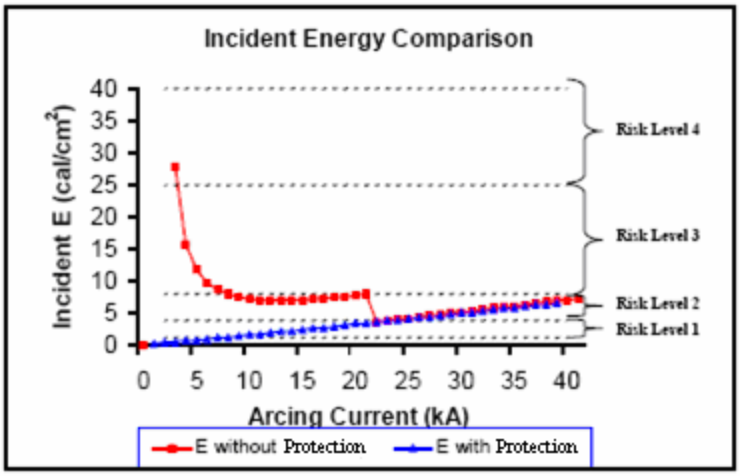

Figure 2.2. Incident energy levels with backup instantaneous and time over-current protection. [10]

Another method of performing arc fault assessment includes a detailed analysis of the system in conjunction with specialized computer software to simulate and to determine the arc flash incident energy potential. To adequately complete such an analysis, the estimated power system impedance is once again assumed at the service to the site of interest. This type of analysis goes a step further to include all wires sizes and lengths, protection equipment, and enclosure types for the system. Then, this data can be entered into the appropriate analysis program, and the results can be obtained. While this method is valid and has a high degree of accuracy, it tends to be time and labor intensive, which leads to large costs for compliance. Also, in many cases, one-line diagrams for an industrial site are out-dated and do not contain modifications that have been completed over the years. Incorrect drawings may result in incorrect estimates of arc fault potential due to errors in calculated fault duty.

One recent paper has been presented in the IEEE Transactions on Power Systems that suggests an alternate method for obtaining bolted arc fault potential. In the article, "Using a Microprocessor-Based Instrument to Predict the Incident Energy From Arc Flash Hazards" by Baldwin, Hittel, Saunders, and Renovich [11], it is suggested that the application of current injection at varying frequencies be used to obtain impedance values. The frequency modulation of the current signal quite accurately yields an X/R ratio and the application of Ohm's Law will yield the impedance modulus. To obtain accurate results, current levels in the thirty amp range are specified to mitigate the effects of power system noise. This implies that a significant amount of power may be required, particularly on higher voltage systems.

Another method is presented in the article, "Method for AC Powerline Impedance Measurement" by Gasperi, Jenson and Rollay [12], wherein a similar approach of introducing a load to the power system is used to measure transient effect due to the known load. In this case, the load is an RC load is used to create an electrical transient oscillation. The transient ring frequency and damping factor are the variables used in this case to determine system inductive and resistive parameters. This solution can be problematic in systems that are highly sensitive to transient over voltage events as in the case of electric motor drives. Exposing systems to transient over voltages should be avoided to reduce the risk of exciting further resonance in the power system or disrupting protective devices such as metal oxide varistors (MOVs).

To date there has been little or not literature documenting the dynamic nature of the power system as it applies to impedance at the point of utilization. With the development of devices like the IADD, additional studies on this topic are possible.

CHAPTER 3

THEORY AND EXPERIMENTAL DEVELOPMENT

Chapter Three serves to explain the basic principles of operation of the IADD. The device operates on basic principles of electrical engineering and electricity through conductors. An example of how the IADD operates, its effect on a subject power system, and the resultant measurable changes is demonstrated in this chapter. By creating subtle changes in an electrical distribution system and measuring very specific parameters, the IADD is able to determine the bolted arc flash incident energy. A simplified power circuit topology is also presented.

The goal of this thesis is to produce a device that can accurately and correctly predict the expected bolted fault current at the test location of interest. To accomplish this goal, the device will apply a known load at the test location. The device also will measure the change in RMS (Root Mean Squared) voltage due to the step increase in loading conditions and the accompanying phase shift in the voltage waveform as a result of the change in loading conditions at the test node. Subsequently, the load current is measured to more accurately measure the real time load imposed upon the system. With knowledge of the load impedance, an accurate equivalent Thevenin or Norton system, resistive and reactive parameters and X/R ratio, can be derived through a series of mathematical calculations. Then, using the derived equivalent circuit, an accurate estimate of the fault duty can be obtained.

The IADD is developed based on these principles and is devised as an alternative means to accurately predict arc fault incident energy potential through measurement rather than computation and modeling. Through development, several applications for this device have been realized including applications in the power industry for gauging system equivalent impedance and establishing or confirming protection schemes. It will additionally provide industrial customers with more accurate fault duty values at an electrical service entrance. The possibility for real time monitoring and evaluation of changing impedance on a dynamically changing power system may also be realized through the efforts of this project. The device has been developed through a joint venture between Clemson University and Duke Energy.

The underlying principle for arc fault detection and the operation of the IADD is the ability to determine the Thevenin equivalent circuit as seen "looking" into the buss at the test location. This equivalent circuit would include all series and parallel devices connected to the buss, including switchgear, cables, transformers, and other devices as well as networked sources such as rotating machines. In general, the Thevenin equivalent impedance can be determined from two conditions:

1. The open circuit voltage, which is the Thevenin voltage source
2. The short circuit current in a zero impedance fault at the test location buss

Alternatively, the IADD can compute the dual of the Thevenin equivalent circuit, called the Norton equivalent circuit. The Norton equivalent circuit comprises a parallel ideal current source and impedance. The Norton current source is equal to the

short circuit current into a zero impedance fault (the so-called “bolted fault current”), and the Norton impedance is equal to the Thevenin equivalent impedance.

There is difficulty in defining these values from an intrinsic sense. Due to the dynamic nature of the power system, the voltage at any given location in the power grid is always in a state of flux, both in magnitude and phase angle. There are several reasons for voltage fluctuation on the power system including, but not limited to, the amount of generation present on the system and voltage regulation devices such as switching power factor correcting capacitors and tap changing transformers. A significant source of voltage variation is the constant changes in loading conditions, particularly large load changes such as motor starting or arc furnaces that may cause brief changes in the RMS voltage. Several strategies must be employed to mitigate the likelihood of error due to voltage/load variation. To minimize the likelihood of error due to voltage variation and changes in loading conditions, the time of a complete test must be minimized such that establishment of baseline voltage data is not skewed when the test load is applied.

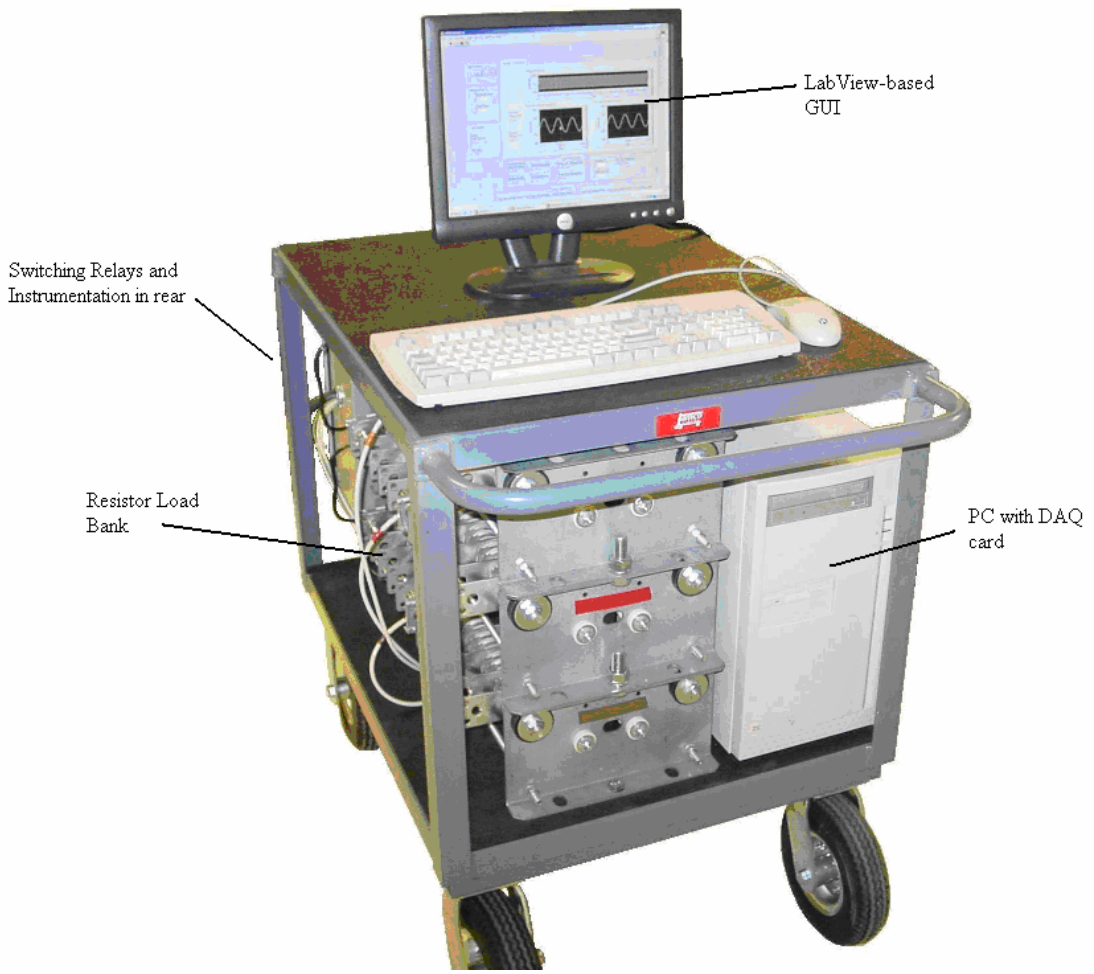

Figure 3.1. IADD – Impedance based Arc-Fault Determination Device.

The theory of voltage division states that the voltage across any series element will be distributed according to the ratio of total series impedance to the impedance of measurement. Therefore, any change in the system will result in a change in the observed voltage at any given point, except at the point of equivalent generation where voltage is assumed to be regulated and constant. This idea is illustrated in Figures 3.2 and 3.3.

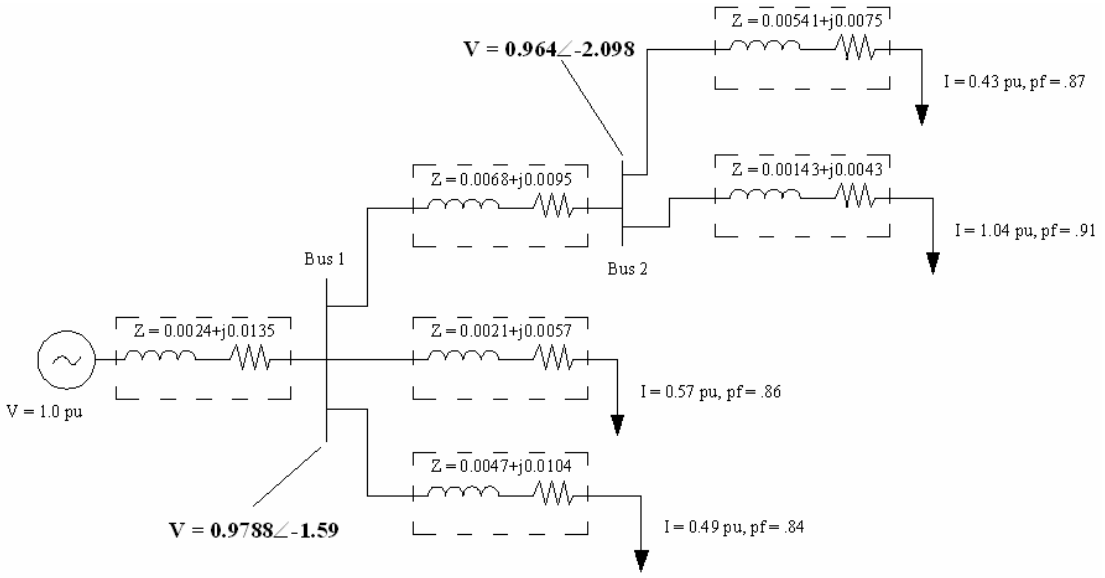

Figure 3.2. Simulation system without IADD device installed.

Figure 3.2 shows a subject electrical power system with a single point of generation, and four loads drawing current with specified magnitude and power factor. Voltages at busses one and two are also displayed in per unit magnitude and phase angle with respect to a reference angle of zero at the generator. Figure 3.3 shows the addition of another load, in this case the addition of the IADD device, which draws current at a unity power factor and affects both the voltage magnitude and phase angle at buss two.

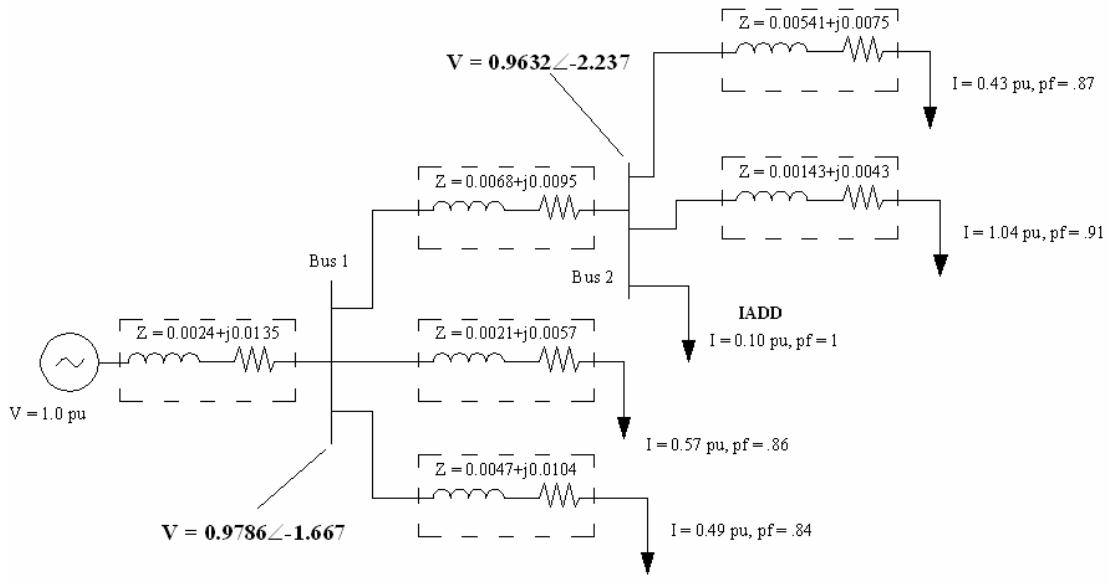

Figure 3.3. Simulation system with IADD device installed and drawing current.

Figures 3.2 and 3.3 serve to illustrate the small variations in voltage and phase angle that occur when a step change in loading condition is made on a system. If these variables, voltage magnitude change and voltage phase angle change, can be measured, then a determination on impedance between the test node and the source can be made. With this information, the bolted fault current at the test node becomes apparent. Initial testing to determine feasibility of this idea involved the construction of a test stand by which waveforms could be captured and analyzed for voltage change and phase shift. The “version one” IADD is constructed as follows:

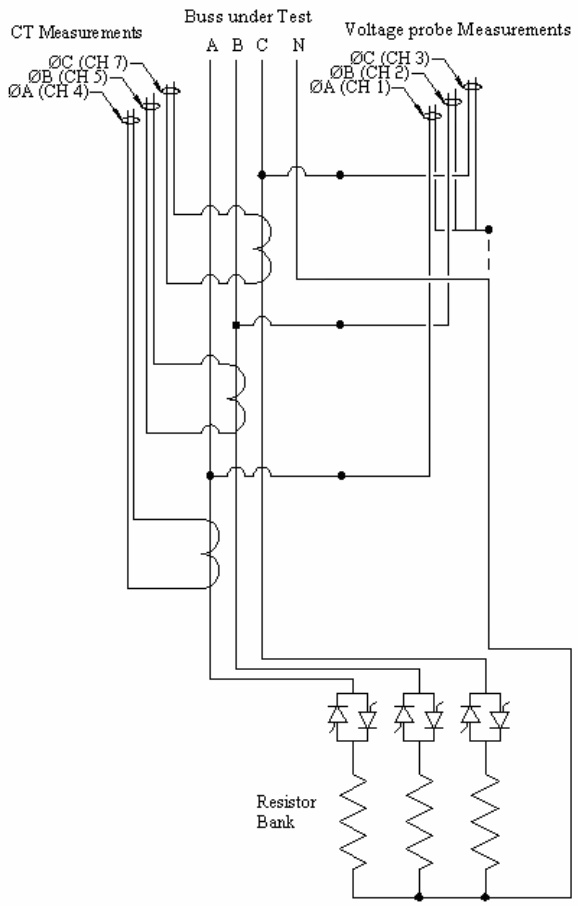

Figure 3.4. IADD system design, including voltage and current measurement for resistive load condition.

Figure 3.4 depicts the topology of the IADD. It features three phase, real-time voltage and current measurement through optically isolated differential voltage probes and current transformers (CT). The current transformers are Hall Effect type CTs that have the ability to measure DC offsets present during most transient events. The resistor bank is a modified dynamic braking resistor bank commonly used in adjustable speed motor drives for dissipating energy from a regenerating or overhauling rotating load or other energy source. The resistors are switched in and out of the circuit through three solid state voltage controlled relays with a gate signal provided by the control unit. These are modeled here as two thyristors with bipolar operation. Subsequent versions of the IADD double the current-drawing capacity by adding a second set of

solid state relays in parallel with the three shown in Figure 3.4 It uses a separate digital gating signal that may be selected on demand via user control input. The control system (not shown in Figure 3.4) is a custom built PC running LabView development software and integrates an eight channel simultaneously sampling data acquisition (DAQ) card as the principle method of both gathering measurement data and outputting control signals to the SSRs. Detailed descriptions of these components are presented in Chapter Four.

CHAPTER 4

HARDWARE DEVELOPMENT

Chapter Four introduces the hardware configuration and components used to construct the IADD. This chapter describes several iterations of construction and details many of the challenges experienced during the development of the IADD. The IADD continues to evolve as these challenges are met, and new improvements in functionality and capability are realized.

The IADD has been developed in the Power Quality and Industrial Applications (PQIA) lab at Clemson University to implement the required tests necessary to determine the Thevenin or Norton equivalent system impedance at the point of testing. The project is funded by Duke Energy to address concerns of their customers regarding fault duty values provided by Duke. All components were chosen based on specific needs and specifications required to complete this goal. This chapter details the various components, the specifications, and the method by which they were chosen and applied. There are several components that make up the IADD system. They have been grouped into the following subsections and will be discussed in detail in this chapter:

1. Resistive load bank
2. Voltage measurement circuitry
3. Current measurement circuitry
4. Solid state switching relays
5. Data acquisition, measurement and control

Initial development and testing has been carried out in the PQIA lab in Riggs Hall at Clemson University. Additional details on field tests conducted with the IADD are found in Chapter Nine of this thesis.

4.1. Resistive Load Bank

Several loading options were considered during the concept phase of the IADD project including capacitor switching, motor starting, resistive loads and reactive loads. Of these possible loads, two types were investigated: the resistive load and motor starting load. After reviewing and analyzing sample waveforms captured through the use of a digital oscilloscope, the resistive load is selected. Additional support of this decision is presented in Section 4.2.

The three plate resistors used in the initial design were measured with a precision resistance meter to be 1.25 ohms each at room temperature. There is negligible measured capacitive and inductive reactance at the specified voltage and the frequency levels between the terminals of the resistive banks. These resistors are rated for three kilowatts under steady state conditions. Grid type resistors have a particular advantage over wire-wound resistors in that the inductance and capacitance for the grid type resistor is significantly smaller than its wire-wound counterpart. Due to construction practices and design, these resistors typically cool at a much faster rate. All surfaces are exposed to open or forced air cooling. During testing, these resistors can be required to dissipate to up to 200 kilowatts of power for short durations when testing is performed at 575 volts (line to line voltage). This voltage level is specified as the maximum operating voltage to accommodate most arc flash assessment needs in industrial and commercial locations. The IADD has been initially tested on a 208 volt,

three phase system attached to the Riggs Hall building supply. At this voltage level, the current is calculated and observed to range around 96 amps. Typically, the voltage in the building during the day is lower than nominal; therefore, the current is most often observed to be approximately 91 amps. Potential changes in resistance due to heating are taken into account, because both load current and voltage waveforms are being measured simultaneously; thus, the system is effectively immune to resistive changes due to heating.

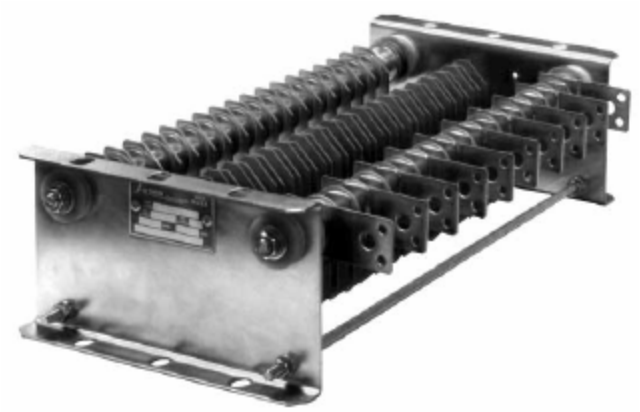

Figure 4.1. Avtron stamped metal grid resistor, AGR series

At 575 volts, the original resistors used in testing on a 208 volt system would be inadequate to handle the power seen on higher voltages systems. As such, a load configured to handle higher power is utilized in future embodiments of the IADD, which are exposed to higher voltages. A dynamic breaking resistor from Avtron Manufacturing of Cleveland Ohio is used. The AGR41 resistor is a tapped resistor, which is capable of handling 8.3 kilowatts of power continuously and has a maximum resistance of 5.1 ohms. These characteristics allow the resistive load to be used on systems of varying voltage levels. A relatively heavy load can be created by appropriate selection of one of eleven taps on the resistor for the desired load. For

instance, on a 600 volt system, the phase voltage is approximately 380 volts. A resistance between three or four ohms might be chosen to draw currents of approximately 100 amps. On a 208 volt system, a resistance closer to 1 ohm might be chosen to draw the same amount of current. These were considerations that were taken into account when specifying what type of resistive load to use in design and construction of the IADD.

The amount of current to be drawn depends on the "stiffness" of the system. Specifically, the stiffness is characterized by how much impedance is between the test location and the Thevenin equivalent voltage source. Field tests have shown that, in some instances, the current drawn during testing must be increased based on the parameters of the system and based on how immune the system is to transient load changes. Generally, the accuracy of the results improves with increases in loading. However, increases in loading cause increases in voltage drop. It is undesirable to cause a voltage drop (a so-called voltage "dip" or "sag") deep enough that either equipment in the facility malfunctions or that an undesired power system dynamic results. Voltage drop at or below five percent will be well-tolerated in most situations based on the ITI/CBEMA curves. [13] An analysis examining the impact of current drawn to detection accuracy is presented in Chapter Eight.

Of course, each electrical power system differs, and additional studies have been planned to determine the optimum amount of current to draw in order to create a measurable change in voltage sag and phase shift. Additional future plans would include a switching scheme that automatically selects the appropriate resistance level

based on measured voltage prior to testing. Further discussion about future development is included in Chapter Ten of this thesis.

4.2. Other Loading Options

Other loads were considered for the test load including inductors, capacitors, combinations of RL and RC circuits, and induction motor starting (especially one with a high inertia mechanical load). Depicted in Figure 4.2, an examination of phasor diagrams is used to illustrate the potential advantages and disadvantages of using such loads.

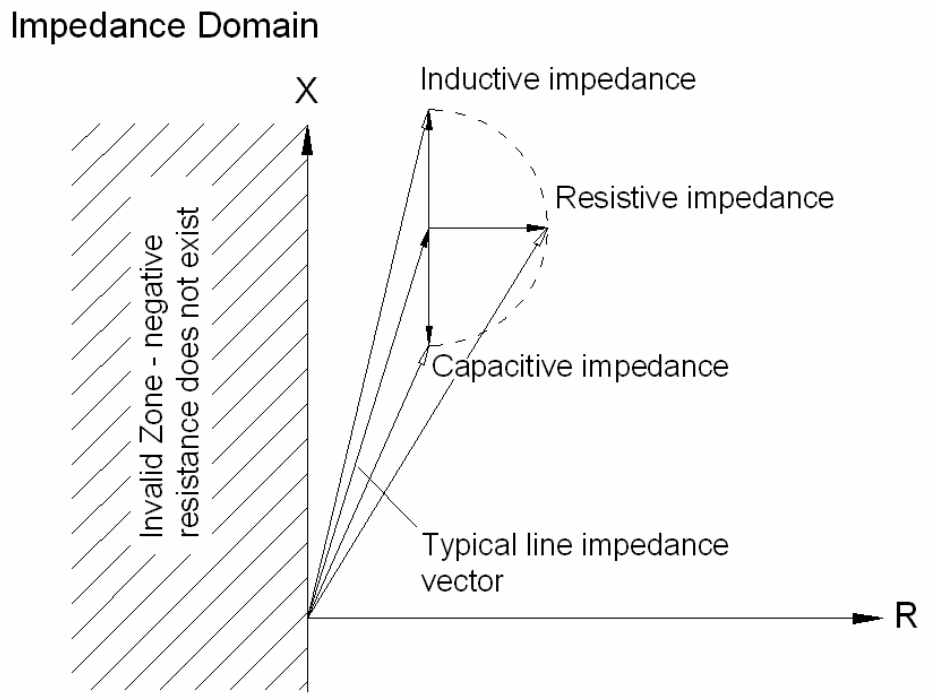

Figure 4.2. Impedance diagram illustrating the effect of various loading conditions on resultant impedance phasor.

Each loading condition offers different results in terms of changes in magnitude and phase angle of the resultant impedance phasor. For instance, both the inductive and capacitive loads offer large changes in impedance magnitude, but only a marginal

change in impedance angle. The resistive load, however, changes both the magnitude and phase angle of the resultant phasor significantly. Based on these considerations, the resistive load appears to offer the best compromise in affecting both voltage magnitude and phase angle of the electrical system to successfully measure changes in both magnitude and phase angle.

There are some additional concerns with using a capacitive load due to the potential for exciting resonances between capacitance and natural inductance present in the system. These transient over-voltages can sometimes result in voltage magnitudes twice that of system steady-state voltage. Over-voltage may cause measurement error due to A/D saturation, can pose threats to the test equipment as it is rated for 600 volts as well as for the system itself under certain conditions. Adjustable speed drives might also trip due to over-voltage transients, and the IADD needs to be able to conduct testing without disturbing a facility's loads. A paper discussing the application of a capacitive load to measure bolted arc flash potential entitled "Method for AC Powerline Impedance Measurement" has been presented in 2007 at the Pulp and Paper Industry Technical Conference. [12] The paper concludes that the device has performed well in prototype testing under laboratory controlled and field testing but that the device "is a single point measurement made under specific line conditions."

Conversely, a purely inductive load offers the least change in apparent load since the impedance angle observed at most points in an electrical power system are generally largely inductive. Providing load impedance that is significantly in phase with system impedance results in only incremental changes in phase shift. The importance of maximizing phase shift due to a step load change will be discussed in

Chapter Five, and maximizing the phase shift for measurement purposes and is preferred.

Any combination of resistance, inductance, and capacitance is possible, spanning the entire right half side of the impedance domain. This point is illustrated by the semi-circle surrounding the current fundamental phasor in Figure 4.2. These options were all considered. The resistive load is selected, because it provides a large step change in terms of impedance angle while simultaneously providing a stable load that is relatively transient free. While some transients are inherent due to stray capacitance between the plates of the resistor bank, the system is heavily damped, and transients are quick to dissipate below the noise level.

4.3. Voltage Measurement Circuitry

Voltage waveform information is obtained through the use of a custom designed optically isolated voltage measurement board. These probes are rated for 10 volts and they convert the input signal from a voltage to an optical (light) signal and back to a voltage signal. The input voltage signal is reduced by 180 times through the use of a resistive divider circuit.

Voltage can be measured in single and poly-phase systems as line-to-line, line-to-neutral, and in a three-phase system. The measurement board is configured to measure either in delta or wye through the user interface on the IADD terminal. Figure 3.4 illustrates the circuit board layout. The board also serves to drive the contactor coils used to dynamically configure the IADD test load during testing. Additional information about board functionality is included in Section 4.7.

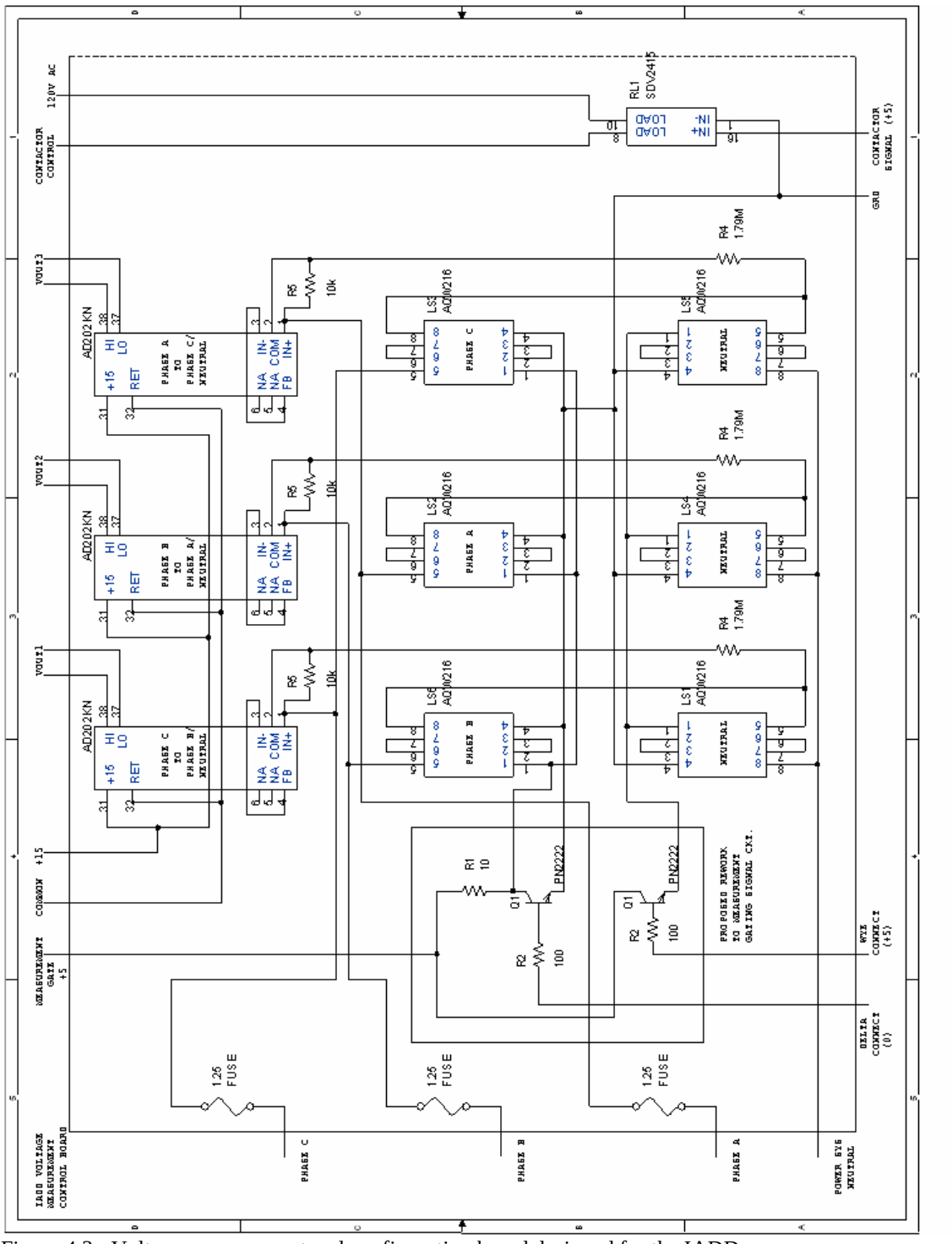

Figure 4.3. Voltage measurement and configuration board designed for the IADD.

Magnetic voltage transformers were initially tested for use with the device. In measurement applications, these are commonly referred to as potential transformers

(PT) because of the large turns ratios used when compared to typical power transformers. They also typically have very low power ratings.

Problems were encountered in using magnetic transformers to measure signals. Due to the small amount of current typically drawn in measurement signals, transformers are susceptible to operating in their non-linear region. When transformer secondary voltages were observed, they contained higher than expected amounts of third harmonic, and they appeared almost triangular in form. Initially, these waveforms were the result of transformer saturation or ferro-resonance under no load conditions. In an attempt to mitigate these non-linearities, five watt, 50 ohm resistors were placed on the secondary of the transformers to artificially load the transformers under test conditions. No noticeable change in wave shape is noticed with the addition of these resistors, so the neutral is added to the system. The waveforms were then observed to be typical of 60 Hertz (Hz) sinusoidal waveforms containing harmonic loads. This is illustrated in Figure 4.4b.

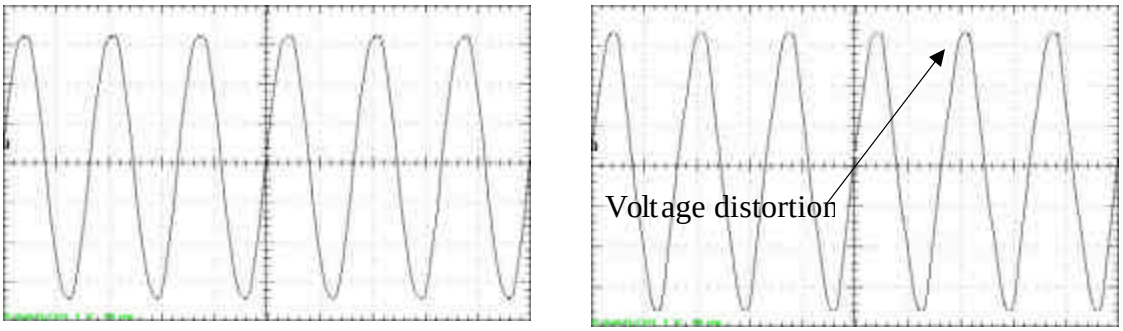

Figure 4.4. (a) Voltage waveform at test site with neutral connection (left) and (b) and without neutral connection (right), both scaled identically.

With no neutral connection (b), the observed voltage waveform is rich in 3rd harmonic content. Zero sequence voltage is typically seen in ungrounded systems or in systems with voltage imbalance where zero sequence current is present and where there

is no grounding point for this current to flow. Zero sequence components are analogous with triplen harmonics, which are harmonics that are multiples of three times the fundamental power frequency. These frequencies are particularly prevalent when non-linear switching power supplies are present on the power system.

Additionally, because the system is rated for up to 600 volts, there is the possibility of measurement saturation because of the turns ratio of the transformers selected. This results in a flat-topping effect of the voltage waveform. It is imperative to capture voltage waveforms as accurately as possible, because the change in RMS value is often very small. Since the data acquisition card can only resolve voltage signals up to 10 volts peak, a simple resistive voltage divider is placed on the secondary of the transformer. This divider serves two purposes: first, it serves as a steady state load on the transformer secondary, reducing transient effects often associated with unloaded transformers. Second, it provides further voltage division of the input signal such the output remains below the 10 volt limit, even at maximum input voltage levels.

Despite implementation of these mitigating techniques, the transformers continued to operate in the non-linear region and were particularly susceptible to saturation on three wire systems. Rather than continuing to increase the loading factor on the transformer's secondary, it had been decided to discontinue development with the transformers and use the optical isolators described initially. While much more expensive, these devices remain linear under all power configurations. The optical isolators were connected in exactly the configuration that the transformers were connected, and for all intent and purpose, perform the same function. Therefore, no change in programming is necessary.

4.4. Current Measurement Circuitry

Current measurements are made through the use of three externally powered Hall-effect current transformers (CT). A Hall-effect current sensor manufactured by Tamura Corporation of Temecula, California is chosen for this application. It is rated for a nominal current of 250 amps, 4 volt output; these were tested in the lab for linearity over the range of anticipated currents and the desired bandwidth. These tests were necessary to assure that readings from CTs are accurate in magnitude and phase. Tests show that the CTs perform well for currents greater than 10 amps, which is typical of current transformer performance. Tests also showed that the CTs have good frequency response at 60 Hz, with a -3 decibels (dB) frequency response at 10 kHz. Current transformers designed for both AC and DC signals measure transverse force on moving charge carriers. Typically referred to as the Hall Effect, it measures any variations in DC current. Specifications on this current transformer are included in Appendix C.

Hall Effect sensors require an external power supply to measure transverse forces. The CTs chosen require positive and negative 15 volts (DC) power to operate. The power requirements were satisfied by using a single 30 volts (DC) switching power supply that operates on 120 volts. Building a resistive divider creates a phantom neutral that is used as the reference on all CTs. A wiring diagram and pinout can be found in Appendix C of this paper.

4.5. Solid State Switching Relays

The Crydom HD60125-10 series solid state relay is chosen to serve as a controllable switching means for transferring load during the testing sequence. These

relays have a load current rating of 125 amps per device and are controlled by a 5 volt (DC) signal supplied by the DAQ card. There are several reasons this component is chosen. It is small in size, relatively inexpensive, and rated to handle currents in the range specified for testing. Additional rating information can be found in Appendix C of this thesis. This relay also has a random turn-on feature, making it ideal for this application. All three relays must turn on at the same point to minimize any transient reaction and provide a balanced load to all three phases whenever possible. The devices were paralleled, two per phase, to double the ampacity of the device. This step is necessary after testing had been conducted in a power substation where the high power rating of transformers made observing a measurable change in voltage with one triac device troublesome. The added capacity allows for greater latitude in measuring at high power locations. The IADD has the potential to be made modular based on the required test load and system stiffness by successively paralleling additional solid state switches and load banks to fit any application.

There are some advantages and disadvantages to using the solid state relay versus a traditional voltage controlled electromechanical solenoid-type contactor. During initial testing to determine device feasibility, a three phase voltage controlled contactor is used as the switching device for connecting the resistive load to the power system. The source of control is a variable transformer, supplying 120 volts to the control input of the relay. There has been some concern about contactor bounce and impedance across mechanical relays; however, these were secondary concerns because similar concerns apply to the solid state relay as well.

Solid state relays are found to be extremely reliable and uniform from an operational standpoint. In Figure 4.5, are waveform captures from the test system. The graph on the left measures the voltage across the relay and compares it with the current flowing through the relay. The graph on the right shows the control signal applied to the three relays and the resulting current flow through the test resistance when the switch operates.

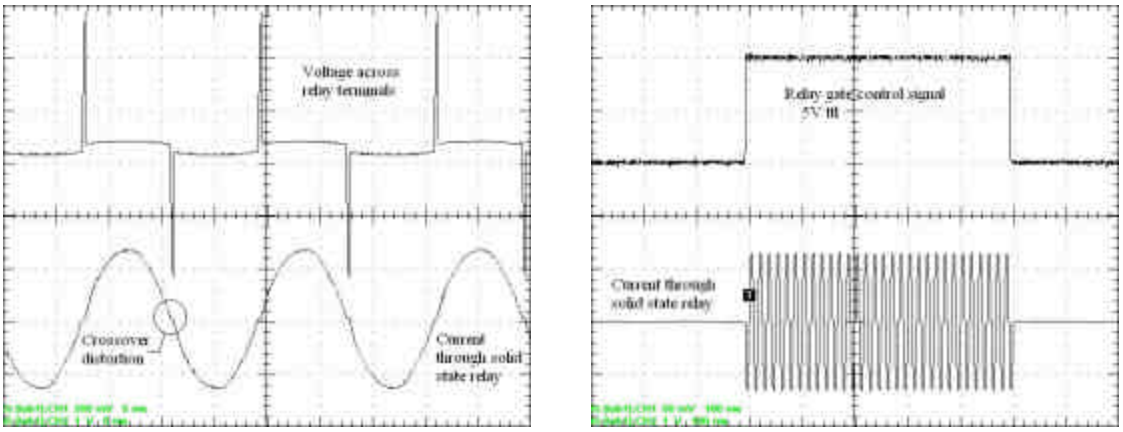

Figure 4.5. (a) Relay voltage drop during commutation (left) and (b) relay signal control (right)

In Figure 4.5a, the upper waveform depicts the voltage across the solid state relay. The sharp spikes seen in the waveform are indicative of commutation of SCRs during transition from one conduction path to the other. These solid state relays are constructed with two SCRs in an anti-parallel configuration such that each provides a conduction path dependent upon the direction of current flow at any given instant in time. The junctions that make up these devices have a minimum biasing voltage required to make them conduct. During the transient period between non-conduction and turn on, there is a brief moment where no current flows through either path of the SCRs. This results in a voltage drop across the relay seen in Figure 4.4a. Consequently, there is a corresponding distortion of the sinusoidal current waveform,

depicted in the lower waveform of Figure 4.5a. This phenomenon is commonly referred to as crossover distortion.

The voltage drop across the solid state relays represent a measurable impedance that would require compensation if voltage measurements were taken downstream of this device. By taking voltage measurements upstream of this device, it becomes part of the steady state load. Furthermore, because the voltage distortion is cyclic and consistent in magnitude from cycle to cycle, it does not skew phase angle measurement in a steady state condition. Based on these considerations, no need for additional compensation due to the effects of crossover distortion or gated voltage drop is required. The system is immune to these effects in this case.

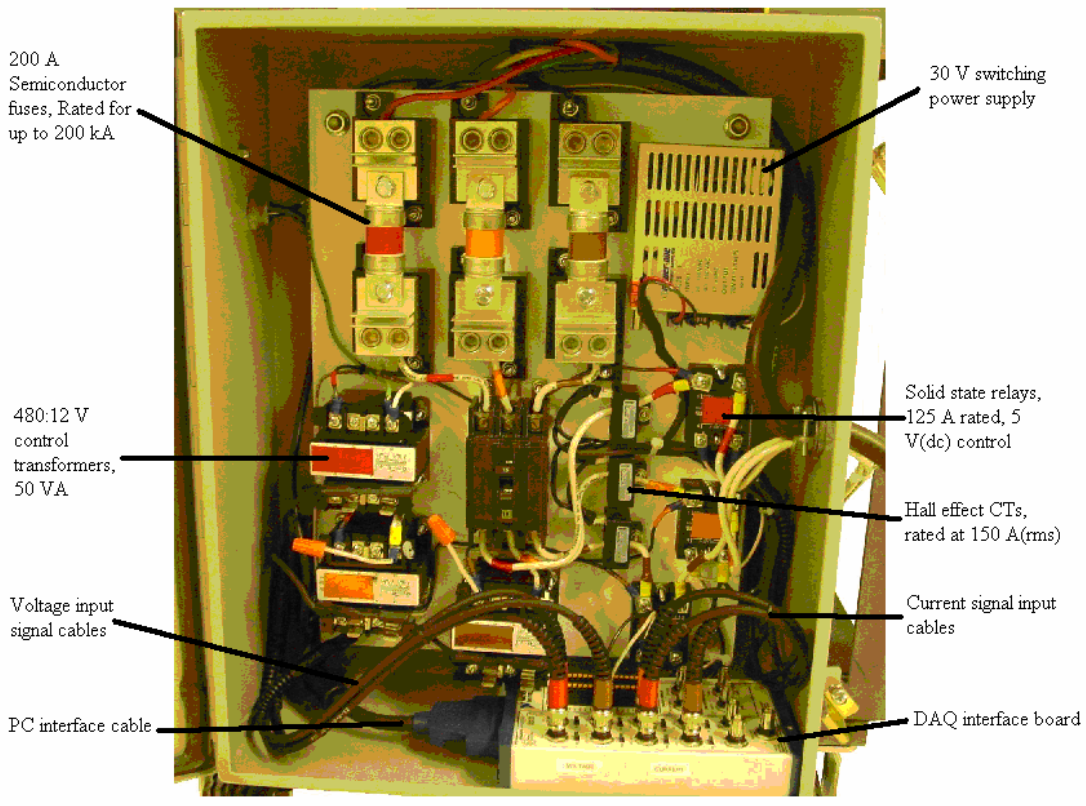

Figure 4.6. Control cabinets mounted to the IADD with voltage/current sensors and interface board.

4.6. Measurements and Acquisition

The National Instruments PCI-6123 data acquisition card is chosen to sample and capture data. This card is chosen based on a number of factors:

1. Final calculations are highly susceptible to phase shift, therefore simultaneous sampling is desired to minimize phase shift due multiplexing of voltage and current signals on different channels
2. 16-bit precision on sampled values versus 12 or 14 bit options increases the accuracy of readings by a factor of 4 to 16 times
3. Sampling frequency is sufficiently high to capture all spectral data of interest and further minimize error due to phase shift and quantization error

This card offers eight analog differential inputs. Six inputs are currently being used in the design to capture voltages and current waveforms on all three phases. Future development may include observation of neutral and ground currents on the remaining analog inputs. Figure 4.7 depicts images of the data acquisition components. The DAQ card is to the left, which includes the eight independent A/D converters, amplifiers, and memory modules. The BNC connection port is to the right, which takes analog signals from shielded coaxial cables to the proprietary National Instruments data cable that interfaces with the DAQ card. Coaxial cables and BNC connectors were chosen because they perform well in electrically noisy environments. Electromagnetic fields that typically couple to signal wires are shielded, which is a feature that is necessary due to the large current and voltage levels present in the proximity of the measurement devices.

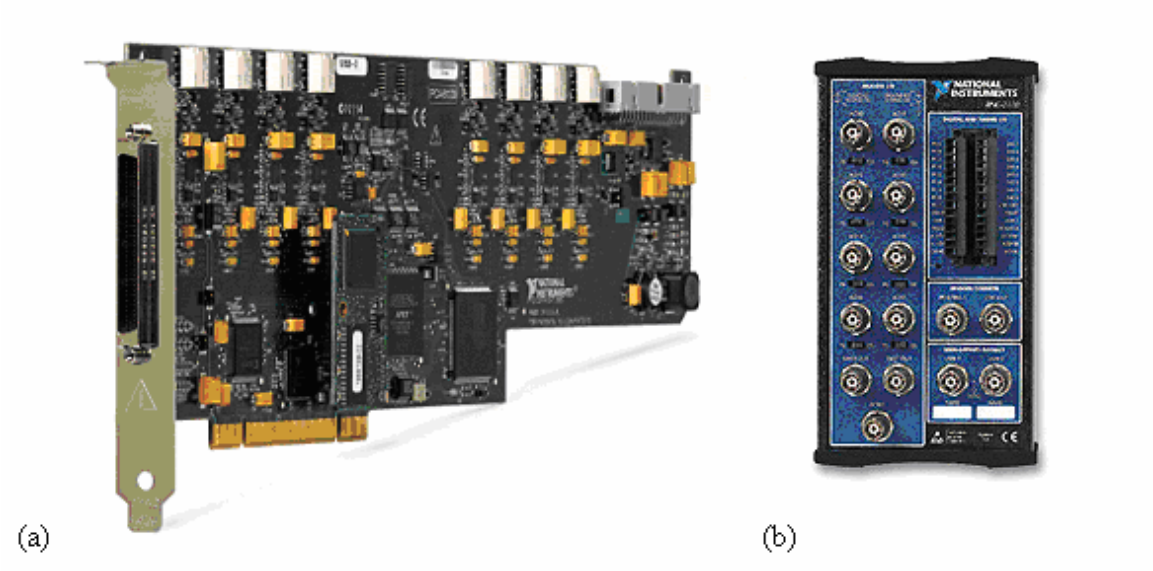

Figure 4.7. (a) NI PCI-6123 DAQ and (b) NI BNC-2110.

4.7. Resistor Dynamic Configuration Modes

The resistor bank has been segregated into two effective load banks by creating a neutral at the center tap of each phase of the resistor bank. Several modes of operation have been developed to more easily discuss the different configurations implemented in the IADD defined in Figure 4.8.

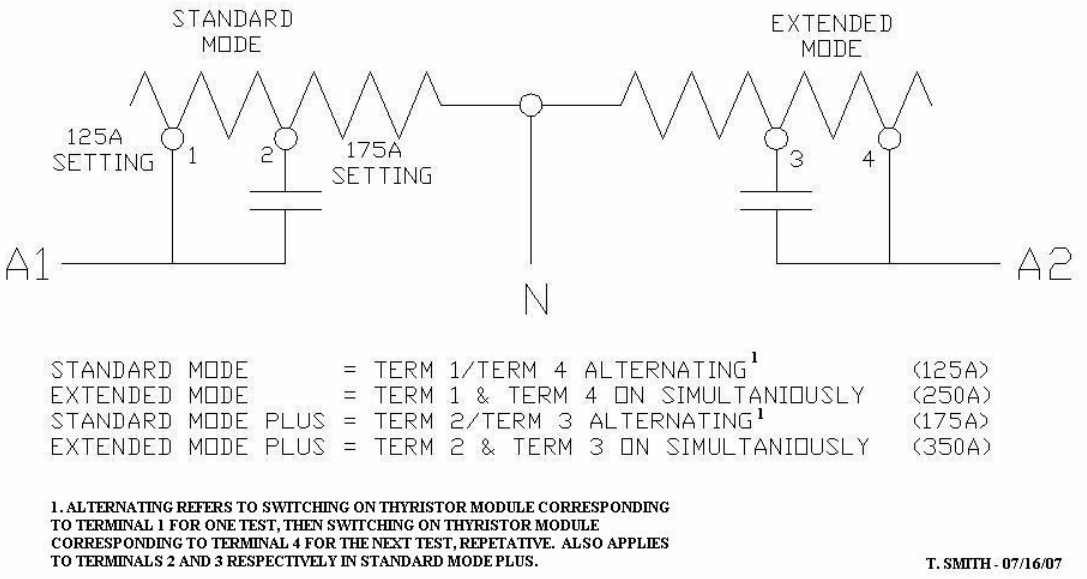

Figure 4.8. Resistor bank relay diagram.

Standard mode uses one half of the resistor bank as a load resistor to draw current. As note one of Figure 4.8 indicates, when the IADD is operating in Standard mode or Standard Mode PLUS, relays are cycled to more evenly distribute heat between all available relays. For example, under Standard Mode operation, relay gate one is triggered for test one. On the subsequent test two, relay gate four is triggered. When the IADD is used in Extended Mode or Extended Mode PLUS, both sides of the resistive load bank are energized and current flow is approximately doubled.

Additionally, the IADD has the option to be operated in Standard Mode PLUS and Extended Mode PLUS. Caution should be used when operating the IADD in PLUS mode, because the solid state relays are being used above their steady state rating (up to fifty percent). When operating the IADD in PLUS mode, it is suggested that cycle time between subsequent tests be increased to allow time for the solid-state relay's semiconductor material to cool properly prior to additional test runs. The suggested cycle time for Standard or Extended Mode is one test every thirty seconds. The suggested cycle time for PLUS mode is one test every sixty seconds. Testing to optimize time between testing has not been completed. These suggestions are based on empirical testing and experience working with the IADD.

Three-pole shorting contactors are used during PLUS mode to increase the IADD test load. The contactors are produced by Telemecanique of Rueil-Malmaison France and have a resistive load rating of 50 amps continuous duty. However, they are used to carry current up to 175 amps for the short duty cycle used during testing. The 120 volt contactor coils are user controlled (see Section 5.1.1) by digital output on the

DAQ card (see Section 4.3) through optically isolated gate drivers to supply power to the contactor coils.

Measurements taken on a delta configured system can be problematic when considering that the reference neutral is undefined and may be inadvertently grounded in some cases. This topic is discussed in detail in Chapter Eight where an analysis of the effect of neutral shift is investigated. To reduce the error introduced in measuring an ungrounded or delta connected system a method of dynamically switching between a wye and delta measurement configuration allows the IADD to be configured for either measurement instantaneously. In Figure 4.3, a measurement circuit is presented that, when gated using two of the digital logic outputs provided on the DAQ board, will automate the process of measuring the load voltage in either a delta or wye configuration.

Because the IADD measures only differential phase shift in each phase on the input voltage, no significant changes to programming is required. One noted exception is scaling of the input voltage to determine the phase voltage during post processing. The incident energy calculations require phase voltage, rather than line-to-line voltage in order to properly calculate the arc flash incident energy. As mentioned, differential phase shift is measured so no further changes will be required with respect to calculation of the X/R ratio. The differential in phase shift remains constant between phases when a load current is applied, regardless of measurement in delta or wye.

CHAPTER 5

FRONT PANEL SOFTWARE DEVELOPMENT

Chapter Five further develops key concepts of the IADD by introducing the reader to the graphical user interface (GUI) developed for this device allowing the user to easily begin working with and gathering data through the IADD. Development of software for the IADD is accomplished by using National Instruments' LabView software. In conjunction with the DAQ, signals are processed and analyzed to determine the bolted fault current at the buss of interest. Several program screens are developed to accomplish this task and are discussed in sequence. A detailed description of the IADD GUI and its many functions are presented.

The PC used on the IADD is custom built on site at Clemson to be able to handle large amounts of incoming data efficiently while still having enough processor power to send control signals to switching elements at the proper time. The computer is comprised of a 3.2 GHz duel-core Intel™ processor and has a data bus speed of 800 MHz. The IADD first operated using a 1.0 GHz Intel™ processor but had been prone to software problems due to data underwriting. The program uses software based timers to create control signals that gate the solid state relays and periodically, the program would "freeze", resulting in longer than expected gating of the thyristors. The improvement in computing resources results in a much more stable software environment that is not prone to these problems.

The front panel refers to the GUI that users see and interact with when the application is running. The screens described in the proceeding sections were developed to present the user with as much information during testing as possible.

5.1. Incident Energy

Figure 5.1 shows a screen capture of the front panel GUI used in the IADD system. The main panel that opens when the program is executed features a large number, centrally located, that represents the NFPA arc flash hazard rating category previously discussed in Chapter One. This number is based on the cal/cm^2 criteria presented in Table 1.1. The incident energy exposure in cal/cm^2 is given in the upper right hand corner, and a graphic representation of this data with respect to category level is given in the vertical meter on the right hand side.

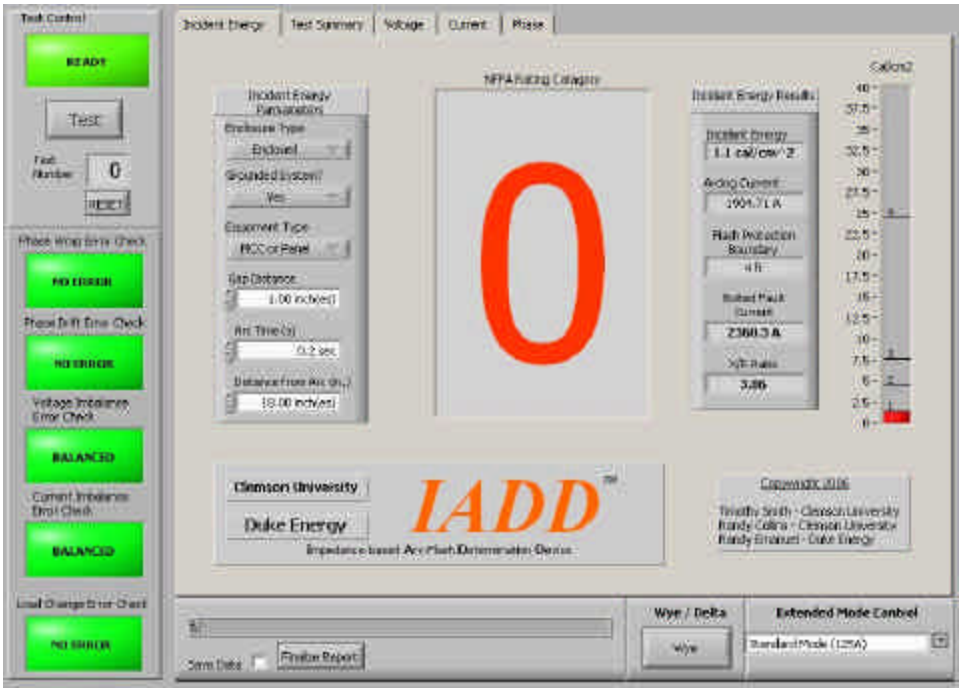

Figure 5.1. Incident energy report screen.

By using the equations developed in IEEE 1584 (see Chapter Six), the category rating is calculated based on bolted fault current and several other variables. These user selectable variables are listed under the "Incident Energy Parameters" menu to the left of the arc flash hazard rating. Changing any of these values will instantly change the calculated incident energy and may change the rating category.

"Enclosure Type" is a variable used in the incident energy calculations as shown in Figure 5.1. The user can select either an enclosed or non-enclosed panel configuration. Enclosed panels can reflect energy off of interior surfaces and increase exposure to radiating energy.

"Grounded System" is a yes or no variable used in arcing current calculations to categorize the system connection type as shown in Figure 5.1. Grounded electrical systems are known to have reduced the fault current due to ground resistance and ground fault protection schemes.

"Equipment Type" is a variable used to categorize the type of system being tested as shown in Figure 5.1. Certain types of equipment are more robustly constructed and provide lower fault resistance, such as MCCs when compared to an arc occurring in a cable.

"Gap Distance" is user specified in inches based on the distance between conductors with potential to arc as shown in Figure 5.1. The arcing distance has a small effect on both arcing current and the amount of energy radiated during an arcing event.

"Arc Time" is user specified in seconds based on the type of protection present upstream of the test location as shown in Figure 5.1. As discussed, protection plays a key role in reducing energy exposure levels by reducing arcing time.

"Distance from Arc" is user specified in inches based on the type of equipment, voltage level, and standard practices used at a test location as shown in Figure 5.1. For example, closer working distances are expected at voltage levels below 600 volts when compared to voltages of 4.16 kV.

The selection button in the lower left-hand corner of the screen is user selectable and determines if the IADD will operate in one of the four selectable resistor bank configurations discussed in Section 4.7.

5.1.1 Front Panel Test Control and Data Capture

To the left of the main page are the "Test Control" and "Error Codes" dialog boxes. These are always visible while the program is running and allows the user to initiate a test at any time. The large button labeled "Test" initiates the IADD program, and a test is immediately performed. A numeric indicator below the test button indicates the test sequence number and serves as a marker for tracking data. The test counter can be reset to zero by pressing the reset button below the test count indicator. Also, the test value is automatically reset every time the program is terminated or reinitialized. As shown in Figure 5.1, the test status indicator is green and displays "Ready" indicating that the system is ready to test the connected buss. The indicator will turn yellow and display the message, "Test in Progress," while the IADD is performing a test and making result calculations. A test typically takes about three seconds to complete.

The "Error Codes" dialog box is displayed below the "Test Control" box previously discussed. This dialog allows the user to determine the validity of the most recent test. The "Phase Wrap Error Check" determines if an error has occurred due to phase wrap phenomenon. This error is discussed in Chapter Six of this thesis, as is the "Phase Drift Error Check". If significant voltage or current imbalance is observed during a test sequence, the appropriate indicator will change to red, and the message "Voltage Imbalance" or "Check Connection" will be displayed based on the type of error detected. Voltage imbalance errors are triggered by the voltage imbalance calculation that is discussed in Chapter Six. In the case of current imbalance in the presence of balanced phase voltage, the connections and load taps should be examined and confirmed prior to additional testing. The relay gating control wires and connections should also be examined if current imbalance is detected.

Capturing data is accomplished through the dialog box at the bottom of the screen. To save test data, the user must check the box next to "Save Data." After the first test is complete, the user will be prompted to save the file in a specified file location. Once this location is established, the data capture process is automated. When all tests in a series have been completed, the user has the option to finalize testing. Finalizing the test will append all the selected incident energy parameters to the data file for later reference. After finalizing the test series, the user is then prompted to start a new test or end the session.

5.2. Test Results

The "Test Summary" page gives numerical information about the last test conducted. The tab, "Test Overview / Per Unit," is displayed in Figure 5.2. Additional test information is provided in the "Test Results – Detail" tab in Figure 5.3 and the "Phase Array / Compensation" tab in Figure 5.4.

5.2.1. Test Results - Test Overview / Per Unit

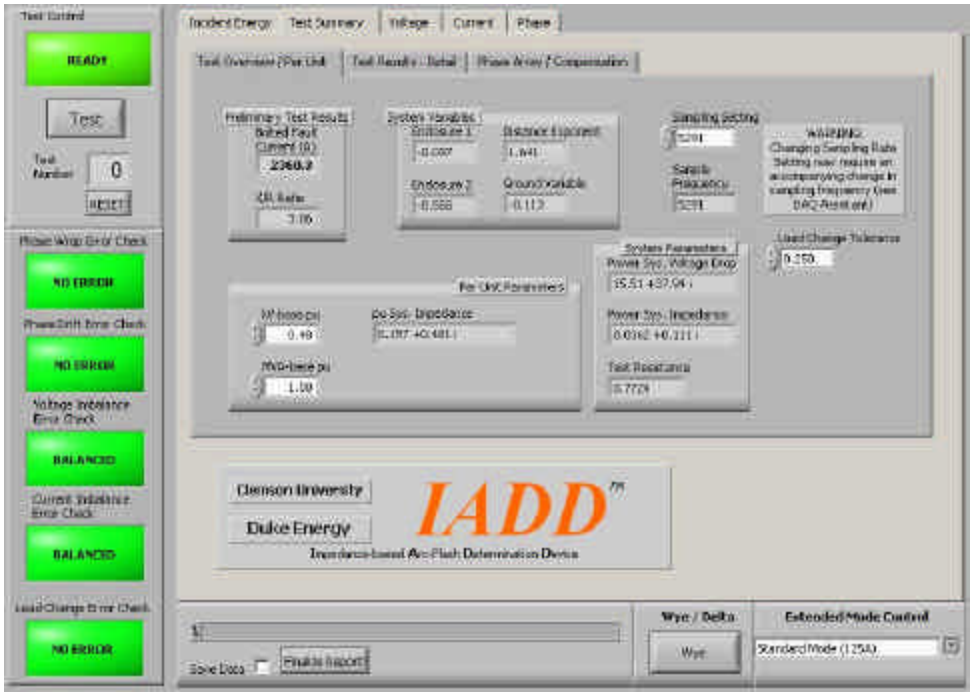

Figure 5.2. Test summary overview and per unit setting.

The "Preliminary Test Results" box contains two numeric indicators that present intermediate results of the most recent test. This is displayed on the "Incident Energy" tab. These indicators display estimated bolted fault current in amps and reactance-resistance ratio (X/R ratio) of the system's Thevenin impedance. Calculations and algorithms used in calculating these values are discussed in detail in the forthcoming subsection.

In the lower left-hand corner of the page titled "Per Unit Parameters," additional calculations are incorporated to determine the per-unit system impedance based on user input values. To obtain these values, the user must manually enter the system per-unit voltage base (V_{base}) and per-unit power base (S_{base}).

In the lower center of this screen is an additional informational box titled "System Parameters." This box provides data about measured system parameters used in calculating intermediate results, which are bolted fault current and X/R ratio.

The "Power System Voltage Drop" is a complex numeric value that estimates the voltage drop in the power system due to the change in loading conditions. This value is derived from measured values of voltage drop across a known load and observed phase shift of the voltage fundamental.

The "Power System Impedance" is a complex numeric value that estimates the power system impedance in terms of resistance and reactance on a 60 Hz base. This value is used to compute the bolted fault current that is possible at the test site.

The "Test Resistance" gives information on the resistance calculated by taking a ratio of averaged load voltage to averaged load current during the test. This value should remain relatively constant since the load is resistive. However, some variation may be observed due to heating of the resistor coils, and it is a function of the duration and frequency of testing.

Some compensation is provided to these values based on the lead wire used to connect the test buss to the IADD. Additional information on definition and application of this correction factor is found in Section 5.2.3.

Throughout this chapter, two operational modes or time periods will be commonly referred to throughout this chapter. The Pre-Test Mode is the time period prior to switching of the resistive load bank into the circuit. The In-Test Mode is the time period in which current is flowing through the load bank. Refer to Figures 6.4 and 6.5 for a graphic representation as it applies to measured voltage and current waveforms.

5.2.2. Test Results - Test Results - Details

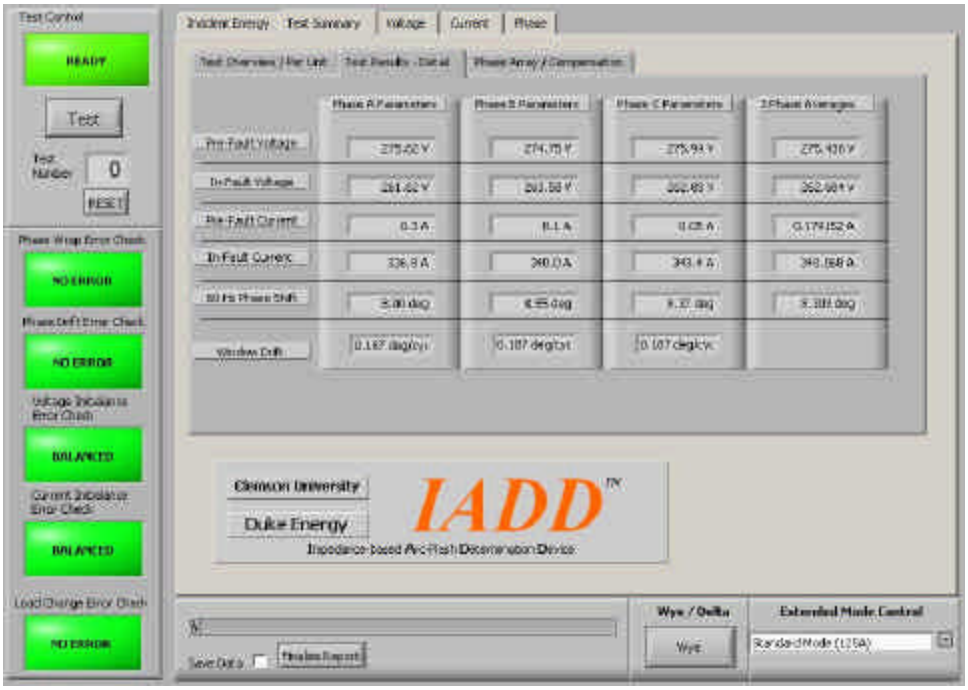

Figure 5.3. Test summary detailed data log.

The “Test Results – Details” tab displays all measured values taken from each phase of the system, and it is depicted in Figure 5.3. The three phase values are averaged, and the calculated average value is shown in the fourth column of the display. Several frequency based measurements are made on the incoming voltage

waveforms. These are explained in detail, and the significance of these measurements is made apparent in the following sections.

The "Pre-Test Voltage" parameter measures and displays the three phase voltages prior to switching in the resistive load bank. The RMS measurement is made over approximately thirty cycles just before switching in the load in an attempt to mitigate load switching as a source of error during a test sequence. The three phases are then averaged and displayed in the first row, of the fourth column in Figure 5.3.

The "In-Test Voltage" parameter measures and displays the three phase voltages after switching in the resistive load bank. The RMS measurement is made over approximately twenty-one cycles after switching, again, to mitigate load switching as a source of error during a test sequence. The three phases are then averaged and displayed in the second row, of the fourth column in Figure 5.3.

The "Pre-Test Current" parameter is displayed for test validation purposes and is measured over the same time interval as the "Pre-Test Voltage" parameter. These values should always be approximately zero. Although, some variation, less than 0.5 amps, is often observed due to noise inherent in the system and to a large gain factor used in signal processing.

The "In-Test Current" parameter measures and displays the three phase currents after switching in the resistive load bank. The RMS measurement is made over the same time interval as the "In-Test Voltage" parameter. The three phases are then averaged and displayed in the fourth row, of the fourth column in Figure 5.3.

The "60 Hz Phase Shift" parameter is a measure of the change in phase shift based on calculations including Window Drift compensation shown in Figure 5.3. Accurate phase shift detection is extremely critical in estimating system parameters, particularly X/R ratio. The method and means of compensation are discussed in detail in Chapter Seven.

The "Window Drift" parameter displays the estimated shift in voltage from the reference phase angle due to sampling frequency imposed during test conditions. The optimal sampling frequency is determined b applying guidelines from National Instruments related to sampling. The sampling frequency is optimized by conducting an analysis presented in Section 7.1.2. This results in a sampling frequency that most closely coincides with the 60 Hz fundamental frequency to be measured. The system is not synchronized with the power system frequency. Sampling frequency is generated by a voltage controlled oscillator, and frequency drift may vary with changes in ambient temperature inside of the computer chassis. The "Phase Drift Error Check" indicator light alerts the user if phase drift exceeds one degree per cycle.

5.2.3. Test Results – Phase Array / Compensation

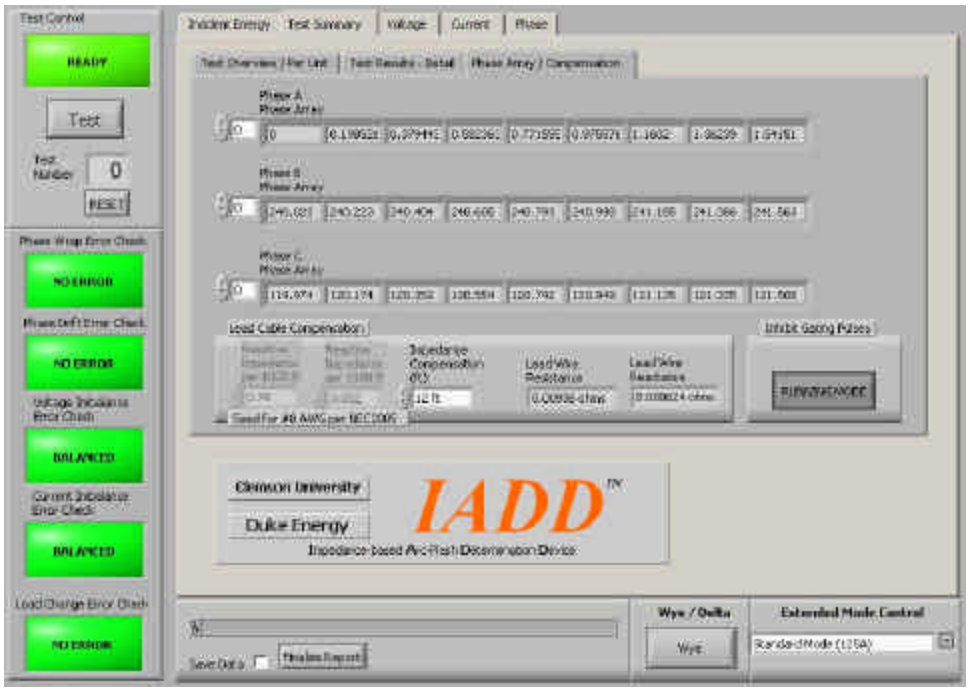

Figure 5.4. Phase Array and Compensation Page.

Depicted in Figure 5.4, the "Phase Array / Compensation" tab displays information about phase angle changes on a cycle by cycle basis, which allows the user to compensate for wire lead impedance that may otherwise skew final bolted fault current calculations.

The three arrays that are displayed on this tab give information on phase angle as produced by the FFT calculations used to track phase shift. Each number represents a fundamental phase angle unique to each cycle of the phase voltage waveform for each phase measured during the entire duration of the test. Ideally, the value should not vary under steady state conditions from cycle to cycle except when there is a change in the system, such as the moment that the resistive load bank is switched into the circuit. However, due to slight differences in sampling frequency with respect to the 60 Hz

input waveform, there is some drift noted from cycle to cycle. The program has been optimized with respect to sampling frequency to minimize the amount of variation. Additional compensation is made as part of the window drift parameter previously discussed in Section 5.2.2.

Compensation for connection cable length has been implemented for additional impedance of the lead wires that would not be present should a fault occur at the point of connection. The user can select the length of the wire connection. A calculation is made based on the expected additional impedance input to the system as a result of the specified wire length. Additional compensation is made internally for the line-side fuses used to protect the system and is not a user defined variable. Additional details concerning lead length compensation are found in Chapter Six.

5.3. Voltage

The "Voltage" page gives graphical information about the last test conducted. The "Overview" tab is displayed in Figure 5.5, and additional test information is provided in "Gate On" tab in Figure 5.6a and "Commutation OFF" tab in Figure 5.6b.

5.3.1. Voltage – Overview

Shown in Figure 5.5, the "Voltage – Overview" tab displays detailed Pre-Test and In-Test voltage waveforms, approximately three cycles each, in the two smaller waveform graphs at the bottom. The top graph shows the total observed waveform for the duration of the test. This is useful in quickly evaluating the validity of test results since the user can view voltage waveforms to verify that no unexpected transient

condition is present during the test. To the left of the detailed Pre-Test and In-Test graphs are RMS calculations and approximate voltage imbalance.

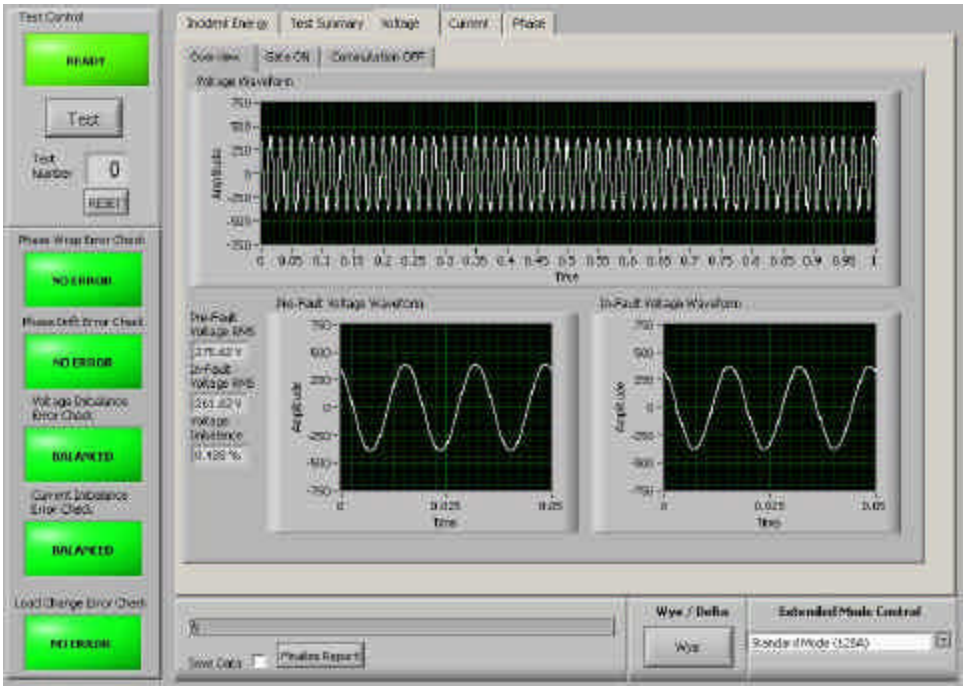

Figure 5.5. Voltage waveform overview visual display.

Because the system measures voltage on a per phase basis, the voltage imbalance equation has been modified from the standard accepted National Electric Manufacturers Association (NEMA) voltage imbalance equation. The calculation assumes that phase voltages are reasonably balanced, and the following formula is applied:

$$V_{\text{Imbalance}} = \frac{(V_{q-MAX} - V_{3q-Average})}{V_{3q-Average}} \tag{5.1}$$

Care should be taken when applying this equation as it assumes that phase-to-phase voltages are reasonably balanced. Therefore, this equation is valid. The reported voltage imbalance should not be used as a power quality measurement, because the

equation to calculate imbalance does not conform to the standard NEMA calculation for voltage imbalance. Application of the IADD under extreme voltage imbalance is a topic for future development.

5.3.2. Voltage – Gate ON

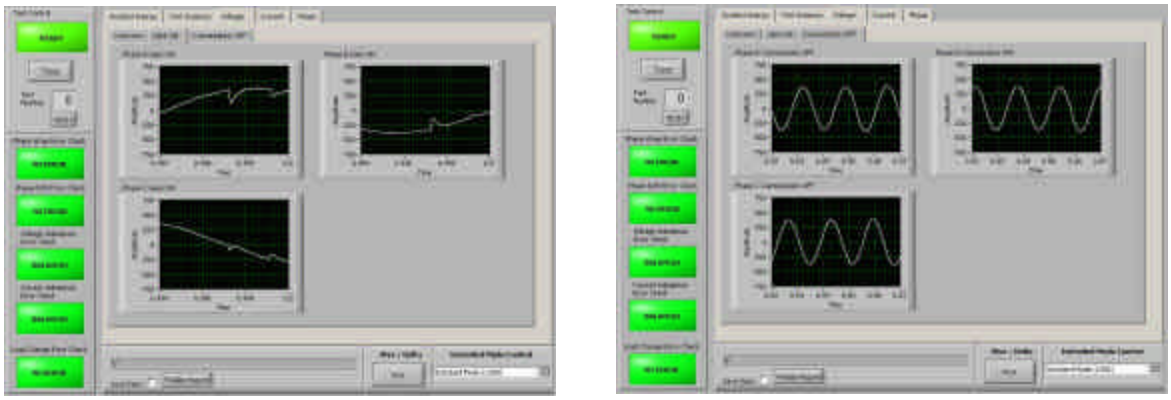

Figure 5.6. (a) Gate on voltage waveform detailed view and (b) Commutation off voltage waveform detailed view.

The "Voltage – Gate ON" tab displays the three phase voltage waveforms at the moment of switching, shown in Figure 5.6a. No calculations are associated with this tab, and the waveforms are presented for information purposes only.

5.3.3. Voltage – Commutation OFF

The "Voltage – Commutation OFF" tab displays the three phase voltage waveforms at the moment of switching, shown in Figure 5.6b. No calculations are associated with this tab, and the waveforms are presented for information purposes only.

5.4. Current

The "Current" page gives graphical information about the last test conducted. The "Overview" tab is displayed in Figure 5.7, and additional test information is provided in "Gate On" tab in Figure 5.8a and "Commutation OFF" tab in Figure 5.8b.

5.4.1. Current – Overview

Shown in Figure 5.7, the "Current – Overview" tab displays detailed Pre-Test and In-Test current waveforms, approximately three cycles each, in the two smaller waveform graphs at the bottom. The top graph shows the total observed waveform for the duration of the test. This graph is useful in quickly evaluating the validity of test results, since the user can view current waveforms to verify that no unexpected switching transients occurred during the test. As shown in Figure 5.7, the Pre-Test and In-Test RMS current calculations are presented, and approximate current imbalance is calculated using the same method presented in Equation 5.1.

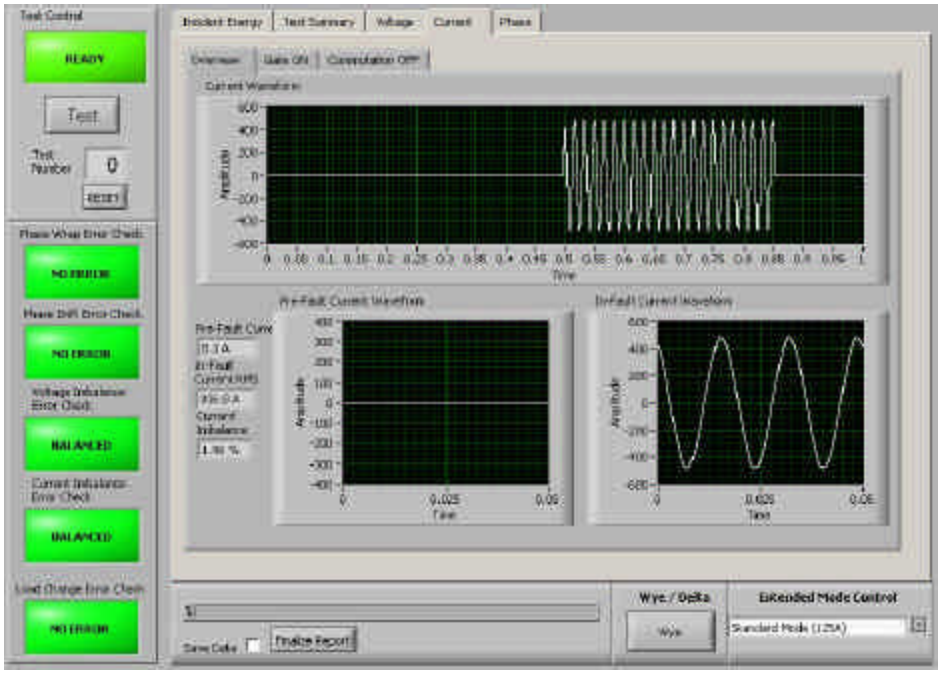

Figure 5.7. Current waveform overview visual display.

5.4.2. Current – Gate ON

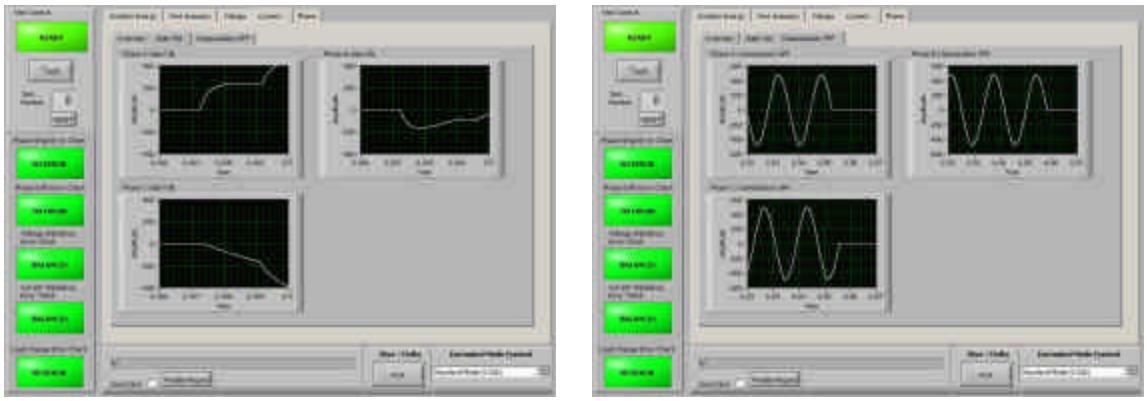

Figure 5.8. (a) Gate on current waveform detailed view and (b) Commutation off current waveform detailed view.

The "Current – Gate ON" tab displays the three line current waveforms at the moment of switching, shown in Figure 5.8a. No calculations are associated with this tab, and the waveforms are presented for information purposes only.

5.4.3. Current – Commutation OFF

Shown in Figure 5.8b, the "Current – Commutation OFF" tab displays the three line current waveforms at the moment of commutation. No calculations are associated with this tab, and the waveforms are presented for information purposes only. These views each span several cycles of data, because commutation occurs naturally at a zero crossing and can vary between two cycles depending on point in wave when the gating signal is removed from the relays. This has an effect on the phase angle during switching that is discussed in the following section.

5.5. Phase

The "Phase" page gives graphical information about the last test conducted. The "Overview" tab is displayed in Figure 5.9, and additional test information is provided in the "Details" tab displayed in Figure 5.10.

5.5.1. Phase – Overview

Shown in Figure 5.9, the "Phase – Overview" tab displays a view of phase angles for each power phase on a cycle by cycle basis. Because the FFT algorithm produces only one phase data point at the fundamental per cycle, this graph is made of discrete points representing the values discussed in Section 5.2.3. As expected, a phase shift occurs at the point when the load is connected to the system, and an identical shift in the opposite direction is observed when the load is disconnected.

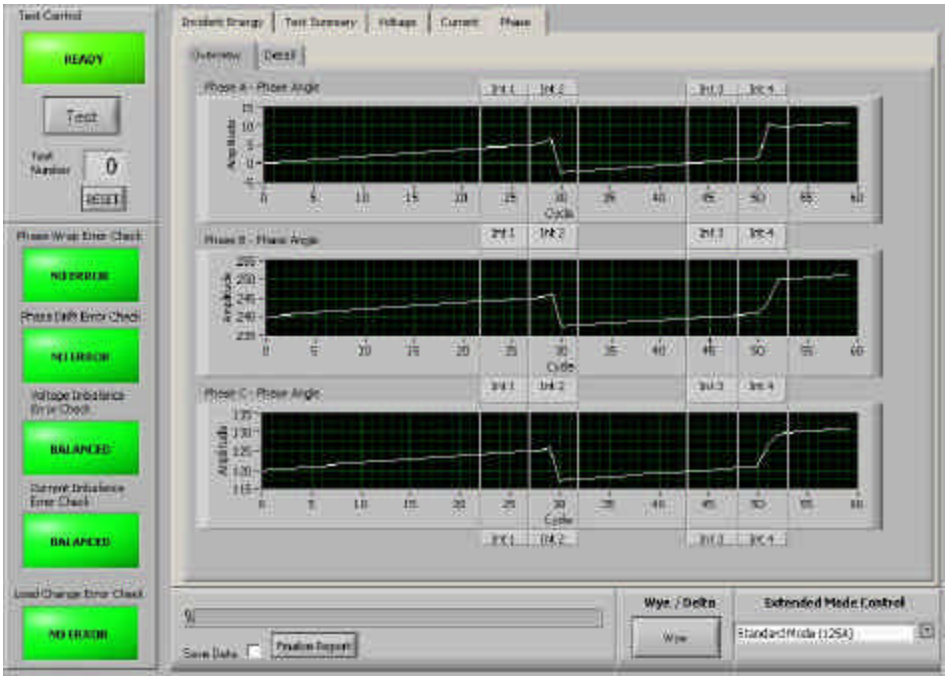

Figure 5.9. Phase angle visual overview.

Measurements to determine phase angle shift are split into four sections and are discuss in greater detail in Chapter Seven of this thesis.

5.5.2. Phase – Details

The "Phase – Details" tab shows more clearly how phase angle is affected due to load switching at the test point, shown in Figure 5.10. The window drift is apparent and manifests itself in the form of a slope in the phase angle from point to point that remains constant for the entire length of the test. Compensation is made for this known error and discussed in more detail in Chapter Seven of this thesis.

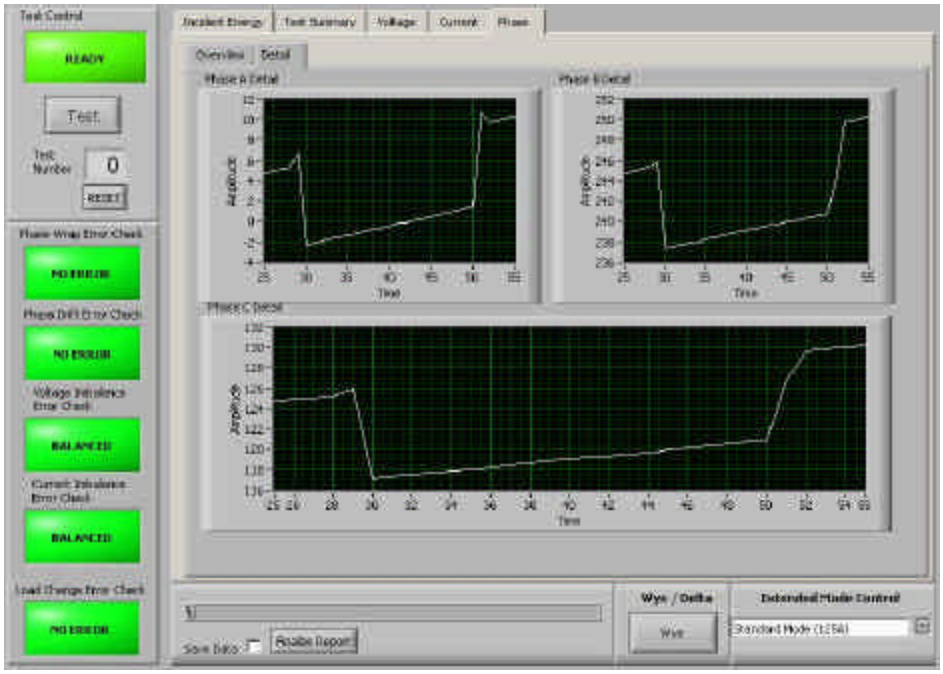

Figure 5.10. Phase angle visual detailed view.

An additional variation in the phase angle can been seen when the resistive load is disconnected from the source. This variation is due to commutation of the current wave at the zero crossing in each line of the current waveform. One solid state relay will always commutate off prior to the other two, which results in a single phase circuit. Current continues to flow through the two remaining conduction paths until these also

commutate off. This transient condition manifests itself as a larger than expected change in phase angle during the cycle when the single phase condition exists. As shown in Figure 5.9, the phase returns to its steady state pre-test condition after the remaining conduction paths have commutated off, and the load is fully disconnected from the source.

CHAPTER 6

BACK PANEL SOFTWARE DEVELOPMENT

Chapter Six presents calculations used to determine power system impedance, bolted arc fault current, and incident energy. These calculations are paramount to the operation of the IADD, and the results are ultimately applied to assigning an NFPA arc flash category to the electrical node connected to the IADD.

6.1. Measurement of Voltage and Current Variables used in Calculations

As part of the LabView software, the DAQmx™ Assistant allows the user to easily configure an NI DAQ (data acquisition) card to input and output digital and analog signals. This module is used to capture voltages and currents during the testing sequence. This module also outputs control signals to relays using internal computer power. Upon initialization, the IADD is configured to obtain a predetermined number of samples at a user specified sampling rate. Once measured data has been placed into an array, then mathematic operations can be applied to the acquired input signals for post processing.

For this application, a test sequence is divided into separate and independent acquisitions. During the first portion of the test, voltage and current are measured on a three phase basis to obtain baseline RMS values. Voltage and current RMS calculations are performed on each phase of the system using analysis tools that accompany the National Instruments software. The card samples with 14-bit accuracy; therefore, there is some quantization error associated with the RMS measurements.

This percent error is a function of the voltage and current magnitude being measured. The bits are distributed evenly over the range zero to ten volts. A 120 volt signal has a maximum quantization error of 0.04%, and a 330 volts (575 volts line to line) signal has a maximum quantization error of 0.01%. The IADD is constructed for 600 volts maximum.

In an attempt to further reduce error, the RMS values of each phase are averaged in the standard method, and the average three phase RMS value is used in final calculations. During the first capture portion of testing, no current flows in the test circuit, therefore, there is no phase shift due to the testing that occurs. See Figure 6.5 for a visual representation and an example current waveform capture.

Relay timing is accomplished through software code and software based timers as implemented in Figure 6.1. The function block on the right side of the figure counts thirty milliseconds. Then, the gating signals are sent to the relay circuit. Gating signals are released by counting in a similar fashion shown in the left block.

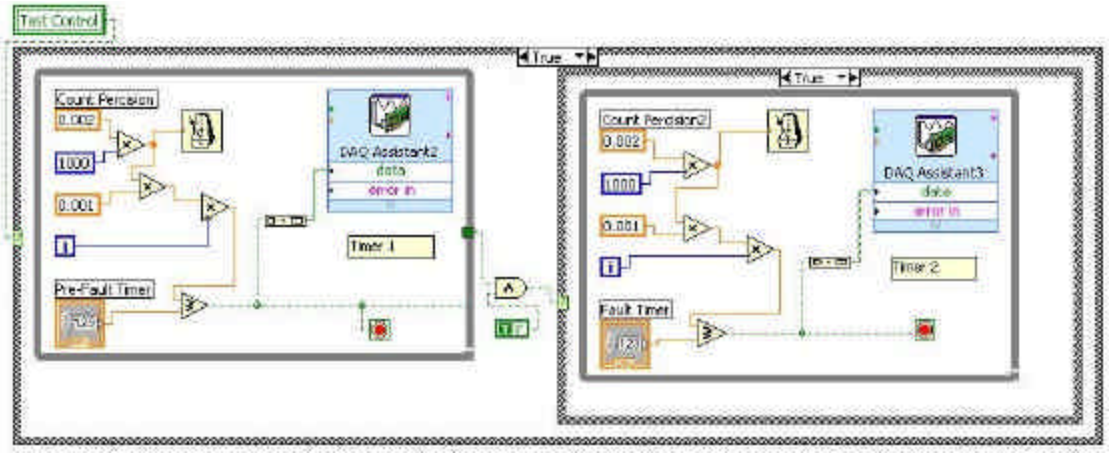

Figure 6.1. Implementation of relay control timers algorithm.

The second capture is taken immediately after the first. Upon completion of the baseline voltage and current measurements, the control gate signals are sent to three solid state relays to close the test circuit as discussed previously. Additional sets of solid state relays may be paralleled with the first three relays to increase the capabilities of the IADD. Measurements are then taken on the three phase voltages and currents in a similar fashion as is discussed previously. The RMS values are obtained for all three phases, and an average of the three voltage and current waveforms is taken respectively. A determination of the measured change in voltage is taken by subtracting the post-switching voltage ($V_{In\text{-}Test}$) from the pre-switching voltage ($V_{Pre\text{-}Test}$). This value is used in further calculations to be discussed.

Additional details on capturing data are presented in Chapter Seven as they apply in determining phase angle shift and measurement of X/R ratio. For simplicity, it is assumed throughout the rest of this chapter that the Average 60 Hz Phase Shift variable has been calculated.

6.2. Calculations on Measured Data

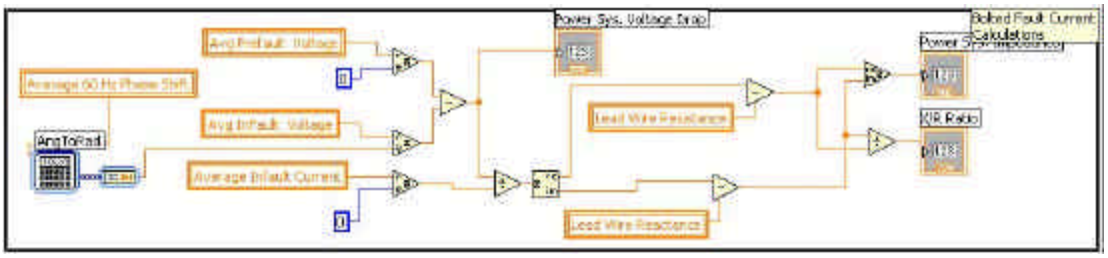

Figure 6.2. Implementation of calculations leading to determination of bolted fault duty.

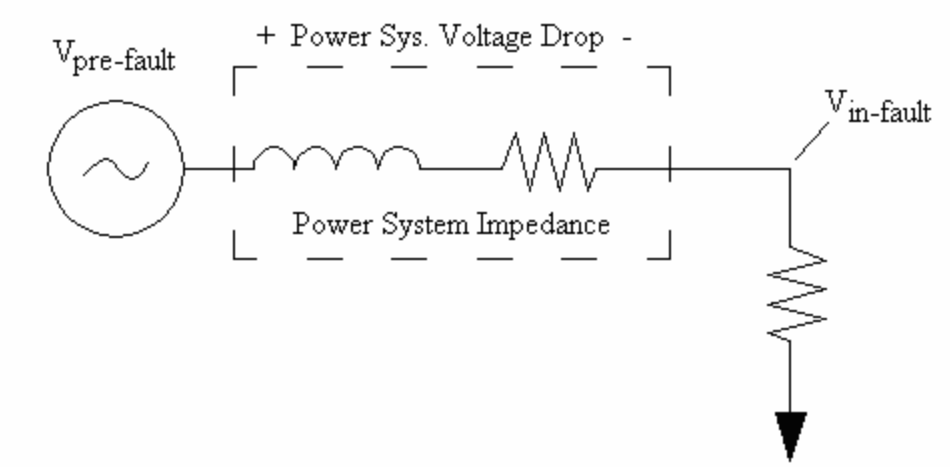

Figure 6.3. Diagram illustrating block diagram implementation in figure 6.2.

The IADD must ultimately calculate the power system impedance to determine bolted fault current, arc flash incident energy, and X/R ratio. This is completed by solving Equation 6.1 and results from nodal analysis of the circuit presented in Figure 6.3:

$$Z_{\text{Power System}} = \frac{\overline{V}_{\text{Pre-Test}} \angle 0^0 - \overline{V}_{In-Test} \angle \overline{q}_{PhaseShift}}{I_{In-Test} \angle \overline{q}_{PhaseShift}} \tag{6.1}$$

$Z_{\text{Power System}}$ is a complex number comprised of a real (resistive) component, $R_{\text{Power System}}$, and an imaginary (reactive) component, $X_{\text{Power System}}$, such that:

$$Z_{\text{Power System}} = R_{\text{Power System}} + jX_{\text{Power System}} \tag{6.2}$$

Therefore, the following values must be obtained: $\left|\overline{V}_{\text{Pre-Test}}\right|, \left|\overline{V}_{In-Test}\right|, \left|\overline{I}_{In-Test}\right|$ and $\left|\overline{q}_{PhaseShift}\right|$.

The IADD performed two separate calculations simultaneously to find these variables. One algorithm is used to determine voltage and current magnitudes, and the other is used to define phase angle. Furthermore, the phase angle algorithm is sub-

divided into two parts. These parts form the phase angle data into a matrix and then performing specific calculations using elements of this matrix. Calculations to determine the phase shift variable, $q_{PhaseShift}$, are presented in Chapter Seven.

The algorithm to determine the magnitudes required for calculation is performed under the following procedure for each phase independently:

1. Portions of the pre-test voltage and current waveforms for each phase are isolated and measured to determine the RMS magnitude of $|V_{pre\text{-}test}|$ and $|I_{pre\text{-}test}|$.
2. Portions of the in-test voltage and current waveforms for each phase are isolated and measured to determine the RMS magnitude of $|V_{in\text{-}test}|$ and $|I_{in\text{-}test}|$.
3. The three phases are averaged resulting in:
   i. $\left|\overline{V}_{Pre-test}\right|$ - Three phase averaged pre-test voltage magnitude
   ii. $\left|\overline{I}_{Pre-test}\right|$ - Three phase averaged pre-test current magnitude (not currently used in further fault current calculations)
   iii. $\left|\overline{V}_{in-test}\right|$ - Three phase averaged in-test voltage magnitude
   iv. $\left|\overline{I}_{in-test}\right|$ - Three phase averaged in-test current magnitude

This is graphically presented in Figures 6.4 and 6.5:

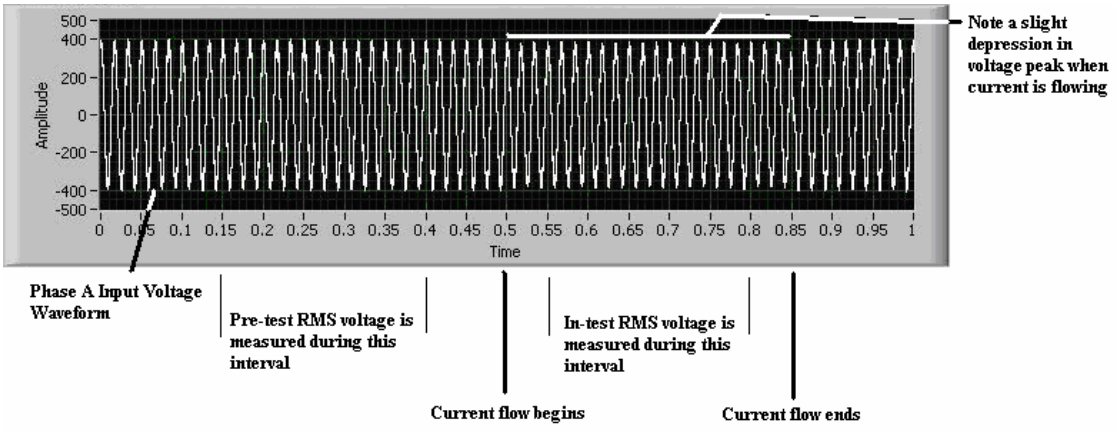

Figure 6.4. Defining input voltage waveform pre-test and in-test RMS magnitude.

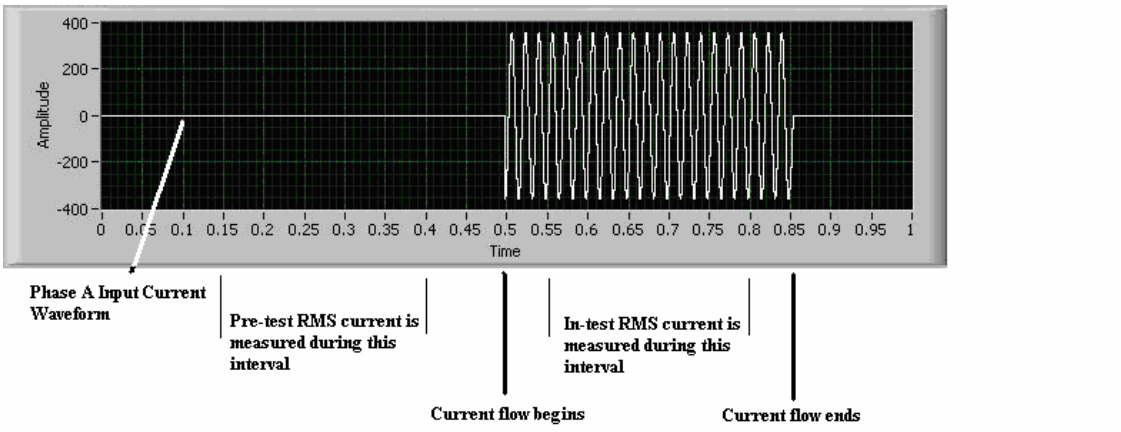

Figure 6.5. Defining input current waveform pre-test and in-test RMS magnitude.

Lead length wire impedance compensation has been integrated into the IADD. Currently the values are set static and applies only to the AWG 8 (American Wire Gauge) wire used in the prototype model. The values are calibrated for resistance and reactance of free wire per NEC2005 Table 9. They may be adjusted by changing values only in the back panel program. Future development would allow the user to select the type and condition of wire used for measurement lead. This will be implemented as a lookup table that selects values as they are given in the National Electric Code (NEC) or other appropriate documents. Users are allowed to specify the wire lead length. This variable is then put into a calculation that subtracts this impedance from the calculated power system impedance shown in Figure 6.2. Effectively, this removes error due to impedance introduced by the IADD when measuring the system parameters.

$$Z_{\text{Power System Compensated}} = R_{\text{PowerSystem}} + X_{\text{PowerSystem}} - \frac{L \times (R_{\text{Cable Z/1000ft}} + jX_{\text{Cable Z/1000ft}})}{1000} - R_{\text{connection}} \tag{6.3}$$

where L is the user specified lead length between the line side fuse block and node connection point.

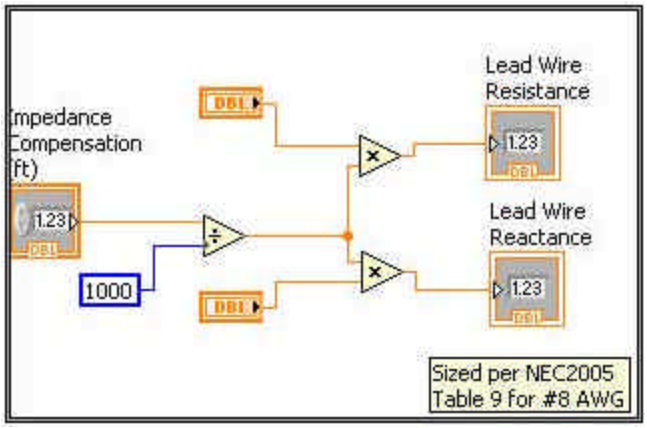

Figure 6.6. Compensation algorithm to determine lead length impedance.

From the values calculated in Figure 6.2, the bolted fault current duty can be determined. Measured test resistance is also calculated here.

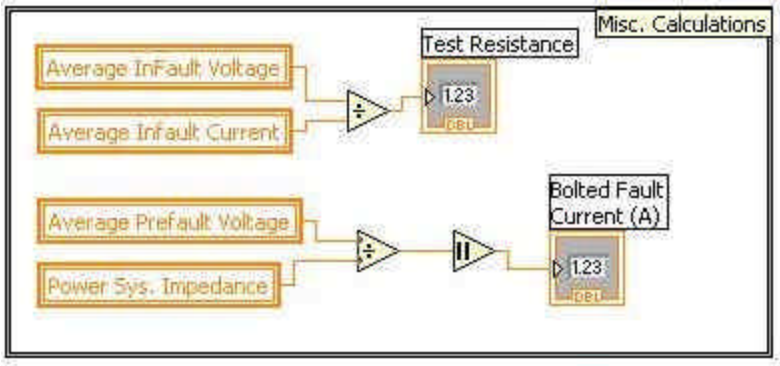

Figure 6.7. Resulting calculations for bolted fault current and test resistance.

6.4. Determining Arc Flash Incident Energy from Calculated Parameters

In Figure 6.8, the algorithm to determine arc flash incident energy is presented using LabView graphical coding. This calculation is based on several variables including the type of enclosure, the working distance from the arc, and the distance between conductors, which is also called the gap distance. These variables were presented and defined in Section 5.1.

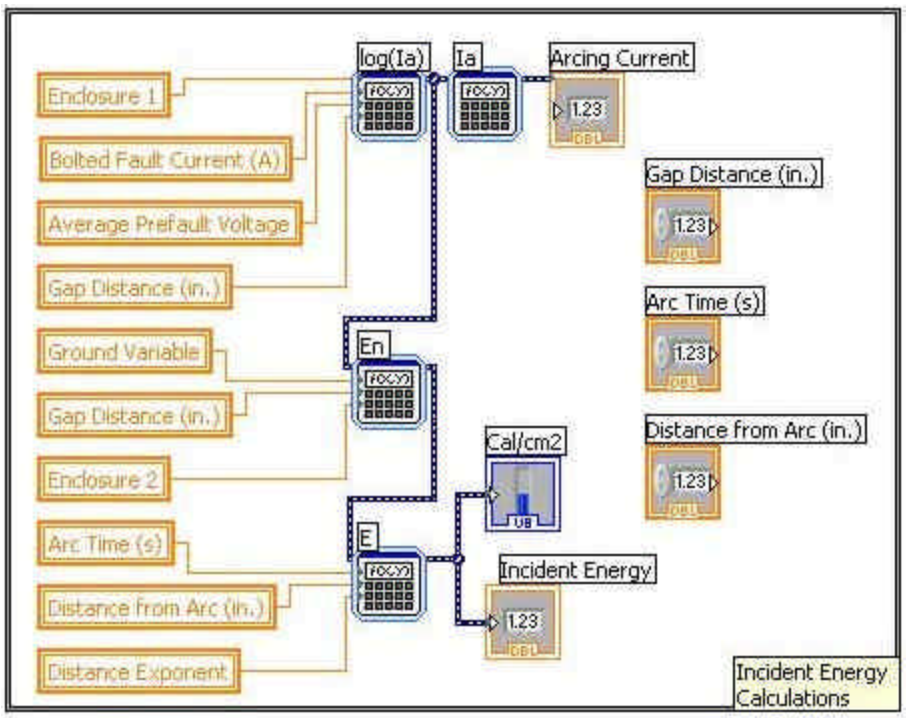

Figure 6.8. Implementation of incident energy calcuations.

The following equations were implemented in the programming block depicted in Figure 6.8. The equations implemented in the program differ slightly from the ones given in Equation 6.4, 6.5, and 6.6 from IEEE 1584 because the user is prompted to enter all variables in Standard English units.

$$\log(I_a) = K + 0.662 \times \log(I_{bf}) + 0.0966 \times V + 0.000526 \times G + 0.5588 \times V \times \log(I_{bf}) - 0.00304 \times G \times \log(I_{bf}) \quad (6.4)$$

where,

I_a is arcing current (kA)

K is -0.153 for open configurations and

is -0.097 for box configurations

I_{bf} is bolted fault current for three-phase faults (symmetrical RMS) (kA)

V is system voltage (kV)

G is the gap between conductors (mm).

$$\log(E_n) = K_1 + K_2 + 1.081 \times \log(I_a) + 0.0011 \times G \quad (6.5)$$

where,

E_n is the incident energy (J/cm2) normalized for time and distance

K_1 is -0.792 for open configurations (no enclosure) and
is -0.555 for box configurations (enclosed equipment)

K_2 is 0 for ungrounded and high-resistance grounded systems and
is -0.113 for grounded systems

G is the gap between conductors (mm)

Converting from normalized incident energy:

$$E = C_f E_n \left(\frac{t}{0.2} \right) \left(\frac{610^x}{D^x} \right) \quad (6.6)$$

where,

E is incident energy (cal/cm2)

C_f is a calculation factor: 1.0 for voltages above l kV, and
1.5 for voltages at or below 1 kV

t is arcing time (seconds)

D is distance from the possible arc point to the person (mm)

x is the distance exponent from Table B.3 in Appendix B of this thesis.

As noted in Section 5.1 and in Equations 6.4, 6.5, and 6.6, several selections must be made to complete the incident energy calculations. For instance, selection of an open or closed configuration from the pull-down menu shown in Figure 5.1 can

result in one of two different values for the variable K in Equation 6.4. Similar decisions must be made for K_1, K_2, and x. Algorithms to select values for these variables based on user specification are given in Figures 6.9, 6.10, and 6.11.

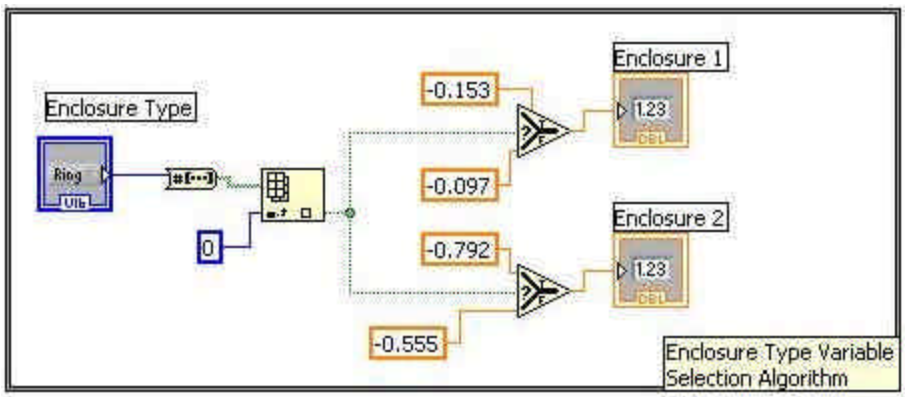

Figure 6.9. Selection of variables K and K_1 based on enclosure type based on equations 6.4 and 6.5.

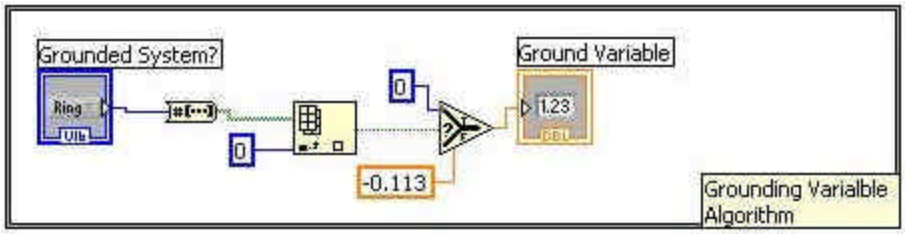

Figure 6.10. Selection of variable K_2 based on presence or absence of a ground.

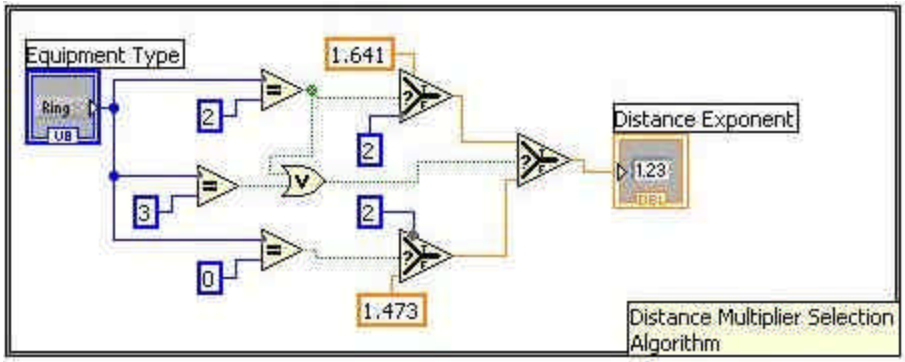

Figure 6.11. Selection of variable x based on equipment type (see table B.3).

After determining the incident energy in cal/cm^2, an algorithm has been written to determine the NFPA category number based on the values specified in Table 1.1.

This algorithm generates the large red number, $N_{NFPA\ Rating}$, seen in the center of Figure 5.1 and ranges from zero to four.

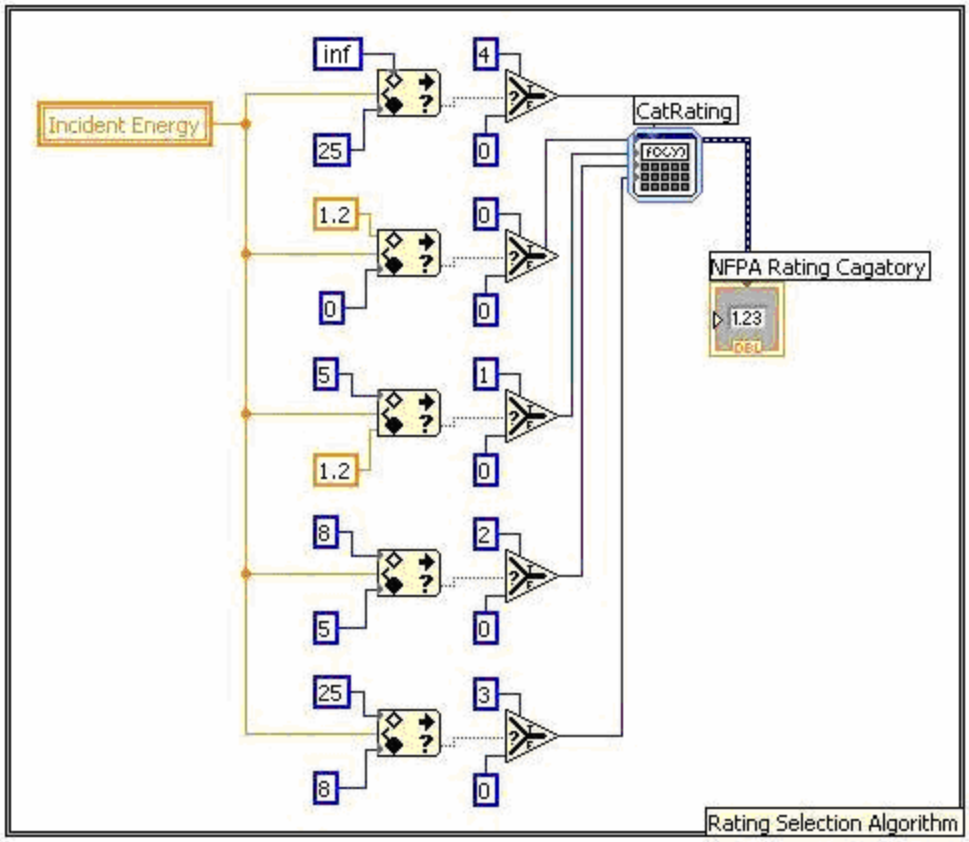

Figure 6.12. Algorithm to determine NFPA rating category based on calculated incident energy.

$$N_{NFPARating} = \begin{cases} 0 \le E_{Incident} < 1.2, & 0 \\ 1.2 \le E_{Incident} < 5, & 1 \\ 5 \le E_{Incident} < 8, & 2 \\ 8 \le E_{Incident} < 25, & 3 \\ 25 \le E_{Incident} < \infty, & 4 \end{cases} \tag{6.7}$$

6.3. Miscellaneous Calculations

From the adjusted power system impedance value, Equations 6.8 and 6.9 are utilized in LabView. These equations assumes a balanced voltage on all three phases, and the per-unit system impedance is calculated.

$$Z_{base} = \frac{(V_{base})^2}{S_{base}} \tag{6.8}$$

$$Z_{\text{Per Unit}} = \frac{Z_{\text{PowerSystem}}}{Z_{base}} \tag{6.9}$$

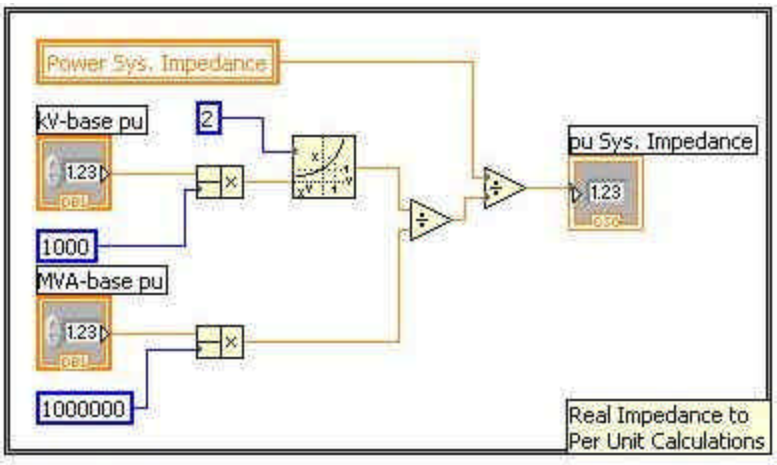

Figure 6.13. Implementation of per-unit calculations.

As mentioned in Section 5.3.1, the voltage and current imbalance is measured in a method differing from the standard NEMA calculation. This is done to account for the possibility of measuring in a wye configuration rather than in delta. In Figures 6.14 and 6.15, the software code implemented to measure voltage and current imbalance is presented, respectively. A boundary condition is set to alert the user if voltage or current imbalance exceeds five percent as calculated in Equation 5.1.

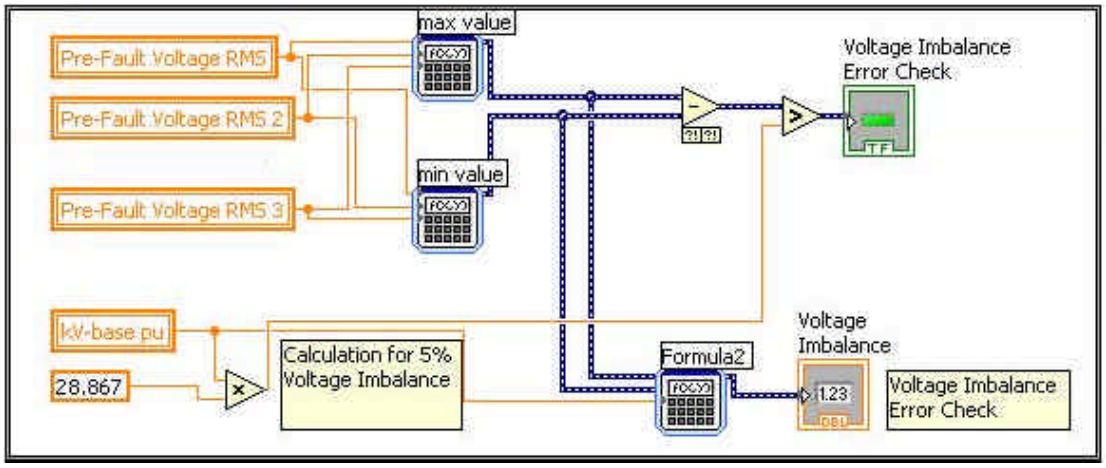

Figure 6.14. Voltage imbalance error check implementation in LabView code.

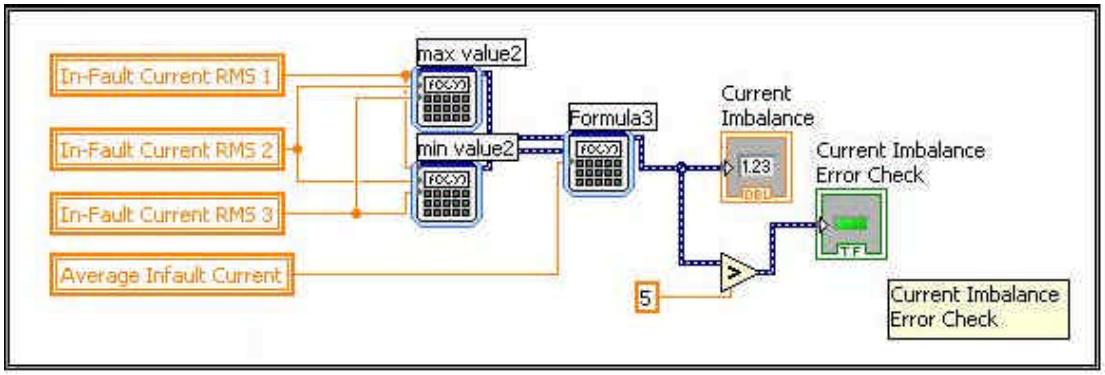

Figure 6.15. Current imbalance error check implementation in LabView code.

Additional error check algorithms have been implemented in code to note other anomalies observed during testing. Figure 6.16 presents the algorithm for determining if a phase wrap error has been detected. Each of the three phase shifts are examined. If phase shift exceeds 90 degrees, then the phase wrap error is toggled.

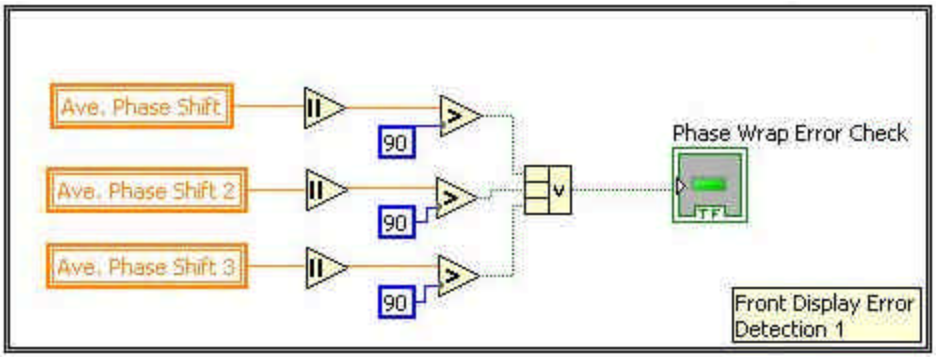

Figure 6.16. Phase wrap error check implementation in LabView code.

Figure 6.17 presents the algorithm for determining if a phase angle drift error has been detected. Because the IADD does not rely on a phase locked loop to maintain a synchronized sampling frequency with the power system, phase drift is monitored. Causes of phase drift are discussed in further detail in Section 7.1. The voltage controlled oscillator (VCO) on the National Instruments DAQ card is subject to changes due to temperature variation internal to the IADD onboard computer. The electrical power system itself is subject to variation in fundamental frequency; although, typically not exceeding 0.02 Hz. Both of these play a role in creating drift that will be discussed in more detail in Chapter Seven. The error check algorithm examines the phase drift on each of the three sampled phases and is triggered if the value exceeds one in any case. Phase drift is ignored if a phase wrap error is detected.

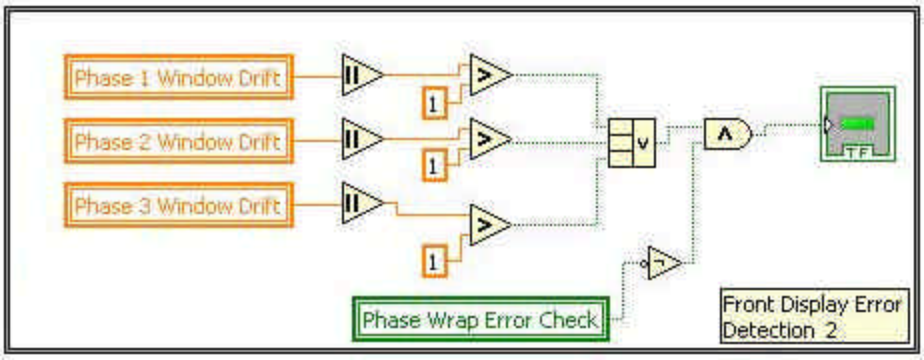

Figure 6.17. Phase drift error check implementation in LabView code.

6.3. Data Collection

Algorithms have been implemented in the IADD program to collect and store data into comma separated variable (*.csv) format.

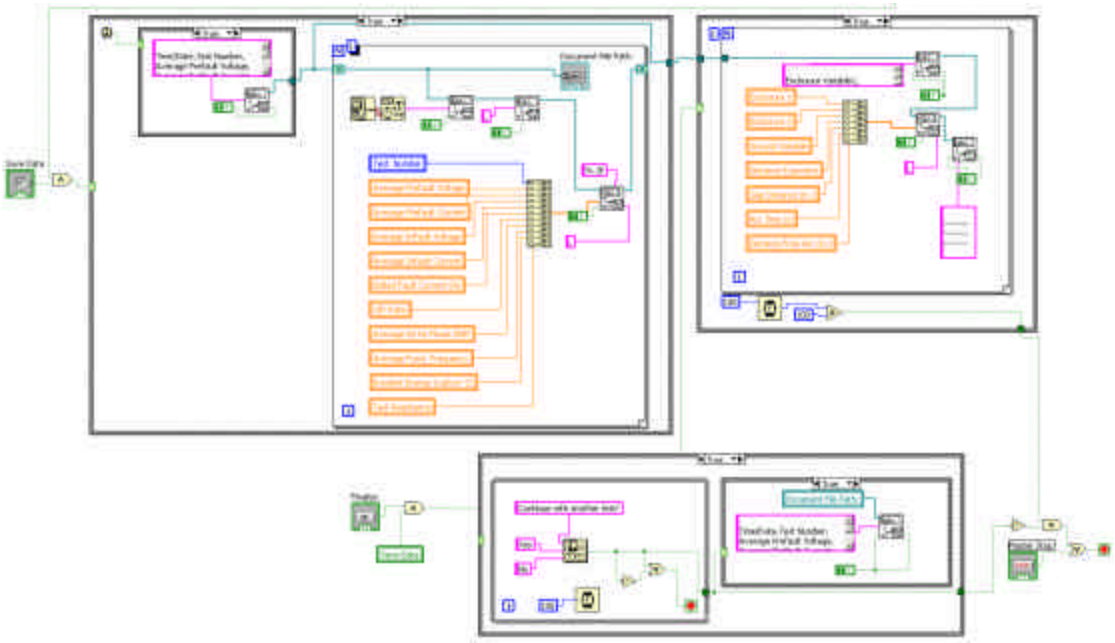

Figure 6.18. Data collection algorithm implemented in LabView.

The algorithm is executed every time a test is completed if the Save Data dialog box is marked. The first line written contains descriptive headers, which defines what each column of data represents. This line is written once and is followed by data on the following line. One line of data is written for each test. Several data points have been selected for data collection including bolted fault current, X/R ratio, incident energy, and average pre- and In-Test currents and voltages. If the "Finalize" button is pushed, addition information on user setting is written to the file including the variables used in the incident energy calculations. A sample report is included in Appendix D.

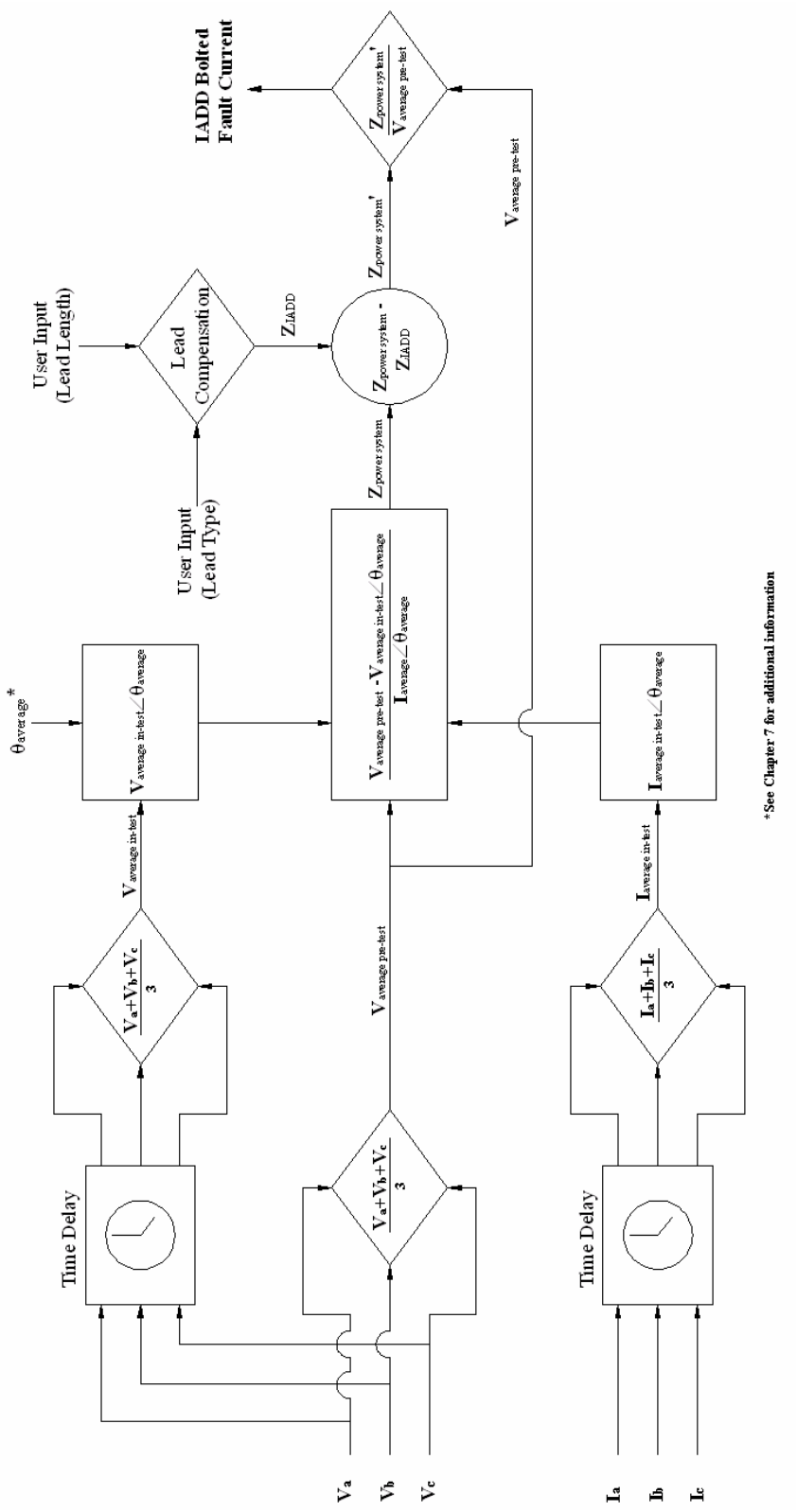

Figure 6.19. IADD bolted fault current and X/R ratio calculation flow diagram, refer to figure 7.11.

CHAPTER 7

DETERMINING X/R RATIO AND CONSIDERATIONS IN CALCULATIONS

Chapter Seven presents the means by which phase shift and X/R ratio are resolved in the IADD. In Chapter Six, the computations for determining power system impedance, bolted fault current, and incident energy are discussed. Phase shift of the measured input voltage waveform is one of the variables used in calculations to determine these resultants and is assumed to be given in Chapter Six. Several algorithms are developed to determine the power system X/R ratio and unique challenges are faced in the implementation of each. This chapter presents these methods and the final algorithm developed for calculating phase shift.

7.1. Introduction to Phase Shift Detection and Challenges

Accurately determining phase shift due to a step load change in a time varying voltage waveform is one of the more challenging aspects of this project. Several factors affect measurement and determination of phase shift including:

1. Sampling frequency
2. Spectral leakage
3. Power system frequency drift
4. Neutral shift introduced in un-grounded systems

Several techniques are employed to minimize the effects of these factors. For instance, sampling frequency has been initially set to 6000 Hz, or 100 sample points per cycle. Any sampled signal is subject to some uncertainty with respect to phase. Some error is associated with choosing non-integer samples per cycle. This is not an issue in

this case, because LabView only allows integer frequency and sample points to be chosen. Typically, additional accuracy can be obtained by choosing a sampling frequency that produces an integer number of samples per cycle that is also a power of two (i.e., 256, 516, 1024 …). This is not true in the case of the IADD because there is no synchronization between the sampling clock on board the IADD and the power system fundamental frequency. After testing the system at 6000 Hz, the frequency is modified to 61.44 kHz, or 1024 samples per cycle. Currently the sampling frequency has been increased to 5291 samples per cycle or 317.46 kHz, taking advantage of reduced error due to spectral leakage while minimizing phase drift. Considerations in selection of this sampling frequency are presented in Section 7.1.1.

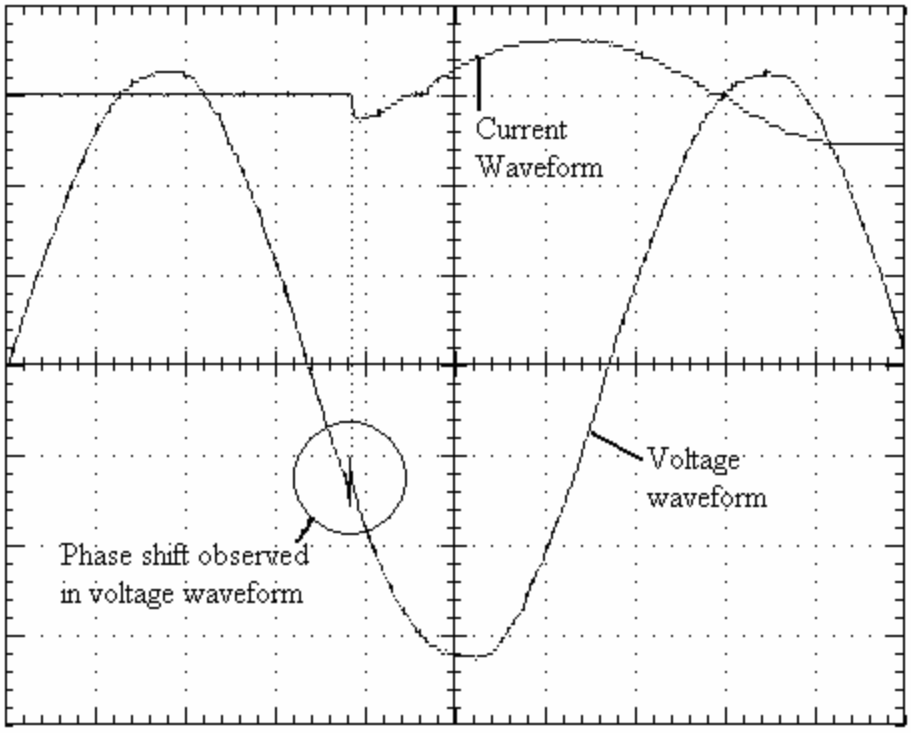

Figure 7.1. Current and voltage waveforms demonstrating observed phase shift and moment of switching

7.1.1 Sampling Frequency Considerations and Spectral Leakage

The higher sampling frequency reduces error in phase due to bin size. Bin size is the measure of how much spectral data is lumped into a specific data point when performing the FFT algorithm. For example, using a sampling frequency of 6 kHz, each bin represents 1/100th of the sampled cycle. In terms of phase, each bin represents 3.6 degrees of phase shift; this implies that the accuracy of phase measurement would be bounded by a random error of no less than +/- 3.6 degrees. Calculations to determine X/R ratio are highly dependent upon accurate measurement of phase shift due to the increase in load by the IADD. Therefore, minimizing error due to sampling rate is extremely important. The increase in sampling frequency to 317.46 kHz reduces the bin size such that the random phase error due to sampling is now +/- 0.102 degrees, which is an increase in accuracy by a factor of more than 35 (see Table 7.1 for additional details).

Spectral leakage affects any frequency component of a signal which does not exactly coincide with a frequency bin. For instance, suppose a bin size of 1 Hz centered around 60 Hz is defined; all spectral content between 59.5 Hz and 60.5 Hz will be contained in this bin. Now consider a signal with spectral content centered at 59.5 Hz under the same conditions. Some signal information will leak into the adjacent bin and may cause unintentional error in the data being measured.

Since the frequency components of an arbitrary signal are unlikely to satisfy this requirement, spectral leakage is more likely to occur than not with real-life sampled signals. Therefore, some error is introduced when additional signals are present near any harmonic of the fundamental. Since the device only uses the fundamental, there is

little error due to spectral leakage because signals near 60 hertz are typically much lower than the power signal; however, these errors must be considered for completeness.

The power system is commonly thought to operate at a constant 60 Hz. However, this is a generalized simplification that makes typical power system calculations easier with little to no appreciable error introduced as a result of this generalization. The power system must maintain a frequency very close to 60 Hz at all times to remain stable due to the interconnectedness of the power grid. In fact, small fluctuations are tolerated and are to be expected as any change in loading condition will effect the steady state fundamental frequency, or phase angle, in some way. In addition, generators operate on a closed loop control scheme that must constantly adjust generator torque to react to dynamically changing loading conditions present on the power system.

The US Department of Energy (DOE) specifies that any producer of power that is attached to one of the three main power grids that span the continental US and Canada operates at 60 +/-0.02 Hz under normal operating conditions. Furthermore, the time-averaged frequency of the power system over a given twenty-four hour period must be exactly 60 Hz to insure correct and accurate operation of all timing circuitry that operates based on power system frequency. The fluctuations due to the dynamic nature of the power system must be taken into account when performing the FFT over many cycles, because a small change in fundamental frequency away from 60 Hz will impact the accuracy of phase shift measurement.

To compensate for these random fluctuations in fundamental frequency, the IADD actively measures the per-cycle phase drift from one cycle of the FFT to the next. With knowledge of frequency drift in the power system, the appropriate error can be estimated such that the IADD is now significantly more immune to random shifts in frequency due to normal power system operations, i.e., a reference is established. While this method decreases the phase shift measurement error by several orders of magnitude, there is still some additional error due to the fact that the FFT is a discrete function. When the program estimates the phase shift attributed to power system frequency drift, it must choose the point that is closest to the expected data point in which no phase shift is expected. An additional +/- one half of the error in degrees is introduced because of the discreetness inherent in the calculations.

An equation for expected phase shift error bounds can be obtained from these considerations based on the sampling frequency chosen, once again assuming that the frequency chosen is an integer power of two:

$$e_p = 1.5 \times \frac{60 \times 360}{f_s} \tag{7.1}$$

where e_p is the error bound on phase shift accuracy, and f_s is the sampling frequency in hertz. Table 7.1 details the expected error band for integer power of two sampling frequencies (2^n) from n = 2 to 16.

Sampling Frequency	+/- Phase Error Band (Degrees)	Sampling Frequency	+/- Phase Error Band (Degrees)
480	67.5	61440	0.5273
960	33.75	122880	0.2637
1920	16.875	245760	0.1318
3840	8.4375	491520	0.0659
7680	4.2188	983040	0.033
15360	2.1094	1966080	0.0165
30720	1.0547	3932160	0.0082

Table 7.1. Phase error in degrees due to sampling frequency

7.1.2. Sampling Frequency Considerations and Synchronization with the NI-DAQ

In Section 7.1.1, it is proven that maximizing the sampling frequency is preferred to reduce measurement error by increasing differentiation in phase angle measurements. The maximum sampling frequency of the DAQ card is 500 kHz. However, additional consideration must be made in selecting the sampling frequency based on the DAQ card's internal timing circuitry. The master clock has a switching frequency of 20 MHz. Optimization of the sampling frequency to the master clock requires some careful consideration. The selected sampling frequency should be as close as possible to an integer value of 20,000,000 and be a multiple of 60, the fundamental frequency being measured. Therefore, there are four factors to consider when selecting the appropriate sampling frequency based on these considerations:

1. Sampling frequency is an integer number
2. Sampling frequency is an integer divisor of 20 MHz
3. Sampling frequency is an integer multiple of 60 Hz
4. Sampling frequency is less than 500 kHz

An analysis to determine the optimal sampling frequency is conducted using principles of abstract algebra. The modulus function is used to determine the best choice of sampling frequency given the constraints presented.

$$f_s = \mathrm{mod}\left(\frac{20{,}000{,}000}{N}, 60\right)_{N=40}^{200} \tag{7.2}$$

The selection is further constrained by the maximum sampling frequency. N=40 is the minimum value that satisfies constraint four. An upper bound for N=200 is selected, defining a lower acceptable sampling frequency of 100 kHz. The function defined in Equation 7.2 is then evaluated for all values of N from 40 to 200.

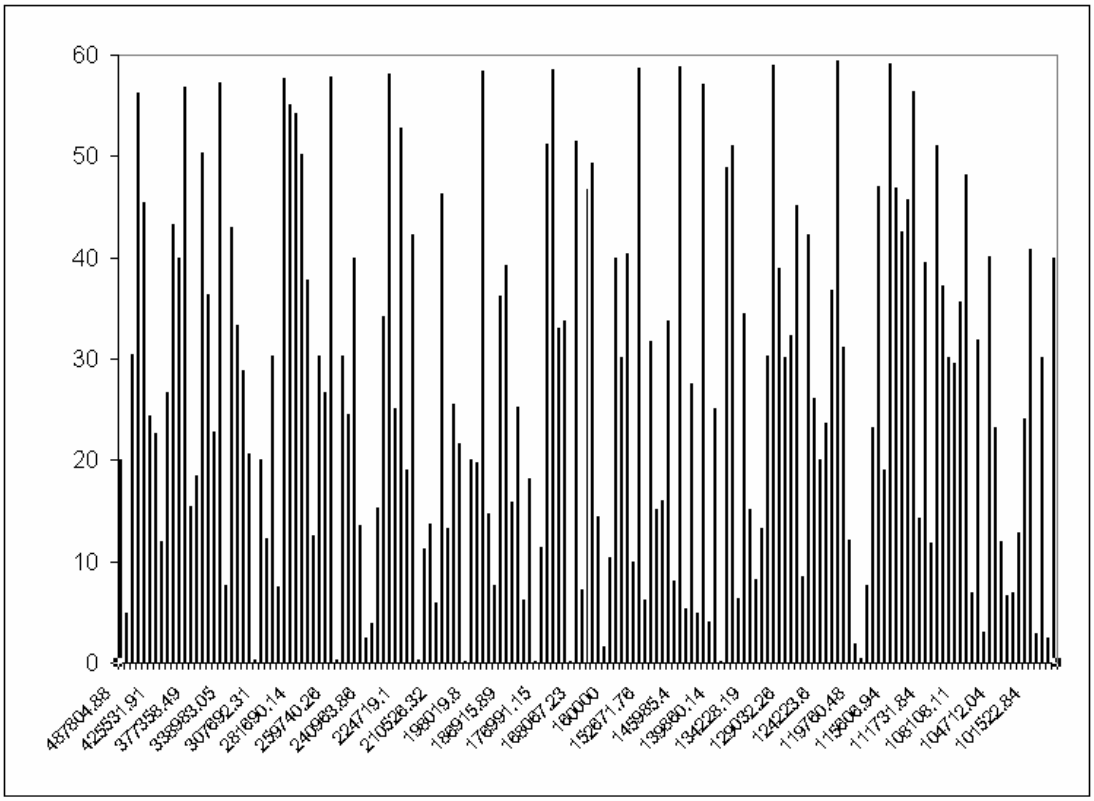

Figure 7.2. Results of the analysis to optimize sampling frequency.

Figure 7.2 displays the results of performing the 60 Hz modulus operation over all integer multiples of 20 MHz from 40 to 200. The goal is to find the values that best satisfy constraints two and three explained previously. From this data, the following table of acceptable sampling frequencies is generated.

N	$f_s = N / f_c$	int (f_s)	mod(f, 60)
63	317460.32	317460	0.32
77	259740.26	259740	0.26
91	219780.22	219780	0.22
99	202020.20	202020	0.20
111	180180.18	180180	0.18
117	170940.17	170940	0.17
143	139860.14	139860	0.14
167	119760.48	119760	0.48

Table 7.2. Acceptable sampling frequencies for optimization of the IADD measurement system.

The sampling frequencies listed in column three of Table 7.2 represent the integer frequencies optimized based on the four constraints given. Shown in column four of Table 7.2 are the resultant modulus values that most closely satisfy minimizing constraints two and three to reduce sampling error due to phase drift. A method has been developed to compensate for phase drift error, so the maximum sampling frequency is chosen to reduce error due to phase measurement differentiation. The sampling frequency selected for the IADD is 317.46 kHz.

7.2. Phase Shift Detection – Preliminary Trials

Initial tests to evaluate feasibility are discussed in Chapter Four. The preliminary test circuit to determine phase shift measurement feasibility consists of a set of three plate-construction power resistors and a NEMA size 3 contactor with 120 volt coil operation. A Tektronics™ digital oscilloscope is set up to trigger on the coil signal, and captures of voltage and current waveforms are taken. The data is transferred to a mobile laptop using Tektronics WaveStar™ software. The raw data is imported into an Excel spreadsheet and graphed as shown in Figures 7.3 and 7.4.

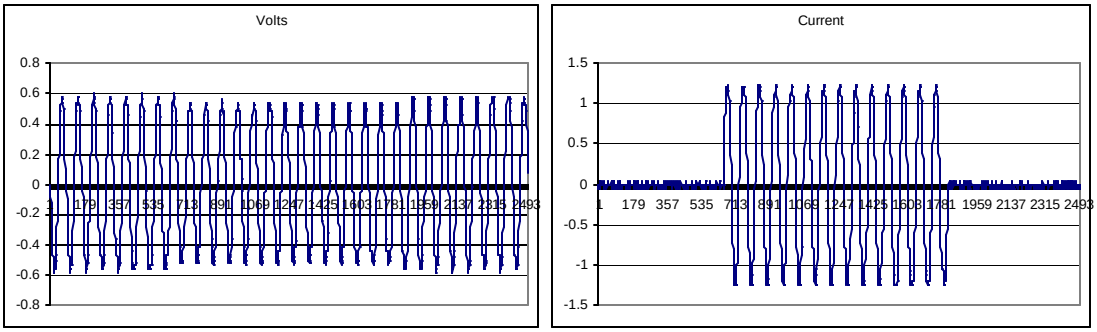

Figure 7.3. Initial trial captures with tektronics wavestar, resistive loading (a) observed voltage waveform and (b) observed current waveform.

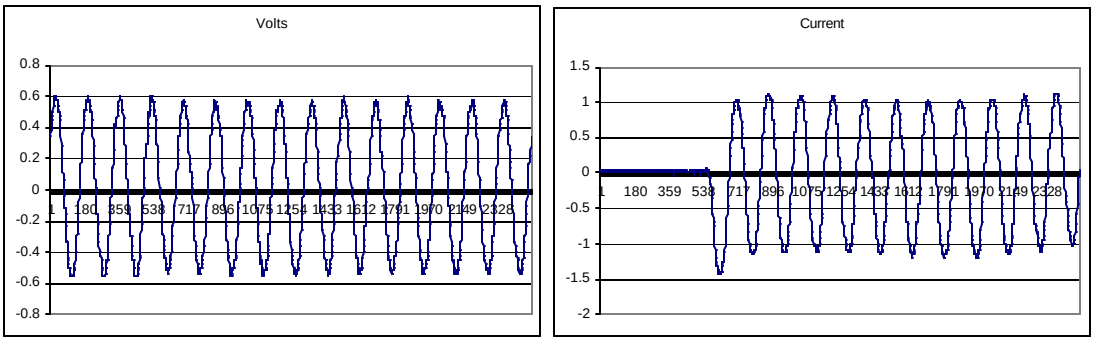

Figure 7.4. Initial trial captures with tektronics wavestar, motor loading (a) observed voltage waveform and (b) observed current waveform.

Tests are also performed by replacing the static resistive load with an induction motor start. Using a motor start can be particularly advantageous because a motor is installed at the electrical buss to be tested, in most cases. It provides the variable controlled load required to measure the voltage and current parameters used in the IADD calculations. When induction motors are started across the line, the input impedance at the moment of energization is extremely low, typically consisting of only the winding resistance and sub-transient reactance of the motor stator. As the motor accelerates, this impedance increases as the slip decreases. By examining the voltage and current waveforms during the first few cycles of starting, a similar observation concerning voltage drop and phase shift can be observed. Assuming that the motor has

significant inertial load and takes several seconds to reach full speed, the first several cycles during a motor start should closely approximate using a resistive load.

Using a motor load presents some additional challenges with respect to accurately measuring voltage drop and phase shift. Because the motor contains a large reactive impedance component, a transient is always associated with motor starting. This is evident in the graphs presented in Figure 7.4b. Residual flux and physical relationship between the rotor and stator orientation play a part in determining how each phase of the voltage and current waveform will react during the first cycle of starting. This is referred to as the sub-transient response and typically lasts for less than a full cycle. Additional transients continue to a lesser degree for several more cycles as the motor begins to rotate. These are second order transients that are natural resonant responses to the power system capacitive, inductive and resistive variables.

Based on the complex transient response of a motor start event discussed in the previous paragraph, a resistive load bank is chosen as the test load for the IADD. Considering the transient conditions associated with motor starting waveforms, it would be unnecessary to add an additional element of uncertainty and computational challenges that should be avoided during initial concept development. A motor based load solution may be re-evaluated in future stages of development.

7.3. Phase Shift Detection – Software Implementation Version One

The development of a software based algorithm to determine phase shift has been implemented relatively early in the development of the IADD. Based on a brief analysis of the effects of phase shift on short circuit current calculations, it is known that accurately determining phase shift due to changes in loading conditions would be

critical in determining X/R ratio. A qualitative analysis of the effects of phase shift on bolted fault current calculations is presented in Section 8.2 of Chapter Eight. The preliminary algorithm developed to measure and calculate X/R ratio is presented in Figure 7.5.

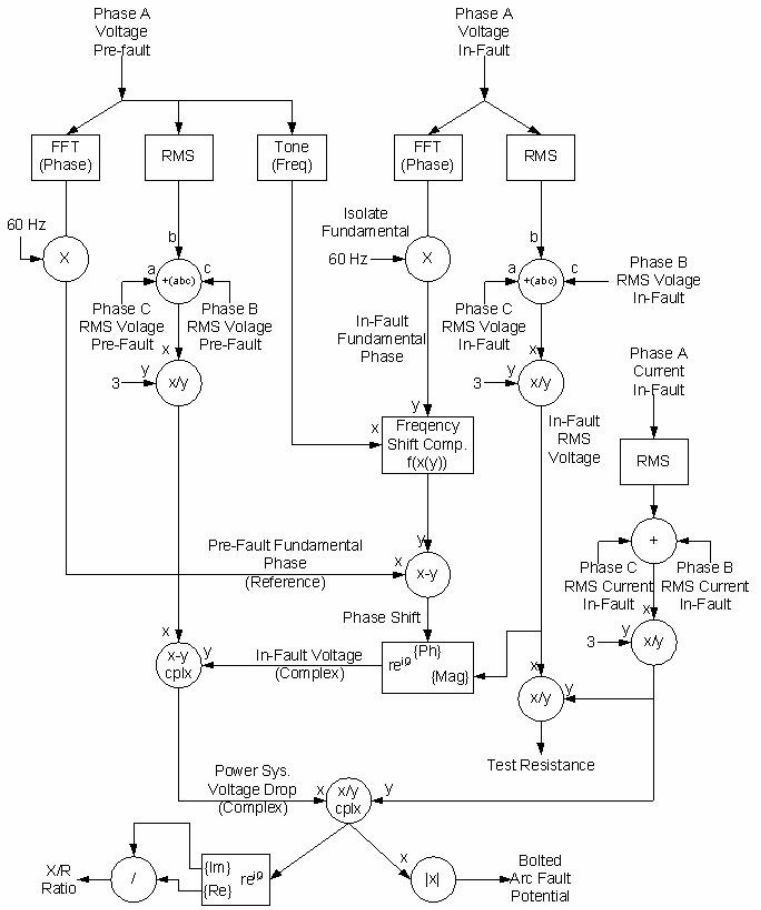

Figure 7.5. Version one cycle-by-cycle phase extraction algorithm.

The algorithm presented in Figure 7.5 resembles the present X/R calculation with respect to the way in which phase angle is measured. An FFT is performed during the pre-switching portion of the test cycle by measuring the input voltage waveform, and the 60 Hz fundamental frequency is isolated. The FFT considered five cycles to resolve a reference phase angle. Because the FFT window spans five cycles of data, the fifth harmonic phase angle data point is observed. The intention is to use this method

as a form of phase angle averaging to mitigate random variation in phase angle that may occur over several cycles of data due to local load shifts.

This process is again repeated twenty cycles later during the portion of the test when the load is switched into the circuit. A differential between the observed pre-switching averaged phase angle and the phase angle measured during switching is then calculated.

There are some inherent difficulties that became apparent when repeated testing is performed using the IADD under this configuration. The FFT algorithm is not an absolute function with respect to phase angle. The phase angle is referenced to the first data point of a waveform data array. To accurately measure phase shift using the methodology previously described, both the pre-switching waveform and waveform capture taken during switching must be synchronized with respect to time.

The method of synchronization implemented in software between the two waveform captures is based on the sampling frequency used during capture. During development, 512 samples per cycle are chosen to determine feasibility of the device, resulting in a sampling frequency of 30.72 kHz. Reasons for selecting sampling frequency that provides an integer number of data points that is also a power of two have already been discussed. As is mentioned previously, the internal clock onboard the IADD is not synchronized to the power system. The implications of this fact were not immediately realized, but it is obvious from initial testing that additional compensation would be required to obtain reasonable results.

A method of active compensation of phase drift is investigated by examining the power system frequency. This is accomplished through empirical testing; two

temporally disjoint sampling windows are created and examined for phase shift in the 60 Hz fundamental under no-load conditions. Since the system is presumed static with respect to frequency between the two sampling windows, a linear mathematical function is used to select the first point of the shifted voltage waveform with the assumption that there should be no measured phase shift observed under these conditions. Optimizing this algorithm is done by repeatedly testing the system under no load conditions and minimizing the value of observed phase shift between the two disjoint sampling windows. Thus, any change in the system due to load introduced by the IADD would cause a measurable phase shift and would not be due to variation in electrical power system frequency.

As is stated previously in Chapter Six, the onboard sampling clock is not synchronized to the electrical power system. However, the algorithm is being implemented under the assumption that the sampling frequency selected produced exactly 512 samples per cycle, which is not the case. Additionally, the major source of variation is attributed to small changes in fundamental (60 Hz) electrical power system frequency. Some consideration is given to synchronizing the clock to the power system by using a phase locked loop (PLL); however, dynamic manipulation of the sampling frequency clock is not readily apparent through the LabView program.

With compensation for frequency sampling discrepancies in place, reasonable values of bolted fault duty and X/R ratio are observed. In fact, it can be noted that the results has a large variance in range. At this stage of development, this is believed to be the natural response of the power system. To the knowledge of the author, no studies

have been conducted regarding the dynamic nature of the power system as it applies to bolted fault current availability.

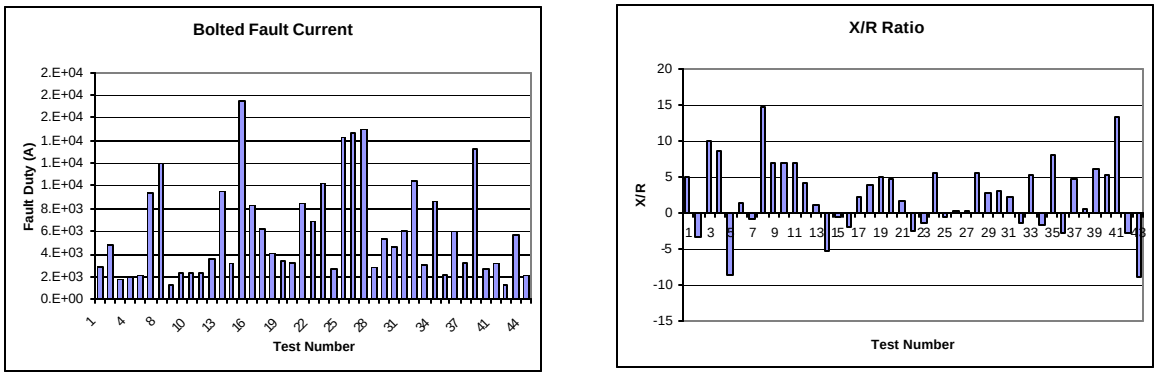

Figure 7.6. Variation in test results affected by FFT window synchronization error during phase one development.

As is demonstrated in sample results from testing in Figure 7.6, there is significant variance in both the bolted fault current calculations and X/R ratio. This variation in results can be largely attributed to a lack of synchronization between the sampling frequency clock, and power system fundamental frequency. To correct this problem, an algorithm is developed based on a continuous FFT calculation that spans the entire testing cycle. This solution eliminates the need to synchronize the IADD to the system clock and other advantages of having a system independent of the power system frequency become apparent.

7.4. Phase Shift Detection – Software Implementation Version Two

A determination on phase shift can be made by comparing the fundamental phase angle prior to and after test conditions have been applied. Using calculated phase shift and voltage change, a determination of X/R (reactance over resistance) and power system impedance can be made. The X/R ratio has several effects on how faults behave. A large reactance will make extinguishing an arc more difficult. Depending

upon the time of fault inception, a decaying DC component may be present in the current waveform with an overshoot and time constant based on this ratio.

Several methods of determining phase shift have been discussed previously in this chapter. Each is implemented in LabView with varying degrees of success. Phase shift has been shown to be extremely critical to producing valid, reproducible results when measuring system parameters, particularly when determining X/R ratio. The solution presented here is a culmination of the lessons learned from each of the previous attempts at determining phase shift.

Phase shift is measured using the FFT analysis toolbox. The fundamental power phase angle is obtained prior to applying the test impedance. The phase angles of the three phase voltage signals are established on a cycle by cycle basis using the Extract Portion of Signal tool that comes with the LabView software package.

The IADD does not use a phase locked loop or trigger on zero crossing. Since the initiation of the test is pseudo-random (initiated by the user clicking on the Test button), a reference (relative) angle can be established based on the first cycle as measured by the onboard FFT calculation. The measurement board has been calibrated to match as closely as possible to the true 60 Hz power system signal. This is why a "phase drift" error indicator has been implemented to warn the user if the power system frequency or sampling frequency of the computer is disrupted or drifts.

Measurements are taken on a cycle by cycle basis and are examined as a single point phase angle determined by the 60 Hz fundamental frequency by extracting that data point and appending it to an array of values from the previous cycle data points. This procedure is used to create the graphs seen in Figures 5.9 and 5.10. Averaging to

reduce random error is accomplished by looking at the turn-on and turn-off phase shift of each phase and is analyzed as described on page 78 of this thesis.

By observing the phase angle of each cycle of the signal, a phase shift differential can be observed prior to and after switching. A similar phase shift of opposite magnitude is observed when the gating signal to the solid state switches is removed. The resistors are then switched out of circuit; this shift is presented graphically in Figures 5.9 and 5.10 and discussed briefly in Chapter Six. Distinct regions of phase shift are identified by collecting the cycle phase angles in a vector form and analyzing the typical cycles of switching.

The phase angle capture algorithm is performed by collecting data and forming a matrix defined by the following procedure:

1. Input voltage waveform is sampled at the user defined sampling frequency.
2. The data is further segregated to analyze each cycle independently.
3. Data for the first cycle of each phase is input into an FFT algorithm and the 60 Hz fundamental phase angle is extracted from the resultant FFT vector (this defines a reference angle for subsequent calculations).
4. The phase angle is placed in a matrix array as shown in Equation 7.1. The subscripts are (θ,n), defining the phase and cycle in sequence.
5. The matrix is populated until fundamental phase angle of all 60 cycles for each phase voltage signal have been defined.

conforming to the following mathematical format:

$$\begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} q_{a,0} & q_{a,1} & \cdots & q_{a,59} \\ q_{b,0} & q_{b,1} & \cdots & q_{b,59} \\ q_{c,0} & q_{c,1} & \cdots & q_{c,59} \end{bmatrix} \tag{7.3}$$

This matrix is formed using the following Labview code for phase A, identical blocks were created for phases B and C:

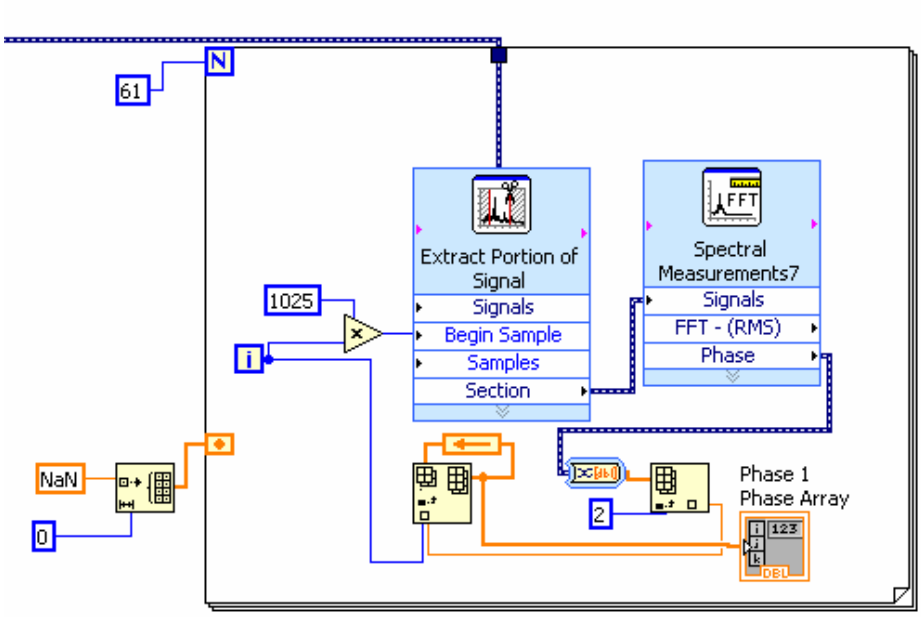

Figure 7.7. Cycle-by-cycle phase extraction algorithm.

The phase angle shift determination algorithm is performed under the following procedure for each phase independently once the phase angle matrix (Equation 7.3) has been completed:

1. Five cycles of the pre-switching waveform data are analyzed, and the average phase differential (drift) per cycle is determined. This establishes synchronization error between sampling frequency and power system frequency.
2. Five cycles of waveform data, during switching in the resistor banks, are analyzed, and the phase shift between the first and last cycle are determined.
3. Based on the average phase drift determined in step one, phase drift compensation is introduced, and an observed phase shift is determined.
4. Five cycles of waveform data, while switched, are analyzed, and the average drift during the switched condition is determined on a per cycle basis.
5. Five cycles of the waveform data, during switching out the resistor banks, are analyzed, and the phase shift between the first and last cycle are determined.
6. Based on the average phase drift determined in step four, phase drift compensation is introduced, and an observed phase shift is determined.

7. Observed phase shift from switching in the resistor banks and switching out the resistor banks are averaged together to yield an average phase shift value for the phase measured.

Steps one through six are repeated concurrently for the remaining two phases.

This is graphically presented in Figure 7.8.

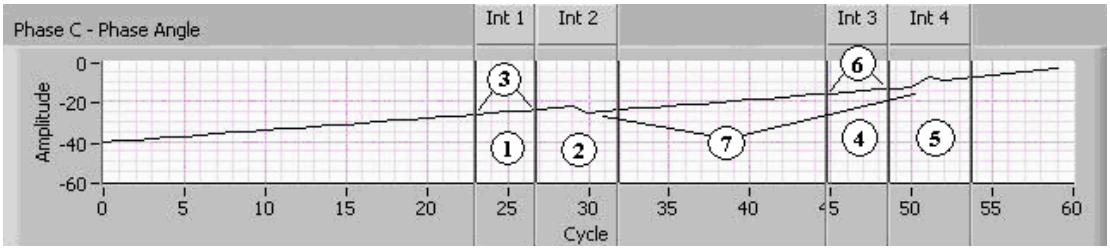

Figure 7.8. Seven step algorithm for determining phase shift in each phase of the incoming current waveform.

And described by Equation 7.4:

$$\bar{q}_{PhaseShift} = \frac{1}{6}\left\{\sum_x \left[(q_{x,53} - q_{x,48}) + \frac{(q_{x,43} - q_{x,48})}{5} + (q_{x,27} - q_{x,32}) + \frac{(q_{x,27} - q_{x,22})}{5} \right]\right\} \quad (7.4)$$

where x is phases a, b and c.

This calculation is implemented in LabView using the code displayed in Figure 7.9. Some attempts have been made to mitigate the effects of phase wrap, but currently no solution is available to solve this issue. Thus, there is the need to have a phase wrap error indicator on the front panel as is discussed in Chapter Five.

Determining phase shift becomes a matter of measuring and compensating for six observed phase shifts, two shifts on three phases. By averaging over the six observable changes in phase angle, the chance of measurements being effected by changes in load to the system during the test can be reduced. Furthermore, the interval, referred to as "Int 1", "Int 2", "Int 3", and "Int 4" in Figure 7.8, where differential measurement of phase shift and intervals of compensation, are minimized. This makes

the calculation immune to relative changes in phase due to changing loading conditions on the system outside of these intervals specifically.

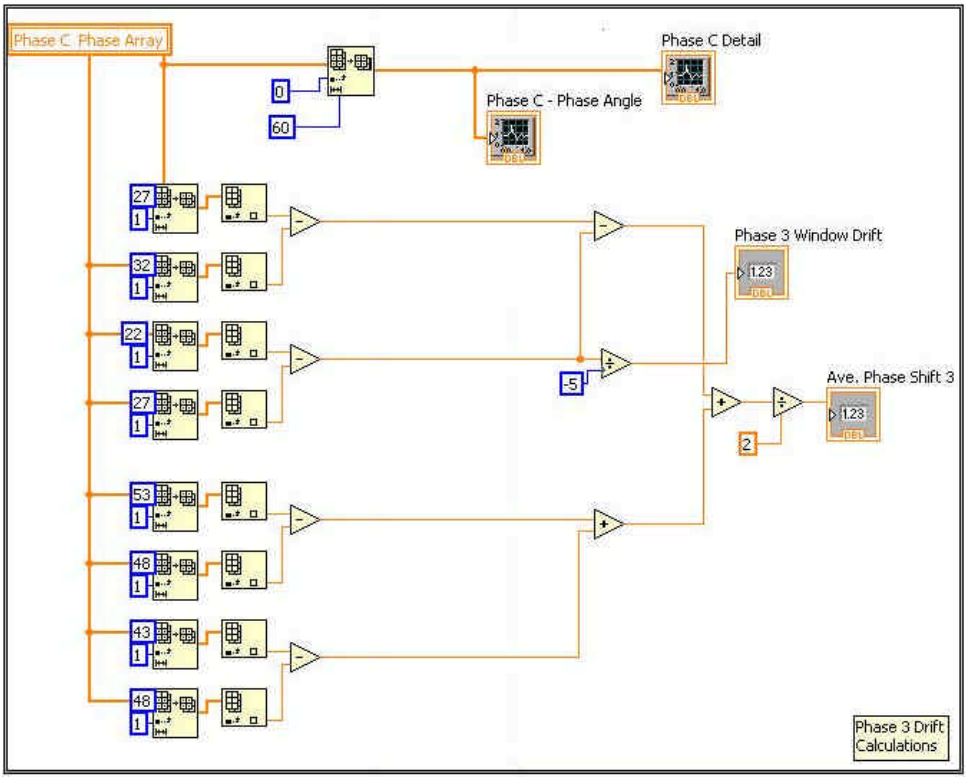

Figure 7.9. Labview implementation of phase detection algorithm.

As long as the system does not change significantly with respect to phase during the ten cycle interval of switching on or off of the IADD resistive load, there will be no affect to the calculation of phase shift, even if system phase shift occurs (and transients dissipate) outside of these intervals.

Isolating the sampling frequency from the electrical power system frequency presents an added advantage of being able to detect changes in power system loading conditions independent of measurement. If loading conditions on the power system change during a test sequence, there will be an associated shift in phase not attributed to the IADD. Furthermore, because the IADD is actively monitoring the phase

differential between consecutive phase angles on a cycle-by-cycle bases, the system has been programmed to predict the observed power system phase angle after testing has been completed.

Data on phase drift collected prior to switching in of the IADD load is used to predict the observed phase angle of the power system after a test has been completed. This takes advantage of a known phase differential due to a lack of synchronization between the IADD and power system fundamental frequency. Once the test sequence is complete, the IADD compares the predicted power system phase angle to the observed power system phase angle. If the observed and predicted angles do not match within a pre-determined error bound, a test reliability warning is activated to alert the user that test data is subject to error due to power system load change. Currently this error bound is set to 0.25 degrees, and future development has been planned to test the sensitivity of load change detection by subjecting the IADD to systems under transient loading conditions.

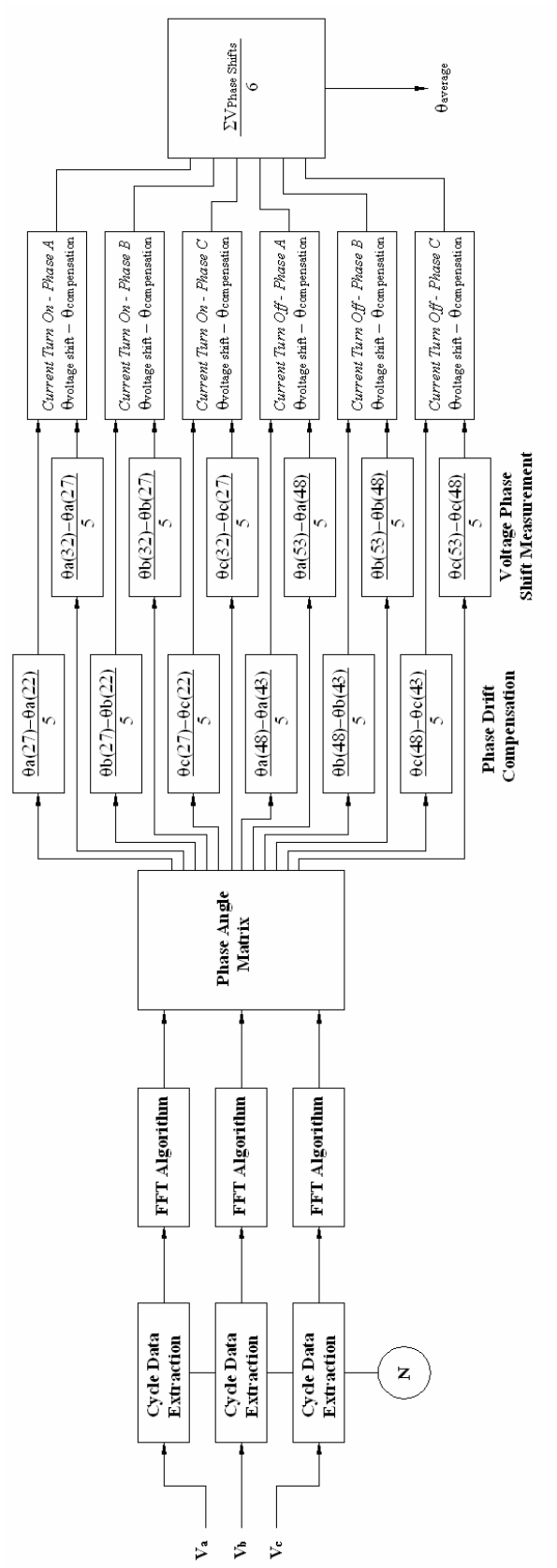

Figure 7.10. IADD voltage phase shift calculation flow diagram, refer to figure 7.11.

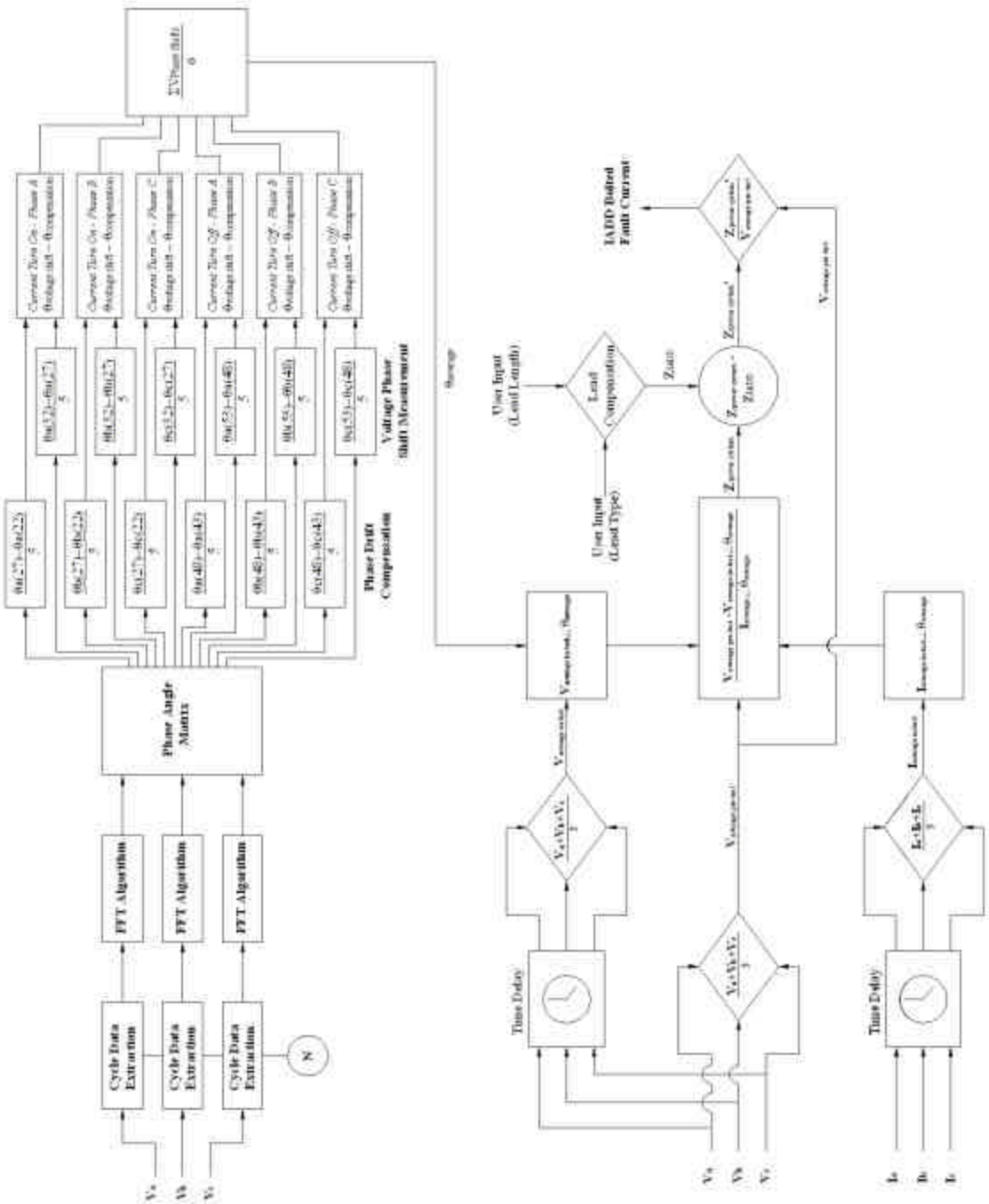

Figure 7.11. IADD calculations flow diagram.

CHAPTER 8

ANALYSES OF FACTORS EFFECTING MEASUREMENT PERFORMANCE

Throughout development of the IADD, several factors that effect measurement performance have been noted. To more completely understand these factors and apply solutions to positively impact performance, analysis is performed to determine the effects of these factors on bolted arc flash calculations as they apply to measurement using the IADD. Chapter Eight presents four such analyses as follows:

1. Qualitative sensitivity analysis of phase shift
2. Qualitative incident energy sensitivity analysis
3. Quantitative analysis of error introduced by neutral shift
4. Analysis of IADD imposed loading on test result variability

8.1. Qualitative Sensitivity Analysis of Phase Shift

A qualitative analysis of sensitivity of measurement to the resultant fault duty and phase angle can be conducted by examining Equation 5.1, which defines the relationship between measured voltage drop and phase shift to calculated system impedance and X/R ratio.

The analysis is conducted by making generalizations of the information provided in Figure 8.1 in a qualitative approach. The figures present a series of curves that represent varying voltage drop in percent. From the graph, there is a strong correlation between percent voltage drop in systems with the system X/R ratio. However, in systems with X/R ratios greater than 1.5, there is a linear region in which

variations in detected phase shift do not significantly affect the calculated bolted fault current.

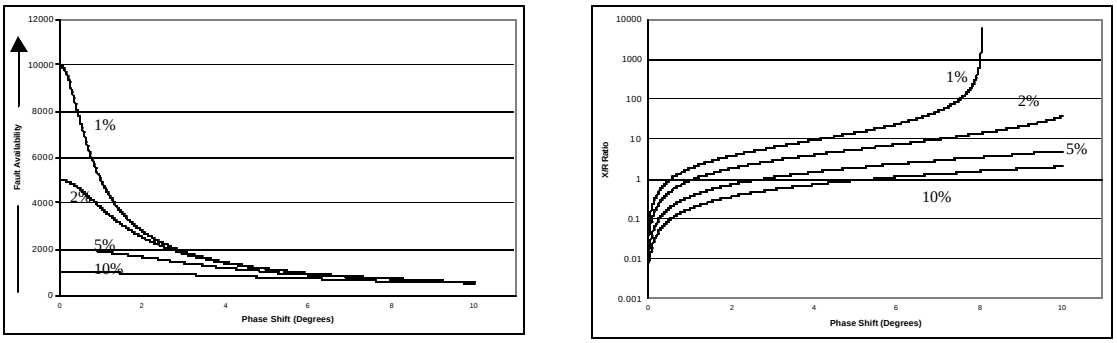

Figure 8.1. Effect of a) fault duty (system impedance) and b) X/R ratio on measured phase shift.

If the error in phase detection given by Table 7.1 is taken to be the total detection error, then it can be seen that errors have a greater effect with respect to bolted fault current on a system with an X/R ratio less than 1.5.

Several other generalizations can be made based on these results. Systems with a high X/R ratio, greater than ten, exhibit invariance with respect to the amount of voltage drop applied to the system during test. This means that less voltage drop needs to be applied to highly inductive systems than those that are principally resistive in nature. Furthermore, there is typically a strong correlation between system stiffness and X/R ratio, which means that for systems with a high X/R ratio, large currents must be drawn to see even an incremental depression in voltage. Conversely, weak systems are typically resistive due to the fact that low voltage feeder impedance is typically resistance dominated.

There is also a correlation between current drawn and observed phase shift. This can be seen by evaluating a system with constant impedance. Where drawing

sufficient current to result in a one percent drop in voltage, the observed phase shift is relatively low. When the voltage drop is increased, more current is drawing through the IADD, and the phase shift increases.

When considering these factors, some general statements can be made. Less voltage drop, thus less current flow is required to be drawn from the system when the X/R ratio is high to obtain a valid, stable result. More voltage drop is required when the system's X/R ratio is low. Unfortunately, as discussed previously, a small drop in voltage on a system with high X/R ratio typically requires drawing significant current due to system stiffness. Obtaining voltage drop on systems with a low X/R ratio is more feasible as these systems are typically considered to be weak and are typically located well downstream of the source.

8.2. Qualitative Incident Energy Sensitivity Analysis

An analysis of resultant incident energy as a function of calculated bolted fault current and time to arc extinction is now conducted. The point of this analysis is to gauge the effects of these factors independently to gain an understanding of what factors play a significant role.

Figure 8.2 shows that incident energy is highly dependent on the type and effectiveness of the protection scheme used in the circuit. For example, an arc extinction time of less than one-quarter (1/4) cycle yields a manageable amount of risk for fault duties less than 100 kA. Therefore, properly functioning primary (or branch) protection should not result in serious, life threatening injury. This fact is supported by the case studies presented in OSHA literature. [17] A review of incident accounts shows that, in most cases, the primary protection is either intentionally disabled or

malfunctioned due to maintenance issues, relying on secondary protection to trip the circuit. However, secondary (or feeder) protection is almost always specified with a coordinated time delay that can sometime reach several seconds in length depending upon the type and speed of primary protection specified.

Arc flash incident energy is also dependent on bolted fault duty so consideration should be given to the type of equipment work that is to be performed prior to selecting the proper protective equipment. Equipment such as switchgear and Motor Control Centers (MCCs) typically have higher fault availability than local disconnect switches. Several assumptions were made in the generation of Figure 8.2: the system is assumed to be grounded; the enclosure type is assumed to be a boxed configuration; the working distance is assumed to be eighteen inches, and the conductor gap is assumed to be one inch.

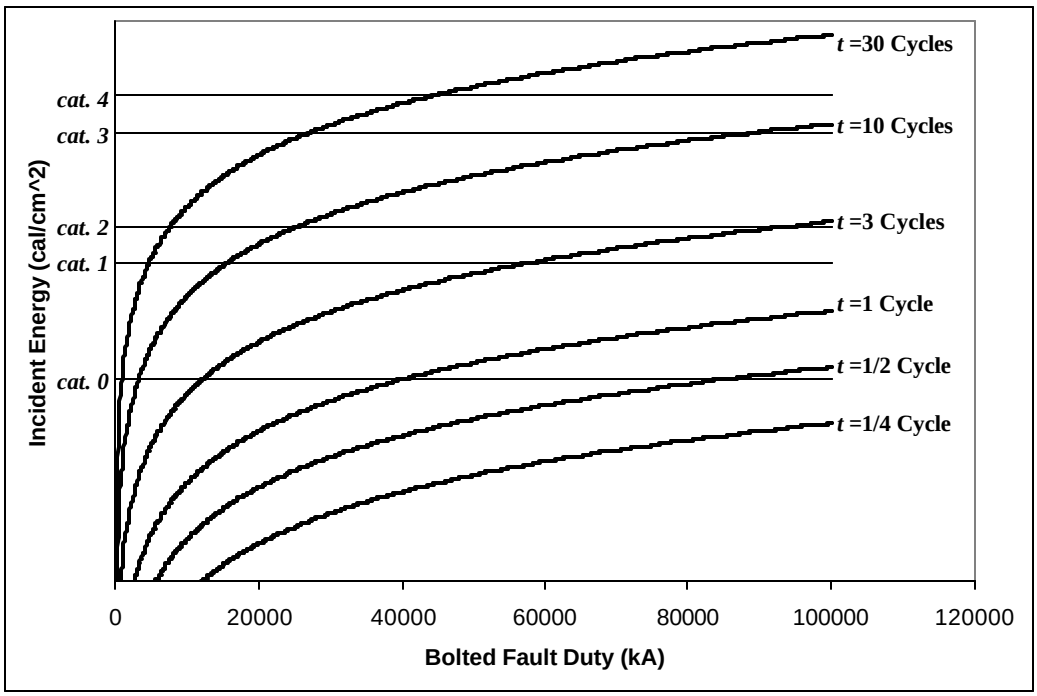

Figure 8.2. Incident energy hazard category assignment as a function of bolted fault duty and primary protection trip times (based on 60 Hz cycle period).

Assignment of an arc flash PPE category number is further complicated by the fact that protective equipment typically has an inverse current-time relationship as discussed in Figure 2.1. This means that faults with a high impedance and less current may take longer to clear than if the fault availability is high. This further complicates the determination of proper PPE for a given work environment. Future development of the IADD will integrate typical current-time trip curves to more accurately assign an arc flash category based on calculated arcing fault current values.

8.3. Quantitative Analysis of Error Introduced by Neutral Shift

Additional error can be introduced in calculated phase shift due to the physical construction of the IADD. The IADD has been initially built and tested on a grounded wye connected system, but may be applied to delta connected systems as well. If a delta system is not well balanced, the load's neutral point will drift with respect to ground. This shift results in skewed voltage measurements that may cause additional error in the phase shift calculations.

This phenomenon is first observed in examination of graphs similar to those depicted in Figure 5.9, which show phase angle variation in all three phases of the input voltage waveforms. It is noted that, when the IADD neutral is not solidly bonded to the power system neutral, unbalanced shifts in phase angle are observed. When the neutral is connected to the system neutral, the phase shifts are balanced in all three phases. This variation in phase angle between individual phases is attributed to neutral shift between the floating neutral of the IADD load bank and the actual system neutral. To determine the effect of neutral shift initial, several example cases are examined.

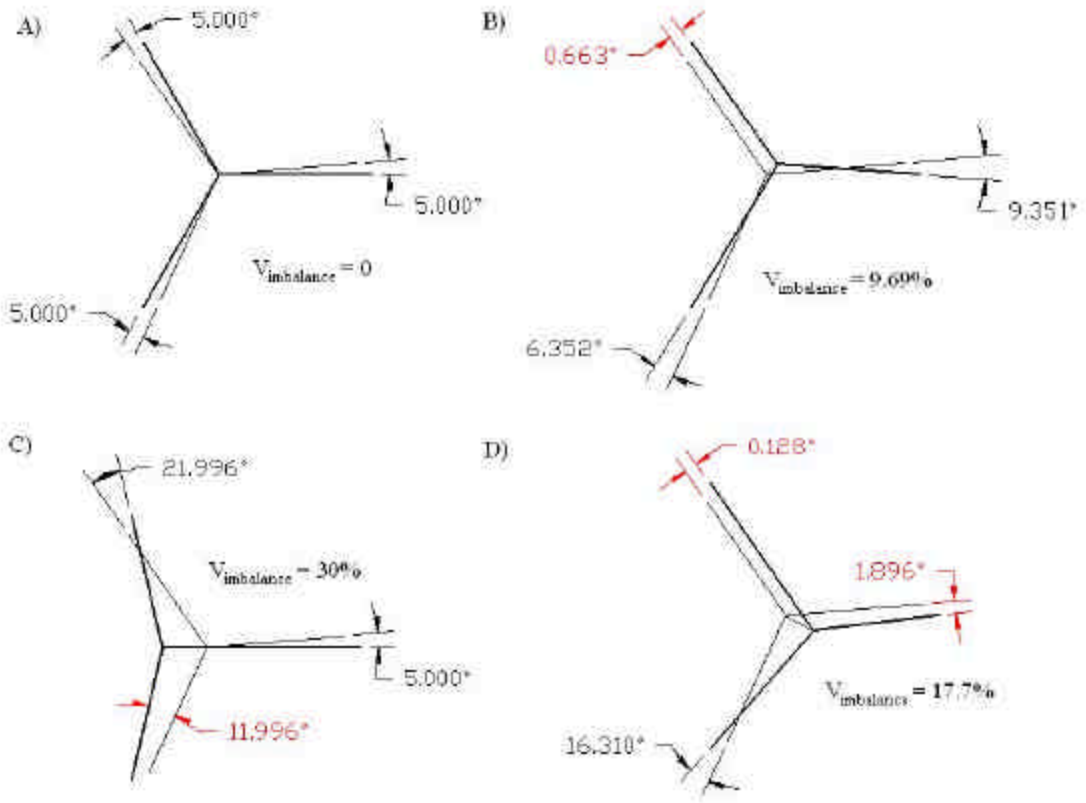

Figure 8.3. Phase angle quantitative evaluation of four neutral position conditions common to delta connected systems.

Cases A, B, C, and D depict typical phase shift in the power system that may affect three phase average phase shift. Case A depicts the system in a balanced state that can be assumed to be the observed system when the neutral is solidly bonded to the resistive load bank. Under this condition, there should be no perceivable shift in neutral position when a load is imposed on the system. Conversely, cases B, C, and D depict cases in which the system is still in a balanced condition due to the floating neutral with respect to the load bank. A perceived shift in neutral is observed when the load is switched into the circuit.

Cases B and C exhibit no significant change in the three phase averaged phase shift using the equations implemented in the IADD software. Under conditions similar to those depicted in these examples, there would be no discernable difference in final

calculations when compared to the system with a bonded neutral. Case D, however, would result in an error in measured phase shift by approximately six percent under the loading conditions shown. Based on these results, a more thorough analysis of the effect of neutral shift is presented in Figure 8.4.

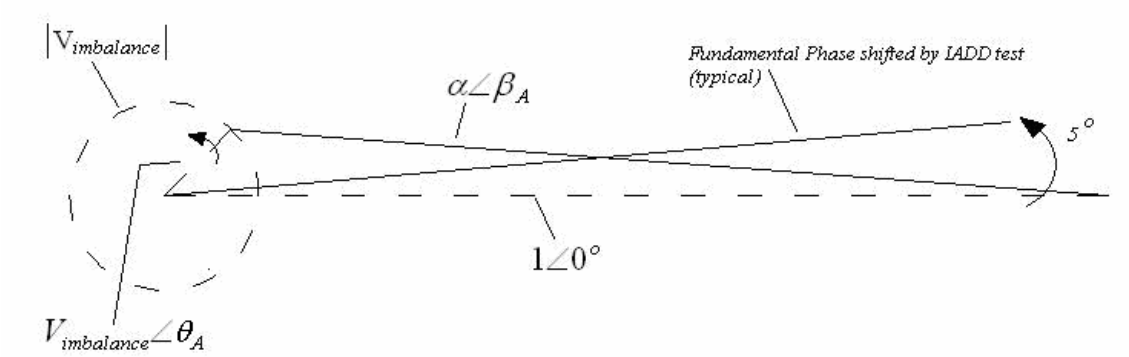

Figure 8.4. Notation used in development of equations to describe phase variation due to neutral shift.

Figure 8.4 depicts the phase A condition where neutral shift plays a factor in the overall determination of calculated phase shift as determined by the IADD. Assuming that at any given point in time, the magnitude of phase A is unity (one) with a phase angle of zero degrees and assuming the phase shift of five degrees. The notation presented in Figure 8.4 is used to develop equations for β_A, the angle of the fundamental phase in the presence of neutral shifting.

$$1\angle 0^{o} = V_{imbalance}\angle q_A + a\angle ß_A \tag{8.1}$$

$$1 = V_{imbalance}\cos(q_A) + V_{imbalance}\sin(q_A) + a\cos(ß_A) + a\sin(ß_A) \tag{8.2}$$

Separating sine and cosine terms yield:

$$1 = V_{imbalance}\cos(q_A) + a\cos(b_A) \tag{8.3a}$$

$$0 = V_{imbalance}\sin(q_A) + a\sin(ß_A) \tag{8.3b}$$

From Equation 8.2, solving for α:

$$a = \frac{1 - V_{imbalance}\cos(q_A)}{\cos(ß_A)} \tag{8.4}$$

Substituting back into Equation 8.2 yields:

$$1 = V_{imbalance}\cos(q_A) + V_{imbalance}\sin(q_A) + 1 - V_{imbalance}\cos(q_A) + [1 - V_{imbalance}\cos(q_A)]\tan(ß_A) \tag{8.5}$$

$$0 = V_{imbalance}\sin(q_A) + [1 - V_{imbalance}\cos(q_A)]\tan(ß_A) \tag{8.6}$$

Solving for β_A yields:

$$ß_A = \frac{\arctan[V_{imbalance}\sin(q_A)]}{[1 - V_{imbalance}\cos(q_A)]} \tag{8.7a}$$

Making appropriate considerations for phases B and C yield the remaining phase angle functions with respect to time:

$$ß_B = \frac{\arctan\left[V_{imbalance}\sin(q_A - 2p/3)\right]}{\left[1 - V_{imbalance}\cos(q_A - 2p/3)\right]} \tag{8.7b}$$

$$ß_C = \frac{\arctan\left[V_{imbalance}\sin(q_A + 2p/3)\right]}{\left[1 - V_{imbalance}\cos(q_A + 2p/3)\right]} \tag{8.7c}$$

These are non-linear equations that are evaluated in the following three figures for selected values of $V_{imbalance}$ at 5%, 10%, 20%, 35% and 50%. The solutions to Equations 8.7a, b, and c are highly sinusoidal when magnitude of imbalance is low (below twenty percent). However, when the imbalance is high due to neutral shift, the resultant is no longer a sinusoidal wave, instead taking on the characteristics of the arctangent function. This is due to the fact that the arctangent function is linear near the zero point and becomes increasingly non-linear with increased magnitude.

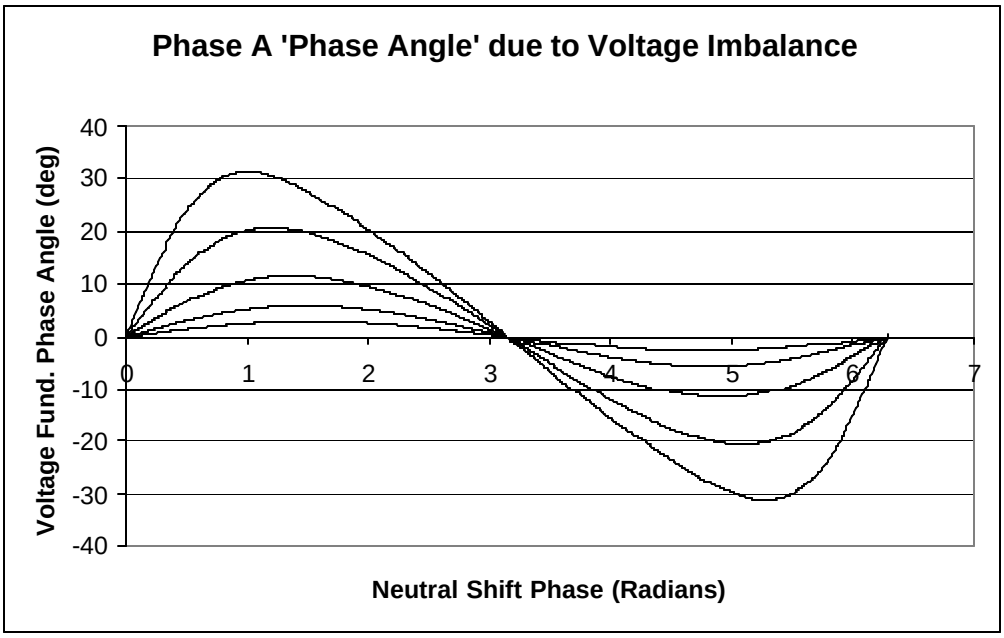

Figure 8.5. Phase angle error contribution for phase A due to voltage imbalance at 5%, 10%, 20%, 35% and 50% respectively.

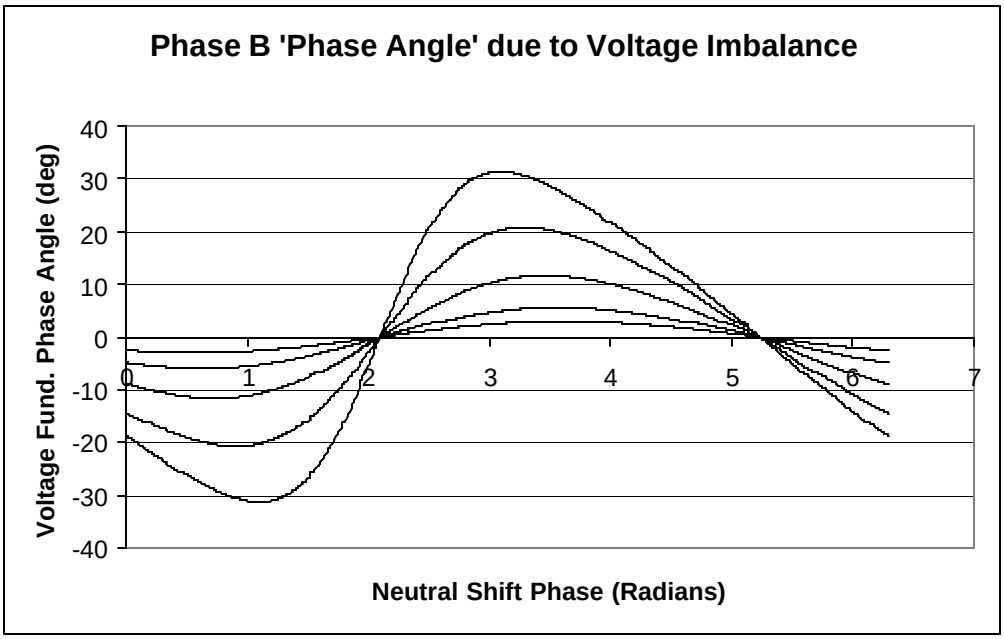

Figure 8.6. Phase angle error contribution for phase B due to voltage imbalance at 5%, 10%, 20%, 35% and 50% respectively.

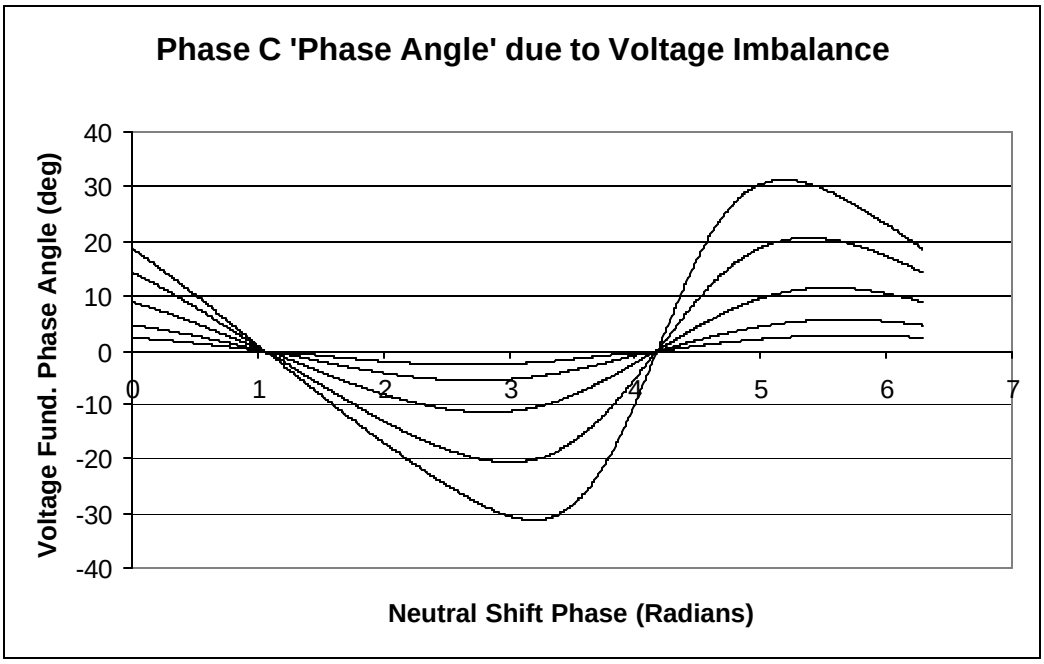

Figure 8.7. Phase angle error contribution for phase C due to voltage imbalance at 5%, 10%, 20%, 35% and 50% respectively.

Again, the previously three figures represent the angle Beta described in Figure 8.4. The angle and magnitude of the waveform shifted by the IADD is arbitrary in this case because of three phase averaging of the waveforms. As defined by the arctangent forcing function, deviation from a sinusoidal wave is exponential in nature.

Figure 8.8 shows average deviation from the nominal phase shift of five degrees. The smallest variations near the center line represent the limit defined by the IADD program as voltage imbalance. Variations in neutral shift as much as twenty percent show calculated phase variation less than five percent under these conditions.

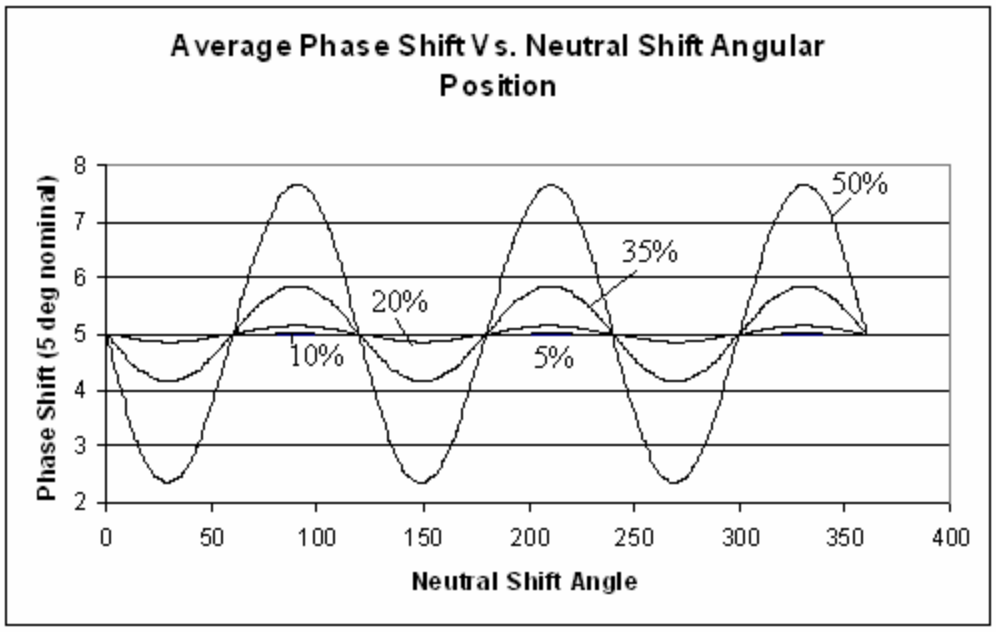

Figure 8.8. Phase angle error reduction due to averaging of 3 phase voltage imbalance at 5%, 10%, 20%, 35% and 50% respectively.

Variation in three phase average phase shift exhibits a third harmonic component as would be expected in a three phase system with non-linear response. This is obvious in Figure 8.8. In considering the case described in Figure 8.4, the percent error is given for a five degree phase shift in the second column of Table 8.1.

In normalizing the final result, the percent error is a function of the phase shift observed during testing. Once again, the magnitude of phase shift determines the accuracy of the IADD when there is no neutral bonding. Therefore, the absolute error due to neutral shift in any quadrant can be related to the percent loading condition previously investigated. Based on the results of this analysis, the error at an assumed limit of acceptable voltage imbalance is defined by Equation 8.8:

$$e = \frac{0.24\%}{\#\text{ of degrees observed phase shift}} \tag{8.8}$$

In equation 8.8, phase shift refers to the angle β induced when the neutral is allowed to float independent of the three phase voltage phasors.

Percent Imbalance	Maximum Percent Error from Nominal	Maximum Percent Error / Degrees
5%	0.05%	0.24%
10%	0.38%	1.92%
20%	3.10%	15.48%
35%	17.14%	85.70%
50%	53.29%	266.43%

Table 8.1. Percent error for a supposed five degree phase shift and normalized percent error per degree as a function of voltage imbalance and neutral shift.

Testing has been conducted at the Riggs Hall 480 V buss test site as described in Section 9.3 to further examine the effects of grounding on actual test results. Three series of tests have been conducted to examine three conditions:

Condition 1: The IADD has been connected to the four wire system presented in Figure 9.4, and the neutral of the resistive load bank has been connected to the system neutral. This serves as the base case for comparison.

Condition 2: The IADD has been connected to the four wire system without connecting the neutral of the load to the system neutral.

Condition 3: The IADD has been connected to the four wire system with the neutral connected and operating in extended mode.

	Condition 1 Bonded Load Neutral			Condition 2 Unbonded Load Neutral			Condition 3 Bonded Neutral Extended Mode Operation		
	Bolted Fault Current	*X/R Ratio*	*Incident Energy*	*Bolted Fault Current*	*X/R Ratio*	*Incident Energy*	*Bolted Fault Current*	*X/R Ratio*	*Incident Energy*
Mean	**8692.80**	**2.47**	**3.64**	**8394.43**	**2.54**	**3.53**	**8691.79**	**2.16**	**3.64**
Standard Error	102.80	0.03	0.04	102.78	0.04	0.04	66.08	0.02	0.03
Median	8671.12	2.53	3.63	8537.49	2.59	3.58	8678.11	2.15	3.63
Standard Deviation	471.07	0.14	0.18	471.01	0.19	0.18	302.84	0.10	0.12
Range	2154.13	0.57	0.83	1676.06	0.63	0.65	985.70	0.40	0.38
Minimum	7384.59	2.24	3.13	7375.38	2.17	3.13	8197.65	1.96	3.45
Maximum	9538.71	2.80	3.96	9051.44	2.80	3.78	9183.35	2.36	3.83
Confidence Level(95.0%)	214.428	0.066	0.082	214.402	0.088	0.083	137.850	0.044	0.053

Table 8.2. Statistical results of the three power circuit configurations described.

Table 8.2 presents statistical analysis of the first twenty one successful tests obtained using the IADD on the system described in Figure 9.4 under the described power circuit configurations.

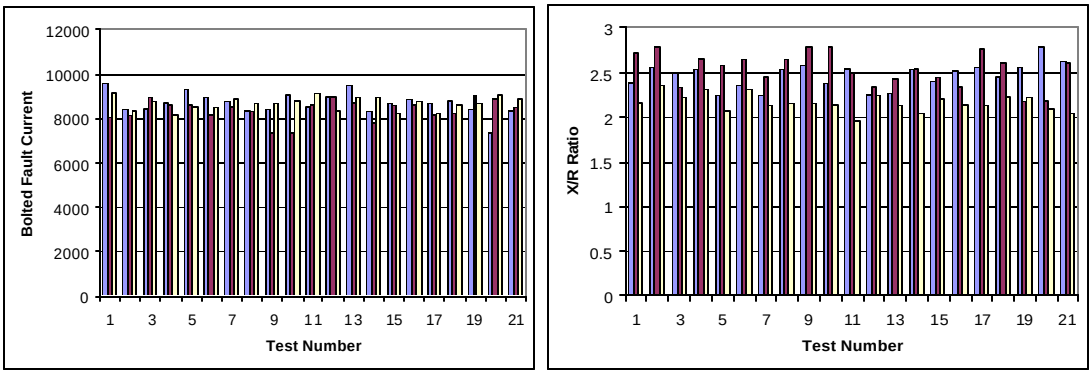

Figure 8.9. (a) Bolted fault current graphical results for conditional testing conducted in case 3 and (b) X/R ratio graphical results for conditional testing conducted in case 3.

A graphical distribution of results shows a high degree of repeatability in the bolted fault current estimation reported by the IADD under all testing conditions. Prior to implementing improved methods of phase shift calculation, variability of results generated by the IADD has been found to be much greater when multiple test sequences that were run as presented in Figure 7.6. Similarly, the X/R ratio results show a high degree of repeatability over the range of tests conducted.

The largest variation between test conditions is observed in the calculated X/R ratio reported. This calculation is highly sensitive to small variations in detected phase shift as is presented previously. The discrepancies noted between conditions 1, 2, and 3 can result if calculated impedance values differ by as little as 1 mΩ of power system impedance. The bonded system (condition 1) has an average detected phase shift of 0.8560 degrees. The un-bonded system (condition 2) has an average detected phase shift of 0.8886 degrees, and the IADD running in extended mode (condition 3) has an average detected phase shift of 1.6824 degrees. This result is expected when twice the current is drawn from the system, as it is predicted that approximately twice the phase shift should be observed given that the system is unchanged with respect to fault duty and X/R ratio. These results confirm that the system is consistently measuring phase shift between the conditions presented. Additional testing will be conducted on delta and ungrounded wye systems to determine the effects of grounding conditions on these system configurations as well.

8.4. Analysis of IADD Imposed Loading on Test Result Variability

In Chapter Four, it is stated that IADD test results and the resulting change in system parameters as measured by the IADD are expected to be dependent on the amount of current drawn. To quantify and prove this statement, tests have been conducted on the Riggs Hall 480 volt test site; site parameters are described in Section 9.3. For this test, a data sample of twenty one tests is conducted at various load conditions. These loading conditions are observed, because it has been noted that changes in IADD test result repeatability becomes more variable with reduced system loading.

The amount of power system loading by the IADD should have direct correlation with calculated results. As the system is more heavily loaded, the transients measured by the IADD to calculate bolted fault current and X/R ratio become more pronounced. It has also been shown that results are highly dependant on measuring phase shift during switching; thus, it creates a larger shift in phase by applying additional load to the system, which should reduce error and produce more stable results.

The transformer parameters presented in Chapter Nine yield a full load current by using the voltage and power ratings of the transformer:

$$\frac{S_{Base}}{V_{Base}} = \frac{500{,}000\ \text{VA}}{480\ \text{V}} = 1041.7\text{A} \tag{8.9}$$

The current values drawn for this test are presented in Table 8.3, and percent loading is calculated based on the full load current calculated in Equation 8.9.

IADD Current Drawn	Percent System Loading
65	6.24%
75	7.20%
87	8.35%
105	10.08%
130	12.48%
255	24.48%

Table 8.3. IADD test loading conditions and percent system load for a 500 kVA, 480 V transformer.

The method for quantifying IADD test variability has been chosen to be test sample standard deviation for the sampled bolted fault current, and X/R ratio data points have been taken at each current value. Standard deviation is chosen as a means

of variability measurement, because it is easily calculated, well understood, and generally accepted as a good measure of data distribution. As stated before, each sample consists of the first twenty one successful test sequences observed and recorded by the IADD.

Figure 8.10 presents the results of this analysis. As expected, test variability has a direct correlation with system loading conditions. As the load on the system is increased, results become increasingly stable. Unfortunately, the limitations of the IADD in its present state preclude testing at higher loading conditions, but it is expected that test precision is not significantly improved above twenty five percent loading. At twenty five percent loading, three percent voltage drop is observed for the system tested. This should be well tolerated by even sensitive loads present at the point of testing, proving that the IADD can be used to produce precise data sets and test critical systems even when under power.

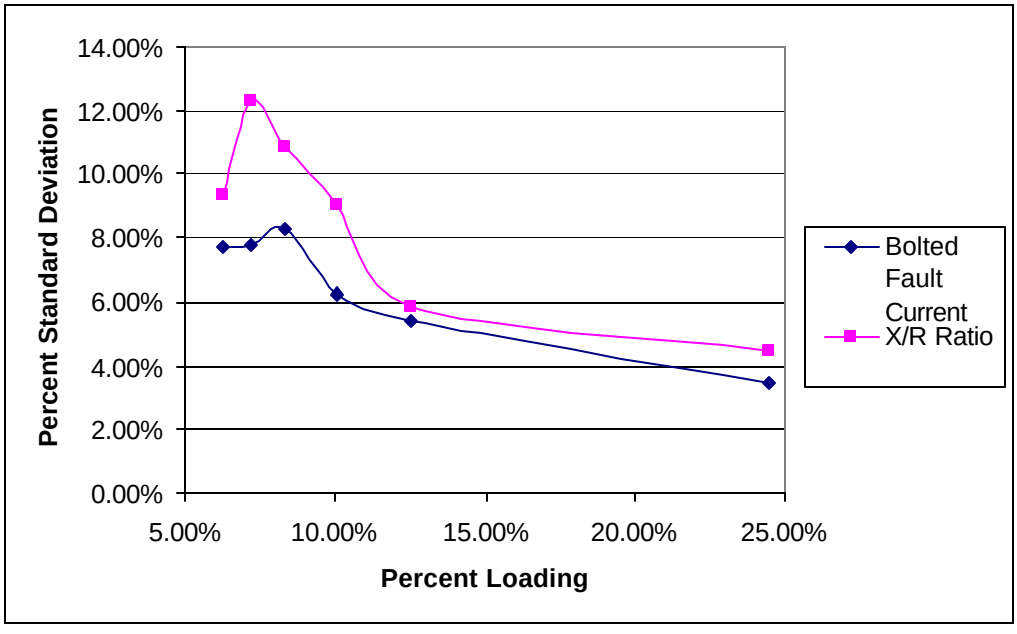

Figure 8.10. Test variability as a measure of sample data standard deviation for various loading conditions.

To complete this analysis, bolted fault current and X/R ratio data is averaged for each set of test data under the previously discussed loading conditions and presented in Figure 8.11. The figures show that, with averaging, the calculated bolted fault current and X/R ratio is generally invariant with respect to the amount of load current drawn during testing. Therefore, while precision is dependant on the loading condition of the IADD, accuracy through averaging is not greatly dependant. Observed voltage drop will not be dependant on the loading condition and is a function of the power system parameters at the point of testing.

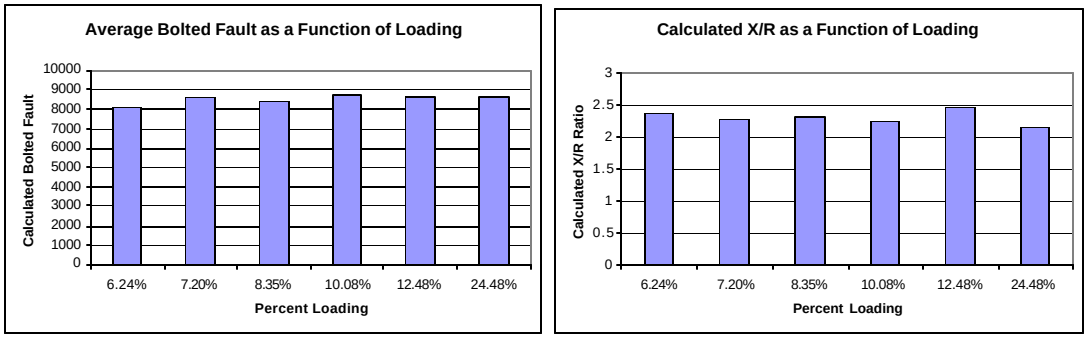

Figure 8.11. (a) average calculated bolted fault current and (b) average calculated X/R ratio for various loading conditions.

CHAPTER 9

CASE STUDIES

Chapter Nine will present several case studies that demonstrate the ability of the IADD to accurately predict bolted fault current. This is presented through several different methods of verification. Through estimation of the power system parameters, taking into consideration the prime contributors to impedance, the IADD will prove to provide realistic results in estimating bolted fault current and ultimately arc flash incident energy as defined in the IEEE 1584 standard. Initial testing and verification has been conducted in the PQIA lab in Riggs Hall, Clemson University. Similar results are presented in real world testing and through other accepted fault current availability calculations, such as voltage rise due to addition of capacitance (capacitor voltage rise testing).

9.1. Case 1: Riggs Hall 208V Test Site

Upon completion of initial tests to determine viability of concept, the first IADD prototype has been constructed in the PQIA laboratory. Riggs Hall is supplied power through a 500 kVA, 12.47 kV/208 V Forced Oil Cooled (FOC) delta-wye transformer. The nameplate data on the transformer is given as 500 kVA, 12.47 kV-208/120Y V, with an impedance value of 5.66%. From industry tables for transformers of this type and size, the X/R ratio for this transformer is approximately 3.71. [14] The service impedance feeding the transformer is considered negligible because of the extremely high fault duty reported by university officials at the primary side of the

transformer. The 12.47 kV fault duty for the Riggs Hall transformer is reported as 9,780 amps at the high voltage terminals of the transformer.

The specific test site for trials is the main power panel feeding the laboratory. The panel is fed by a four-wire 4/0 cable run of approximately 100 feet from switchgear in the transformer room. Wire is run through three inch aluminum thin-wall conduit that is solidly bonded at both ends. Tests are made in the panel by connecting to a spare 20 amp over-current breaker rated for 10 kA interrupting current.

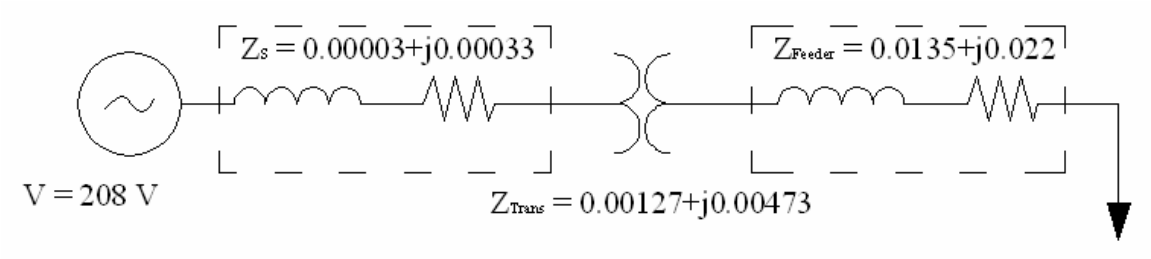

Figure 9.1. Riggs Hall test site wiring diagram.

It is important to note here that this test has been performed during the early stages of the IADD development. Phase shift algorithms are less robust, and non-linear transformers are used as the method of voltage detection. This case is presented as a demonstration of how averaging can further reduce errors.

AWG	Resistance /1000 ft	Reactance /1000 ft
8	0.78	0.052
4/0	0.067	0.041

Table 9.1. Selected impedance values for 4/0 copper wire in conduit, source: NEC-2000, table 9.

$$Z_{base} = \frac{208^2}{500000} = 0.086528 \text{ Ohms} \tag{9.1}$$

$$\left|Z_{Transformer}\right| = Z_{Base} \times 0.0566 = 0.0048975 \text{ Ohms} \tag{9.2}$$

$$0.0048975 = \sqrt{(3.71 * R_{Trans})^2 + R_{Trans}^2} \rightarrow R_{Trans} = 0.0012745 \text{ Ohms} \quad (9.3)$$

$$X_{Trans} = \sqrt{(0.0048975^2 - 0.0012745^2} \rightarrow X_{Trans} = 0.004728 \text{ Ohms} \quad (9.4)$$

$$Z_{Trans} = 0.0012746 + j0.004728 \text{ Ohms} \quad (9.5)$$

$$Z_{Line} = \frac{120\,ft}{1000\,ft} \times (0.067 + j0.041) = 0.00804 + j0.00492 \text{ Ohms} \quad (9.6)$$

$$Z_{System} = Z_{Trans} + Z_{Line} = 0.009315 + j0.009648 \text{ Ohms} \quad (9.7)$$

$$X / R = 1.036 \quad (9.8)$$

$$Z_{Lead} = \frac{15\,ft}{1000\,ft} \times (0.78 + j0.052) = 0.0117 + j0.00078 \text{ Ohms} \quad (9.9)$$

$$Z_{Total} = Z_{System} + Z_{Lead} = 0.0210 + j0.01042 \text{ Ohms} \quad (9.10)$$

$$I_{bf} = \left| \frac{120}{0.0210 + j0.01042} \right| = 5115 \text{ Amps} \quad (9.11)$$

where, I_{bf} is bolted fault current for three phase faults (symmetrical RMS) (kA)

A test has been conducted at the Riggs Hall test location in which twenty five random samples have been taken over the course of one hour. The results of the test yield positive results in terms of approximating the fault current magnitudes expected for a bolted fault. From the tests conducted using the IADD, the average bolted fault current value is 3792 amps with an error from the expected value of 3.6 percent. The minimum reported value for the population is 2316 amps, and the maximum reported value for the population is 5022 amps. The 95% confidence interval for the mean is 298 or 7.8%, which is an acceptable value for the goals of the project.

The X/R ratio is calculated to be 1.036. The reported average X/R ratio is 0.849, a lower value than expected, due to the wire and breaker impedance.

Riggs Hall Test Site Summary
208V

	Bolted Fault Current	*X/R Ratio*
Mean	3791.68	0.8486
Standard Error	144.2298	0.0839
Median	3813	0.759
Standard Deviation	721.149	0.4194
Range	2706	1.688
Minimum	2316	0.212
Maximum	5022	1.9
Confidence Level (95.0%)	297.6757	0.1731

Table 92. Case 1 test results after implementation of continuous FFT windowing for phase shift monitoring.

To complete this study, the incident energy is examined. These equations come from IEEE 1584 that are presented in Chapter Five. Some assumptions are made in this example to give a final numerical result. These assumptions are stated in IEEE 1584 as standard values and working conditions for typical installations under 1000 volts. The typical working distance is 455 mm (18 in.) for panel work. The typical gap spacing between conductors is 25 mm (1 in.). The Riggs Hall test location is considered an enclosed panel or MCC, and the nominal system voltage is 208 volts.

$$\log I_a = -0.097 + 0.39343 + 0.0201 + 0.01315 + 0.06908 - 0.045167 = 0.35359 \quad (9.12)$$

$$\text{kA } I_a = 10^{\log I_a} = 2.2573 \text{ kA} \quad (9.13)$$

$$\log E_n = -0.555 - 0.113 + 1.081 \times 0.35359 + 0.0011 \times 25 = -0.25827 \quad (9.14)$$

$$E_n = 10^{\log E_n} = 0.551734 \tag{9.15}$$

$$E = (1.5)(10^{0.5517})\left(\frac{0.05}{0.2}\right)\left(\frac{610^{1.641}}{455^{1.641}}\right) = 1.965\,\text{cal/cm}^2 \tag{9.16}$$

From the previous assumptions made, a worker would sustain second degree burns from an arc sustained for 50 ms (three cycles) while standing 18 inches from the electrical panel. This panel would be rated as a category one safety hazard as defined by the NFPA 70E document. Under these conditions, the worker would be required to wear a flame retardant shirt and pants in addition to any other PPE normally mandated in an industrial environment. Of course, this does not mean that the panel is clear to work in without observing standard safety procedures, and injury may still occur to the hands, which may be closer than the specified working distance used in the equations. Sturdy leather or rubber gloves should still be worn to prevent possible injury.

Test results, as presented in Figure 9.3, demonstrate marked improvement in data repeatability in terms of both bolted fault duty and X/R ratio calculations obtained during concept development. Results obtained at the site 1 test location prior to implementing continuous FFT sampling of phase angle (see Section 7.3) are presented in Figure 9.2. Results at the same test location after implementing continuous monitoring of phase angle change (see Section 7.4) are presented in Figure 9.3.

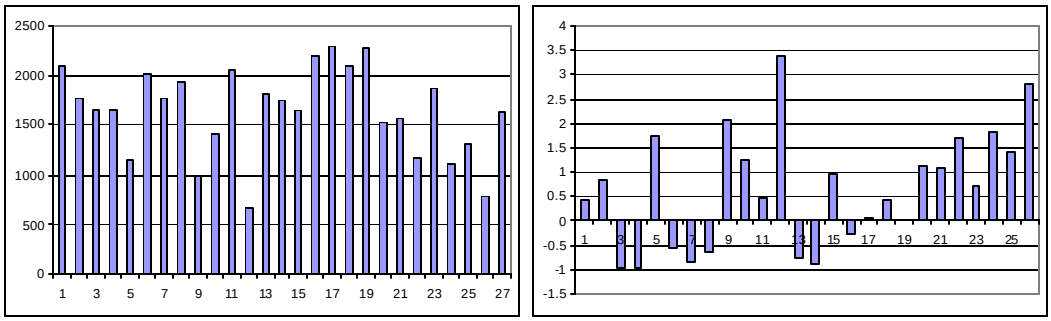

Figure 9.2. Riggs Hall 208V test site (a) bolted fault current and (b) X/R ratio results prior to implementation of continuous FFT phase angle monitoring.

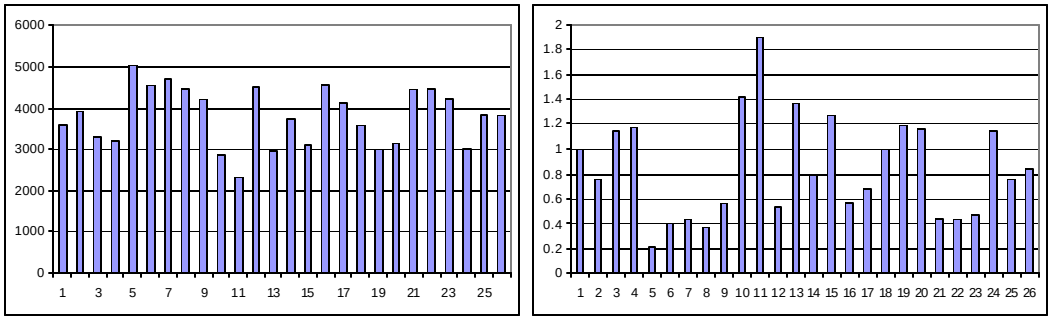

Figure 9.3. Riggs Hall 208V test site (a) bolted fault current and (b) X/R ratio results after implementation of continuous FFT phase angle monitoring.

Additional steps to improve repeatability are described in Chapter Seven and Chapter Eight, including averaging of three phase data points to reduce error due to random fluctuations in the electrical power system under transient and load shifting conditions.

9.2. Case 2: Mooresville Water Treatment Plant, Mooresville, NC Test Site

This test has been conducted at the municipal water treatment plant in Mooresville, NC. The system impedance and transformer nameplate data has been supplied by Randy Emanuel, representing Duke Energy.

The nameplate data on the transformer is given as 750 kVA, 12.47 kV-480/277Y V, with an impedance value of 5.32%. From industry tables for transformers of this type and size, the X/R ratio for this transformer is approximately 3.44. [12] The

system impedance feeding the transformer has been reported as 0.6608+j2.27 ohms. The 12.47 kV fault duty on the primary side of the transformer is reported as 5,274 amps.

$$Z_{base} = \frac{12470^2}{100000000} = 1.555 \text{ Ohms} \tag{9.17}$$

$$Z_{System} = 0.6608 + j2.27 \text{ Ohms} \tag{9.18}$$

Now, the power base is changed reflecting the VA rating of the transformer:

$$Z_{System}' = Z_{System} \times \frac{750{,}000}{100{,}000{,}000} = 0.004956 + j0.01705 \text{ Ohms} \tag{9.19}$$

$$Z_{Transformer} = 0.003072 + j0.01327 \text{ Ohms} \tag{9.20}$$

$$Z_{Total} = Z_{System}' + Z_{Transformer} = 0.008028 + j0.03032 \text{ Ohms} \tag{9.21}$$

During this test, a 21 foot, 8 AWG, copper lead is used:

$$Z_{Lead} = \frac{21\,ft}{1000\,ft} \times (0.78 + j0.052) = 0.01638 + j0.001092 \text{ Ohms} \tag{9.22}$$

$$Z_{Test} = Z_{Total} + Z_{Lead} = 0.024409 + j0.03141 \text{ Ohms} \tag{9.23}$$

$$I_{bf} = \left| \frac{277}{0.024409 + j0.03141} \right| = 6.962 \text{ kA} \tag{9.24}$$

where, I_{bf} is bolted fault current for three phase faults (symmetrical RMS) (kA).

$$X / R = 1.2869 \tag{9.25}$$

A statistical analysis of the results of this test is presented in Table 9.3.

Mooresville Test Site Summary

	Bolted Fault Current	*X/R Ratio*	*Incident Energy*
Mean	5955.552442	2.540232558	6.393953488
Standard Error	661.1125358	0.769091385	0.655296093
Median	4117.366	2.462	4.63
Standard Deviation	4335.204811	5.043269474	4.297063848
Range	16165.27	23.664	15.875
Minimum	1374.484	-8.828	1.683
Maximum	17539.754	14.836	17.558
Confidence Level (95.0%)	1334.179096	1.552089233	1.32244104

Table 9.3. Case 2 test results.

Case two is evaluated prior to implementation of cycle-by-cycle FFT algorithm for evaluating phase shift. Therefore, averaging is implemented to reduce random noise, as in case one. Additional tests are conducted to test the revised measurement scheme.

9.3. Case 3: Riggs Hall 500 kVA, 480 V Test Site

The case three test site is also located in the sub-basement of Riggs Hall. A 500 kVA, 12.47 kV/480 V transformer is located outside of Riggs Hall and feeds the sub-basement 480 volt electrical distribution buss exclusively. These facts make this source particularly stable and immune to load variation and harmonic distortion typically seen on the Riggs Hall building system.

The transformer feeds the 480 volt buss via two parallel runs of 250 kcmil stranded copper wire estimated at 150 feet in length. The IADD interfaces the buss through a blade type disconnect switch and runs seven feet to a line reactor rated at 600 V, 87 amps. An additional twenty feet of AWG 8 wire connects the reactor to the IADD.

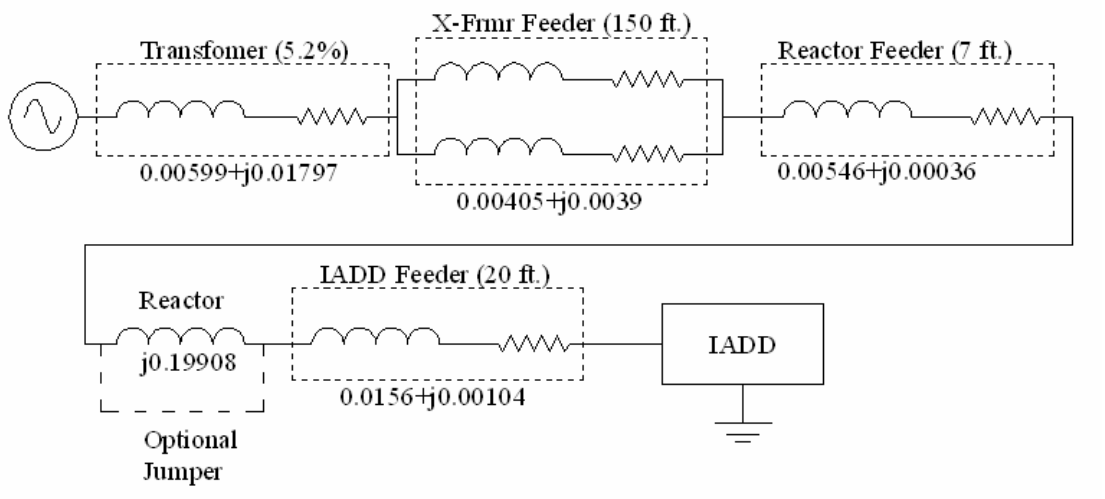

Figure 9.4. Case 3 system diagram illustrating system impedances

Since the IADD implements compensation for lead length, the impedance designated as "IADD Feeder" can be ignored. First, a baseline test is performed on the system with a jumper around the reactor bank as shown in the Figure 9.4.

$$Z_{System} = Z_{Transformer} + Z_{T-Feeder} + Z_{R-Feeder} = 0.0155 + j0.02223\,\text{Ohms} \tag{9.26}$$

$$I_{bf} = \left| \frac{271.9}{0.0155 + j0.02223} \right| = 10.03\,\text{kA} \tag{9.27}$$

$$X/R = 1.43 \tag{9.28}$$

A statistical analysis of the results of this test is presented in Table 9.4.

Riggs Hall Test Site Summary

	Standard Mode (175A)			Extended Mode (250A)		
	Bolted Fault Current	*X/R Ratio*	*Incident Energy*	*Bolted Fault Current*	*X/R Ratio*	*Incident Energy*
Mean	**8692.80**	**2.47**	**3.64**	**8691.79**	**2.16**	**3.64**
Standard Error	102.80	0.03	0.04	66.08	0.02	0.03
Median	8671.12	2.53	3.63	8678.11	2.15	3.63
Standard Deviation	471.07	0.14	0.18	302.84	0.10	0.12
Range	2154.13	0.57	0.83	985.70	0.40	0.38
Minimum	7384.59	2.24	3.13	8197.65	1.96	3.45
Maximum	9538.71	2.80	3.96	9183.35	2.36	3.83
Confidence Level (95.0%)	214.42773	0.065821	0.082145	137.8497	0.043806	0.053043

Table 9.4. Case 3 test results without reactor in series.

The jumper is then removed, and the reactor bank is placed in series. In two different configurations, parameters of the reactor are measured during testing to obtain the actual impedance, Z, of the reactor.

Test 1

IADD Observed Results		Reactor Parameters		Calculated Results	
Measured reactor voltage drop:	2.52	R	X	Calculated change due to Addition of Reactor based on observed voltage drop	
Observed current:	132	0.00697	0.017773		
Reactor impedance Z:	0.019091	Estimated Total Resultant Z:		Sys Impedance	0.0497
Observed X/R Ratio:	**2.55**	0.018049	0.046307	X/R Ratio	**2.565656**
Observed Power System Z:	0.0183+i0.0467			Bolted fault current	**5507.757**
Observed Bolted Fault Current:	**5468**				
Test Measured Parameters Current and Voltage and IADD reported I_{bf} and X/R					

Test 2 (Reactor Reconfigured)

IADD Observed Results		Reactor Parameters		Calculated Results	
Measured reactor voltage drop:	14.75	R	X	Calculated change due to Addition of Reactor based on observed voltage drop	
Observed current:	130	0.02366	0.110967		
Reactor impedance Z:	0.113462	Estimated Total Resultant Z:		Sys Impedance	0.143761
Observed X/R Ratio:	**4.69**	0.034739	0.139501	X/R Ratio	**4.01566**
Observed Power System Z:	0.0183+i0.0467			Bolted fault current	**1904.085**
Observed Bolted Fault Current:	**1935.5**				
Test Measured Parameters Current and Voltage and IADD reported I_{bf} and X/R					

Table 9.5. Case 3 test results with reactor in series in varying configurations

These tests confirm very stable and predictable results with little variation from test to test. The tests are also conducted at two different current levels and similar results are seen in both cases. Discrepancies in results have initially been attributed to unaccounted resistances in the connections, estimated wire run from the transformer to the switching station, molded case switch, and buss work. The power system short circuit availability is reported to be 9,780 amps at the high voltage terminals of the transformer.

Because of distortion in the voltage waveform due to flux saturation in the magnetic core of the reactor bank, the actual X/R ratio of the reactor is indeterminate.

The observed X/R ratio is used to define the parameters of the reactor in both cases; therefore, conclusions regarding X/R ratio could not be verified at this time. However, the tests conclusively prove that by adding additional known impedance, the IADD accurately predicts a change in bolted arc fault current due to a known load condition change.

9.4. Case 4: Modena Street, Gastonia, NC Test Site

The Modena Street location has been selected, because it provides safe access to the power system through disconnected capacitor banks. After connecting the IADD to the system at the capacitor bank terminals, a capacitor rise test could then be performed to determine the available fault duty at the buss by using voltage rise calculations. The following information is provided by Duke Power about the buss characteristics:

1. The average three phase voltage at the line side terminals prior to switching in the capacitor bank is measured to be 490.5 volts.
2. The average three phase voltage at the line side terminals after switching in the capacitor bank is measured to be 506.8 volts.
3. The three phase average current drawn is measured to be 820 amps.

$$V_{Rise} = \frac{(506.4 - 490.5)}{490.5} = 3.24\% \tag{9.29}$$

$$KVA_{Capacitor} = \frac{\sqrt{3} \times 506.4 \times 820}{1000} = 719.2 \text{ KVar} \tag{9.30}$$

The capacitor kVar rating is converted to a per unit value on a 100 MVA base as follows:

$$\%Z_{Total} = \frac{3.24 \times 100000}{719.2} = 451\% \tag{9.31}$$

$$KVA_{3q-Fault} = \frac{10000000}{451} = 22172.9 \text{ KVA} \tag{9.32}$$

$$I_{3q-Fault} = \frac{22172.9 \times 1000}{\sqrt{3} \times 490.5} = 26099 \text{ A} \tag{9.33}$$

The following results were obtained during testing of the IADD under several conditions:

Modena Street Test Summary

Bolted Fault Current Statistics	*120A*	*175A*	*250A*	*350A*
Mean	**24703.07068**	**27387.16**	**28457.77211**	**26833.3998**
Standard Error	1654.622892	1513.388448	1961.679254	2293.03327
Median	27739.131	29104.678	30398.918	29872.7025
Standard Deviation	**7212.333975**	**7257.956026**	**8550.761628**	**10254.75653**
Range	21018.394	23617.543	29172.172	31579.975
Minimum	12234.641	11943.684	10266.254	11508.431
Maximum	33253.035	35561.227	39438.426	43088.406
Confidence Level (95.0%)	**3476.233696**	**3138.575529**	**4121.335174**	**4799.37378**

Table 9.6. Statistical results of test conducted at Modena Street distribution site, Gastonia, NC.

The results presented in Table 9.6 closely match the expected fault duty based on the calculations provided by Duke Power when averaged over all test samples. However, there is variation in the calculations that is reflected in the standard deviation for the samples collected. This is found to be due to the configuration of the power system and limitations of the IADD at the time of testing. The system being measured is an ungrounded wye system with a floating neutral point. This has been discussed in detail in Chapter Seven. Plans have been created to configure the IADD to take measurements in both delta and wye configurations, presumably eliminating the variation seen due to the floating neutral. See Chapter Ten for details.

9.5. Case 5: Tuscarora Yarns, Greenville, NC Test Site

The Tuscarora Yarns Inc, test site has been selected for similar reasons as is noted in Case 4. The Tuscarora site includes an installed 750 kVAr capacitor back that can be connected to the IADD safely, prior to connecting to the buss. After connecting the IADD to the system at the capacitor bank terminals, a capacitor rise test is performed to determine the available fault duty at the buss by using voltage rise calculations. The results of this test are shown in Figure 9.5.

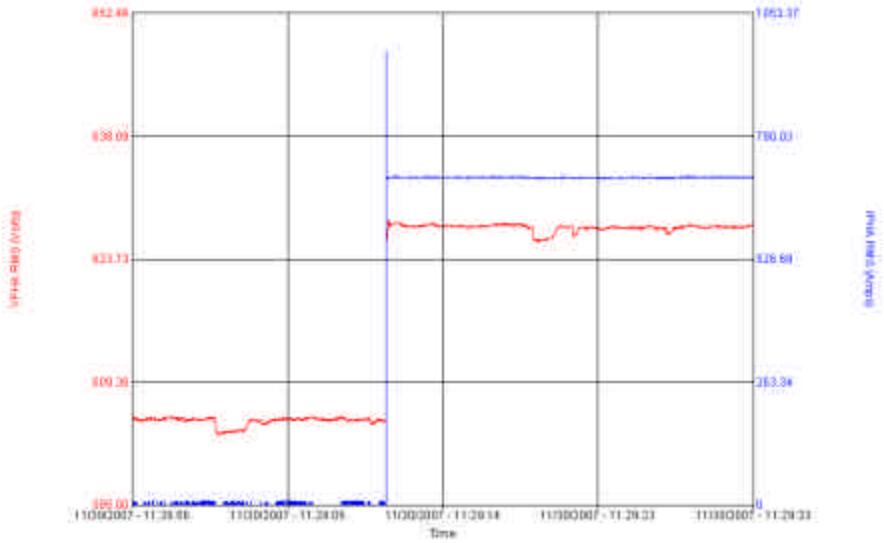

Figure 9.5. Tuscarora capacitor bank rise RMS voltage and current data.

Data during the test rise was captured using a PA-9 Plus power analyzer. Using this data, a measurement of the power system fault availability can be calculated as follows:

$$V_{Boost} = \frac{V_{Rise} - V_{Nominal}}{V_{Nominal}} = \frac{627.6 - 604.83}{604.83} = 3.76\% \tag{9.34}$$

$$CAP_{kVAr} = \frac{\sqrt{3} \times V_{Rise} \times I_{Cap}}{1000} = \frac{\sqrt{3} \times 627.6 \times 700}{1000} = 760.9 \tag{9.35}$$

$$Z_{P.U.} = \frac{V_{Boost} * 100000}{CAP_{kVAr}} = \frac{3.76 * 100000}{760.9} = 494.1\% \tag{9.36}$$

$$KVA_{3-PhaseFault} = \frac{S_{Base}}{Z_{P.U.}} = \frac{10000000}{494.1} = 20237\,kA \tag{9.37}$$

$$I_{3-PhaseFault} = \frac{20237 \times 1000}{\sqrt{3} \times 604.83} = 19318\,kA \tag{9.38}$$

Tests are now conducted with the IADD to verify these results. During this field trial, an equipment malfunction occurred in the data acquisition system and prohibited collection of data reported by the IADD. However, RMS data was collected using the same PA-9 as was used to conduct the capacitor rise test calculations. No information on phase angle is captured with the PA-9, however, some analysis can be performed. Figure 9.6 depicts some of the results using RMS values

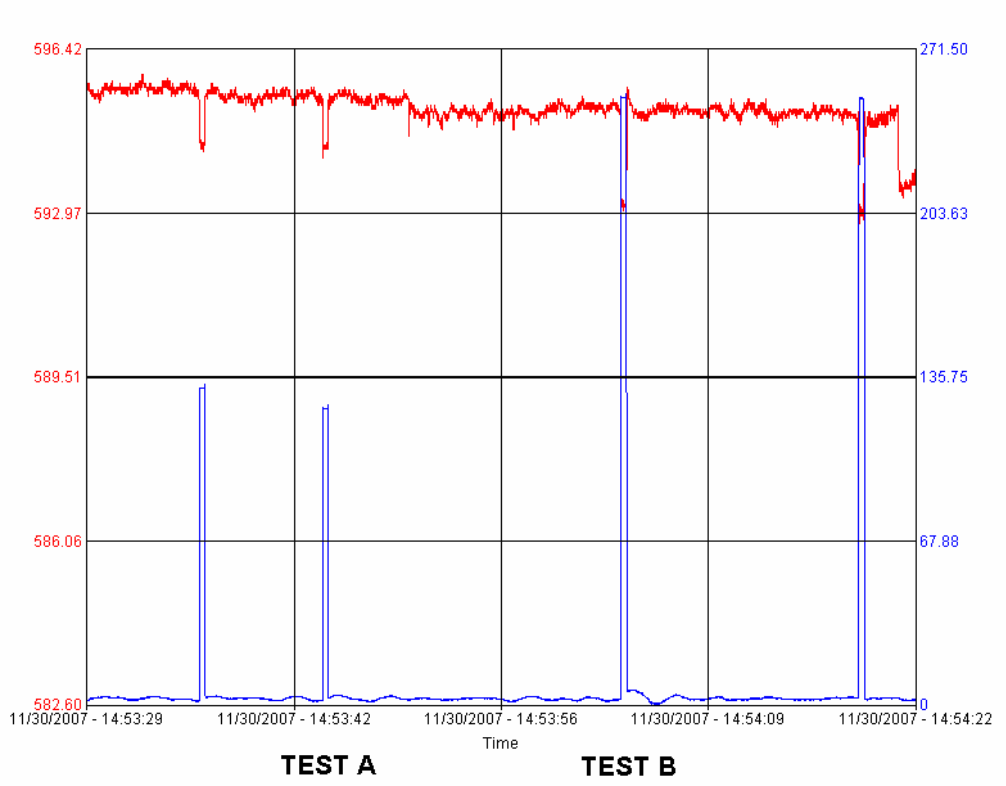

Figure 9.6. Tuscarora site IADD induced RMS voltage and current data.

During each test interval, a corresponding dip in voltage is observed due to loading by the IADD. Calculations are performed by applying Equations 5.1 to determine the bolted fault current and assuming no phase shift was observed.

For Test A, I_{test} = 122.83 A:

$$Z_{PowerSystem} = \frac{\left[\left(\frac{595.36}{\sqrt{3}}\right) - \left(\frac{594.45}{\sqrt{3}}\right)\right]}{122.83} = 0.004277 \text{ ohms} \quad (9.39)$$

$$I_{bolted\text{-}fault} = \frac{\left(\frac{595.36}{\sqrt{3}}\right)}{0.004277} = 80.36 \text{ kA} \quad (9.40)$$

For Test B, I_{test} = 251.46 A:

$$Z_{PowerSystem} = \frac{\left[\left(\frac{595.04}{\sqrt{3}}\right) - \left(\frac{593.22}{\sqrt{3}}\right)\right]}{251.46} = 0.004179 \text{ ohms} \quad (9.41)$$

$$I_{bolted\text{-}fault} = \frac{\left(\frac{595.04}{\sqrt{3}}\right)}{0.004179} = 82.21 \text{ kA} \quad (9.42)$$

In both cases, neglecting phase shift results in a calculated bolted fault current of four times the measured value when performing the capacitor rise test. In Section 8.1, an analysis is presented that proves that phase shift, or X/R ratio, significantly effects bolted fault current. The ability to observe and measure voltage phase shift is critical to the operation of the IADD and the correct values using any type of load test. To better analyze the test results taken at the Tuscarora site, Equation 9.39 is modified to vary measured phase angle. The results are presented in Figure 9.7.

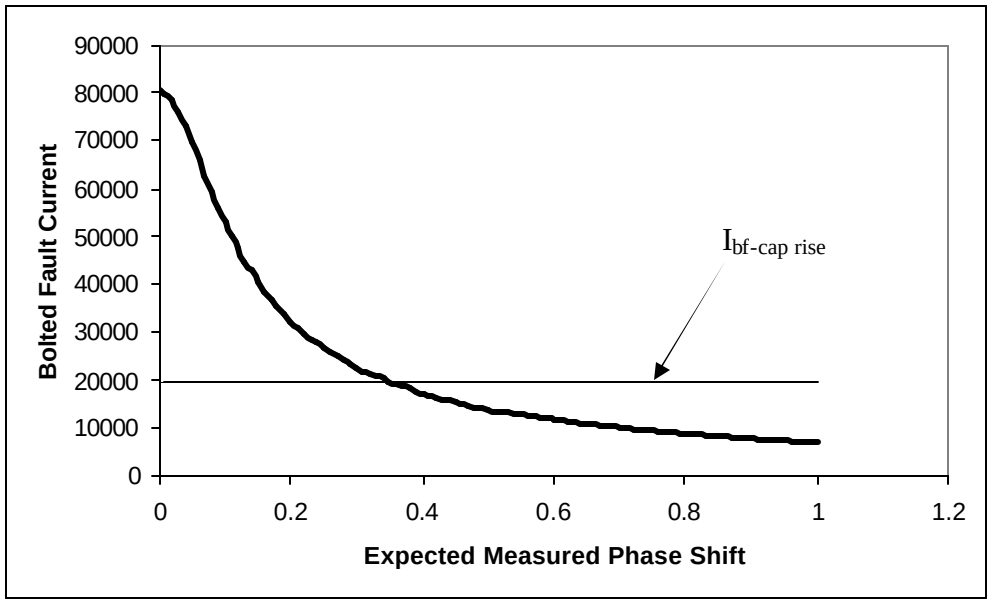

Figure 9.7. Bolted fault current calculations versus observed phase shift in degrees.

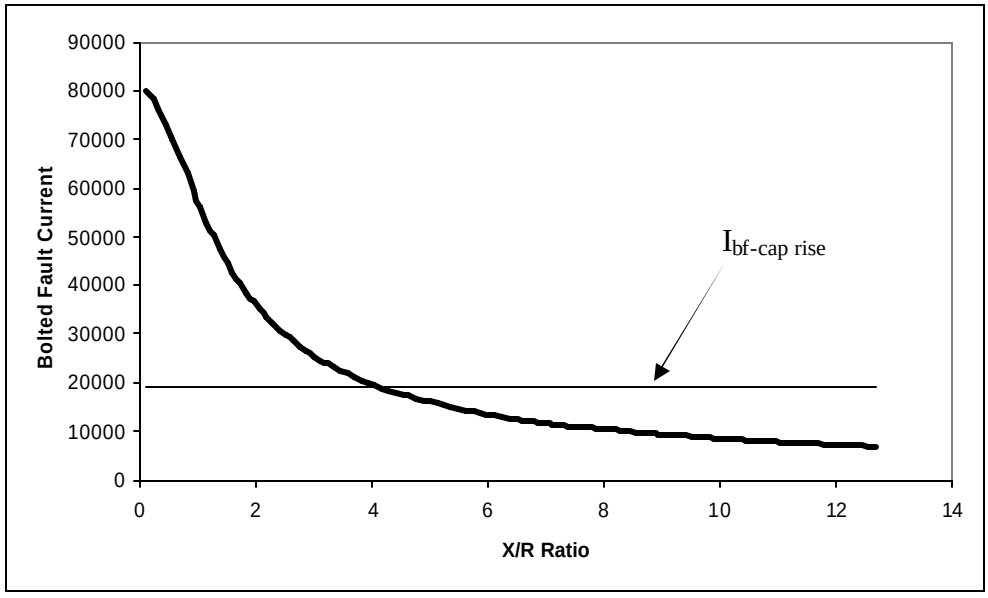

Figure 9.8. Bolted fault current calculations versus calculated X/R ratio.

Figure 9.7 illustrates how measured phase angle affects the bolted fault current reported by the IADD. The flat line represents the bolted fault current calculated during the capacitor rise test presented in Figure 9.5. The point of intersection corresponds to the solution to Equation 9.39 if a phase shift of 0.34 degrees is observed. Note that graphs in figure 9.7 and 9.8 appear nearly identical. This results because

there is a direct correlation between phase angle and X/R ratio as was discussed in Section 8.1. The relationship between observed phase shift angle and X/R ratio remains linear until about an X/R ratio of 12.

An X/R ratio of approximately four results in a bolted short circuit fault current identical to that calculated for the capacitive rise test. This X/R ratio is generally accepted as typical at distribution level service entrances.

This test serves to exemplify the importance of accurately measuring and applying voltage phase shift to the RMS voltage waveform to obtain actual bolted fault current at the point of measurement. Note how sensitive the fault current is to accurate phase angle measurement. Without the development of algorithms to process and compensate for small variations in the voltage waveforms induced by the IADD, a realistic bolted fault current value could not be realized. And, reporting a realistic bolted fault current is critical to correctly gauging the hazard level that workers are exposed to when working on energized equipment.

CHAPTER 10

FUTURE DEVELOPMENT AND APPLICATIONS

Chapter Ten outlines future development and other foreseeable uses for the IADD. Development, as presented in this thesis, is the completion of phase one of the proposed devolvement for this device. The function of the device is to obtain data to make a determination on bolted fault capacity and to determine an equivalent X/R ratio for the given system at the test point. Testing and development for phase two of this project has already been proposed.

10.1. Future Hardware Development

In the current design, resistance must be user selected through the LabView front panel interface by selecting one of four pre-determined resistor bank configurations. This provides a balanced load that will draw a manageable current while simultaneously providing sufficient load to the power system such that a measurable reduction in voltage and phase shift is observed. Future development of the system includes automation of the resistance selection procedure through the use of adaptive program algorithms that will automatically conduct a series of tests and determine the optimal load to be applied to the system for measurement with the IADD.

Additional investigation into using other loads such as capacitors and/or inductors will be conducted. The possibility of using a user supplied load, such as an existing motor installation to implement testing will be further considered and tested to determine feasibility. Induction motors with high initial loads provide dynamically

changing impedance that, at starting, is very low and similar to the tests currently performed with the resistive elements. By taking advantage of an existing motor load, the size of the IADD could conceivably be greatly reduced in size and cost.

Studies on resistor power rating and heat dissipation should be conducted to investigate the ability to reduce total size of the IADD by using smaller resistive load banks. The load banks chosen were sized initially large for testing purposes and allow for several successive test cycles without the need to cool the resistor coils by any other method than natural convection. It is conceivable that, by using forced air cooling, resistor bank size could be reduced considerably; duty cycle time between successive tests may increase if resistor power rating is reduced.

Forced air cooling of the resistor coils can be implemented by the addition of low cost electric fans. These fans are available and are most commonly used in large computer server applications. They are powered by the same 120 volt supply that powers the computer and power supply that drives the Hall Effect CTs.

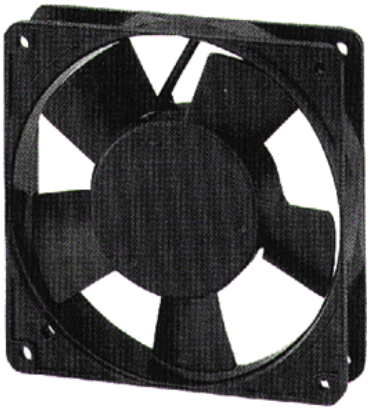

Figure 10.1. 120V, 2000 RPM, 120mm, 105 cubic feet/minute (CFM) muffin style cooling fan for proposed cooling of resistor banks.

The CT chosen in initial designs operate on +/- 15 volts (DC) by using a single 30 volt (DC) switching power supply. While this solution is functional, future designs would use +/- 5 volts (DC) Hall Effect current transformers and take advantage of computer power supply outputs to operate the CTs.

Wireless mouse and keyboard components are considered as upgrades to the system because they reduce wires from the work surface to the computer terminal, mounted on the lower level of the device. While offering no performance enhancements to the system, they offer a cleaner look to the device. Some consideration should be taken in using these components in inherently electrically noisy environments as the signals may be distorted or not picked up by the receiver.

Additional hardware will be implemented to observe neutral to ground voltage and neutral current. This will also serve a duel purpose if the IADD is used as a power quality meter. Excessive neutral currents can be used as a software trigger to inform the user of voltage imbalance or grounding problems.

10.2. Future Software Development

The initial stages of development focus on determining the three-phase balanced equivalent circuit at the point of testing. If all the phases are balanced, then the results will be very close to the actual fault duty value. However, in practical situations, the system may not be perfectly balanced. Additionally, loads present on the system could be imbalanced such as single phase motors. This could add further downstream imbalance when considering regenerating loads and cause the fault duty of each phase to be different. Future iterations may take this imbalance into consideration by loading all three-phases and analyzing each phase individually. In this thesis, computations on

unbalanced systems and system loads are not discussed, but are within the capability of the device.

Software changes can be implemented to automate the monitoring of voltage and current imbalance. One method of imbalance detection is presented here, based on the mathematical variance of the three incoming voltage and current RMS values. Suppose voltages V_1, V_2, and V_3 are reported as the voltages for phases A, B, and C respectively. Taking the variance of these three values can be used to define a threshold for voltage imbalance; the same can be applied to current values. Suppose these calculations on a base voltage of 120 volts, and a maximum excursion of +/-5% is deemed acceptable for two phases. Let $V_1 = V_2 = 114$ and $V_3 = 120$.

$$AVG(V_1, V_2, V_3) = \overline{V} = \frac{114 + 114 + 120}{3} = 116 \tag{10.1}$$

$$VAR(V_1, V_2, V_3) = \frac{\sum (V_n - \overline{V})^2}{(n-1)} = \frac{(114-116)^2 + (114-116)^2 + (120-116)^2}{2} = 12 \tag{10.2}$$

$$AVG(V_1, V_2, V_3) / V_{BASE} = 116/120 = AVG_{SCALED} = 0.9667 \tag{10.3}$$

$$\frac{VAR(V_1, V_2, V_3)}{(AVG_{SCALED})^2} = V_{Unbalance-factor-\max} = 12.18145 \tag{10.4}$$

$$\text{If } V_{Unbalance-factor} > 12.18145, \tag{10.5}$$

then the voltage is deemed unbalanced, and a notice is displayed on the front panel GUI informing the user of possible test errors due to imbalance. This method is used because different voltage levels are used with the IADD and must have a voltage base scaling factor. Based on the voltage base chosen, the decision threshold varies.

Automation of the testing procedure will be implemented in the second phase of development. It is envisioned that, after connecting the IADD to a test node, the user would begin the testing process and passively monitor the system as the IADD conducts a bank of tests. Conducting several tests at one location will reduce variability in the final rating and can supply information on the variability of the test location to changes in the power system with respect to fault duty. The testing should be done in a pseudo-random fashion to avoid correlating the response to any cyclic loads that may affect the final results.

Automation of the relaying scheme presented in Figure 4.3 to choose the correct impedance value to obtain a desired voltage drop will be implemented. Software will be written to perform a series of experimental tests using successively decreasing impedance values until the observed voltage drop reaches a predetermined value.

Additional software safeguards, such as under-voltage alarming, may be implemented in the event that testing causes the voltage to sag below a pre-set limit below the Pre-Test voltage. If a severe sag in the RMS voltage is detected during testing, the IADD would immediately end the test sequence and alert the user to take appropriate action. Calibration of the detection threshold may require calibration during testing to insure that an error is not reported due to voltage depressions intentionally imposed by the IADD.

During testing with the line reactor described in case three, some anomalous readings were observed. These anomalies were attributed to saturation in the core of the inductors. Such saturation could lead to error in the calculations implemented by the IADD, because the equations assume a linear system with sinusoidal response.

Saturation of the core would cause a non-linear response in the current waveforms measured at the IADD. Further, these non-linearities in current may be transposed to the voltage waveform, because the load is resistive in nature.

A method of detecting current and voltage distortion due to core saturation or any other undetermined sources can be implemented in the IADD programming by examining each phase of the input current and voltage waveforms during the portion of the test when current is being conducted through the load bank. Using the FFT analysis tool previously discussed in Chapter Seven, a measure of total harmonic distortion (THD_i and THD_v) may be implemented to determine if significant current or voltage distortion is present in the incoming waveforms. A trigger level determining the maximum allowable amount of waveform distortion must be established, and additional user warning may be implemented on the front panel of the program. It should be noted, as was discussed in Chapter Four and exhibited in Figure 4.5a, that a certain amount of distortion is inherent due to the physical construction of the IADD. This distortion is a result of crossover distortion during change of conduction path in the solid state relays. A nominal value for current distortion to account for this phenomenon must be noted when establishing a decision threshold on acceptable current distortion.

10.3. Additional Applications for the IADD

With knowledge of the effective impedance at a test node, several applications of the IADD become apparent:

1. Capacitor/Filter bank studies
2. Motor/Drive studies
3. Power Quality studies

Sizing of capacitor banks often requires a site study to find electrical system parameters in an effort to mitigate resonances that may occur and are typical in RLC circuits. Sometimes these studies do not take all factors into account, and resonances occur anyway. This situation can result in costly additional expenses to design, build, and install filter units to correct for resonance. As a device to determine possible resonance issues by examining the effective system impedance at the proposed installation site, the use of the IADD can help mitigate some of these expenses. This device can also provide capacitor bank designers with a more accurate model of the effective impedance when designing capacitor banks or filters.

In installations involving large motor/drives, the input impedance can be important for several reasons. Motor starting has an adverse effect on power quality, particularly at sites that are at the end of a long feeder and are considered "weak." Motor starts can cause large dips in the voltage (so-called "flicker") because of the reduced impedance of the motor during speed-up. Knowledge of the upstream impedance at a potential installation site would help in designing and sizing the proper protective and compensative equipment to combat this problem.

Using the PCI-6123 card, the IADD has the ability to become a power quality (PQ) monitor. PQ monitors have already been developed using LabView software, and one such monitor is commercially available from APNA group. [16] By replacing the current inputs with standard clamp-on style CTs, the IADD could be used as a PQ monitor, adding functionality to the device.

CHAPTER 11

CONCLUSION

In this thesis, a device dubbed as the IADD is developed and described in detail. The importance and necessity of arc flash assessments are first introduced, supplying the reader with background information on OSHA requirements, NFPA 70E, and IEEE 1584 standards. The difficulties inherent in these assessments are made relevant. Also, a discussion of how an assessment is prepared, and a survey of possible alternative methods is presented.

The IADD presents a method of performing arc flash assessment testing in a manner that yields nearly instantaneous results. Moreover, connection and testing can be performed on energized circuits without interrupting service to other loads on the circuit. This feature clearly sets this device apart from other devices of a similar nature. Current methods of performing these assessments are both time consuming, costly, and require disconnecting the test location from the rest of the system to insert a testing device. The IADD eliminates the need to perform a detailed analysis of the electrical system and accounts for regenerating loads and cable lengths that may be impossible to accurately model.

The basic principles of operation for the IADD are explained, giving background detail on how voltage and phase angle change with a change in load. This point is noted with the demonstration of a test system in which an additional resistive load modeling the IADD is introduced into a system operating in steady-state with

constant linear loads. A change in both voltage magnitude and phase angle are both seen when the additional load is injected into the system.

Details of the physical construction of the device are presented, along with wiring diagrams, photos, and data sheets for parts used in the IADD. The device utilizes a load bank typically used in regenerative breaking. The device also integrates solid state relays as a means of load switching, and a National Instruments PCI-6123 data acquisition card to read voltage and current waveforms as well as supply control signals to the switches.

Software has been developed using LabView in conjunction with the PCI-6123 card. The algorithms used in the operation of the IADD are presented, and an explanation of operation is offered. The IADD determines the bolted fault current expected at the test location and uses this information, along with some user specified variables, to determine the arc flash incident energy exposure. This value is subsequently used to define the NFPA arc flash category number used to select the proper PPE required when work on energized equipment is necessary. Screenshots of the IADD front panel GUI are shown to introduce the reader to the look and feel of the program from a user's perspective.

Several case studies are presented, and comparisons were made between the observed results given by the IADD and those calculated using the NEC handbook. The results of these tests conclude that the IADD can consistently determine bolted fault current. Additional testing has been performed at several field locations, giving further proof of accurate and precise results. The bolted fault current results are verified by applying several different calculation methods.

Finally, future plans for the IADD in terms of hardware and software upgrades are proposed and several other possible applications for this device are presented.

11.1. Epilogue

Development of this device has been a great personal learning experience for me. Challenges have presented themselves at every point during this project and often times, solutions were not found for weeks or months at a time. What seems like a very simple concept turns out to be extremely difficult to realize when you start with a blank canvas. By far, phase shift detection and determination has been the most difficult concept to understand and account for throughout the development of the process. With the requirement of fully understanding two variables, voltage magnitude variation and phase shift, observation of voltage magnitude change is trivial when compared with the difficulties of developing an algorithm to pick out minute variations in the phase angle of a dynamic signal. I have struggled with the development of this device over the course of the past eighteen months and continue to make improvements on the IADD all the time. Through the efforts to create this device and writing this thesis, I hope to improve safety for all and reduce the chance of people being seriously injured by electricity. Thank you.

NOTES

APPENDICES

Appendix A – Interpretation of NFPA 70E by OSHA [17]

This is an excerpt from the OSHA website, classified as an interpretation of OSHA standards regarding compliance with the regulations set forth in NFPA 70E. This correspondence was held between James Brown of Associated General Contractors of Indiana and Russell Swanson, Directorate of Construction for OSHA. 07/25/2003 - General Duty Clause (5(a)(1)) citations on multi-employer worksites; NFPA 70E electrical safety requirements and personal protective equipment.

Question (2) – James Brown:

I note that OSHA has not incorporated the personal protective equipment portions of NFPA 70E by reference in §1910.132 (personal protective equipment, general requirements) or §1910.335 (safeguards for personal protection). Does an employer have an obligation under the General Duty Clause to ensure that its own employees comply with personal protective equipment requirements in NFPA 70E?

Answer – Russell Swanson, OSHA:

These provisions are written in general terms, requiring, for example, that personal protective equipment be provided "where necessary by reason of hazards..." (§1910.132(a)), and requiring the employer to select equipment "that will protect the affected employee from the hazards...." (§1910.132(d)(1)). Also, §1910.132(c) requires the equipment to "be of safe design and construction for the work performed."

Similarly, §1910.335 contains requirements such as the provision and use of "electrical protective equipment that is appropriate for the specific parts of the body to be protected and the work to be performed (§1910.335(a)(i)).

Industry consensus standards, such as NFPA 70E, can be used by employers as guides to making the assessments and equipment selections required by the standard. Similarly, in OSHA enforcement actions, they can be used as evidence of whether the employer acted reasonably.

Under §1910.135, the employer must ensure that affected employees wear a protective helmet that meets either the applicable ANSI Z89.1 standard or a helmet that the employer demonstrates "to be equally effective." If an employer demonstrated that NFPA 70E contains criteria for protective helmets regarding protection against falling objects and electrical shock that is equal to or more stringent than the applicable ANSI Z89.1 standard, and a helmet met the NFPA 70E criteria, the employer could use that to demonstrate that the helmet is "equally effective."

Appendix B – Selected Portions of NFPA 70E [4] and IEEE 1584 [6]

(A) Flash Protection Boundary. For systems that are 600 volts or less, the Flash Protection Boundary shall be 4.0 ft, based on the product of clearing times of 6 cycles (0.1 second) and the available bolted fault current of 50 kA or any combination not exceeding 300 kA cycles (5000 ampere seconds). For clearing times and bolted fault currents other than 300 kA cycles, or under engineering supervision, the Flash Protection Boundary shall alternatively be permitted to be calculated in accordance with the following general formula:

$$D_c = \left[2.65 \times MVA_{bf} \times t\right]^{1/2} \tag{B.1}$$

or

$$D_c = \left[53 \times MVA \times t\right]^{1/2} \tag{B.2}$$

where,

D_c is distance from an arc source for a second-degree burn (feet)

MVA_{bf} is bolted fault capacity available at point involved (mega volt-amperes)

MVA is the capacity rating of transformer (mega volt-amperes). For transformers with MVA ratings below 0.75 MVA, multiply the transformer MVA rating by 1.25

t is time of arc exposure (seconds)

At voltage levels above 600 volts, the Flash Protection Boundary is the distance at which the incident energy equals 5 J/cm^2 (1.2 cal/cm^2). For situations where fault clearing time is 0.1 second (or less), the Flash Protection Boundary is the distance at which the incident energy level equals 6.24 J/cm^2 (1.5 cal/cm^2).

(1)	(2) Limited Approach Boundary[1]	(3)	(4) Restricted Approach Boundary[1]; Includes Inadvertent Movement Adder	(5)
Nominal System Voltage Range, Phase to Phase	Exposed Movable Conductor	Exposed Fixed Circuit Part		Prohibited Approach Boundary[1]
Less than 50	Not specified	Not specified	Not specified	Not specified
50 to 300	3.05 m (10 ft 0 in.)	1.07 m (3 ft 6 in.)	Avoid contact	Avoid contact
301 to 750	3.05 m (10 ft 0 in.)	1.07 m (3 ft 6 in.)	304.8 mm (1 ft 0 in.)	25.4 mm (0 ft 1 in.)
751 to 15 kV	3.05 m (10 ft 0 in.)	1.53 m (5 ft 0 in.)	660.4 mm (2 ft 2 in.)	177.8 mm (0 ft 7 in.)
15.1 kV to 36 kV	3.05 m (10 ft 0 in.)	1.83 m (6 ft 0 in.)	787.4 mm (2 ft 7 in.)	254 mm (0 ft 10 in.)
36.1 kV to 46 kV	3.05 m (10 ft 0 in.)	2.44 m (8 ft 0 in.)	838.2 mm (2 ft 9 in.)	431.8 mm (1 ft 5 in.)
46.1 kV to 72.5 kV	3.05 m (10 ft 0 in.)	2.44 m (8 ft 0 in.)	965.2 mm (3 ft 2 in.)	635 mm (2 ft 1 in.)
72.6 kV to 121 kV	3.25 m (10 ft 8 in.)	2.44 m (8 ft 0 in.)	991 mm (3 ft 3 in.)	812.8 mm (2 ft 8 in.)
138 kV to 145 kV	3.36 m (11 ft 0 in.)	3.05 m (10 ft 0 in.)	1.093 m (3 ft 7 in.)	939.8 mm (3 ft 1 in.)
161 kV to 169 kV	3.56 m (11 ft 8 in.)	3.56 m (11 ft 8 in.)	1.22 m (4 ft 0 in.)	1.07 m (3 ft 6 in.)
230 kV to 242 kV	3.97 m (13 ft 0 in.)	3.97 m (13 ft 0 in.)	1.6 m (5 ft 3 in.)	1.45 m (4 ft 9 in.)
345 kV to 362 kV	4.68 m (15 ft 4 in.)	4.68 m (15 ft 4 in.)	2.59 m (8 ft 6 in.)	2.44 m (8 ft 0 in.)
500 kV to 550 kV	5.8 m (19 ft 0 in.)	5.8 m (19 ft 0 in.)	3.43 m (11 ft 3 in.)	3.28 m (10 ft 9 in.)
765 kV to 800 kV	7.24 m (23 ft 9 in.)	7.24 m (23 ft 9 in.)	4.55 m (14 ft 11 in.)	4.4 m (14 ft 5 in.)

Table B.1. Approach boundary to live parts for shock protection. Source: NFPA 70E, table 130.2(C). [10]

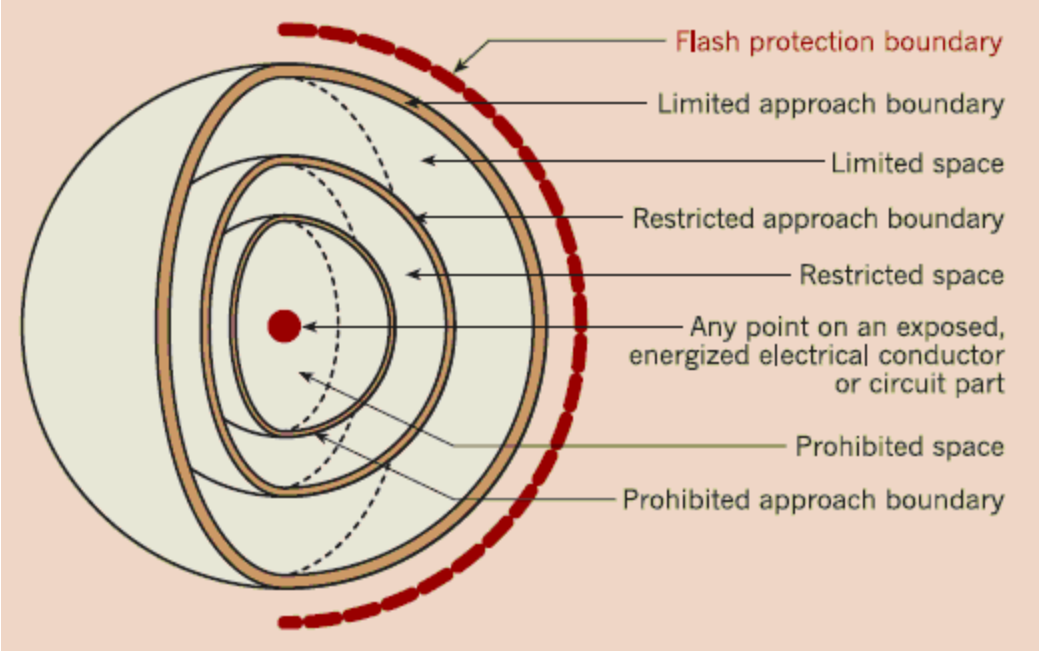

Figure B.1. Limits of approach graphic. Source: NFPA 70E, figure C.1.2.4. [10]

Protective Clothing and Equipment	Protective Systems for Hazard/Risk Category					
Hazard/Risk Category Number	**−1 (Note 3)**	**0**	**1**	**2**	**3**	**4**
Non-melting (according to ASTM F 1506-00) or Untreated Natural Fiber						
a. T-shirt (short-sleeve)	X			X	X	X
b. Shirt (long-sleeve)		X				
c. Pants (long)	X	X	X (Note 4)	X (Note 6)	X	X
FR Clothing (Note 1)						
a. Long-sleeve shirt			X	X	X (Note 9)	X
b. Pants			X (Note 4)	X (Note 6)	X (Note 9)	X
c. Coverall			(Note 5)	(Note 7)	X (Note 9)	(Note 5)
d. Jacket, parka, or rainwear			AN	AN	AN	AN
FR Protective Equipment						
a. Flash suit jacket (multilayer)						X
b. Flash suit pants (multilayer)						X
c. Head protection						
1. Hard hat			X	X	X	X
2. FR hard hat liner					AR	AR
d. Eye protection		—	—	—	—	—
1. Safety glasses	X	X	X	AL	AL	AL
2. Safety goggles				AL	AL	AL
e. Face and head area protection		—	—	—	—	—
1. Arc-rated face shield, or flash suit hood				X (Note 8)		
2. Flash suit hood					X	X
3. Hearing protection (ear canal inserts)				X (Note 8)	X	X
f. Hand protection			—	—	—	—
Leather gloves (Note 2)			AN	X	X	X
g. Foot protection						
Leather work shoes			AN	X	X	X

AN = As needed
AL = Select one in group
AR = As required
X = Minimum required

Table B.2. Protective Clothing and Personal Protective Equipment (PPE) Matrix, Source: NFPA 70E, table 130.7(C)(10). [4]

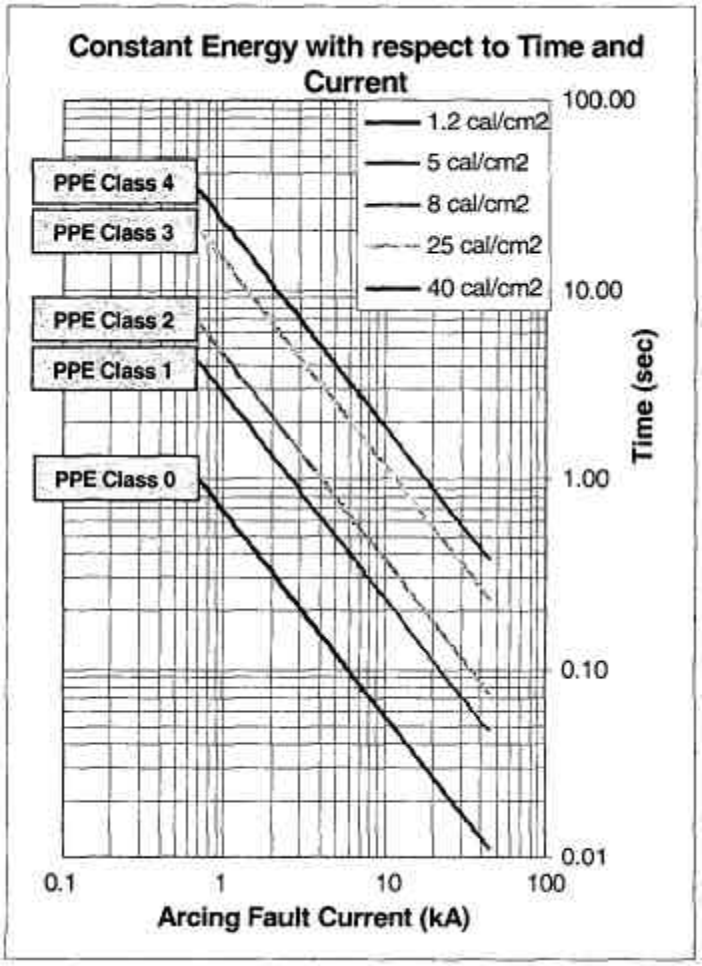

Figure B.2. OSHA PPE requirement chart, current vs. time. [17]

System voltage (kV)	Equipment type	Typical gap between conductors (mm)	Distance *x* factor
0.208–1	Open air	10–40	2.000
	Switchgear	32	1.473
	MCC and panels	25	1.641
	Cable	13	2.000
>1– 5	Open air	102	2.000
	Switchgear	13–102	0.973
	Cable	13	2.000
>5–15	Open air	13–153	2.000
	Switchgear	153	0.973
	Cable	13	2.000

Table B.3. Factors for equipment and voltage classes. Source: IEEE-1584, table 4. [6]

Appendix C – Additional Hardware Documentation

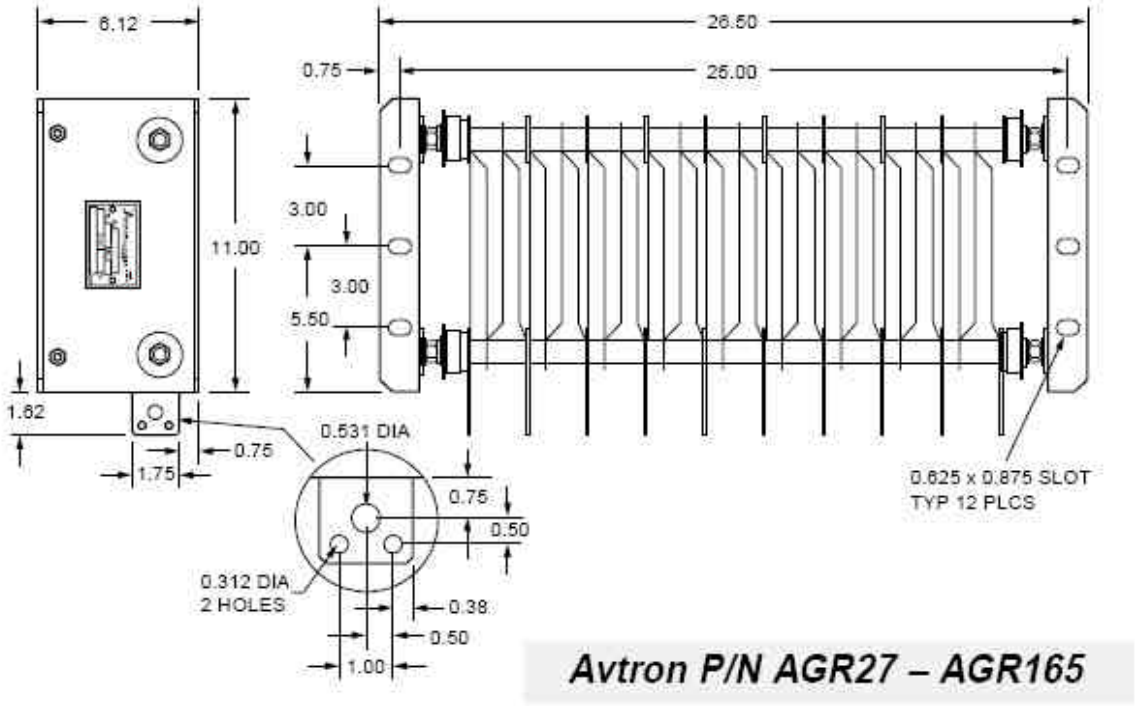

Figure C.1. Avtron grid resistor dimensional diagram

Specifications Measured at 25°C, RL-10KΩ, Vcc=±15V

Specification		L03S050D15	L03S100D15	L03S200D15	L03S300D15	L03S400D15	L03S500D15	L03S600D15
Nominal Primary DC Current	(If)	50AT	100AT	200AT	300AT	400AT	500AT	600AT
Maximum Current	$If_{(max)}$	±150AT	±300AT	±600AT	±700AT	±700AT	±700AT	±700AT
Output Voltage @ If	V_{OUT}	4V						
Offset Voltage	V_{OE}	<± 40mV	<±30mV					
Accuracy @ If[2]	X	±1% of If						
Output Linearity[2] (0..If MAX)	E_L	±1% of If						
Power Supply	V_{CC}	±15V±5%						
Response Time	t_r	<5μ Sec						
Current Consumption	Ic	12mA typ						
Output Temperature Characteristic	TCE_G	<±0.1% / °C						
Offset Temperature Characteristic	V_{OT}	<±2mV / °C	<±1mV / °C					
Hysteresis Allowance @ If=0	V_{OH}	±30mV			±20mV		±10mV	
Withstand Voltage (50/60Hz)	V_d	2,500VACrms for 1 minute (sensing current 0.5mA)						
Insulation Resistance @ 500VDC	R_S	≥500MΩ						
Operating Bandwidth[1] (-3dB)	f	DC - 50kHz						
Operating Temperature	T_A	-10 - +80°C						
Storage Temperature	T_S	-15 - +90°C						

[1] Small signal only; derating needed to avoid excessive core heating at high frequency

[2] Without offset

Table C.1. Tamura Hall effect current transformer electrical specifications.

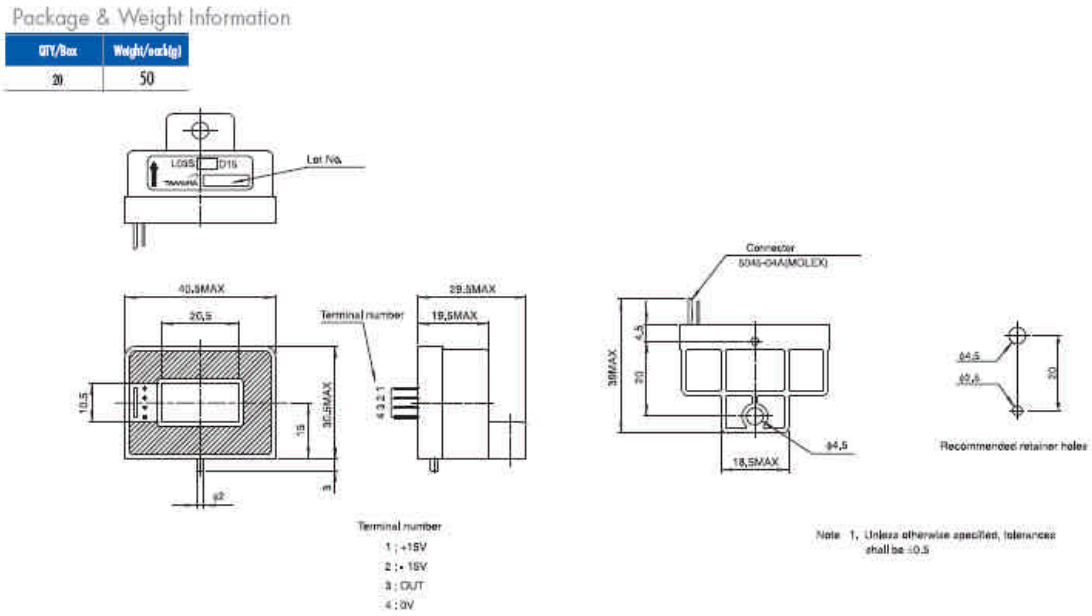

Figure C.2. Tamura Hall effect current transformer physical layout.

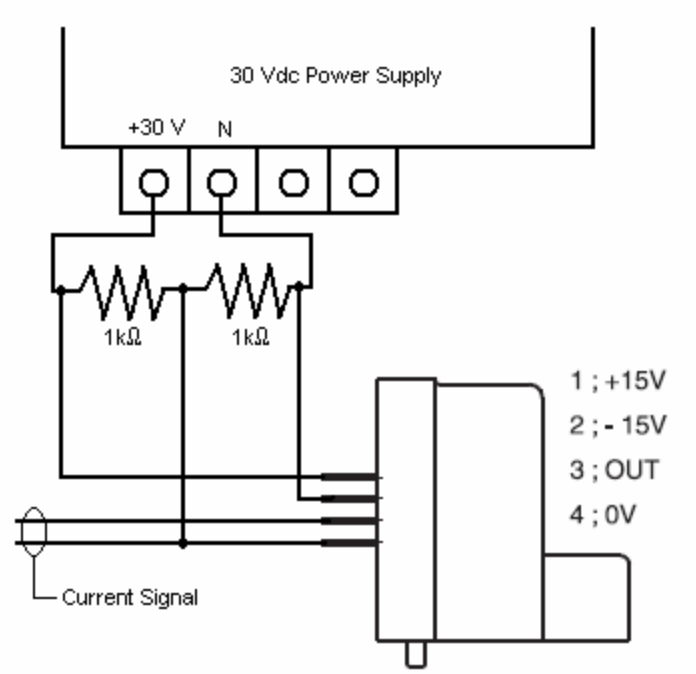

Figure C.3. Current transformer wiring diagram

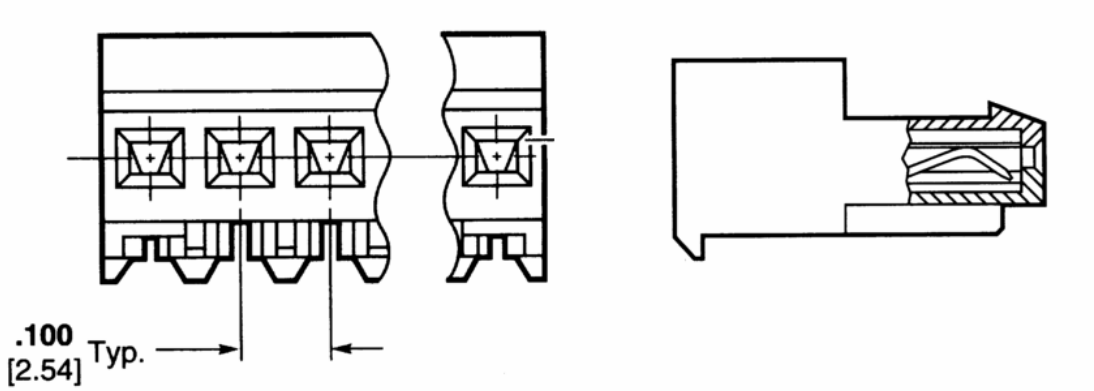

Figure C.4. 4-pin connectors used to interface CTs, switching power supply, and DAQ card

MODEL NUMBERS	AC CONTROL	HA6025	HA6050	HA6090	HA60125
	DC CONTROL	HD6025	HD6050	HD6090	HD60125
OUTPUT SPECIFICATIONS ①					
Nominal Line Voltage (±10%) [Vrms]		600	600	600	600
Operating Voltage Range (47-63 Hz) [Vrms]		48-660	48-660	48-660	48-660
Max. Load Current ③ [Arms]		25	50	90	125
Min. Load Current, [mArms]		40	40	40	150
Transient Overvoltage [Vpk]		1200	1200	1200	1200
Max. Surge Current, (16.6ms) [Apk]		250	625	1,200	1,750
Max. On-State Voltage Drop @ Rated Current [Vpk]		1.7	1.7	1.7	1.7
Thermal Resistance Junction to Case ($R_{\theta JC}$) [° C/W]		1.02	0.63	0.28	0.22
Maximum I^2t for Fusing, (8.3 msec.) [A^2sec]		260	1,620	6,000	12,700
Max. Off-State Leakage Current @ Rated Voltage [mArms] ⑦		5	5	5	5
Min. Off-State dv/dt @ Max. Rated Voltage [V/µsec] ②		500	500	500	500
Max. Turn-On Time ⑤		1/2 Cycle (DC Input), 10.0 msec (AC Input)			
Max. Turn-Off Time		1/2 Cycle (DC Input), 40.0 msec (AC Input)			
Power Factor (Min.) with Max. Load		0.5	0.5	0.5	0.5

INPUT SPECIFICATIONS ①	DC CONTROL (D PREFIX)	AC CONTROL (A PREFIX) ④	AC CONTROL (E SUFFIX)
Control Voltage Range	3-32 Vdc	90-280 Vrms (60Hz)	18-36 Vrms
Max. Reverse Voltage	-32 Vdc	---	---
Max. Turn-On Voltage	3.0 Vdc	90 Vrms	18 Vrms
Min. Turn-Off Voltage	1.0 Vdc	10 Vrms	4.0 Vrms
Nominal Input Impedance	See Note ⑥	60K Ohms	9.0K Ohms
Typical Input Current	2.0 mA⑥	2mA @ 120 Vrms, 4mA @ 240 Vrms	3mA @ 24 Vrms

Table C.2. Crydom solid state relay electrical specifications.

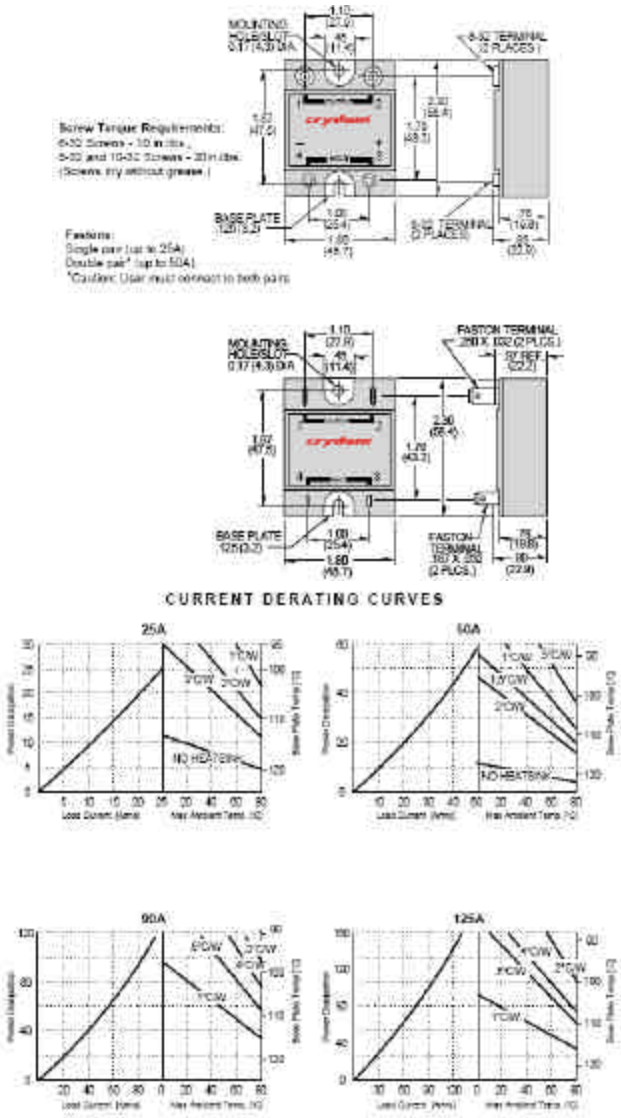

Figure C.5. Crydom re lay physical layout (top) and current derating curves (bottom).

Appendix D – Sample Test Results File

Time/Date	Test Number	Average Prefault Voltage	Average Prefault Current	Average Infault Voltage	Average Infault Current	Bolted Fault Current	X/R Ratio	Average Phase Shift	Incident Energy	Test Resistance
7/12/2007 17:50	1	273.76	0.19	268.63	132.92	8982.6	2.447	0.851	3.767	2.021
7/12/2007 17:51	2	273.91	0.13	268.84	133.70	8959.5	2.639	0.866	3.760	2.011
7/12/2007 17:51	3	273.60	0.16	268.52	133.29	8726.0	2.659	0.886	3.667	2.015
7/12/2007 17:51	4	273.59	0.19	268.32	133.40	8872.2	2.273	0.856	3.723	2.011
7/12/2007 17:53	5	273.73	0.20	268.66	133.64	8906.5	2.652	0.871	3.737	2.010
7/12/2007 17:53	6	273.74	0.16	268.70	133.36	9168.5	2.600	0.844	3.838	2.015
7/12/2007 17:53	7	273.70	0.16	268.48	133.34	8939.0	2.322	0.852	3.750	2.014
7/12/2007 17:53	8	273.67	0.18	268.64	133.11	8927.6	2.671	0.867	3.745	2.018
7/12/2007 17:53	9	273.67	0.18	268.57	133.22	8826.6	2.564	0.873	3.706	2.016
7/12/2007 17:53	10	273.66	0.20	268.56	132.96	8891.1	2.543	0.864	3.731	2.020
7/12/2007 17:54	11	273.64	0.17	268.52	133.18	9049.1	2.476	0.849	3.791	2.016
7/12/2007 17:54	12	273.47	0.12	268.50	132.89	9403.7	2.635	0.823	3.926	2.021
7/12/2007 17:54	13	273.62	0.12	268.62	133.22	9124.6	2.679	0.850	3.820	2.016
7/12/2007 17:54	14	273.79	0.18	268.75	133.02	8756.7	2.704	0.883	3.680	2.020
7/12/2007 17:54	15	273.76	0.14	268.69	133.28	8758.4	2.665	0.883	3.681	2.016
7/12/2007 17:55	16	273.86	0.16	268.79	132.97	8773.2	2.642	0.879	3.687	2.021
7/12/2007 17:55	17	273.79	0.11	268.68	133.18	9011.7	2.498	0.853	3.779	2.017
7/12/2007 17:55	18	273.75	0.18	268.67	132.82	8897.8	2.562	0.863	3.734	2.023
7/12/2007 17:55	19	273.84	0.16	268.77	133.16	8931.3	2.612	0.865	3.748	2.018
7/12/2007 17:55	20	274.02	0.11	268.87	132.85	8571.1	2.553	0.894	3.611	2.024
7/12/2007 17:56	21	273.96	0.19	268.82	133.17	9032.6	2.439	0.848	3.788	2.019
7/12/2007 17:56	22	273.76	0.23	268.70	132.98	8879.1	2.637	0.869	3.727	2.021
7/12/2007 17:56	23	273.58	0.19	268.66	133.27	9110.7	2.900	0.859	3.814	2.016
7/12/2007 17:56	24	273.70	0.20	268.63	133.19	9301.5	2.487	0.827	3.889	2.017
7/12/2007 17:57	25	273.79	0.20	268.74	132.88	8831.0	2.665	0.874	3.709	2.022

Enclosure Variable1	Enclosure Variable2	Grounding Variable	Distance Exponent	Gap Distance(in)	Arc Time(s)	Distance from Arc(in)
-0.097	-0.555	-0.113	1.641	1	0.2	18

Table D.1. Sample test data file in *.csv format, taken from Riggs Hall sub-basement 480V remote connection.

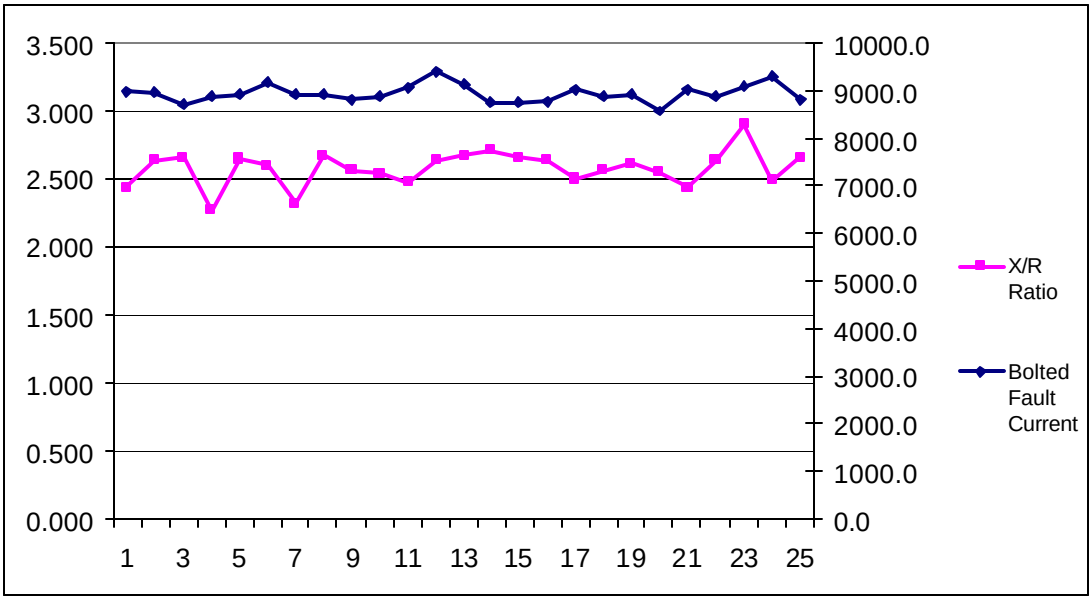

Figure D.1. Graphed results of sample test data presented in table D.1.

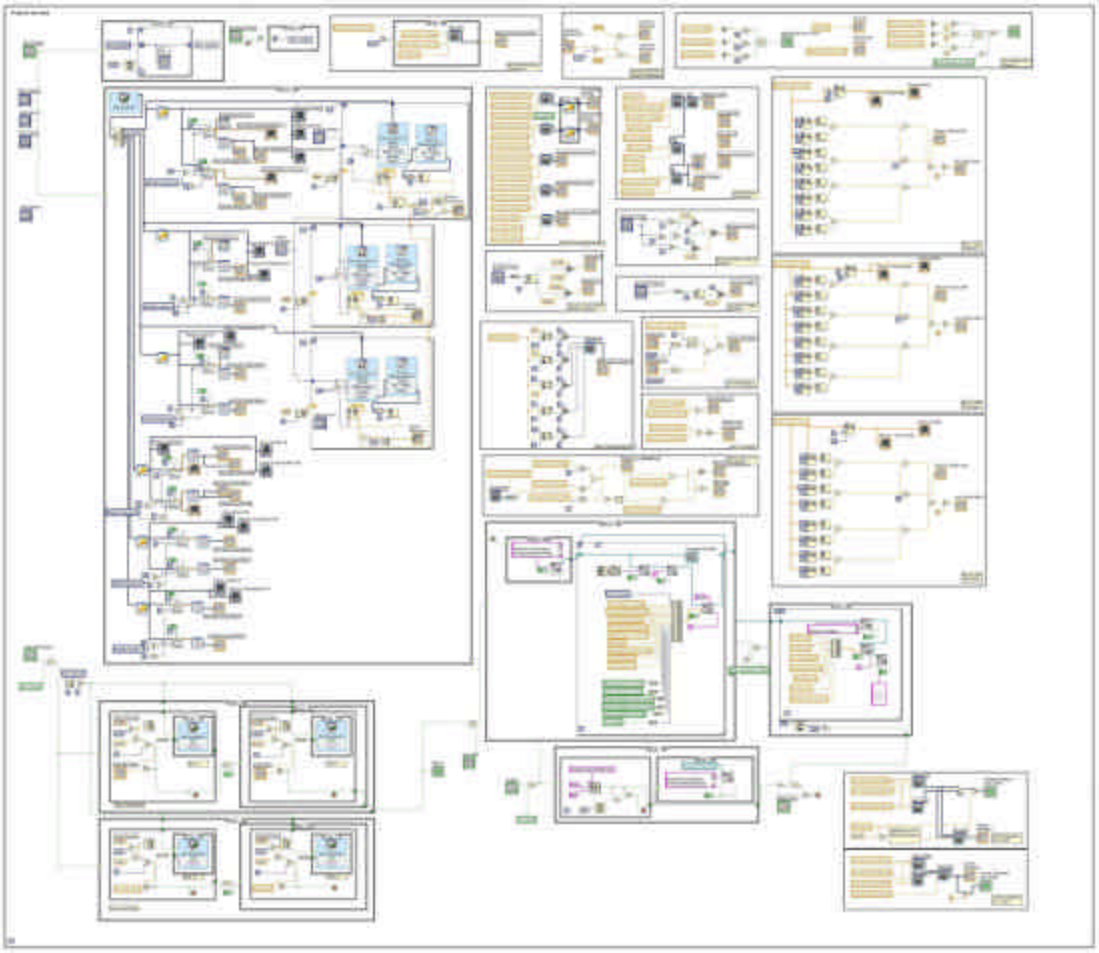

Figure D.2. LabView code for the IADD, complete.

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