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FABRICATION, ELECTRICAL CHARACTERIZATION AND ANNEALING OF AL/, CU/, AND AU/4H-SIC SCHOTTKY DIODES

A Thesis
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science
Electrical Engineering

---

by
Nikhil Karkhanis
December 2007

Accepted by:
William R. Harrell, Committee Chair
Kelvin F. Poole
Michael A. Bridgwood

ABSTRACT

Schottky diodes were fabricated on n-type 4H-SiC with Nickel ohmic contacts and Aluminum, Copper, and Gold Schottky contacts. An improved and revised fabrication process was developed in the course of this research project. The Schottky diodes were electrically characterized using I-V and C-V measurements to extract electrical parameters which include Schottky barrier height, ideality factor, the diode series resistance, and substrate doping density. Al/4H-SiC and Au/4H-SiC were annealed at 600ºC and 500ºC respectively to improve the Schottky parameters. Schottky barrier height was raised and the ideality factor was reduced in both cases. Significant improvement was observed in the ideality factor of Al/4H-SiC diodes. XPS was performed on Al/4H-SiC samples to investigate the effects of annealing at the Aluminum-SiC interface. Analysis of the XPS results showed traces of Aluminum-Silicon bonding at the interface. The change in the Schottky parameters is attributed to this phenomenon. The electrical characterization of Au/4H-SiC showed that the devices had a very low ideality factor of 1.1 and represented some of the best results obtained in our research lab. The thesis establishes the effect of annealing on Schottky diodes and presents some of the very few surface analysis results performed on Al/4H-SiC.

DEDICATION

I would like to dedicate this thesis to my parents for their continuous support and faith in me. It is also dedicated to my brother for all the advice and aid he has provided.

ACKNOWLDEGEMENTS

I would like to thank my advisor Dr. William R. Harrell for all his help and contribution throughout the duration of my research. This thesis would not have been possible without his direction and guidance. I would also like to thank Dr. Jim Harriss, who has been an ideal mentor and teacher throughout my training and research. I am indebted to Dr. Poole for his experienced advice and criticisms, which were useful during my graduate student life and beyond. I am also grateful to Dr. Bridgwood for his time and efforts in reviewing my thesis. Finally, I would like to thank Dr. Doug Hirt, Dr. Chad Sosolik and Dr. Santosh Rahane for their help in analyzing XPS results.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Silicon Carbide (SiC) is the only known stable binary compound of Silicon and Carbon. SiC is an attractive semiconductor due to its superior electrical, thermal, chemical and mechanical properties. Its properties such as wide band gap, high thermal conductivity, high breakdown field, high saturation electron drift velocity, high chemical stability, and strong mechanical strength make it a promising material for next generation electronic devices for high power, high temperature and high frequency applications.

One unique aspect of SiC is that it possesses a one-dimensional polymorphism called polytypism. Among the numerous known polytypes, three polytypes have generated much interest, namely 3C-, 4H- and 6H-SiC. There have been a large number of studies on 6H-SiC because single crystal 6H-SiC has been relatively easy to obtain as compared to other polytypes. However, 4H-SiC has superior electronic properties over the other two, including wider band-gap and higher, more isotropic electron mobility.

Schottky Barrier Diodes (SBDs) are used as rectifiers to suppress high-voltage transients induced on the power line during current switching. For a negligible dissipation of power during switching, the reverse current transient of the SBD must be suppressed, maintaining a high reverse voltage without breakdown. SiC Schottky Barrier Diodes are especially attractive because of their high breakdown voltages and low leakage currents.

The focus of this research project is to fabricate and characterize metal/4H-SiC Schottky Diodes and to study the effects of annealing on the Schottky parameters.

1.2 Synopsis of the chapters

Chapter 2 reviews the basic properties of SiC in terms of Crystal structure, various polytypes with an emphasis on the three primary polytypes, thermal, mechanical, optical, and electronic properties. The comparison of these properties with Silicon (Si) and Gallium Arsenide (GaAs) will also be included, highlighting the superiority of SiC and in particular, the 4H polytype.

Chapter 3 reviews the theory of metal-semiconductor contacts, both rectifying and ohmic. The various current conduction mechanisms in metal-semiconductor contacts are also reviewed.

Chapter 4 introduces the entire fabrication process of metal-4H-SiC diodes followed in this research project. This includes the previous fabrication process and the revised fabrication process, with emphasis on the reasons for the changes in the process and the consequent improvements.

Chapter 5 explains the different measurement techniques used, the measurement setup for each technique and the extraction of Schottky parameters from the measured results. The theories behind each technique, along with the tools used for the parameter extractions are also discussed.

Chapter 6 discusses the results of the measurements in detail. The performance of the Schottky diodes is discussed in detail, with comparison of the Schottky parameters for different metals used. The benefits of the revised fabrication process are also explained. Finally, the effect of annealing of Schottky contacts on the device performance is explained with comparison of the Schottky parameters before and after annealing.

CHAPTER 2

REVIEW OF SILICON CARBIDE

SiC is an attractive semiconductor due to its superior electrical, thermal, chemical and mechanical properties such as wide band gap, high thermal conductivity, high breakdown field, high saturation electron drift velocity, high chemical stability, and good mechanical strength. These properties make SiC a promising material for next generation electronic devices for high power, high temperature and high frequency applications that are not possible using Si or GaAs. SiC is also resistant to high radiation doses, which makes it potentially the ideal material for nuclear power applications [1]. SiC can also be used for various optical device applications such as blue and ultraviolet (UV) light emitting diodes (LEDs) and photodetectors. In this chapter, some of the basic physical, thermal, mechanical, optical and electronic properties are discussed.

2.1 Physical Properties

2.1.1 Crystal Structure

SiC is the only known stable binary compound of Silicon (Si) and Carbon (C). It contains an equal number of Silicon and Carbon atoms. The basic structural unit of SiC is a covalently bonded (88% covalent and 12% ionic) tetrahedron between Si and C atoms. Each Si atom is covalently bonded with four C atoms in a tetrahedral structure and similarly, each C atom is bonded to four Si atoms. The approximate bond length between

the Si-Si or C-C atoms is 3.08Å, while the approximate bond length between the Si-C atoms is 1.89Å [1]. The SiC crystals are formed by the tetrahedrons joined to each other at the corners.

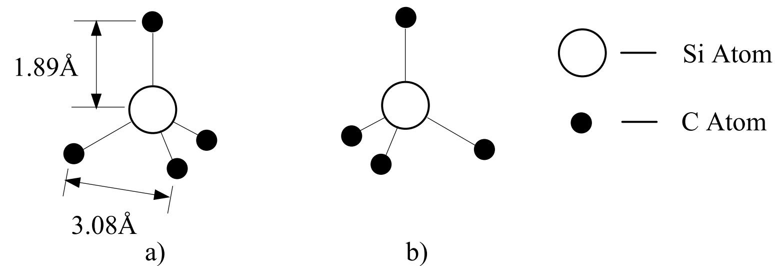

Figure 2.1 Basic tetrahedral unit in SiC consisting of a tetrahedron of four C atoms with one Si atom in the middle: a) Basic tetrahedron with bond lengths. b) Basic tetrahedron rotated 180º around the stacking direction.

2.1.2 Polytypes

SiC possesses a one-dimensional polymorphism called polytypism. In a polytypic compound, similar sheets of atoms are stacked on top of each other and related according to a symmetry operator. The differences among the polytypes arise in the direction perpendicular to the sheets. In SiC, each sheet represents a bilayer composed of one layer

of Si atoms and one layer of C atoms. To stack an identical second sheet on top of the first, there are two possibilities for arranging the second sheet relative to the first sheet, as shown in Fig. 1.2. Thus a sheet can be denoted as A, B or C depending on its position of the spheres relative to the previous layer.

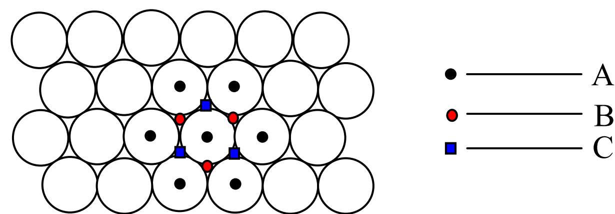

Figure 2.2 Different possible stacking positions relative to a bilayer.

Depending on the stacking sequence, the crystal structures of SiC are cubic, hexagonal, or rhombohedral. The only known cubic polytype (3C) is referred to as β-SiC, while the hexagonal and rhombohedral polytypes are collectively referred to as α-SiC. Depending on the periodicity in the stacking sequence, the polytypes are referred as 3C, 4H, 6H, 15R, etc. Thus, 4H-SiC has a hexagonal crystal structure with a periodicity of 4 bilayers, while 15R-SiC has a rhombohedral crystal structure with a periodicity of 15 bilayers. The stacking sequences of the common polytypes of SiC are shown in Fig. 1.3.

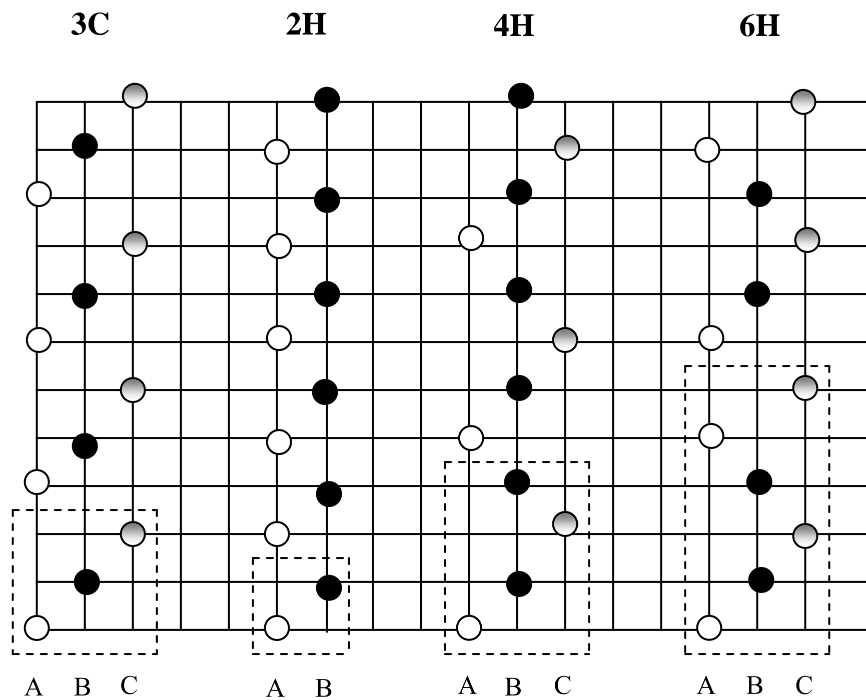

Figure 2.3 Stacking sequences of SiC bilayers in common polytypes.

The unit cell of the hexagonal polytypes of SiC is shown in Fig. 1.4. The plane formed by the bilayer sheet of Si and C atoms is known as the basal plane [2]. The basal plane has 3 axes at an angle of 120º with each other. The axis perpendicular to the basal plane is the *c*-axis, which is also the stacking direction of the bilayers. The SiC crystal planes thus need four Miller indices for reference. Thus, the stacking direction or the [0001] direction is the crystallographic *c*-axis which is defined normal to the basal plane.

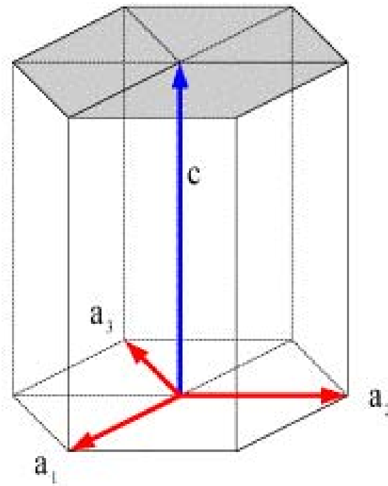

Figure 2.4 Unit cell of hexagonal polytypes of SiC.

SiC is a polar semiconductor across the *c*-axis. As shown in Fig. 1.5, one surface normal to the *c*-axis is terminated with Si atoms while the opposite surface is terminated with C atoms. These surfaces are commonly referred to as “Silicon face” and “Carbon face” respectively. The Silicon atoms in Fig. 1.5 labeled “*h*” or “*k*” denote the Si-C bilayers which are in “quasi-hexagonal” or “quasi-cubic” environments with respect to their immediate neighboring bilayers.

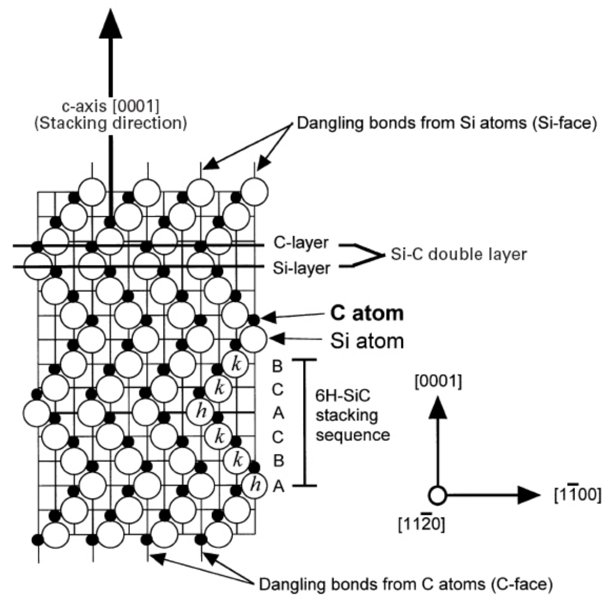

Figure 2.5 Schematic cross-section of the 6H-polytype illustrating the silicon face and carbon face[2].

2.2 Thermal Properties

The excellent high-temperature properties make SiC very suitable for high-temperature electronic applications. The high elastic modulus of SiC and the relatively low atomic weights of Si and C promote harmonic lattice vibrations, giving SiC a high thermal conductivity [1]. From the device application point of view, the thermal conductivity of SiC exceeds that of Copper, BeO, Al_2O_3 and AlN [3]. The thermal properties of 3C-, 4H- and 6H-SiC are listed in Table 2.1.

Table 2.1 Thermal properties of common polytypes of SiC [1], [4].

Properties	3C	4H	6H
Melting Point (ºC)	~3100K	~3100K	~3100K
Specific Heat (J g^{-1} ºC^{-1})	0.69	0.69	0.69
Thermal Conductivity (W cm^{-1} ºC^{-1})	4.9	4.9	4.9
Thermal Diffusivity (cm^2 s^{-1})	1.6	1.7	2.2
Thermal Expansion (ºC^{-1})	~3.8 * 10^{-6}		4.3 * 10^{-6} ($\perp c$-axis) 4.7 * 10^{-6} (|| c-axis)

2.3 Mechanical Properties

SiC is one of the hardest known materials and is widely used as a cutting tool or an abrasive. Listed below in Table 2.2 are some of the excellent mechanical properties.

Table 2.2 Mechanical properties of common polytypes of SiC [1].

Properties	3C	4H	6H
Bulk Modulus (GPa)	392-448		97
Mohs hardness	~9	~9	~9
Acoustic velocity (ms^{-1})	12600	13730	13100 - 13260

2.4 Optical Properties

Silicon carbide is an electroluminescent material and hence is widely used for manufacturing blue LEDs and ultraviolet detectors. Table 2.3 lists some of the optical properties of SiC.

Table 2.3 Optical properties of common polytypes of SiC [1], [4].

Properties	3C	4H	6H
Optical Bandgap (eV)	2.4-2.6		2.86
Excitation Energy Gap (eV)	2.39	3.27	3.02
Infrared Refractive Index	2.55	2.55 ⊥ *c*-axis 2.59 ∥ *c*-axis	2.55 ⊥ *c*-axis 2.59 ∥ *c*-axis

2.5 Electrical Properties

SiC has generated much interest in power applications due to its superior electrical properties. Among other properties, the wide bandgap energy and low intrinsic carrier concentration of SiC allow it to maintain semiconductor behavior at much higher temperatures than Silicon, which permits SiC device functionality at elevated temperatures. A natural consequence of the wider bandgap of SiC is higher effective Schottky barrier heights, which allows Schottky Barrier Diodes to suppress currents at high reverse voltages without breakdown. Also, a lower intrinsic carrier concentration leads to lower leakage currents due to minority carriers. Listed below in Table 2.4 are

some of the important electrical properties of the common polytypes of SiC. Comparison of some the properties with the corresponding properties of Silicon (Si) and Gallium Arsenide (GaAs) are presented in Table 2.5.

Table 2.4 Electrical Properties of common polytypes of SiC [1], [4].

Properties	3C	4H	6H
Breakdown Field (V cm^{-1})	$\sim 10^6$	$6*10^5$	$6*10^5$
Mobility (cm^2 V^{-1} s^{-1})			
electrons	≤800	≤900	≤400
holes	≤320	≤120	≤90
Diffusion coefficient (cm^2 s^{-1})			
electrons	≤20	≤22	≤10
holes	≤8	≤3	≤2
Electron Thermal Velocity (m s^{-1})	$2 * 10^5$	$1.9 * 10^5$	$1.5 * 10^5$
Hole Thermal Velocity (m s^{-1})	$1.5 * 10^5$	$1.2 * 10^5$	$1.2 * 10^5$
Saturated Electron Drift Velocity (cm s^{-1})	$2 * 10^7$	$2 * 10^7$	$2 * 10^7$
Electron Affinity (eV)		3.6	3.3

2.6 Choice of 4H-SiC polytype

A large number of studies have been done on 6H-SiC because single crystal 6H-SiC has been relatively easy to obtain as compared to other polytypes [5]. However, 4H-SiC is a superior semiconductor because of its wider bandgap and higher electron mobility. Table 2.5 lists the important properties of 4H-SiC in comparison with the other polytypes, along with Silicon and GaAs.

Table 2.5 Properties of Silicon, GaAs, and SiC at T=300K [1], [4], [6].

Property	Si	GaAs	SiC		
			3C	4H	6H
Bandgap Energy (eV)	1.12	1.42	2.36	3.26	3
Breakdown Field (V cm^{-1})			$\sim 10^6$	$6*10^5$	$6*10^5$
Density (gm cm^{-3})	2.33	5.32	3.21	3.21	3.21
Static Dielectric Constant	11.7	13.1	9.72	9.66 ⊥ *c*-axis 10.03 ‖ *c*-axis	9.66 ⊥ *c*-axis 10.03 ‖ *c*-axis
Electron Mobility (cm^2 s^{-1})	1350	8500	≤800	≤900	≤400
Hole Mobility (cm^2 s^{-1})	480	400	≤320	≤120	≤90
Intrinsic Carrier Concentration (cm^{-3})	$1.5*10^{10}$	$1.8*10^6$	6.9	$8.2*10^{-9}$	$2.3*10^{-6}$
Saturated Electron Drift Velocity (cm s^{-1})	$1.0*10^7$	$1.0*10^7$	$2.0*10^7$	$2.0*10^7$	$2.0*10^7$
Thermal Conductivity (W cm^{-1} $^oC^{-1}$)	1.5	0.5	4.9	4.9	4.9
Electron Affinity (eV)	4.01	4.07	4.0	3.6	3.3
Effective Conduction Band Density of States (cm^{-3})	$2.8*10^{19}$	$4.7*10^{19}$	$1.5*10^{19}$	$1.7*10^{19}$	$8.9*10^{19}$
Effective Valence Band Density of States (cm^{-3})	$1.04*10^{19}$	$7.0*10^{18}$	$1.2*10^{19}$	$2.5*10^{19}$	$2.5*10^{19}$
Effective Electron Mass (in units of m_0)					
longitudinal m_l/m_0 transverse m_t/m_0	0.98 0.19	0.067	0.68 0.25	0.29 0.42	2.0 0.42
Effective Hole Mass (in units of m_0)	0.49	0.45	0.6	~1	~1

The basal plane electron mobility of 4H-SiC is reported to be more than twice than that of 6H-SiC, while the electron mobility of 4H-SiC in the direction of *c*-axis is almost 10 times that of 6H-SiC [7]. Furthermore, the anisotropy ratio (A_e = 0.83) of 4H-SiC between the electron mobilities parallel to and along the *c*-axis is much closer to unity than the anisotropy ration (A_e = 4.9) in 6H-SiC [1]. Hence, to realize Schottky Barrier Diodes with maximum performance, 4H-SiC was chosen for this work.

CHAPTER 3

METAL-SEMICONDUCTOR CONTACTS

The earliest investigation of metal-semiconductor rectifying contacts is attributed to Braun, who in 1874 noted the dependence of the total resistance on the polarity of the applied voltage and on detailed surface conditions [8]. In 1931, it was discovered that if a current flows through a metal-semiconductor contact, then the potential drop occurs almost entirely at the contact, implying the existence of a potential barrier. In 1938, Schottky and Mott, both independently, came up with a theory explaining the transport of electrons over the potential barrier through drift and diffusion. This was the groundwork on which subsequent work done on Schottky and Ohmic contacts was based. In this chapter, the theory of ideal metal-semiconductor contacts is introduced. Then, the concept of barrier height and the various current conduction mechanisms are reviewed. Finally, the applications of metal-semiconductor contacts in microelectronics will be discussed.

3.1 Ideal Metal-Semiconductor contacts

A Metal-Semiconductor contact is formed when a metal and a semiconductor are brought into intimate contact with each other. Depending on the work-functions of the metal and the semiconductor, the contact may be either Schottky (rectifying) or Ohmic (non-rectifying). In this chapter, we will primarily focus on the Schottky contacts because the majority of metal-semiconductor combinations form rectifying or "blocking" contacts.

To see how a Schottky barrier is formed, suppose that the metal and semiconductor are both electrically neutral and isolated from each other. The energy band-diagram in Fig. 3.1(a) is for an n-type semiconductor whose work function (ϕ_s) is less than that of the metal (ϕ_m). This is the most common case observed when forming Schottky contacts. If the metal and semiconductor are electrically connected by a wire, electrons will pass from the semiconductor into the metal and the two Fermi levels are forced to align as shown in Fig. 3.1(b). There is an electric field in the gap and there is a negative charge on the surface of the metal, which is balanced by a positive charge in the semiconductor. If the metal and the semiconductor approach each other as shown in Fig. 3.1(c), the potential difference between the electrostatic potentials between the surfaces of the metal and the semiconductor tends to zero, since the electric field is finite. When they finally touch, the barrier due to the gap vanishes altogether and we get an ideal metal-semiconductor contact.

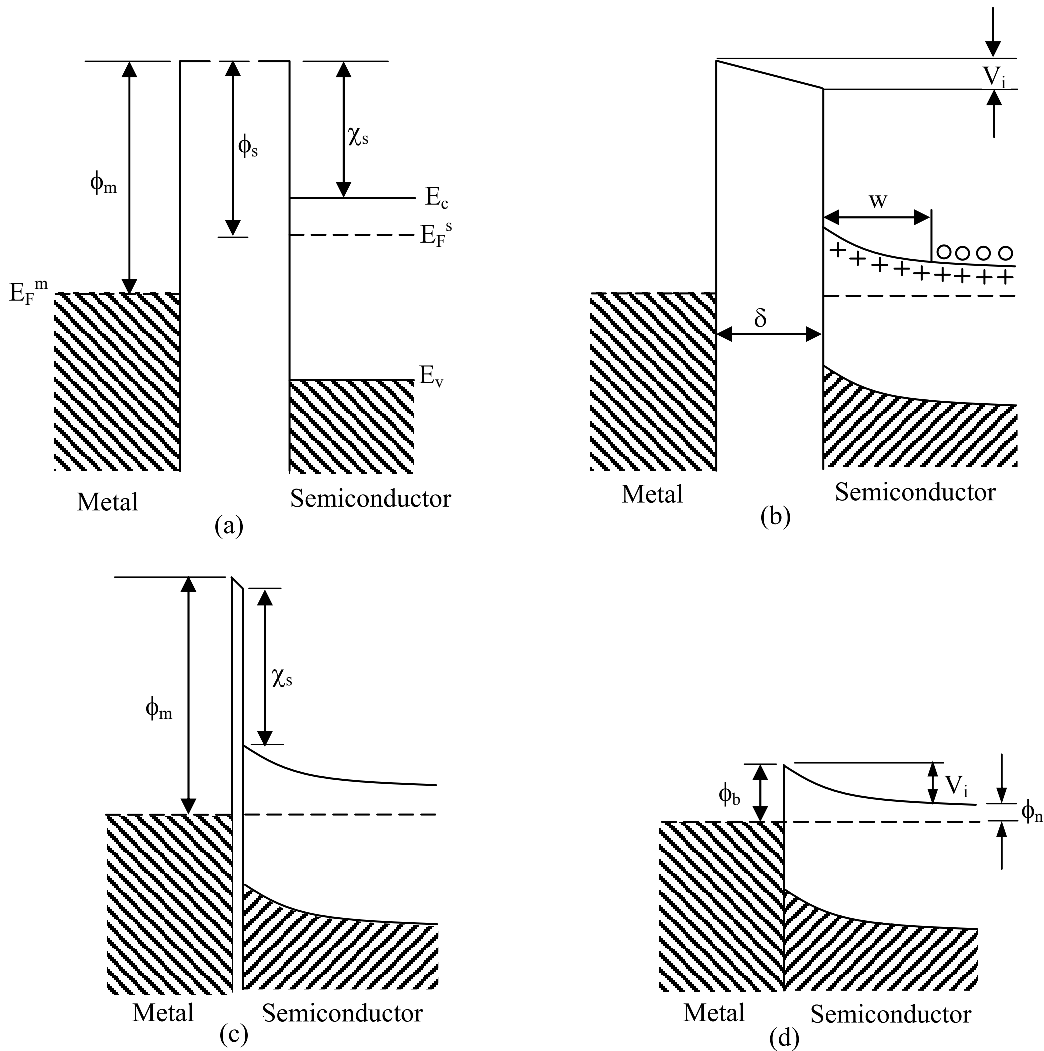

Figure 3.1 Formation of Schottky barrier between metal and n-type semiconductor: (a) neutral and electrically isolated, (b) electrically connected, (c) separated by a narrow gap, (d) in perfect contact[9].

In most practical cases, the ideal situation shown in Fig. 3.1(d) is never reached because there is usually a thin insulating layer of oxide about 10-20Å thick on the surface of the semiconductor. Such an insulating layer is called an interfacial layer. A practical

contact is thus more like that shown in Fig. 3.1(c). However, the barrier presented to the electrons by the interfacial layer is usually so narrow that the electrons can tunnel through it quite easily.

Fig 3.2 illustrates barrier height for various combinations of the semiconductor type and the M-S work function difference (ϕ_{ms}). The cases shown in Fig. 3.2 (b) and (c) are very uncommon in practice and the majority of the metal-semiconductor combinations form rectifying contacts.

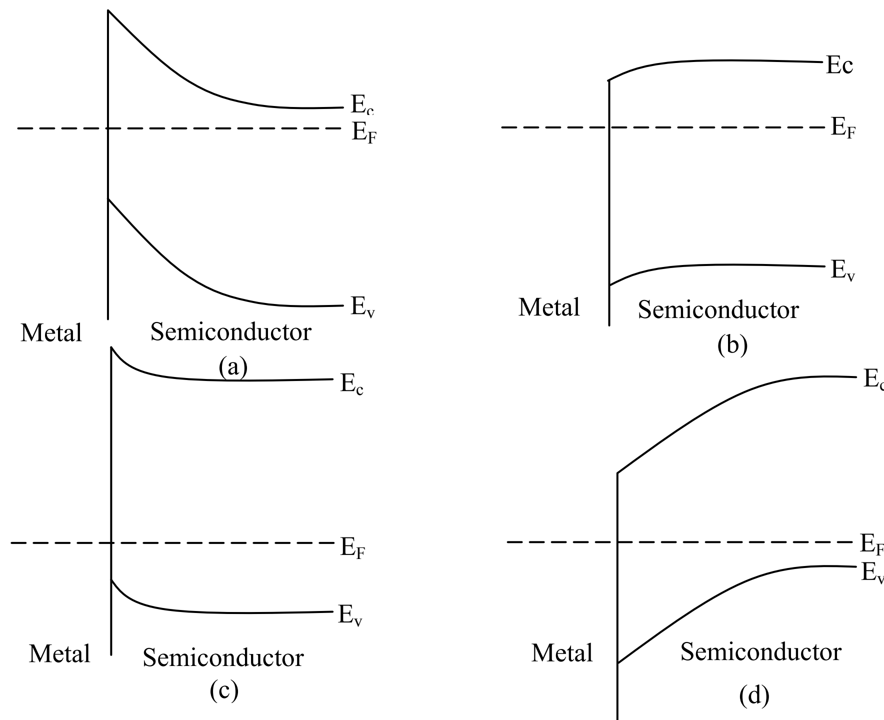

Figure 3.2 Barriers for semiconductors of different types and work functions; n-type: (a) $\phi_m > \phi_s$ (rectifying), (b) $\phi_m < \phi_s$ (ohmic). p-type: (c) $\phi_m > \phi_s$ (ohmic). (d) $\phi_m < \phi_s$ (rectifying).

If we consider other combinations of the semiconductor type and metal, for instance a case when ϕ_s is greater than ϕ_m as shown in Fig. 3.2(b), then the barrier height encountered in the Fig. 3.1(d) is no longer applicable. If the contact was biased such that the electrons flow from semiconductor to the metal, they encounter no barrier. The current is then determined by the bulk resistance of the semiconductor. Such a contact is called an Ohmic contact. This type of contact has sufficiently low resistance for the current to be determined by the resistance of the bulk semiconductor rather than the contact properties.

3.2 Schottky Barrier Height

3.2.1 Schottky-Mott Limit

The work function is defined as the energy difference between the vacuum level and the Fermi level. This quantity is denoted by ϕ_m for the metal and ϕ_s for the semiconductor. The semiconductor work function is given by:

$$\phi_s = \chi + \phi_n \qquad 3.1$$

where ϕ_n is the energy difference between the E_C and the Fermi level E_F, and is given by

$$\phi_n = E_C - E_F = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \qquad 3.2$$

The potential difference between the work functions ϕ_m and ϕ_s is called the contact potential and is equal to the built-in potential at equilibrium when no bias is applied. The potential difference is given by:

$$\phi_{ms} = V_i = \phi_m - \phi_s \qquad 3.3$$

Thus the barrier height, ϕ_{Bn}, for the ideal case is given by

$$\phi_{Bn} = \phi_m - \chi \qquad 3.4$$

For an ideal contact between a metal and a p-type semiconductor, the barrier height ϕ_{Bp} is given by

$$\phi_{Bp} = Eg - (\phi_m - \chi) \qquad 3.5$$

Equation 3.4 is referred to as the Schottky-Mott Limit, and gives the limiting value for the barrier height in ideal metal-semiconductor contacts. In obtaining equation 3.4, a number of important assumptions have been made, specifically:

a) The surface dipole contributions to ϕ_m and χ do not change when the metal and semiconductor are brought in contact with each other.
b) There are no localized states on the surface of the semiconductor.

c) There is perfect contact between the metal and the semiconductor; i.e., there is no interfacial layer of any kind.

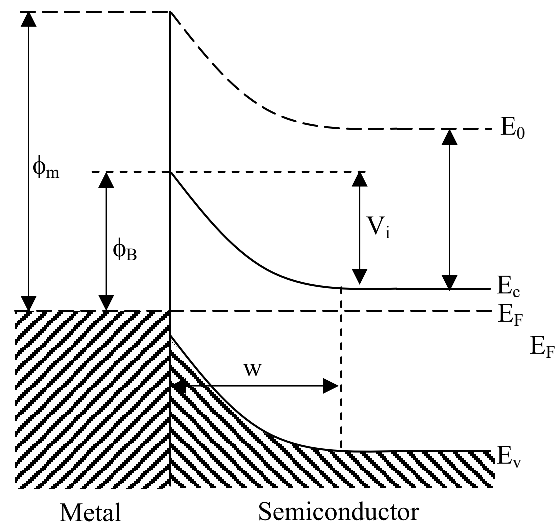

Figure 3.3 Energy Band Diagram of the Schottky contact

3.2.2 Bardeen Limit

The Schottky-Mott theory suggests that the barrier height, ϕ_B, is strictly a function of the metal work function and the electron affinity of the semiconductor. However, it is practically found that the barrier height is a less sensitive function of ϕ_m and in some circumstances is almost independent of ϕ_m. An explanation of this was put forward by Bardeen in 1947, who suggested that the discrepancy may be due to the effect of surface states. Figure 3.4 illustrates a Schottky contact with the presence of a thin interfacial layer, and a continuous distribution of surface states at the interface.

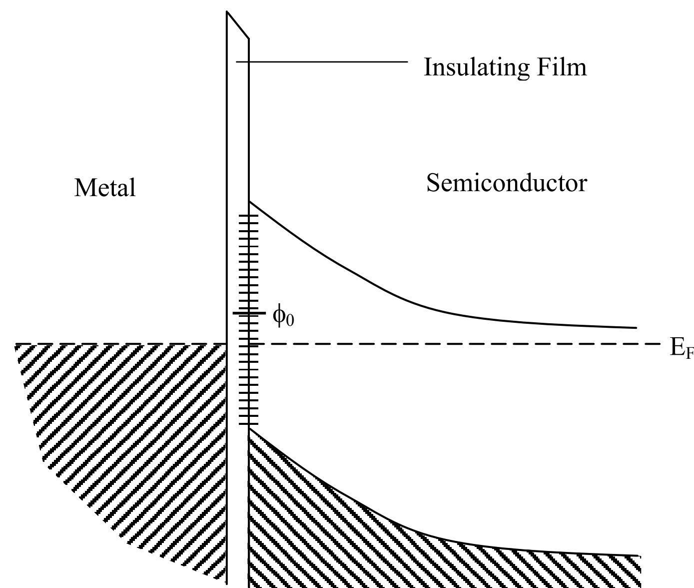

Figure 3.4 Metal-Semiconductor contact with surface states.

The occupancy of the surface states is determined by the Fermi level. If the neutral level ϕ_0 of the insulator is above the Fermi level E_F, the surface states contain a net positive charge. On the other hand, if ϕ_0 is below E_F, then the surface states have a net negative charge. The surface states behave like a negative feedback loop, the error signal of which is the deviation of ϕ_0 from E_F. If the density of surface states becomes very large, the error signal will be very small and $\phi_0 \approx E_F$. In this case, the density of surface states is large enough to accommodate any additional surface charges without appreciably altering E_F. As a result, the barrier height is determined by the property of the semiconductor surface and not the metal work function. When the limit is reached, the barrier height is said to be “pinned” by the high density of the surface states. This is called the Bardeen Limit. Effectively, when the Bardeen Limit is reached, the surface states screen the semiconductor from the electric field in the insulating layer so that the charge in the depletion region and the barrier height are independent of the metal work function ϕ_m. The Bardeen Limit is given by:

$$\phi_B = E_g - \phi_0 \qquad 3.6$$

The Schottky-Mott Limit and the Bardeen Limit are the two limiting cases of the barrier height, ϕ_b, for a metal-semiconductor contact. Usually the actual Schottky Barrier Height falls somewhere between the Schottky-Mott Limit and the Bardeen Limit. In SiC, there is no Fermi-level pinning, thus the SBH is metal work function dependant [10].

3.3 Current Transport Mechanisms

The current transport mechanisms which determine the conduction in the Schottky contact are discussed in this section. The ways in which electrons can be transported from the semiconductor across the barrier into the metal are:

a) Emission of electrons over the top of the barrier.

b) Quantum-mechanical tunneling through the barrier.

c) Electron-hole recombination in the space-charge region.

d) Electron-hole recombination in the neutral region of the semiconductor.

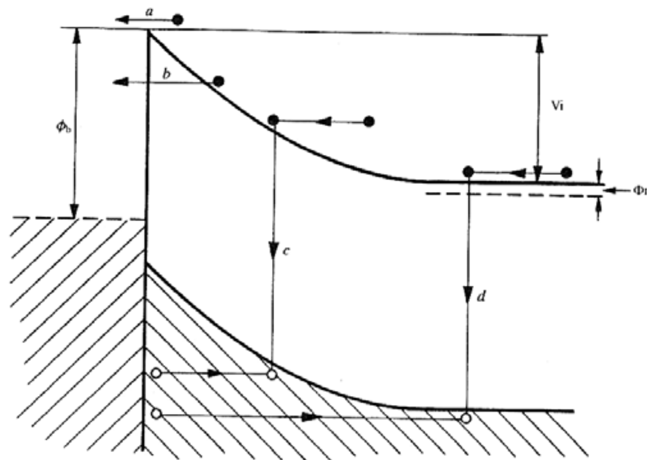

Figure 3.5 Current transport mechanisms in a forward-biased Schottky Barrier.

3.3.1 Electron Emission over the Barrier

The flow of electrons from the semiconductor to the metal is mainly governed by two processes. First, the electrons traverse the depletion region in the semiconductor near the metal under the influence of the drift and diffusion mechanisms. When they arrive at the metal/semiconductor interface, they are emitted into the metal across the boundary. The two processes are effectively in series and the current is predominantly controlled by the mechanism which offers the most obstruction to the flow of the electrons. According to the diffusion theory, the first process is the limiting factor, while the thermionic-emission theory claims the second process is the limiting factor. The primary difference between the two theories is the behavior of the quasi-Fermi level in the semiconductor.

According to the diffusion theory, the quasi-Fermi level at the interface coincides with the Fermi level in the metal. When the electrons flowing in the semiconductor arrive at the interface, they are in thermal equilibrium with the conduction electrons in the metal. Thus, the concentration of the electrons on the semiconductor side is unaltered by the application of bias, and the transition of the quasi-Fermi level from the semiconductor bulk Fermi level, E_{Fs}, to the metal Fermi level, E_{Fm}, occurs in the depletion region.

The thermionic-emission theory postulates that the quasi-Fermi level at the interface is not coincident with the Fermi level of the metal, and remains constant throughout the depletion region at E_{Fs}, similar to a p-n junction. Therefore, the electrons emitted from the semiconductor are not in thermal equilibrium with the conduction electrons in the metal, but have an energy which equals the sum of the Fermi energy of

the metal and the barrier height. These are referred to as “hot electrons”. When these hot electrons penetrate into the metal, they lose energy by collisions with the conduction electrons and eventually become in equilibrium with them. This indicates that the quasi-Fermi level falls in the metal until it coincides with the metal Fermi level.

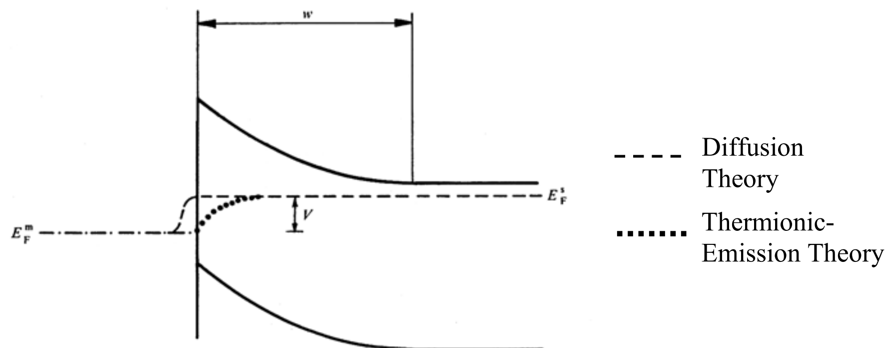

Figure 3.6 Electron quasi-Fermi level in a forward-biased Schottky barrier

Thus, even though the gradient of the quasi-Fermi level is ultimately the driving force for electrons, the diffusion theory claims that the gradient occurs in the depletion region, while the thermionic-emission theory claims that it occurs in the metal. The diffusion theory attributes the main obstacle to the current flow to be the combined effects of drift and diffusion, while the thermionic-emission theory attributes the main obstacle to the current flow to the process of thermionic emission of electrons into the metal. In practice however, the true behavior of the current transport lies somewhere between the two extremes of the diffusion theory and the thermionic emission theory.

3.3.2 Quantum-mechanical tunneling through the barrier

Under certain circumstances, it may be possible for electrons with energies below the top of the barrier to penetrate the barrier through quantum-mechanical tunneling. In the case of degenerate semiconductors at low temperature, current may arise from tunneling of electrons close to the Fermi level. This is called "field emission". Field emission is of considerable importance for ohmic contacts. Ohmic contacts usually consist of Schottky barriers on very heavily doped material, which makes the depletion region so thin that field emission takes place and the contact has very low resistance.

As the temperature is increased, electrons are excited to higher energies and the tunneling probability increases since they face a thinner barrier. However, the number of excited electrons decreases rapidly with increasing energy. There will be an optimum energy at which the contribution of excited electrons to the current will be maximum. This is called "thermionic-field emission". If the temperature is further raised, more and more electrons will be energized to go over the top of the barrier, until a point is reached when the effect of tunneling as compared to the pure thermionic emission is negligible.

3.3.3 Electron-hole recombination in the space-charge region

The recombination in the depletion region normally takes place due to the localized states in the semiconductor. The localized states are often referred to as “traps” since they tend to capture minority carriers. The localized states are formed due to a number of reasons such as defects, surface states, dangling bonds, and impurities. These traps have an energy level associated with them, which is usually located in the forbidden energy gap. The most effective trap centres are those with energies lying near the center of the forbidden gap. The theory of current due to such recombination centers is similar to that for p-n junctions, and is predicted by the S-H-R (Shockley, Hall and Read) model. Recombination current is a common cause for non-ideal behavior in Schottky diodes. Such departures from ideal behavior are more pronounced at low voltage and low temperature conditions.

3.3.4 Hole Injection in the neutral region of semiconductor

When the height of the Schottky barrier is higher than half of the energy band gap, then the semiconductor region at and near the surface becomes p-type and contains a high-density of holes. The holes diffuse into the neutral region under the influence of forward bias and recombine with the electrons in the neutral region. If the hole concentration exceeds that of the electrons, then the surface is inverted and forms a p-n junction with the bulk. This effect is only noticeable in large barrier heights with weakly-

doped semiconductors. Since SiC has a very low intrinsic carrier concentration and has a large bandgap, the hole injection is negligible in SiC devices.

3.4 Ohmic Contacts

Ohmic contacts are contacts whose current-voltage (I-V) characteristics are determined by the resistivity of the semiconductor rather than the behavior of the actual metal-semiconductor contact. The essential criteria for this contact is that its resistance should be very small compared with the resistance of the semiconductor. Also, the contact itself should be both electrically and mechanically stable and should not inject minority carriers.

The fabrication of ohmic contacts more or less follows one of the following methods:

a) An ohmic contact can be formed by finding a suitable metal-semiconductor combination which yields a negative barrier height or a positive barrier height, as shown in Fig. 3.2(b) and (c), that is so small that the contact can have a low enough resistance to be effectively ohmic.

b) An ohmic contact can also be formed by having a heavily doped semiconductor immediately adjacent to the metal. Thus, the depletion region can be so thin that field emission is dominant enough for the contact to have a very low resistance

c) Crystal defects formed near a damaged surface of a semiconductor can act as efficient recombination centres. If the density of the defects is high enough, the recombination in the depletion region can become the dominant current conduction mechanism and will reduce the contact resistance significantly.

The most widely used of these methods is the second method. However, for SiC, the first method is preferred. It is generally difficult to make ohmic contacts on wide bandgap semiconductors like SiC as a metal does not exist with a work function low enough to yield a low barrier height. Since there aren't a lot of metal-SiC combinations available which naturally yield an ohmic contact, the common process is to create a Schottky contact and then modify the contact properties to reduce the Schottky barrier height enough to make it ohmic. The most commonly used method is to anneal certain metal-SiC contacts at the corresponding eutectic temperature in an inert gas to yield ohmic behavior. For example, Nickel/SiC contacts annealed at 1000°C corresponds to a barrier height of 0.38eV [11].

CHAPTER 4

FABRICATION OF METAL/4H-SIC SCHOTTKY DIODES

This primary aim of this project is to research the effect of thermal annealing on the parameters of Schottky diodes. The three metals used in this project for the Schottky contacts to SiC are Copper, Aluminum and Gold. The Schottky devices were fabricated on SiC substrates using an elaborate fabrication process. The Schottky devices are then annealed in a furnace for an appropriate time at an appropriate temperature. Electrical measurements were performed on the sample upon fabrication. These measurements will be presented and analyzed in detail in the next chapter. In this chapter, the entire fabrication procedure is presented in detail. The problems encountered and their solutions are discussed, which resulted in the development of a revised fabrication process. The annealing of ohmic and Schottky contacts is also discussed in detail in this chapter, and the schematics and temperature profiles of the furnace are presented to assist in the understanding of the process.

4.1 Basic Structure of Schottky Diode

A Schottky diode consists of a metal-semiconductor junction as compared to a semiconductor-semiconductor junction in p-n diodes. The metal is the anode terminal of the diode while the semiconductor substrate is the cathode. An ohmic contact is made to the substrate to provide the cathode terminal. To form a good ohmic contact, a substrate with high doping concentration is preferred. On the other hand, a good Schottky contact requires a substrate with moderate doping concentration. Hence, a highly-doped substrate with an loe to moderately doped epitaxial layer is often preferred for creating Schottky diodes.

The basic structure of a typical SiC Schottky diode is shown in Fig 4.1. The Schottky contacts are formed on the epitaxial layer (also known as epilayer). The side of substrate on which the Schottky contacts are deposited will be called as the Front-side. Ohmic contacts are formed on the other side of the substrate, which is also called as the Back-side. Since Schottky diodes are majority-carrier devices, n-type substrates are preferred since electron-mobility is usually higher than hole-mobility in semiconductors.

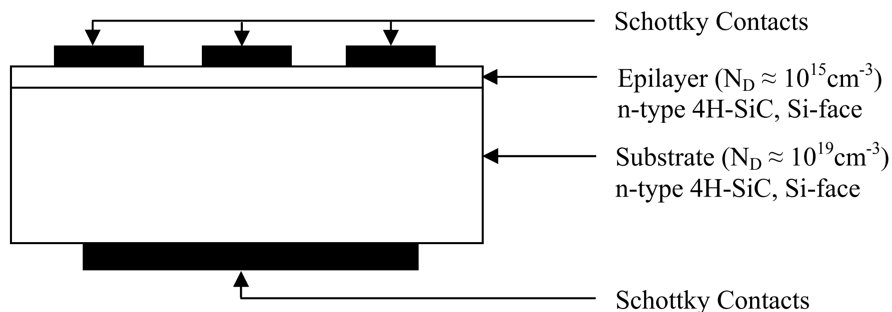

Figure 4.1 Basic Structure of a Schottky Diode

4.2 Materials and Resources Used

In this project, the substrates used were n-type 4H-SiC with Si-face purchased from Cree, Inc. The SiC die used were from a 1.5-inch wafer with 0.3375mm thickness cut into 6mm squares. The bulk doping concentration was on the order of 10^{18} cm^{-3}. The epilayer had a thickness of 5-10μm with a doping concentration on the order of 10^{15} cm^{-3}.

The Schottky diodes were fabricated at the Microstructures Laboratory in the Milton W. Holcombe Department of Electrical and Computer Engineering, Clemson University. The wet chemical processes were performed in a Class-100 cleanroom. The thermal evaporations were performed using a thermal evaporator made by Edwards Vacuum Ltd. The annealing steps were performed in a Thermo Products Ltd. Mini-Brute furnace. Post fabrication, the I-V measurements were taken with a Hewlett-Packard 4156B Precision Semiconductor Parametric Analyzer and the C-V measurements were taken using a Deep Level Transient Spectrometer from Sula Technologies. For surface characterization, X-ray Photoelectron Spectroscopy was performed using a XPS-KRATOS AXIS 165.

4.3 Preceding Procedure for Fabrication of Schottky Diode

The fabrication of a Schottky diode involves an elaborate procedure including surface treatment, thermal evaporation, and annealing. Since the metal-semiconductor interface is the most critical aspect of a Schottky diode, the fabrication processes used plays an important role in determining the Schottky parameters of the diode. Typical processes use surface treatments for etching the surface oxide and any other surface contaminants present on the semiconductor substrate, followed by thermal evaporations to deposit the Schottky and ohmic contacts. Annealing is performed at suitable stages for either obtaining ohmic behavior on the back-side contacts or improving the Schottky parameters of the front-side contacts. Prior research done by this group at Clemson University utilized a procedure which is reviewed in the following sub-sections [12], [13].

4.3.1 Initial Degrease and Back-side Surface Etch

The substrates used in fabricating these Schottky diodes were 6mm square die obtained from a 1.5-inch n-type 4H-SiC wafer with Si face. In factory-sealed condition, the SiC die were attached to a plastic pellicle with an adhesive, with a plastic layer on top to prevent exposure to atmosphere. As a result, the first logical step was to put the SiC substrate through a surface clean to remove any contaminants from the packaging. Also, before proceeding to deposit any metal contacts on the substrate, any oxide on the

substrate surface must be removed to expose the semiconductor surface below. To achieve these steps, the following processes were used:

1) The sample was degreased by immersion in Acetone for 2 minutes followed by immersion in Methanol for 2 minutes.

2) The sample was then immersed in a solution of diluted Hydrofluoric Acid (48% HF) and water in the volumetric ratio 1:25 HF:H_2O for 2 minutes.

3) The sample was rinsed in three beakers of de-ionized (DI) water for a period of 15 seconds, 30 seconds and 5 minutes respectively.

4) The sample was blow-dried with a Nitrogen gun.

During the degreasing of the sample with Acetone and Methanol, care was taken to flip the sample upside-down halfway during each step to make sure that each surface received equal exposure to the Acetone and Methanol. However, during the etching of the sample with HF, the sample was placed with the back-side facing up so that the back-side received the most exposure to the acid. The reason for this was since the next step was to deposit the Nickel contacts on the back-side, more emphasis was given to cleaning the back surface.

4.3.2 Deposition of Nickel on the Back-side

Nickel is widely used as an ohmic electrode to n-type 4H-SiC and 6H-SiC [14]. The choice of Nickel as the metal for creating ohmic contacts is elaborated in the next sub-section. In creating the ohmic contacts, approximately 1700Å of Nickel was deposited by thermal evaporation on the back-side of the sample. The thermal evaporation was performed at a pressure of 5 x 10^{-6} Torr to minimize contamination. During the evaporation, the sample rests on top of a suitable shadow mask so that the Nickel is deposited in the desired pattern. The pattern used for depositing the Nickel dots is shown in Fig. 4.2. Ideally the ohmic contact should cover a large portion of the back-side of the sample. However, this particular pattern was chosen because it provides two physically separated Nickel dots. The separate dots are useful in testing the resistance of the ohmic contacts at a later stage. The measurement will be discussed in greater detail in Chapter 5.

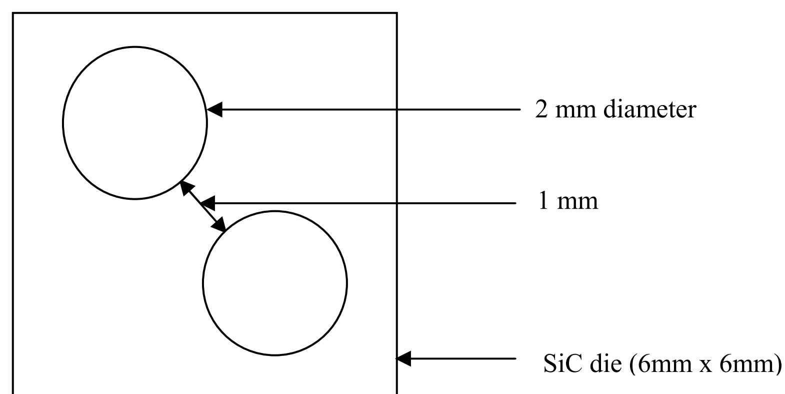

Figure 4.2 Pattern of Ohmic contacts on the back-side of 4H-SiC sample.

4.3.3 Annealing of Nickel to make Ohmic contacts

As discussed in Chapter 3, the most popular method of formation of ohmic contacts to SiC is to modify a Schottky contact to make it ohmic in behavior. This approach was employed in this project by annealing the Nickel contact for a suitable time and at a suitable temperature to make it ohmic. In the previous section, it was mentioned that Nickel was the metal of choice as an ohmic electrode for n-type 4H-SiC and 6H-SiC. The reason for the choice of Nickel is that Nickel forms an excellent ohmic contact with SiC after annealing [11], [14-16]. During the annealing, formation of a Ni_2Si phase occurs in a large temperature range between 600°C and 950°C [16]. However, below 900ºC-950ºC a rectifying behavior is observed [11], [16]. To obtain the lowest contact resistivity, the optimum condition for annealing Nickel ohmic contacts is approximately 1000ºC for 3 minutes [15]. The specific contact resistivity of such a contact is reported to be in the range of $10^{-6}\ \Omega\ cm^2$ [14].

The as-deposited Nickel contacts were annealed in a Mini-Brute furnace at 1000ºC for 3 minutes under an inert atmosphere consisting of a mixture of 10% Hydrogen and 90% Argon (Forming Gas). Annealing in an Argon environment reduces structural defects as the Argon atoms penetrate the material and occupy the interstitial vacancies, thereby reducing stress. The addition of H_2 leads to the saturation of the dangling bonds at the surface, thus reducing leakage current [17].

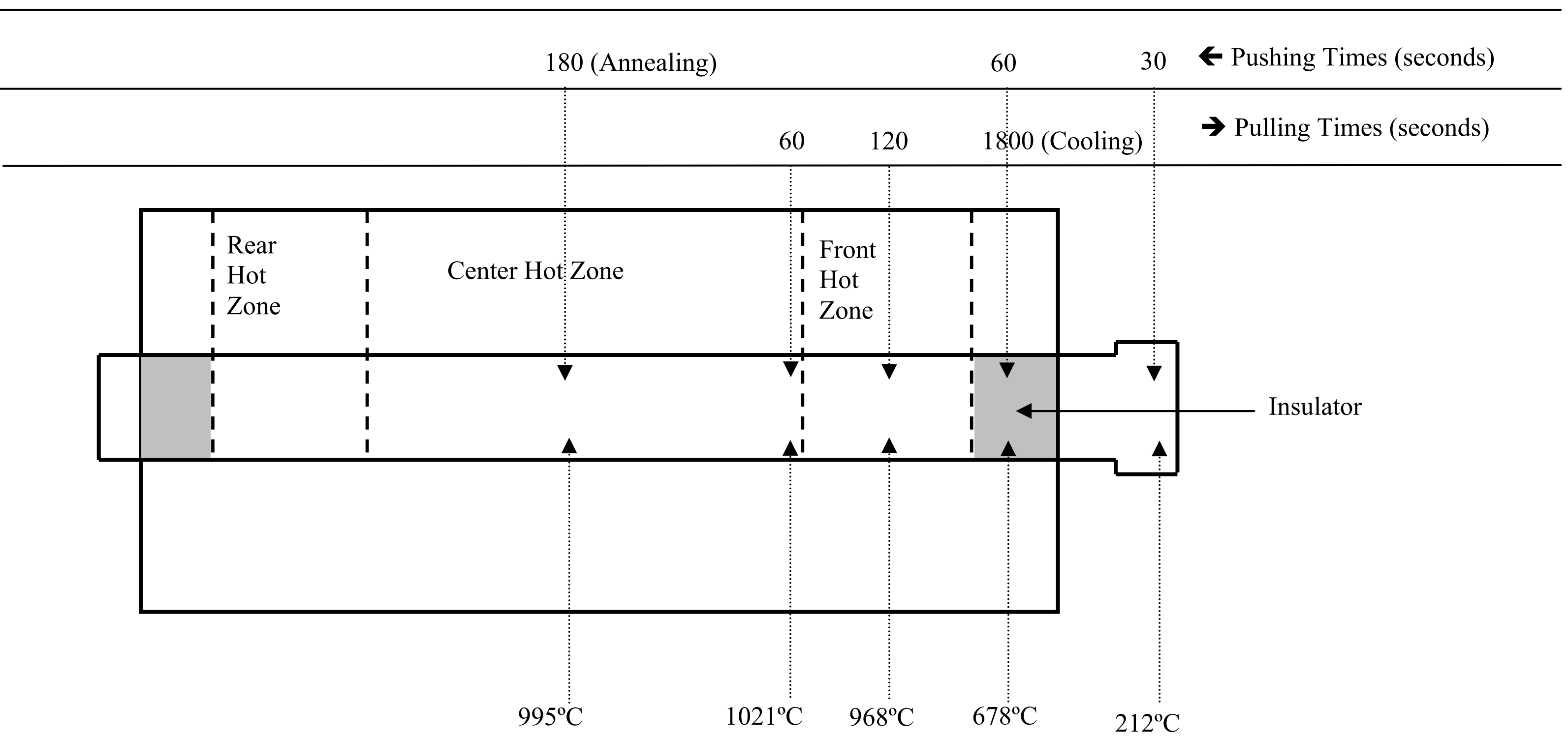

Figure 4.3 Schematic of Annealing Furnace tube with temperatures and time for annealing Nickel contacts at 1000ºC.

Figure 4.3 shows a detailed schematic of the furnace tube is shown along with the temperatures at various points during the annealing and the time intervals for which the sample was let sit at each point. The Mini-Brute furnace mainly consists of a quartz furnace tube surrounded by heating coils. The quartz tube is held in place with the help of white insulation pads at the front and back end of the furnace and thus is physically separated from the heating coils. The heating coils are arranged in three separate zones; front, center and rear. The center heating coils are heated to the desired temperature, while the front and the rear heating coils are adjusted relative to the center heating coils to compensate for the heat loss at either ends of the furnace tube, thus creating a uniform temperature in the center of the furnace. The forming gas is injected into the furnace tube via an inlet located at the rear, while the sample is inserted into the furnace tube through the front mouth. Before insertion, the sample is placed on a quartz boat, which can be pushed into and pulled out of the furnace tube with the help of a quartz rod.

For the sake of convenience, the length of the furnace tube is considered to be divided into four regions:

1) The Rear Hot Zone (upstream of the forming gas flow).
2) The Center Hot Zone.
3) The Front Hot Zone (downstream of the forming gas flow).
4) The White Insulation located at the front (near the mouth of the tube).

The placement of the sample during insertion, annealing, and extraction are discussed in terms of there four regions or zones. Figure 4.3 shows the placement of the sample relative to these zones for annealing Nickel at 1000ºC along with the time intervals for which the sample sits at a particular point along with the temperature at that point.

The detailed annealing process is explained below:

1) Before starting the annealing process, sufficient time was allowed for the furnace to stabilize at 1000ºC.

2) The forming gas flow was started at 30 s.c.c.h. and let flow for 3 minutes to purge the entire furnace quartz tube of any contaminant gases.
3) The sample was placed with the back-side facing up on a quartz boat before inserting it into the furnace. The sample was inserted slowly into the center of the furnace in the following steps to reduce thermal stress:

    a) The sample was placed at the edge of the furnace tube for 30 seconds then pushed further ahead.

    b) The sample was placed at the center of the tube holder (white insulation isolating the quartz tube from the furnace body), for 60 seconds then pushed further ahead in the center.

    c) The sample was pushed all the way into the middle of the center hot zone.
4) The sample was placed at the center of the furnace for 3 minutes, which is defined as the actual annealing time.

5) The sample was slowly pulled out of the furnace in the following steps to reduce the thermal stress and also reduce the risk of oxidation of the Nickel dots.

    a) The sample was placed for 1 minute at the boundary between the center hot zone and front hot zone then pulled further back.

    b) The sample was placed for 2 minutes at the center of the front hot zone then pulled further back.

    c) The sample was placed at the center of the white insulation for 30 minutes to cool down. Finally, the sample was completely pulled out of the furnace.

The annealing of Nickel at such temperatures leads to the formation of Nickel Silicide (Ni_2Si) at the interface. However, the Nickel dots still exhibit rectifying behavior for annealing temperatures below 900ºC. Annealing of SiC above 900ºC results in the out diffusion of a large number of free Carbon atoms towards the surface. This out-diffusion of Carbon atoms is supposed to be the reason for the ohmic behavior of annealed Nickel contacts on SiC [11].

It was observed frequently that the Nickel dots were darkened in varying degrees after annealing. This was attributed to oxidation of Nickel during the annealing process. A layer of oxide covered the surface of the Nickel dots, which could result in problems during the measurements by preventing good electrical contact of the measurement probes with the ohmic contacts. The most obvious cause was the mouth of the furnace tube being open during the annealing process, which could easily allow the inflow of atmospheric gases into the furnace tube. Even though the forming gas continuously flowed throughout the annealing process, there was no absolute control over the ambience in the furnace tube. Also, during the cooling off period of 30 minutes, the sample was located over the white insulation region where the temperature was recorded as approximately 678ºC. This white insulation region is very close to the mouth of furnace tube and hence, the sample has higher risk of oxidation in this region. Ideally, the mouth of the furnace should be closed completely with an end-cap containing a small outlet tube for the forming gas. Also, during the cooling period, the sample should be rested in a cooler region with a neutral ambience. This suggests the use of an extension tube to the furnace whereby the sample can rest in a much cooler place and still be in the

of the forming gas. Since neither the end-cap nor the extension tube was available, a work-around was developed to reduce the risk of oxidation. An end-cap was designed using Aluminum foil which could be wrapped around the mouth of the furnace tube with a small opening in it for the push-rod. This significantly reduced the risk of oxidation; however, a more robust solution was required.

4.3.4 Deposition of Protective Layer on the Back-side

After the annealing of the back-side contacts to make them ohmic, the next goal is to deposit Schottky contacts on the front-side. Prior work done on this project has revealed that at this stage of fabrication, there is significant oxide present on the front-side [12]. The presence of an oxide layer presents an undesirable effect on the Schottky barrier and hence, additional surface treatment is recommended. Hydrofluoric Acid (HF) is widely considered to be one of the best etchants for Silicon Dioxide (SiO_2) and was used for the second surface etch. However, HF is also a known etchant of Nickel. Therefore, it was imperative that the Nickel contacts be protected during the HF etch.

A protective coating of Aluminum was deposited over the back-side contacts to protect them from getting etched during the second surface etch. A 0.5μm thick layer of Aluminum was thermally evaporated onto the back-side with an appropriate shadow mask pattern such that both the Nickel dots were completely blanketed by the Aluminum layer. The sample was then allowed to rest for 24 hours to improve the adhesion of Aluminum to the surface.

4.3.5 Second Degrease and Front-side Surface Etch

The second surface treatment was similar to the first surface clean, with some suitable changes in etch time to make sure that the Nickel dots on the back-side are not affected. The procedure for the second surface clean is listed in detail:

1) The sample was degreased by immersion in Acetone for 2 minutes followed by immersion in Methanol for 2 minutes.

2) The sample was immersed in a solution of diluted Hydrofluoric Acid (48% HF) and water in the volumetric ratio of 1:25 $HF:H_2O$ for 45 seconds.

3) The sample was rinsed in three beakers of de-ionized (DI) water for a period of 15 seconds, 30 seconds and 5 minutes respectively.

4) The sample was dried with a Nitrogen gun.

The second surface etch with a dilute solution of HF was significantly shorter than the first surface etch. The sample was immersed in HF for only 45 seconds during the second surface etch as compared to 2 minutes during the first surface etch. This was done to reduce the etching of the Aluminum protective layer by HF. Although Aluminum is deposited as the protective layer, it was observed that it still gets etched slowly by the HF. This etching of Aluminum is particularly fast over the Nickel dots, indicating that the Aluminum does not adhere particularly well to the Nickel.

4.3.6 Deposition of Schottky contacts on the Front-side

After the second surface clean, Schottky contacts were deposited on the front-side. Since the project involved investigating different metals for Schottky diodes, the fabrication process is not discussed relative to any particular Schottky metal, but rather as a general process which can be employed with suitable changes for the different metals. The deposition of Schottky contacts is also discussed in general because the same evaporator was used in the case of all metals.

The Schottky contacts were deposited on the front-side by thermal evaporation performed under high-vacuum of 5×10^{-6} Torr. The deposited Schottky dots were roughly 630μm in diameter and 0.5μm thick. Figure 4.4 exhibits the pattern of dots deposited on the front-side by the use of a suitable shadow mask. The pattern consists of 14 dots arranged in four separate rows, thereby yielding 14 Schottky diodes on one die.

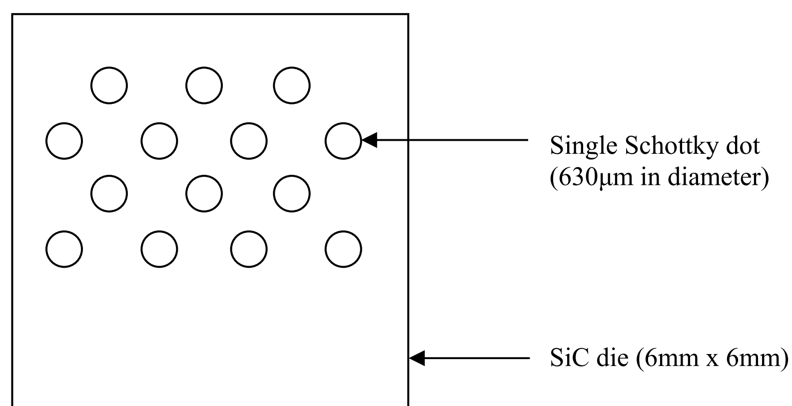

Figure 4.4 Pattern of Schottky contacts on the Front-side of the sample.

4.3.7 Removal of Protective Layer

The final step of the fabrication process is to remove the remnant of the Aluminum layer covering the back side so that the ohmic Nickel dots can be exposed for measurement purposes. Aluminum can be easily etched away with Potassium Hydroxide (KOH) without adversely affecting the Nickel contacts. However, the same cannot be said about the effect of KOH on the Schottky contacts. Along with Aluminum, KOH also readily attacks Copper. Therefore, a similar protective approach must be employed while removing the Aluminum layer to keep the Schottky contacts intact. To achieve this, the front-side of the sample was coated with nail paint and dried for at least 60 minutes. This dried nail paint thus forms a protective layer over the Schottky contacts, protecting them from the consecutive chemical treatments. The elaborate method for removing the Aluminum protective layer is listed below:

1) Apply an even coating of nail paint on the front-side of the sample, taking care not to spill any nail paint on the back-side of the sample. Let the sample sit for at least 60 minutes for the nail paint to dry completely before proceeding.

2) Immerse the sample in Potassium Hydroxide (KOH) with the back-side facing up. Let the sample sit in KOH for ample time to ensure complete etching of Aluminum from the back-side.

3) Immerse the sample in Acetone with the front-side facing up. Let the sample sit in Acetone for ample time to ensure complete removal of nail paint from the front-side.

4) The sample was rinsed in three beakers of de-ionized (DI) water for a period of 15 seconds, 30 seconds and 5 minutes respectively.

5) The sample was dried with a Nitrogen gun.

After the completion of this final step, the Schottky diode is ready for electrical measurement. The sample was stored in an airtight container for handling and moving.

4.4 Shortcomings of the Preceding Fabrication Process

The fabrication process highlighted in the previous section was successfully employed in fabricating Schottky diodes on 4H-SiC. However, there were some shortcomings in the process which caused problems during the fabrication process. As such, successful repeatability of the process could not be guaranteed. Listed below are the encountered problems in detail. The probable causes of and possible solutions to the problems are also discussed.

1) During the second front-side surface etch, the back-side Aluminum protective layer gets etched away by HF. This etching is particularly noticeable right over the Nickel dots, indicating that Aluminum does not adhere well to Nickel. Consequently, the annealed Nickel dots are exposed to the HF and hence get etched away. Since ohmic contacts are essential to provide an electrode to the substrate, even partial etching of the dots gives significant problems during electrical measurements. Also, the choice of Aluminum as the protective material is not the best one. Efforts should be made to find a better protective material which resists etching by HF.

2) During the removal of Aluminum covering the back-side by KOH, it is necessary to protect the front-side Schottky contacts from KOH. This requires coating of the front-side with nail paint. This is an additional step introduced in the process, which could probably be avoided. The Aluminum coating could be stripped with a different chemical which doesn’t chemically affect the front-side Schottky contacts. Also, a material other than Aluminum could be used to protect the back-side contacts. The chief requirements for such a material should be resistance to the HF etch, while also is easily removable by a chemical which doesn’t affect any of the Schottky metals used.

3) It was observed that during the stripping of Aluminum with KOH, the nail paint coating had a tendency of getting detached from the front-side of the sample, thereby exposing the Schottky contacts to the KOH. Also, sometimes the Schottky contacts come loose along with the nail paint coating. This was mostly observed in the case of Copper, which has poor adhesion with the surface anyhow. The probable cause of this was that the nail paint was not allowed to dry completely before proceeding with immersion in KOH. The most logical solution was to let the sample sit for 24 hours before proceeding with the removal of the Aluminum layer on back-side with KOH.

4) One of the most vital concerns with the use of nail paint was the matter of its composition. The nail paint used in the fabrication process was not an electronic grade material and there was no strict control of its composition since different manufacturers use different compositions. Also, colored nail paint consists of suspended metal flakes, which is highly undesirable from a contamination perspective. Therefore, clear nail paint is preferred over the colored nail paint.

After reviewing the shortcomings in the above process, the most preferable solution was to substitute another material for Aluminum as the back-side protective layer. The requisites for this material were as follows:

1) The material should be strongly resistant to HF.

2) The material should be removable by a chemical which does not adversely affect any of the Schottky metals or the Nickel contacts.

3) The material should be an electronic grade material with high purity.

The two prospective materials readily available were nail paint and soft-baked positive photoresist. While nail paint was not electronic grade, it met the first two criteria perfectly. Trial runs proved that dried nail paint was resistant to HF and it was readily removable by Acetone which does not adversely affect metals. However, the concerns about using nail paint were that it was not an electronic grade material and there was no strict control over its composition, thereby inherently carrying a risk of contamination.

In contrast, soft-baked positive photoresist solved all of these problems. Positive Photoresist S1813 is an electronic grade material readily available in the cleanroom. Soft-baked positive photoresist resists HF very well, and it can be easily stripped by Acetone, which does not attack metals. Trial runs proved that S1813 baked at 90ºC for 20 minutes and then cooled for 10 minutes adequately survived in dilute Hydrofluoric acid HF:H2O (1:5) for more than 5 minutes. Therefore, it was concluded that soft-baked Positive Photoresist S1813 should be used as the protective coating to protect the back-side Nickel contacts during the front-side surface etch.

4.5 Revised Procedure for Fabrication of Schottky Diode

The revised fabrication process for SiC Schottky diodes incorporated the changes proposed in the previous section. Soft-baked positive photoresist was used as the protective material for the back-side ohmic contacts. Thus, the revised fabrication process up to the annealing of the ohmic contacts is nearly identical to the prior process. However, the use of photoresist as the back-side protective layer required some further changes in the process; mainly in the front-side surface clean. Also, for annealing purposes, an extension tube to the main furnace tube referred to as an elephant tube was obtained for use. This modified the annealing slightly, which will be discussed in greater detail later in this section. Overall, the revised fabrication process was found to be more

reliable, streamlined, and robust in implementation. The detailed steps of the revised fabrication process are listed below.

4.5.1 Initial Degrease and Back-side Surface Etch

The first step in the fabrication process is identical to the one discussed in sub-section 4.3.1. Listed below are these various processes in detail.

1) The sample was degreased by immersion in Acetone for 2 minutes followed by immersion in Methanol for 2 minutes.
2) The sample was immersed in a solution of diluted Hydrofluoric Acid (48% HF) and water in the volumetric ratio 1:25 HF:H_2O for 2 minutes.
3) The sample was rinsed in three beakers of de-ionized (DI) water for a period of 10 seconds, 20 seconds and 30 seconds respectively.
4) The sample was dried with a Nitrogen gun.

During the degreasing of the sample with Acetone and Methanol, care was taken to flip the sample upside-down halfway through each step to make sure that either surface got equal exposure to the Acetone and Methanol. However, during the etching of the sample with HF, the sample was placed with back-side facing up so that the back-side got the most exposure to the acid. The reason for this was since the next step was to deposit the Nickel contacts on the back-side, more emphasis was given to cleaning the back surface. As compared to the prior process, the water rinses were considerably shortened. The main reason for this was to avoid re-oxidation of the surface in the final water rinse. Therefore, the final water rinse period was shortened from 5 minutes to 30 seconds.

4.5.2 Deposition of Nickel on the Back-side

This step was also identical to the one in the prior fabrication process as discussed in sub-section 4.3.2. For creating the ohmic contacts, approximately 2700Å of Nickel was deposited by thermal evaporation onto the back-side of the sample. The thermal evaporation was performed at a pressure of 5 x 10^{-6} Torr. During the evaporation process, the sample lies on top of a suitable shadow mask so that the Nickel is deposited in the desired pattern. The pattern used for depositing the Nickel dots is shown in Fig. 4.5. This pattern is similar to the one shown in Fig. 4.2, with the slight change that instead of depositing two dots of 2mm diameter each, one dot of 4mm diameter and two dots of 1mm diameter each were deposited. This essentially provides a large ohmic contact covering most of the substrate area, while the two smaller dots are used for characterizing the ohmic behavior. The details of the measurements are discussed in Chapter 5.

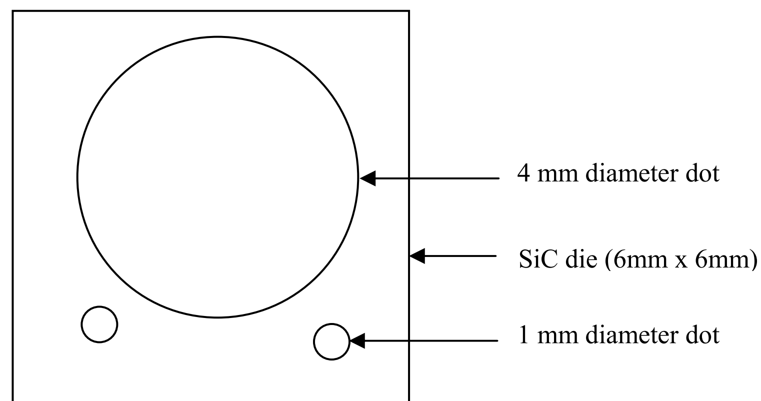

Figure 4.5 Pattern of Ohmic contacts on the back-side of 4H-SiC sample.

4.5.3. Annealing of Nickel to form Ohmic Contacts

This is the first step where the revised process significantly deviates from the old process. As discussed at the end of sub-section 4.3.3, the Nickel dots were frequently oxidizing during the annealing step. Two solutions considered to that problem were either the use of an end-cap or more preferably, the use of an extension tube to the main furnace tube. Such an extension tube, also known as an elephant tube was obtained and attached to the mouth of the main furnace tube. The main advantage of using the elephant tube was that the sample could now be cooled at some distance away from the heating coils while remaining in the forming gas (10% Hydrogen and 90% Argon). This significantly reduced the risk of oxidation and also decreased the time required by the sample to cool.

Figure 4.6 shows a detailed schematic of the furnace tube with the extension or elephant tube attached. The elephant tube has a small opening at its far end to insert the quartz rod to push/pull the quartz boat inside the furnace. Figure 4.7 shows the temperatures at various points in the furnace tube when the furnace is set to operate at 1000ºC. The figure also shows the annealing time intervals for which the sample was rested at each marked position during the annealing process.

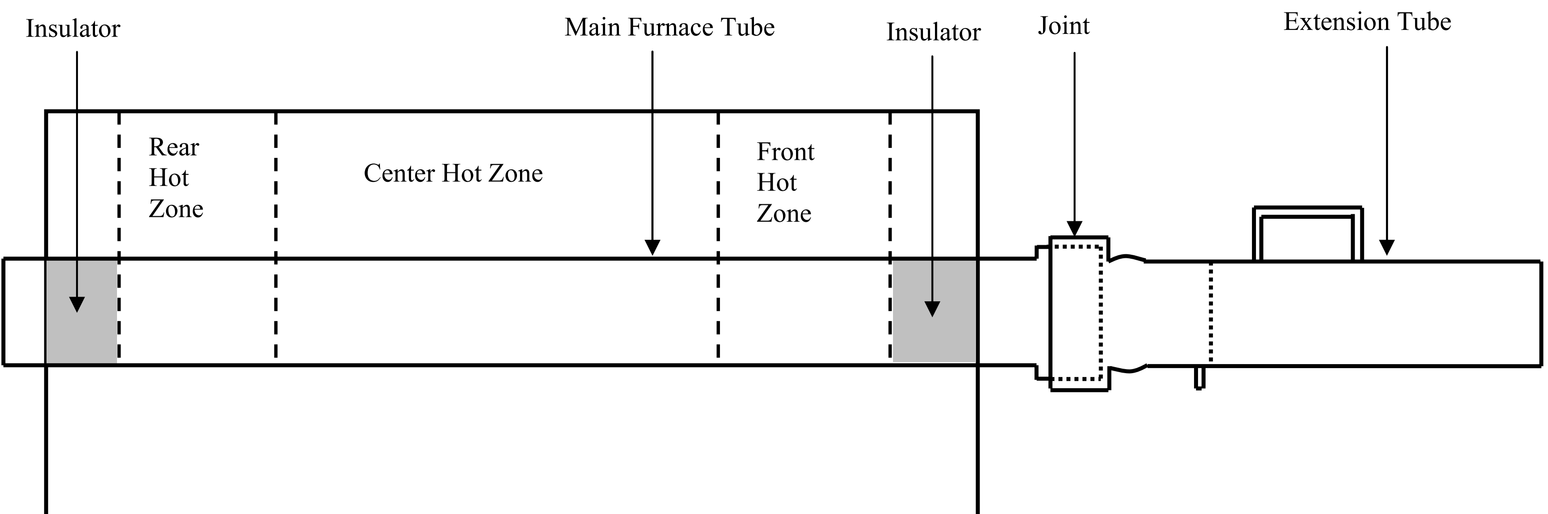

Figure 4.6 Schematic of the Annealing Furnace tube with the extension tube attached to the main furnace tube.

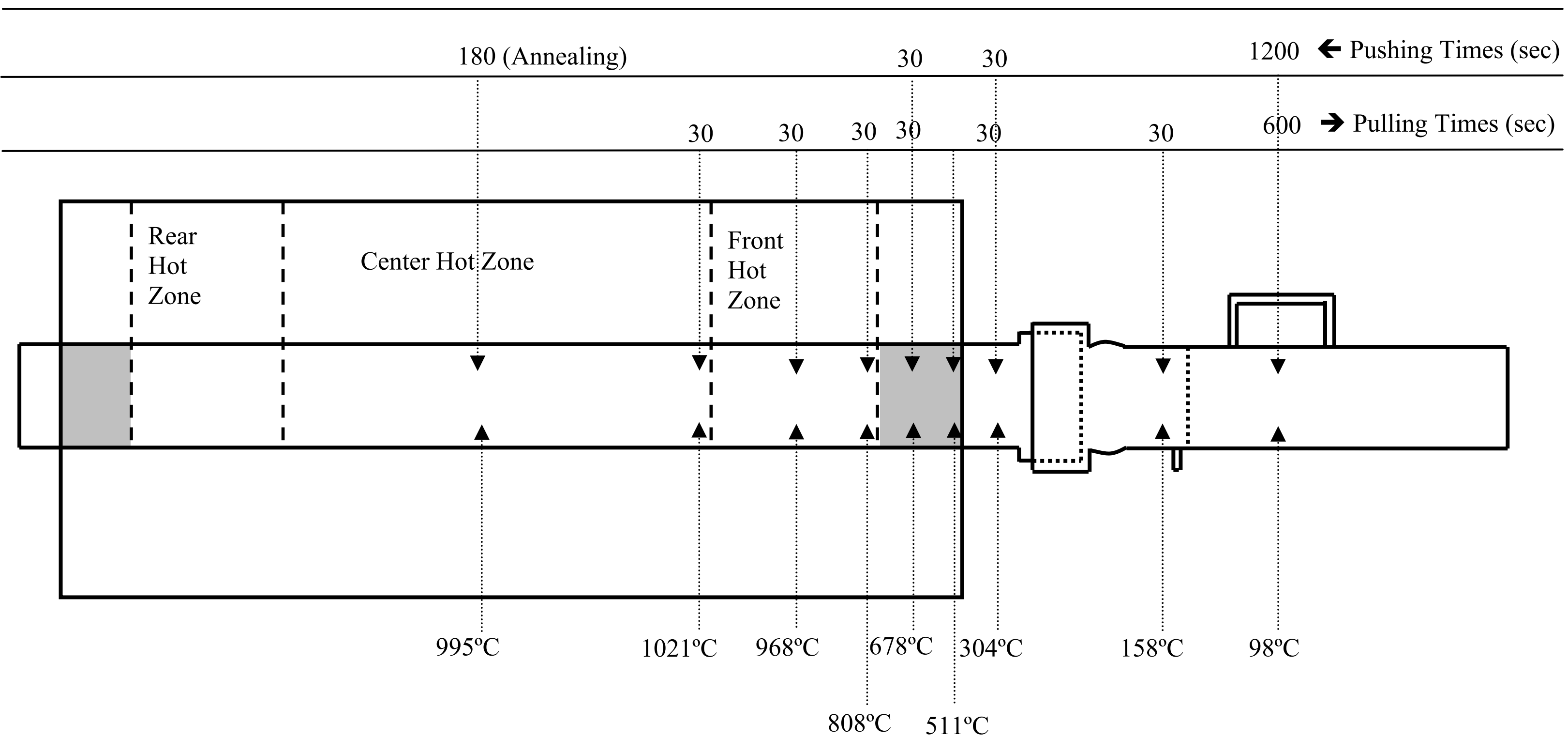

Figure 4.7 Schematic of Annealing Furnace tube and Extension tube for Annealing Nickel at 1000ºC.

The detailed process for annealing Nickel at 1000ºC is given below:

1) Before starting the annealing process, sufficient time was allowed for the furnace temperature to reach and stabilize at 1000ºC.

2) The forming gas flow was started at 10 s.c.c.h. and flowed for 10 minutes to purge the entire furnace quartz tube of any contaminant gases.

3) The sample was placed with the back-side facing up on a quartz boat before inserting it in the middle of the extension tube. The extension tube was then attached to the main furnace tube.

4) The entire setup was left undisturbed for 20 minutes to completely fill the extension tube with the forming gas and purge it of the atmospheric gases. Halfway through this waiting period, the gas flow was increased to 30 s.c.c.h.

5) The sample was inserted into the furnace slowly in the following steps to reduce thermal stress:

    a) The sample was placed for 30 seconds in the main furnace tube just beyond the joint with the extension tube then pushed further ahead.

    b) The sample was placed for 30 seconds at the center of the tube holder (white insulation isolating the quartz tube from the furnace body), then pushed further ahead.

    c) The sample was then pushed all the way into the middle of the center hot zone.

6) The sample was placed at the center of the furnace for 3 minutes, which is the actual annealing time.

7) The sample was slowly pulled out of the furnace in the following steps to reduce the thermal stress and also reduce the risk of oxidation of the Nickel dots:

    a) The sample was placed for 30 seconds at the boundary between the center hot zone and front heating zone then pulled further back.

    b) The sample was placed for 30 seconds at the center of the front hot zone then pulled further back.

    c) The sample was placed for 30 seconds at the boundary of the front hot zone and the white insulation.

d) The sample was placed at the center of the white insulation for 30 minutes to cool down.

e) The sample was placed for 30 seconds at the downstream boundary of the white insulation near the edge of the furnace body

f) The sample was placed for 30 seconds in the main furnace tube near the joint with the extension tube.

g) The sample was carefully pulled over the joint and then let rest in the extension tube.

h) The sample was placed for 10 minutes in the middle of the extension tube to cool off.

i) Finally, the extension tube was pulled off the main furnace tube. The quartz boat with the sample on it was extracted from the extension tube.

The annealing step of the new fabrication process differs significantly from that of the old process. First of all, care has to be taken while attaching the extension tube to the main furnace tube to avoid damaging the quartz tubes. The wait time before pushing the sample into the furnace is also significantly higher. The principal reason behind this was the added volume of the extension tube to be purged. It is also seen that the sample is pulled out slower from the furnace. There is a very big temperature gradient across the front insulator where the temperature changes by almost 400ºC in the length of a few inches. Therefore, the sample is pulled out slower in this region by adding more wait periods.

An obvious advantage of the use of the extension tube is that the sample cools off at a much lower temperature. The sample is rested for 10 minutes in the middle of the extension tube where the temperature is less than 100ºC. Hence, the sample cools off

quicker than it did in the old process. In the prior fabrication process, the sample was cooled off in the white insulator region, where the temperature is more than 500ºC. Therefore, when the sample was pulled out of the furnace, there was significant risk of oxidation of the Nickel dots as the sample was still hot. With the use of the extension tube, the sample is allowed to cool off in a region which is at a distance from the opening to the atmosphere. As an added precaution, the opening in the extension tube was covered with Aluminum foil during the actual annealing period (3 minutes) and during the cooling off period (10 minutes).

4.5.4 Deposition of the Protective Layer on the Back-side

The next step in the fabrication process is to apply a protective coating over the back-side contacts to protect them during the second surface etch. As discussed in Section 4.4, soft-baked positive photoresist was chosen to protect the back-side Nickel dots. The photoresist was evenly applied on the back-side of the sample with the use of a plastic applicator. While applying, care was taken not to let any photoresist spill over to the front-side. Then the sample was placed with the back-side facing up on a hot plate pre-heated to 90ºC. The sample was allowed to be heated for 20 minutes, after which the sample was lifted from the hot plate and cooled for 10 minutes. At the end of cooling period, the back-side of the sample was evenly covered with a soft film of photoresist which adequately protects the Nickel dots during the second surface etch.

In the initial stages of implementing the new fabrication process using photoresist, it was observed that while heating the sample at 90ºC for 20 minutes, small bubbles formed in the photoresist. These bubbles are initially small, but tend to gather towards the center of the sample. Although no adverse effects were evident from this phenomenon, it was still a matter of concern since the presence of bubbles suggests less photoresist protecting the sample in that area. The formation of bubbles was attributed to the photoresist solvent evaporating during the heating of the sample. To counter the formation of bubbles in the photoresist, a much thinner layer of photoresist was applied. This solved the problem of the bubbles since the bubbles formed could rise through the photoresist and be released into the air. Although a thinner layer of photoresist may sound contradictory to the goal of protecting the Nickel dots, the obtained layer was still much thicker than the thicknesses achieved by the conventional spin coating application method.

4.5.5 Second Degrease and Front-side Surface Etch

The use of soft-baked positive photoresist necessitated some major changes in this step of the new fabrication process. In the old process, the front-side surface clean was achieved by degreasing in Acetone and Methanol followed by a short HF etch. However, similar degreasing cannot be performed in the revised fabrication process due to the photoresist coating being soluble in both Acetone and Methanol. One possible solution was to completely remove the degreasing part and proceed directly with the HF etch. However, this was considered to be the last resort, and efforts were made to introduce a substitute surface treatment prior to the HF etch.

The use of the RCA clean procedure is very common in the semiconductor industry and is one of the most standard surface treatments employed. The RCA cleaning procedure has three major steps used sequentially [18], [19]:

1) Removal of insoluble organic contaminants with a solution of 5:1:1 H_2O:H_2O_2:NH_4OH.

2) Removal of a thin silicon dioxide layer using a diluted solution of 5:1 H_2O:HF solution.
3) Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O:H_2O_2: HCl.

Since the primary aim of the degreasing step was the removal of organic contaminants, the substitution for Acetone and Methanol of the diluted solution of Ammonium Hydroxide (NH_4OH) and Hydrogen Peroxide (H_2O_2) seemed to be the ideal candidate for the new pre-etch surface treatment. The use of H_2O_2 leads to the formation of a non-porous oxide layer on the SiC surface, which can be removed later by HF,

exposing the pure SiC surface [20]. The modified degreasing and surface etch process is described in detail as follows:

1) The sample was degreased in a 5:1:1 H_2O:H_2O_2:NH_4OH solution for 3 minutes. Throughout this time interval, the sample was immersed in the solution with the front-side facing up.

2) The sample was immersed in a solution of diluted Hydrofluoric Acid (48% HF) and water in the volumetric ratio 1:25 HF:H_2O for 3 minutes.

3) The sample was rinsed in three beakers of de-ionized (DI) water for a period of 10 seconds, 20 seconds and 30 seconds respectively.

4) The sample was blow-dried with a Nitrogen gun.

The surface etching with HF lasts for 3 minutes in the revised process as compared to 45 seconds in the old process. The longer surface etch provides a more thorough surface clean and the photoresist coating on the back-side adequately protects the Nickel dots on the back-side.

4.5.6 Deposition of Schottky contacts on the Front-side

The deposition of the Schottky contacts is accomplished using thermal evaporation performed under a high vacuum of $5x10^{-6}$ Torr. The as-deposited dots were approximately 630μm in diameter and 0.5μm thick. The pattern of the Schottky dots is the same one as that shown in Fig. 4.4. The pattern consists of 14 dots arranged in four separate rows, thereby yielding 14 Schottky diodes on one die.

4.5.7 Removal of Protective Layer

The final step is to remove the protective Photoresist coating on the back-side of the sample. This is accomplished by immersing the sample in Acetone until the entire photoresist film is dissolved. As a precaution, after it was visual confirmation that the photoresist film was dissolved, the sample remained in Acetone for 2 more minutes to ensure that all of the photoresist coating was removed. Finally, the sample was rinsed in three beakers of de-ionized (DI) water for a period of 10 seconds, 20 seconds and 30 seconds respectively and then was blow-dried with a Nitrogen gun.

This removal method was substantially quicker and more convenient than the intricate procedure employed in the old fabrication process. The new process completely disposes of the need to use KOH, which poses a significant threat to the Schottky contacts on the front-side. It also removes the additional step of covering the front-side dots while stripping the protective layer from the back-side.

After removing the protective layer from the back-side, the sample is ready for measurement. At this stage, the SiC die has 14 Schottky contacts on the front-side with Nickel dots on the back-side functioning as ohmic contacts. Current vs. Voltage (I-V) and Capacitance vs. Voltage (C-V) measurements were performed on the 14 Schottky diodes before proceeding with the annealing of the Schottky contacts. The details of these measurements are discussed in detail in the next chapter.

4.6 Annealing of the Schottky Contacts

The next step is to anneal the Schottky contacts at a suitable time and temperature. Thermal annealing of Schottky contacts has been shown to lead to the following effects on the performance of the Schottky diode [21]:

a) Reduction in leakage current.

b) Increase in barrier height.

c) Improvement in ideality factor.

Thermal annealing makes the metal-semiconductor contact more intimate, thus lessening the barrier lowering phenomenon caused by the presence of a thin interfacial layer [21]. This results in increasing the barrier height. Annealing can also reduce the reverse current in the Schottky diode by eliminating low-barrier secondary diodes formed due to the presence of barrier inhomogeneities [22].

The ideal approach for determining the optimum annealing time and temperature for each metal-SiC combination would be to identify a specific temperature range and then perform annealing at incremental temperatures within that range. The Schottky parameters of each sample would then be extracted and compared, focusing on obtaining the highest Schottky barrier height with the lowest ideality factor. However, lack of resources prohibited annealing of such a large number of samples. The optimum combination of annealing time and temperature was chosen for Cu/4H-SiC, Al/4H-SiC and Au/4H-SiC after carefully reviewing the literature on the work done on identical or

similar metal-semiconductor combinations. Table 4.1 shows the annealing times and temperatures employed in this project for annealing Cu, Al, and Au on 4H-SiC.

Table 4.1 Annealing Times and Temperatures for different metals on 4H-SiC

Metal	Annealing Time (seconds)	Annealing Temperature(ºC)	Reference
Copper (Cu)	300	500	[23-25]
Aluminum (Al)	300	600	[5], [26], [27]
Gold (Au)	300	500	[5]

The procedure for annealing the Schottky contacts remains the same as that described in Section 4.5.3 for annealing ohmic contacts. The only factor that changes is the furnace temperature and the actual annealing time when the sample is in the middle of the center heating zone. The push/pull procedure remains the same, with identical stop points along the furnace tube length and the extension tube.

4.7 Conclusions

Cu/4H-SiC, Al/4H-SiC, and Au/4H-SiC Schottky diodes were designed and fabricated as a part of our research on the effect of annealing on the Schottky parameters. A new, improvised fabrication procedure was developed to eliminate the shortcomings of the old fabrication process. Soft-baked photoresist was effectively employed as a protective material to protect the Nickel ohmic contacts during the front-side surface etch. Overall, the new fabrication process was found to be very streamlined and easy to follow. An extension tube to the main furnace tube was successfully employed to anneal the Ohmic and Schottky contacts. The use of the extension tube greatly reduced the risk of oxidation of Nickel dots in the furnace during annealing. The Schottky contacts were annealed at a suitable combination of time and temperature in order to study the effects of annealing on the Schottky parameters.

CHAPTER 5

MEASUREMENTS AND PARAMETER EXTRACTION

The Schottky diodes were characterized on the basis of their most important electrical parameters, some of which include Schottky Barrier Height (SBH, ϕ_B), ideality factor (η), and on-state series resistance (R_{on}). In this chapter, the determination of the parameters of the fabricated diodes is presented in detail. Some of the parameters are determined using more than one measurement technique, which is a means of verifying the obtained values. Each measurement technique is explained elaborately, starting with the theory behind the method. Then measurement of the required data from the physical sample is presented and explained, highlighting the equipment and software tools used. Finally, the extraction of the required parameters from the obtained data is shown.

The surface characterization of one of the samples is also presented in this chapter. Surface characterization differs notably from the electrical characterization techniques, because surface characterization focuses on obtaining physical and chemical information on the sample rather than electrical parameters. However, a combination of electrical and surface characterization provides insight on the effects of fabrication processes on the electrical parameters. This combination is widely adopted in research on SiC devices. In this project, such an approach was employed to study the effect of annealing on the Schottky parameters of Al/4H-SiC.

5.1. Measurement Techniques

During the course of this project, the following measurement techniques were used for obtaining physical, electrical and chemical data:

1) Profilometry

   Profilometry is the measurement of a feature's length or depth, usually at the micron or nanometer scale. The instrument used for this kind of measurement is called a profilometer. In a profilometer, a diamond stylus is moved vertically until it comes into contact with the sample, and then it is moved laterally across the sample for a specified distance. The profilometer measures small variations in the surface topology as a function of lateral position. While it does not provide any electrical parameters or any chemical compositions, it is very useful in determining the roughness and the curvature of the surface. In this project, the profilometer was actively used for determining surface profiles of the substrate and the metal contacts. The primary use of the profilometer was in determining the dimensions of the metal contacts and their thicknesses.

2) Current-Voltage (I-V) Measurements

Current-Voltage or I-V Measurements are essentially the measurement of current flowing between two contacts as a function of voltage. This is by far the most common type of electrical measurement performed on semiconductor devices. Many parameters can be extracted from the I-V measurements. In the case of Schottky diodes, for performing I-V measurements the current is measured between the anode and the cathode while the voltage applied between the two terminals is varied between set limits. The plot of current measured as a function of applied voltage is called the I-V characteristic curve. Depending upon the polarity of the voltage applied, the measurements are either Forward or Reverse I-V characteristics. For the forward I-V measurements, the voltage applied to the anode is positive, which forward-biases the Schottky Diode. Typically the forward I-V curves are used to extract the Schottky Barrier Height, the ideality factor and the on-state series resistance. The reverse I-V curves are usually used to measure the breakdown voltage of the diode by reverse biasing it well-beyond the normal operating voltages. The theory behind I-V measurements and the manipulation of raw data to extract the required parameters is discussed in detail in Section 5.2.

3) Capacitance-Voltage (C-V) Measurements

Capacitance-Voltage or C-V measurements are measurement of the capacitance C between two terminals as a function of voltage. In the case of Schottky diodes, the voltage applied between anode and cathode is of negative polarity for C-V measurements. The depletion region inside the semiconductor, with the ionized dopants inside it behaves like a capacitor. The variation of the negative voltage changes the width of the depletion region, thereby changing the capacitance. The plot of capacitance C versus voltage V is called the C-V curve. The C-V curves are useful for the determination of Schottky Barrier Height, the built-in voltage, the doping concentration of the substrate, and the breakdown voltage of the diode. The theory behind the C-V measurements and the extraction of the desired parameters from raw data is further detailed in Section 5.3.

4) Surface Analysis

Surface analysis is the broad term given to the investigation of the surface phenomenon to understand the properties and reactivity of the surface of a material. Different techniques deal with different aspects and different levels of surface. The choice of a particular surface analysis technique is largely determined by the nature of required information, the type of surface, and the resolution. Almost all of the surface analysis techniques involve bombardment of the surface with particle radiation and the detection of the out-coming

radiation from the surface. Most of the surface analysis techniques are carried out in vacuum. The principal reason for this is that particles are scattered by the molecules in the ambient gas and thus interfere with the analysis. Even photon-based techniques require vacuum since gas-phase absorption of photons can occur with the ambient molecules. The surface analysis technique used in this project was X-ray Photoelectron Spectroscopy (XPS) also known as Electron Spectroscopy for Chemical Analysis (ESCA). The choice of this technique along with a detailed explanation of its functioning is elaborated in Section 5.4. This technique is a very popular and information-rich method. Basic XPS provides qualitative and quantitative information on almost all elements present. More sophisticated application of this method yields detailed information about the chemistry, organization, and morphology of the surface. In this project, XPS was used to analyze the sample surface after annealing to study the effect of annealing on the metal-semiconductor interface.

5.2. Current-Voltage (I-V) Measurements

5.2.1 Theory

According to the ideal diode equation, the current density of a forward-biased diode is given by

$$J = J_s\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right] \tag{5.1}$$

where η is the ideality factor and V is the applied voltage. The reverse saturation current density of the diode J_s is given by

$$J_s = A^{**}T^2 \exp\left\{-\frac{q\phi_B}{kT}\right\} \tag{5.2}$$

where A^{**} is the Richardson's constant. Assuming that the value of exponential term in Equation 5.1 is much higher than 1, the ideal diode equation becomes

$$J = J_s\left[\exp\left(\frac{qV}{\eta kT}\right)\right] \tag{5.3}$$

Taking the natural logarithm of both sides of Equation 5.3, we obtain the following relationship:

$$\ln(J) = \ln(J_s) + \frac{qV}{\eta kT} \qquad 5.4$$

This equation is in the form of a linear equation from which we get the slope and intercept as

$$Slope = \frac{q}{\eta kT} \qquad 5.5$$

$$Y - Intercept = \ln(J_s) \qquad 5.6$$

Thus, the ideality factor η can be extracted from the slope of the linear region of the I-V characteristic, while the Schottky Barrier Height ϕ_B can be extracted from the intercept and Equation 5.2.

The method to determine ϕ_B and η as shown above is for an ideal diode, which neglects the diode series resistance. Hence, while the above equations are sufficient to determine ϕ_B and η, the diode series resistance cannot be determined. To extract the series resistance of the diode from the I-V measurements, a procedure developed by Cheung et. al. was employed [28]. The effect of a diode series resistance is usually modeled as the series combination of an ideal diode and a resistor R through which the

diode current I flows. The effect of this resistor can be incorporated into equations 5.1 and 5.3 by replacing the applied voltage V with an effective applied voltage (V-IR). This effective voltage is the actual voltage that gets applied between the anode and the cathode of the diode. Thus, we can rewrite the ideal diode equation 5.3 to account for series resistance, which can be written as:

$$J = J_s \exp\left(\frac{q(V - IR)}{\eta kT}\right) \qquad 5.7$$

Taking the natural logarithm of both sides and rearranging writing in terms of the applied voltage V, we obtain:

$$V = AJR + \eta\phi_B + \frac{\eta kT}{q}\ln\left(\frac{J}{A^{**}T^2}\right) \qquad 5.8$$

where A is the area of the diode. Differentiating Equation 5.8 with respect to ln(J) and rearranging the terms, we obtain:

$$\frac{dV}{d\ln(J)} = AJR + \frac{\eta kT}{q} \qquad 5.9$$

The plot of dV/dln(J) versus current density J is linear in nature and the slope of this graph is equal to AR. Since the area of the diode is known, the series resistance can be easily calculated from the determined slope.

5.2.2 Data Plotting and Extraction of Parameters

I-V measurements were performed with a Hewlett-Packard 4156B Semiconductor Parametric Analyzer interfaced with a Micromanipulator Probe Station. For the forward-biased measurements, the voltage was varied between 0V and 5V in steps of 10mV. The current compliance limit was set at 100mA. The data obtained from the HP4156B was plotted and analyzed using Kaleidagraph 3.5 by Synergy Software. The current density J was plotted on a logarithmic scale versus the applied voltage V. The resulting plot exhibits a linear region in the low voltage range of the semi-log.

Such a J-V characteristic curve is shown in Figure 5.1. The linear region of Figure 5.1 extends over eight orders of magnitude. The equation of exponential curvefit to the linear region of the semilog J-V curve is of the form:

$$y = M_0 \exp(M_1 x) \qquad 5.10$$

where M_0 and M_1 are the curvefit parameters. The correlation coefficient is also displayed, which should be unity to indicate a perfect curvefit. Applying an exponential curvefit to the linear region of the J-V curve in Figure 5.1, we obtain the values of M_0 and M_1 as 2.5565e-17 and 35.34 respectively. The correlation coefficient of the exponential

curvefit is 0.99555. Such a value close to unity indicates that the curvefit values fit the experimental data quite well.

Since the current density J is plotted on the Y-axis and the applied voltage is plotted along X-axis, equation 5.10 can be rewritten as

$$J = M_0 \exp(M_1 V) \quad 5.11$$

Comparing Equations 5.11 and 5.3, we see that M_0 is the reverse saturation current J_s and M_1 is equivalent to $q/\eta kT$ according to our model.

Thus, the ideality factor η can be easily obtained by the following equation:

$$\text{Ideality Factor } \eta = \frac{q}{M_1 kT} \quad 5.12$$

From Equation 5.2, taking the natural logarithm of both sides, we obtain:

$$\ln(J_s) = \ln(A^{**}T^2) - \frac{q\phi_B}{kT} \quad 5.13$$

Since M_0 is equivalent to J_s, we obtain the Schottky Barrier Height ϕ_B from:

$$\phi_B = \frac{kT}{q}\left[\ln\left(A^{**}T^2\right) - \ln\left(M_0\right)\right] \qquad 5.14$$

The values of M_0 and M_1 are obtained from the exponential curvefit to the linear region of semilog J-V curve in Figure 5.1. Using these values in Equations 5.12 and Equation 5.14, we obtain the value of ϕ_B as 1.263eV and the value of η as 1.094.

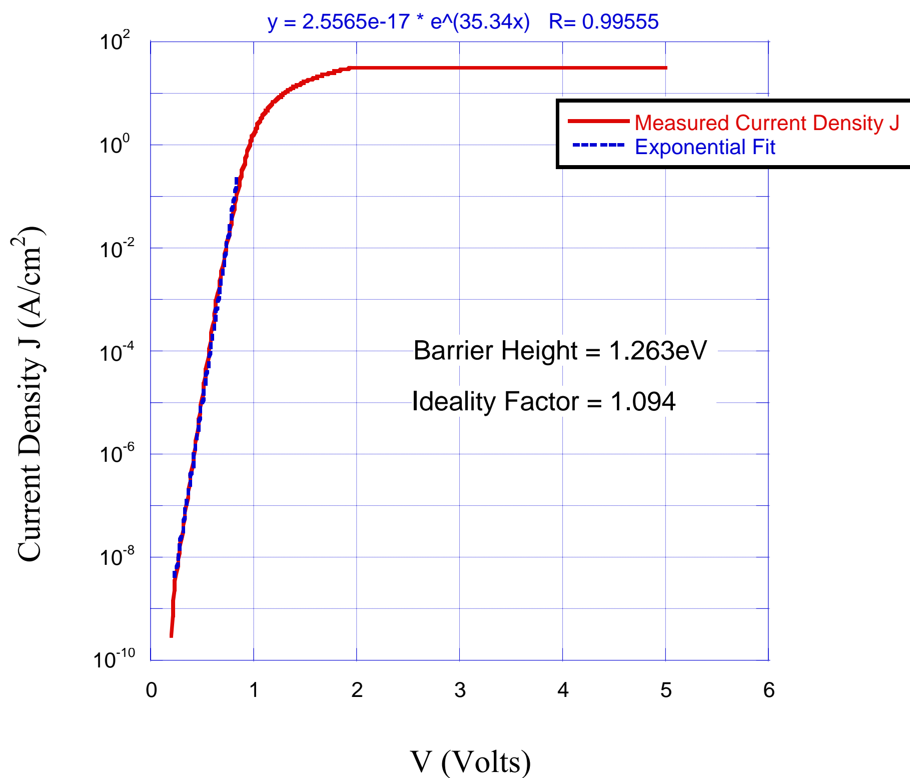

Figure 5.1 Forward I-V Characteristics of a Cu/4H-SiC Schottky Diode.

For calculation of the barrier height ϕ_B, we need the value of Richardson's constant. The theoretical value of A^{**} for 4H-SiC is 146 A/cm^2K^2 [5], [29], [30]. The

theoretical value of A^{**} can be verified by a simple calculation. The Richardson's constant is assigned to replace a collection of other constants [6]:

$$A^{**} = \frac{4\pi q m_n^* k^2}{h^3} \qquad 5.15$$

where m_n^* is the effective electron mass for 4H-SiC. Substituting the value of m_n^* as $1.217m_0$ [30] in Equation 5.15, the theoretical value of A^{**} is approximately 146 A/cm^2K^2.

For extracting the series resistance of the diode, the function *d*V*d*ln(*J*) was plotted versus J for the same experimental data used in Figure 5.1. Such a plot is shown in Figure 5.2. The plot is linear and a linear curve is fit to the plot to obtain the slope. As seen in Equation 5.9, the slope of such a curve is given by AR where A is the area of the diode and R is the series resistance of the diode. Thus, R was easily calculated from the slope of the plot as 13.78 ohms.

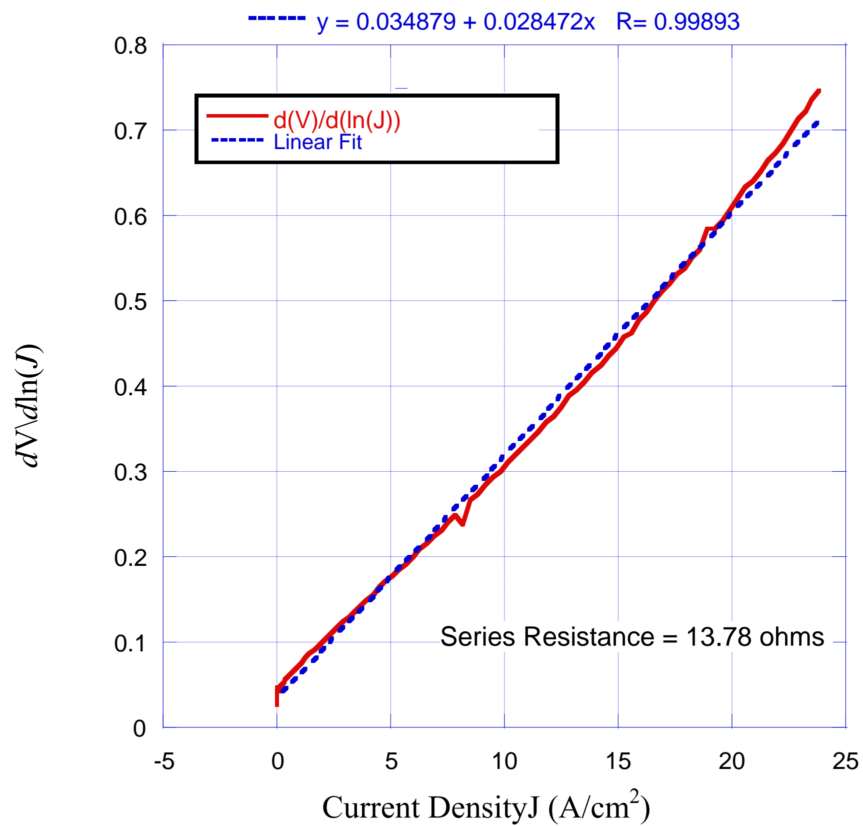

Figure 5.2 Plot of *d*V*d*ln(*J*) vs. J for extracting Diode Series Resistance

5.3 Capacitance-Voltage (C-V) Measurements

5.3.1 Theory

The capacitance per unit area C' in a n-type Schottky diode is given by [6], [31]:

$$C' = \sqrt{\frac{q\varepsilon_s N_d}{2(V_i - V_a)}} \qquad 5.15$$

where V_a is the applied voltage, V_i is the built-in voltage and N_d is the donor doping concentration. In reverse bias, Va = $-V_R$ where V_R is the magnitude of the applied reverse voltage. Thus, Equation 5.15 becomes

$$C' = \sqrt{\frac{q\varepsilon_s N_d}{2(V_i + V_R)}} \qquad 5.16$$

Rearranging the terms in Equation 5.16, we can write,

$$\left(\frac{1}{C'}\right)^2 = \left(\frac{2}{q\varepsilon_s N_d}\right)V_R + \frac{2V_i}{q\varepsilon_s N_d} \qquad 5.17$$

The above equation is in the form of a linear equation from which we obtain the slope and intercept as

$$Slope = \frac{2}{q\varepsilon_s N_d} \qquad 5.18$$

$$Y - Intercept = \frac{2V_i}{q\varepsilon_s N_d} \qquad 5.19$$

The plot of 1/C'2 versus V_R is linear in nature and the doping concentration N_d can be extracted from the slope of the plot. Substituting its value into Equation 5.19, the built-in voltage V_i can be extracted from the Y-intercept. The Schottky barrier height can be determined from the relationship,

$$\phi_B = V_i + \phi_n \qquad 5.20$$

where ϕ_n is the energy difference between E_C and the Fermi level E_F and is given by:

$$\phi_n = E_C - E_F = \frac{kT}{q}\ln(\frac{N_c}{N_d}) \qquad 5.21$$

The value of N_d obtained from the C-V measurements can also be used to confirm the actual doping density of epitaxial layer of the substrate.

5.3.2 Data Plotting and Extraction of Parameters

C-V measurements were taken using a Deep Level Transient Spectrometer by Sula Technologies, interfaced with a Micromanipulator Probe Station. The applied reverse voltage was varied from 0V to -10V in steps of 0.25V. The measured data was plotted using the Sula DLTS software. The "Analysis" option provided in the software plots the $1/C'^2$ versus the reverse voltage and automatically applies a linear curvefit to the plot to extract the doping concentration N_d and the built-in voltage V_i. This convenient functionality of the software was used to determine the built-in voltage V_i for all the Schottky devices.

In Figure 5.3 we present a sample plot and its analysis as provided by the Sula DLTS software. The plot on the left is the raw capacitance versus voltage curve. The plot on the right is $1/C'^2$ plotted as a function of voltage along with the linear fit to the data. The extracted V_i and N_d values are shown on the top of the software window. The obtained values of N_d were very similar to the actual doping concentration of the SiC substrates. From equations 5.20 and 5.21 the barrier height was calculated using the extracted value of built-in voltage V_i.

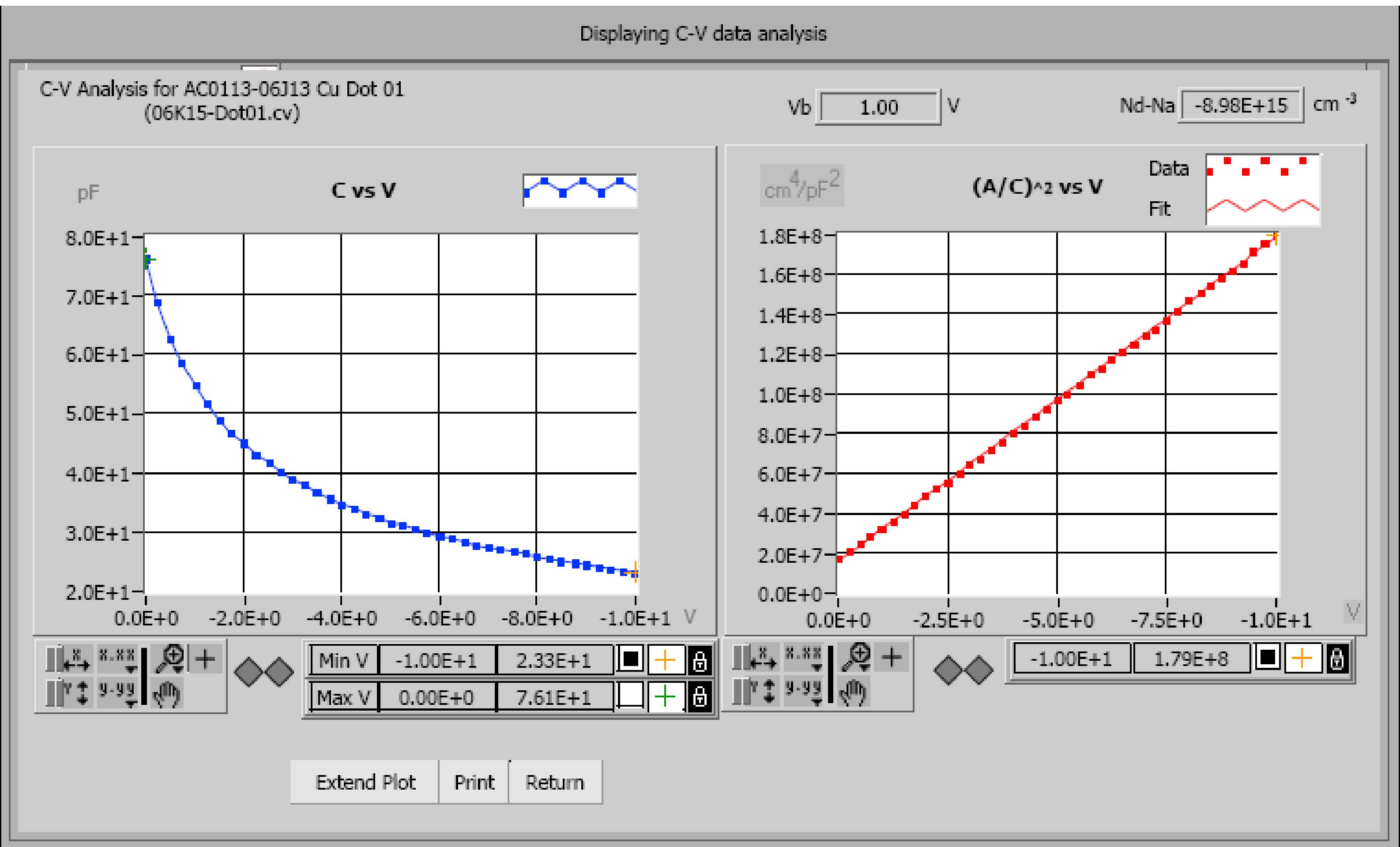

Figure 5.3.C-V Characteristics of a Schottky Diode as obtained from Sula Software for extracting built-in voltage V_i and doping density N_d.

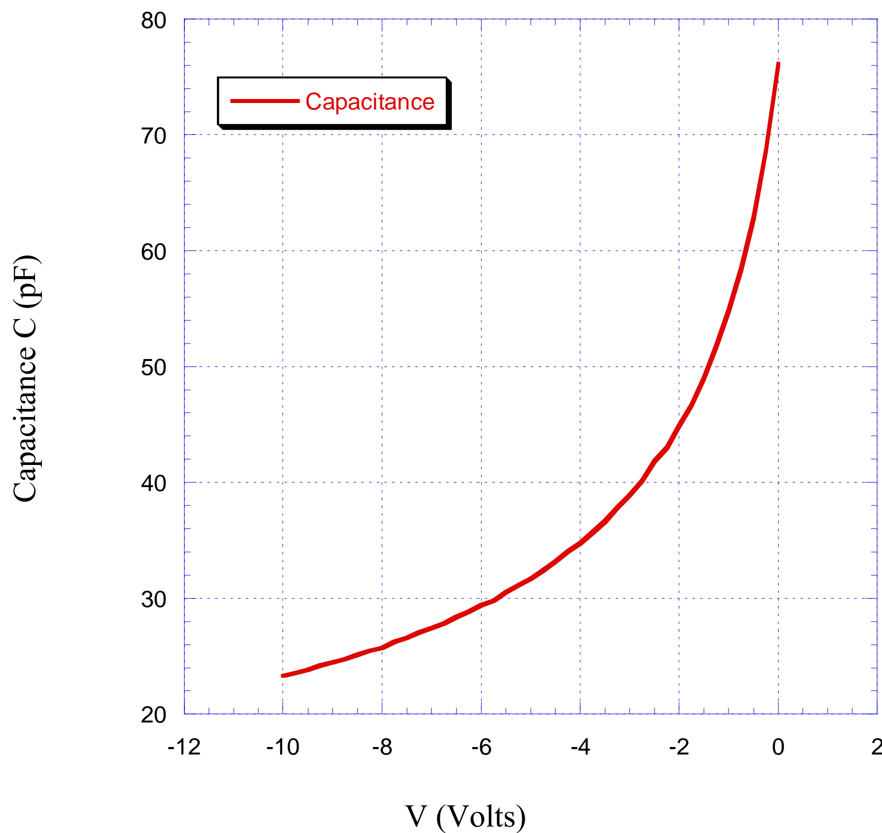

Figure 5.4 C-V Characteristics of a Cu/4H-SiC Schottky Diode.

In Figure 5.4, we show the plotted C-V characteristic for the measurement data collected for a Cu/4H-SiC diode using the Sula DLTS system as shown in Figure 5.3. As explained previously in Section 5.3.1, the plot of $1/C'^2$ versus voltage V should be linear in nature. Such a plot is shown in Figure 5.5 along with the linear curvefit applied to the plot. The curvefit has a slope of $1.6241*10^{-7}$ and the value of Y-intercept is $1.5751*10^{-7}$. Using these values in Equations 5.18 and 5.19, we obtain the extracted values of N_d and V_i as and $1.5*10^{15}$ cm^{-3} and 1.144eV respectively. These values compare well with the values of Vi and Nd obtained through the “Analysis” option of the Sula DLTS software.

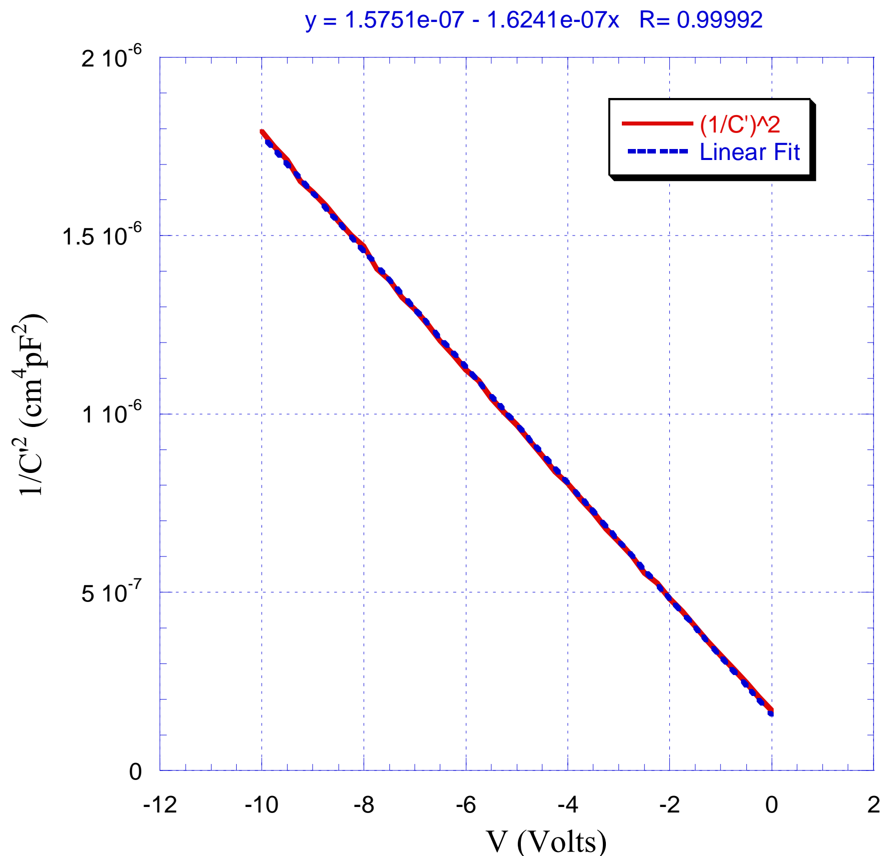

Figure 5.5 Plot of $1/C'^2$ versus voltage V with linear curvefit to the plot.

The correlation coefficients for the curvefit lines to $1/C'^2$ vs. voltage curves were in the range of 0.992 – 0.999, which indicates almost perfect linearity of the plots. The extracted values of Nd were in the same order of magnitude as the specified doping density of the epilayer. The Schottky barrier heights extracted from the C-V measurements were typically higher than those obtained from the I-V measurements. This has been attributed to the presence of interfacial oxide layer. This oxide layer decreases the total capacitance and thus increases the built-in voltage, resulting in a higher value of the barrier height.

5.4 X-ray Photoelectron Spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) or Electron Spectroscopy for Chemical Analysis (ESCA) is the most widely used of the contemporary surface characterization methods. XPS is very popular due to its information-rich content and the flexibility in its application to a wide variety of samples. In XPS, the sample is bombarded with photon radiation under high vacuum and the emitted photoelectrons from the sample surface are separated according to their energies and subsequently counted. The photon source is in the X-ray energy range, hence the name X-ray Photoelectron Spectroscopy.

The theory behind the operation of the XPS is largely based on the photoelectric effect. When a photon collides with an atom, one of the possible outcomes is that the photon may interact with an atomic orbital electron with total energy transfer. If the incident photon is of sufficiently high frequency υ, electrons are emitted from the atom with a specific kinetic energy (KE). The basic physics of this process is described by the Einstein equation,

$$E_B = h\upsilon - KE \qquad 5.22$$

where E_B is the binding energy of the electron to its atom and KE is the kinetic energy of the emitted electron. Thus, the binding energy can be easily calculated from $h\upsilon$ (known) and the kinetic energy (measured).

Binding energy is the energy with which an orbital electron is bound to the nucleus of the atom. The closer the electron is to the nucleus, the more tightly the electron is bound to the nucleus. Binding energy varies with the type of atom as well as the number of other atoms bound to that atom. Since different isotopes of an element have the same nuclear charge, the isotopes do not affect the binding energy. Any variations of the binding energy are associated with the covalent or ionic bonds between atoms. Therefore, the calculated binding energy gives a lot of information about the electronic structure of the sample. Any change in the atomic bonding causes a change in the binding energy. Such a change is referred to as binding energy shift or chemical shift. Binding energy shifts are suggestive of the chemical reactions at the surface of the sample and can be effectively used to determine the nature of the reaction.

The XPS results are typically presented on a graph on which the electron counts measured are plotted as a function of binding energy Thus, the XPS spectrum of a material consists of peaks which are associated with various elements. XPS analyses are typically performed by first taking a wide-spectrum scan covering more than 1000eV, then performing a high-resolution scan over smaller ranges of around 20eV at the peaks in the wide-spectrum scan. The area under these peaks is related to the amount of each element present. In Figure 5.6, we show a sample wide-spectrum XPS scan of Al/4H-SiC. The scan consists of a number of peaks, each of which corresponds to a specific element orbital.

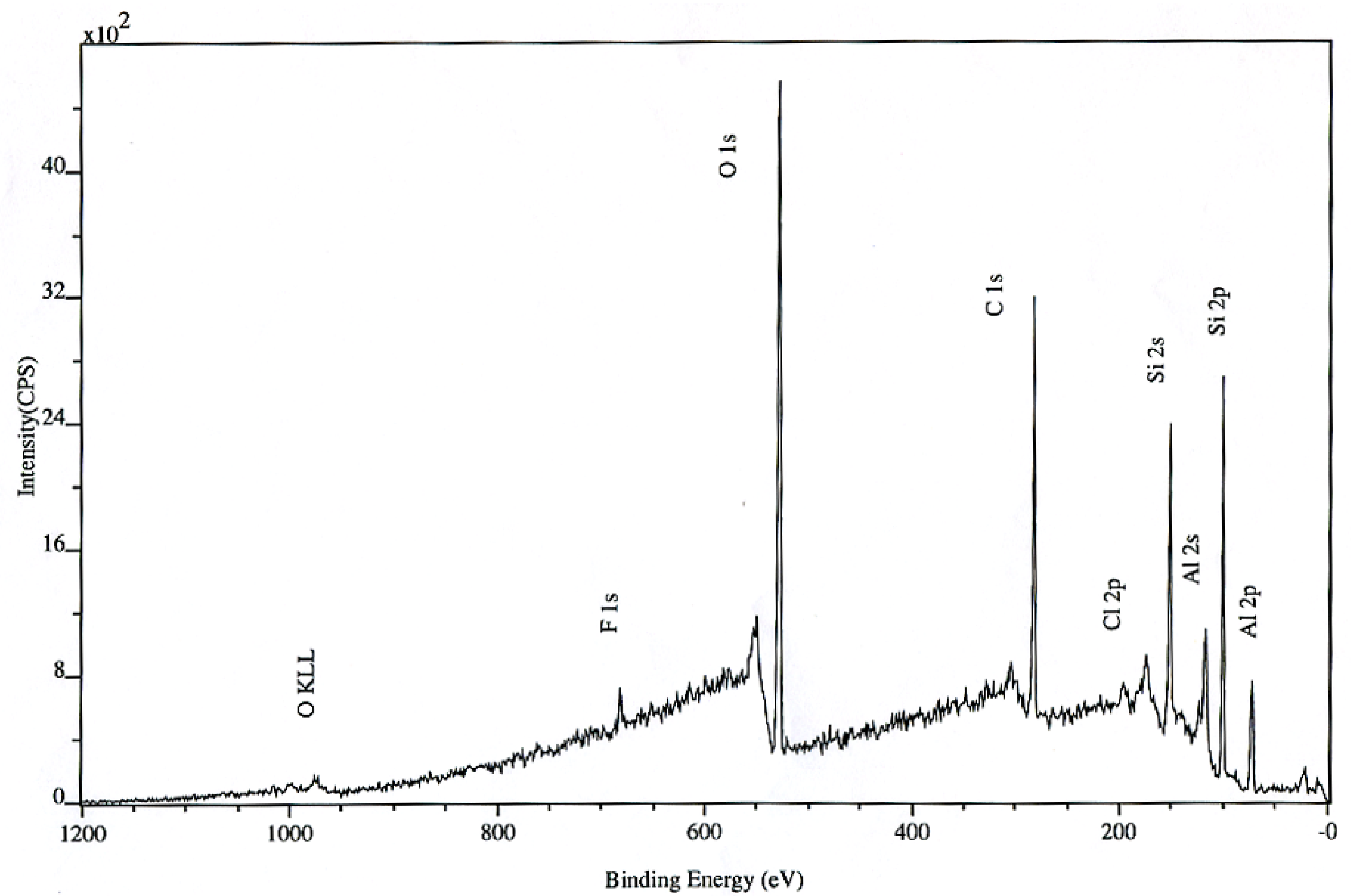

Figure 5.6 XPS Wide-Spectrum Survey Scan of Al/4H-SiC.

The high-resolution scan is conducted at a smaller range of binding energies (typically around 20eV) around the binding energy of the peak of interest. The binding energy is a calculated value determined from the kinetic energy of the emitted electrons, the energy of the X-ray photons, the work function of the surface and a correction term for the electrical charge on the sample surface [32]. In Figure 5.7, we show a sample high-resolution scan of the Al2p peak of the survey scan in Figure 5.6. The Al2p peak shape is composed of a number of full-width half-maximum (FWHM) peaks. Each sub-peak is attributed to an atomic bond having the binding energy at which the sub-peak has maximum intensity. The area under each peak corresponds to the relative amount of the respective composite present. For example, in Figure 5.7 the blue peak corresponds to the composite present in the maximum concentration. The maximum of the blue peak is at a binding energy of 72.8eV, which corresponds to an Al-O bond [33].

Thus, from XPS the following relevant information can be obtained:

1) Identification of all elements except H and He and their atomic concentrations greater than 0.1%.
2) Approximate elemental surface composition
3) Information such as oxidation state and bonding atoms.
4) Identification of materials using identification of bonding orbitals.

The above-listed information would be very useful in determining the chemical composition at the Al/SiC interface after annealing, thus providing insight into the Al-SiC chemistry during the annealing process

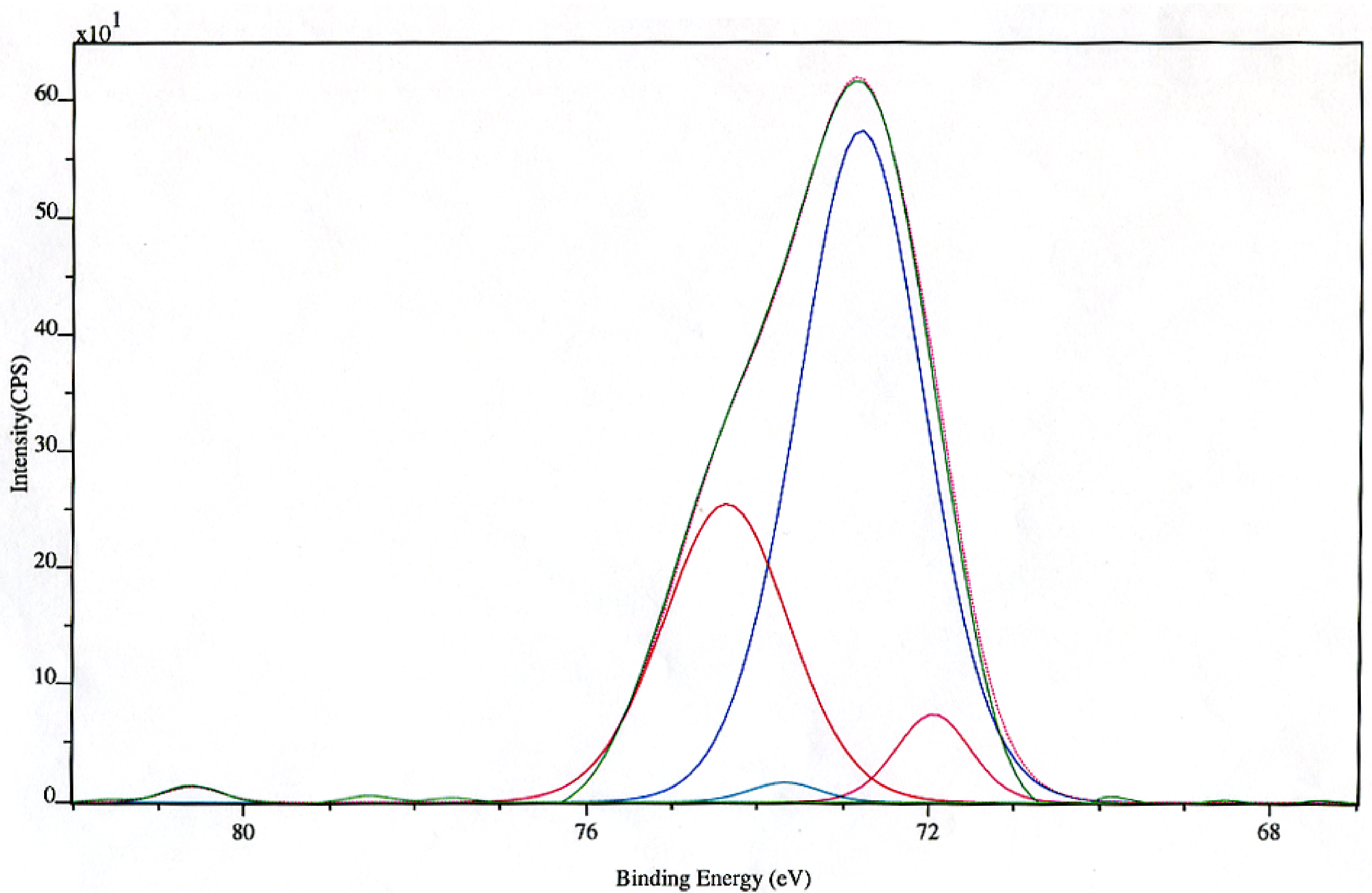

Figure 5.7 High-Resolution XPS Scan of the Al2p peak of Al/4H-SiC.

5.5 Conclusions

All the different measurement techniques discussed in this chapter were employed at some stage during the course of this research project. I-V and C-V measurements were by far the most frequently employed techniques, since they are the necessary techniques to determine the essential results of this thesis. During the initial phases of this project, I-V measurements were employed to test the Nickel contacts for ohmic behavior immediately after they are annealed. I-V measurements were frequently used post-fabrication to obtain the forward and reverse I-V characteristics on each of the fabricated devices. From the I-V characteristics, important parameters such as the Schottky Barrier height, the ideality factor, and the diode series resistance were extracted. C-V measurements were also used post-fabrication to determine the Schottky Barrier Height and the doping concentration. The DEKTAK profilometer was intermittently used to determine the dimensions of the deposited metal contacts. Finally, X-ray Photoelectron Spectroscopy was used as the preferred technique of surface characterization to study the effects of annealing on Aluminum/4H-SiC contacts. The results of all the above measurement techniques are presented and discussed in the next chapter.

CHAPTER 6

RESULTS AND DISCUSSION

Schottky diodes were fabricated on 4H-SiC using the fabrication process presented in Chapter 4. The various measurement techniques explained in Chapter 5 were performed on the fabricated Schottky diodes for electrical characterization of the diodes and surface characterization of the interface. In this chapter, the results obtained from the measurement techniques are provided and the inferences derived from the results are stated. During the course of this project, three different metals were used for interfacing with 4H-SiC to create Schottky diodes; namely Aluminum (Al), Copper (Cu), and Gold (Au). The Schottky diodes were fabricated on substrates from two different wafers.

For the sake of comparison with the experimental data, Table 6.1 lists the different wafers used with their varying doping levels. Also calculated are the semiconductor work function ϕ_S and the energy difference between E_C and E_F denoted by ϕ_n, which will be useful in the determination of the built-in voltage V_i and the Schottky barrier height ϕ_B. Table 6.2 lists the three Schottky metals used in this project, along with the calculated Schottky-Mott limits. Also calculated is the built-in voltage V_i for each of the substrate wafers, which is useful for comparison with the C-V measurement results.

Table 6.1 List of 4H-SiC Wafers used with their Doping Concentrations

Wafer	Doping Conc. N_D (bulk)	Doping Conc. N_D (epi)	Epilayer Thickness (μm)	ϕ_n (eV)	ϕ_S (eV)
AC0113-04	9.6×10^{18}	2.1×10^{15}	10	0.232	3.832
B1145-08	4.5×10^{18}	5.0×10^{15}	5	0.210	3.810

Table 6.2 Schottky-Mott Limits for Al, Cu and Au for SiC polytypes used

Metal	ϕ_M (eV)	ϕ_B (eV) (Schottky-Mott Limit)	V_i (eV)	
			AC0113-04	B1145-08
Aluminum (Al)	4.28	0.68	0.448	0.47
Copper (Cu)	4.7	1.1	0.868	0.89
Gold (Au)	5.01	1.5	1.268	1.29

For the calculation of ϕ_s and ϕ_n in Table 6.1, Equations 3.1 and 3.2 are used respectively. For calculating V_i and ϕ_B in Table 6.2, Equations 3.3 and 3.4 are used respectively. The value of the Schottky-Mott Limit can also be confirmed by using Equation 5.20 to get ϕ_B by adding V_i and ϕ_n.

6.1 Characterization of Al/4H-SiC Schottky Diodes

6.1.1 Electrical Characterization by I-V and C-V Measurements

The Al/4H-SiC sample on which the I-V and C-V measurements were performed was denoted AC0113-06J23. As the name suggests, the Schottky diodes were fabricated using a SiC die from the AC0113-04 wafer. Initially, I-V and C-V measurements were performed on the 14 as-deposited Aluminum Schottky contacts. The extracted values of ideality factor η, Schottky barrier height ϕ_B and the diode series resistance R are listed in Table 6.3.

The sample was then annealed at 600ºC for 5 minutes under a neutral ambient provided by the forming gas flow. I-V and C-V measurements were performed again on the annealed sample. The extracted data from the I-V and the C-V measurements is listed in Table 6.4. It was found that the Schottky parameters of the sample changed substantially after annealing. To observe the effects of annealing, a comparison of the ideality factor and the Schottky barrier height before and after annealing is provided in Table 6.5. In Figure 6.1, the I-V characteristics for the as-deposited Al/4H-SiC diodes are presented along with an annealed sample. It is seen that the slope of the as-deposited characteristics is smaller than the annealed characteristics, indicating a higher ideality factor. Both the as-deposited and annealed characteristics start rolling off in the same current range. This indicates that the series resistance of the diode does not change substantially due to annealing for Al/4H-SiC diodes.

Table 6.3 List of Parameters for As-deposited Al/4H-SiC Sample AC0113-06J23

Dot #	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
Dot01	1.692	0.618	11.15	0.23	0.46	8.25×10^{15}
Dot02	1.667	0.632	9.59	0.32	0.55	9.47×10^{15}
Dot03	1.712	0.636	9.76	0.36	0.59	9.88×10^{15}
Dot04	1.717	0.612	9.21	0.20	0.43	8.76×10^{15}
Dot05	1.651	0.619	9.08	0.25	0.48	9.32×10^{15}
Dot06	1.662	0.631	9.25	0.33	0.56	9.26×10^{15}
Dot07	1.710	0.641	9.19	0.38	0.61	1.05×10^{16}
Dot08	1.657	0.615	9.85	0.23	0.46	8.74×10^{15}
Dot09	1.644	0.618	9.84	0.20	0.43	8.89×10^{15}
Dot10	1.660	0.622	9.66	0.25	0.48	9.34×10^{15}
Dot11	1.664	0.620	9.82	0.23	0.46	7.25×10^{15}
Dot12	1.684	0.618	9.03	0.25	0.48	7.70×10^{15}
Dot13	1.627	0.635	9.62	0.30	0.53	7.31×10^{15}
Dot14	2.056	0.606	10.06	0.23	0.46	8.25×10^{15}
Average	1.700	0.623	9.651	0.27	0.50	8.82×10^{15}

Table 6.4 List of Parameters for Annealed Al/4H-SiC Sample AC0113-06J23

Dot #	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
Dot01	1.572	0.637	6.61	0.39	0.62	8.49E+15
Dot02	1.528	0.653	6.65	0.45	0.68	9.54E+15
Dot03	1.543	0.656	5.61	0.31	0.54	9.23E+15
Dot04	1.538	0.651	8.39	0.36	0.59	9.01E+15
Dot05	1.491	0.652	9.07	0.43	0.66	9.66E+15
Dot06	1.498	0.655	6.57	0.46	0.69	9.35E+15
Dot07	1.517	0.660	5.75	0.47	0.70	1.05E+16
Dot08	1.511	0.650	11.23	0.42	0.65	9.12E+15
Dot09	1.495	0.655	12.86	0.37	0.60	9.16E+15
Dot10	1.514	0.653	9.87	0.43	0.66	9.62E+15
Dot11	1.526	0.596	12.95	0.42	0.65	7.58E+15
Dot12	1.461	0.665	12.78	0.45	0.68	8.04E+15
Dot13	1.519	0.663	14.06	0.45	0.68	7.49E+15
Dot14	1.572	0.637	6.61	0.39	0.62	8.49E+15
Average	1.516	0.650	9.415	0.42	0.65	8.98×10^{15}

Table 6.5 Comparison of Average Parameters for As-deposited and Annealed Al/4H-SiC Sample AC0113-06J23

Annealing Condition	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
As-deposited	1.700	0.623	9.651	0.27	0.50	8.82×10^{15}
600ºC for 5 minutes	1.516	0.650	9.415	0.42	0.65	8.98×10^{15}

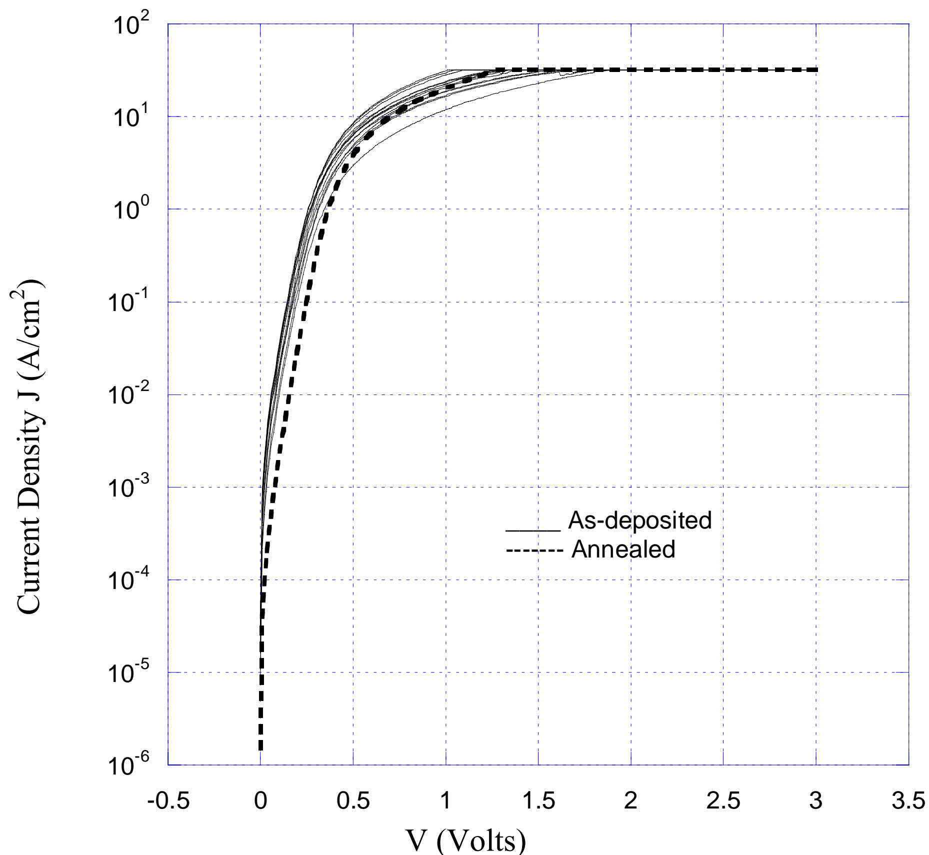

Figure 6.1 Forward I-V Characteristics of Al/4H-SiC Schottky diodes.

The results tabulated in Table 6.3 indicate a poor Aluminum-SiC interface in the sample under test. The C-V characteristics of the as-deposited Al/4H-SiC diodes along with an annealed sample are presented in Figure 6.2.

The most prominent observation that can be seen from the comparison of the parameters in Table 6.5 is the decrease in the ideality factor from 1.7 to 1.516. The average barrier height of the Schottky diodes after annealing is 0.65eV from both the I-V and the C-V measurements, which is very close to the Schottky-Mott Limit value of

0.68eV as stated in Table 6.2. Thus, annealing the Al/4H-SiC sample at 600ºC for 5 minutes results in improving the ideality factor and increasing the Schottky Barrier Height. The obtained values for the ideality factor are the lowest figures obtained by us including the previous work done on this topic [34], [35].The improvement of the ideality factor suggests a more intimate surface contact, while the increased barrier height suggests a change in the surface chemistry.

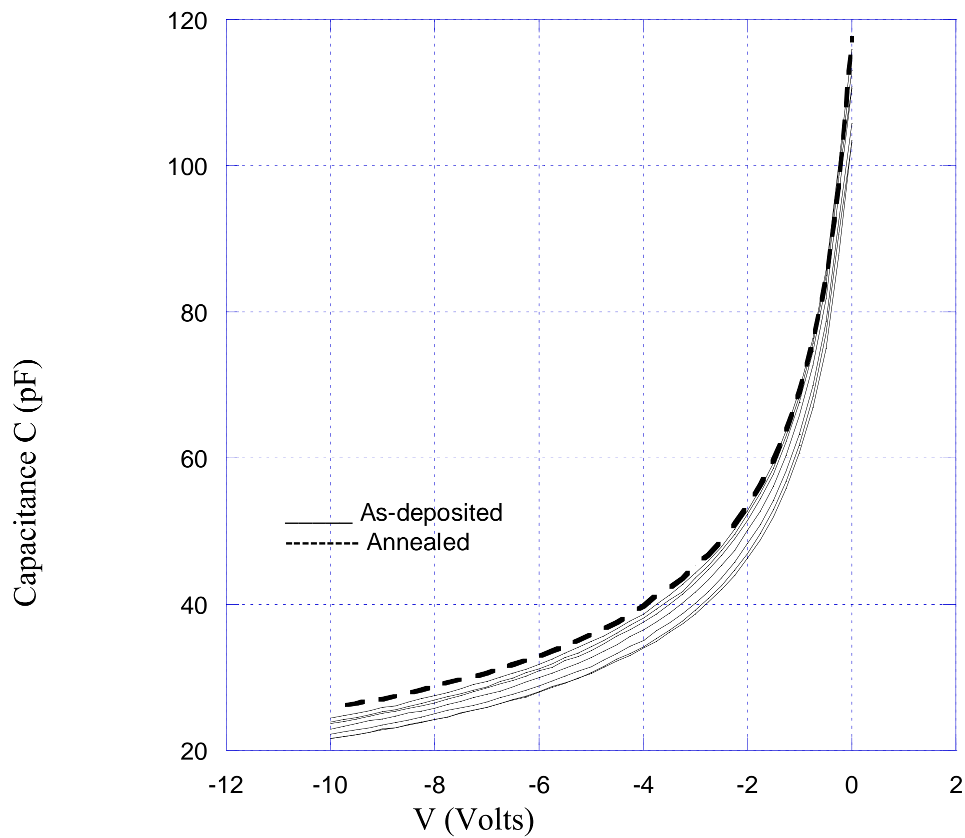

Figure 6.2 C-V Characteristics of Al/4H-SiC Schottky diodes.

6.1.2 Surface Characterization by X-ray Photoelectron Spectroscopy (XPS)

The results stated in Table 6.5 warrant a deeper investigation into the physical and chemical aspects of the effects of annealing on the metal-semiconductor interface. The comparison of the Schottky parameters before and after annealing at 600ºC strongly suggests some change in the interface chemistry at the Aluminum-SiC junction. To further investigate this, XPS was performed on Al/4H-SiC samples specifically fabricated to suit the XPS measurement requirements. The Schottky diodes conventionally fabricated according to the fabrication process described in Chapter 4 were unsuitable for XPS analysis on account of the fact that XPS is mainly a surface analysis tool, thereby lacking deep penetration of the X-ray photons into the sample. Depending on the incident angle, the depth to which the incident photons penetrate can be controlled between the top few atomic layers. When the incident angle is normal to the sample surface, the penetration depth is maximum, which is typically 8-10nm. The samples conventionally prepared according to the fabrication process typically have the Schottky contacts at least 300nm thick. Therefore, special samples were prepared for the XPS analysis.

For obtaining the desired information from the XPS measurements, it was essential that the Schottky contact on the surface be as thin as possible to allow maximum exposure of the interface to the photon radiation. With this aim, two samples were prepared for XPS analysis. Nickel deposition and annealing was skipped for both samples since focus was on the Schottky contacts on the front-side. Also, instead of the usual 14 dots, only 2 big dots of Aluminum were deposited to achieve maximum surface area.

During the deposition of the Schottky contacts, a minimum amount of Aluminum metal was used for the evaporation and the samples were placed as far as possible from the heating coil to achieve very thin Aluminum contacts on the front-side. One of the samples was completely covered during evaporation to make certain that no Aluminum was deposited on it. This became the reference sample for XPS analysis.

After the deposition of the Schottky contacts, the thicknesses of the deposited dots were measured using the DEKTAK Profilometer. It was seen that despite the efforts taken, approximately 1500Å of Aluminum was deposited on the front surface. It was decided to anneal the dots for a prolonged period of time with expectations that much of the deposited metal would diffuse into the semiconductor. Therefore, the XPS sample was annealed for 45 minutes at 600ºC under an inert atmosphere of forming gas. Upon profilometry of the dot right after annealing, it was observed that still approximately 1000Å of Aluminum was still remaining on the surface of SiC. It was decided to proceed with the XPS analysis despite the thick layer of Aluminum. The sample that had the 1000Å Aluminum dots on it was labeled XPS Sample I and the blank SiC sample was labeled XPS Sample II. Four separate XPS measurements were made on these two samples. Figure 6.3 shows positions A, B, C and D on the two XPS samples. The chief measurements of interest were A, B and C, with measurement D as reference.

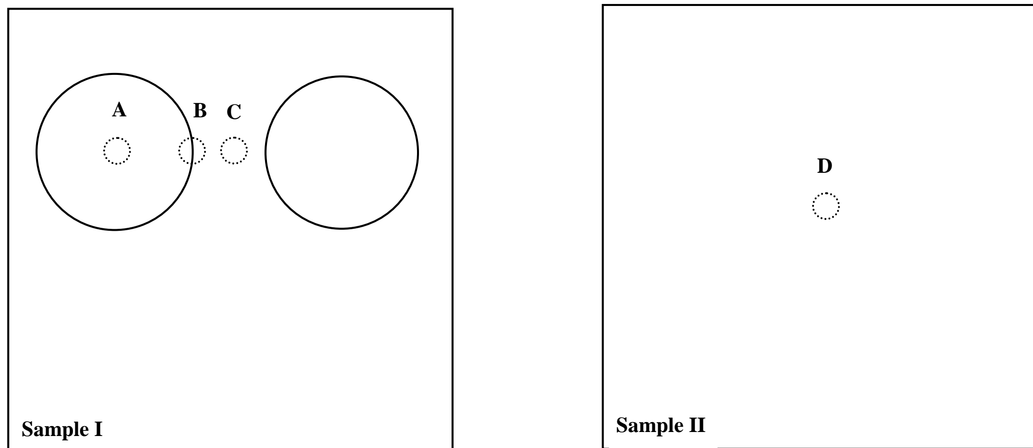

Figure 6.3 XPS samples and Measurement Positions for XPS

Each XPS measurement is composed of a wide-survey scan and the high-resolution scans of the individual peaks on the wide-survey scan. Figure 6.4 shows the wide-spectrum scan of the XPS Measurement A. The primary area of interest in this figure is the presence of C peak, with the notable absence of a Si peak. The high-resolution scan of C1s peak is shown in Figure 6.5. The FWHM peak has its maximum value at binding energy of 283.4eV, which corresponds to elemental Carbon. Thus, it is seen that the major peak of the de-convolved graph is elemental Carbon. Since the only source of Carbon is the SiC substrate, then it is logical to surmise that the Carbon must have migrated from the interface through the Aluminum layer to the surface. Out-diffusion of elemental Carbon implies dissociation of the Si-C bonds present in SiC. If Carbon is still in its elemental form, then this suggests that the free Silicon from the dissociated bonds must be bonding with Aluminum, which is the only other element present at the interface.

Figure 6.6 shows the wide-spectrum survey scan of Measurement B taken on the edge of the Aluminum dot. In this figure, we see the first signs of Si peaks. This is to be expected since part of the measured area contains bare SiC. Figure 6.7 shows the de-convolved high-resolution scan of the Si2p peak first seen in Figure 6.4. The Si2p peak is made up of 3 FWHM peaks, the largest one of which has a maximum value at 100.8eV, which corresponds to SiC. There are also two smaller peaks, whose maxima lie at 101.1eV and 101.5eV. A maxima located at a binding energy of 101.5eV indicates presence of Zeolite or Aluminosilicate ($AlSiO_4$) [33]. This is evidence of Aluminum-Silicon bonding at the Al/4H-SiC interface. Similar interactions between Al and SiC have been observed by Bermudez et. al. [36]. The bonding between Aluminum and Silicon strongly suggests the formation of an Al-Si compound at the interface due to annealing at 600ºC. The change in the barrier height and the ideality factor of the Al/4H-SiC devices as shown in Table 6.5 is attributed to the formation of such an Al-Si compound as a result of annealing.

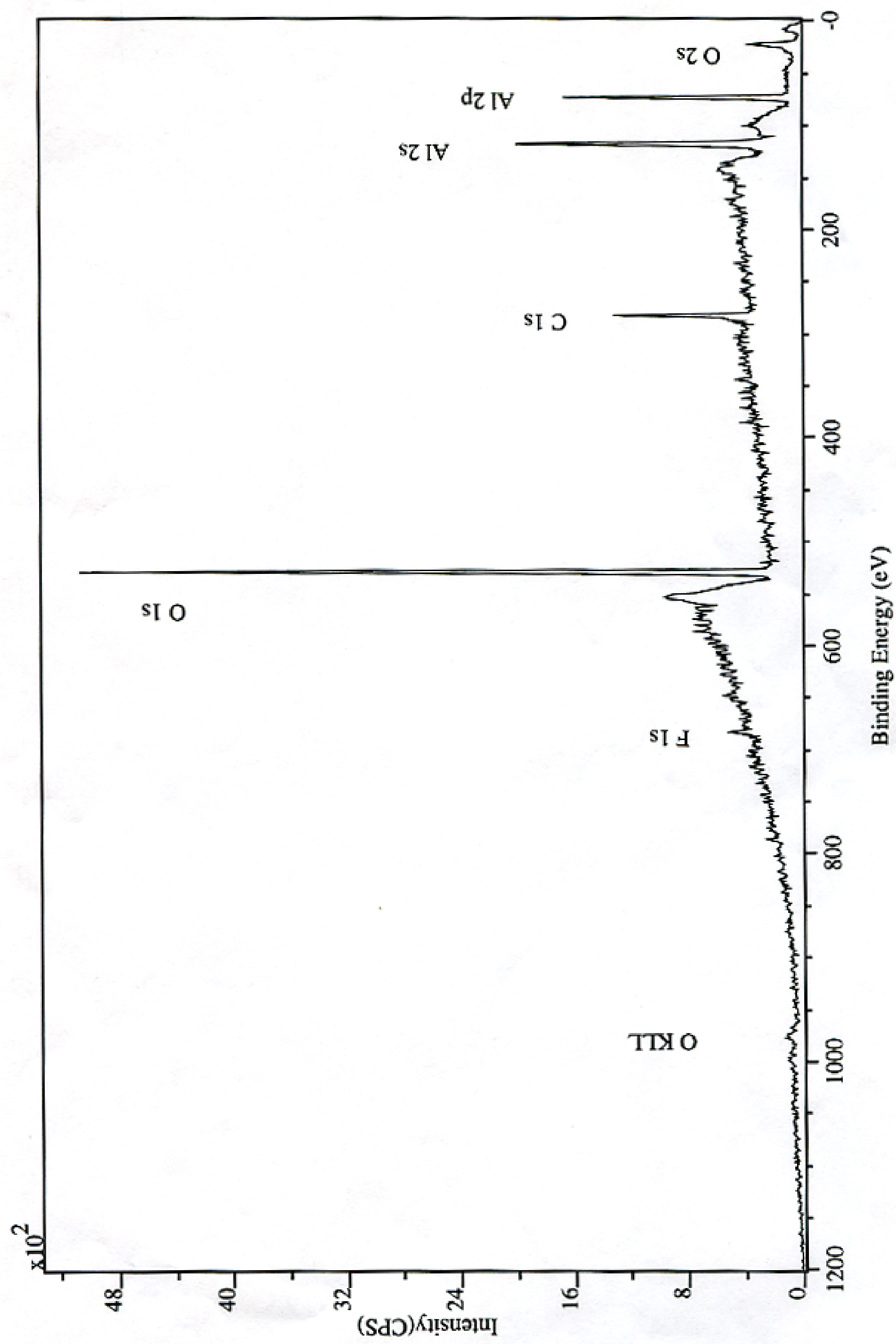

Figure 6.4 Wide-Spectrum XPS Survey Scan of Measurement A on the Aluminum Dot on Al/4H-SiC.

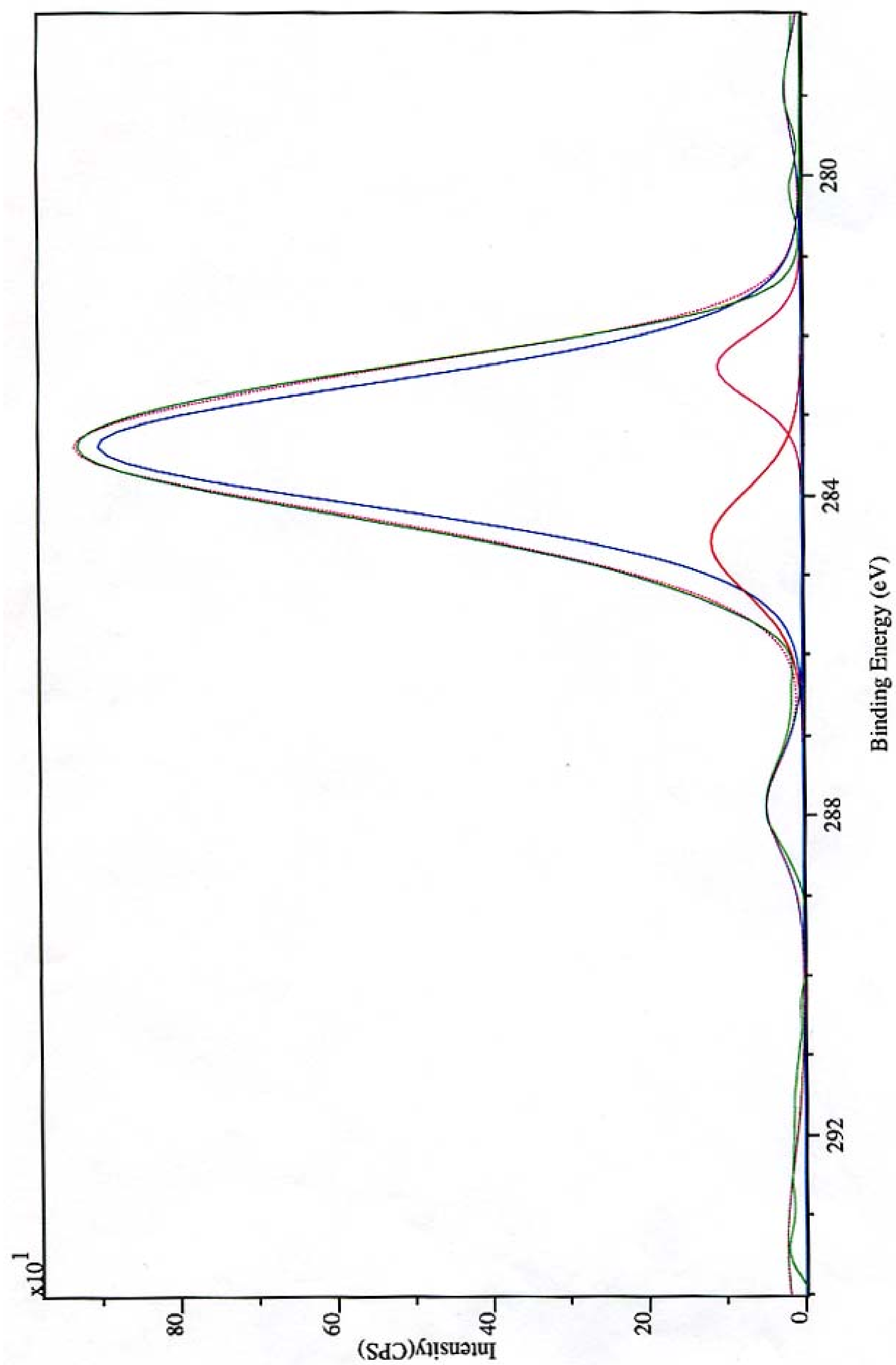

Figure 6.5 High-Resolution XPS Scan of the C1s peak of Measurement A on Al/4H-SiC.

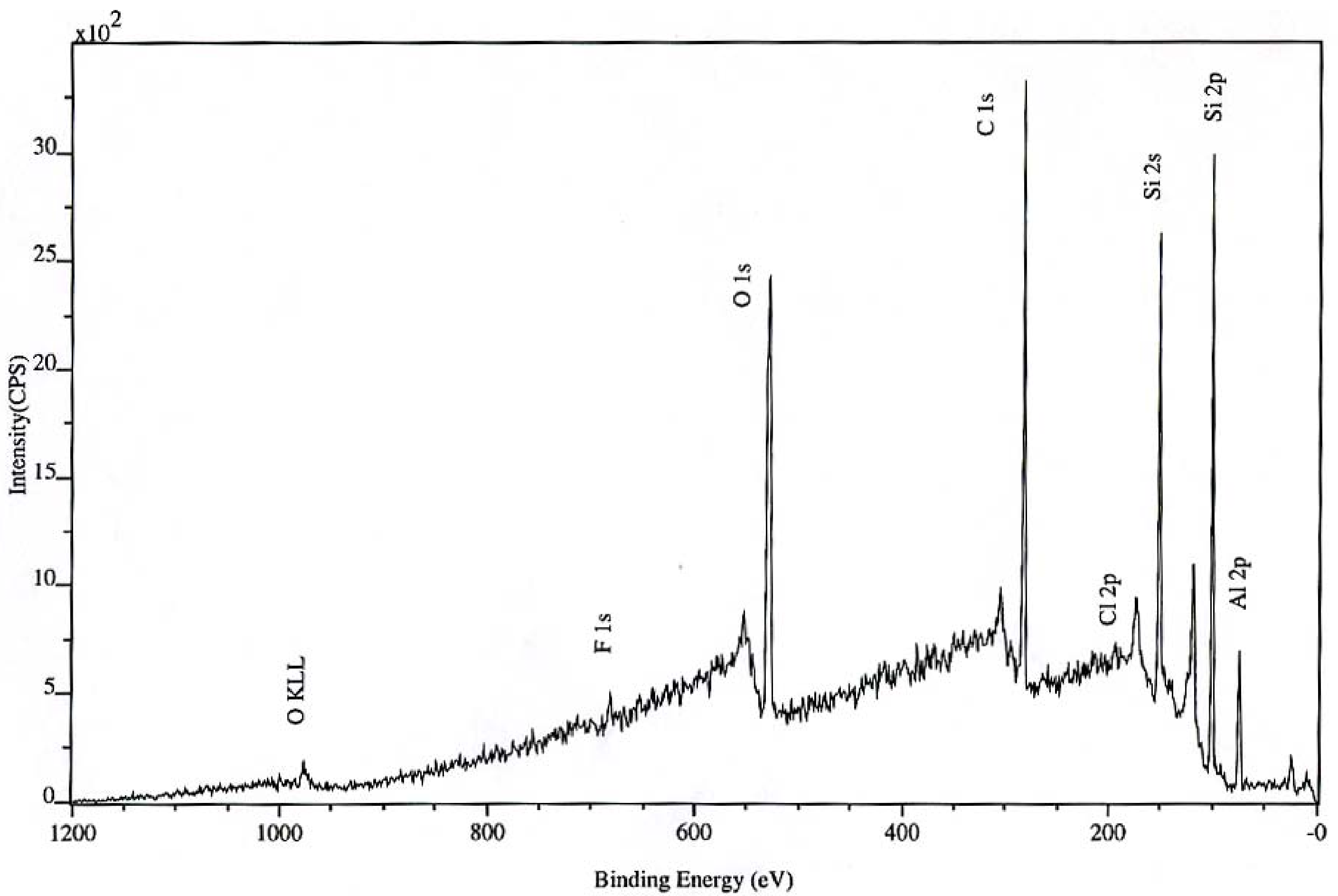

Figure 6.6 Wide-Spectrum XPS Survey Scan of Measurement B on the edge of Aluminum Dot on Al/4H-SiC.

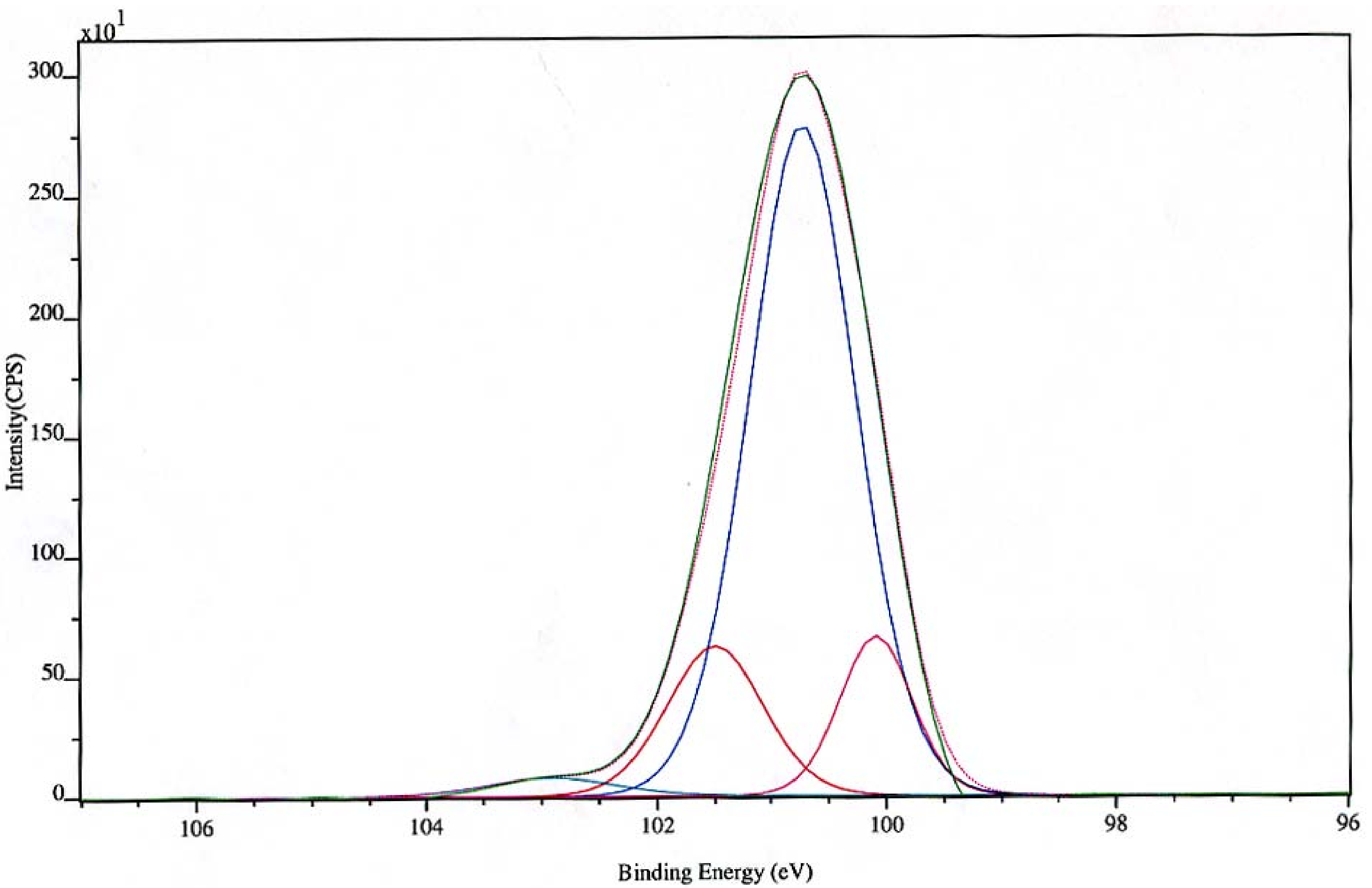

Figure 6.7 High-Resolution XPS Scan of the Al2p peak of Measurement B on Al/4H-SiC.

Further XPS measurements C and D did not reveal any other evidence of Al-Si bonding or Al-C bonding. The fact that there was only one measurement which shows evidence of an Aluminum-Silicon compound is not surprising considering the emission depth limitations of the XPS and the nature of the sample. The deposited dots are rarely in the form of strict cylindrical shapes and the edges of the dots have a definite slope to them. As such, a measurement made at the edge of the Schottky dot is most likely to detect the interfacial chemistry rather than a measurement made directly on the surface of the Schottky dot.

6.2 Characterization of Cu/4H-SiC Schottky Diodes

6.2.1 Electrical Characterization by I-V and C-V Measurements

The Cu/4H-SiC sample on which I-V and C-V measurements were performed was denoted B1145-06I12. The Schottky diodes were fabricated on a SiC die from the B1145-08 wafer. Initially, I-V measurements and C-V measurements were performed on the 14 as-deposited Copper contacts. Table 6.6 lists the extracted values of ideality factor η, Schottky barrier height ϕ_B and the diode series resistance R, which are extracted from the I-V measurements; and, the built-in voltage V_i, the calculated Schottky barrier height ϕ_B and the doping concentration N_d, are extracted from the C-V measurements.

The sample was then annealed at 500ºC for 5 minutes under a neutral ambient provided by the forming gas flow. I-V and C-V measurements were performed again on the annealed sample. Table 6.7 lists the detailed extracted data from the I-V and the C-V measurements. It was observed that the Schottky parameters were significantly altered after the annealing step. A comparison of the as-deposited and annealed Schottky parameters of the device is shown in Table 6.8. The forward I-V characteristics of the Cu/4H-SiC diode are shown in Figure 6.8. The I-V curves presented are for the 14 as-deposited diodes along with an annealed sample for comparison. It is observed that the I-V curve for annealed sample has a greater slope and is linear over a larger current range compared to the as-deposited samples. This indicates that the annealed samples have an improved (smaller) ideality factor over the as-deposited samples. This conclusion is verified in Table 6.8, where the ideality factor for annealed samples is 1.138 in contrast to

the ideality factor of 1.446 for the as-deposited sample. The average extracted values for the diode series resistance for as-deposited and annealed Cu/4H-SiC diodes are 9.158Ω and 15.526Ω respectively.

Table 6.6 List of Parameters for As-deposited Cu/4H-SiC Sample B1145-06I12

Dot #	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
Dot01	1.247	1.148	7.700	1.57	1.78	1.20E+15
Dot02	1.432	1.042	17.180	1.55	1.76	1.06E+15
Dot03	1.728	1.020	8.120	1.69	1.90	1.00E+15
Dot04	1.204	1.174	7.800	1.54	1.75	1.05E+15
Dot05	1.386	1.093	8.200	1.54	1.75	1.09E+15
Dot06	1.407	1.078	7.980	1.58	1.79	9.50E+14
Dot07	1.302	1.089	11.210	1.64	1.85	1.05E+15
Dot08	1.397	1.062	7.880	1.59	1.80	1.05E+15
Dot09	1.219	1.153	8.880	1.55	1.76	9.88E+14
Dot10	1.763	1.061	7.710	1.88	2.09	1.00E+15
Dot11	1.324	1.091	8.080	1.61	1.82	9.83E+14
Dot12	1.395	1.094	8.660	1.68	1.89	9.53E+14
Dot13	2.105	1.012	10.890	1.82	2.03	8.73E+14
Dot14	1.339	1.057	7.920	1.70	1.91	9.07E+14
Average	1.446	1.084	9.158	1.64	1.85	1.01E+15

Table 6.7 List of Parameters for Annealed Cu/4H-SiC Sample B1145-06I12

Dot #	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
Dot01	1.124	1.259	16.130	1.78	1.99	1.07E+15
Dot02	1.116	1.277	11.830	2.02	2.23	8.28E+14
Dot03	1.157	1.314	11.980	2.46	2.67	7.99E+14
Dot04	1.094	1.263	13.780	1.74	1.95	9.91E+14
Dot05	1.105	1.267	21.060	1.75	1.96	1.02E+15
Dot06	1.108	1.285	23.700	1.97	2.18	7.89E+14
Dot07	1.106	1.297	12.270	1.97	2.18	9.61E+14
Dot08	1.100	1.274	12.750	2.00	2.21	1.04E+15
Dot09	1.100	1.270	12.770	1.83	2.04	8.70E+14
Dot10	1.284	1.252	17.980	2.20	2.41	7.16E+14
Dot11	1.208	1.197	14.260	1.90	2.11	9.12E+14
Dot12	1.113	1.272	17.900	1.93	2.14	7.89E+14
Dot13	1.167	1.299	15.430	2.29	2.50	6.26E+14
Dot14	1.145	1.300		2.34	2.55	7.68E+14
Average	1.138	1.273	15.526	2.01	2.22	8.70E+14

Table 6.8 Comparison of Average Parameters for As-deposited and Annealed Cu/4H-SiC Sample B1145-06I12

Annealing Condition	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
As-deposited	1.446	1.084	9.158	1.64	1.85	1.01E+15
600ºC for 5 minutes	1.138	1.273	15.526	2.01	2.22	8.70E+14

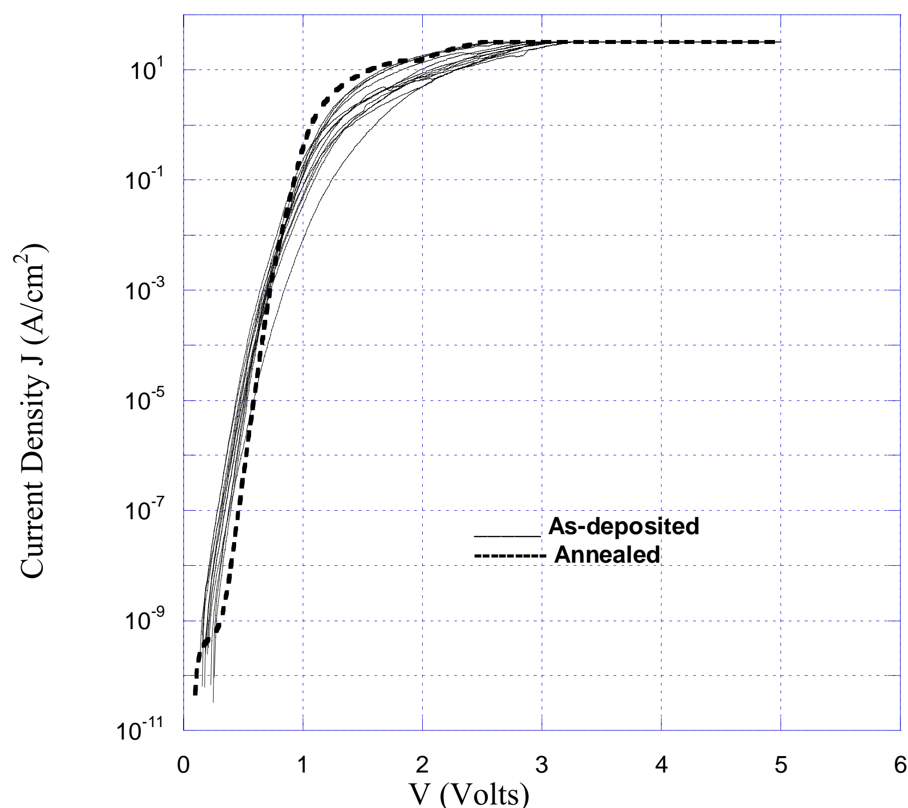

Figure 6.8 Forward I-V Characteristics of Cu/4H-SiC Schottky Diodes.

The results shown in Table 6.6 show that the Schottky Barrier height is very close to the Schottky-Mott Limit value of 1.1eV calculated in Table 6.2. However, the obtained value of the ideality factor is far from an ideal figure. The same parameter extracted from the I-V characteristics after annealing gives a much improved value. As seen in Table 6.8, the Schottky Barrier Height value increases by almost 0.2eV and the ideality factor is improved (decreased) by more than 0.3. The obtained value of 1.138 as the ideality factor is a probably the best value that can be obtained from the Schottky diodes fabricated using the available resources.

In Figure 6.9, we present the C-V characteristics for the as-deposited Cu/4H-SiC diodes along with an annealed sample. It is observed that the annealed sample has significantly lower capacitance values compared to those of as-deposited diodes. We can conclude that the Schottky barrier height is increased for the annealed samples, since the lower capacitance values suggest a higher-built-in voltage and consequently, a higher barrier height. The average values of the Schottky barrier height extracted from the C-V characteristics are 1.85eV and 2.22eV for as-deposited and annealed Cu/4H-SiC diodes respectively. From Table 6.8, it is observed that the average values obtained from I-V and C-V measurements differ considerably. This is not uncommon, since the values obtained from C-V measurements are typically higher than those obtained from I-V measurements [2]. This is because C-V measurements are strongly affected by presence of interfacial layer between the metal-semiconductor interface. However, in this case, the SBH obtained from C-V measurements is lower than that obtained from I-V measurements.

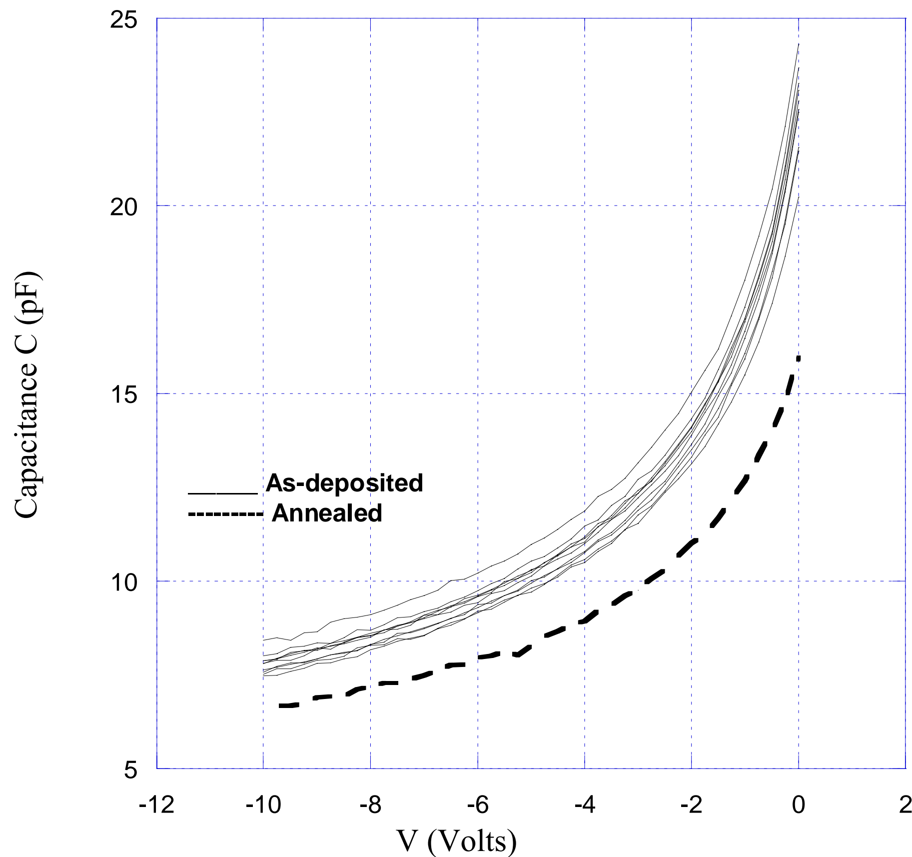

Figure 6.9 C-V Characteristics of Cu/4H-SiC Schottky Diode

Comparing the as-deposited and annealed values of the Schottky Barrier Height ϕ_B and the ideality factor η, it can be safely concluded that annealing the Cu/4H-SiC Schottky diodes at 500ºC for 5 minutes leads to an increase in the barrier height and an improvement (decrease) in the ideality factor. This trend is identical to the change seen in the Al/4H-SiC Schottky diodes and is more prominent in the case of Cu/4H-SiC Schottky diodes. Traditionally the Cu/4H-SiC have been known to exhibit dual Schottky behavior, in which the diode shows two linear regions of conduction parallel to each other [12].

This dual-behavior phenomenon is usually modeled as two diodes in parallel with two separate barrier heights associated with the diodes [29]. This behavior was not seen at all in the Cu/4H-SiC diodes fabricated in this project. The low ideality factor values obtained are also superior to the previously obtained values [12], thereby exhibiting the advantages of the revised fabrication procedure over the pre-existing procedure.

6.3 Characterization of Au/4H-SiC Schottky Diodes

6.3.1 Electrical Characterization by I-V and C-V Measurements

The Au/4H-SiC sample on which the I-V and C-V measurements were performed was denoted AC0113-06K13. As the name suggests, the Schottky diodes were fabricated using a SiC die from the AC0113-04 wafer. I-V and C-V measurements were performed on the 14 as-deposited Gold Schottky contacts. In Table 6.9, the extracted values of ideality factor η, Schottky barrier height ϕ_B and the diode series resistance R are presented.

Table 6.9 List of Parameters for as-deposited Au/4H-SiC Sample AC0113-06K13

Dot #	I-V			C-V		
	η	ϕ_B (eV)	R (Ω)	V_i (eV)	ϕ_B (eV)	N_D (cm^{-3})
Dot02	1.115	1.299	10.020	1.09	1.32	9.39E+15
Dot03	1.138	1.273	12.540	1.06	1.29	9.56E+15
Dot04	1.087	1.314	18.060	1.06	1.29	8.71E+15
Dot05	1.135	1.285	22.690	1.11	1.34	9.52E+15
Dot06	1.113	1.302	14.230	1.08	1.31	8.70E+15
Dot07	1.100	1.288	11.060	1.01	1.24	1.02E+16
Dot08	1.119	1.268	9.610	1.00	1.23	9.13E+15
Dot09	1.111	1.275	14.400	1.03	1.26	8.91E+15
Dot12	1.108	1.252	11.070	0.97	1.20	8.46E+15
Dot13	1.115	1.266	8.930	0.99	1.22	8.33E+15
Dot14	1.116	1.308	19.650	1.13	1.36	8.97E+15
Average	1.114	1.285	13.842	1.05	1.28	9.08E+15

In Figure 6.10, the I-V characteristics of the Au/4H-SiC Schottky Diode are presented. The tight distribution of the curves indicates a well-controlled process. The linear region of the semilog I-V characteristics extends over 9 orders of magnitudeThe average extracted value of the ideality factor is 1.114, which represents an excellent set of diodes. The deviation of the ideality factors for individual samples from the average is very small, with the ideality factors for all the Au/4H-SiC diodes falling in the range of 1.087 – 1.138. In Figure 6.11, the C-V characteristics for Au/4H-SiC diodes are presented. The C-V characteristics also follow a very tight distribution and the average

extracted values of the barrier height and the doping concentration are 1.28eV and 9.08×10^{15} respectively.

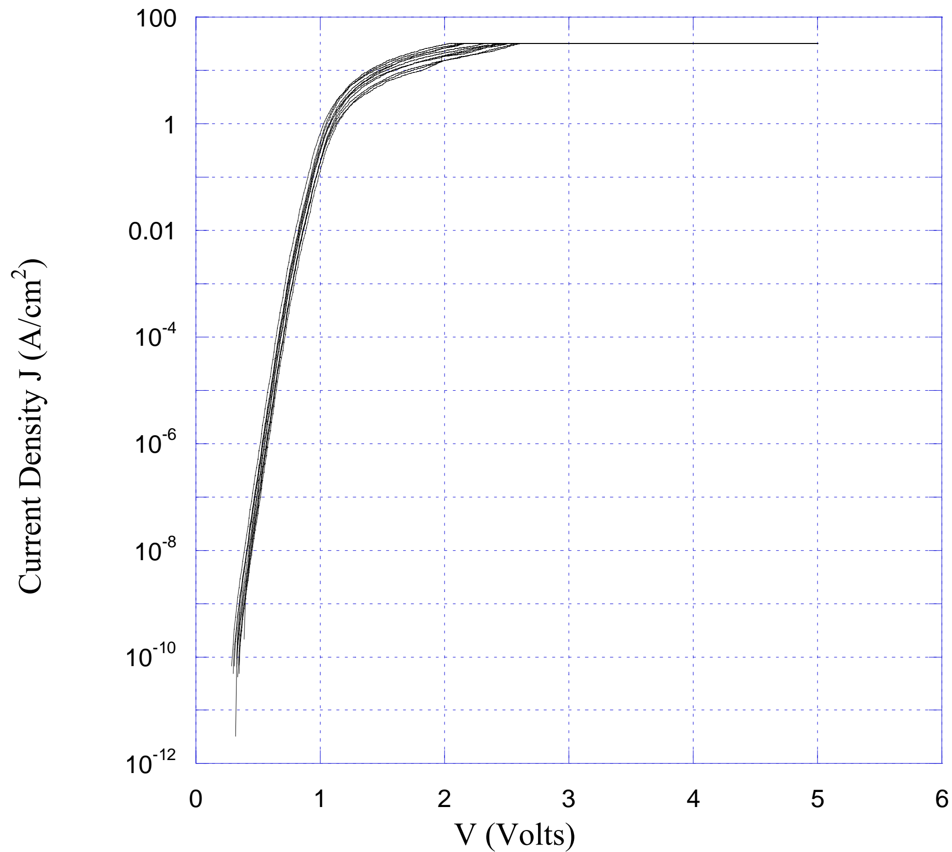

Figure 6.10 Forward I-V Characteristics of Au/4H-SiC Schottky Diodes

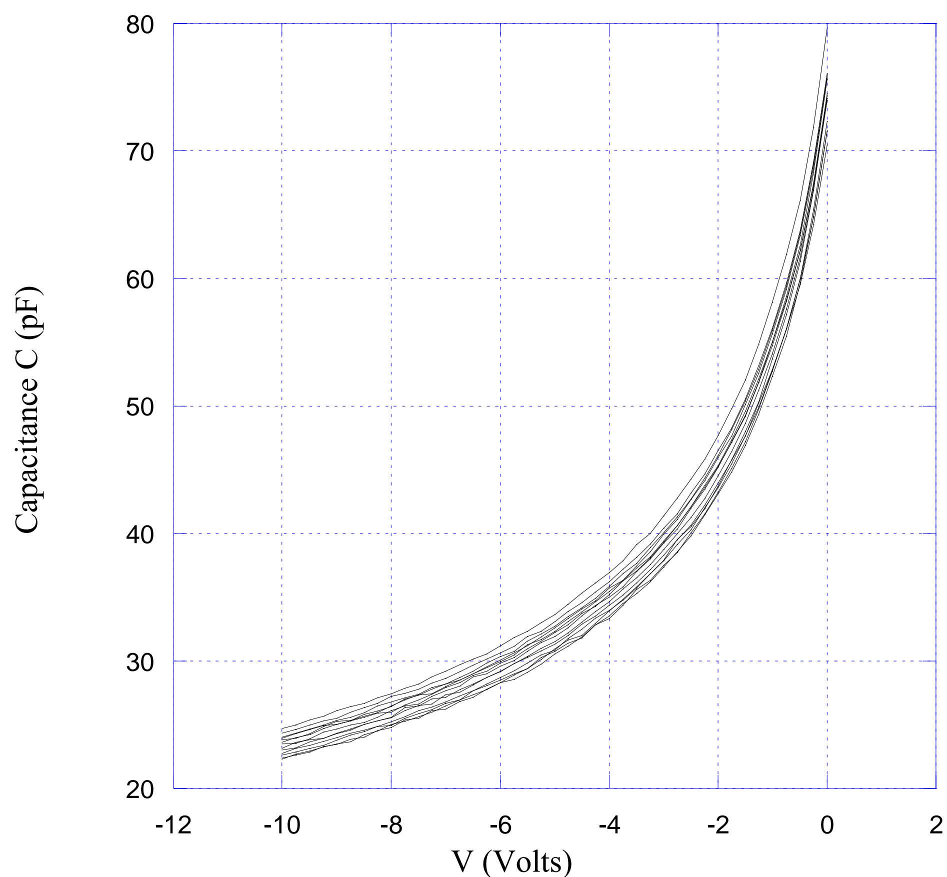

Figure 6.11 C-V Characteristics of Au/4H-SiC Schottky Diodes.

The Au/4H-SiC Schottky diodes have an average barrier height of 1.285eV with the ideality factor of 1.11. This is one of the most ideal diodes fabricated by us. The obtained value of the Schottky barrier height is still well below the Schottky-Mott Limit of 1.5eV. The value of SBH extracted from the C-V measurements is slightly less than that obtained from the I-V measurements. A similar observation was seen in the case of Al/4H-SiC diode where the C-V values of SBH were very similar to the I-V measurements.

6.4 Conclusions

Schottky diodes using three different metals, namely Aluminum, Copper and Gold were fabricated on 4H-SiC die using the revised fabrication procedure and electrically characterized employing I-V and C-V measurements. For each of the as-deposited metal/4H-SiC combinations Schottky Barrier Height ϕ_B, ideality factor η, on-state resistance R, built-in voltage V_i, and the doping concentration were determined. The average value of ideality factor for Au/4H-SiC is 1.11, which is one of the best figures we have got from our fabricated samples. In the case of Al/4H-SiC and Cu/4H-SiC diodes, the diodes were annealed at suitable time-temperature combination and their Schottky parameters were extracted again after annealing. These were then compared with the corresponding as-deposited parameters to study the effect of annealing. It was concluded that annealing strongly affects the metal-semiconductor interface, thus altering the Schottky parameters of the devices.

In both Al/4H-SiC and Cu/4H-SiC diodes, it was observed that annealing at 600ºC and 500ºC respectively for 5 minutes results in an increase in the Schottky Barrier Height and improves (decreases) the ideality factor. Diodes thus annealed have resulted in some of the most ideal diodes fabricated in our lab. To further study the effect of annealing, XPS was performed on the Al/4H-SiC diodes. The XPS results provided a deeper insight into the interface chemistry and revealed that annealing at 600ºC results in Aluminum-Silicon bonding at the interface. It was concluded that the change in the

Schottky parameters of the diodes due to annealing is attributed to the Aluminum-Silicon compound formation at the interface.

CHAPTER 7

SUMMARY AND CONCLUSIONS

In this project, three different types of Schottky diodes, namely Al/4H-SiC, Cu/4H-SiC and Au/4H-SiC were fabricated and electrically characterized. Initial efforts to fabricate the Schottky diodes using a fabrication procedure developed earlier resulted in the partial etching of the Schottky and ohmic contacts. Efforts were made to modify the fabrication process to eliminate the problematic steps of this fabrication process. A new and revised fabrication process was developed for the fabrication of the devices. This new fabrication process employed negative photoresist instead of Aluminum as a protective layer for the ohmic contacts during fabrication. This resulted in a shorter and simpler fabrication process as compared to the old fabrication process. An extension tube was used in addition to the furnace tube during annealing to make the annealing step more robust and to reduce the chances of oxidizing the Nickel ohmic contacts.

The fabricated Schottky diodes were electrically characterized by performing I-V and C-V measurements on them. From these measurement results, Schottky barrier height, ideality factor, substrate doping density, and diode series resistance were extracted. Furthermore, Al/4H-SiC and Cu/4H-SiC diodes were annealed at 600ºC and 500ºC respectively for 5 minutes each using forming gas and then electrically characterized again. Comparison of the as-deposited and annealed parameters revealed that results in increasing the Schottky Barrier Height and lowering the ideality factor. For Al/4H-SiC diodes, the average Schottky barrier height increased to 0.65eV from 0.63eV,

while the average ideality factor was lowered to 1.5 from as-deposited value of 1.7 after 5 minutes of annealing at 600ºC. For Cu/4H-SiC diodes, the average Schottky barrier height increased to 1.28eV from 1.1eV and the average ideality factor was lowered to 1.1 from 1.4 after 5 minutes of annealing at 500ºC. There was insufficient data to exactly determine the cause of the change in the Schottky parameters. Possible reasons for the increase in barrier height and improvement in the ideality factor include formation of point-contact diodes or improved interface due to annealing. For Au/4H-SiC diodes, measurements on the as-deposited diodes gave an average Schottky barrier height of 1.3eV and an average ideality factor of 1.1.

XPS was performed on the Al/4H-SiC samples to study the effects of annealing in further detail. The surface characterization of the Al/4H-SiC revealed than upon annealing at 600ºC, the Si-C bond in SiC dissociates and Aluminum starts bonding with Silicon, leaving free Carbon behind. Analysis of the XPS results shows the presence of $AlSiO_4$ at the Aluminum-SiC interface. It is proposed that the Aluminum-Silicon compound at the Al-SiC interface played a significant role in the change in Schottky parameters of the Al/4H-SiC diode. The data available at this stage is insufficient to conclusively determine the exact mechanisms occurring at the interface.

My original contributions to the research on Schottky contacts to Silicon Carbide can be summarized as below:

- Implemented a revised fabrication process for SiC Schottky diodes. Changes included using a combination of RCA and HF for etching the SiC surfaces and using negative photoresist as a protective layer for back-side Nickel contacts.

- Improved the annealing process by using an extension tube in addition to the annealing furnace tube. Use of the extension tube minimized the chances of the Nickel contacts oxidizing and made the annealing process more robust and standardized.
- Fabricated and electrically characterized Al/4H-SiC, Cu/4H-SiC and Au/4H-SiC Schottky diodes. As-deposited Au/4H-SiC Schottky diodes of ideality factor as low as 1.1 were fabricated, which is very close to an ideal diode. Results portray some of the lowest numbers for ideality factor achieved in our research lab.
- Annealing performed on Al/4H-SiC and Cu/4H-SiC diodes and then electrically characterized again for comparison with as-deposited results. Results show the effect of annealing as increasing the Schottky barrier height and lowering the ideality factor.
- X-ray Photoelectron Spectroscopy (XPS) performed on the annealed Al/4H-SiC to further investigate the effects of annealing. XPS shows the presence of an Al-Si compound, suggesting that upon annealing SiC may dissociate into Si and C, from which the free Si bonds with Aluminum. The formation of an Al-Si phase is proposed to play a significant role in the change in Schottky parameters upon annealing. Further research is required to completely understand the effects of annealing on the interface chemistry

For future work, it is proposed that additional XPS measurements might provide more information on the interface chemistry observed in this project. Efforts should be

made to analyze the metal-semiconductor interface more thoroughly and efficiently. To study the effects of annealing in better detail, it is also proposed that more metal/semiconductor diodes be fabricated using the established fabrication process. Different metals should be used as Schottky contacts and the diodes characterized for comparison. Further annealing tests at varying temperatures might provide deeper insight into the dependence of the Schottky parameters of the diode on the annealing temperatures. Efforts should be made to fabricate Schottky diodes with lower ideality factors for as-deposited contacts. A good starting point for this would be to ensure that the SiC surface is reasonably clear of oxide before proceeding with the deposition of Schottky contacts. Electrical characterization, and more specifically I-V and C-V measurements performed over a suitable range of temperatures, might prove useful in the experimental determination of the Richardson’s constant.

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