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ENERGY LOSS OF IONS IMPLANTED IN MOS DIELECTRIC FILMS

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Abstract

Energy loss measurements of ions in the low kinetic energy regime have been made on as-grown SiO_2 (170-190nm) targets. Singly charged Na^+ ions with kinetic energies of 2-5 keV and highly charged ions Ar^{+Q} (Q=4, 8 and 11) with a kinetic energy of 1 keV were used. Excitations produced by the ion energy loss in the oxides were captured by encapsulating the irradiated oxide under a top metallic contact. The resulting Metal-Oxide-Semiconductor (MOS) devices were probed with Capacitance-Voltage (C-V) measurements and extracted the flatband voltages from the C-V curves.

The C-V results for singly charged ion experiments reveal that the changes in the flatband voltage and slope for implanted devices relative to the pristine devices can be used to delineate effects due to implanted ions only and ion induced damage. The data shows that the flatband voltage shifts and C-V slope changes are energy dependent. The observed changes in flatband voltage which are greater than those predicted by calculations scaled for the ion dose and implantation range (SRIM). These results, however, are consistent with a columnar recombination model, where electron-hole pairs are created due to the energy deposited by the implanted ions within the oxide. The remaining holes left after recombination losses are diffused through the oxide at the room temperature and remain present as trapped charges. Comparison of the data with the total number of the holes generated gives a fractional yield of 0.0124 which is of the same order as prior published high energy irradiation experiments. Additionally, the interface trap density, extracted from high and low frequency C-V measurements is observed to

increase by one order of magnitude over our incident beam energy. These results confirm that dose- and kinetic energy -dependent effects can be recorded for singly charged ion irradiation on oxides using this method.

Highly charged ion results also confirm that dose as well as and charge-dependent effects can be recorded for irradiation of oxides using this method**.** In particular, the results as a function of charge state indicate that there is a significant enhancement in the induced flatband voltage shift as the charge state of the beam is increased. This was quantified by measuring the flatband voltage shift across multiple ion doses for fixed incident charge states to obtain a normalized value of the shift induced per incident ion. These normalized results show an enhancement in the shift, which grows monotonically across our charge state data, from 1.14 x 10^{-12} V/ion for Ar^{1+} ions to 1.12 x 10^{-11} V/ion for Ar^{11+} ions. It is probable that this enhancement in the shift is due to the different potential energy for the two charge states (15 eV for Ar^{1+} and 2004 eV for Ar^{11+}). For example, potential energy deposited into the oxide could produce more electron-hole pairs beyond those generated by kinetic losses such that both effects are captured in the C-V measurements of the MOS devices. If these data are interpreted as a record of the energy loss, then a near-quadratic dependence on the incident charge state emerges which is consistent with results obtained elsewhere.

Dedication

I would like to dedicate my Ph.D. to my parents, Sh. Sukhbir Singh Lakra & Smt. Birmati and my loving daughter Shriya Lakra.

.

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Chapter 1

Introduction

1.1 Ion-Solid Interactions

Decades of research have focused on the mechanisms by which ions lose their energy to a material target upon impact and on the target modifications that can occur. These modifications can involve a complex interplay of effects such as electronic friction, roughening and amorphisation. In general, the dominant phenomena are energy dependent, ranging from quantum mechanical diffraction effects at few meV energies to track formation via atomic displacements at MeV energies[1]. In an applied context, understanding ion-solid interactions is also important, such as in the microelectronics industry where integrated circuits are doped using ion-implantation. With the continuing trend of new devices being scaled down to the atomic level, a better understanding of ion-solid interactions is required if we are to dope the very shallow and laterally constrained target regions these new devices present.

The results of experiments which explore ion-induced damage in oxides are presented in this dissertation. In next two sections, I review relevant studies on ion-oxide interactions and radiation-induced effects in oxides from the 1960's to the present day. Following these reviews, motivation for the experiments I have performed and an overview of the remaining chapters is given.

1.2 Background

The interactions of ions with a target are typically described in terms of the kinetic energy of the incident ions as shown in the Figure 1.1. For incident energies less than thermal energy (below ~ 25 meV), incident ions are trapped at the surface through physisorption or chemisorption. In the energy range of 1 eV to 1 keV, this surface trapping is less effective and there is a high probability of scattering of the ions from the surface. As the energy of the ions increases above 1 keV, more of the ions are implanted into the target. The main interactions for these ions are Coulombic and elastic collisions of the ions with target atoms until the ions are fully stopped and implanted in the target. Additionally, the energy transfer to the target surface lattice atoms induces oscillations which can heat parts of target surface to a very high temperature (thermal spike). Above 100 keV, the main interaction processes are between the ions and the target electrons, and this becomes the dominant interaction in the MeV range. Finally, at energies above several MeV, energy loss occurs by radiative processes. In this dissertation, I have worked in low energy regime (incident energies from 1 to 5 keV) where the ion is most likely implanted in the target.

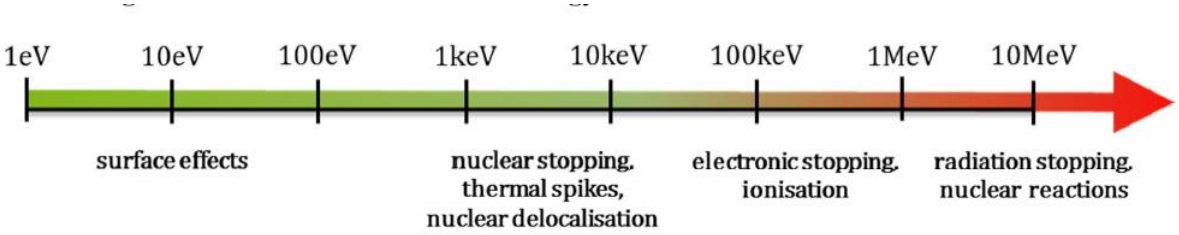


Figure 1.1: Schematic showing the primary interactions of an ion with a solid target as a function of the ion's kinetic energy, from [2].

During the impact of an ion with a material, the ion will lose kinetic energy and the energy loss can be described using the stopping power $S(E)$, which is defined as the energy loss ΔE of the ions per unit distance travelled in the material Δx [3],

$$S(E) = -\frac{\Delta E}{\Delta x} \tag{1.1}$$

The stopping power refers to macroscopic systems and has units of [keV/cm]. This concept is extended to the microscopic level using the atomic density of the target material, ρ, as in

$$s(E) = -\frac{1}{\rho}\frac{\Delta E}{\Delta x} = \frac{1}{\rho}S(E) \tag{1.2}$$

The units of microscopic stopping power, $s(E)$, are [MeV·cm^2/g].

At lower energies, the stopping or slowing of ions is traditionally separated into two distinct processes: electronic and nuclear stopping. The sum of these two processes is called the total stopping power, $S(E)$, which is defined as

$$S(E) = S_e(E) + S_n(E) \tag{1.3}$$

Nuclear stopping power ($S_n(E)$) is the momentum transfer between the ion and the target nuclei. Electronic stopping ($S_e(E)$) is the slowing down due to the inelastic collisions between electrons in the target material and the ion moving through it. Since the number of collisions an ion experiences with electrons is large, and since the charge state of the ion while traversing the medium may change frequently, it is very difficult to describe all possible interactions for all possible ion charge states. Instead, the electronic stopping power is given as a simple function of energy which is an average taken over all energy loss processes for different charge states. It can be theoretically determined to an accuracy of a few percent in the energy range above several hundred keV from theoretical treatments, the best known being the Bethe-Bloch formula[3]. At energies lower than about 100 keV it becomes very difficult to determine the electronic stopping theoretically. Hence several semi-empirical stopping power formulas have been devised. The most used today is the model given by Ziegler, Biersack and Littmark (ZBL stopping) [2]. Below 10 keV/amu, there is sparse data and high uncertainty (> 30%) in the theoretical stopping power vs. experimental stopping power, as shown in Figure 1.2. Also, we can see from figure 1.2 (a), the ion kinetic energy range starts from 1 keV/amu (23 keV for Na ions) which suggests that there is little or no experimental stopping data

for Na^+ ions at low energy(below 10 keV). Therefore, one of the motivations for our study was to obtain data for energy loss in the low kinetic energy regime. Also, there is little experimental data or theoretical predictions for stopping power for highly charged ions (HCI). The MOS devices used in this study can be used to obtain quantitative data for the energy loss of HCIs and preliminary data for such studies is discussed in the Chapter 4.

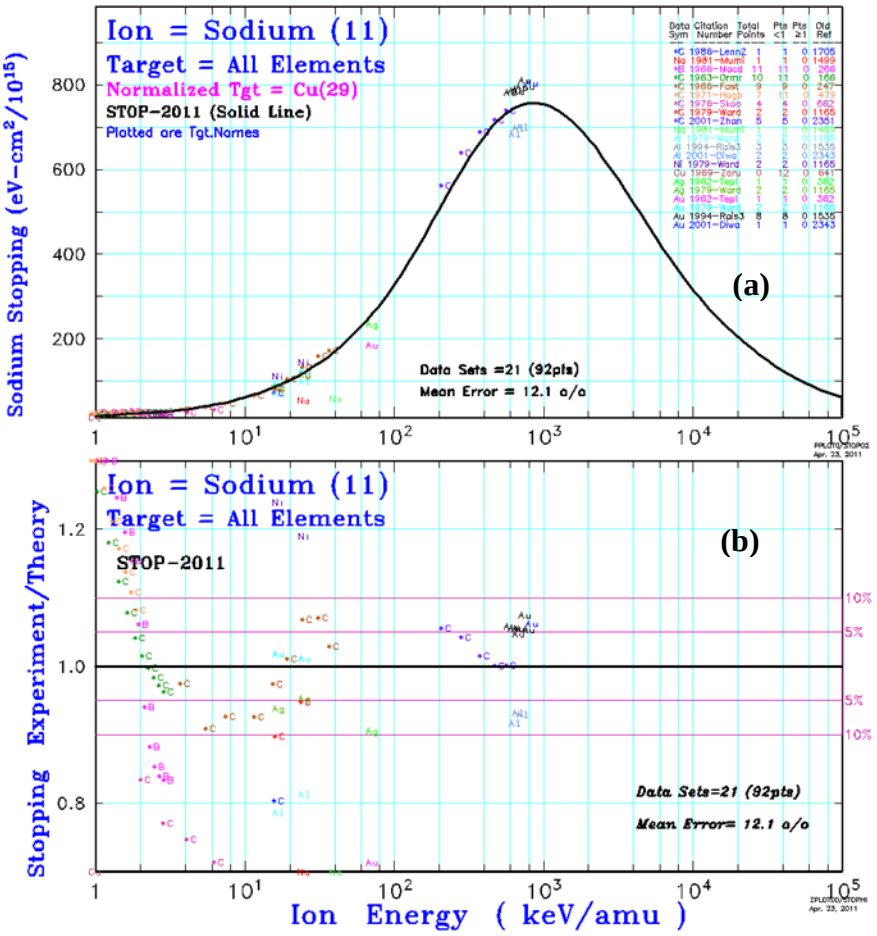


Figure 1.2: Comparison of experimental and theoretical stopping power data for sodium ions on various targets as obtained from SRIM. The upper plot (a) shows data and theory, normalized to a Copper target. The lower plot (b) shows the ratio of data and theory. Adapted from [3,4].

1.3 Ion-Oxide Studies

Initial studies of ion-oxide interactions focused on ion-implantation which was first used in the 1960s to dope silicon at precise depths below the surface. These early studies showed that there is damage during the implantation which can be removed by thermal annealing. This was a primary focus since removing the damage was important for using doped silicon in the semiconductor industry[5]. The understanding of the ion-solid interactions remains important for the microelectronics industry as most integrated circuits are still doped using ion-implantation. The continuing trend of new devices being scaled down to the atomic level requires a better understanding of ion-solid interactions for doping of very shallow and laterally constrained regions [6].

One of the early studies to see the effects of ion implantation was made in 1970 by Chou *et al.*[7] at IBM Watson Research Center using O^+ and Ne^+ of various energies (20 to 150 keV) on thermally grown silicon dioxide films having various thicknesses. Metal-oxide-semiconductor (MOS) capacitors made with these films were subsequently annealed at different temperatures to remove implantation effects. They found that the damage due to ion implantation may include one or all of the following effects: displacement damage in the oxide, creation of fixed positive charge and fast states near the silicon interface.

In 1975 Bruce E. Deal reviewed the different types of oxide charges (fixed charge-state charges, charges due to mobile impurity alkali ions, fast surface states and charges introduced by ionizing radiation) present in thermally grown silicon

dioxide. Additional radiation induced charges may arise from x-rays, electrons, neutrons etc., or may be introduced during the manufacturing process, such as ion-implantation, sputtering or electron-beam metallization. Deal concluded that the physical origin of these charges, except mobile charges, was related to silicon bond defects introduced by processing [8].

In 1979 McCaughan *et al.*[9,10] studied the effects of low energy ions (N_2^+) and neutral (N_2^0) particles on silicon dioxide films at Bell Labs. They found that the neutral particle bombardment produces substantially less fixed charge at the SiO_2/Si interface as compared to ions at the same dose, but the neutral particles produce a large interface density across the bandgap. The two possible explanations are mobile impurity ions and holes generated due to neutralization of the ions. In the ion bombardment of SiO_2/Si structures holes are produced by both potential and kinetic processes whereas in the case of neutral particles, holes are produced only by kinetic processes. Holes produced in the process are mobile and they move towards the interface under internal the electric field and can be trapped there.

Powell *et al.*[11] studied the effects of the location of the radiation onto oxide using ultraviolet (UV) rays as they can control the depth of the radiation absorption into the oxide. They showed large positive charge effects in MOS structures irradiated with photon energies above 8.8 eV under positive gate biasing, and etching experiments showed that the positive charge was induced near the SiO_2/Si interface (within 300 Å) even when radiation was absorbed near the gate electrode.

Mizutani *et al.*[12,13] also studied the effects of Ne^+ ions and Ne^0 neutral particles with doses in the range of 10^{15} to 10^{18} /cm^2 on 115 nm thick SiO_2 which was not annealed after the irradiation. They found that the amount of radiation damage caused by Ne^0 particles is significantly smaller than that by Ne^+ ions. They also etched the SiO_2 in steps and found that most of the positive charge is at metal/SiO_2 and that the trapped charge is present throughout the oxide, a result which is consistent with other studies.

In 1991 Yokogava *et al.*[13] also irradiated 120 nm SiO_2 with ion or neutral beams of He, Ne, Ar and Xe having beam energy between 300 and 800 eV with doses ranging from 10^{16} to 10^{17} /cm^2. They did electron spin resonance (ESR) measurements on the samples to study the defect generation mechanism. They found that the E' defect center (unpaired electron on the Si atom) yield was greater for ion than for neutral bombardment. Also, the E' center generation yield was greater for He^+ ions, which has a higher ionization energy (E_i= 24.58 eV) than for lower ionization energy ions of Ar^+ (E_i =15.96 eV) or Xe^+(E_i =12.08eV). The E' center peak was also observed to disappear after etching of the top 10 nm of the oxide, which suggests that they exist only in the top SiO_2 surface layer.

Mizutani *et al.*[14] have also used Rutherford backscattering data to study structural modifications induced by irradiating amorphous SiO_2 with (300-500 eV) ion and neutral beams of Ne, Ar and Kr. They found that in case of Ne^+ beam irradiation, the top surface is oxygen deficient and silicon rich which suggests that the oxygen was preferentially sputtered by the ion beam. In the case of neutral beam irradiation, no preferential sputtering of oxygen was observed.

Nagai *et al.*[15] recently studied the effect of 100 keV Na^+ ions implanted into SiO_2 (1μm) at a dose of 10^{15} /cm^2. They studied the samples with infrared absorption(IR) and electron paramagnetic resonance (EPR) and found that E' and peroxl defect centers are uniformly distributed throughout oxide and peak at the Si/SiO_2 interface even though the projected range of the damage from the ions obtained from SRIM is 400 nm. They concluded that dangling bonds are created by ion-implantation and that annealing at 600°C for 30 minutes restores the Si-O bonds. Furthermore, they found that ion-implantation induces micro voids in the films and that the void volume does not change even after annealing.

Devine [16-18] has discussed the mechanism of creation of E' defects by radiation as a physical knock on of one of the bridging oxygen atoms followed by the trapping of a hole in the radiation cascade. He has shown that radiation and implantation damage involve large changes in the Si-O-Si bond angle with small densification of SiO_2. Also, he has shown that for this to occur the energy deposited into the nuclear displacement process must be greater than 3×10^{23} eV cm^{-3}(this corresponds to 3.4 eV per Si-O bond which is close to the Si-O bond energy or energy deposited into ionization/electronic greater than 2×10^{26} eV cm^{-3}).

Lenahon *et al.*[19,20] have extensively reviewed the EPR measurements of Si/SiO_2 systems. They find that there are two types of defects: P_b and E' centers. P_b are "trivalent" silicon centers which are the dominating interface trap centers at or near the Si/SiO_2 interface. They have also shown that when MOS capacitors are subjected to ionizing radiations, P_b centers are generated in densities approximately similar to the average of

the interface trap densities generated in the mid gap and the annealing characteristic of P_b centers and interface trap densities are identical as shown in Figure 1.3. This shows that the radiation induced interfaces traps are the P_b centers.

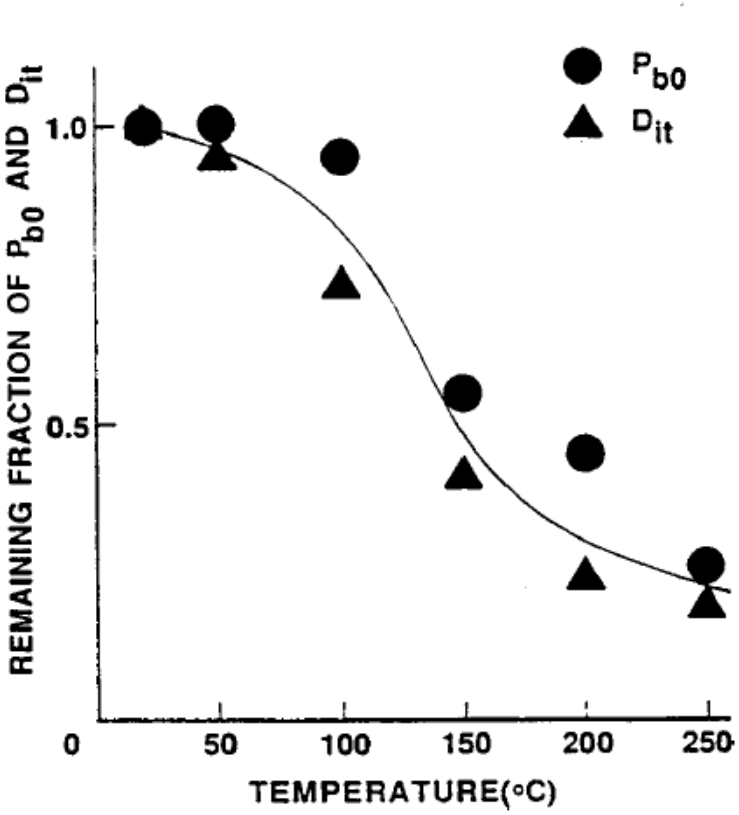


Figure 1.3: Annealing behavior of P_b centers and interface trap densities at the silicon midgap from [19].

E' centers are the dominant hole trap centers in the thermally gown oxide and involve an unpaired electron localized on a silicon which is backbonded to three oxygen atoms. In the case of particle bombardment, the Si-O bond is broken and if a hole comes to reside on the broken bond site, the unpaired electron on the Si atom at the broken bond

site gives rise to an E’ center. Lenahon *et al.* also found roughly one to one correspondence between E’ density and trapped hole density in the oxide and that they have the same annealing response in air as shown in Figure 1.4.

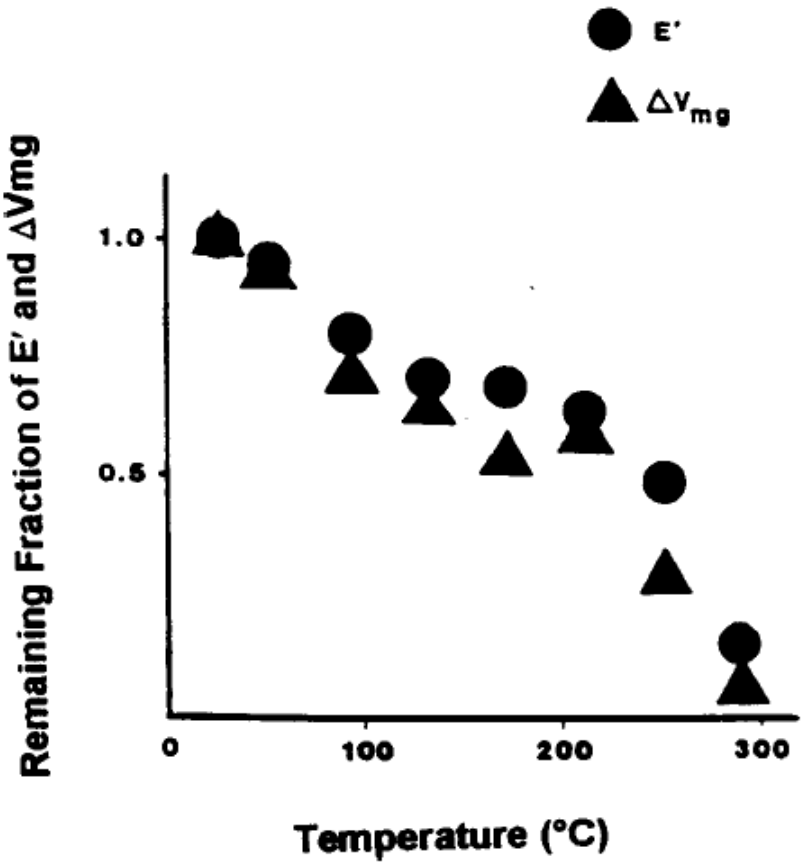


Figure 1.4: Annealing behavior of E' centers and trapped hole densities from [19].

1.4 Radiation Effects

The first studies of radiation effects in semiconductor devices were made in the 1960s following the detonation of the high-altitude nuclear device Starfish by the U.S. in 1962 and other similar events by the Soviet Union in the same year[21]. As a result of these events, the nuclear contamination of the exoatmospheric region caused the failure

of the communication satellite Telstar I in 1963. Detailed studies of the radiation damage in semiconductor devices followed, and with the knowledge gained from these studies, the satellite was successfully repaired by modifying the electrical biasing of the transistors using commands from the ground. Prior to this time, radiation-effects studies were done on the bulk properties of semiconductor materials and devices.

The birth of this new field led the way for the study of radiation effects in metal-oxide-semiconductor (MOS) devices as the emphasis shifted from bipolar transistors to MOS field effect transistors (MOSFETs) used in high-density, low-power complementary MOS (CMOS) integrated circuits required for satellite systems [21].

The initial studies of total-ionizing-dose (TID) degradation in MOS devices were done at the Naval Research Laboratory (NRL) in 1964 by Hughes and Giroux. They found a high sensitivity to ionizing radiation by Co^{60} γ irradiation in both n-channel and p-channel transistors[21]. The following year, Hughes found a metal-oxide-semiconductor (MOS) structure to be a powerful tool to study the effects of radiation. Using MOS capacitor threshold voltages and flatband voltages, he concluded that the major effects of the radiation were buildup of positive charge in the silicon dioxide and that this charge was able to drift under an applied electric field[22]. Later in 1967, Snow *et al.* studied the irradiation of MOS capacitors for many types of radiations: Co^{60} γ rays, low energy electrons, high energy electrons and ultraviolet rays and x-rays. It was concluded that any ionizing radiation with an energy greater than 8 eV (bandgap of SiO_2) can cause the following effects: 1) the buildup of positive space charge within the oxide, and 2) the creation of interface states at the oxide/silicon interface. These charges can be

neutralized if electrons are introduced into the oxide. Both of these effects saturate at a dose of 10^8 to 10^9 rad, and they can be completely annealed out at 250°C[21,23]. A simple model explaining these effects was given by Zainiger[24] and Snow et al.[23]. The ionizing radiation incident on the oxide creates electron-hole pairs by breaking silicon-oxygen bonds. Some of these induced carriers recombine and the remaining carriers drift to the appropriate electrodes under the applied electric field (e.g. the holes towards the silicon interface under positive gate biasing). Because of the higher mobility of electrons versus holes (several (at least 6) orders of magnitude), the electrons are swept out of the oxide and the holes drift to the Si/SiO_2 interface under positive gate biasing, where a fraction of them are trapped near the interface (few nanometers).

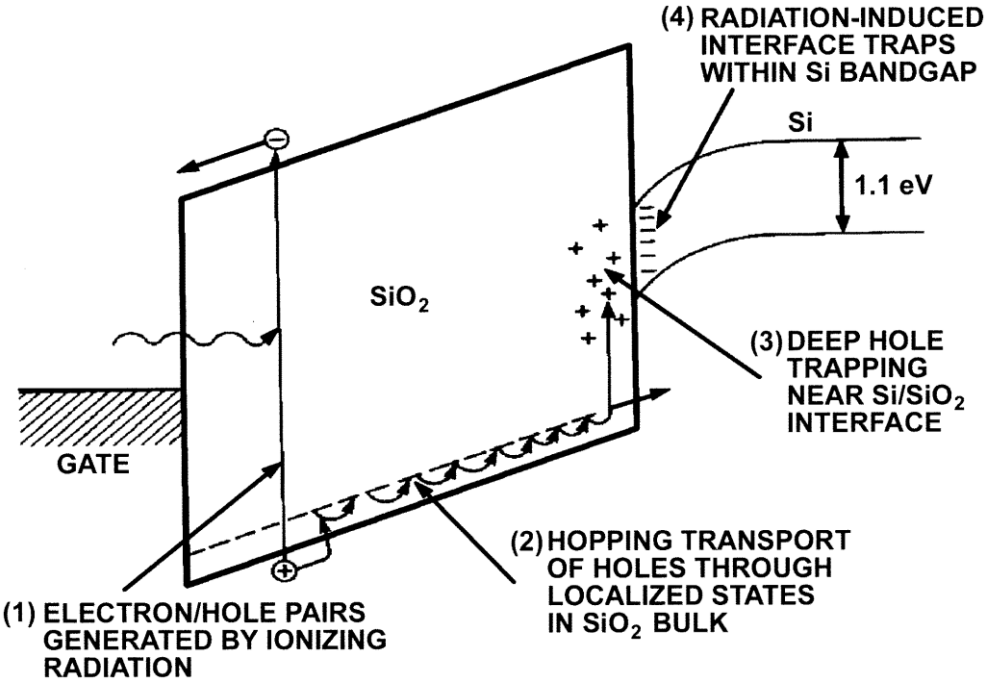


Figure 1.5: MOS energy band diagram showing the major physical processes after irradiation, from [25].

There are four major processes as shown in the figure 1.5 following irradiation under positive gate biasing:

1) Electron-hole pairs are produced because of the energy deposited into the oxide by the ionizing radiation. The electrons are swept out of the oxide in a picosecond or less as the mobility of the electrons is eleven orders higher than the holes[26]. Some fraction of the created holes will recombine with electrons in that picosecond which depends upon the electric field and the type of radiation. The holes will be immobile in that time frame and they will remain at the place of their generation.

2) Then, the holes diffuse through the oxide and Si/SiO_2 interface by hopping through the localized states. At room temperature, this process is completed within 1 second (our case) as it has been verified from numerically solving the differential equation for transport of holes[27]. In general this process is dependent on the applied/internal electric field and on temperature.

3) When the holes reach the Si/SiO_2 interface, some fraction of them are trapped into deep level traps near the interface. These traps are located near the Si/SiO_2 interface because of incomplete oxidation. There is one single oxygen atom missing from a Si-O-Si bond leaving a weak Si-Si bond where each silicon is bonded to three oxygen atoms. This oxygen deficiency is also linked to the E' center , which is an oxygen deficient "trivalent silicon" [20].

4) The fourth process is the radiation/implantation induced buildup of the interface traps at the Si/SiO_2 interface having energy levels in Si band gap. Their occupancy is determined by the Fermi level and they change their occupancy with response to the biasing voltage. Also, they are dependent on the oxide processing. When the holes are trapped in the oxide, they releases positive ions (protons) and these ions (protons) migrate under the applied bias towards the Si/SiO_2 interface. These ions (protons) then interact with dangling bonds at the interface that have been passivated earlier with another proton. Because of this interaction, H_2 is released and a dangling bond is reformed, which is called an interface state[21,28].

A new field of radiation hardening (the fabrication of electronics resistant or tolerant to damage from ionizing radiation) was started in 1971 by Aubuchon [29]. He obtained the best radiation hardening with the following parameters: 1) use of <100> Si as starting wafers, 2) oxidation growth in dry O_2 at 1000°C, 3) to avoid post-oxidation anneal in N_2 4) deposition of Al gates via thermal evaporation (electron beam evaporation generates soft x-rays, which degrade the oxide and these effects can be annealed out at 400°C for short times), 5) avoidance of ion implantation, as ion implantation causes radiation damage, which can then be annealed out at 500°C.

Another study was done by Derbenwick and Gregory on process optimization of radiation hardness of CMOS circuits [30,31]. They found that thinning of the oxides reduced the voltage shifts by a factor of t_{ox}^3 due to 1) the total number of holes created is proportional to the volume of the oxide, 2) the voltage shifts are proportional to the first moment of the charge distribution, and 3) the characteristic penetration depth of hole traps at the Si/SiO_2 interface is proportional to the oxide thickness (processing). Also in general thicker oxides have high defect density because they are subjected to high temperature during subsequent growth. Reducing the growth temperature near 1000°C and hydrogen content during post oxidation steps was found to be useful for increasing the radiation hardness of the oxides.

Later in 1985, the thickness dependence of the thinner oxides was investigated by Saks and Bednett[31]. They found a rapid decrease in hole trapping for thinner oxides (below 10 nm) at both interfaces, Si/SiO_2 and metal/SiO_2 interface because of removal of the trapped holes due to tunneling.

In the last 50 years, great progress has been made to understand the radiation effects in MOS capacitors, MOSFET transistors, bipolar devices and ICs. The defects responsible for radiation induced effects have been identified as O vacancies in SiO_2 and dangling Si bonds at the Si/SiO_2 interfaces. Methods and processes have been developed to reduce these effects to make radiation hardened (tolerant) technologies for application such as space, defense and radiation environments [31].

In this dissertation I have studied ion-solid interactions, with a focus on singly charged ions, in the kinetic energy range of 1 to 5 keV. In particular, I have studied the electronic losses of the ions in this regime using MOS capacitors. In chapter 2, I describe MOS physics including the band diagram, flatband condition, definition of different types of oxide charges and the modes of operation of an MOS capacitor. In chapter 3 experiments are presented where singly charged ions are implanted into the oxide of MOS devices which are then characterized by high/low frequency capacitance-voltage (C-V) measurements. The results of these experiments reveal that flatband voltage shifts and changes in the C-V slope of beam irradiated devices are energy dependent. In particular, the flatband voltage shifts are greater than those expected for mobile charges only, implying an irradiation-dependent effect. Finally, in Chapter 4, I summarize this work and present preliminary results for highly charged ion irradiated MOS devices.

Chapter 2 Metal Oxide Semiconductor Devices

2.1 Introduction

In the semiconductor industry, the Metal-Oxide-Semiconductor (MOS) capacitor forms the basis of the MOS Field Effect Transistor (MOSFET) which is the backbone of integrated circuits. It also serves as a useful diagnostic tool for determining the process quality of integrated circuit fabrication because it is easy to fabricate and analysis requires only one dimensional treatment[32]. MOS capacitors have a simple structure which we can think of as a parallel plate capacitor with a metal gate as one electrode and silicon as the other electrode separated by an insulating layer of oxide as shown in Figure 2.1.

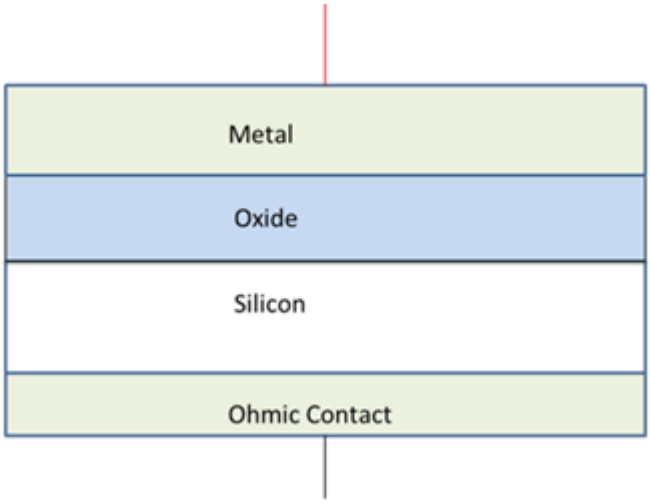


Figure 2.1: MOS Capacitor. Basic design consists of top metal contact and silicon separated by an oxide. The ohmic contact is necessary to give the device a non-rectifying characteristic in a circuit.

MOS capacitors are sensitive to charges and hence, they can be used to detect charges in the SiO_2, at the Si/SiO_2 interface, and in the silicon. They are also used for measuring the following properties of the MOS system: a) obtain oxide thickness, oxide breakdown field b) charge configurations in the oxide and at the Si/SiO_2 interface c) interface traps level density as a function of energy in the bandgap d) properties of electron and hole traps in the oxide and at the Si/SiO_2 interface e) capture probability for both electrons and holes as a function of energy in the bandgap f) surface band bending, and g) depletion layer width in the silicon as a function of gate biasing and doping profile in the silicon.

In this chapter, in section 2.2, we describe MOS physics including the band diagram, flatband condition and the definition of different types of oxide charges. Also, we derive the flatband voltage condition for an ideal MOS and a non-ideal MOS capacitor in the presence of the oxide charges. In section 2.3, we describe the modes of operation of MOS capacitor.

2.2 MOS Physics

2.2.1 Band Diagram

To understand the operation of an MOS device, we must first examine its energy-band diagram. Figure 2.2 shows the energy levels of Metal (Aluminum), Oxide (SiO_2) and Semiconductor (p type Si) as three separate components of an ideal MOS system*. The vacuum level, E_o, represents the energy that an electron would have if it is free of the influence of any material and thus must be continuous in space. The work function is represented by $q\Phi$ having units of energy (eV) and it is the difference between the

vacuum level, E_o and the Fermi level, E_f. In Fig. 2.2, the work function for p-type Si** having doping concentration, $N_a \approx 1.1\times10^{15} cm^{-3}$ is shown as $q\Phi_S$ =4.9 eV and for Aluminum it is, $q\Phi_M$ =4.1 eV.

In figure 2.2, electron affinity is denoted by $q\chi_s$ having units of energy (eV) and it is the difference between the vacuum level and the conduction-band edge. It is a constant for the material, which for silicon is , $q\chi_{si}$=4.05eV and for silicon dioxide is $q\chi_{ox}$ =0.95 eV. Also shown in the figure is the bandgap for Si (1.12 eV) and for SiO_2 (8 eV).

* An ideal MOS capacitor consisting of its oxide and interface with Si free of any charges.

** In the semiconductor, $E_{f,}$ is a function of the doping concentration. For example for p-type Si , $E_f = E_i - kT\ln\left(\frac{N_a}{N_i}\right)$. Hence semiconductor work function, $q\phi_s$, is also a function of Si doping.

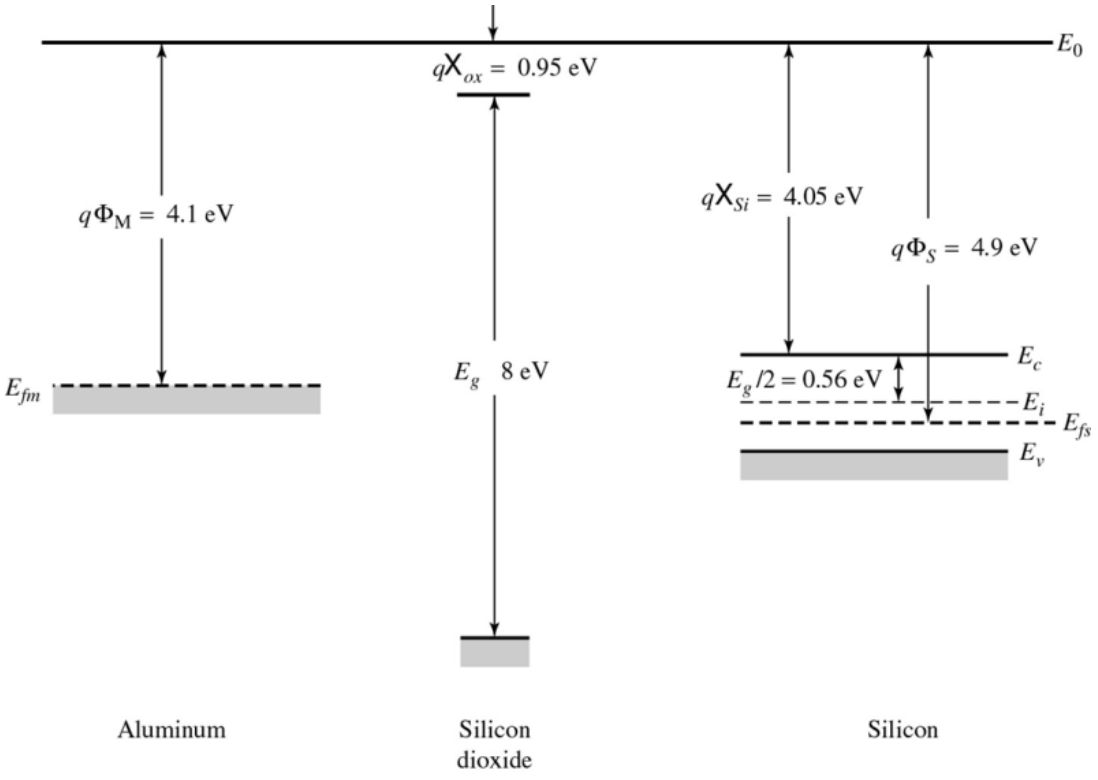


Figure 2.2: Energy levels of Metal [Al] , Oxide[SiO_2] and p-type Semiconductor[Silicon] in separated form[33].

If there is no path for charge flow between the metal and semiconductor, then the MOS capacitor can remain in non-equilibrium condition for a long time as shown in the figure 2.2. However, the MOS capacitor is generally a part of a larger integrated circuit and there is always an alternate path for charge flow between the metal and semiconductor. Hence the MOS capacitor archives the thermal equilibrium condition which is discussed in the next section.

2.2.2 Thermal Equilibrium

When the metal, oxide and semiconductor are brought together, the Fermi levels in the different materials are equalized by the transfer of negative charge from materials with a higher Fermi level (lower work function) across the interfaces to materials with a lower Fermi level (higher work function). The combined system will be at thermal equilibrium only when E_f is constant throughout the system because all quantum levels at a given energy must have equal occupation probabilities[32]. We can see this in our case for the MOS system as shown in figure 2.3, where negative charge will be transferred from the aluminum to the silicon due to their work function difference, $q\Phi_M = 4.1eV < q\Phi_s = 4.9eV$ to bring the system to thermal equilibrium*. The electrons from the metal move into the silicon, where they recombine with the holes from the Si making it less p-type, so the conduction band bends towards the Fermi level to make it less p-type or more n-type since for n-type Si the conduction band is nearer to the Fermi level as shown in figure 2.3.

*The state of thermal equilibrium is defined as the state of an isolated system when any of its macroscopic quantities like temperature, potential, charge and volume does not change with time. (Practically, the quantities are constant for time scale of interest).

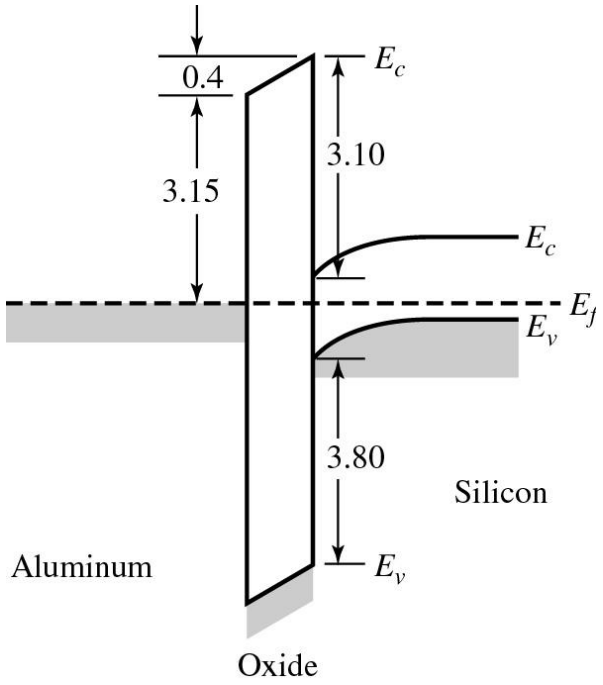


Figure 2.3: Energy-band diagram of MOS system at thermal equilibrium [33]. All energies are in units of eV.

However, the presence of the insulating layer prevents the charge transfer through the oxide but the charge is transferred through an external circuit as discussed in the previous section. The electrons are transferred from the metal to silicon which leaves a thin sheet of positive charge at the metal surface and negatively charged acceptors extend into the silicon from the oxide/silicon interface. There is a voltage drop across the MOS capacitor because of the charges stored on both sides which is shown as a tilt in figure 2.3. The total voltage corresponding to the difference in their work functions (for Al and Si case, it is 0.8V) is divided across the oxide and space charge region in silicon given by

$$V_{total} = V_{oxide} + V_{Si} \tag{2.1}$$

2.2.3 Flatband Voltage: Ideal case

The MOS system at thermal equilibrium is like a capacitor which is charged to the voltage difference between the metal and semiconductor work functions. When we apply a biasing voltage, then it changes the thermal equilibrium condition. In our case, the Al gate has a positive charge and the Si has a negative charge at the thermal equilibrium condition. When we apply a negative 0.8 V to the gate, then it opposes the built-in voltage on the MOS capacitor and the stored charge is reduced to zero. At this condition, as shown in figure 2.4, the energy bands in the silicon are flat near the surface and in the bulk; the voltage which produces this condition is called the flatband voltage(V_{FB}). This particular example assumes that there are no charges in the oxide (ideal case).

Therefore,

$$V_{FB} = \Phi_M - \Phi_S = \Phi_{MS} \tag{2.2}$$

where Φ_M and Φ_S are the work functions of the metal and semiconductor respectively, and Φ_{MS} is defined as the metal-semiconductor work function difference.

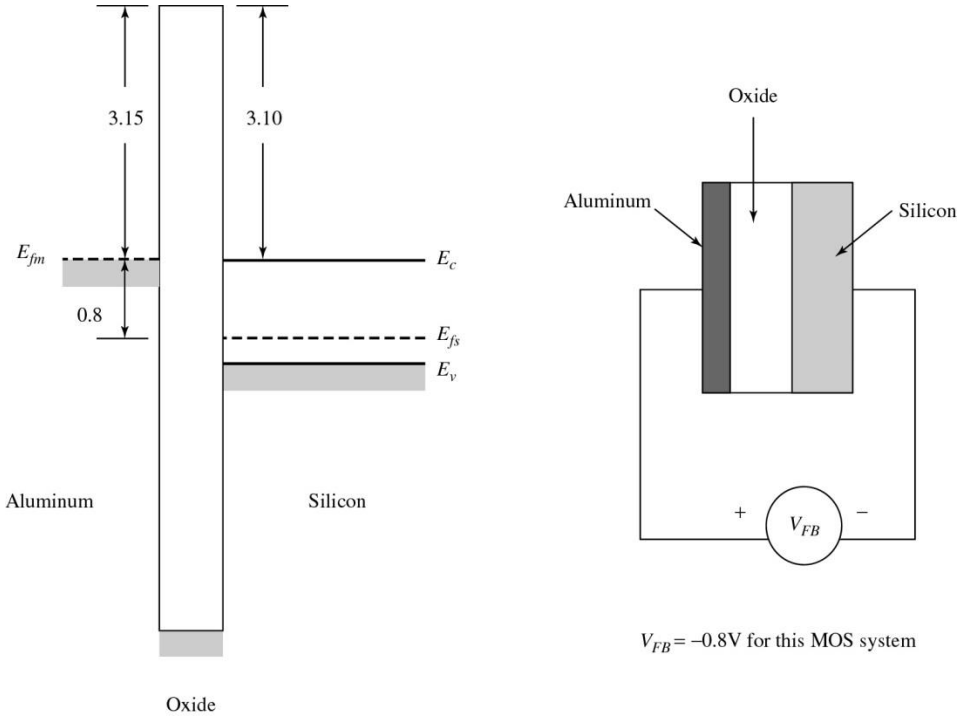


Figure 2.4: Energy-band diagram of the MOS system under flatband conditions. A flatband voltage of -0.8V is applied at the Al gate[33].

2.2.4 Flatband Voltage: non-ideal case

In the previous section, we have assumed a charge-free oxide for determining the flatband voltage of Eq. 2.2, but in reality the oxide will have charges in the bulk and at the oxide-silicon interface which will shift V_{FB} from the ideal case. In order to make the MOS system useful for normal operation in MOSFETs, oxide charge densities are typically kept on the order of 10^{10} cm^{-2} or lower. For example, in 190 and 50 nm SiO_2 an oxide charge density of 10^{10} cm^{-2} will produce maximum flatband voltage shifts of

0.08 V and 0.02V respectively, which are acceptable for normal device operation. However, an oxide charge density of 10^{12} /cm^2 will produce maximum flatband voltage shifts of 8 V and 2V in 190 and 50 nm of SiO_2 respectively, which are not acceptable for the normal operation of a MOSFET transistor. In this section we will derive the flatband condition in the presence of oxide charges.

First we consider a positive charge sheet of density $Q_{ox}^{'}$ in the oxide at a distance x_1 from the metal-oxide interface. It will induce equal and opposite charges that are divided between, Q_G, in gate and Q_s, in silicon as shown in the figure 2.5 (a). The closer the charge sheet is to the oxide-silicon interface ($x \approx x_{ox}$) the larger the fraction of the induced charge will be in the silicon. These induced charges change the total stored charge in the silicon at thermal equilibrium as shown in figure 2.5 (a), and hence it changes the flatband voltage condition which is illustrated in the figure 2.5(b).

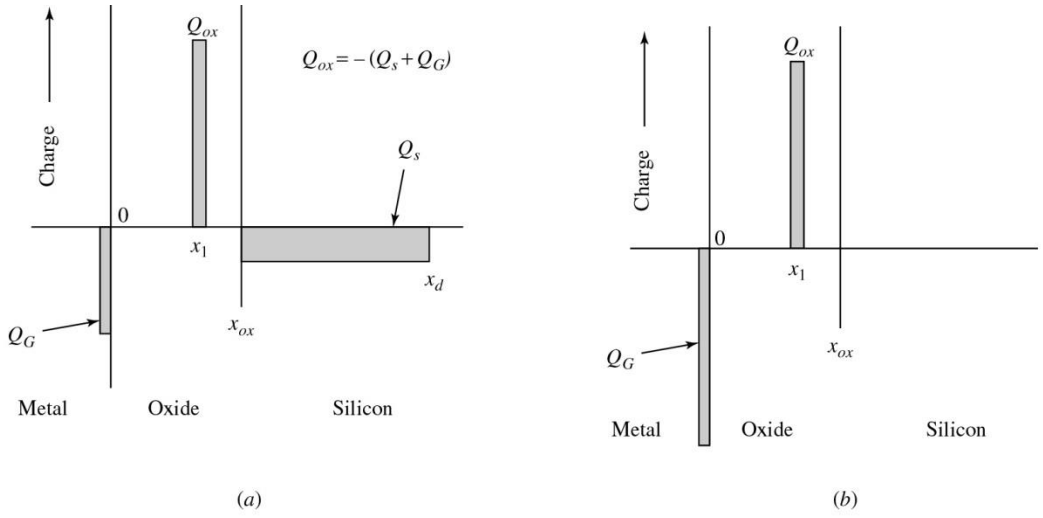


Figure 2.5: Effects of oxide charge on an MOS capacitor (a) charge configuration at zero biasing; b) charge configuration under flatband condition [33].

The magnitude of the flatband voltage shift can be found by using Gauss's law to determine the value of gate voltage such that all the induced charge due to oxide charges is in the gate electrode and none is in the silicon as shown in figure 2.5 (b). The electric field is constant between x=0 to x=x_1 and is given by Guass' law as

$$\oint_s \overrightarrow{E}.\overrightarrow{dS} = \frac{Q_{ox}}{\varepsilon_o \varepsilon_{ox}} \tag{2.3}$$

For a uniform device area, *A*, Equation 2.3 becomes,

$$E_{ox} \bullet A = -\frac{Q_{ox}}{\varepsilon_o \varepsilon_{ox}} \tag{2.4}$$

Therefore,

$$E_{ox} = -\frac{Q_{ox}^{'}}{\varepsilon_o \varepsilon_{ox}} \tag{2.5}$$

where $Q_{ox}^{'} = Q_{ox} / A$ is oxide charge per unit area ($Coul \cdot cm^{-2}$) and the negative sign

is used for negative image charge induced in the gate electrode due to positive charges in the oxide.

The voltage which causes this condition is called the flatband voltage and is given by

$$\Delta V_{FB} = -\int \vec{E} \bullet \vec{dl} = E_{ox} \bullet x_1 \qquad (2.6)$$

Using oxide capacitance per unit area, $C' = \frac{\varepsilon_o \varepsilon_{ox}}{x_{ox}}$, Equation 2.6 gives the change in flatband voltage due to a charge sheet , Q'_{ox} ,as

$$\Delta V_{FB} = -\frac{Q'_{ox} \bullet x}{C'_{ox} \bullet x_{ox}} \quad (\ 0 \le x \le x_1) \qquad (2.\ 7)$$

where $C'_{ox} = C_{ox} / A$ is capacitance per unit area ($F \cdot cm^{-2}$) and $C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{x_{ox}}$ is the capacitance of a capacitor having device area, A , and oxide thickness, x_{ox} , and for a MOS capacitor, it is the capacitance in the accumulation region.

For an arbitrary oxide charge density, we can write a differential slice of charge density of thickness, *dx*, as

$$Q'_{OX} = \rho(x)dx \qquad (2.8)$$

Using equations 2.7 and 2.8, we can write the differential flatband voltage change as

$$dV_{FB} = -\frac{\rho(x)xdx}{C_{ox}^{'} \bullet x_{ox}} \tag{2. 9}$$

Integrating across all the oxide, we can write the total change in flatband voltage for an arbitrary oxide charge density as

$$\int_{0}^{\Delta V_{FB}} dV_{FB} = -\int_{0}^{x_{ox}} \frac{\rho(x)xdx}{C_{ox}^{'} \bullet x_{ox}} \tag{2.10}$$

Rearranging the terms, finally, we get change in flatband voltage for an arbitrary oxide charge density $\rho(x)$ as

$$\Delta V_{FB} = -\frac{1}{C_{ox}^{'}} \int_{0}^{x_{ox}} \frac{\rho(x)xdx}{x_{ox}} \tag{2.11}$$

This is the change in flatband voltage for an arbitrary charge density, $\rho(x)$, in the oxide and is useful for the case when we know the oxide charge density distribution in the oxide.

2.2.5 Oxide Charges

There are four types of oxide charges associated with the Si/SiO_2 system. Because of lack of terminology, a committee was established in January 1978 by the Electronics Division of the Electrochemical Society and IEEE-sponsored Semiconductor Interface specialists Center Conference [34] and they recommended names for four types of oxide charges as shown in figure 2.6.

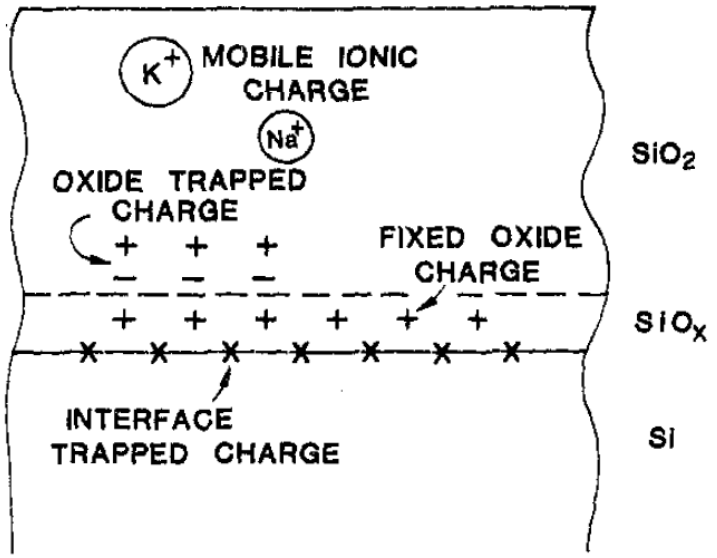


Figure 2.6: Names and location of charges in thermally oxidized silicon from [34].

The oxide charges[34] are defined in terms of

Q: defined as the net effective charge per unit area at the Si-SiO_2 interface (C/cm^2), although the actual charge density may be considerably larger if the charge is located some distance from that interface.

N: defined as the net number of charges per unit area at the Si-SiO_2 interface ($number/cm^2$), although the actual number density may be considerably larger if the charge is located some distance from that interface

1) Fixed Oxide Charges (Qf, Nf): Positive charges, primarily due to structural defects (ionized silicon) in the oxide located within a very thin (< 2.5 nm) transition layer of non-stoichiometric silicon labeled as SiOx at the boundary between Si and SiO2. They are not in electrical communication with the underlying silicon.

2) Mobile Ionic Charge (Q_m,N_m): Primarily due to ionic impurities such as alkali-metal ions Li^+, Na^+, K^+ and H^+. They will drift under bias above 100 °C and cause device instabilities as they affect the flatband voltage. Their mobility increases rapidly with temperature[8].
3) Oxide Trapped Charge(Q_{ot}, N_{ot}): Positive or negative, due to holes or electrons trapped in the bulk of the oxide. The trapping may be due to production of electrons-holes due to ionizing radiation, avalanche injection, ion implantation damage, sputtering of metals or dielectrics and electron beam metallization. They are located in traps distributed throughout the oxide layer.
4) Interface Trapped Charge(Q_{it}, N_{it}): Positive or negative charges, due to structural, oxidation induced effects, metal impurities and other defects caused by radiation or breaking of the bonds. They are in electrical communication with the underlying silicon.

In case of interface traps, Q_{it} is the interface trapped charge or interface trap level density[32] residing in trapping levels N_{it} (traps cm^{-2}). The N_{it} levels are located at the oxide-silicon interface and have energies within the forbidden energy gap. They are distributed with density D_{it} (number cm^{-2} eV^{-1}).

In our experiments with ion-implanted oxides, both oxide trapped charges as well as interface trapped charges are observed due to the implantation of the ions in the oxide and the generation of electron-hole pairs from electronic losses in the oxide.

2.3 MOS Modes of Operation: C-V behavior

MOS capacitance–voltage (C-V) measurements and analysis are standard techniques to study MOS behavior. To measure capacitance of an MOS device, an AC voltage is superimposed on the DC voltage applied to the gate, and the response is usually measured with a vector ammeter and a vector voltmeter which determine both the magnitude and the phase of the current through the MOS capacitor and the voltage across it, respectively, as shown in figure 2.7 (a). The capacitance is then extracted from the impedance Z=V/I or the conductance G=I/V. In general, the charges in the MOS structure cannot respond as quickly as the changing voltage and the capacitance will depend on the frequency of the applied AC signal.

There will be three modes of operation depending on the biasing and response of the silicon surface: accumulation, depletion and inversion as shown in figure 2.8 (b). When a negative gate biasing greater than the flatband voltage ($|V_g| \rangle |V_{FB}|$) is applied in a p-type MOS, then it attracts the positive charge at the Si/SiO_2 interface and the device is in accumulation mode and the capacitance reaches the maximum value as shown in figure 2.7 (b). When we keep on reducing the negative gate bias voltage, for $|V_g| \langle |V_{FB}|$ the capacitance starts dropping and reaches its minimum value. If we further apply positive gate bias, then the device will reach in inversion and the capacitance depends on the frequency of the applied signal. For high frequency it will remain at its minimum value but for low frequency the capacitance will start rising as generated

minority carries with respond to low frequency signal and the total capacitance reaches its maximum value as shown in figure 2.7 (b).

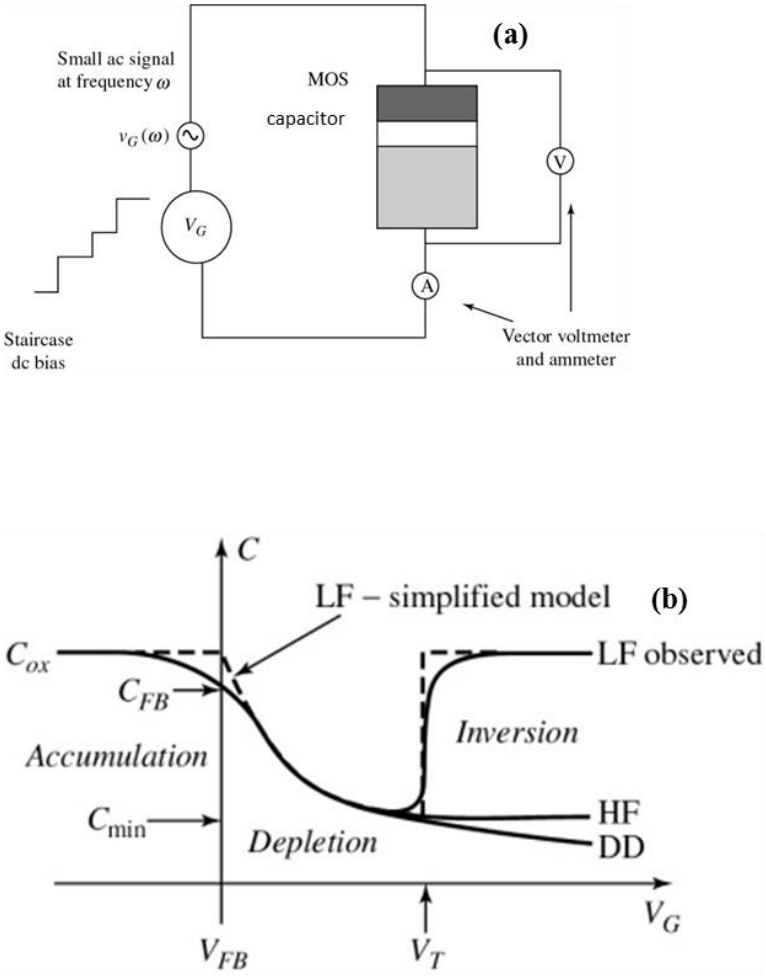


Figure 2.7: a) MOS C-V measurement system b) Plot of capacitance(C) vs. gate voltage (V_G) of a typical MOS capacitor measured at low(LF) and high frequency(HF) [33].

2.3.1 Accumulation

As shown in figure 2.7(b) starting from a negative gate voltage, the first region of the C-V curve is called accumulation. When we apply a negative gate bias, greater in magnitude than the flatband voltage (p-type Si), then the majority carrier holes will be attracted to the silicon surface and the silicon bands bend up near the Si/SiO_2 interface as shown in figure 2.8(a). The MOS capacitor starts storing positive charges inside the silicon accumulation layer near to the Si/SiO_2 interface such that hole density is greater than the acceptor density, N_a. The region at the silicon surface having increased hole density is called the accumulation layer. The surface is electrically connected (p^{++}-p) to the bulk p-type silicon and the charge distribution is illustrated in Figure 2.8(b) for case of zero oxide charge.

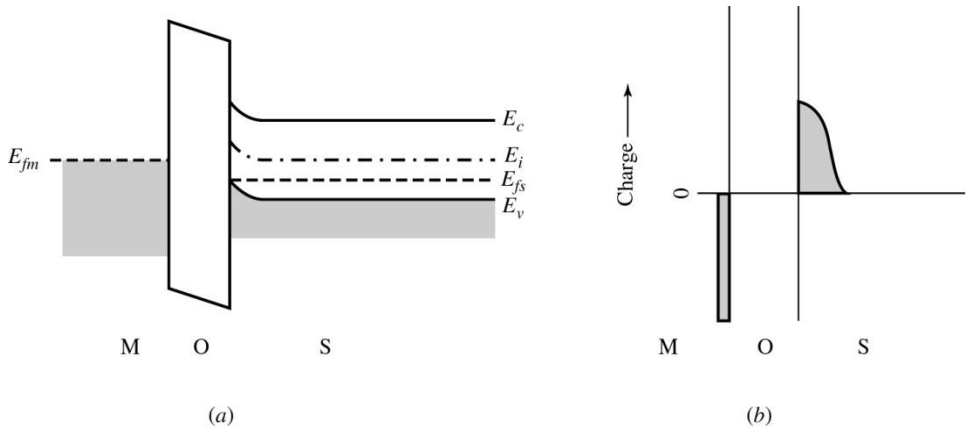


Figure 2.8: a) Energy-band diagram of an MOS system with p-type Silicon in accumulation region, b) corresponding charge density distribution[33].

For a very thin accumulation layer, which occurs when in strong accumulation, the capacitance is just that of the SiO_2 layer.

$$C'_{ox} \approx \frac{\varepsilon_o \varepsilon_{ox}}{x_{ox}} \text{ [F/cm}^2\text{]} \tag{2.12}$$

where C'_{ox} is capacitance per unit area (accumulation capacitance/device area) and x_{ox} is the oxide thickness.

From high frequency C-V measurements, we can find the oxide capacitance, C_{ox}, by measuring the capacitance in the accumulation region, and hence, we can calculate x_{ox}, the thickness of the oxide from equation 2.12.

2.3.2 Depletion

When we apply a negative gate bias such that $|V_g| < |V_{FB}|$, holes will be repelled from the p-type silicon and the region near to Si/SiO_2 called depletion region will be depleted of the holes. It has depletion width, x_d, which varies with gate voltage The concentration of the majority carrier holes will decrease in this region and hence the silicon bands bend down near the Si/SiO_2 interface making it less p type as shown in figure 2.9(a). The corresponding charge configuration for the depletion condition is shown in figure 2.9(b). The negative charge in the silicon consists of uncompensated acceptors (uncompensated acceptors) in a region depleted of holes. The total capacitance per unit area of the device will be a series combination of oxide capacitance per unit area, C'_{ox} and the silicon capacitance per unit area, $C'_s = \frac{\varepsilon_o \varepsilon_s}{x_d}$ where ε_s is the dielectric constant of silicon which is given by following equation

$$C'_T = \frac{C'_s \times C'_{ox}}{C'_s + C'_{ox}} \tag{2.13}$$

The depletion width, x_d, reaches its maximum width at a gate voltage called the threshold voltage, V_T, such that $V_g \langle V_T$ and silicon capacitance reaches its minimum value, $C'_{s_{\min}} = \frac{\varepsilon_o \varepsilon_s}{x_{d_{\max}}}$. Therefore the total capacitance per unit area, $C'_{T_{\min}}$ will reach its minimum value at maximum depletion width, given by

$$C'_{T_{\min}} = \frac{C'_{s_{\min}} \times C'_{ox}}{C'_{s_{\min}} + C'_{ox}} \tag{2.14}$$

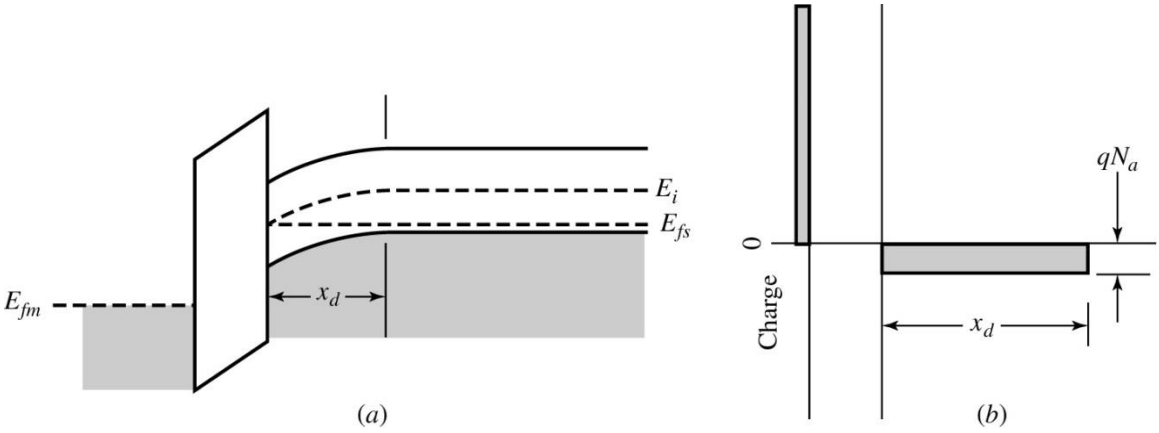


Figure 2.9 a) Energy-band diagram of an MOS system with p-type silicon in depletion region b) corresponding charge[33]

2.3.3 Inversion

When we further increase the positive bias on the gate beyond the depletion condition, the holes are repelled from the silicon surface and the electron density must increase to conserve the p-n (number of holes-number of electrons) product constant. The energy bands bend considerably as shown in figure 2.10 (a). The generation rate of the

carriers (mobile charge) exceeds the recombination rate and the generated electron-hole pairs are separated by the field. The holes will be swept to the silicon bulk and the electrons move to the oxide/silicon interface where they are confined by the SiO_2 layer. These generated electrons then form a thin inversion layer (Q_n) located near the Si/SiO_2 interface as shown in figure 2.10(b). Below the inversion layer the depletion layer still exits and below the depletion layer is the neutral silicon[32]. If we increase the gate biasing more, then gate charge is balanced by addition of electrons to the inversion layer. When the frequency of the AC signal is low (below 10 Hz) then these generated electrons can follow the AC signal and the capacitance in inversion rises to its maximum value as shown in figure 2.7(b) for the low frequency(LF) case. If the frequency of the measuring AC signal is high, then the inversion charge cannot follow the AC signal and the silicon capacitance remains the minimum as the depletion layer has reached its maximum value and the total capacitance is the series combination of the oxide capacitance and silicon capacitance. This case is shown in figure 2.7(b) as the high frequency (HF) case.

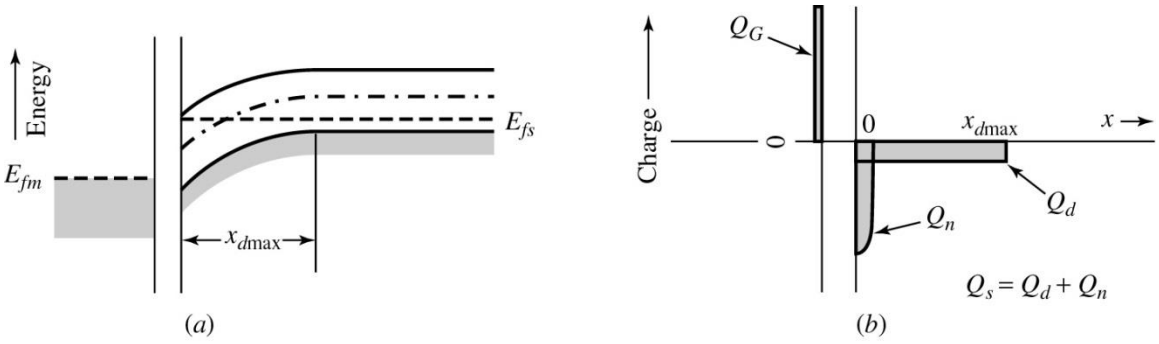


Figure 2.10 a) Energy-band diagram of an MOS system with p-type silicon in inversion region b) corresponding charge[33]

Chapter 3

Ion Irradiation and MOS Encapsulation of SiO_2

3.1 Overview

Experimental measurements of the effects of low energy ion irradiation on insulating solids can be challenging to interpret as the primary probe, atomic force microscopy, is a top-layer specific technique. In the work described here, we demonstrate that irradiation effects from ions can be probed after an insulator is encapsulated into a finished metal-oxide semiconductor (MOS) device. Specifically, by measuring capacitance-voltage (C-V) of the MOS structure we can resolve the residue of energy-dependent electron-hole pair excitations induced by the passage of ions into the subsurface of the previously exposed insulator.

In previous work on encapsulation of irradiation effects, it was shown that crater formation on a thin film dielectric (Al_2O_3) can be probed in a metal-insulator-metal (MIM) device[35]. Each device was probed using differential conductance measurements through films that had been exposed to highly charged ions, and the conductance change per ion impact was interpreted as a single ion effect dependent on charge state. In this chapter we focus on singly-charged ions which are embedded near the surface of an oxide film. The unique sensitivity of an MOS device to interstitial ions and trapped charge effects through C-V measurements[32] is then exploited to explore how the kinetic energy of the stopped ions was dissipated. Studies of the dependence of MOS device

performance on radiation damage have a long history[22,23,25,27,31] in the context of applied device physics given their relevance to fabrication-induced effects [7-10,29,30], such as those arising from the passage of dopant ions through the oxide and bound for the underlying semiconductor substrate. To understand these effects as well as those arising in deployed MOS devices, i.e. devices in harsh radiation-intensive environments, numerous investigations have employed intentional sources of radiation damage, such as gamma rays[22,23], high energy ions[23,25,27,31], and UV sources[11]. It is from these experiments that a detailed picture was developed for oxide radiation damage in MOS structures which incorporated data on depth, time, and voltage-dependent observations.

In the context of applied devices, the transition of MOS and MOSFET structures to ever thinner oxides has diminished the role that radiation damage plays in state-of-the-art device performance[31] (and references therein). In contrast, for the work we present here, we intentionally utilize thicker oxide layers to show that their inherent sensitivity to radiation damage allows ions with shallow implantation depths to give rise to significantly shifted C-V signatures that are linked to inelastic energy losses within the oxide.

3.2 Experiment

3.2.1 Fabrication

Our MOS devices were fabricated in-house at Clemson University. The starting materials were 3-inch p-type Si [100] wafers purchased from Silica-Source, Inc. The wafers, which had resistivities of 1-10 ohm-cm, were pre-cleaned to remove organic surface contaminants prior to oxide growth. The cleaning procedure was a standard RCA clean (1:1:5 solution of NH_4OH + H_2O_2 +H_2O) for five minutes under ultrasonic agitation. The cleaned surface was then etched with dilute 1% HF for two minutes to remove any native oxide followed by a triple rinse in deionized water for a total of six minutes. Oxide was grown on the samples by placing them in an oxidation furnace for 25 minutes at 1000 °C under a steam flow. The thickness of the oxide was measured with a NanoSpec AFT (Automatic Film Thickness) made by Nanometrics which gave a nominal value of 1900 Å (1887 Å ± 43 Å). To make Ohmic contacts, the wafer backside is etched with dilute 1% HF to remove native oxide followed by a deposition of 0.5 µm of Al from a thermal evaporator. The as-deposited Al contacts were sintered at 450 °C for 30 mins. in a nitrogen environment. Finally, the wafers were diced into 12 mm x 12 mm squares to accommodate the sample mount for our ion irradiation setup.

3.2.2 Beam line

A schematic of Clemson University's Surface and Interface Nanoscience group's beamline is shown in figure 3.1 (a) and is described in detail in Ref.[36]. The beamline design, which is based on an ion source with a planar emitting surface, is described by Peale *et al*.[37] and is shown in figure 3.1(b). The source uses a commercially available

ion emitter (HeatWave Inc.). The emitter consists of a heater cavity which is completely isolated from porous plug. The almuniosilicates, which are known to be best ion emitters, have been fused on the emitter surface in controlled amounts. A fine wire grid (stainless steel mesh of 1 mil wire on 10 mil centers) is separated (1-2 mm) from the emitter surface. The grid is nearly planar and it extracts a planar beam of uniform current density from the emitter surface. The ion emitter surface is held at the beam voltage with respect to ground. For extracting the beam, the grid and confinement electrode are biased few volts (15 V) below the beam accelerating voltage volts (using an external dc radio battery). By adjusting the grid biasing voltage, we can control the beam current independent of the beam energy which also enables us to correct the beam current due to change in emitter emissivity due to aging or temperature changes. The alkali ion source slips into the heat sink of our Colutron source [36] where the grid and confinement electrode makes contact with the heat sink at the mounting flange. The accelerating electrode is insulated from the confinement electrode but is pressed to make electrical contact with the first element of the einzel lens with the help of spring loaded support rods. The beam generated from the extraction stage is accelerated to its final energy in the second stage and focused using an einzel lens and then mass selected using the Wein filter into a Faraday cup mounted after the sample irradiation stage.

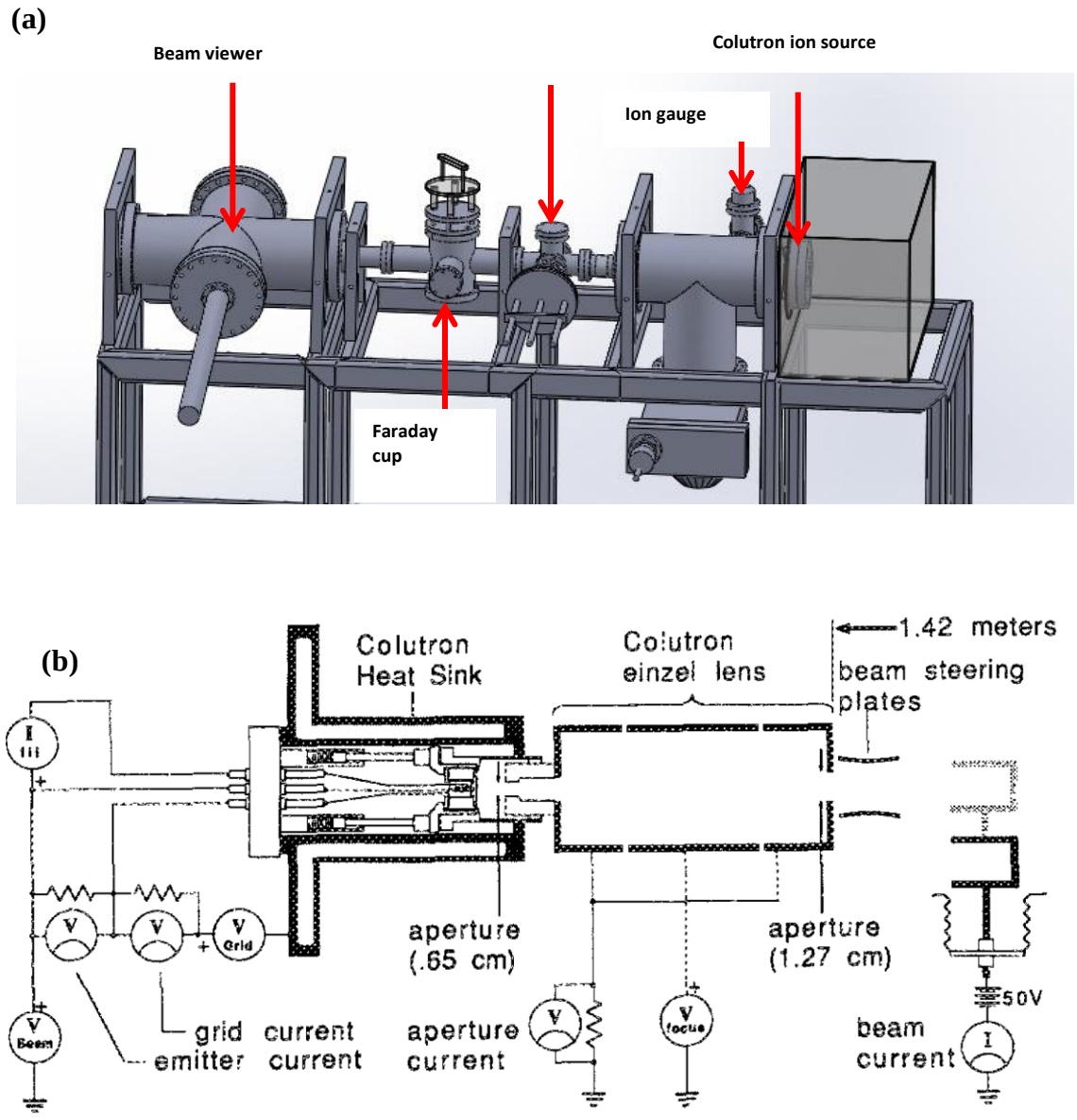


Figure 3.1: a) Schematic of beam line. The sample is mounted on a transferable plate which can be moved into the beam path using a linear manipulator. b) ion source optics and its associated circuitry from [37].

3.2.3 Irradiation Mask

The plate holding each target was masked so that only a central circular region (6 mm diameter) would be exposed to the incident ions as shown in figure 3.2 (a) and (b). Prior to each irradiation, an initial beam tuning was obtained by focusing the beam through an aperture as shown in figure 3.2 (b), which was equivalent in size to the central irradiating aperture as shown in figure 3.2 (a), and into the Faraday cup mounted directly behind the sample position as shown in figure 3.1(a) . To study the profile of the focused beam, a beam viewer was placed after the Faraday cup and was translated in the plane perpendicular to the beam. The focused beam was passed through the same aperture through which the irradiations were made and images of the focused beams were obtained. An example of one such image of the ion beam is shown in figure 3.2(c).The beam image has a circular shape because it passes through a circular aperture used for the irradiation, and the intensity of the beam has a Gaussian profile as shown in figure 3.2(d).

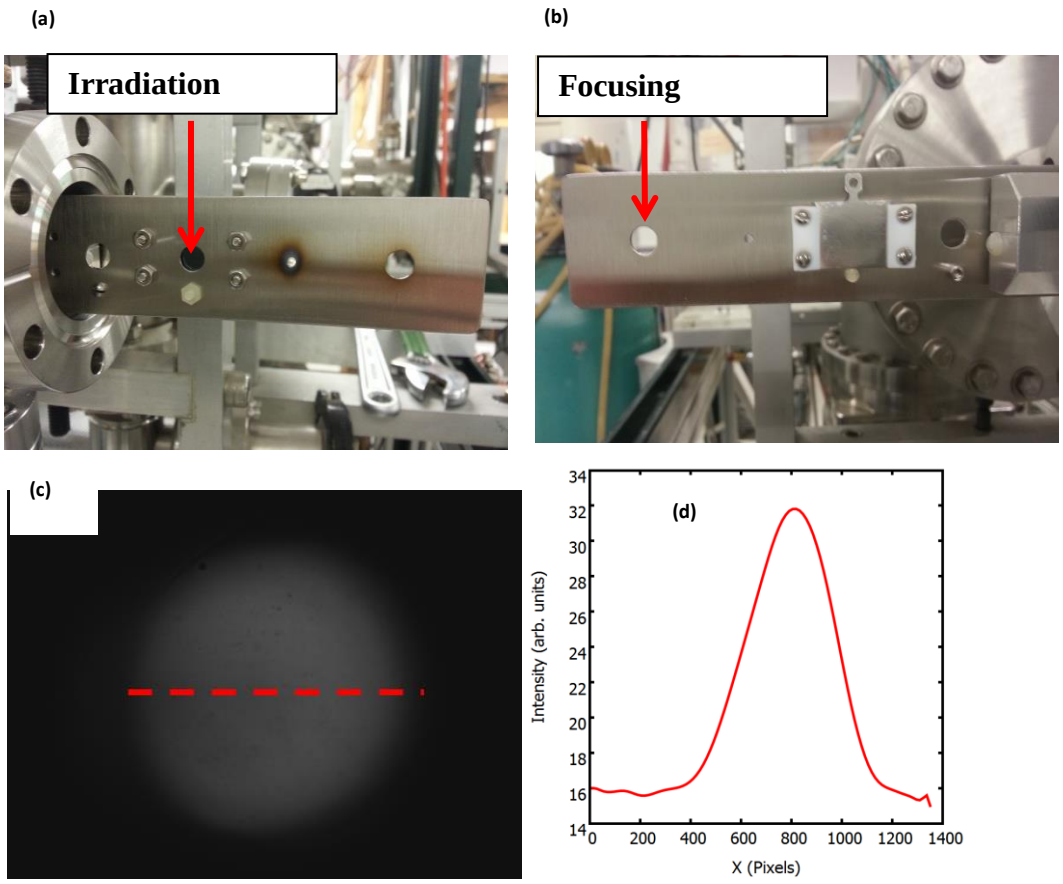


Figure 3.2 (a) Irradiation mask front (b) Irradiation mask back (c) Image of a Na^+ beam with 1 keV kinetic energy with the beam viewer d) central intensity profile of the beam image in (c) taken at the position of the dashed line shown in (c).

The base pressure within the beamline during irradiations was on the order of 5×10^{-7} Torr as measured by an active ion gauge as shown in figure 3.1 (a). After each irradiation, the target was removed from the beamline so that MOS top contacts of Al could be deposited. For these depositions, a custom-built mask shown in figure 3.2 (a) and (b) was used which placed four Al top contacts in the central, irradiated region and four Al top contacts in the corner, unirradiated regions of the target. Figure 3.3 (c) and (d)

show eight such MOS devices fabricated per target (4 irradiation-encapsulated and 4 pristine).Both pristine and irradiated devices were characterized using C-V measurements.

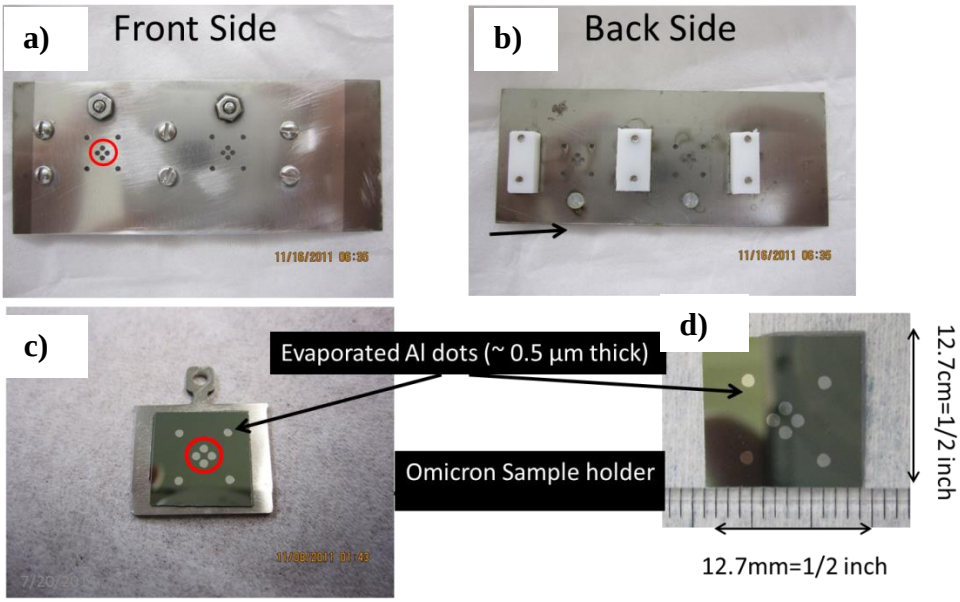


Figure 3.3 (a) Deposition mask front side (b Deposition mask back side (c) MOS capacitors fabricated by thermal evaporation of aluminum contacts having 0.5 µm thickness and 1 mm diameter on a diced wafer of Si/SiO_2 mounted on an Omicron sample holder d) image of (c) with scale.

3.2.4 Ion Dose

Ion dose are calculated as follows. The sample plate has two apertures of ¼" inch diameter: first for tuning the beam and second for the irradiation of the unfinished MOS capacitors. The beam current passing through the first aperture is measured using the Faraday cup as I_{FC} and A is the area of ¼" inch aperture. Then the dose is calculated as

$$Dose(\#/cm^2) = \frac{I_{FC}t}{eA}$$

where t is the time of irradiation in seconds. For our experiments, the current through the aperture is on the order of 5 nA so that an irradiation time, t, of 60 seconds will give a dose of 5.9×10^{12} cm^{-2}.

3.2.5 C-V Measurement Setup

A Micromanipulator probe station connected to a HP4280A for high frequency (HF) measurements and a HP4140B for low frequency (LF) measurements was used to obtain the C-V characteristics of the MOS capacitors. The sample was loaded on the chuck of the micromanipulator, and a vacuum pump was used to create suction to hold the sample tightly to the chuck so that the aluminum Ohmic contacts on the backside of the sample could make electrical contact (Lo connection) through the chuck. A probe tip mounted on a manipulator was used to make the connection to the top Aluminum contact (Hi connection) as shown in Figure 3.4.

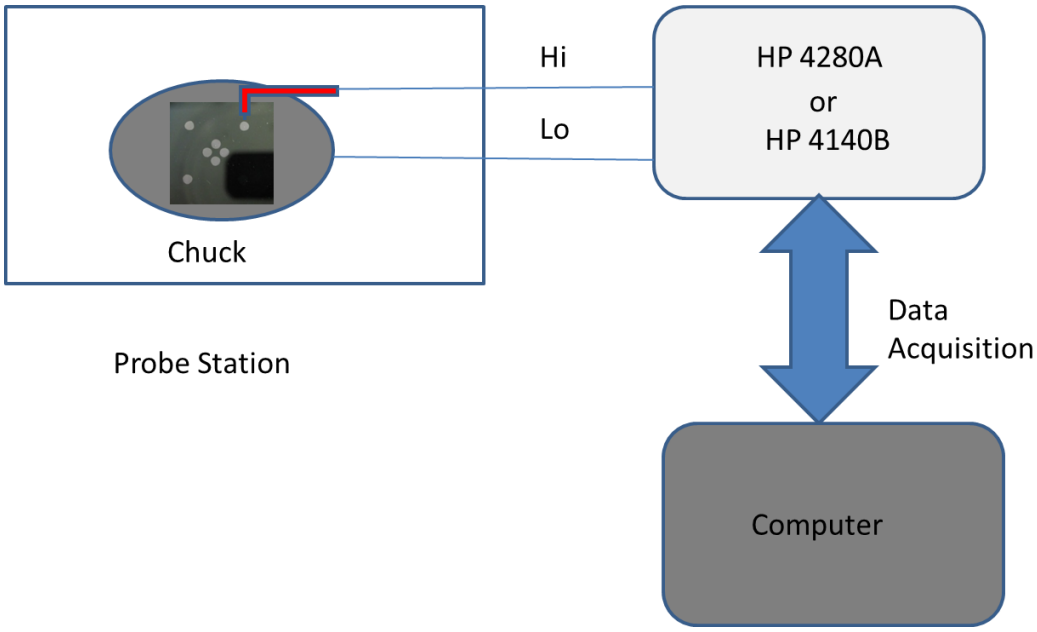


Figure 3.4: Schematic of C-V meaurement system using HP 4280A/ HP 4140B and data was taken by connecting a HPIB-USB controller between HP 4280A / HP 4140B and a computer.

Both pristine and irradiated devices were characterized using C-V measurements. Typical low frequency (LF) and high frequency (HF) signatures of a pristine MOS capacitor are shown in Fig. 3.5 (b) for one of our unirradiated devices. As a function of the applied gate voltage, both the LF and HF C-V curves show accumulation behavior at the most negative applied voltages and hence give similar capacitance values due to the intrinsic capacitance of the 1900 Å oxide layer. For the LF C-V this result is mirrored at the most positive applied gate voltage where the MOS device goes into inversion, whereas the HF C-V is lower due to the capacitance of the depletion layer. Between these two extremes, both C-V curves show a distinct drop beginning at a point in voltage that is near to the so-called flatband voltage (V_{FB}) where, for an ideal system, the applied gate

voltage equals the difference in work functions between the Al gate and the Si substrate (0.8 eV) as discussed in chapter 2 section 2.3. More generally, however, V_{FB} can be considered as sensitive to the detailed conditions of the oxide and its interfaces and, in particular, to implanted charged species and any additional charges, such as excited holes, left by irradiation. For example, the 3 keV Na^+ irradiated device in Fig. 3.5 (c) shows a significant shift in the V_{FB} position. Therefore, it is through V_{FB} that we track the energetics of kinetic energy dissipation for the Na^+ ions which have irradiated the MOS oxide layer.

3.3 Data

For this study, we irradiated our as-prepared SiO_2 (~1900 Å) targets with beams of Na^+ ions that had energies between 1 keV and 5 keV. All target doses were in the range of 6-8 x 10^{12} ions/cm^2. Following each irradiation, Al top contacts were deposited as noted above and the finished MOS devices were characterized by C-V measurements. Representative C-V data for an unirradiated device and for four devices in the irradiated energy range are shown in figures 3.6 to 3.11. It is clear from these spectra that there is a significant shift in the position of the flatband toward more negative gate voltage values as the incident beam energy is increased.

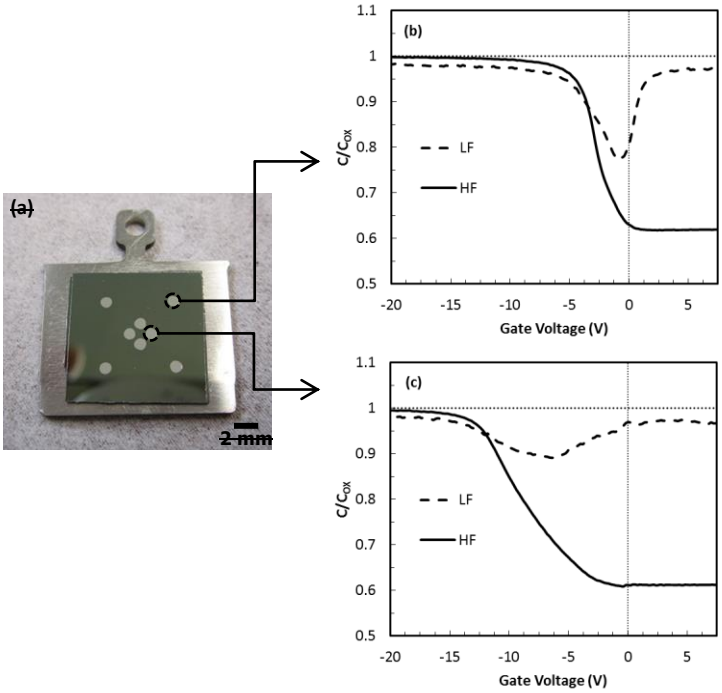


Figure 3.5 (a) A diced, oxidized Si sample mounted on an Omicron-style sample holder showing four central (irradiated) and four corner (unirradiated) MOS devices. (b) High frequency (HF) and low frequency (LF) capacitance-voltage (C-V) curves for an unirradiated device. (c) HF and LF C-V curves for a device encapsulating an oxide layer irradiated by 3 keV Na^+ ions. Note: The capacitance values in both (b) and (c) have been normalized by the oxide capacitance, C_{OX}.

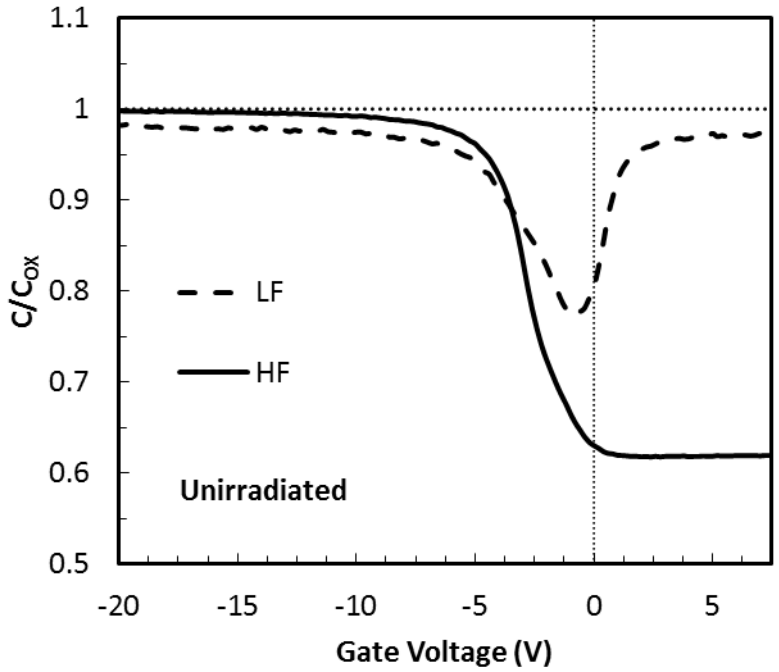


Figure 3.6: High frequency (HF) and low frequency (LF) capacitance-voltage (CV) curves for an unirradiated device. The capacitance values have been normalized by the oxide capacitance, C_{OX}.

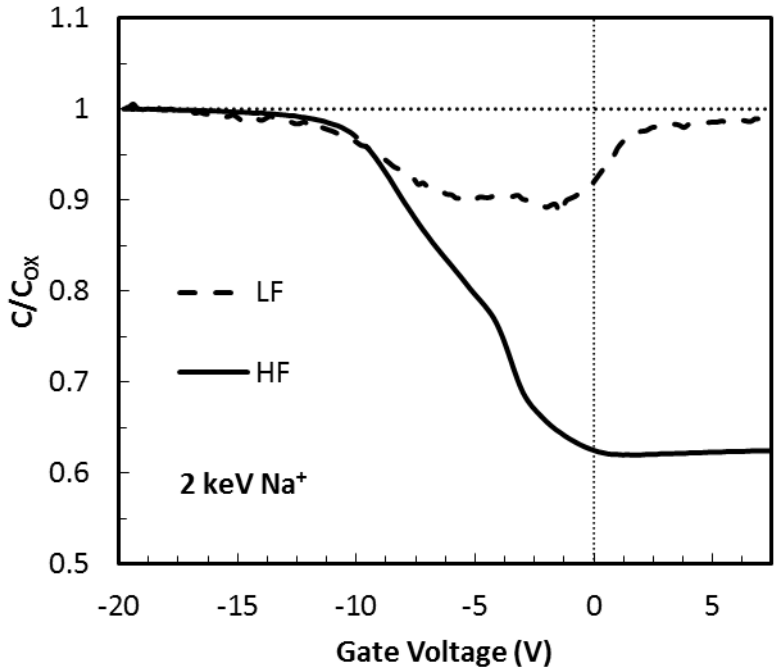


Figure 3.7: HF and LF C-V curves for a device encapsulating an oxide layer irradiated by 2 keV Na^+ ions. Note: The capacitance values have been normalized by the oxide capacitance, C_{OX}.

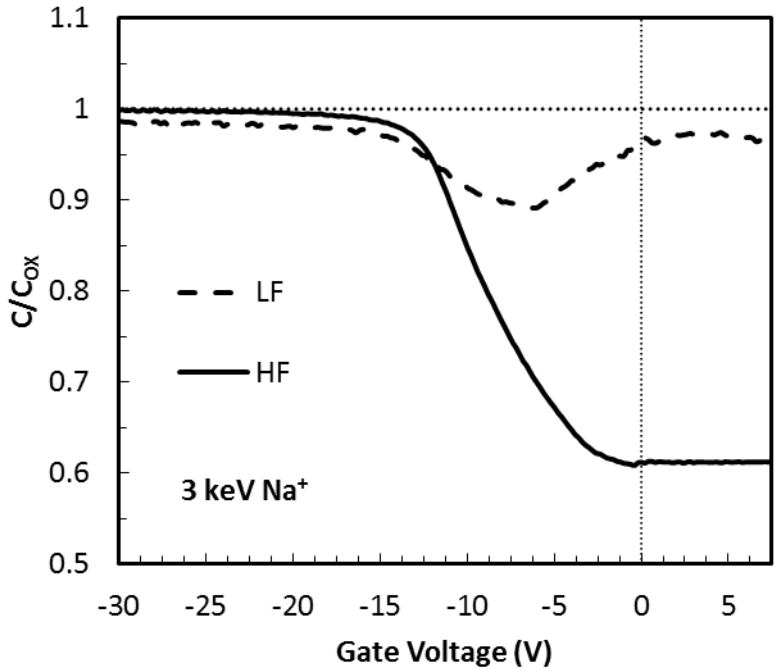


Figure 3.8: HF and LF C-V curves for a device encapsulating an oxide layer irradiated by 3 keV Na^+ ions. Note: The capacitance values have been normalized by the oxide capacitance, C_{OX}.

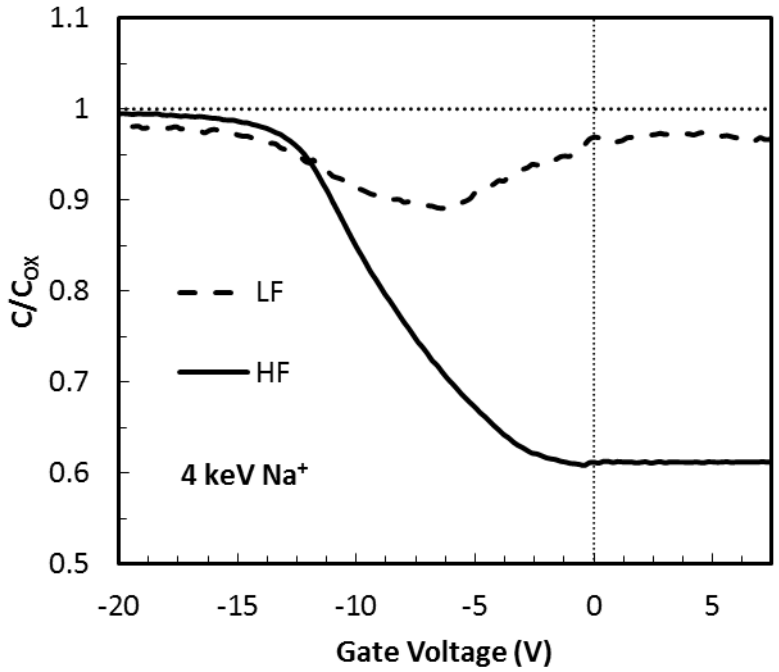


Figure 3.9: HF and LF C-V curves for a device encapsulating an oxide layer irradiated by 4 keV Na^+ ions. Note: The capacitance values have been normalized by the oxide capacitance, C_{OX}.

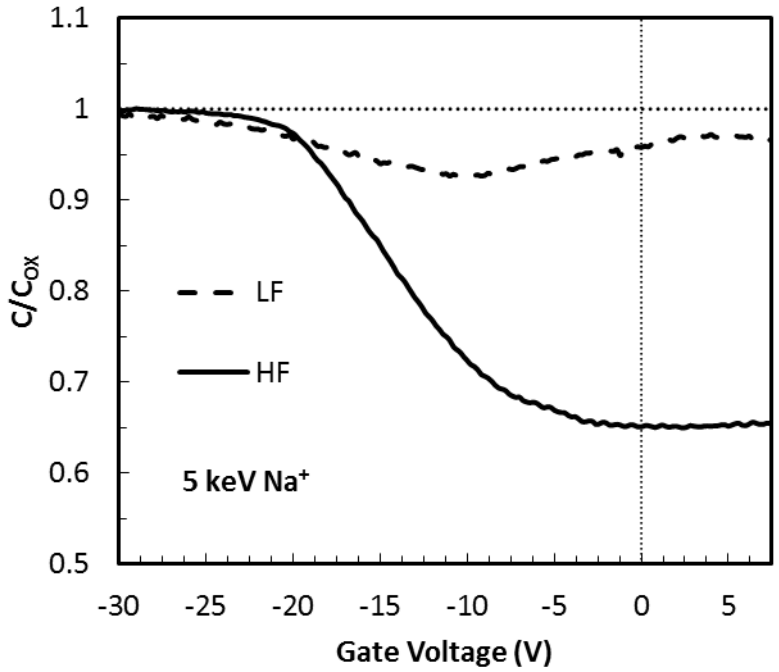


Figure 3.10: HF and LF C-V curves for a device encapsulating an oxide layer irradiated by 5 keV Na^+ ions. Note: The capacitance values have been normalized by the oxide capacitance, C_{OX}.

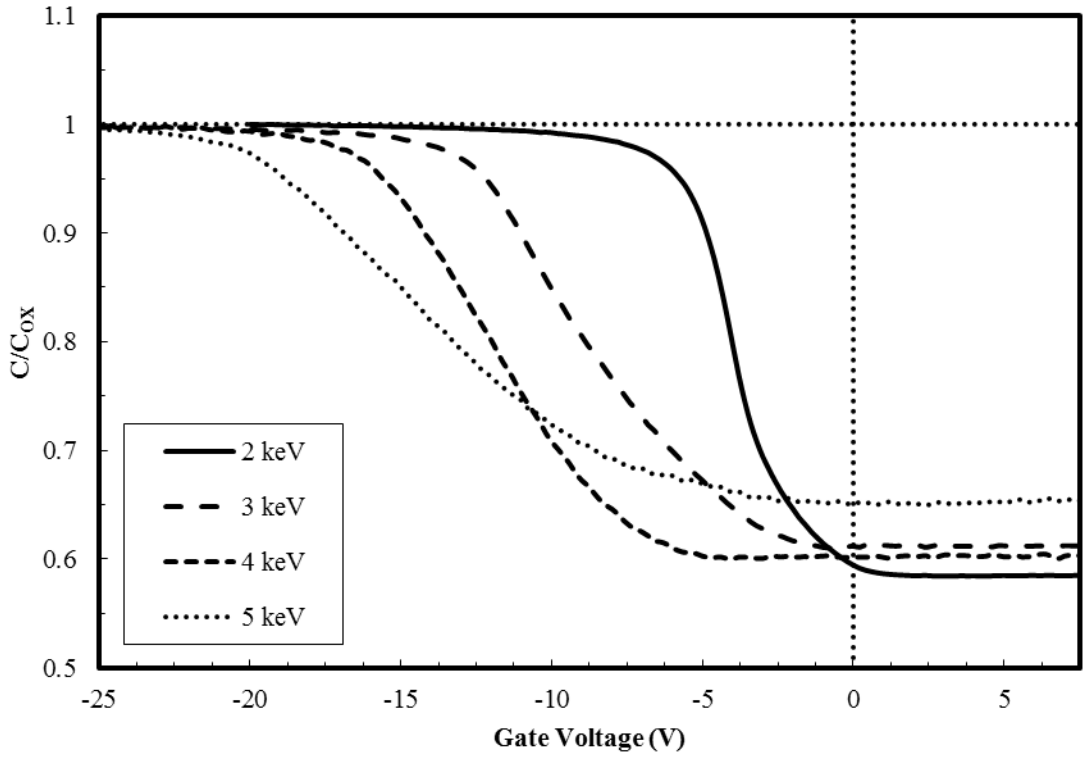


Figure 3.11: Irradiated device CV curves (HF) for devices exposed to Na^+ ions in the range of 2 keV to 5 keV. The capacitance values have been normalized by the oxide capacitance, C_{OX}.

3.4 Analysis

3.4.1. Calculation of Flatband Voltage

Flatband capacitance is useful for comparing C-V curves and it is also a universally accepted reference point on the C-V curve[32]. The flatband voltage is defined in chapter 2 section 2.3 as the condition at which the energy bands in the silicon are flat near the surface and in the bulk. At flatband condition, oxide capacitance, $C_{ox,}$ is in series with the silicon flatband capacitance, $C_{FBS,}$ and the total capacitance is given by

$$\frac{1}{C'_{FB}} = \frac{1}{C'_{ox}} + \frac{1}{C'_{FBS}} \tag{3.1}$$

where C'_{FB} is flatband capacitance per unit area , C'_{ox} is oxide capacitance per unit area and C'_{FBS} is silicon flatband capacitance per unit area. Rearranging the terms, we get flatband capacitance per unit area, C'_{FB}, as

$$C'_{FB} = \frac{C'_{FBS}.C'_{ox}}{C'_{FBS} + C'_{ox}} \tag{3.2}$$

Rearranging equation 3.2, we get normalized flatband capacitance as

$$\frac{C'_{FB}}{C'_{ox}} = \frac{C'_{FBS}}{C'_{FBS} + C'_{ox}} \tag{3.3}$$

where the silicon flatband capacitance per unit area, C'_{FB}, is defined as

$$C'_{FBS} = \frac{\varepsilon_s}{\lambda_p} \tag{3.4}$$

In equation 3.4, ε_s is the permittivity of the silicon and λ_p is extrinsic Debye Length given by

$$\lambda_p = \left(\frac{kT}{q} \frac{\varepsilon_s}{qN_a} \right)^{1/2} \tag{3.5}$$

As described in the previous section, our p-type Si wafers have resistivity of 1-10 Ohm-cm which corresponds to $N_a \approx 10^{15} cm^{-3}$ to $N_a \approx 10^{16} cm^{-3}$, and we get a normalized flatband capacitance per unit area ranging from 0.814 to 0.933. Taking the average value of the doping concentration, $N_a = 5 \times 10^{16} cm^{-3}$, we get $\lambda_p = 57.81 nm$ and a normalized flatband capacitance per unit area, $C'_{FB} / C'_{ox} = 0.91$. Finally, we pick the normalized capacitance value corresponding to 0.91 in the C/C_{ox} vs. V curves and locate the voltages corresponding to this value on pristine and irradiated devices. The difference between these two voltages is the change in flatband voltage.

We obtain flatband voltages of 3.7 to 3.8 V for the pristine devices. In chapter 2, section 2.2.3 that we noted that in the case of an ideal MOS capacitor (no charges in the oxide) the flatband voltage is the difference of aluminum and silicon work functions, which is equal to 0.8 V for our systems. But, in reality, there are some charges in the SiO_2 and fixed charges at the Si/SiO_2 interface.

From equation 2.7, the change in flatband voltage for a uniform charge sheet at *x* is

$$\Delta V_{FB} = -\frac{Q'_{ox} \bullet x}{C'_{ox} \bullet x_{ox}}$$

If we assume a charge sheet at the Si/SiO_2 interface, for $x = x_{ox}$

$$\Delta V_{FB} = -\frac{Q'_{ox}}{C'_{ox}}$$

Therefore, $Q_{ox}^{'} = -\Delta V_{FB} \times C_{ox}^{'} = \frac{-(-3) \times 1.83 \times 10^{-8}}{1.602 \times 10^{-19}} = 3.43 \times 10^{-11} cm^{-2}$

Therefore, the net number of charges per unit area at the Si-SiO_2 interface is 3.43 x 10^{11} cm^{-2} which is acceptable in case of the thicker oxides [38].

By using above method, the flatband voltages, V_{FB} of the unirradiated (pristine) and irradiated MOS capacitors were found .The V_{FB} of the irradiated MOS capacitors showed higher negative values than the unirradiated MOS capacitors, which suggest the presence of net positive charge left in the oxide due to the irradiation of the oxide. The flatband voltage shift increased as the incident beam energy is increased, which can also be seen in figure 3.11.

3.4.2 Calculation of Contribution of Ions

As we already stated in section 2.5 of chapter 2, the calculation of the change in flatband voltage for an arbitrary oxide charge density, $\rho(x)$, is given by equation

$$\Delta V_{FB} = -\frac{1}{C_{ox}^{'}} \int_{0}^{x_{ox}} \frac{\rho(x) x dx}{x_{ox}} \tag{3.6}$$

We obtained the distribution of the ions in the oxide from the Stopping and Range of Ions in Matter(SRIM) [4], which gives us a Gaussian distribution with mean projected depth and straggling/standard deviation of the ions. An example of one such simulation is shown in the Figure 3.12. The y axis of the plot has units of (Atoms/cm^3)/ (Atoms/cm^2)

such that multiplying with the dose (ions) /cm^2 gives us a density distribution with units of (atoms/cm^3).

Therefore, charge density becomes

$$\rho(x) = \frac{\int_0^{x_{ox}} Dose \times e \times G(\mu,\sigma)\, dx}{\int_0^{x_{ox}} G(\mu,\sigma)\, dx} \tag{3.7}$$

where e is the elementary charge and $G(\mu,\sigma)$ is the Gaussian distribution obtained from SRIM [4] simulations having with a mean projected depth, μ, and standard deviation, σ, of the ions. Putting this value of the charge density in equation 3.6, we obtain the change in the flatband voltage due to ions as

$$V_{FB}(ions) = \frac{1}{C'_{ox}} \times \frac{\int_0^{x_{ox}} Dose \times e \times G(\mu,\sigma) \times x\, dx}{\int_0^{x_{ox}} x_{ox} \times G(\mu,\sigma)\, dx} \tag{3.8}$$

where $C'_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$, is the capacitance per unit area of the oxide.

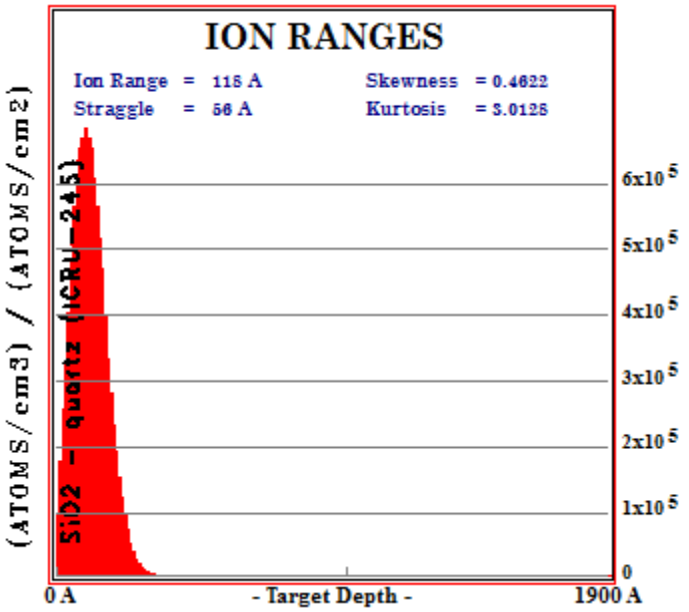


Figure 3.12: Ion range simulation of 5 keV Na^+ ions into 1900 Å SiO_2 from SRIM [38].

The flatband voltages, V_{FB} ,were found from the high frequency C-V curves of irradiated and pristine devices as described in previous section 3.4.1 and are shown in figure 3.13 as function of the kinetic energy of the incident Na^+ ions. The contributions of the Na^+ ions to the flatband voltage were found by the method as discussed above and are shown as "Calculated V_{FB} due to implanted ions" in figure 3.13. Figure 3.13 shows the flatband voltage of the irradiated devices linearly increases as a function of the kinetic energy of the incident ions, which indicates the linear energy loss of the incident ions as a function of their kinetic energy. This confirms that MOS devices are sensitive to the energy loss of the ions in the oxide and can be a viable method for finding the energy loss of ions in the low energy regime.

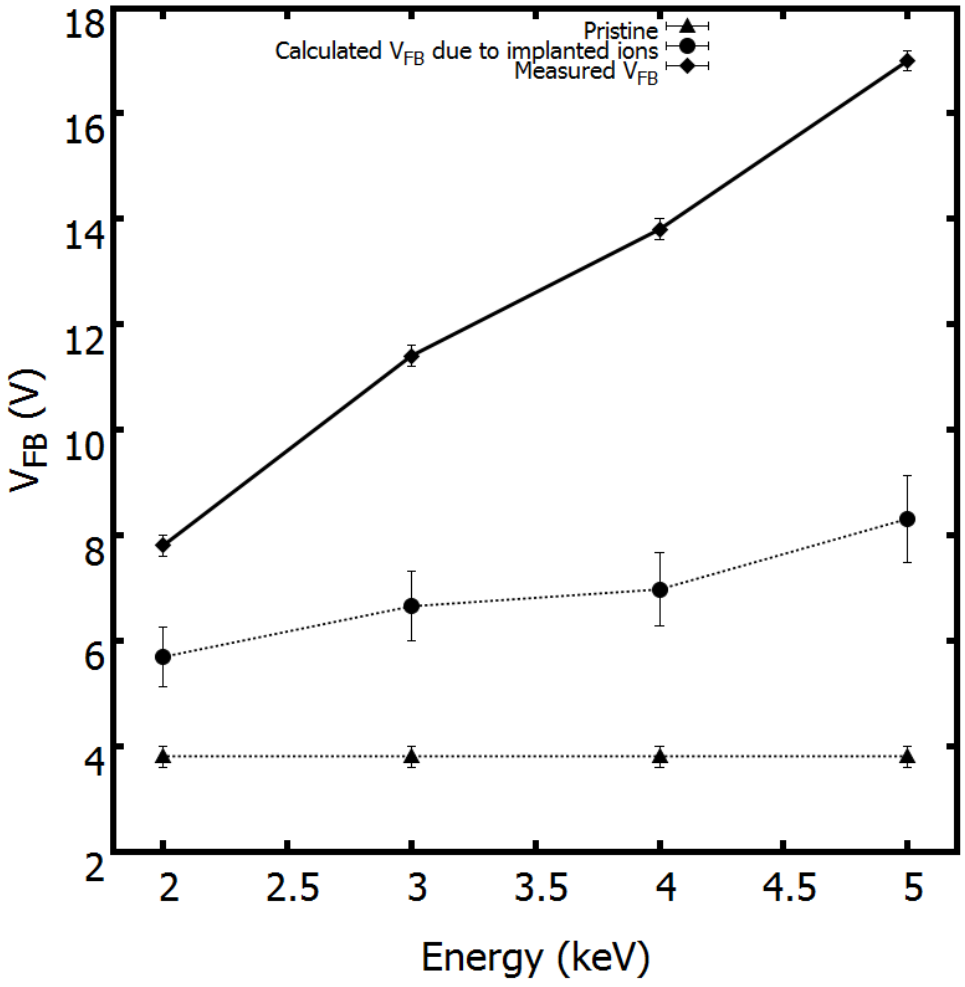


Figure 3.13 Measured flatband voltages for pristine and irradiated MOS devices, plotted with respect to the incident energy of the Na^+ ions. The expected contribution of the implanted Na^+ ions on the overall flatband is also plotted and was determined using the experimental ion dose and device area along with depth profiles obtained from SRIM as discussed above.

3.4.3 Calculation of number of holes escaping recombination

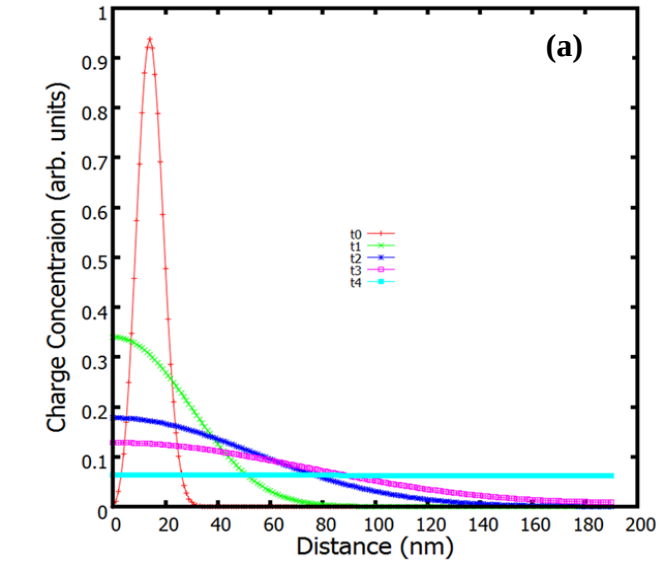
The ions lose their energy as they pass through the oxide. The energy lost by the ion per unit path length is defined as stopping power (*dE/dx*), which is also discussed in Chapter 1, section 1.1. It can be divided into two components: energy transferred by the ion to the target electrons referred to as electronic stopping or inelastic energy loss, and energy loss to target nuclei referred to as nuclear stopping or elastic energy loss. There is no correlation considered between the two energy loss mechanisms [3]. As already discussed in Chapter 1, section 1.3 and 1.4 and [25] (and references therein), the energy lost to the electronic system creates electron-hole pairs in the oxide. Some fraction of the created holes will recombine with electrons in the first picosecond or so, which depends upon the electric field and the type of radiation [25,27] (and references therein). The electrons recombine with holes according to two models: the Columnar model for electron-hole pairs that are close enough (order of 10 nm) or the Geminate model for electron-hole pairs that are far apart. The separation distance between the hole and its corresponding electron at thermal energy is called the thermalization distance and it is of the order of 5 or 10 nm [21]. The mean separation distance between electron-hole pair is inversely proportional to the stopping power of the ionizing radiation. In our case of 1-5 keV Na^+ ions, we have a stopping power of 26.54 to 41.97 eV/nm. Using the electron-hole creation energy of 18 eV[39], we get the electron-hole pair separation distance of the order of 1.47 nm to 2.33 nm, which is less than the thermalization distance of electron-hole pairs. Therefore, we consider the electron-hole pairs recombine according to the

Columnar recombination model given by Jeff and later numerically solved by Oldham [25,27,40](and references therein). It is represented as

$$\frac{\partial n_{\pm}}{\partial t} = D_{\pm}\nabla^2 n_{\pm} \mp \mu_{\pm} E \frac{\partial n_{\pm}}{\partial x} - \alpha n\_n_{+} \tag{3.9}$$

where $n_{\pm}$ represents the hole (+) or electron density (-).The terms on the right-hand side are (left to right), the diffusion term, the drift term and the recombination term. *D* represents the diffusion constant, μ is the mobility of carriers (μ_{-} =40 cm^2/V-s and μ_{+} =10^{-11} cm^2/V-s) in SiO_2, *E* is the applied/internal field and α is the recombination coefficient.

In calculating the evolution of $n_{\pm}$ for our system, we take the initial distribution of the ions as given by SRIM [4]. An example of such a distribution is shown is figure 3.12. The electron-hole pairs are produced when the ions lose energy into the SiO_2 and therefore the distribution of the holes will be similar to the ion distribution (Gaussian) given by SRIM[4]. However, the distribution will be biased by the distance the ions travel inside the oxide and more electron-hole pairs will be produced because of the increased linear energy loss. Two example distributions for the ions having 2 and 5 keV are shown in figure 3.14 (a). Numerically solving equation 3.9 for the initial distribution of 5 keV ions as shown in figure 3.14(a) at room temperature, we get the uniform distribution as shown in figure 3.14(b).



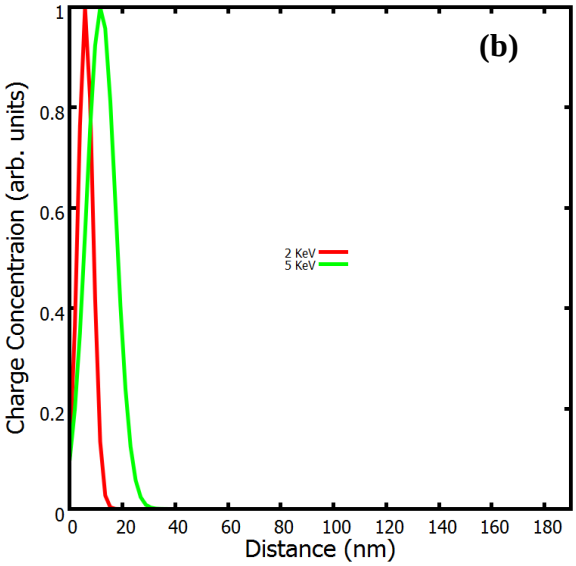


Figure 3.14 a): The initial distribution of the holes obtained from the experimental dose of the ions and SRIM electronic losses for 2 keV and 5 keV Na^+ ions into SiO_2 b) The distribution of the holes for 5 keV Na^+ ions at a later times and finally, the hole distribution is uniform across the oxide after a few ns.

We have taken the contribution from the first term of equation 3.9 only, which is the dominant term for our experiment as we are not applying an external electric field and the internal field due to the ions in the oxide is not strong. Additionally, the recombination term is only effective for the first few ns and will only reduce the initial number of holes. Therefore at room temperature, the remaining holes which escape from initial recombination will diffuse in the oxide and lead to a uniform distribution of the holes in the oxide as shown in figure 3.14 (b).

Experimentally, the number of the holes which escape recombination is determined from the change in the flatband voltage of the irradiated devices with respect to the pristine devices [25,27], i.e. $\Delta V_{FB} = V_{FB}(\text{Irradiated}) - V_{FB}(\text{Pristine})$. The flatband shift will be proportional to the uniform distribution of the holes which escaped recombination as discussed above and will be given as

$$\Delta V_{FB} = \frac{1}{C_{ox}} \times \int_0^{l_{ox}} \rho(x) \frac{x}{x_{ox}} dx \tag{3.10}$$

In the case of a uniform distribution of holes throughout the oxide, eq.3.9 reduces to

$$\Delta V_{FB} = \frac{Q}{2 \times C_{ox}} \tag{3.11}$$

and the change in the flatband voltage is attributable to the holes produced by the energy loss of the ions into the oxide.

To find the experimental number of holes, we rearrange the above equation (3.10) as

$$N_{H-EXPERIMENTAL} = \frac{2 \times \Delta V_{FB} \times C_{ox}}{e} \tag{3.12}$$

3.4.4 Calculation of predicted hole generation

Each ion passing through the oxide loses its energy into the oxide which creates electron-hole pairs[21]. The total number of holes generated are calculated from the experimental ion dose, the predicted Guassian distribution of implanted ions, and the ion electronic energy loss obtained from SRIM[4]. Using the fact that the energy required to produce an electron-hole pair in SiO_2 is 18 eV [25,27,39], we obtain

$$N_{H-SRIM} = \frac{Dose \times Area \times e \times dE/dx}{18} \times \frac{\int_0^{x_{ox}} G(\mu,\sigma) \times x \, dx}{\int_0^{x_{ox}} G(\mu,\sigma) dx} \tag{3.13}$$

where *Dose (#/cm^2)* is calculated from the beam current passing thru the focusing hole as discussed in the section 3.2.4 , *Area* is the device area (0.00899 cm^2) , dE/dx is the electronic loss (eV/Å) obtained from SRIM calculations, $G(\mu,\sigma)$ is the Gaussian distribution of holes obtained from SRIM and biased by *x* (linear energy loss of the ions) and x_{ox} is the oxide thickness.

3.4.5 Fractional Yield of the holes escaping recombination

The fractional yield of the holes which survived the initial recombination is given by [25,27,40] as

$$f(E) = \frac{N_{H-EXPERIMENTAL}}{N_{H-SRIM}} \tag{3.14}$$

where $N_{H-EXPERIMENTAL}$ is the number of holes escaping recombination from equation (3.12) and N_{H-SRIM} is the predicted total number of holes generated obtained from equation (3.13) .

Figure 3.15 shows the data of $N_{H-EXPERIMENTAL}$ Vs. N_{H-SRIM} for different kinetic energies of the ions. A linear fit to the data of figure 3.15 gives a straight line and the slope of this line (0.0124) gives the fractional yield of the holes escaping recombination.

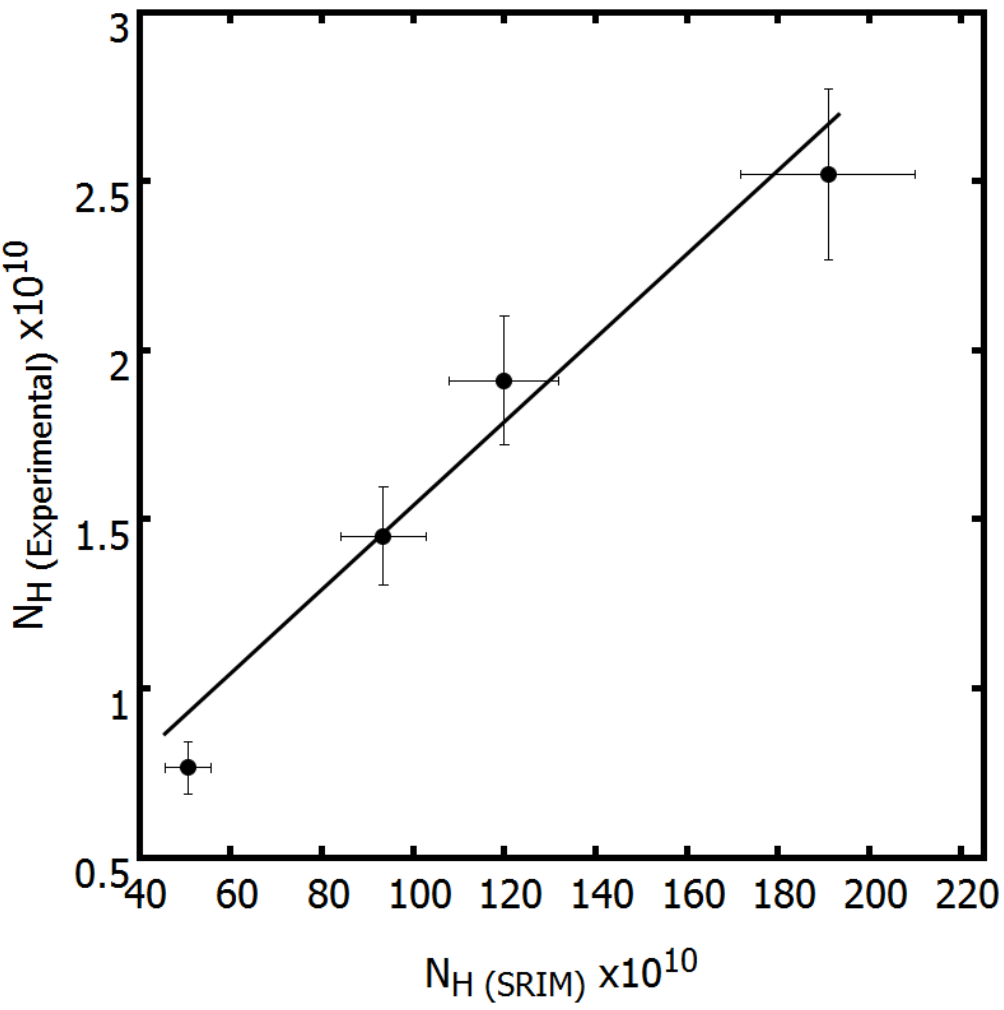


Figure 3.15: Number of "holes" determined experimentally from C-V flatband shifts versus the number of "holes" predicted using SRIM and expected ion energy loss.

3.4.6 Interface Trap Level Density

When silicon is thermally oxidized to make silicon dioxide, the interface between amorphous silicon dioxide and crystalline silicon is generally deficient of oxygen, giving rise to strained or dangling bonds which act as interface traps with energy levels in between the forbidden bandgap at the Si/SiO_2 interface[21]. They may be positive or negative charges, due to 1) structural, oxidation induced effects 2) metal impurities or 3) other defects caused by radiation or breaking of the bonds. They are in electrical communication with the underlying silicon[34].

Figures 3.6 to 3.10 show the HF and LF C-V curves for irradiated devices. We can see from these figures that the stretch-out of the C-V curves along the biasing axis (from accumulation to inversion) increases as we increase the kinetic energy of Na^+ ions, which implies that interface trap density increases as kinetic energy of the ions is increased. This stretch-out is due to the contribution of the interface traps to the capacitance, which can be calculated from the observed HF and C-V curves and is explained in the next section.

3.4.7 Measurement of Interface Trap Density

The interface trap level density was found by comparing the high frequency capacitance with low frequency capacitance. The interface traps change their charge state depending on whether they are filled or empty. The interface trap occupancy change is a function of gate biasing and therefore, stretch-out of C-V curves occurs and it is the only effect at high frequencies[32]. At low frequencies, interface traps respond to the AC

signal biasing and they will contribute an additional capacitance due to the interface, C_{it}. This equivalent circuit is shown below in the figure 3.14.

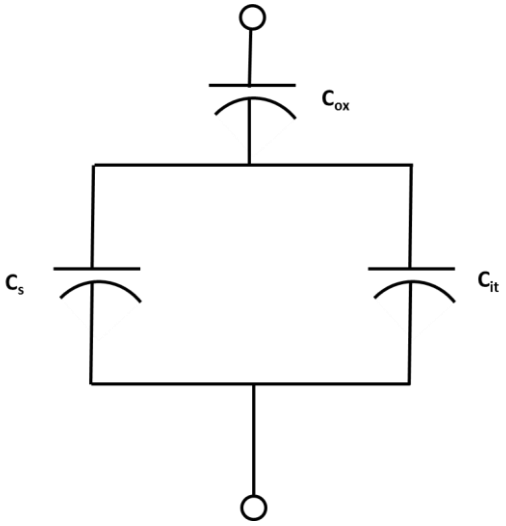


Figure 3.16: Low frequency equivalent circuit of the MOS capacitor[32].

We can see from figure 3.17, C_{it} is in parallel with the silicon capacitance, C_s and then their combined capacitance is in series with oxide capacitance, C_{ox} which can be shown as in the equation[32]

$$\frac{1}{C_{LF}} = \frac{1}{C_{OX}} + \frac{1}{C_S + C_{it}} \tag{3.15}$$

Solving the equation for C_{it}

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}} \right)^{-1} - C_S \tag{3.16}$$

where C_s is found from high frequency C-V data as explained below.

In the case of high frequency, the interface traps do not respond to the high frequency and equivalent circuit is shown in the figure below.

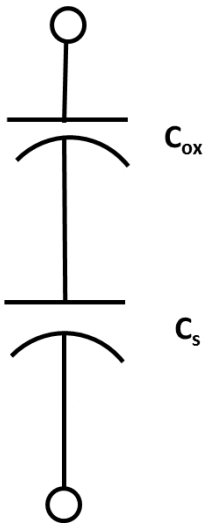


Figure 3.17: High frequency equivalent circuit of the MOS capacitor[32].

In figure 3.18, C_{ox} is in series with C_s and interface traps do not respond at high frequency and hence there is no capacitance due to interface traps. Therefore, we can write the high frequency capacitance as[32]

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{3.17}$$

Solving for C_s we get

$$C_s = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.18}$$

Substituting this value of C_s into equation 3.15, we finally obtain Cit explicitly as

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{Ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.19}$$

Hence, from low frequency and high frequency capacitance measurements, we can determine the capacitance due to interface traps, C_{it} .

For the case of slowly varying interface level densities, interface trap level density, D_{it} , is related to capacitance due to interface level traps, C_{it} , as[32]

$$D_{it} = \frac{C_{it}}{q} \tag{3.20}$$

where e is the elementary charge. Hence, the interface level densities were calculated from our measured low and high frequency measurements using equation 3.19 and 3.20. The results are shown in the figure 3.19 as a function of the ion energy.

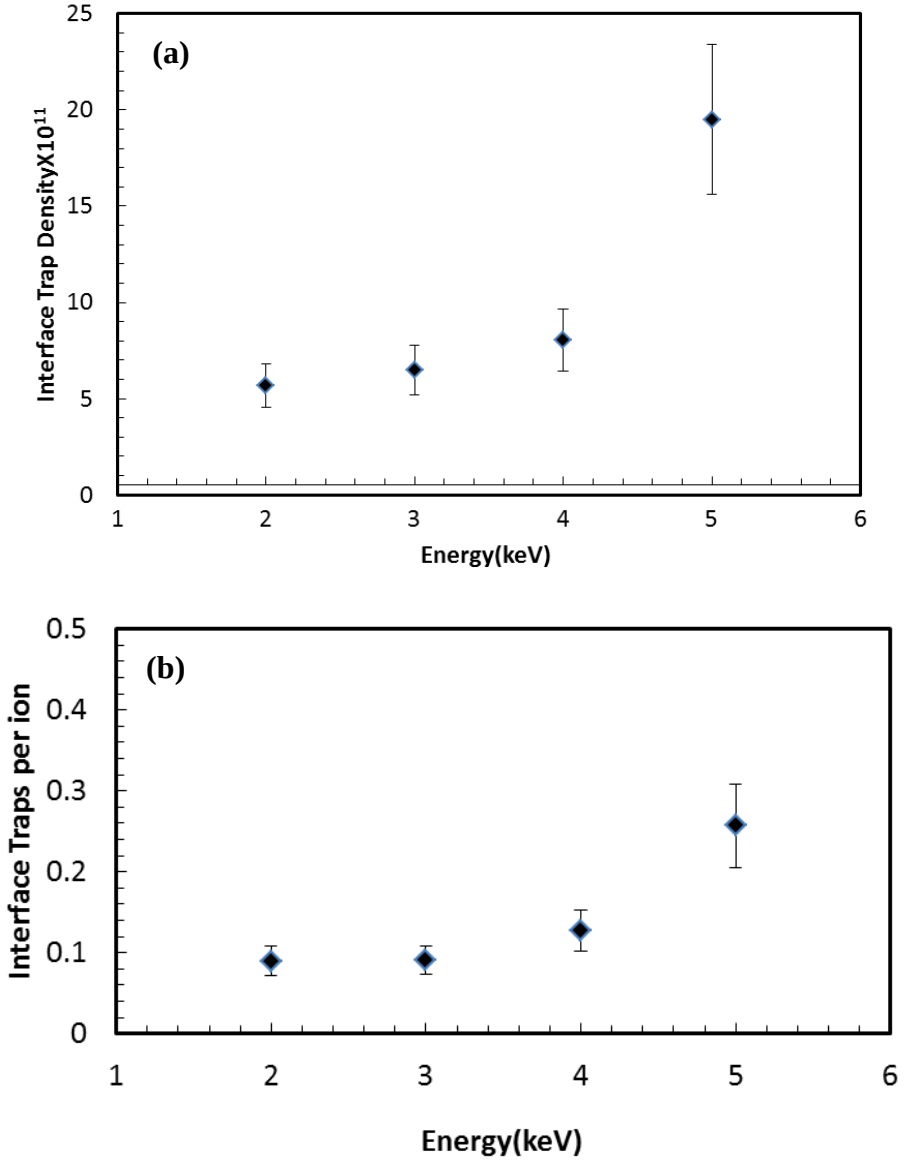


Figure 3.18: a) Interface trap density calculated from comparing of low frequency and high frequency C-V of irradiated and pristine capacitors as a function of the ions kinetic energy b) same quantity normalized by the ion dose.

3.5 Summary

In this chapter, I discussed the motivation for my experiments and compared them with the earlier work done by our group on MIM devices. Also I reviewed studies on irradiation of MOS capacitors and the unique sensitivity of the MOS oxide to irradiation produced charges. I also discussed the fabrication steps for our capacitors and gave an overview of our beamline and the design of the mask used for irradiation. The measurement setup for low frequency and high frequency C-V measurements was also presented along with the C-V data for irradiated oxides.

The C-V results were interpreted as radiation induced generation of holes which lead to flatband voltage shifts for irradiated capacitors as compared to pristine capacitors. The number of holes escaping initial recombination was calculated from the flatband voltage shifts and the ion range data from SRIM [4]. Also, the predicted total number of holes generated was obtained and compared with data to the fraction yield of the holes which escaped the initial recombination. These results confirm that dose- and kinetic energy -dependent effects can be recorded for singly charged ion irradiation on oxides using this method**.**

Chapter 4

Summary and Future Experiments

4.1 HCI Irradiation of MOS Devices

As a first experiment using extracted ions at CUEBIT, unfinished metal-oxide-semiconductor (MOS) devices were introduced into the target region and irradiated with Ar^{Q+} ions (Q=1,4,8 and 11). The goal was to explore whether charge-state dependent stopping effects could be resolved in capacitance-voltage (C-V) measurements. A wafer (3-in. p-type Si<100>) purchased from Silica-Source, Inc. with a resistivity in the 1-10 ohm-cm range was the starting material for these devices. The wafer was precleaned prior to oxide growth using a standard RCA clean (1:1:5 solution of NH_4OH + H_2O_2 +H_2O), etched with dilute 1% HF to remove any native oxide, and triple rinsed in deionized water. An oxide film was then grown on the wafer in an oxidation furnace under steam flow to a nominal thickness of 1750 Å (1746 Å ± 41 Å). A backside Ohmic contact was prepared on the wafer by HF etching the backside, depositing 0.5 μm of Al from a thermal evaporator onto the cleaned surface, and then sintering the wafer at 450 °C for 30 mins. in a nitrogen environment. The prepared oxidized wafer with Al backside contact was then diced into multiple square samples (~12 mm) to accommodate the Omicron-style sample mount of our ion irradiation setup.

For the irradiations, the samples were load-locked into the target region and exposed to focused beams of Ar^{Q+} ions (Q=1, 4, 8, and 11) that were all decelerated to have kinetic energies of approximately 1 keV. For the charge states Q=4, 8, and 11,

multiple samples were exposed at different total ion doses in the range of 5 x 10^{11} - 5 x 10^{12} ions/cm^2.

The dose of the ions is calculated as

$$Dose = f \times \frac{(I_{FC} + I_{FP})}{Qe} t$$

where I_{FC} is the faraday cup current, where I_{Fp} is the faraday faceplate current, Q is the charge state of the ion, e is the elementary charge, t is dosing time in seconds and f is the fraction of the total beam falling on the sample.

The base pressure within the target region during exposures was in the 10^{-8} mbar range. Following each irradiation, the exposed sample was removed and transported to a thermal evaporator so that ~1 mm diameter top Al contacts could be deposited to form multiple, individual MOS capacitors across the sample surface. An example is shown in Fig. 4.2(a) where 25 devices have been created on one sample. Each individual MOS device on a given sample was characterized using a C-V measurement. A typical high frequency C-V curve for an unirradiated MOS capacitor is shown as the dashed line and an irradiated device (1 keV Ar^{4+} ions) as the solid line in figure 4.1. The C-V curves were analyzed by the change in flatband voltage of the pristine and irradiated devices. This method to calculate the flatband voltage is explained in detail in Chapter 3 section 3.4.1.More generally, V_{FB} serves as a measure of the detailed conditions of the oxide and its interfaces. For the preliminary results discussed here, this applies to additional charges, such as excited holes, left by the ion irradiation step.

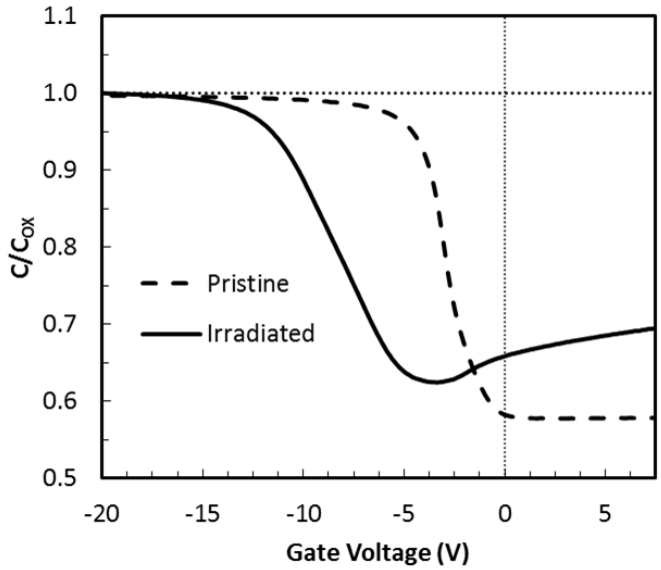


Figure 4.1: Two high frequency C-V curves taken on pristine (dashed line) and irradiated (solid line) MOS devices ($Al/SiO_2/Si$) with an ~1750 Å oxide layer. The irradiated device was constructed on a sample exposed to 1 keV Ar^{4+} ions at a dose of 4.58 x 10^{11} ions/cm^2.

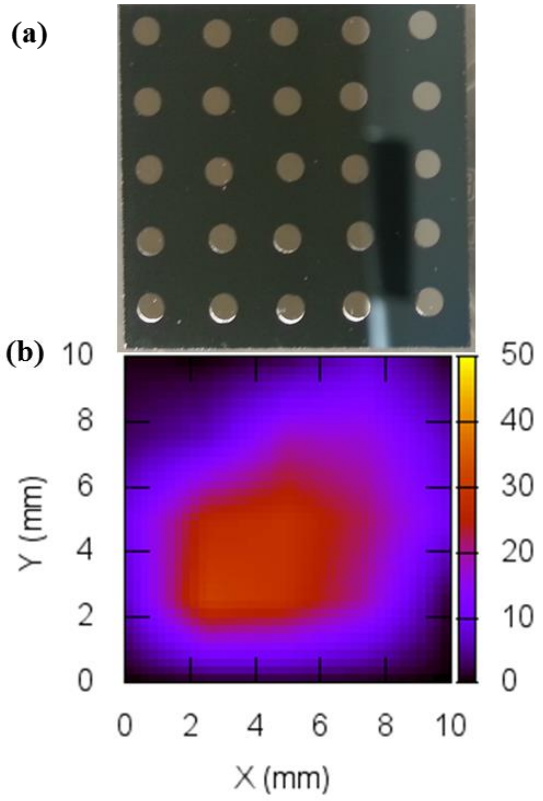


Figure 4.2: (a) Deposited Al dots on an Ar4+ irradiated SiO2/Si wafer with an 1750 Å oxide layer. (b) Interpolated image of the measured V_{FB} shifts obtained for each MOS device from high frequency C-V spectra. Units for color scale are volts.

Figure 4.3 shows the average flatband voltages vs dose of the ions for charge states (Q=1,4,8,11).The average flatband voltage are calculated by integrating the Gaussian fit to interpolated experimental flatband voltage over range of sample divided by the irradiated area of sample. Figure 4.4 shows the normalized flatband voltage shifts

vs. the charge state of the ions. The normalized flatband voltage shifts are found by finding the slopes of linear fit to data in figure 4.3.

This is consistent with radiation damage seen in other systems irradiated by gamma rays and UV radiation[11,31] and with an increase in oxide charge following radiation. Therefore, it is through the shifted V_{FB} values, taken relative to the pristine value measured for our prepared wafer, that we track the energetics of energy dissipation for our Ar^{Q+} ions that have impacted the MOS oxide layer.

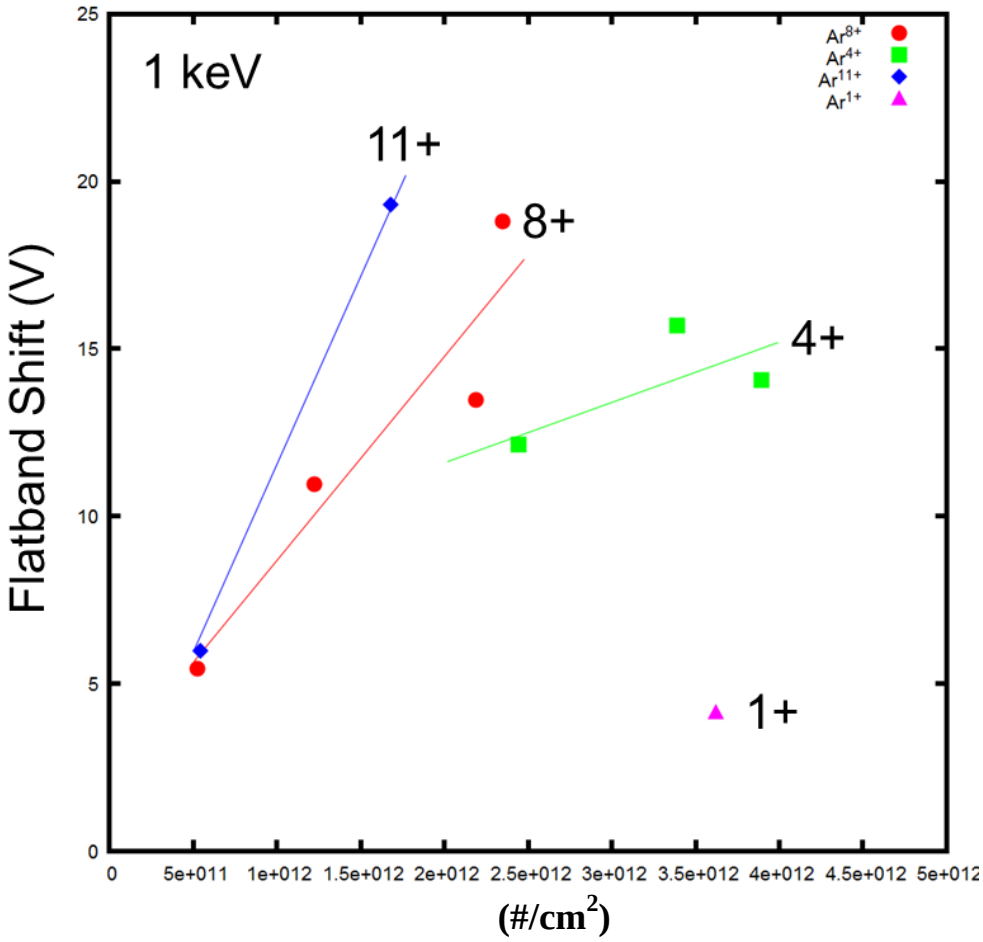


Figure 4.3: Average flatband voltage shift calculated from Gaussian fit to the interpolated experimental flatband voltage obtained from C-V curves vs dose of Ar^{+Q} ions for charge states (Q=1,4,8,11).

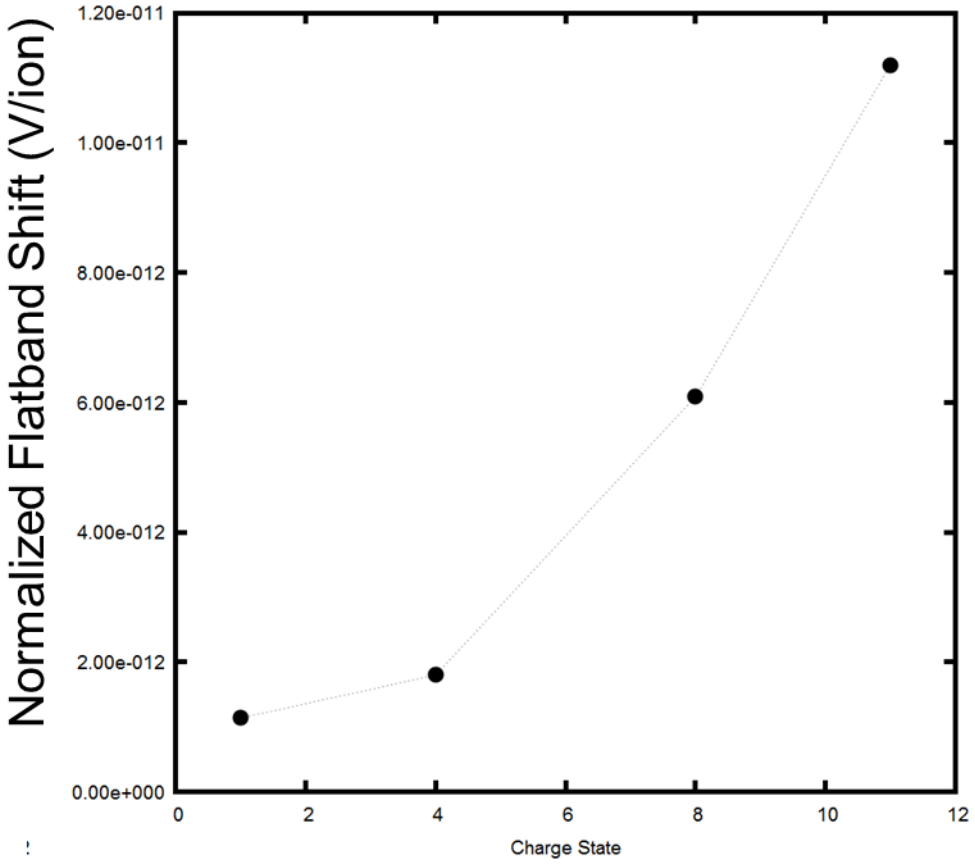


Figure 4.4: (a) Normalized Flatband voltage shifts obtained from the slopes of linear fit from figure 4. 3 vs. charge state of the beam (Q=1,4,8,11).

4.2 Preliminary Results

Given the focused nature of the HCI beams extracted and directed into the target region, it has been observed that there is a distribution of dosed regions across each of the samples irradiated for this measurement. This can be seen in Fig. 4.2 (b), where the measured V_{FB} data taken across multiple deposited Al gates (gate positions indicated by

the white overlaid circles) has been interpolated across the entire sample surface. The figure clearly represents the current density profile of the irradiating beam in terms of the induced shifts it generates in the V_{FB} values for the subsequently deposited MOS devices. This result, which is seen for all the charge states explored, indicates that the dose of ions striking the SiO_2 is recorded by the C-V extracted V_{FB} shifts. Such a dose dependence is consistent with previous results for HCIs and devices, where each ion impact is determined to produce a measurable change in the irradiated target material[35].

In addition, the results obtained to date for multiple charge states indicate that there is a significant enhancement in the induced V_{FB} shift as the charge state of the incoming beam is increased. This can be quantified by measuring the V_{FB} shift across multiple ion doses for fixed incident charge states so that a normalized value of the V_{FB} shift induced per incident ion can be obtained . Although preliminary, the normalized results show an enhancement in the normalized shift per ion, which grows monotonically across our charge state data, from 1.14×10^{-12} V/ion for Ar^{1+} ions to 1.12×10^{-11} V/ion for Ar^{11+} ions. We note that this approximately order of magnitude increase occurs for ions with a fixed incident kinetic energy of 1 keV. Therefore, we can interpret this result as a reflection of the differences in potential energy for the two charge states (15 eV for Ar^{1+} and 2004 eV for Ar^{11+}). In simplest terms, the sensitivity of the C-V results to subsurface oxide damage has served as a record of the enhanced potential energy dissipation of the higher charge state ions as they impact on and are implanted into the oxide layer.

4.3 Summary

As grown samples of SiO_2 have been irradiated by HCIs for different charges states and encapsulated into MOS devices. The ion irradiation effects have been interpreted through C-V measurements. The preliminary data indicates that the energy deposited into the oxide produces electron-hole pairs and that the oxide is sensitive to the ion charge state. These results appear to confirm that dose- and charge-dependent effects can be recorded for HCI irradiation on oxides using the MOS method**.** Also, the energy loss for slow ions shows a quadratic dependency on the incident charge state.

Appendices

Appendix A

High Frequency C-V Measurements with HP 4280A

1. Turn on HP 4280A 1 hour prior to taking measurements by pushing the Line On/Off button so that the lights come on. (Note: the 1 hour prior to taking measurements is a warm up time)
2. Connect a 1 meter test lead (BNC, grey color) between the 'High' input ('Unknown' terminals) on the HP 4280A and 'probe 1' of the probe station via simple coax connectors on the left side of the probe station. (Note: 'probe 1' is an arbitrarily selected probe in the probe station)
3. Connect a 1 meter test lead (BNC, grey color) between the 'Low' input ('Unknown' terminals) on the HP 4280A and 'probe 2' of the probe station via simple coax connectors on the left side(outside) of the probe station. (Note: 'probe 2' is an arbitrarily selected probe in the probe station)
4. If making measurements with voltage magnitudes greater than 42 V, do the following:
    a. Connect the inner conductor of the 'Remote ON/OFF' BNC to ground by using a BNC to alligator clip converter. (Note: ground is to the left of the 'Unknown' terminals. This ground terminal should also be connected to a common system ground…place where all other equipment is grounded) (see p. 3-38 in the manual)
    b. Switch the 'Int Bias' switch to '±100 V Max'.

5. Select ‘Floating’ for ‘Connection Mode’.
6. In ‘Function’ select the parameter(s) that you want to measure (normally we select ‘C’).
7. In ‘C-G Range’ select ‘Auto’ for preliminary test. You can select ‘Manual’ to manually choose between the three options listed to the right if the desired range is known.
8. Set ‘Meas Speed’ to ‘Slow’.
9. Set ‘Sig Level’ to ‘30’ (mV rms).
10. Make sure ‘C-High Resoln’ is disabled (LED off)
11. Make sure all three ‘Math’ buttons are disabled (LEDs off)
12. Make sure the ‘Store Digit Shift’ buttons are disabled (LEDs off for the two buttons with LEDs, not concerned with the button without a LED)
13. Not concerned with the three ‘X-Y Recorder’ buttons
14. For C-V sweep, select the ‘Single’ button above ‘Sweep Mode’. (Note: This button has two purposes depending on the test being run; i.e. ‘Trigger’ vs. ‘Sweep Mode’ functions, see p. 3-7 in the manual).
15. Hit the ‘Internal Bias’ button until the diagram depicting a single staircase sweep is selected (2).
16. Set the ‘Start V’ by doing the following:
    a. Hit the up and down arrow keys in the ‘Parameter’ box until the light next to ‘Start V’ is lit.

b. Hit the blue enable key; the key directly below the ‘Enter’ key (note: keys will now perform the function denoted by the blue ink below the respective keys).
c. Use the keypad (blue ink in the 3 columns of buttons under ‘Math’) to select the values.
d. Hit the ‘Enter’ key to confirm the value (the value should appear in the ‘V-t’ display screen).

17. Set ‘Stop V’, ‘Step V’, ‘Hold Time’, and ‘Step Delay Time’ in the same manner described in the previous step (step 16). Typical values of ‘Hold Time’ and ‘Step Delay Time’ are 60 s and 1 s respectively. (Values can be changed to milliseconds by hitting the down arrow in ‘Parameter’ after selecting the desired value).
18. Internal Error Correction (see p. 3-35 in the manual) (Note: both ‘probe 1’ and ‘probe 2’ should NOT be touching anything at this point)
    a. Make sure ‘Enable’ key in the ‘Correction’ box is disabled (LED off)
    b. Hit the down arrow in the ‘Correction’ box until ‘1’ (m) is selected (the LED next to ‘1’ is on)
    c. Press the small black ‘Open’ button under ‘Zero’ (to the right of the ‘Int Bias’)
    d. Push the ‘Enable’ key (LED lit)
    e. OPTIONAL: Push the ‘Repeat’ button above ‘Sweep Mode’ (LED lit) and change the ‘Internal Bias’ to DC Level (1). The displayed capacitance should be near 0 if the internal error correction was done correctly.

19. Select ‘Single’ above ‘Sweep Mode’ (LED lit) and change the ‘Internal Bias’ to single staircase sweep (2) if the optional step above (step 18-e) was performed.
20. Place the sample to be tested on the chuck and turn the vacuum pump on. Place ‘probe 1’ on the metal contact of the capacitor to be tested. Place ‘probe 2’ on the chuck near the capacitor being tested. Connect the outer conductors of ‘probe 1’ and ‘probe 2’ with a small cable as close as possible to the DUT to remove the parasitic capacitance (see Figure 3.10 on p. 3-33 in the manual; also, see Figure 1 below)

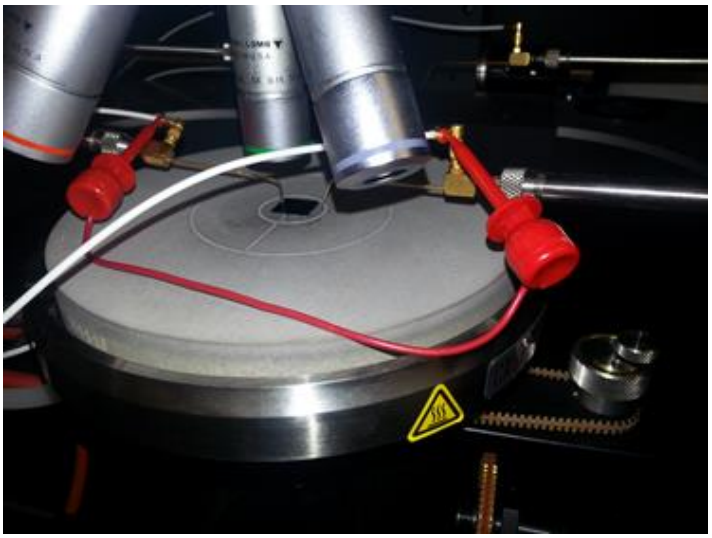


Figure 1: Image showing how to connect the outer conductors of ‘probe 1’ and ‘probe 2’ (color version on computer).

21. Connecting a computer and configuring the settings (note: this is just one of several possible methods):

a. Connect a HPIB-USB controller between the HP 4280A and a laptop
b. Adjust the HPIB settings on the HP 4280A to address '51: Talk Only Comma' (see Figure 2 for clarification).
c. On the HP 4280A, select 'Repeat' above 'Sweep Mode'
d. Boot laptop into Ubuntu (or some type of LINUX system)
e. Open a terminal and type "dmesg | grep –i USB" to identify the USB port where the connecter in part (a) is attached. (Note: you are looking for something in the output like: "FTDI USB Serial Device converter now attached to ttyUSB0")
f. In the terminal type "sudo minicom -s" for serial port setup
g. Scroll down to "Serial port setup" and hit enter
h. Hit the 'A' key and change the serial device address to what was found in part (e). Hit enter.
i. Hit the 'E' key to set 'Bps/Par/Bits' by doing the following:
    i. Hit the 'C' key to select 9600 as the speed
    ii. Hit the 'N' key to select odd parity
    iii. Hit the 'V' key to select 8 bit data
    iv. Hit the 'W' key to select 1 stop bit. Hit enter and verify that the values edited for options 'A' and 'E' are correct. If values are correct, hit enter again.
j. Scroll down to "Save setup as dfl" and hit enter to save the setup as the default setup.

k. Scroll down to “Exit” and hit enter. Data should be displayed in the terminal; if data is not displayed, make sure ‘Repeat’ is selected on the HP 4280A. (Note: if you exit minicom entirely, type “sudo minicom” in the terminal to start dumping data to the terminal)

l. At any point while minicom is running, hit ‘ctrl’ + ‘A’ and then ‘Z’ for the minicom command summary.

m. On the HP 4280A, select ‘Single’ above ‘Sweep Mode’. (Note: the data can be cleared from the terminal by hitting ‘ctrl’ + ‘A’ and then ‘C’ if desired)

n. Hit ‘ctrl’ + ‘A’ and then ‘L’ and type a file name where the data will be captured and then hit enter (Example filename: **C-V_Data.txt**)

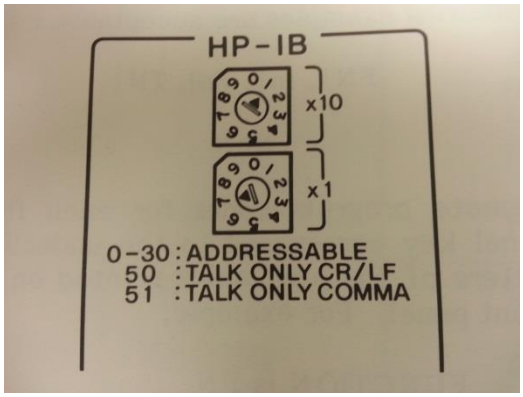


Figure 2: HPIB settings for the HP 4280A (located on the back). The dials should be adjusted to address ’51: Talk Only Comma’. (Note: The address shown in the image above is 17).

22. Hit the orange ‘Start/Stop’ button to begin the C-V sweep (sweep will stop automatically as long as ‘Single’ is selected).

23. After the sweep is completed go to the terminal and hit ‘ctrl’ + ‘A’ and then ‘L’. In the ‘Capture file’ box that comes up select ‘Close’ and hit enter. The file with the captured data will be in the Home Folder.

Appendix B

Quasi-Static C-V Measurements with HP 4140B

1. Turn on the HP 4140B 1 hour prior to taking measurements by pushing the Line On/Off button so that the lights come on. (Note: the 1 hour prior to taking measurements is a warm up time)
2. Make sure the 16054A Connection Selector is attached to the front of the 4140B.
3. Make sure the "Low Lead Connection" switch of the 16054A is set to 'V_A'.
4. Connect a triaxial cable between 'I' on the 16054A (which is connected to 'I Input' on the 4140B) and 'probe 1' via a triaxial to BNC converter connection on the left side of the probe station. (Note: 'probe 1' is an arbitrarily selected probe in the probe station)
5. Connect a short BNC cable between 'V_A' on the 16054A and 'probe 2' via the following steps (Note: 'probe 2' is an arbitrarily selected probe in the probe station):
    a. Connect 'V_A' to a BNC connection outside of the probe station
    b. For the same connector in part (a), connect a BNC to banana (female) converter on the inside of the probe station
    c. Connect a banana (male) to BNC converter to ONLY the outer conductor of the initial coaxial cable (the female banana labeled 'GND'). See Figure 1 for clarification.

d. Connect the BNC output from part (c) to ‘probe 2’. See Figures 2 and 3 for more detail on the circuit created by the connections described in Steps 4 and 5.

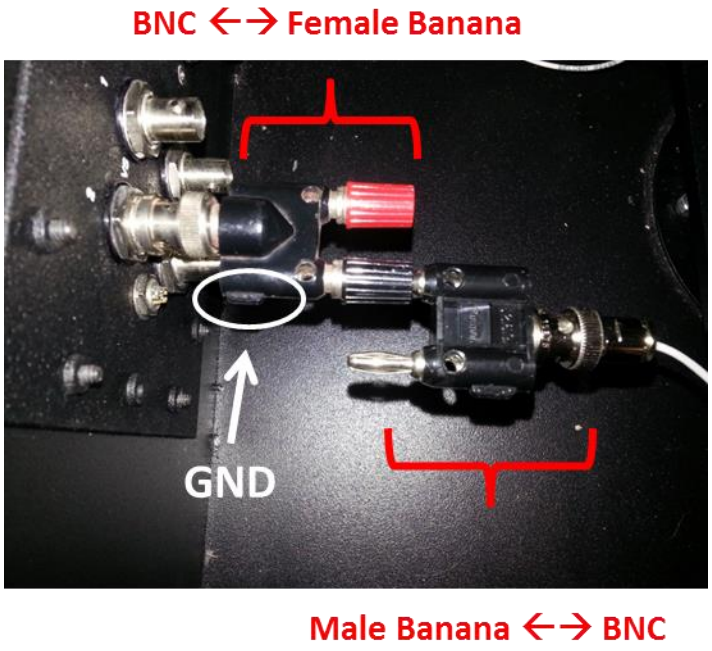


Figure 1: Image showing the details of the connection between ‘V_A’ on the 16054A and ‘probe 2’ (color version on computer).

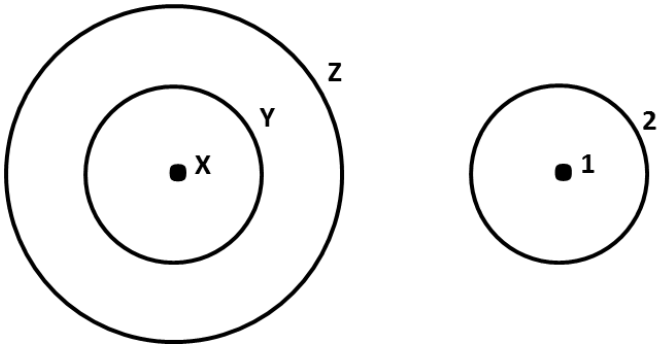


Figure 2: Cross sectional view of cables. Assigning variables to the different conductors of the triaxial cable (left) and the coaxial cable (right).

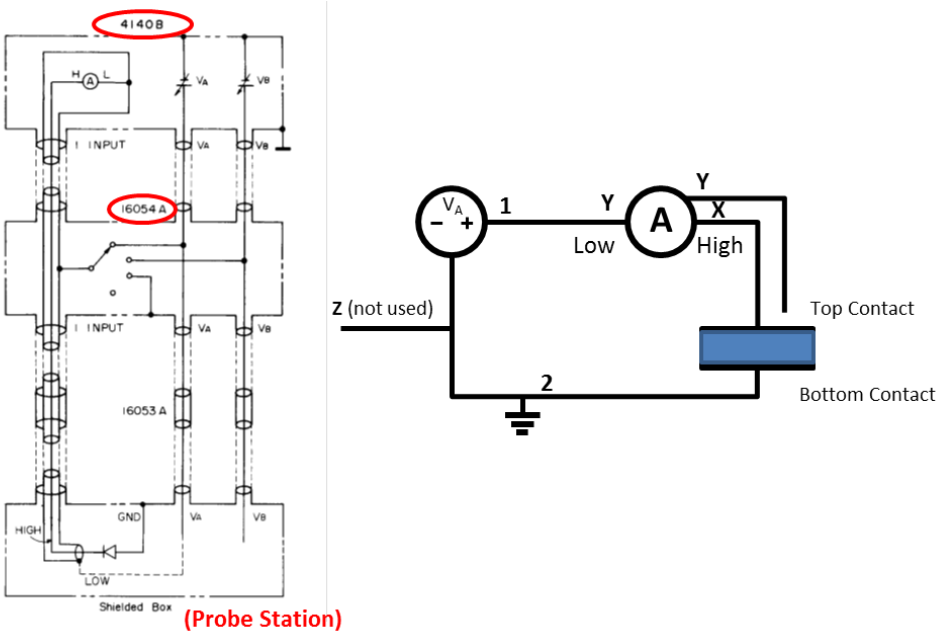


Figure 3: Connection diagram from the manual for 'Grounded DUT Measurement', p. 3-43 (left), and a simplified circuit (right) using the variables defined in Figure 2 (color version on computer).

6. Place the sample to be tested on the chuck and turn the vacuum pump on. Place 'probe 1' on the metal contact of the capacitor to be tested. Place 'probe 2' on the chuck near the capacitor being tested.
7. Setting the appropriate 'I Range':
    a. Select 'I-V' as the 'Function'
    b. Set 'I Range' to 'Auto'
    c. In the 'Function' block for V_A and V_B, make sure the single sided staircase (3) is selected for 'V_A' and 'OFF' (2) is selected for 'V_B'. (Note: These should be the default settings after selecting 'I-V' as the 'Function' as described in part (a)).
    d. Set up a voltage sweep by selecting appropriate values for 'Start V', 'Stop V', 'Step V', 'Hold Time', and 'Step Delay Time' (see Step 12 below). (Note: These values must be the same values that you will use for your C-V sweep).
    e. Hit the 'Auto Start' button under 'V Sweep' (note: if the Red LED near 'V Output' is solid, then a test is running. If the LED is blinking, then there is an error.)
    f. Take note of the highest current magnitude shown in the range display. Range display is between the 'E' and 'A' (Example: -11 is a higher current magnitude than -12).
    g. After the test is complete ('V Output' LED is off), use the up and down arrow keys in 'Manual' under 'I Range' to select the highest current

magnitude observed, as noted in part (f). (Note: Make sure that 'Auto' under 'I Range' is NOT selected; LED off)

8. Select 'C-V' as the 'Function'
9. Select 'Long' for 'Integ Time'
10. Make sure the 'Filter' button is on (LED lit)
11. In the 'Function' block for V_A and V_B, select the smooth, single sided ramp (1) for 'V_A' and select 'OFF' (2) for 'V_B' by using the appropriate down arrow keys
12. Setting the appropriate parameters for V_A:
    a. Push the 'V_A' button in the 'Parameter' box
    b. Push the 'Start V' button and use the keypad to the right to select the desired value. Press 'Enter' to store the value
    c. Set 'Stop V', 'Step V', 'Hold Time', 'dV/dt', and 'Step Delay Time' in the same manner described in part (b). Typical values of 'Hold Time', 'dV/dt' and 'Step Delay Time' are 60 s, 0.01 and 1 s respectively
13. Offsetting the effect of the cables (zero offset)
    a. Remove 'probe 1' from the capacitor, and remove 'probe 2' from the chuck (neither of the probes should be touching anything at this point)
    b. Push the 'Auto Start' switch under 'V Sweep'
    c. Wait for the value in the display under 'I . C' to stabilize
    d. After the value described in part (c) has stabilized, push the 'Zero' button to the left of the 'I . C' display. (The effect is that the displayed capacitance is stored in ROM and it will be subtracted from subsequent

capacitance measurements; therefore, the open circuit value should be approximately zero.)

e. Hit the 'Abort' button

14. Place 'probe 1' on the metal contact of the capacitor to be tested. Place 'probe 2' on the chuck near the capacitor being tested.
15. Use the arrows keys in the 'Current Limit (A)' box (pointing to the right) to select 10^{-4} (1) for both V_A and V_B. (Note: the value corresponding to V_B is not really relevant since we are using V_A)
16. Connecting a computer and configuring the settings (Note: this is just one of several possible methods):
    a. Connect a HPIB-USB controller between the HP 4140B and a laptop
    b. Adjust the HPIB settings on the HP 4140B to 'Talk Only' (see Figure 4 for clarification).
    c. On the HP 4140B, hit the 'Local' button so that **only** the LED below 'Talk' is lit (LED under 'Remote' should be off).
    d. Then hit the 'I' button under 'Function' and make sure that 'Int' is selected under 'I Trig'. (The purpose of this step is to configure the HP 4140B so that it can display values in the terminal in a later step; step (16-L). This is to verify the connection).
    e. Boot laptop into Ubuntu (or some type of LINUX system)
    f. Open a terminal and type "dmesg | grep –i USB" to identify the USB port where the connecter in part (a) is attached. (Note: you are looking for

something in the output like: “FTDI USB Serial Device converter now attached to ttyUSB0”)

g. In the terminal type “sudo minicom -s” for serial port setup

h. Scroll down to “Serial port setup” and hit enter

i. Hit the ‘A’ key and change the serial device address to what was found in part (f). Hit enter.

j. Hit the ‘E’ key to set ‘Bps/Par/Bits’ by doing the following:

    i. Hit the ‘C’ key to select 9600 as the speed

    ii. Hit the ‘N’ key to select odd parity

    iii. Hit the ‘V’ key to select 8 bit data

    iv. Hit the ‘W’ key to select 1 stop bit. Hit enter and verify that the values edited for options ‘A’ and ‘E’ are correct. If values are correct, hit enter again.

k. Scroll down to “Save setup as dfl” and hit enter to save the setup as the default setup.

l. Scroll down to “Exit” and hit enter. Data should be displayed in the terminal; if data is not displayed, consult steps (16-C) and (16-D). (Note: if you exit minicom entirely, type “sudo minicom” in the terminal to start dumping data to the terminal)

m. At any point while minicom is running, hit ‘ctrl’ + ‘A’ and then ‘Z’ for the minicom command summary.

n. On the HP 4140B, select ‘C-V’ under ‘Function’; all sweep parameters previously set should be saved. (Note: the data can be cleared from the terminal by hitting ‘ctrl’ + ‘A’ and then ‘C’ if desired)

o. Hit ‘ctrl’ + ‘A’ and then ‘L’ and type a file name where the data will be captured and then hit enter (Example filename: **C-V_Data.txt**)

Figure 4: HPIB setting for the HP 4140B (located on the back). The switch circled in red should be positioned to the left; ‘talk only’ (color version on computer).

17. Push the ‘Auto Start’ button under ‘V Sweep’ to begin the C-V sweep
18. After the sweep is completed go to the terminal and hit ‘ctrl’ + ‘A’ and then ‘L’.In the ‘Capture file’ box that comes up select ‘Close’ and hit enter. The file with the captured data will be in the Home Folder

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