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EMC in Power Electronics and PCB Design

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EMC IN POWER ELECTRONICS AND PCB DESIGN

A Dissertation
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Electrical and Computer Engineering

by
Chentian Zhu
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Accepted by:
Todd Hubing, Committee Chair
Keith Corzine
Pingshan Wang
John Wagner

ABSTRACT

This dissertation consists of two parts. Part I is about Electromagnetic Compatibility (EMC) in power electronics and part II is about the Maximum Radiated Electromagnetic Emissions Calculator (MREMC), which is a software tool for EMC in printed circuit board (PCB) design.

Switched-mode power converters can be significant sources of electromagnetic fields that interfere with the proper operation of nearby circuits or distant radio receivers. Part I of this dissertation provides comprehensive and organized information on the latest EMC developments in power converters. It describes and evaluates different technologies to ensure that power converters meet electromagnetic compatibility requirements. Chapters 2 and 3 describe EMC noise sources and coupling mechanisms in power converters. Chapter 4 reviews the measurements used to characterize and troubleshoot EMC problems. Chapters 5 – 8 cover passive filter solutions, active filter solutions, noise cancellation methods and reduced-noise driving schemes.

Part II describes the methods used, calculations made, and implementation details of the MREMC, which is a software tool that allows the user to calculate the maximum possible radiated emissions that could occur due to specific source geometries on a PCB. Chapters 9 – 13 covers the *I/O coupling EMI* algorithm, *Common-mode EMI* algorithm, *Power Bus EMI* algorithm and *Differential-Mode EMI* algorithm used in the MREMC.

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PART I

1. INTRODUCTION TO EMC IN POWER ELECTRONICS

Electromagnetic Compatibility (EMC) is the ability of devices and systems to operate without error in their intended electromagnetic environment. An electronic device should not interfere with other devices or be susceptible to electromagnetic emissions from other devices. Electromagnetic interference (EMI) is a key concern in the design of switched-mode power converters. Power converters can be significant sources of electromagnetic fields that interfere with the proper operation of nearby circuits or distant radio receivers. They can also be susceptible to electrical transients or strong coupled fields.

Compared to digital electronics, EMC design in power electronics didn't get much attention until the late 1990s when new developments in power semiconductor technologies made switched-mode power converters more popular due to their high efficiency. In this dissertation, only switched-mode power converters are discussed. Therefore, the term 'power converter' or just 'converter' in the text always refers to switched-mode converters.

Although there are many power converter topologies, this dissertation focuses on basic converters, such as the DC-DC buck converter, boost converter, fly-back converter and the DC-AC inverter. This is because, from an EMC standpoint, most converter topologies share the same characteristics, and the EMC solutions introduced here can be implemented on similar converter topologies with very little effort.

The purpose of this part of the dissertation is to provide comprehensive and organized information on the latest EMC developments in power converters. It describes and evaluates different technologies to ensure that power converters meet electromagnetic compatibility requirements.

Chapters 2 and 3 describe EMC noise sources and coupling mechanisms in power converters. Chapter 4 reviews the measurements used to characterize and troubleshoot EMC problems. Chapters 5 – 8 cover passive filter solutions, active filter solutions, noise cancellation methods and reduced-noise driving schemes.

Abbreviations used in Part I of the dissertation are listed below:

AC Alternating current

AZSPWM Active-Zero-State-Pulse-Width-Modulation

CDCCFB Current-detecting-current-compensating-feedback

CDCCFF Current-detecting-current-compensating-feed-forward

CDVC Current-detecting-voltage-compensating

CM Common-mode

DC Direct current

DM Differential-mode

DUT Device under test

EM Electromagnetic

EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMS	Electromagnetic susceptibility
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FCC	Federal Communications Commission
HF	High frequency
IC	Initial condition
IPEM	Integrated power electronics module
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LF	Low frequency
LISN	Line impedance stabilization network
NSPWM	Near-State-Pulse-Width-Modulation
PCB	Printed circuit board
PFC	Power factor correction
PWM	Pulse width modulation
QP	Quasi-peak

RF Radio frequency

RSPWM Remote-State-Pulse-Width-Modulation

SVPWM Space-Vector-Pulse-Width-Modulation

THD Total harmonic distortion

VDCC Voltage-detecting-current-compensating

VDVCFB Voltage-detecting-voltage-compensating-feedback

VDVCFE Voltage-detecting-voltage-compensating-feed-forward

2. NOISE SOURCES

Electromagnetic noise is electromagnetic energy that produces undesirable effects, such as degraded performance or system malfunctions. Examples of electromagnetic noise sources include lightning, radio frequency transmitters and CPUs operating at high clock speeds. Rapid changes in the electric field (voltage) or the magnetic field (current) are a common characteristic of these noise sources. In switching power converters, high efficiency is achieved by making the power transistors operate either in their cut-off or saturation regions. The less time the power transistors operate in their linear region, the less power loss there will be. As a result, these transistors can generally be modeled as switches, either on (in saturation) or off (in cut-off). The high voltage change rate (dv/dt) and the high current change rate (di/dt) associated with the switching operation of the power transistors are the main sources of electromagnetic noise in modern switching power converters. Typically, the voltage waveforms associated with the switching noise are:

- The switching waveform,
- the ripple waveform,
- ringing after a transition, and
- the diode reverse recovery waveform.

2.1 Switching Waveforms

2.1.1 Switching Waveforms in DC-DC Converters

The switching waveform in power converters is similar to a pulse-width modulated (PWM) signal. In DC-DC converters, the duty cycle of the pulse waveform is constant if the load is constant. FIGURE 2.1, FIGURE, 2.2, FIGURE 2.3 and FIGURE 2.4 show the schematic of a DC-DC buck converter, its SPICE model, the simulated voltage waveform at node A and the simulated current waveform flowing through branch B, respectively. The circuit simulation here and in the rest of the dissertation is performed using NI Multisim software's SPICE simulation. A 30- Ω resistor is inserted between the NMOS gate and the pulse signal to control the voltage rise time at node A for better demonstration of the noise waveform. In the buck converter, when the switch, S, closes, the voltage source, V_{in} , supplies current to the load and the voltage at node A will be same as V_{in} in the ideal circuit model. When the switch opens, the current from V_{in} is cut off, but the inductor, L, keeps the current flowing to the load through the freewheeling diode, D. The voltage at node A becomes -1 V, due to the 1-V voltage drop across the diode. The average voltage across the load is regulated by controlling the duty cycle of the switching operation.

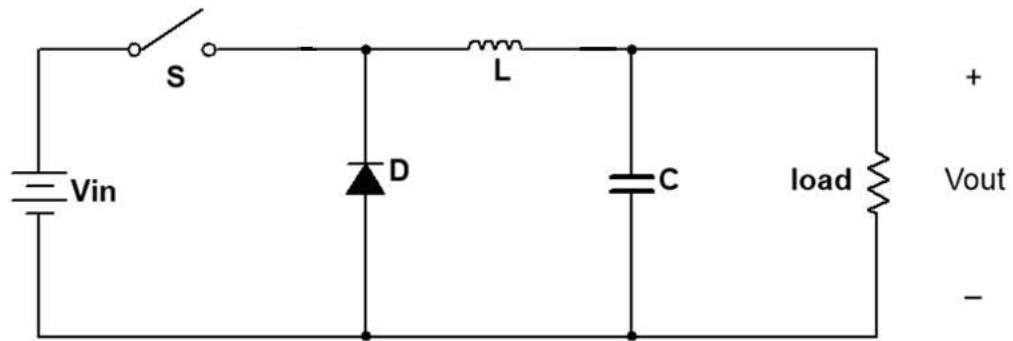


FIGURE 2.1 DC-DC buck converter schematic.

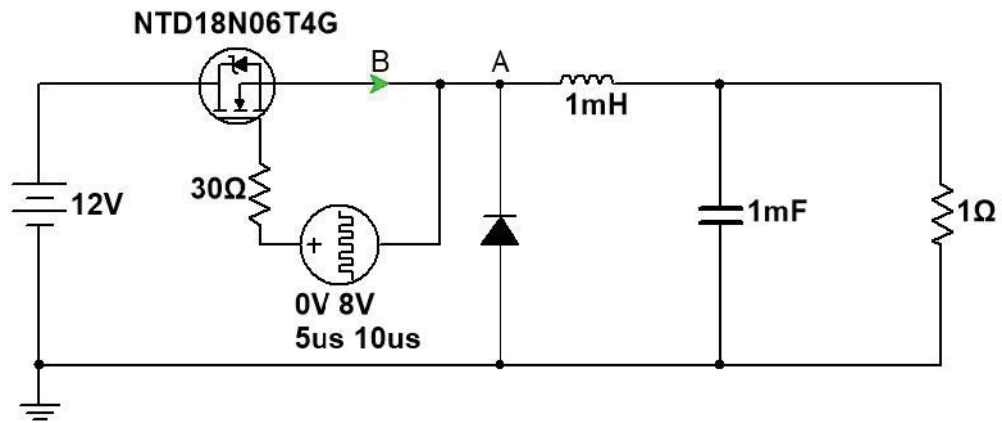


FIGURE 2.2 DC-DC buck converter model for simulation.

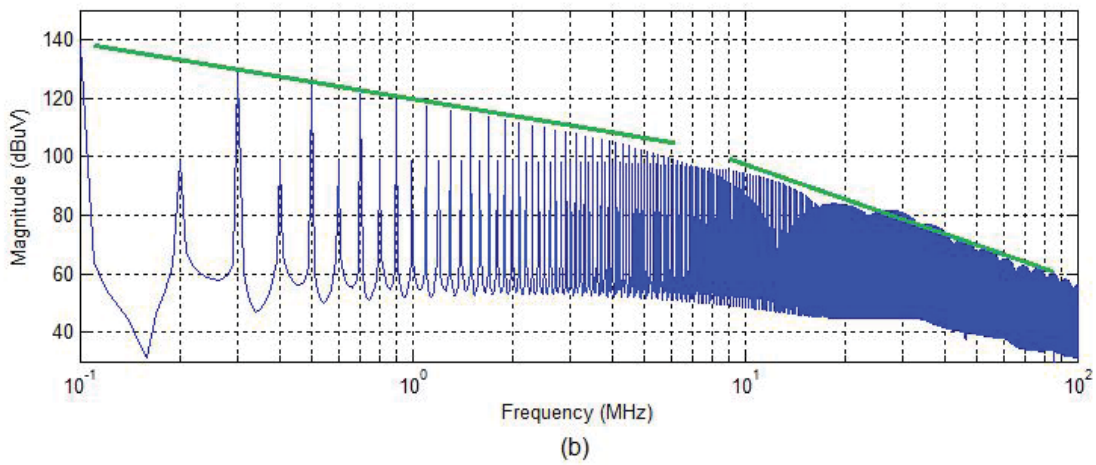
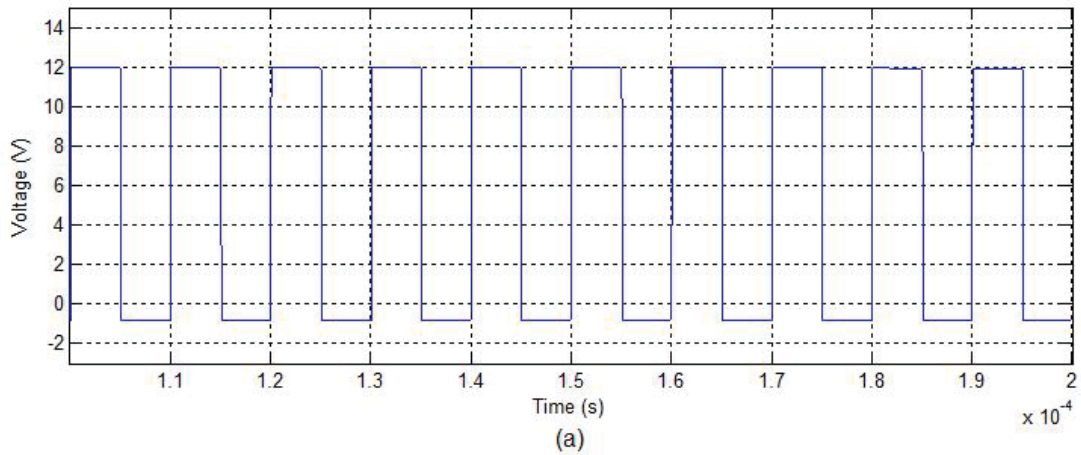


FIGURE 2.3 Voltage waveform at node A: (a) time domain, (b) frequency domain.

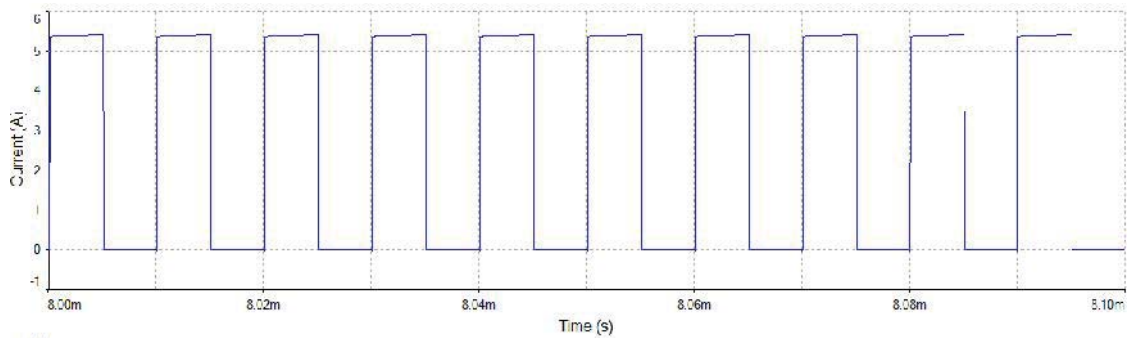


FIGURE 2.4 Waveform of the current flows through B.

Using the *Fourier series* expansion, a periodic signal can be represented by a sum of its frequency components. For example, the perfect square wave with a period, T , and a duty cycle, $T/2$, shown in FIGURE 2.5(a), has the frequency spectrum shown in FIGURE

2.5(b) [1]. In the figure, the magnitude of the even harmonics is zero and the magnitudes of the odd harmonics decrease linearly with frequency (-20 dB/decade). In real power converters, the switching waveform has a finite rise and fall time, t_r and t_f , as shown in FIGURE 2.6. Assuming t_r and t_f are equal, the frequency representation of the trapezoidal waveform is shown in FIGURE 2.7. The envelope of the spectra shows that magnitudes of the harmonics decrease linearly with frequency until a certain frequency, which is usually referred to as the cutoff frequency. Beyond the cutoff frequency, the magnitudes of the harmonics are proportional to $1/f^2$, (-40 dB/decade). The magnitude of the harmonics of the switching frequency and the cutoff frequency of an ideal trapezoidal waveform with the same rise and fall time are given by,

$$V_n = \frac{2A\tau}{T} \left(\frac{\sin\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}} \right) \left(\frac{\sin\left(\frac{n\pi t_r}{T}\right)}{\frac{n\pi t_r}{T}} \right) \quad (2.1)$$

$$f_c = \frac{1}{\pi t_r}, \quad (2.2)$$

where A is the amplitude of the trapezoidal waveform, n is the number of the harmonic, τ is the duty cycle, t_r is the rise time, and T is the period. FIGURE 2.3(b) shows the harmonics of the switching waveform rolling off by 20 dB per decade from 100 kHz to approximately 6 MHz. At higher frequencies, the harmonics roll off by 40 dB per decade. From (2.2), the waveform in FIGURE 2.3(a) has a rise/fall time of about 50 ns.

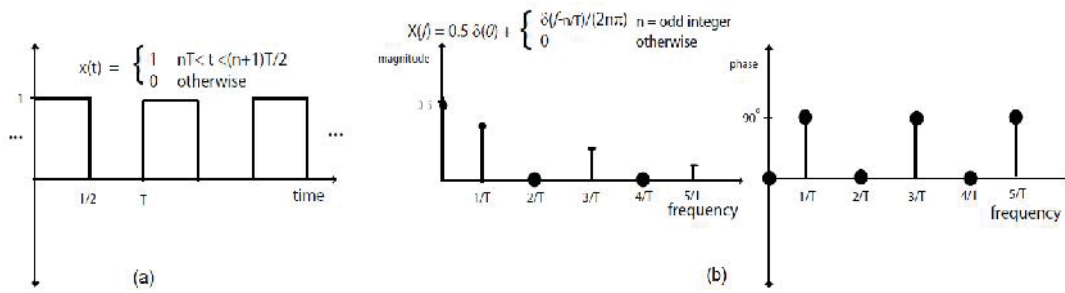


FIGURE 2.5 Periodic signals in the time and frequency domain. [1]

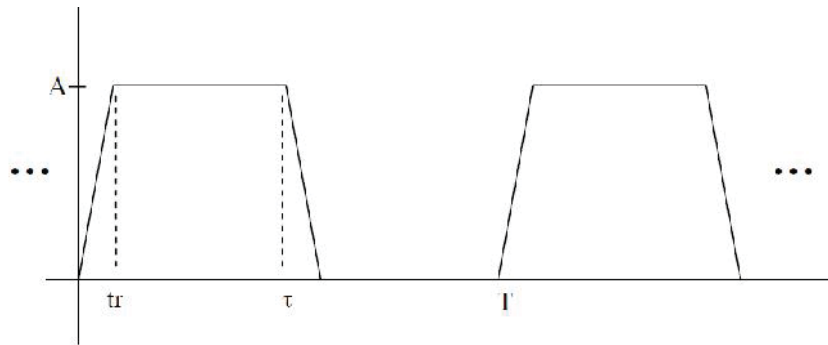


FIGURE 2.6 Trapezoidal waveform. [1]

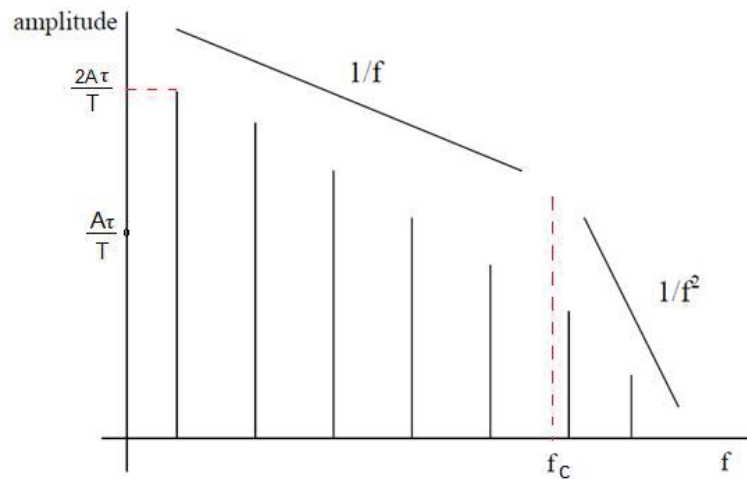


FIGURE 2.7 Frequency Domain representation of a trapezoidal signal. [1]

Although the switching frequencies of power converters are generally much lower than that of most digital circuits, power converters can still generate a lot of high-

frequency noise due to the high magnitude of the fundamental frequency component and the very fast rise times.

2.1.1.2 Switching Waveform in DC-AC Inverters

In DC-AC inverters, in order to output an AC voltage, the duty cycle of the pulse waveform is constantly changing. FIGURE 2.8 shows the schematic of a three-phase DC-AC inverter. In each phase, there are two transistor switches. When the low-side switch at node A is open and the high-side switch is closed, node A is tied to DC+ and current flows from the DC source to the load. When the high-side switch opens, the load inductance keeps the current flowing through the body diode of the low-side switch and node A is tied to DC- through the diode. After a short period of time while both switches are open, the low-side switch is closed and the current changes from being routed through the body diode to being routed through the transistor's pn junction. This is similar to a synchronous DC-DC buck converter. The waveform at node A will have a shape approximated by a series of trapezoidal pulses. The difference between the inverter and the buck converter is that the time-average output current of each phase of the inverter is sinusoidal AC. PWM is employed to change the duty cycle of the voltage waveform as illustrated in FIGURE 2.9(a). In this example, the PWM carrier frequency (switching frequency) is 20 kHz and the AC output waveform has a frequency of 50 Hz. The frequency-domain plot of the waveform in FIGURE 2.9(b) exhibits a 50-Hz peak with a magnitude equal to that of the resulting sinusoidal waveform. The 50-Hz component is the power frequency that drives the load. It is referred to as the normal operating frequency, or power frequency, of the power converter in the rest of this dissertation. The

20-kHz switching frequency and its harmonics can be a source of EMC problems. As a result, we want to design an EMC solution that reduces the switching noise while preserving the power frequency component.

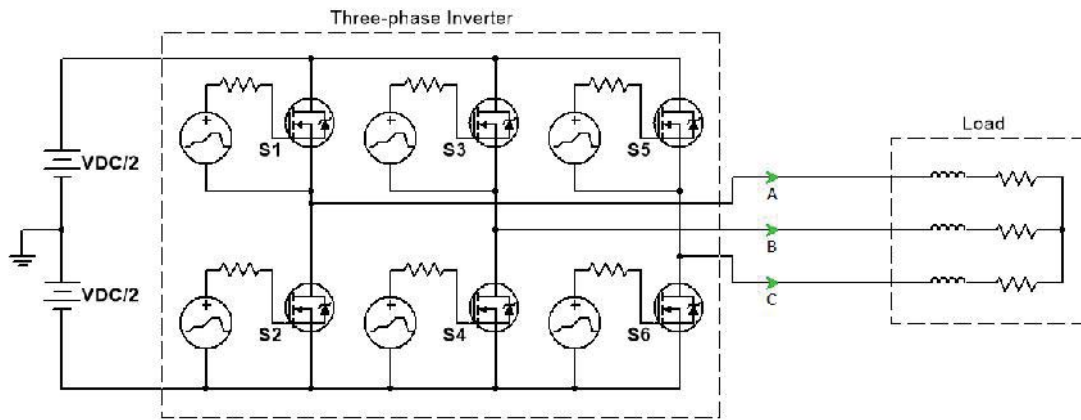


FIGURE 2.8 Three phase inverter model.

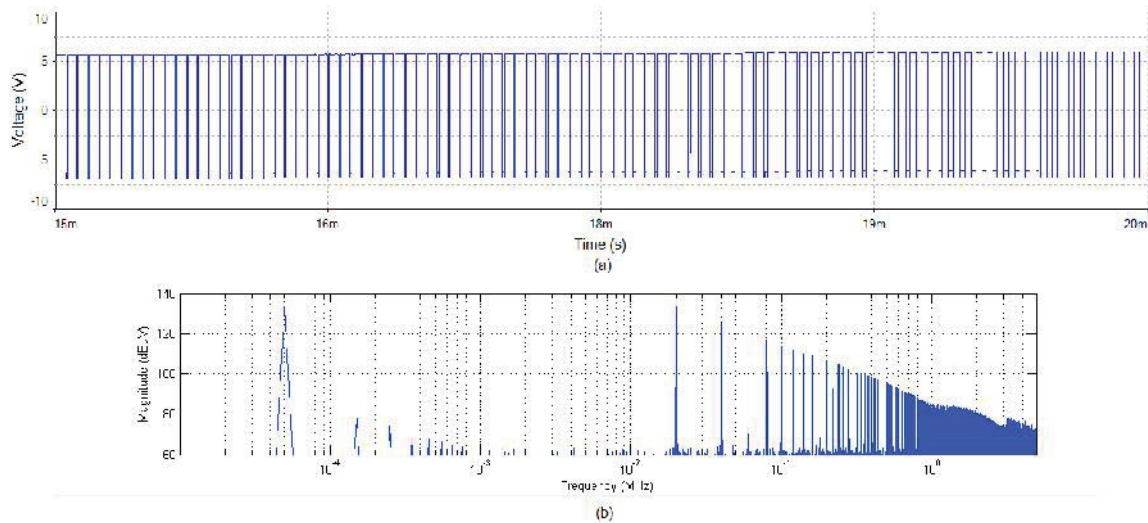


FIGURE 2.9 Waveform at node A. (a) Time domain. (b) Frequency domain.

This type of three-phase inverter is often used to drive three-phase AC motors. It is the current that generates torque in the motors, and the inductance of the motor windings filters (averages) the high-frequency current harmonics, so there is generally no need to

filter the switching noise to make the motor work. FIGURE 2.10 shows a time-domain plot of the phase currents for the inverter model above. As shown in the figure, the waveforms are very close to perfect sine waves. However, from an EMC point of view, the switching noise induces high-frequency currents on the phase cables that can result in conducted or radiated emissions. Thus, quite often, an EMI filter at the inverter output is required.

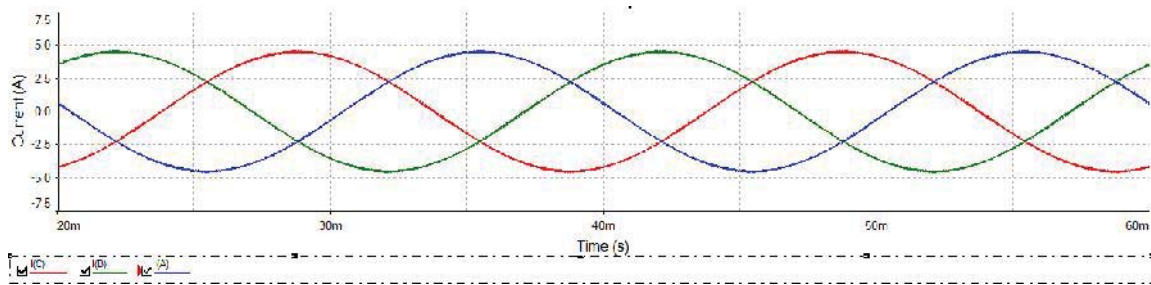


FIGURE 2.10 Phase current waveforms.

2.1.3 CM Voltage Waveform in Three-phase Inverters

Since common-mode (CM) noise on the inverter output cables is the main EMC concern, let's take a look at the CM noise source waveform. FIGURE 2.11 illustrates the Space Vector Pulse Width Modulation (SVPWM) [2] scheme commonly used to drive a three phase motor. The waveform in the lower left of the figure illustrates one period of the SVPWM voltage waveform on each of the three phases. As shown in the figure, the sum of the three phase voltages (relative to ground) is not constant with time. A CM voltage is generated. This CM voltage can drive currents that flow to ground through parasitic capacitances in the inverter and/or motor resulting in various EMC problems. The CM voltage and its spectrum for the inverter model in FIGURE 2.7 are plotted in FIGURE 2.12. Compared to the spectrum for the voltage on a single phase (FIGURE

2.9(b)), the 50-Hz peak is significantly reduced. However the harmonics of the 20-kHz PWM carrier frequency are about 10 dB higher. The three phase voltages cancel each other at the power frequency, but add at the switching frequency and its harmonics. CM currents on the inverter output cables don't contribute to the motor torque. Counter-measures must be employed when there are excessive CM currents that cause EMC problems.

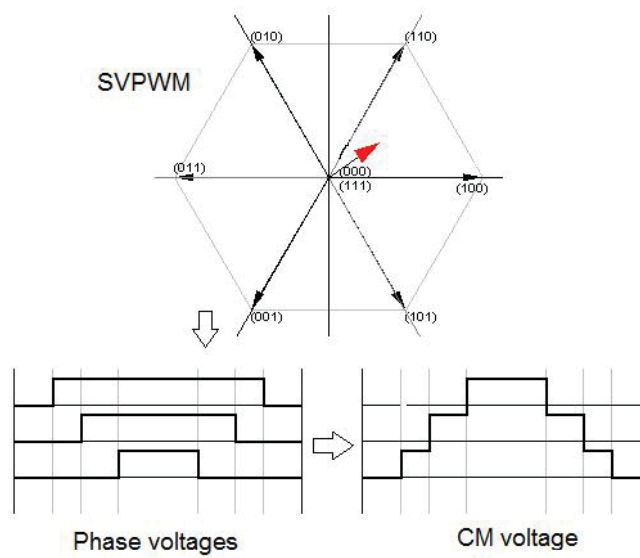


FIGURE 2.11 SVPWM driving scheme

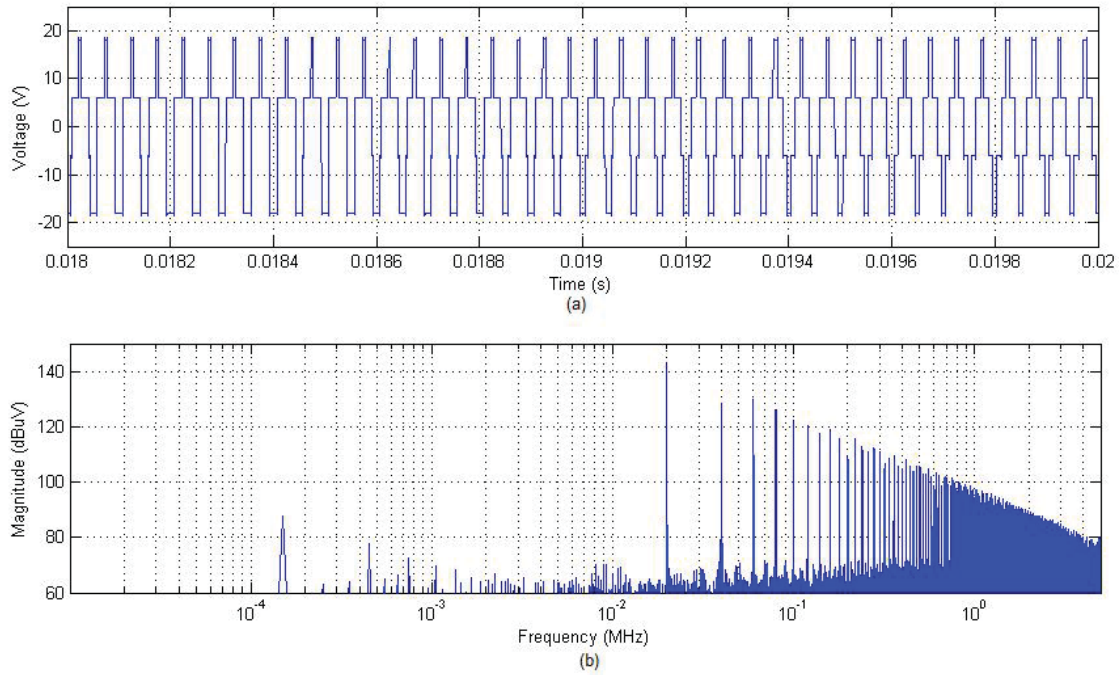


FIGURE 2.12 CM voltage of a three phase inverter. (a) Time domain. (b) Frequency domain.

2.2 Current Ripple Waveforms

Current ripples are very common in power converters. They are the result of charging and discharging of an inductor during the switching operation. Compared to the trapezoidal switching waveform, current ripple is a series of triangular waveforms with much smaller amplitude. It is usually much less of a concern as a noise source than the switching harmonics, but can be problematic in some situations.

2.2.1 Continuous Current Mode

Using the DC-DC boost converter in FIGURE 2.13(a) as an example, the voltage at node A and the current flowing through branch B are plotted in FIGURE 2.15(a) and FIGURE 2.15(b), respectively. During operation, when the switch S closes, current flows from the DC source to charge the inductor, L . When S opens, the energy stored in L will

raise the voltage across the diode until it conducts. When the diode, D, is conducting, the voltage at node A will be same as the output voltage. As shown in the figure, this voltage is a trapezoidal waveform. The current fluctuates between about 21.48 A and 21.54 A and never reaches zero. This operation mode is referred to as the *continuous current mode*. The magnitude of the ripple current, ΔI , can be calculated as [3],

$$\Delta I = \frac{V_s d}{Lf}, \quad (2.3)$$

where V_s is the DC input voltage, d is the switching duty cycle, and f is the switching frequency. Since the magnitude of the ripple is only 6 m thanks to the large value of L , the magnitude of the fundamental frequency component is very small as shown in FIGURE 2.15(c). The harmonics of the triangular current waveform decrease at a rate of 40 dB per decade.

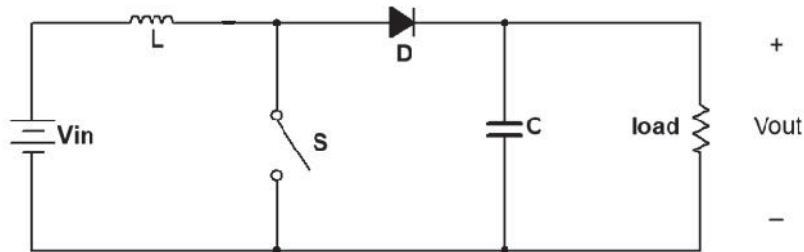


FIGURE 2.13 DC-DC boost converter schematic.

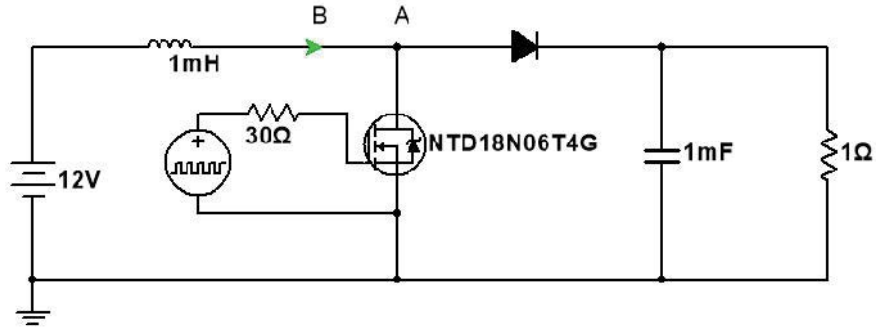


FIGURE 2.14 DC-DC boost converter model for simulation.

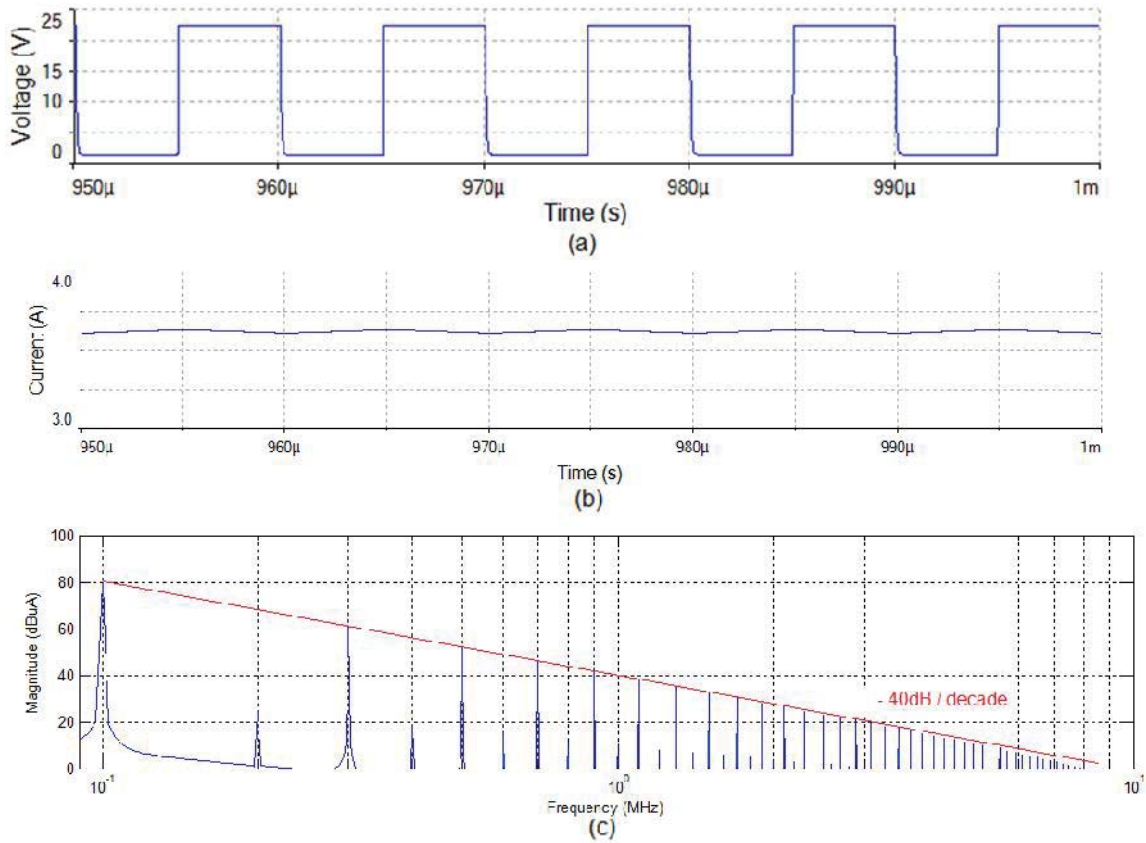


FIGURE 2.15 Waveforms. (a) Voltage at node A. (b) Current flows through B. (c) Current waveform spectrum.

2.2.2 Discontinuous Current Mode

The boost converter can also operate in a mode called *discontinuous current mode*. In this mode, the current flowing through node A will decrease to zero during the operation. One example of this is the boost Power Factor Correction (PFC) circuit shown in FIGURE 2.16. The PFC, inserted between the AC rectifier output and the load, has the same topology as a boost converter. As its name implies, it is used to correct the power factor of the converter. As shown in FIGURE 2.17, with the PFC, the average input current has the same sinusoidal waveform as the rectified input voltage, resulting in a power factor close to 1. For low power applications, the boost PFC often works in the discontinuous current mode as shown in the figure. The switch opens when the current increases to the reference peak and closes when the current decreases to zero. One advantage of the discontinuous current mode is that when the switch turns on, the current going through the diode, D, is zero. As a result, the circuit will not suffer from the *diode reverse recovery* effect, which will be discussed later in this chapter. With a 50-Hz AC input and the reference peak current set to 10 A, the spectrum of the ripple current was simulated and is plotted in FIGURE 2.18. As shown in the figure, the harmonics of the switching frequency roll off by 40 dB per decade, similar to the ripple waveform in the continuous current mode. However, the magnitude of the harmonic at the switching frequency is much higher compared to the magnitude of the same peak in the continuous current mode.

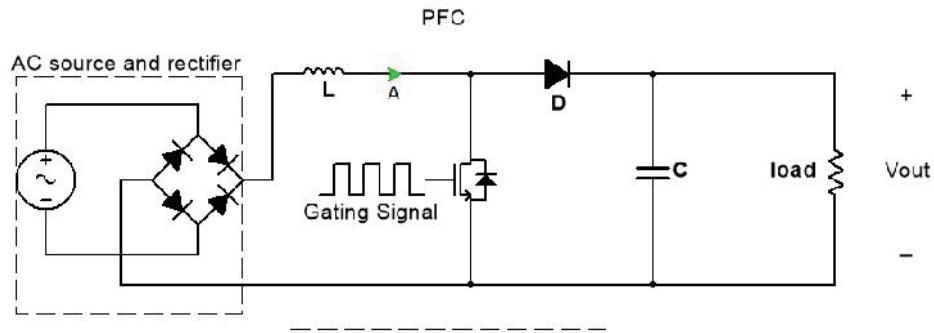


FIGURE 2.16 Boost PFC circuit model

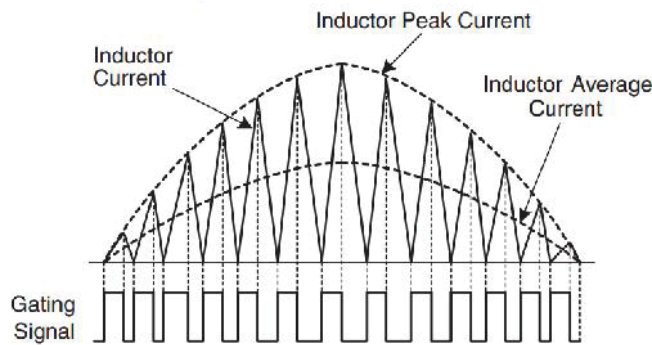


FIGURE 2.17 Ripple current flows through A.

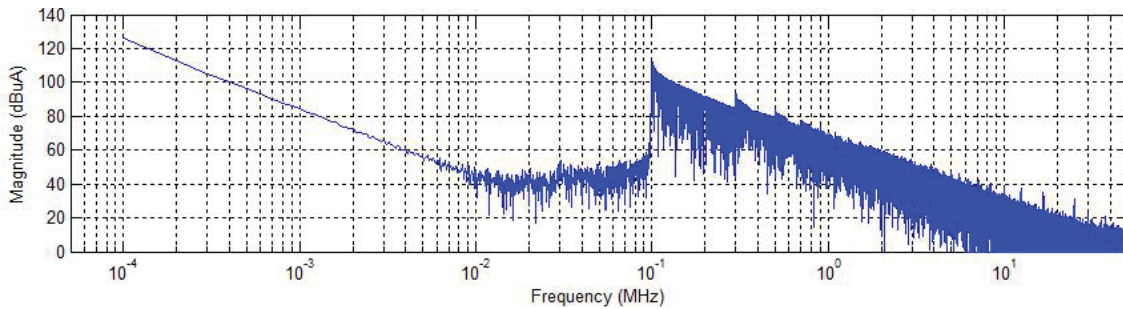


FIGURE 2.18 Spectrum of the ripple current flows through A.

2.3 Ringing in the Switching Waveform

The switching waveform in FIGURE 2.3(a) represents the ideal situation where none of the parasitic parameters of the transistor drive circuitry are considered. In reality, high frequency ringing in the switching waveform, as shown in FIGURE 2.19(a), is often observed. Correspondingly, a peak in the spectrum at harmonics near the ringing

frequency is observed as shown in FIGURE 2.19(b). Since the peak between 70 MHz and 80 MHz is far above the cut-off frequency, it might be ignored in the early product design stages. Understanding the ringing mechanism is an important aspect of the EMC design of power converters.

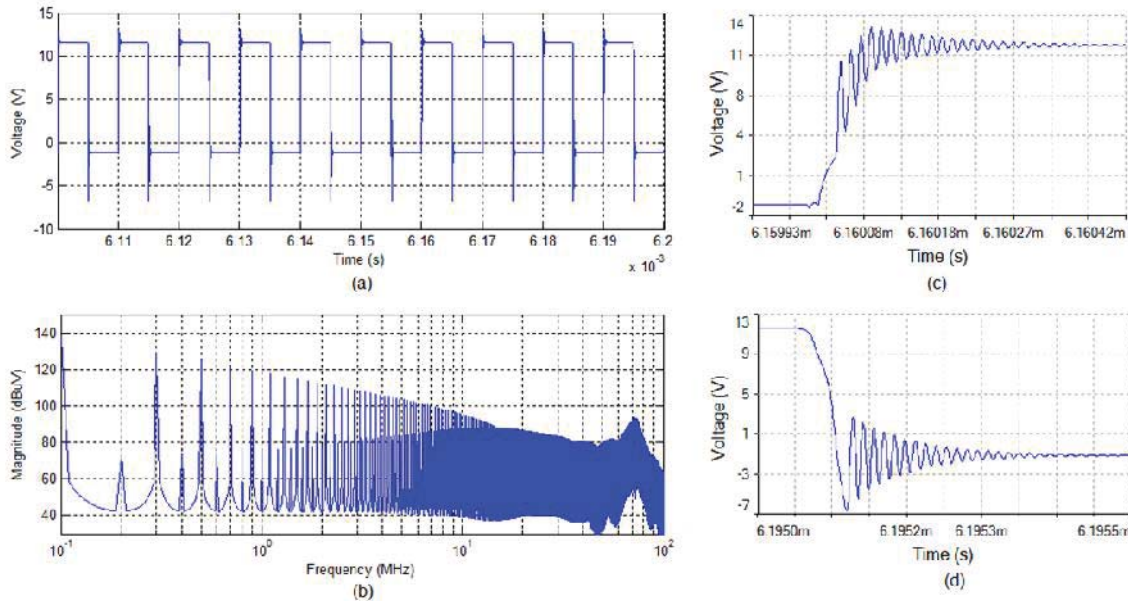


FIGURE 2.19 Ringing in the switching waveform: (a) time domain, (b) frequency domain, (c) ringing during voltage rising in time domain, (d) ringing during voltage falling in time domain.

2.3.1 Ringing in the Rising Edge

When ringing occurs, there is generally an equivalent RLC circuit involved. Kam and others [4] have studied the ringing waveform in synchronous buck converters. The synchronous buck converter has the same topology as the buck converter except that the diode is replaced by a MOSFET to reduce power loss. They concluded that the ringing is generated by the RLC loop shown in FIGURE 2.20. R is the loop resistance including the on-state resistance of the MOSFET, $Q1$. L is the parasitic inductance associated with the

loop, $L1+L2$. C is the drain-to-source capacitance of the power MOSFET, Q2. When the low-side MOSFET is turned off and the high-side MOSFET is turning on, the voltage transient at node A will be equivalent to the step response of the underdamped RLC loop, as shown in FIGURE 2.21(a), assuming $R = 50 \text{ m}\Omega$, $L1 = L2 = 10 \text{ nH}$, and $C = 200 \text{ pF}$. The ringing at node A is plotted in FIGURE 2.21(b). The ringing frequency can be calculated as,

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{20\text{nH}\cdot 200\text{pF}}} = 79 \text{ MHz}. \quad (2.4)$$

The RLC circuit models most of the oscillation mechanism, however, it doesn't account for the freewheeling current (i.e. the current that flows through the reverse recovery diode). Also, it doesn't apply to the ringing on the falling edge of the switching waveform.

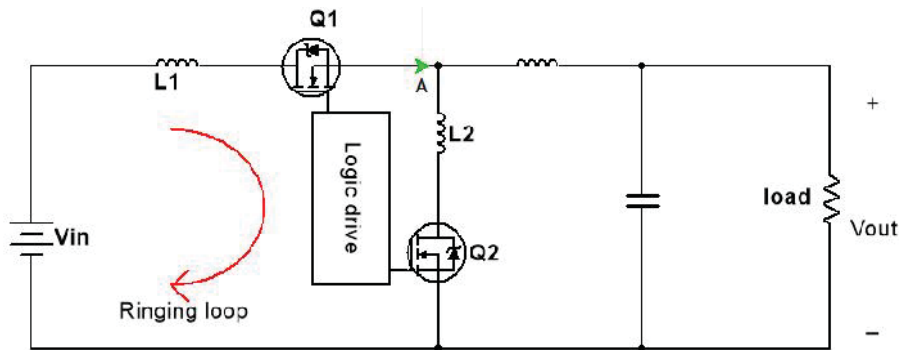


FIGURE 2.20 Ringing loop of a buck dc-dc converter.

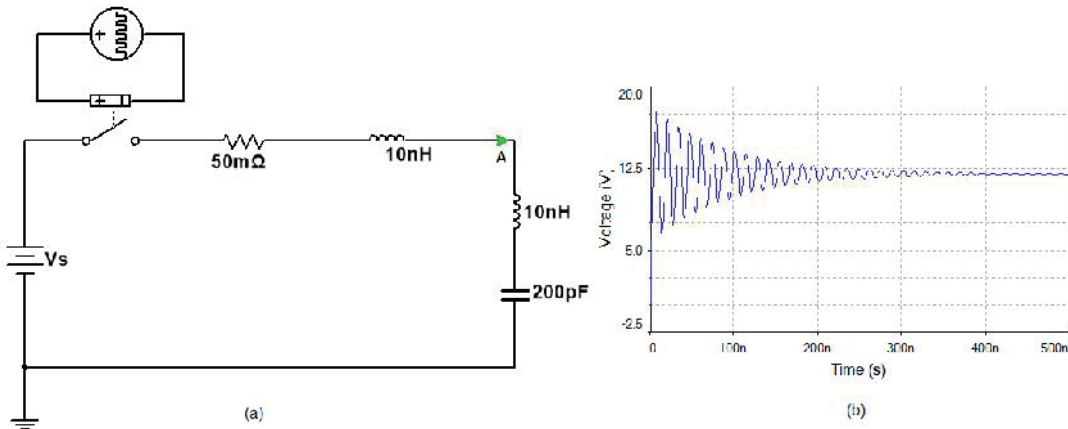


FIGURE 2.21 Simplified RLC model for voltage rising.

Assuming the ripple current in the load is negligible, a DC current source representing the load current that freewheels through the reverse recovery diode is added to the circuit in FIGURE 2.21(a) to model the ringing when the high-side MOSFET closes, as shown in FIGURE 2.22(a). The voltage rise is simulated and plotted in FIGURE 2.22(b) and FIGURE 2.23(b) for 6-amp and 30-amp load currents, respectively. As shown in the figure, the voltage is about 5 V prior to the transition. The delay before the ringing is due to the time needed to shut off the diode. When the Q1 switch closes, current flows from the source and raises the voltage across the body diode in Q2 to shut it off. The time needed to turn off the diode depends on the magnitude of the current flowing in the diode and also on the loop inductance and resistance. By KCL, the current increase in the Q1 branch and the current decrease in the Q2 branch must be the same. Thus, the voltage across the inductances of the two branches, V_{L1} and V_{L2} must be equal. As a result, the voltage at node A will be constant with a value approximately equal to half the source voltage if the loop resistance is ignored. At the point when the body diode of Q2 is completely turned off, the circuit can be as modeled as the circuit shown in

FIGURE 2.24(a). IC stands for ‘Initial Condition’ here. The 200-pF capacitor in the figure represents the drain-to-source capacitance of Q2. Since the circuit is now linear, superposition theory can be applied to remove the current source and the circuit can be simplified as shown in FIGURE 2.24(b). In this figure, when the switch S closes, ringing at node A is expected.

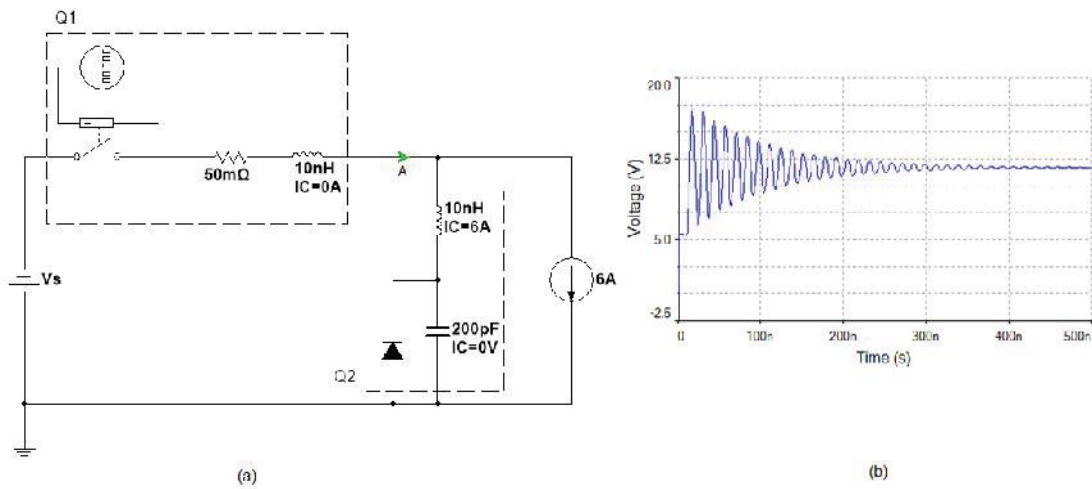


FIGURE 2.22 Synchronous buck converter model for voltage rise with 6 A load current: (a) model schematic, (b) voltage waveform at A.

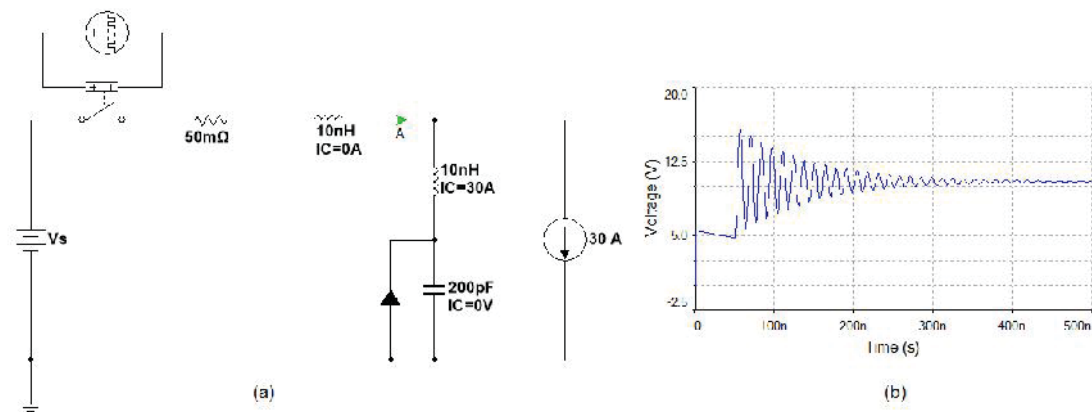


FIGURE 2.23 Synchronous buck converter model for voltage rise with 30 A load current: (a) model schematic, (b) voltage waveform at A.

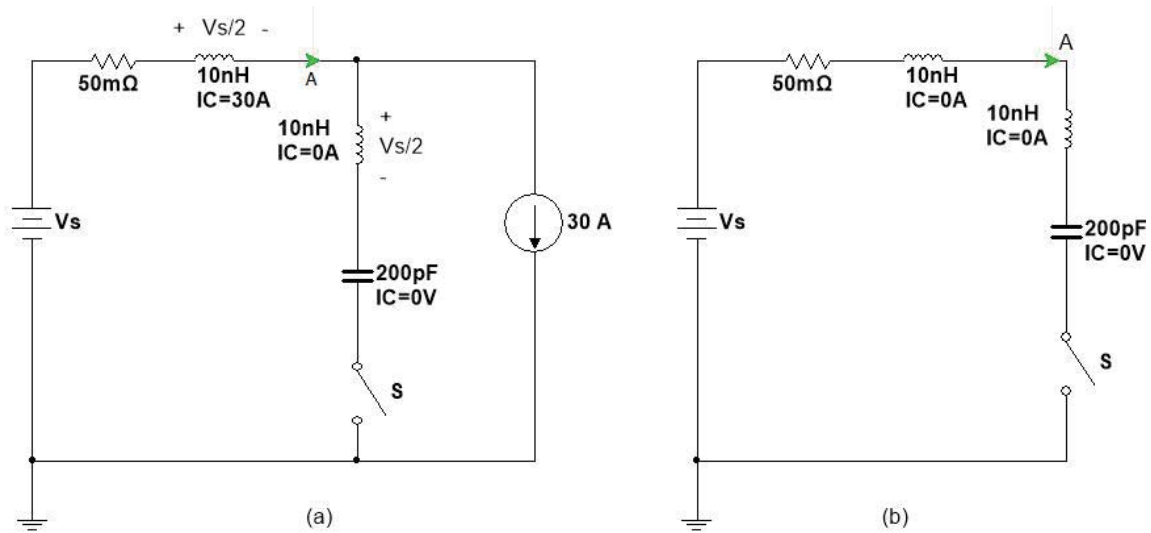


FIGURE 2.24 Circuit model when diode is off: (a) with current source, (b) without current source.

In reality, the MOSFETs won't turn on instantaneously. A rise time on the order of tens of nanoseconds to hundreds of nanoseconds is typical. FIGURE 2.25(b) and FIGURE 2.26(b) show the ringing waveforms during the voltage rise when the ideal switch and the $50\text{-m}\Omega$ resistance in the above models are replaced by a SPICE MOSFET model for 6-amp and 30-amp load currents, respectively. As shown in the figures, the ringing is superimposed on the rising edges of the trapezoidal switching waveforms.

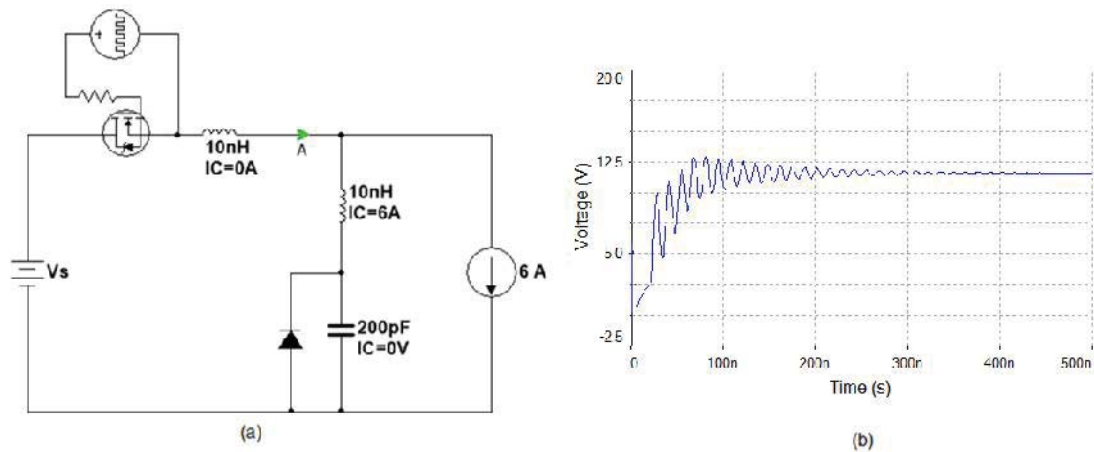


FIGURE 2.25 Synchronous buck converter model for voltage rise with 6A load current: (a) schematic with SPICE MOSFET model, (b) voltage waveform at A.

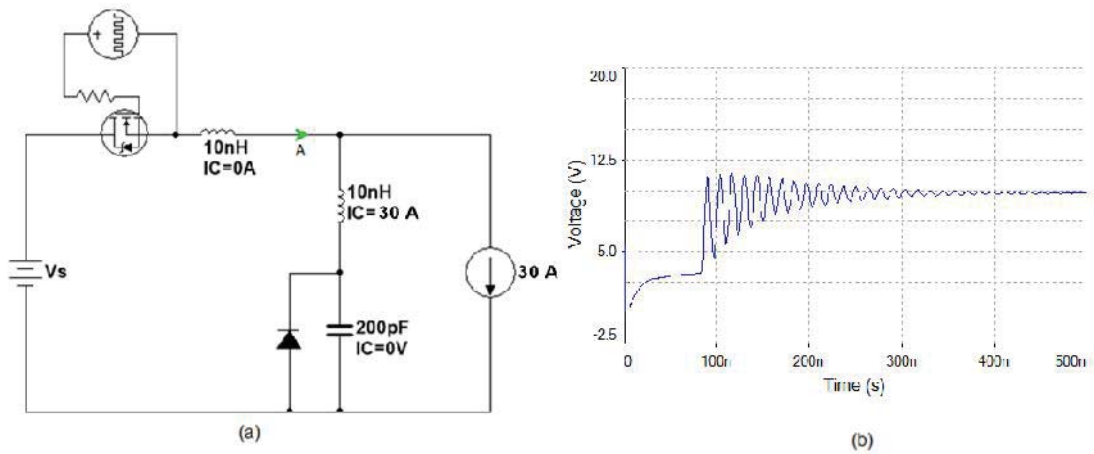


FIGURE 2.26 Synchronous buck converter model for voltage rise with 30 A load current: (a) schematic with SPICE MOSFET model, (b) voltage waveform at A.

2.3.2 Ringing in the Falling Edge

The ringing on the falling edge of the trapezoidal waveform is due to the same RLC loop, however, the R is mainly the on-state resistance of the body diode of Q2, and the C is the drain-to-source capacitance of Q1. FIGURE 2.27(a) shows the circuit model for the ringing on the falling edge. The same 6-A current source representing the load current is used. The 200-pF capacitance in parallel with the diode is shorted as soon as the diode starts conducting. When Q1 is turned off, the current flowing through node A to the load

decreases from 6 A to zero. Meanwhile, the current flowing through the body diode of Q2 increases from zero to 6 A. As a result, the voltages, V_{L1} and V_{L2} are induced across the loop inductances, L_1 and L_2 . The polarities of V_{L1} and V_{L2} are shown in the figure and their magnitudes can be estimated by,

$$V_{L1} = L_1 \frac{di_A}{dt}, V_{L2} = L_2 \frac{di_B}{dt} \quad (2.5)$$

where $\frac{di_A}{dt} = \frac{di_B}{dt}$ are the rates of current change at nodes A and B. Unlike the ringing edge, $V_{L1} + V_{L2}$ does not depend on the source voltage, V_s . After the MOSFET, Q1, is completely turned off, all of the load current freewheels through the body diode of Q2 as shown in FIGURE 2.24(a). Using superposition theory, this model can be simplified to the model in FIGURE 2.24(b). Due to the RLC loop in the model, ringing on the falling edge of the trapezoidal waveform is expected as shown in FIGURE 2.27(b). In the simulation, the switch opens at 5 microseconds and the voltage at node A decreases to $-V_{L2}$ and starts ringing. The ringing magnitude depends on the initial value of $V_{L1} + V_{L2}$, which is load current and switching time dependent. FIGURE 2.29 shows the ringing waveform with the ideal switch replaced by a SPICE MOSFET model. The ringing magnitude is significantly reduced due to the longer switching time associated with the MOSFET.

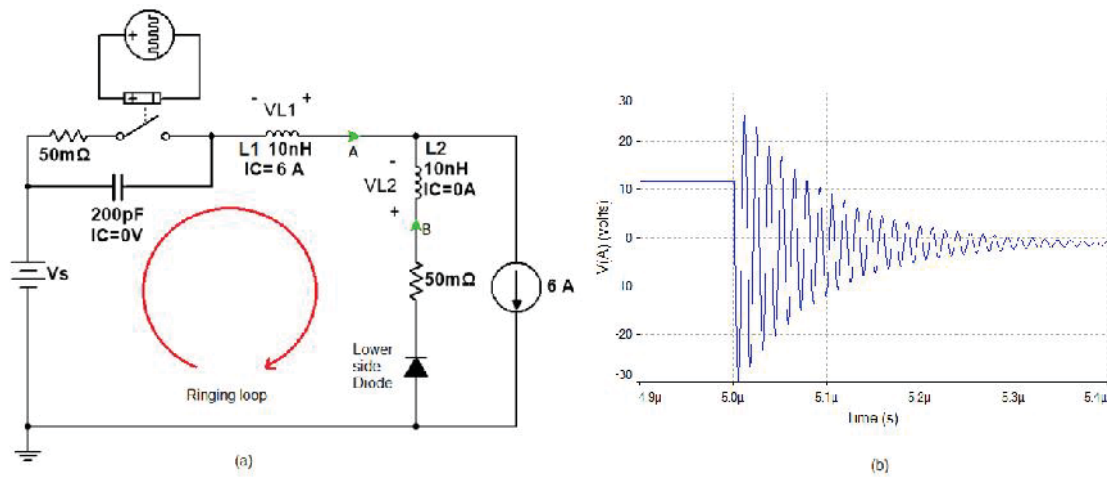


FIGURE 2.27 Synchronous buck converter model for voltage fall with 6 A load current: (a) model schematic, (b) voltage waveform at A.

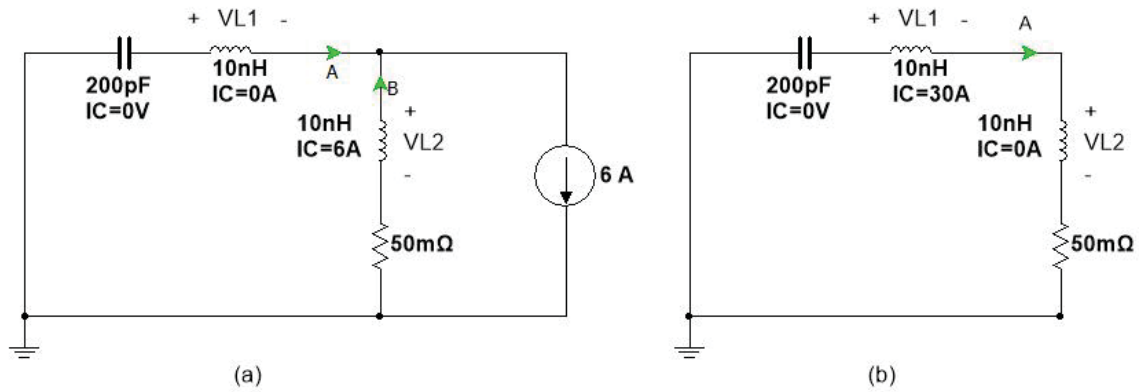


FIGURE 2.28 Circuit model Q1 is completely turned off: (a) with current source, (b) without current source.

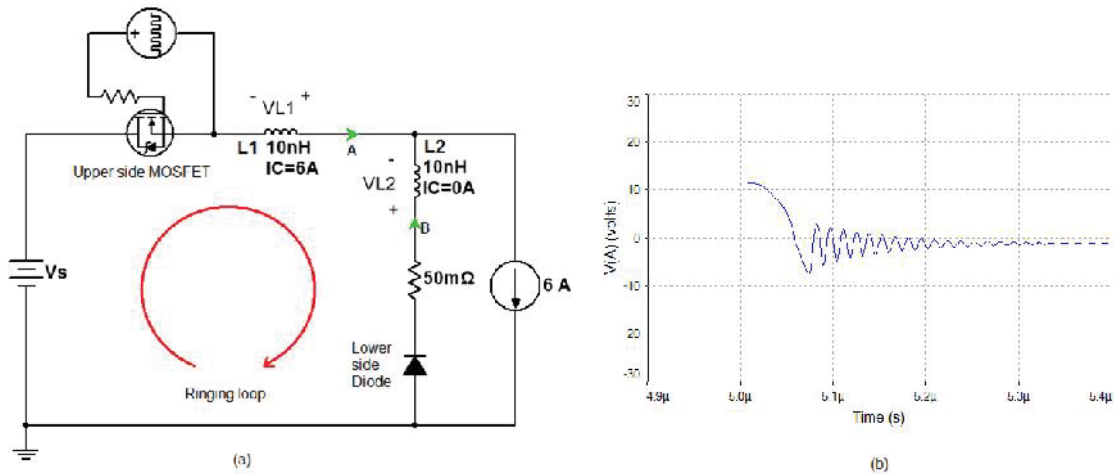


FIGURE 2.29 Synchronous buck converter model for voltage rise with 6A load current: (a) schematic with SPICE MOSFET model, (b) voltage waveform at A.

2.3.3 Ringing in Inverters

The three-phase DC-AC power inverter shown in FIGURE 2.30 has three branches employing the same MOSFET pair that can be found in a synchronous buck converter. Although the load current is AC, it is relatively low frequency and at the moment of phase voltage transition (rise/fall of the trapezoidal waveform), the load current can still be modeled as a DC current source. The major difference between the DC-AC inverter and the DC-DC converter is that the load current can flow in both directions. As shown in the figure, at some point during the operation current is flowing out on phase A and coming back through phase B and phase C. For phases B and C, the load current is in the opposite direction compared to the synchronous DC-DC converter we discussed above.

Using phase B as an example, the switching pattern in a PWM cycle can be decomposed into following steps where initially the load current flows through the pn junction of S4 to DC- and $V_B=0$. (V_B is voltage on phase B)

Step 1: S4 opens, the load current flows through the body diode of S3 to DC+, $V_B = V_{DC}$. (voltage drop across the body diode is neglected)

Step 2: S3 closes, the load current flows through the pn junction of S3 to DC+, $V_B = V_{DC}$.

Step 3: S3 opens, the load current flows through the body diode of S3 to DC+, $V_B = V_{DC}$.

Step 4: S4 closes, the load current flows through the pn junction of S4 to DC-, $V_B = 0$.

The ringing associated with the voltage rise and fall can be modeled as shown in FIGURE 2.31(a) and FIGURE 2.32(a) using the method introduced above. Note that in these models the negative terminal of the battery is the zero-volt reference, branch A is the S3 branch and branch B is the S4 branch.

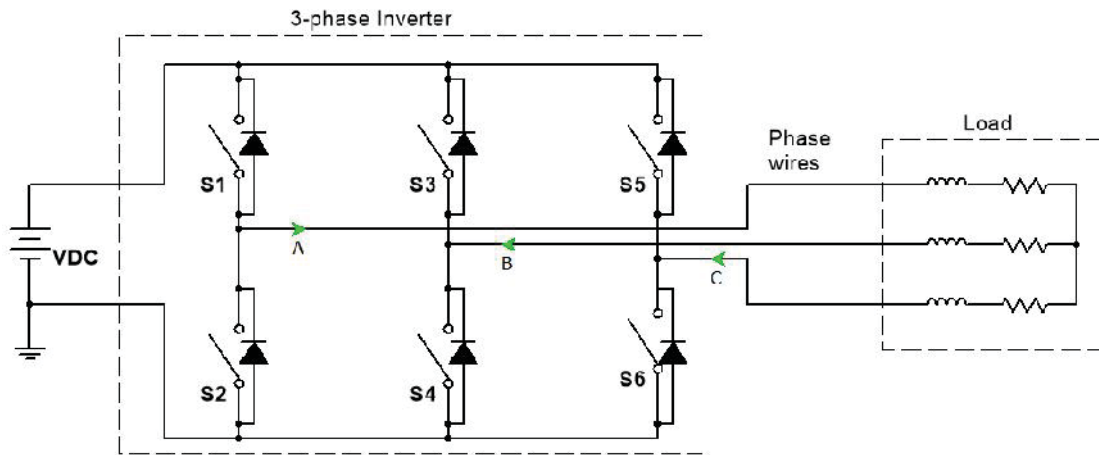


FIGURE 2.30 Three phase DC-AC inverter model.

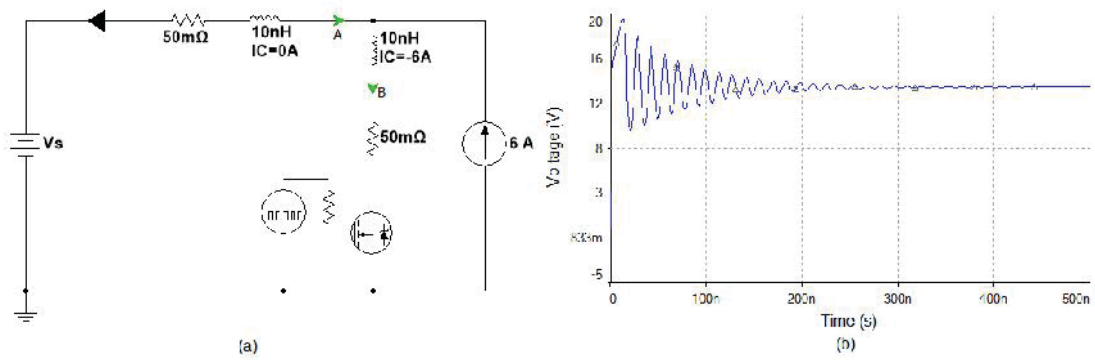


FIGURE 2.31 Inverter phase model for voltage rise with 6 A load current: (a) model schematic, (b) voltage waveform at A

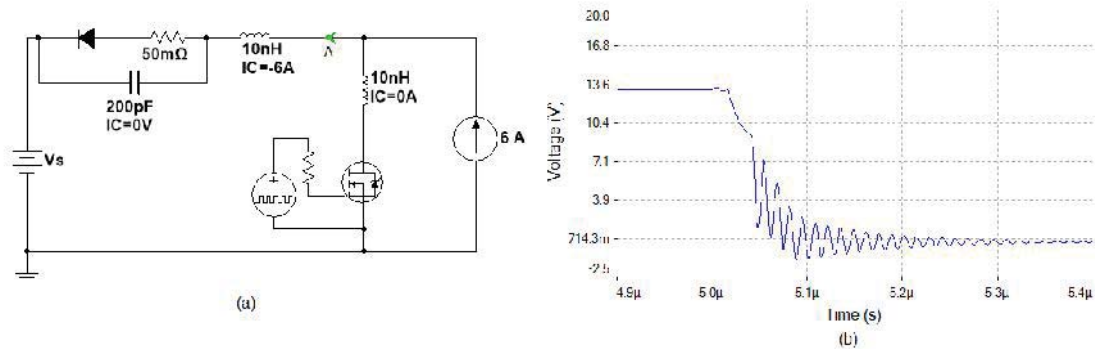


FIGURE 2.32 Inverter phase model for voltage fall with 6 A load current: (a) model schematic, (b) voltage waveform at A.

2.4 Waveform Due to Diode Reverse Recovery

Another well-known EMI source waveform in power electronics is caused by the *Diode Reverse Recovery* effect. It produces a sharp negative current and voltage spike on the output as shown in FIGURE 2.33. When the voltage across a diode transitions from a forward bias to a reverse bias voltage, V_r , it makes the diode transit from the *on* state to the *off* state. However, this doesn't occur instantaneously. As shown in FIGURE 2.33(a), the current in the diode decreases to zero when V_r is first applied. In contrast to an ideal diode in which the current would stay at zero, the current in a real diode increases in the opposite direction to a peak value of I_p , and returns to zero only after a time, t_r . t_r is called

the *reverse recovery time*. As a result, the voltage across the diode will have a negative spike, V_p , before it settles at V_r , as shown in FIGURE 2.33(b). More information about the diode reverse recovery effect can be found in [5].

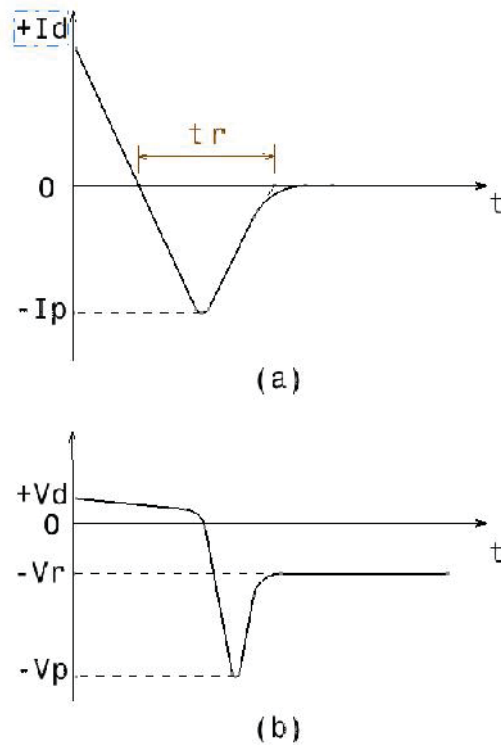


FIGURE 2.33 Diode reverse recovery.

The reverse recovery time of a diode can be of the order of nanoseconds and the negative current spike can be very high. These narrow current spikes produce wide band noise. In power converters, this wideband noise can enhance the ringing in the voltage and current waveforms due to the parasitic L and C in the circuit. In Section 2.3, where the turn-on and turn-off transient response of power converters was modeled, accounting for the diode reverse recovery can significantly increase the amplitude of the ringing.

3. COUPLING MECHANISMS

In this section, main mechanisms that couple noise sources to victim circuits will be discussed. They include:

- DM conducted emissions due to ESR and ESL of the filter capacitor,
- CM conducted emissions through parasitic capacitance,
- Radiated emissions from attached cables, and
- Near-field coupling.

The conducted emissions, both DM and CM, can contaminate the power grid and interfere with the electronic devices connected to it. Radiated emissions and near-field coupling can affect devices whether they are connected to the grid or not. These electromagnetic emissions need to comply with a variety of EMC regulations before the product can be shipped.

3.1 DM Conducted Emissions

The conducted emissions measurements described in regulations such as the FCC Rules and Regulations, Title 47, Part 15, require a Linear Impedance Stabilization Network (LISN) be inserted in the power supply lines to measure the conducted noise from 150 kHz to 30MHz. In this frequency range, the LISN provides a constant 50- Ω power line impedance from each phase to ground, thus the buck converter in FIGURE 2.1 in a DM conducted emissions test can be modeled by the circuit shown in FIGURE 3.1. In the figure, I_s is the noise current source, whose waveform can be found in FIGURE 2.4,

if the ringing and diode reverse recovery effects are ignored. The total LISN impedance is 100Ω , which is the sum of two 50Ω LISN impedances connected in series. In this model, the converter's filter capacitor (X capacitor) is represented by the capacitor labeled C_{in} . The filter capacitor shunts the noise current source, I_s . Theoretically, if the value of the capacitor is large enough, the DM conducted noise can be reduced to an arbitrarily low value. However, the ESR and ESL associated with the filter capacitor will limit its effectiveness.

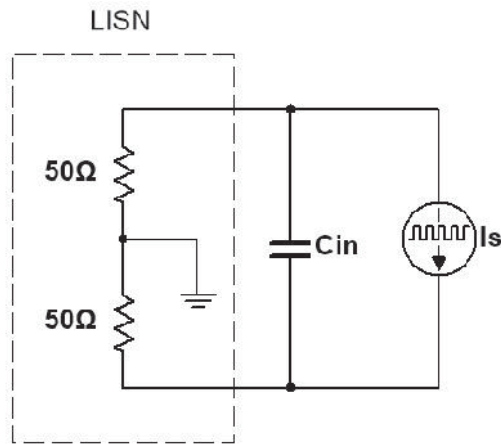


FIGURE 3.1 Simplified noise model of a buck converter with LISN.

A model of the ESR and ESL of the filter capacitor for the buck converter is shown in FIGURE 3.2. Assuming the value of C_{in} is large enough that it can be considered to have an insignificant impedance in the EMI noise frequency range, the DM noise received by the LISN can be calculated as,

$$V_{DM} = \frac{50(R_{in} + j\omega L_{in})}{50 + R_{in} + j\omega L_{in}} I_s . \quad (3.1)$$

Even at 30 MHz (the upper end of the conducted emissions frequency band), $R_{in} + j\omega L_{in}$ is often much smaller than 50 ohms, given that R_{in} is typically much smaller than 1 ohm

and L_{in} is usually on the order of tens of nanohenries at most. As a result, Equation (3.1) can be simplified to,

$$V_{DM} = (R_{in} + j\omega L_{in})I_S . \quad (3.2)$$

From (3.2), we can see how the ESR and ESL of the filter capacitor result in conducted emissions. As discussed above, the harmonics of I_s decrease at a rate of 20 dB per decade up to the cutoff frequency and at 40 dB per decade thereafter. As a result, harmonics of V_{DM} due to the ESR roll off quickly with frequency, while harmonics of V_{DM} due to the ESL stay flat up to the cut-off frequency. Consequently, the ESL of the filter capacitor is often a primary factor affecting DM conducted emissions in the megahertz range, while the ESR can dominate at lower frequencies. Both the ESL and ESR of the filter capacitor depend on the capacitor packaging and layout. For this reason a poor choice of capacitor or a poor layout can result in DM conducted emissions that exceed the regulatory limits.

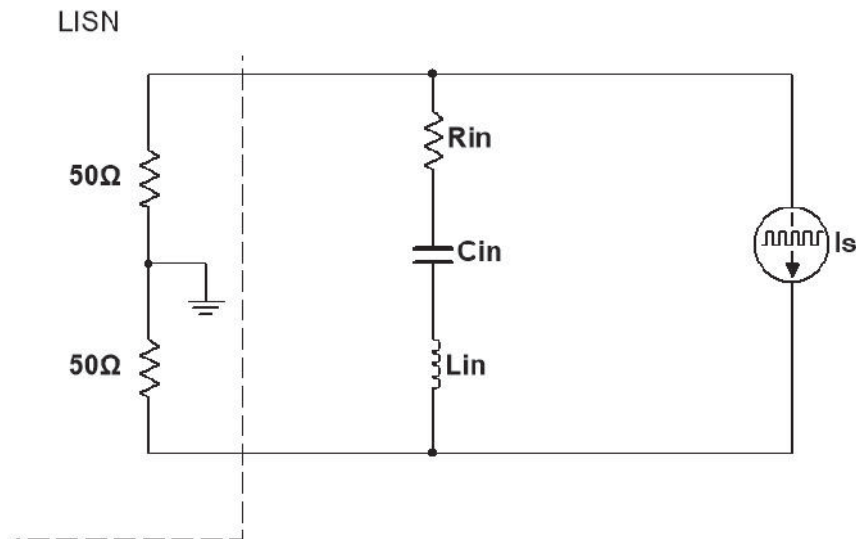


FIGURE 3.2 ESR and ESL of a filter capacitor.

The example shown in FIGURE 3.3(a) illustrates how DM conducted emissions in a buck converter can originate. As shown in the figure, a LISN model is inserted in the power supply lines. The simulated spectrum of the noise current is shown in FIGURE 3.3(b). The magnitude of the noise harmonics at 300 kHz and 5 MHz are 121 dB μ A and 94 dB μ A, respectively. The FCC class B conducted EMI limits at 300 kHz and 5 MHz are 60 dB μ V and 56 dB μ V, respectively. From (3.2), we can calculate and predict that an ESR that is larger than 1 m Ω , or an ESL larger than 2 nH will make the conducted EMI exceed the FCC limit. FIGURE 3.4 compares the noise received by the LISN when the filter capacitor has no ESR or ESL to the noise received when the ESR is 1 m Ω and the ESL is 2 nH, respectively. The FCC Class B conducted emissions limit is also plotted in the figures. For a large electrolytic filter capacitor, the ESR and ESL are often greater than 1 m Ω and 2 nH, respectively, when the capacitor leads and connected traces are taken into consideration. Thus, in order to design a buck converter meeting the above specification, additional noise mitigation solutions may be required.

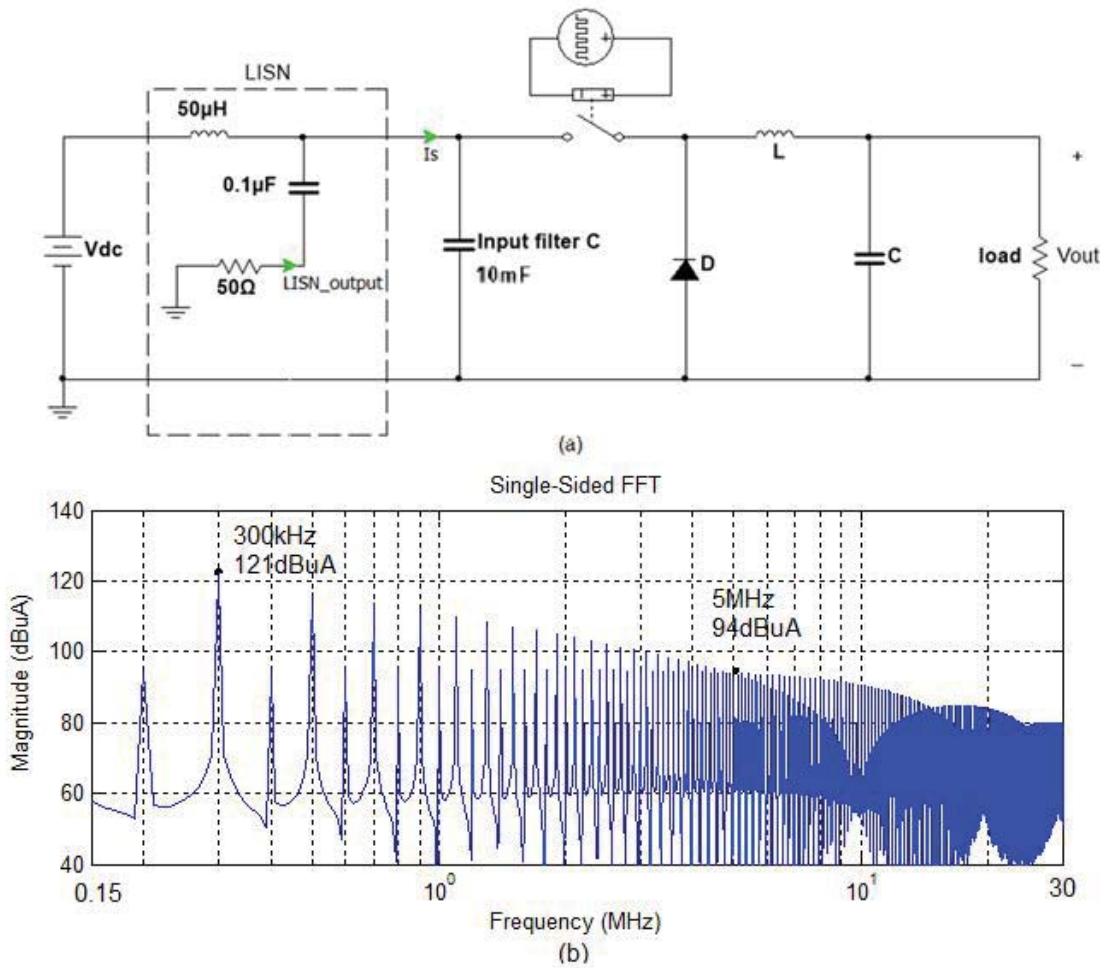


FIGURE 3.3 Buck converter DM conducted emissions example. (a) Circuit model. (b) Noise spectrum.

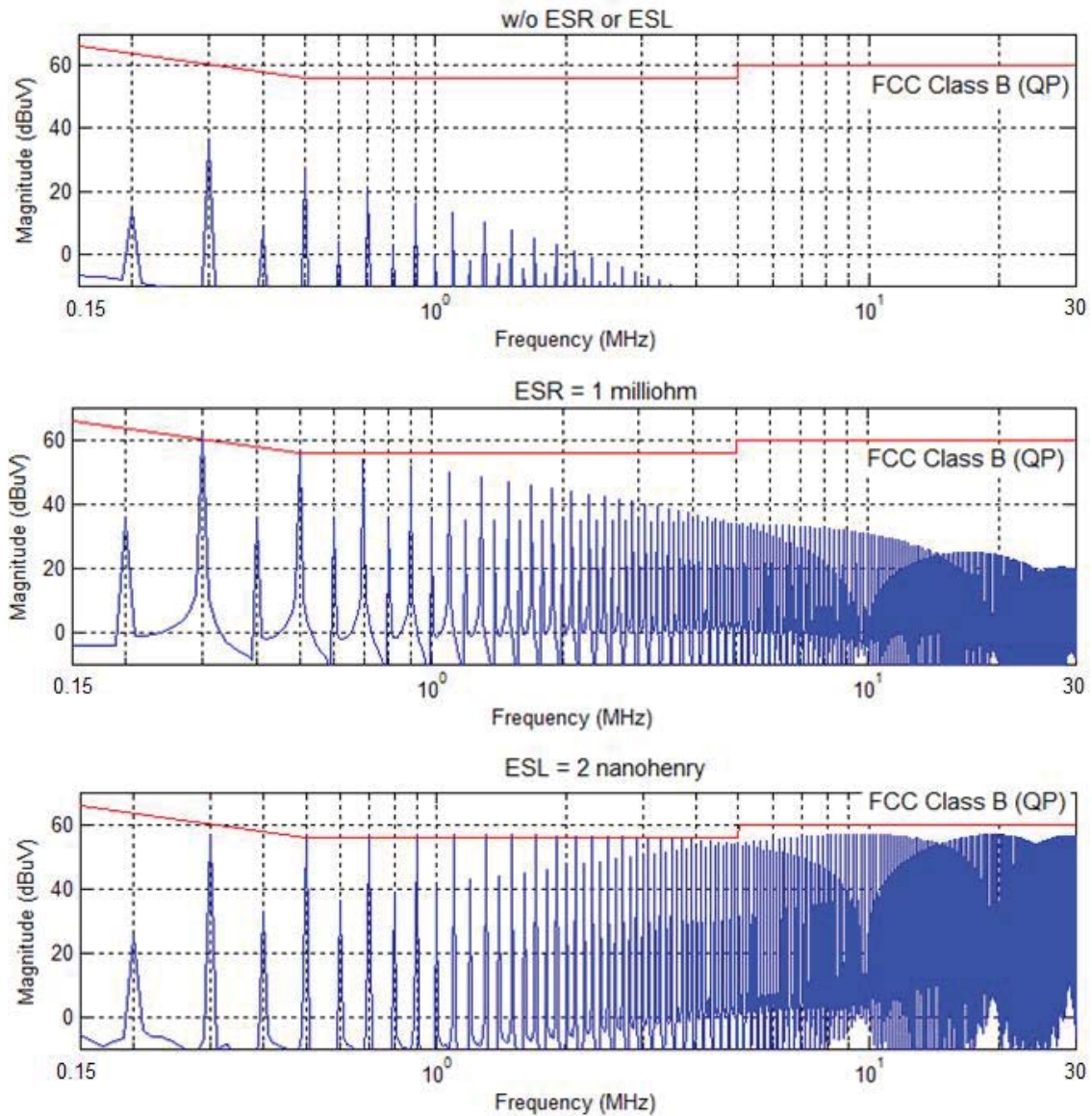


FIGURE 3.4 Effects of ESR and ESL of a filter capacitor.

For a boost converter operating in the continuous current mode, the noise source (harmonics of I_s) is much smaller. For the boost PFC operating in the discontinuous current mode that we discussed in Section 2.2.2, the low frequency noise is large and the ESR of the filter capacitor may cause the converter fail to comply with the EMC regulations.

3.2 CM Conducted Emissions

Parasitic capacitance to ground is usually the main coupling path that contributes to CM conducted emissions in power converters. Three important types of parasitic capacitance that commonly exist in power converters will be discussed. They are:

- I. Parasitic capacitance between thermal pads of the power transistors and the heat sink,
- II. Inter-winding parasitic capacitance in the inductors or transformers, and
- III. Parasitic capacitance between the motor windings and the motor chassis.

3.2.1 Parasitic Capacitance in a Buck Converter

Using the buck converter as an example, the three types of the parasitic capacitances are shown as C1, C2, and C3, respectively, in FIGURE 3.5.

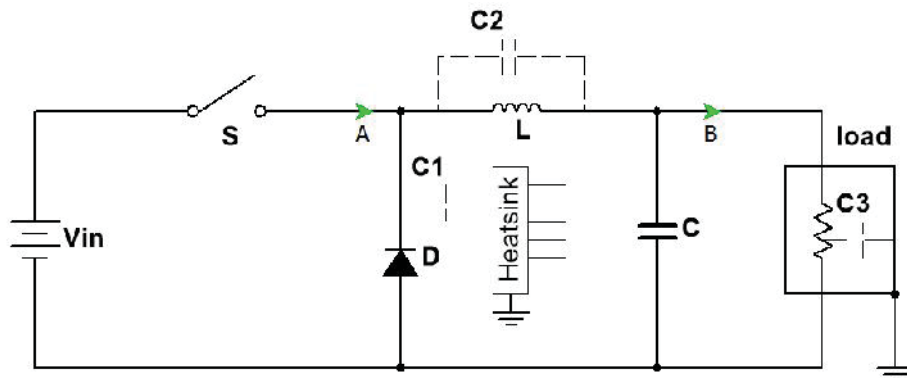


FIGURE 3.5 Model of parasitic capacitances in a buck converter.

Considering only the switching noise at node A , FIGURE 3.5 can be redrawn as the noise source and LISN model shown in FIGURE 3.6, where V_s is the switching noise voltage. FIGURE 3.6 can be further simplified to the model shown in FIGURE 3.7.

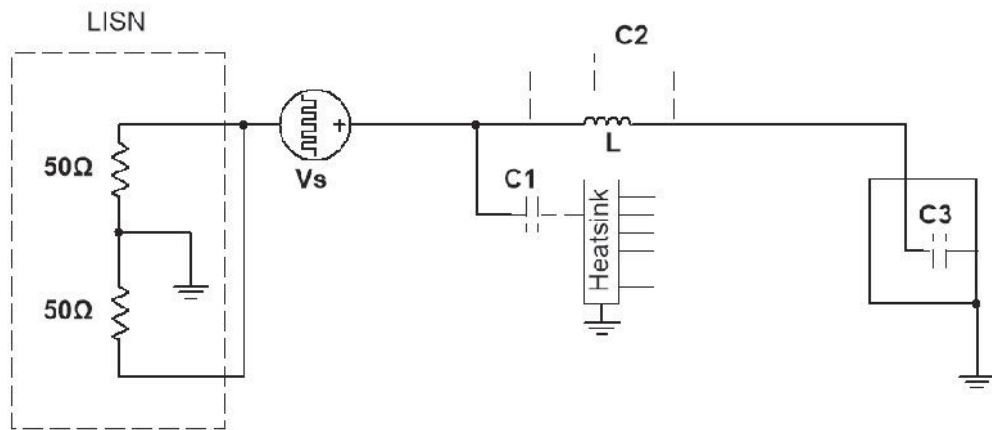


FIGURE 3.6 Model of parasitic capacitances in a buck converter with noise source and LISN.

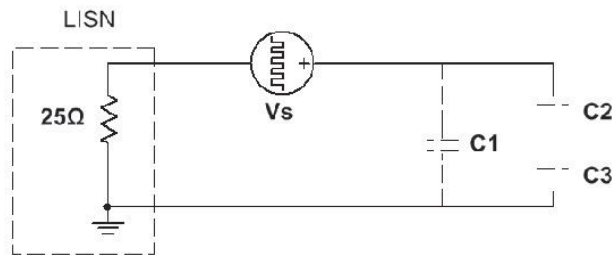


FIGURE 3.7 Simplified model of parasitic capacitances in a buck converter with noise source and LISN.

As shown in the figure, $C1$ is the parasitic capacitance between the power diode thermal pad and the heatsink. In a synchronous buck converter where the power diode is replaced by a power MOSFET or IGBT, $C1$ will be the parasitic capacitance between the drain/emitter of the MOSFET/IGBT and the heatsink. The heatsink is usually bolted to the converter chassis for thermal and safety purposes. (If the heatsink were floated, it could become a shock hazard if the insulation between the transistor and the heatsink broke down.) As a result, $C1$ couples current from the noise source, $V1$, to the ground and results in CM conducted emissions. Since the value of $C1$ is relatively large, this type of parasitic capacitance is usually considered the biggest contributor to the CM conducted

emissions. From the circuit model, the CM conducted emissions, V_{CM} , due to CI can be easily calculated by,

$$V_{CM} = \frac{25}{|25 + 1/j2\pi fCI|} V_s \quad (3.3)$$

where f ranges from 150 kHz to 30 MHz for the FCC test.

The second type of the parasitic capacitance is the inter-winding parasitic capacitance. It makes the inductor look like a capacitor at high frequencies and provides a path for the high frequency noise. In the buck converter, the switching noise is coupled to the load and then to ground through the load parasitic capacitance. In isolated converter topologies, this type of parasitic capacitance exists between the transform windings and couples switching noise from the primary side of the transformer to the secondary side. Increasing the space between the windings can reduce this parasitic capacitance; however, it also increases the volume of the inductor or transformer.

Strictly speaking, the third type of parasitic capacitance is not in the converter. However, it does contribute to the CM conducted emissions in many applications. One example is electric motor drive systems. Since the motor chassis is usually electrically and mechanically connected to the system ground, the parasitic capacitance between the motor windings and the motor chassis can pass PWM noise currents to the chassis ground and cause various EMC problems.

An example of CM conducted emissions in the buck converter is modeled as shown in FIGURE 3.8(a). The filter capacitor in this model doesn't have associated ESR or ESL

in order to excluding the DM conducted emissions. The spectrum of the noise measured by the LISN is shown in FIGURE 3.8(b). At 500 kHz, the magnitude of the harmonic is 124 dB μ V. The FCC class B conducted EMI limit at 500 kHz is 56 dB μ V. From (3.3), we know that the value of the parasitic capacitance, C1, that could make the CM conducted emissions exceed the FCC limit is only 5 pF. FIGURE 3.9 plots the simulated noise received by the LISN with a 5-pF parasitic capacitance. As shown in the figure, the noise level just touches the FCC Class B conducted emissions limit. The parasitic capacitance between the thermal pad of a power MOSFET and the heatsink can range from tens of picofarads to hundreds of picofarads. Thus, without additional effort, the converter will fail to comply with the FCC regulation.

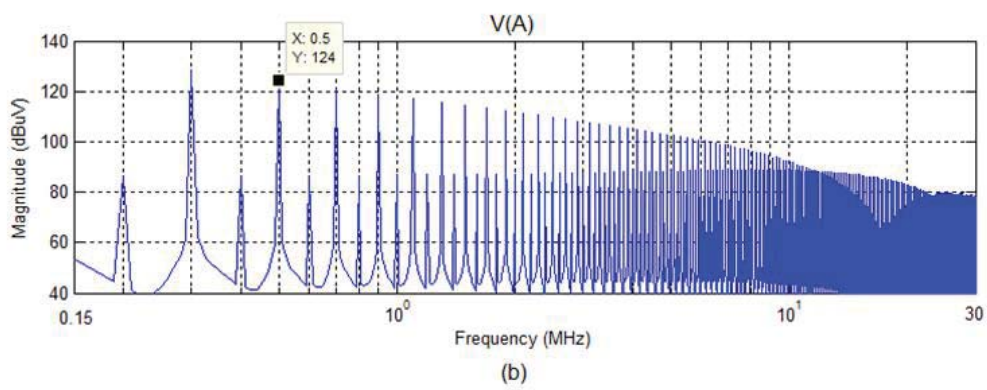
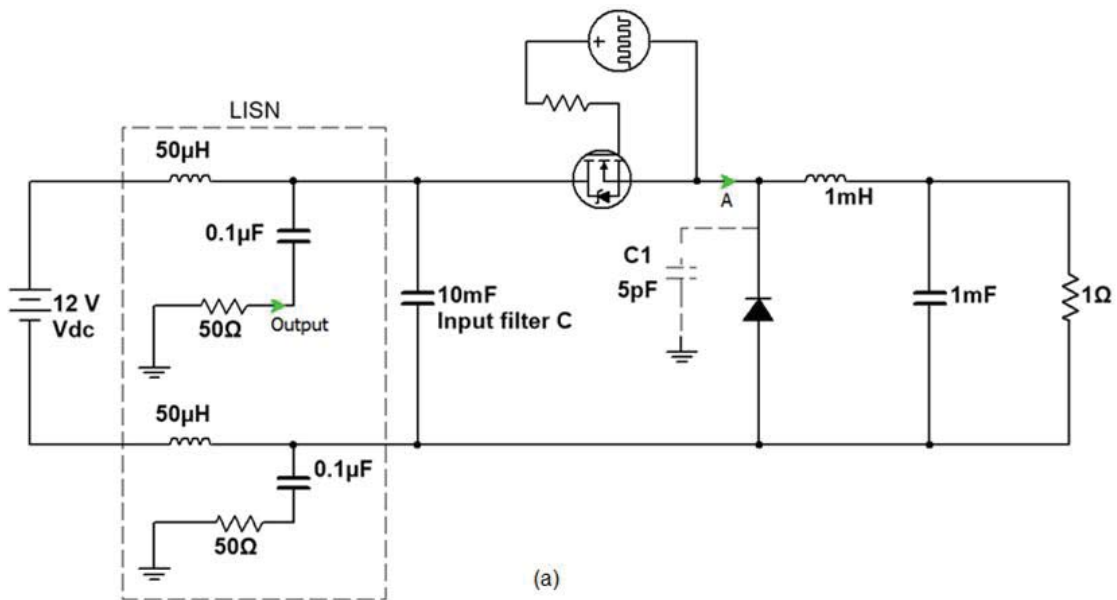


FIGURE 3.8 Buck converter CM conducted emissions example: (a) circuit model, (b) noise spectrum at node A.

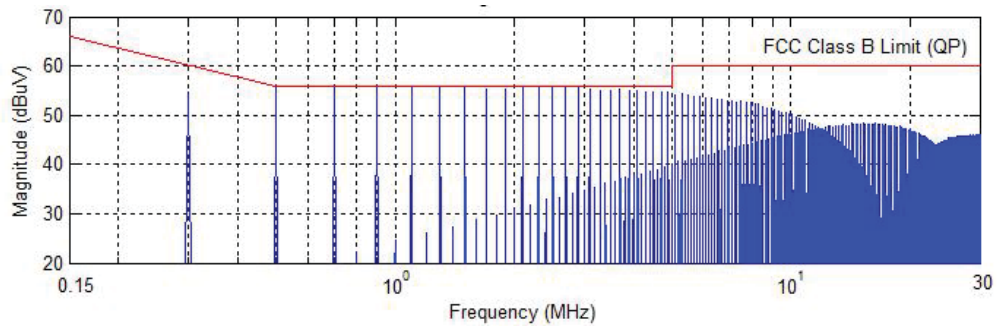


FIGURE 3.9 CM mode conducted emissions with 5pF parasitic capacitance.

3.2.2 Parasitic Capacitance in Other Types of Converters

In an isolated DC-DC converter such as the fly-back DC-DC converter shown in FIGURE 3.10, the parasitic capacitances, through which the CM noise current passes, are similar to those in a buck converter, except that the Type II parasitic capacitance is the parasitic capacitance between the primary and secondary winding of the transformer in the fly-back converter. Note that Type III parasitic capacitance is shorted if the load negative is grounded to the chassis ground as shown in the figure. The switching noise voltage at the drain of the MOSFET generates CM current flowing through C1 and C2 to the chassis ground as shown in the figure.

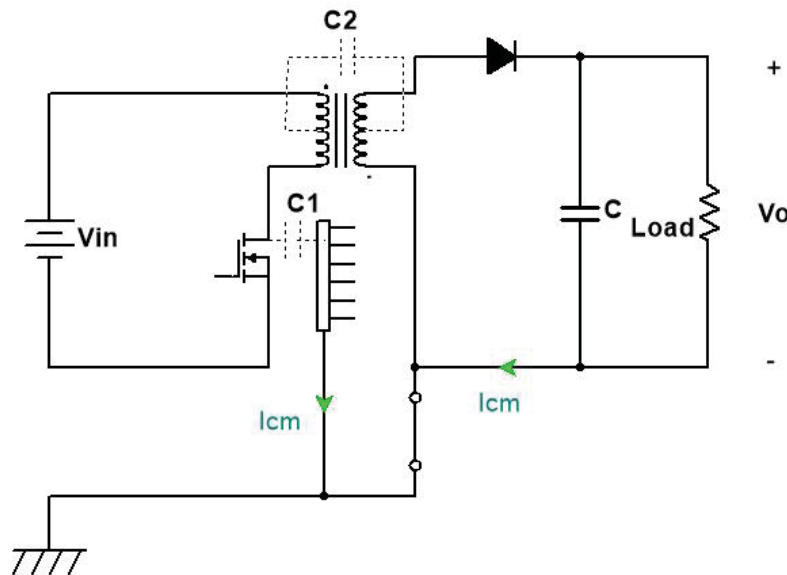


FIGURE 3.10 Model of parasitic capacitances in a flyback converter

In a single phase DC-AC inverter, the three types of parasitic capacitances and the CM current route are shown in FIGURE 3.11. Type I and Type III parasitic capacitances are the same as they were in a buck converter. Noise voltages at the drains of the low side

MOSFETs generate CM current that flows through C1 and C3 to the chassis ground as shown in the figure.

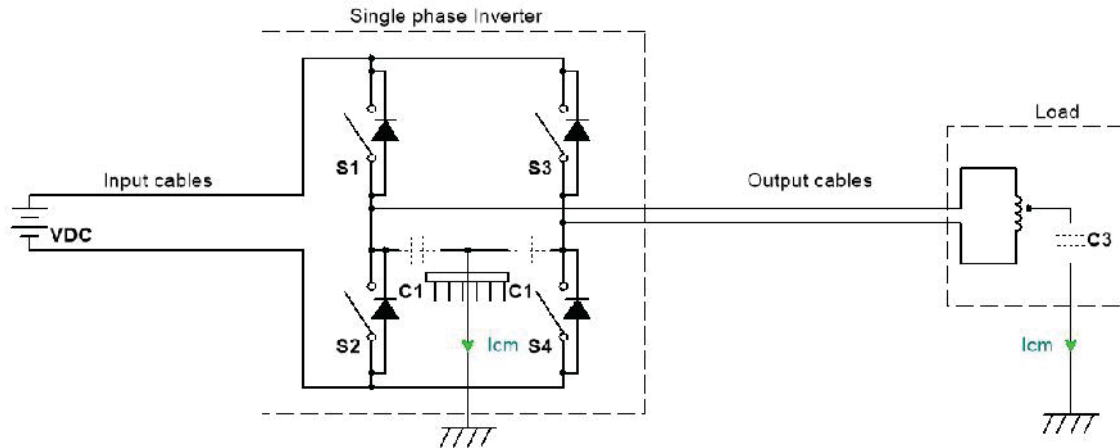


FIGURE 3.11 Model of parasitic capacitances in a single phase inverter

3.3 Radiated Emissions

Noise sources can couple energy through EM radiation and affect nearby or distant systems. This coupling usually requires relatively efficient radiators, such as structures approximating resonant dipole or monopole antennas. In power converters, attached cables are most likely to be the radiators, because the converter circuit board is usually electrically small at the frequencies where the converter noise is strongest. Also, it is mostly likely to be a CM current that causes the radiated emissions if the cables are placed close to each other [6]. Two common radiated emissions mechanisms in power converters occur when a CM voltage drives:

- Attached cables against other electrically large objects, or
- A large cable-chassis loop.

3.3.1 Attached Cables

A power converter PCB layout is illustrated in FIGURE 3.12(a). In this example both input and output have ground connections, and V_o represents the DM output noise. Note that the DM noise voltage cannot radiate efficiently if the output cables are close to each other. As stated earlier, it is usually the CM noise voltage that drives a cable against another electrically large object that causes radiation.

Su and Hubing [7] described a model for determining the CM currents on cables attached to a PCB based on the concept of *imbalance difference*. This model is used here to estimate radiated emissions on the above buck converter. In FIGURE 3.12(a), h_1 , h_2 and h_3 are the imbalance parameters for the part of the board-cable geometry to the left of point a , between points a and b , and to the right of point b , respectively. An imbalance parameter can be defined for any transmission line geometry. It is a number between 0 and 0.5, where a perfectly balanced structure (e.g., two symmetric conductors with identical cross sections) has an imbalance parameter of 0.5. Perfectly unbalanced structures (e.g., a coaxial cable or a trace over an infinite ground plane) have imbalance parameters equal to 0 [7]. As a result, the model in the figure has $h_1 = 0$, $h_3 = 0.5$, and h_2 being between 0 and 0.5. The change in the imbalance at the interconnection can be used to define an equivalent common-mode voltage source. As shown in the figure, there is a change in the imbalance parameter, h , at both ends, a and b , of the output trace. At these two points, CM voltages are generated as shown in FIGURE 3.12(b) and their magnitudes can be calculated by,

$$V_a = (h2 - h1)V_o \quad (3.4)$$

$$V_b = (h3 - h2)V_o \quad (3.5)$$

For microstrip trace structures, the imbalance parameter is given by [7],

$$h = \frac{C_{trace}}{C_{trace} + C_{board}} \quad (3.6)$$

where C_{trace} and C_{board} are the stray capacitances per unit length of the signal trace and the ground plane, respectively. Apparently, $h2$ is very close to zero if C_{board} is much larger than C_{trace} . For the worst case scenario, we assume $h2 = 0$, then V_a will be zero. The model becomes a CM voltage, V_b , driving the input and output cables as shown in FIGURE 3.12(c), assuming the cables are much longer than the length of the PCB. The magnitude of V_b will be half of the DM noise source, according to (3.5).

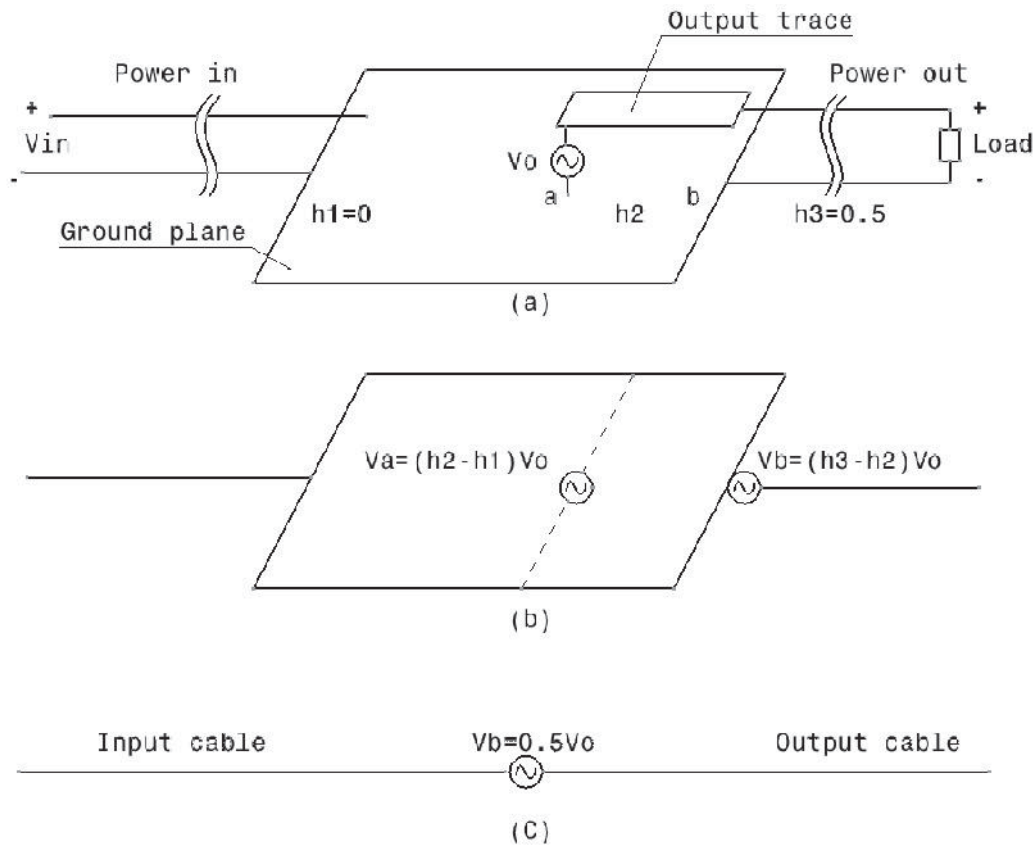


FIGURE 3.12 Imbalance difference model. (a) Trace-board geometry. (b) Equivalent model. (c) Simplified model.

For a DC-DC buck converter, the output DC voltage usually doesn't have radiated emissions problems because the high frequency content of the output can be easily filtered. However, the noise in the output of DC-AC inverters is not easy to filter and thus must be addressed. For example, the single phase inverter shown in FIGURE 3.13 has a trapezoidal DM output waveform similar to that of a three phase inverter, and its spectrum decreases by 20 dB per decade up to the cut-off frequency and 40dB per decade thereafter. Assuming the output power frequency AC voltage has a magnitude of 6 V, and the switching waveform has a rise/fall time of 50 ns, the magnitude of the harmonic at the switching frequency, 20 kHz, will be 6 V, or 135 dB μ V, and the cutoff frequency is at

about 6MHz. Thus the DM noise at 30MHz is about 73 dB μ V. Using the imbalance difference mode, the CM noise at 30 MHz can be estimated as half of the DM voltage, or about 67 dB μ V. If the input and output cable happen to be 2.5 m long, the inverter will become a half-wave dipole at 30 MHz. The resulting maximum electric field can be calculated by [8],

$$|E|_{\max} = 60 \frac{I_{\max}}{r} \quad (3.7)$$

where r is the distance from the inverter and I_{\max} is the peak CM current on the cables. For the dipole antenna, I_{\max} can be found by,

$$I_{\max} = \frac{V_{CM}}{73} \quad (3.8)$$

At $r = 10$ m, the maximum electric field can then be calculated to be 45 dB μ V/m, which is about 15 dB above the FCC class B radiated emissions limit.

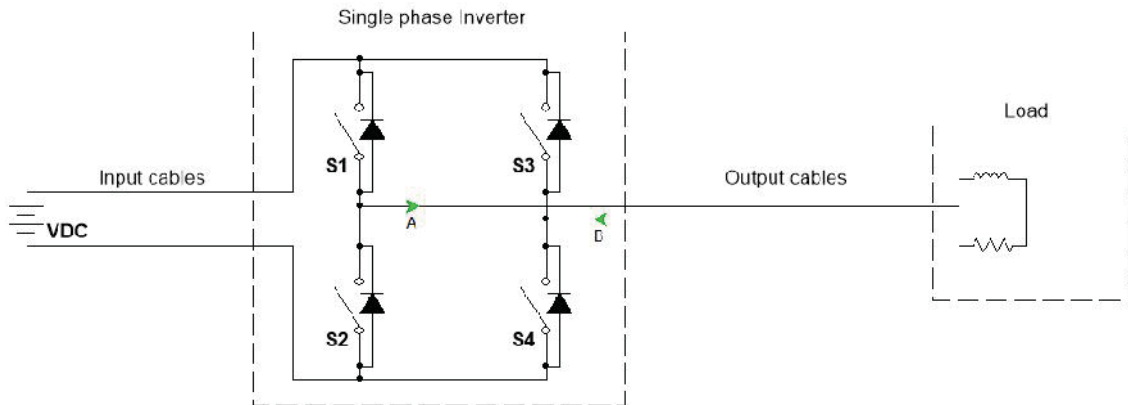


FIGURE 3.13 Single phase DC-AC inverter.

The above example is the worst case scenario for radiation from a cable-inverter configuration. In such cases, it doesn't require a lot of output DM noise to cause the

inverter to fail the FCC radiated emissions test. In real applications, the input voltage may be much higher and the switching faster (shorter rising/falling time, or higher cutoff frequency), which further increases the radiated emissions.

3.3.2 Large Current Loop

If both the inverter and the load are connected to the same chassis ground, a CM current will be generated through the type I and type III parasitic capacitances, as shown in FIGURE 3.14. Assume both parasitic capacitances are 300 pF, and the output cables are 1 m long and 20 cm above a large chassis ground. Using image theory, the current loop is equivalent to a 100 cm \times 40 cm rectangular loop. At 30 MHz, the loop is electrically small and the far field can be calculated from [8],

$$|E|_{\max} = \frac{120\pi^2 I_{\max} A}{r \lambda^2} \quad (3.9)$$

where I_{\max} is the peak current in the loop, r is the distance from the loop, A is the loop area which is 0.4 m², and λ is the wavelength at 30 MHz which equals 10 m. I_{\max} can be found using,

$$I_{\max} = \frac{V_{DM}}{|Z_{C1} + Z_{C4} + R_{rad}|} \quad (3.10)$$

where V_{DM} is the magnitude of the DM output noise source at 30 MHz, which is 73 dB μ V, or 4.5 mV from the previous example. $Z_{C1} + Z_{C4}$ is the impedance of the two parasitic capacitances in series, which is 35 Ω at 30 MHz. R_{rad} is the radiation resistance of the electrically small loop, which can be found by,

$$R_{rad} = \frac{320\pi^2 A^2}{\lambda^4} = 0.05\Omega \quad (3.11)$$

Substituting V_{DM} , $Z_{C1} + Z_{C4}$ and R_{rad} into (3.10), we have $I_{max} = 128 \mu\text{A}$. Then substituting I_{max} into (3.9), at $r = 10 \text{ m}$, the field strength can be calculated to be $60.6 \mu\text{V/m}$, or $35.6 \text{ dB}\mu\text{V/m}$. This is 6 dB above the FCC class B radiated emissions limit.

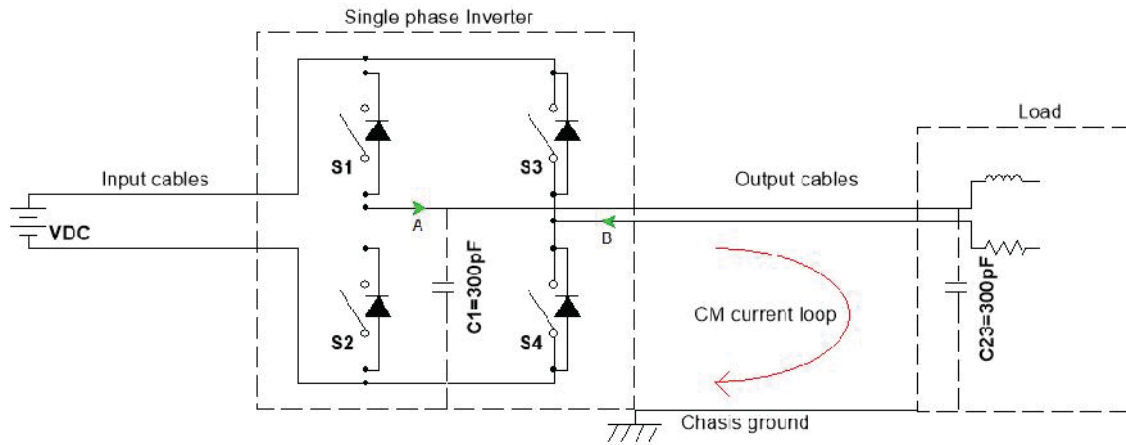


FIGURE 3.14 Single phase DC-AC inverter with chassis ground.

The above example shows the mechanism by which the EM noise is radiated from the CM current loop. As demonstrated in the example, if the parasitic capacitances are large, they could easily cause the inverter to fail to comply with the FCC radiated emissions regulations.

3.4 Near-Field Coupling

The near field usually refers to a distance that is much smaller than a wavelength. For example, the wavelength at 100 MHz is 3 m in free space. Most PCBs for power converters are considered electrically small at that frequency. Thus the coupling from the switching noise to other sensors or devices on the same PCB is considered near-field

coupling. Similarly, at frequencies below 10MHz, the coupling between the converter and sensors or devices several meters away can still be considered near-field coupling. For example, interference between a power inverter on an electric hybrid vehicle and an AM radio in the same vehicle is near-field coupling. There are three types of near-field coupling mechanisms:

- Common impedance coupling,
- Electric field coupling, and
- Magnetic field coupling.

3.4.1 Common Impedance Coupling

FIGURE 3.15 shows two simple circuits sharing a common return path with a finite impedance of R_{RET} . If the source voltage of circuit 2, V_{S2} , is zero, the voltage appearing on the load of circuit 2 due to current in circuit 1 will be $V_{RL2} = I_1 R_{RET}$. Thus the current in circuit 1 affects the load voltage in circuit 2 when the two circuits share a return path. This coupling mechanism is called *common impedance coupling*. Details on calculating common impedance coupling can be found in [9].

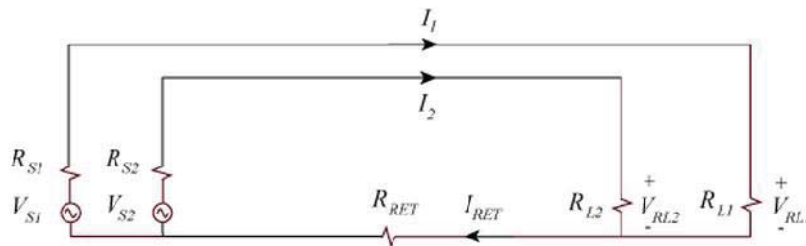


FIGURE 3.15 Common impedance coupling model [9]

Since high current is usually involved in power converters, special care must be taken when laying out the PCB to avoid common impedance coupling. Take the single phase inverter shown in FIGURE 3.16, for example. The inverter controller requires feedback from a sensor at the load, and both the controller and the sensor are referenced to the chassis ground. CM current can cause a potential difference between the inverter chassis ground and load chassis ground due to the finite inductance and resistance of the chassis ground. As a result, the output signal of the sensor will be affected, which may lead to degraded performance or even malfunction of the whole system.

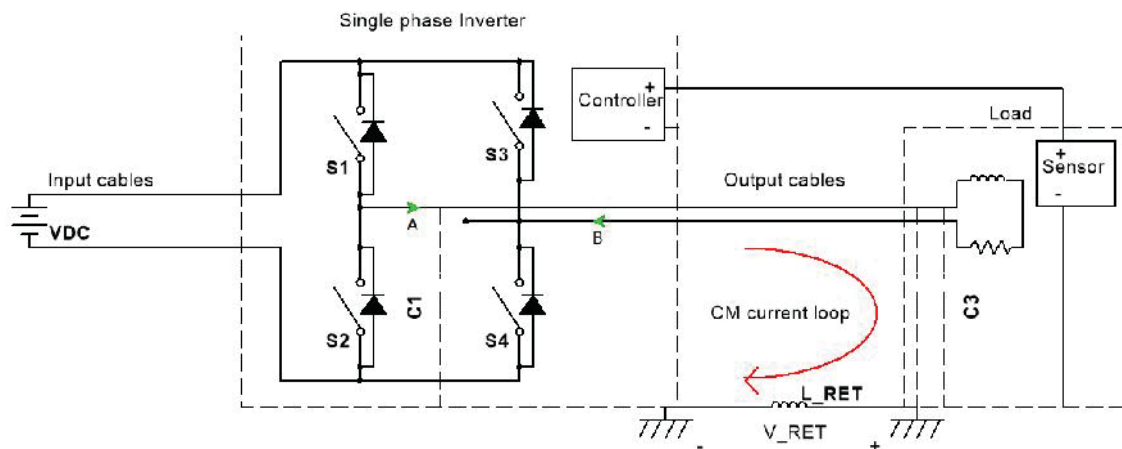


FIGURE 3.16 Common impedance coupling in a single phase DC-AC inverter.

3.4.2 Electric Field Coupling

Electric field coupling occurs when energy is coupled from one circuit to another through an electric field [10]. The coupling path for electric field coupling between two simple circuits can be modeled as a mutual capacitance connecting the two circuits. As shown in FIGURE 3.17, if V_{S2} is zero, a voltage appears on R_{L2} due to V_{S1} because of the coupling path C_{12} . Thus the source voltage in circuit 1 affects the load voltage in circuit 2

due to electric field coupling. Details about calculation of electric field coupling can be found in [10].

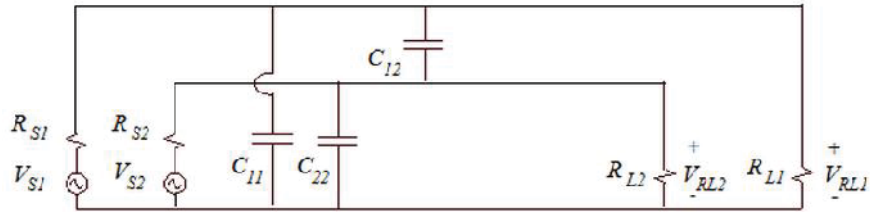


FIGURE 3.17 Capacitive coupling path between two circuits. [10]

In power converters, the switching operation of the power transistors will generate high dv/dt in the circuit. If the trace or wire with high dv/dt is placed close to other sensitive circuits, it can interfere with those sensitive circuits through electric field coupling. FIGURE 3.18 is an example of this coupling mechanism in an inverter. Due to the switching operation, the trapezoidal phase voltage has a very high dv/dt during voltage rise and fall, especially for high voltage applications. If the phase wire is placed close to some I/O wire with critical signals, the mutual capacitance, C_{12} , will be large and it will couple energy from the phase wire to the signal wire, causing problems for the system.

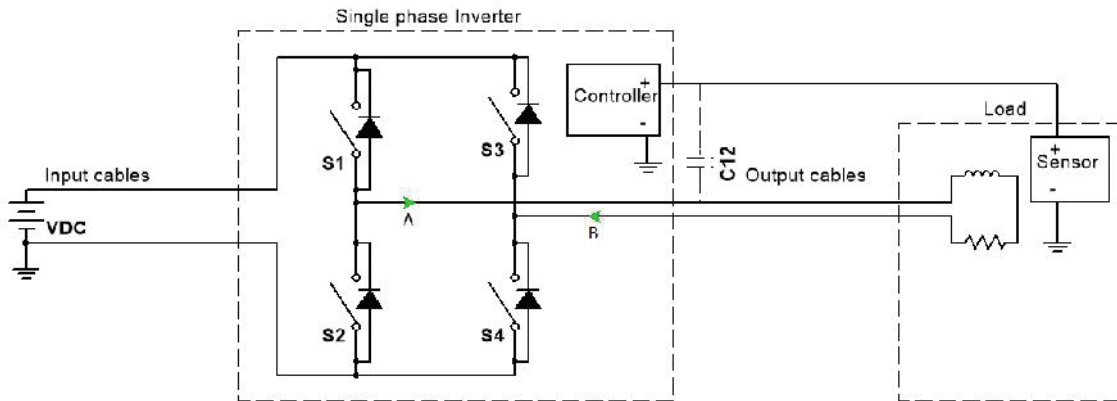


FIGURE 3.18 Electric field coupling in a single phase DC-AC inverter.

3.4.3 Magnetic Field Coupling

Magnetic field coupling occurs when energy is coupled from one circuit to another through a magnetic field [11]. Magnetic field coupling between two simple circuits can be modeled using a mutual inductance. As shown in FIGURE 3.19, if V_{S2} is zero, a voltage appears on R_{L2} due to the current in circuit 1 because of the mutual inductance, M_{12} . Thus the source voltage in circuit 1 produces a load voltage in circuit 2 due to magnetic field coupling. Details about the calculation of magnetic field coupling can be found in [11].

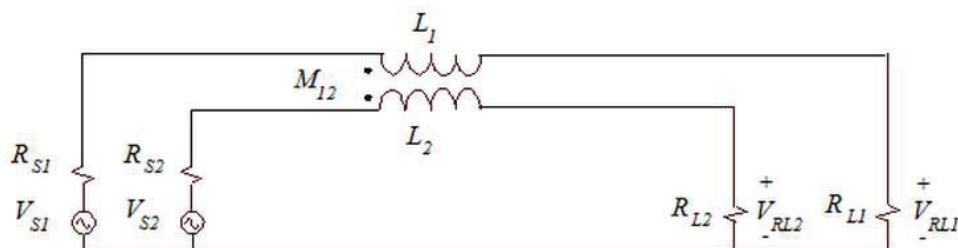


FIGURE 3.19 Magnetic field coupling between two circuits.[11]

In power converters, the switching operation of the power transistors will generate high di/dt in the circuit. If the trace or wire with high di/dt is close to other sensitive circuits, it may couple noise to the circuits through magnetic field coupling. FIGURE 3.20 shows an example of this coupling mechanism in an inverter. Due to the switching operation, the trapezoidal current waveform in circuit loop1 has a very high di/dt during current rise and fall, especially for high current applications. If the circuit loop is placed close to another circuit loop, the mutual inductance, M_{12} , can be very large. This is illustrated in FIGURE 3.20 where loop1 is located close to loop2. For an inverter, the

affected loop could be a MOSFET driver circuit or a voltage/current sensing circuit, both of which are critical to the operation of the inverter.

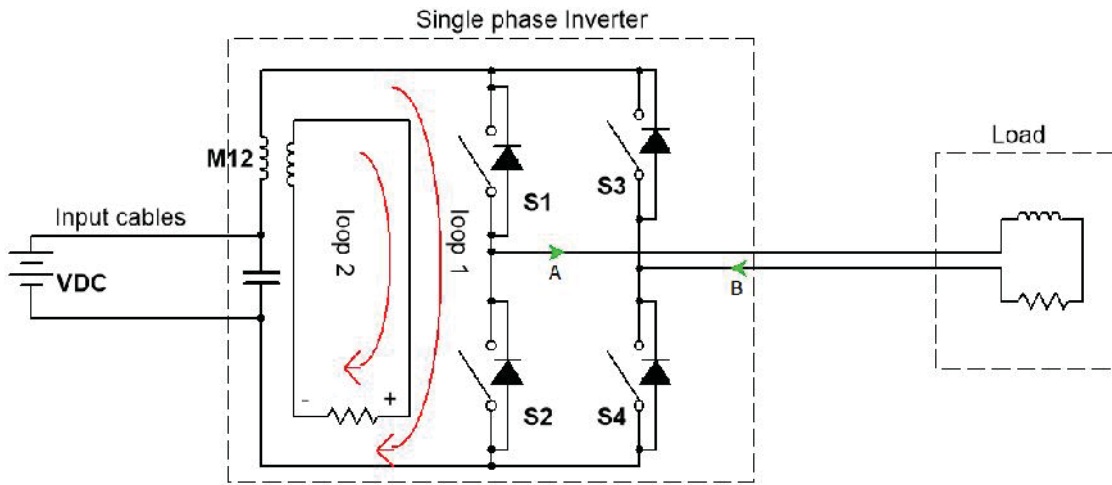


FIGURE 3.20 Magnetic field coupling in a single phase DC-AC inverter.

4. MEASUREMENT

Chapters 2 and 3 discussed how EMI is generated in power converters through various coupling mechanisms. For better EMI mitigation strategy design, it would be helpful to characterize different types of noise source, loads, and coupling paths. It is also important to evaluate a solution for comparison. The most common way to obtain such information is through measurements. This chapter discusses measurements used in EMI mitigation strategy development for power converters.

For noise quantification, 4.1 introduces measurements used for EMC compliance tests, such as conducted and radiated emissions tests. These tests are documented in detail in different standards and regulations, and must be performed with standardized instruments, test setups and test procedures. Obtaining detailed information about the noise source, such as its CM and DM components and its impedance, is the subject of 4.2 and 4.3. To characterize the EMI noise coupling paths, 4.4 introduces a method to extract the key parasitic parameters in power modules used in power converters. Finally, characterization of external filters to predict and evaluate performance is introduced in 4.5.

4.1 EMI Noise Measurement

Although the ultimate motivation of mitigating EMI in power converters is to reduce the risk of problems in real situations, compliance with EMC regulations is usually the main priority. This is because EMC compliance tests are more tangible and consistent; there are clear pass or fail standards. Fortunately compliance with EMC standards does reduce the likelihood of EMI problems in real situations. As a result, EMC compliance

tests are the most common measurements we conduct to determine EMI issues and evaluate EMC solutions. This section uses the EMC compliance test documented in FCC Title 47 Part 15 as an example to introduce a measurement that quantifies the EMI noise level.

4.1.1 Conducted Emissions Test

In a conducted emissions measurement, a Line Impedance Stabilization Network (LISN) is employed to provide consistent test results. An LISN is a device that is placed between the power line and the device under test (DUT), presenting a precise impedance over a designated frequency range during the measurement. The LISN simplifies the measurement of the noise current passing out the power line by converting it to a voltage.

FIGURE 4.1 shows the schematic of an LISN used in the conducted emissions test in FCC Title 47 Part 15. The 50 μH inductor and the 1 μF capacitor form a CL filter, which prevents noise on the power line from entering the DUT and contaminating the measurement. The 0.1 μF capacitor couples the conducted emissions from the DUT to the measuring instrument. Note that the 0.1 μF capacitor has an impedance of 10 Ω to 0.05 Ω in the range of 150 kHz to 30 MHz, which is much smaller than the 50- Ω input impedance of the measuring instrument. The 1-k Ω resistor is used to discharge the capacitors when the LISN is disconnected. The 150 kHz to 30 MHz conducted emissions frequency range is specified by the regulation. Other regulations in different areas for different products may have different frequency ranges and emissions limits. LISN designs could also vary, however, the principle of the LISN of providing a known

impedance for converting noise current to a voltage signal should be the same. The impedance of the DUT port of the LISN in FIGURE 4.1 is plotted in FIGURE 4.2.

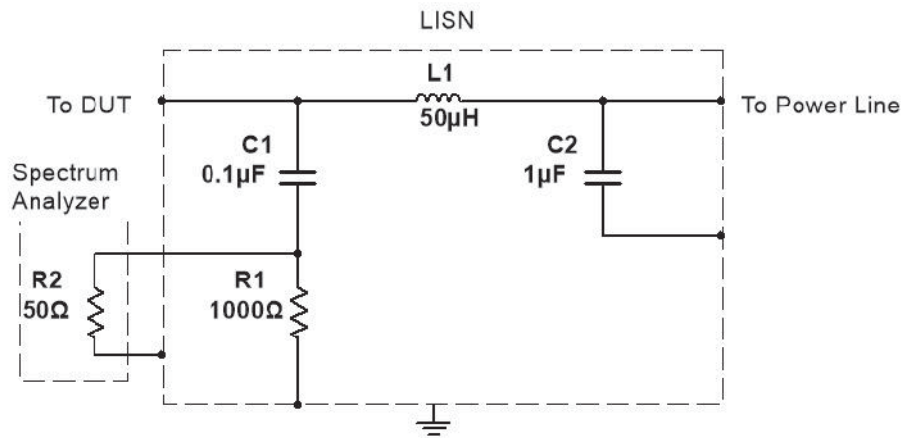


FIGURE 4.1 Schematic of a common LISN.

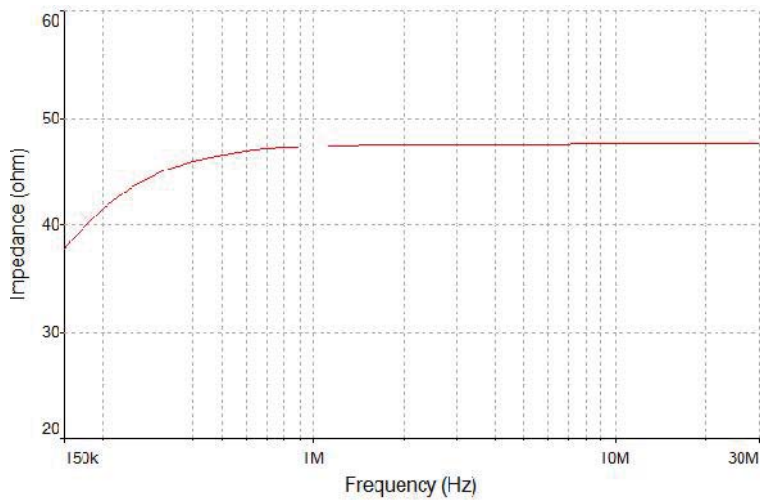


FIGURE 4.2 DUT port impedance of the LISN.

From the plot, we can see that the LISN presents a constant impedance of about 48 Ω from 500 kHz to 30 MHz. For simplicity, the LISN is usually modeled as a 50- Ω impedance over the frequency range of the conducted emissions measurement. Multiple power lines require multiple LISNs.

The voltages across the 50- Ω input resistances of the measuring instrument, v_p and v_n , are recorded to determine the conducted emissions level. Although separation of the DM and CM noises is not required by most regulations, they are extremely important for characterizing the noise and developing noise mitigation strategies. Taking the single phase AC power line for example, the vector form of the conducted noise current on each line, \vec{i}_p and \vec{i}_n can be found by,

$$\vec{i}_p = \frac{\vec{v}_p}{50}, \quad (4.1)$$

$$\vec{i}_n = \frac{\vec{v}_n}{50}. \quad (4.2)$$

The CM and DM conducted noise currents, \vec{i}_{cm} and \vec{i}_{dm} , are given by,

$$\vec{i}_{cm} = \frac{1}{2}(\vec{i}_p + \vec{i}_n) = \frac{1}{100}(\vec{v}_p + \vec{v}_n), \quad (4.3)$$

$$\vec{i}_{dm} = \frac{1}{2}(\vec{i}_p - \vec{i}_n) = \frac{1}{100}(\vec{v}_p - \vec{v}_n). \quad (4.4)$$

(4.3) and (4.4) require both the magnitude and phase information of the two LISN outputs at the same time to calculate the CM and DM noise. As a result, a spectrum analyzer or EMI receiver that doesn't record phase information can't be used to extract the CM or DM noises from the measurement. Separation of the CM and DM conducted emissions will be discussed in 4.2.

4.1.2 Radiated Emissions Test

Radiated emissions tests use antennas to measure the electric field at an open area or in an anechoic chamber. Similar to the LISN in the conducted emissions test, the anechoic chamber shields RF radiation from outside to prevent contamination of the test. It also absorbs RF radiation at the walls inside the chamber to prevent reflection. A tunable half-wave dipole that can be used for sweep-frequency measurements is ideal for the E-field measurement, however, not practical in reality. As a result, antennas with large bandwidths like rod antennas, bi-conical antennas, long-periodic antennas and horn antennas are used for radiated emissions measurements in different frequency ranges.

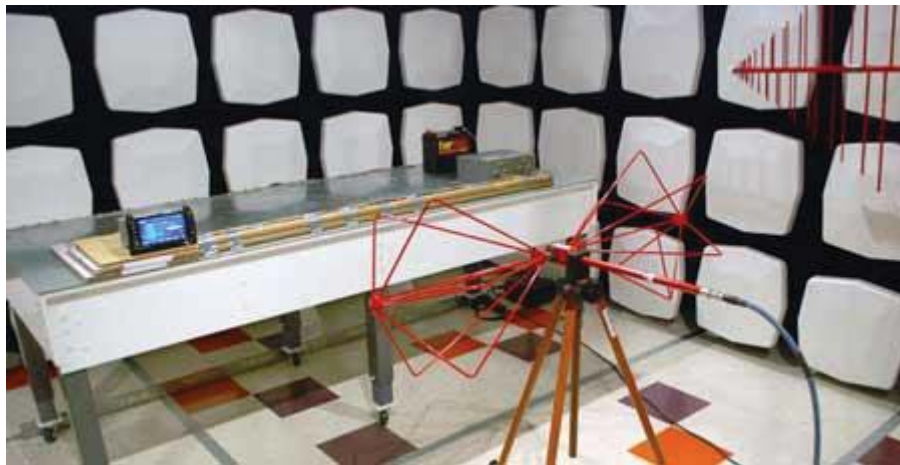


FIGURE 4.3 Radiated emissions test in a semi-anechoic chamber.

4.2 CM and DM Noise Separation

The separated CM and DM noise information is very useful for noise diagnosis and EMI filter design in power converters. However, the standard conducted emissions test does not provide such information. Additional steps can be taken to separate the CM and DM noise.

4.2.1 Vector Spectral Analyzer Measurement

As discussed in 4.1.1, the recorded total conducted emissions in the conducted emissions test, $|v_p|$ or $|v_n|$ is the vector sum or vector difference of the CM and DM noises. (4.3) and (4.4) suggest that the CM and DM noise can be obtained only if we can record both the magnitude and phase of the signal. As shown in FIGURE 4.4, a two-port vector spectral analyzer can be used to obtain \vec{v}_p and \vec{v}_n . Then by using Equations (4.3) and (4.4), the CM and DM noise can be obtained. This method requires more a sophisticated measurement instrument and additional data processing compared to the normal conducted emissions test. Alternatively, a noise separator can be designed for easier CM and DM conducted noise measurement.

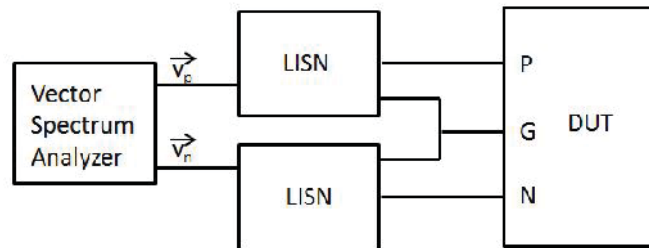


FIGURE 4.4 CM DM noise separation using a two-port vector spectrum analyzer.

4.2.2 CM and DM Conducted Noise Separator

In practice, it is more convenient to use a noise separator with the LISN to separate the CM and DM conducted emissions, because except for the separator, the same instruments for the conducted emissions test can be used and there is no additional data processing required after the measurement. FIGURE 4.5 shows the noise separator used in the conducted emissions measurement. It is usually a three-port system with two input

ports connected to the LISN outputs and one output port connected to a spectrum analyzer. The output of the noise separator is designed to be either $|(v_p - v_n)/2|$ for DM noise measurement or $|(v_p + v_n)/2|$ for CM noise measurement. Also, 50-Ω input impedances for both input ports that are independent of the noise source are required. Let the two input ports and one output port of the noise separator be defined as Ports 1, 2 and 3, respectively. Then the S parameters of the system should have S11, S22, S12 and S21 as small as possible and S31 = S32 = 0.5. S31 and S32 should be out of phase for the DM noise measurement, and be in phase for CM noise measurement.

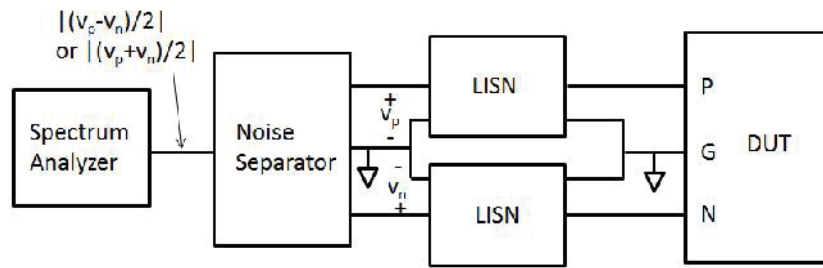


FIGURE 4.5 Noise separator used with LISN.

FIGURE 4.6 is an example of the noise separator proposed in [12]. As shown in the figure, by toggling the DM-CM switch, the polarity of the primary winding of the upper transformer can be changed. For DM measurement, the DM-CM switch is toggled into the position that makes the upper half circuit and the lower half circuit symmetrical. The voltage across the 50-Ω spectrum analyzer input will be $|\overline{v_1} - \overline{v_2}|$. For CM noise measurement, the DM-CM switch is in the opposite position so that the voltage received by the spectrum analyzer is $|\overline{v_1} + \overline{v_2}|$. Two 82-Ω resistors are located in parallel with the transformers so that the input impedances of port 1 and port 2 is around 50 Ω.

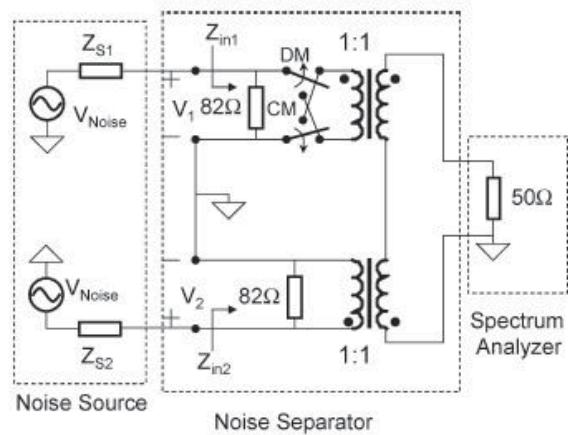
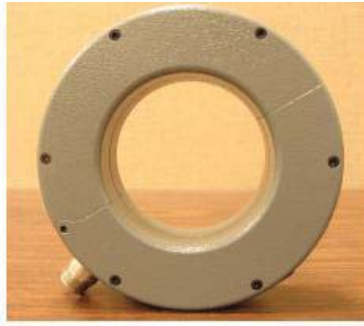


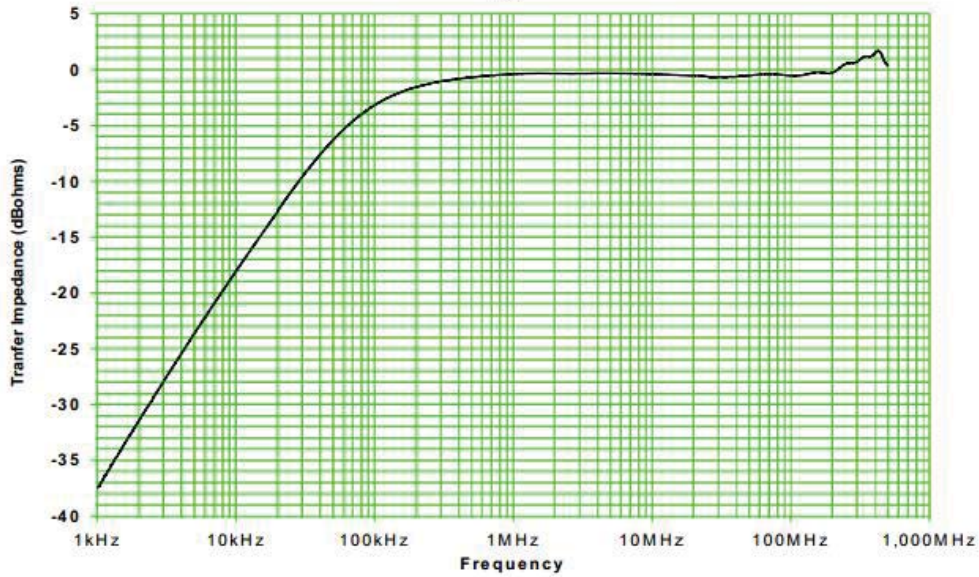
FIGURE 4.6 Noise separator proposed in [12].

4.2.3 Current Probe Measurement

A current probe measures the current that penetrates a surface by measuring the magnetic field induced around the contour of the surface that the current penetrates, which is basically an application of Ampere's law. The induced magnetic field then induces a voltage on the wire winded around the contour according to Faraday's law (I don't understand this sentence). Since the relation between the current to be measured and its induced magnetic field, and the relation between the magnetic field and its induced voltage are well defined by Ampere's law and Faraday's law, by recording the voltage, we can find the current. FIGURE 4.7 (a) shows a current probe made by Fischer Custom Communications. To measure current, the probe is simply clamped on all relevant cables and connected to a spectrum analyzer or oscilloscope for frequency or time domain measurements. The transfer impedance of this probe is shown in FIGURE 4.7(b) [13].



(a)



(b)

FIGURE 4.7 Current probe, (a), probe, (b), transfer impedance plot. [13]

For conducted CM and DM noise separation, first we measure the CM noise by clamping the current probe on the cable bundles which contain the CM noise. After the CM noise current, $|i_{cm}|$, is measured, we place the current probe on an individual cable and measure the current, $|i_p|$ or $|i_n|$. The DM noise current can then be found by,

$$|i_{dm}| = \left| |i_p| - |i_{cm}| \right|, \text{ or} \quad (4.5)$$

$$|i_{dm}| = \left| |i_n| - |i_{cm}| \right|. \quad (4.6)$$

4.3 Impedance Measurement

Besides quantifying and separating EMI noise sources, knowledge of the impedances of the noise source and the load is also essential to a good EMI solution. As discussed in Chapter 3, in the switched-mode power converters, the noise source impedance depends on its coupling mechanism. For example, the CM noise source impedance of a synchronous buck converter is mainly dependent on the parasitic capacitance between the switching semiconductors and the converter chassis (FIGURE 3.7), while its DM noise source impedance depends on the ESR and ESL of the X capacitor (FIGURE 3.2). For the load impedance, different load types (LISN, electric motor, etc.) and noise types (CM, DM) should be treated individually. These impedances are usually obtained through measurements.

4.3.1 Source Impedance

At high frequencies, or the EMI frequency range, the noise source impedance of the switched-mode power converters can be considered independent of switch states (on or off). Ignoring thermal effects, an easy way to estimate the source impedances is by powering off the converter and using an impedance analyzer to measure its input impedances. FIGURE 4.8 shows an example of measuring the DM and CM noise source impedances of the conducted emissions. By connecting the impedance analyzer port to the PG (or NG) port, and PN-G port, the DM and CM source impedances can be measured, respectively.

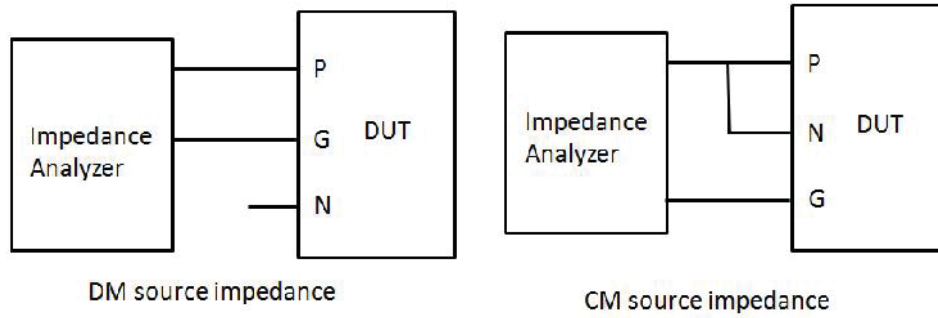


FIGURE 4.8 Source impedance measurements with an impedance analyzer.

Perez, etc. [14] introduced a method to measure the source impedances of the conducted emissions when the converter is powered on, using LISNs and a vector network analyzer. As shown in FIGURE 4.9, the conducted emissions of the power converter can be modeled as a three-impedance network with two voltage sources connected to the P and N terminals. To measure Z_1 , Z_2 and Z_3 , a network analyzer is connected to the LISN outputs, as shown in FIGURE 4.10. The S parameters of the power converter can be obtained from de-embedding the LISN from the measurement. Z_1 , Z_2 and Z_3 can be calculated by,

$$Z_1 = \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0S_{12}S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21} - 2S_{21}}, \quad (4.7)$$

$$Z_2 = \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0S_{12}S_{21}}{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{12}}, \quad (4.8)$$

$$Z_3 = \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0S_{12}S_{21}}{S_{12} + S_{21}}, \quad (4.9)$$

where S_{11} through S_{22} are the de-embedded S parameters of the converter, and Z_0 is the input impedance of the VNA. Note that, the noise level, V_1 and V_2 , must be negligible compared to the power output of the vector network analyzer.

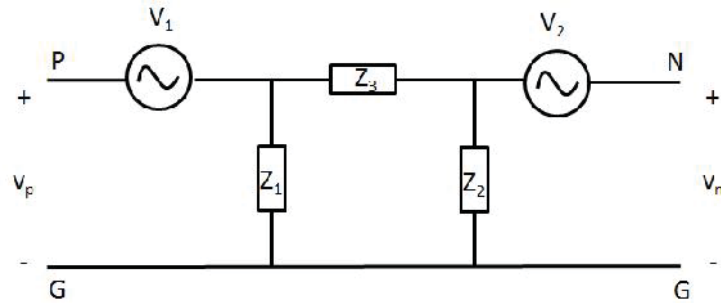


FIGURE 4.9 Three-impedance network of power converters.

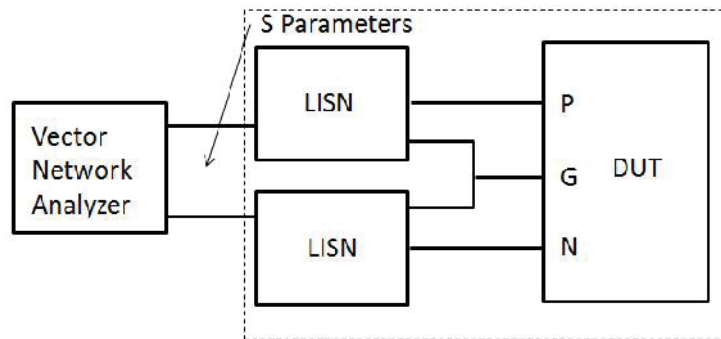


FIGURE 4.10 Characterizing power converters with a vector network analyzer.

The next step is to convert Z_1 , Z_2 and Z_3 into the CM and DM noise impedances, Z_{CM} and Z_{DM} . FIGURE 4.11 shows the model of the power converter in terms of the CM and DM sources and impedances. Their values can be found by,

$$Z_{CM} = \frac{2Z_1Z_2}{Z_1 + 3Z_2} \quad (4.10)$$

$$Z_{DM} = \frac{4Z_1Z_2Z_3}{4Z_1Z_2 + 3Z_2Z_3 - Z_1Z_3} \quad (4.11)$$

$$Z_{TM} = \frac{2Z_1Z_2}{Z_1 - Z_2} \quad (4.12)$$

Z_{TM} determines the conversion between the CM and DM noise. (4.12) indicates that for a perfectly balanced system where $Z_1 = Z_2$, Z_{TM} is infinity and there will be no conversion between CM and DM conducted noises.

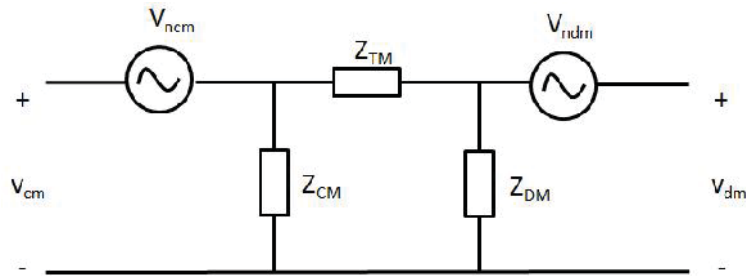


FIGURE 4.11 CM-DM network model of power converters.

Although additional data processing is involved, this method provides a direct way to measure the noise source impedances of the power converters while they are under normal operating conditions.

4.3.2 Load Impedance

LISN

The actual power line is the load for the conducted emissions. Since its impedance is not consistent, the impedance of the LISN is usually used instead. Often making sure the power converter complies with EMC regulations is a priority in EMC designs. As discussed in Chapter 3, the CM and DM impedances of the LISN are 25 Ω and 100 Ω , respectively.

Electric motor

Another common load type is the electric motor at the converter output. Similar to measuring the source impedance when the converter is powered off, an impedance analyzer can be used to measure the CM and DM impedances of the motor, as shown in FIGURE 4.12.

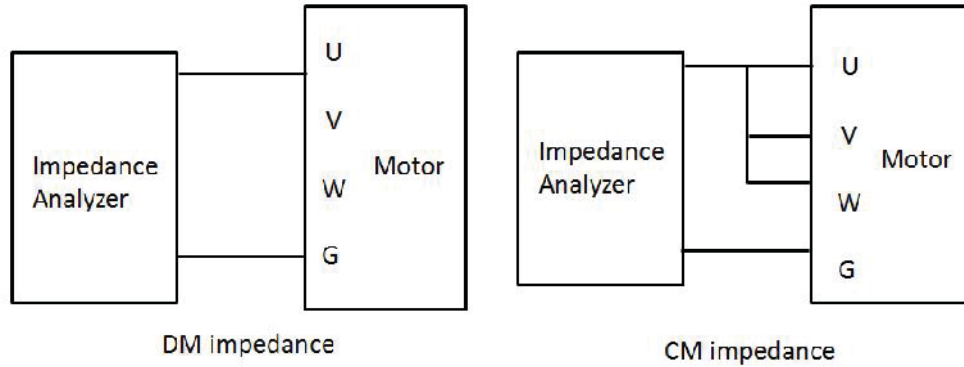


FIGURE 4.12 Motor impedance measurements with an impedance analyzer.

FIGURE 4.13 shows the CM and DM impedances of an IPM motor [15]. The CM impedance is mainly the parasitic capacitance between the stator winding and the motor housing. The DM impedance is the inductance of the stator winding at low frequencies, and above 500 kHz, the inter-winding capacitance dominates DM impedance.

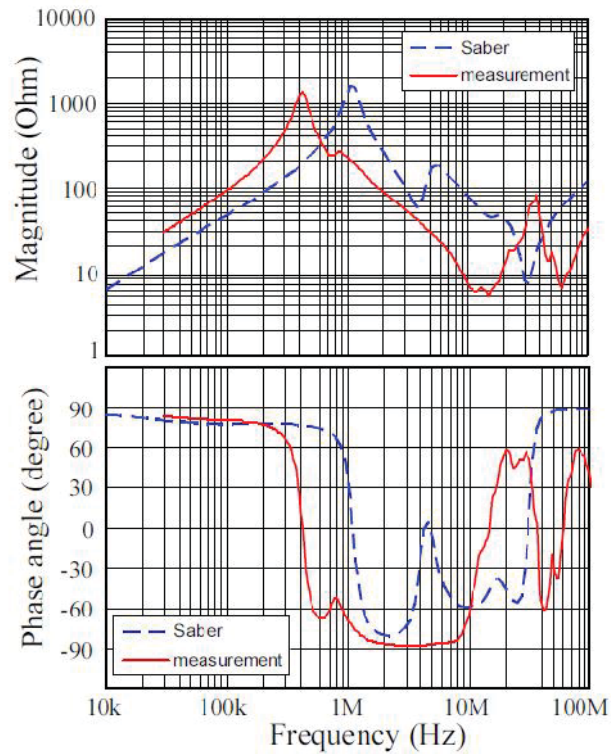
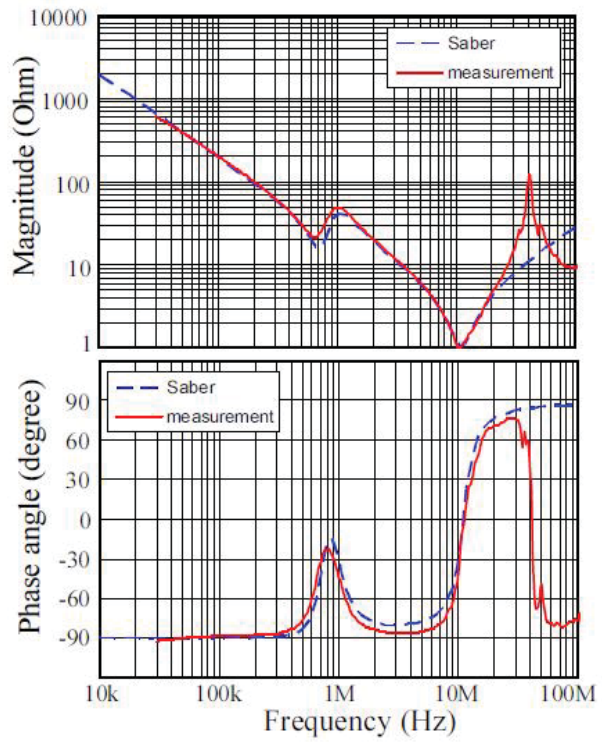


FIGURE 4.13 IPM motor impedances. [15]

This measurement is conducted when the IPM motor is sitting still. Note that when the rotor of the motor is at a different angle, the DM impedance at low frequencies will be different because the mutual inductance between stator and rotor windings is different. However, this doesn't affect the impedance measurement at high frequencies, where the parasitic capacitances dominate.

4.4 Parasitic Parameters Extraction

In 2.3, we discussed the parasitic parameters in the synchronous buck converter that affect the ringing in the noise waveform. In 3.2, we discussed the main CM noise coupling path which is parasitic capacitors in the power module. Later, we will introduce methods of EMI reduction that rely on the knowledge of the parasitic parameters. In this section, we will introduce a method for extracting the parasitic parameters in power modules.

FIGURE 4.14 shows the Integrated Power Electronics Module (IPEM) that is found in many power converters. The IPEM is gaining popularity because it is an off-the-shelf module with wide applications, including motor drives. As shown in the figure, the parasitic parameters of interest are the loop inductances, L_p , L_{o1} , L_{o2} , and L_n , and the parasitic capacitances between the terminals and the module housing, C_p , C_o , and C_n . As discussed in 2.3 and 3.2, the ringing waveform is affected by $L di/dt$ and the CM conducted emissions are due to $C dv/dt$. We want to find the value of these parasitic parameters.

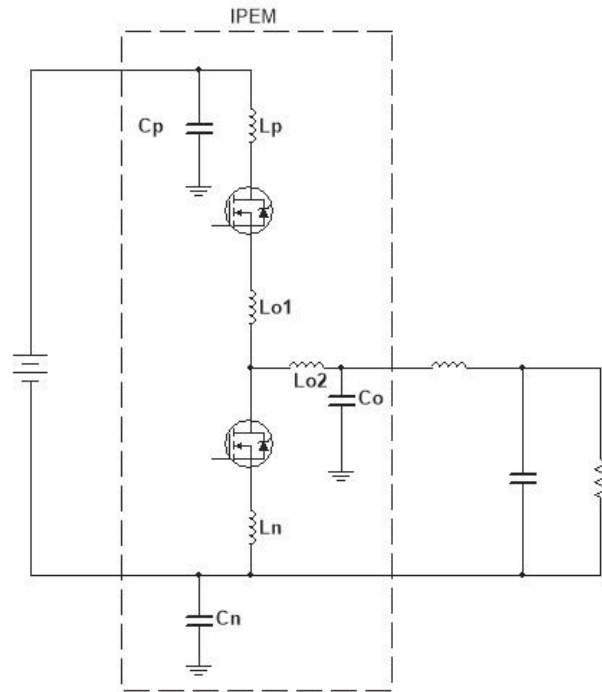


FIGURE 4.14 IPEM model used in a synchronous buck converter.

Methods that use software to extract the parasitic parameters can be found in [16]–[18]. These methods require detailed geometrical information about the structure of the IPEM, which may not be available in some cases. As a result, a method to extract the parasitic parameters based on measurements [19] will be introduced here.

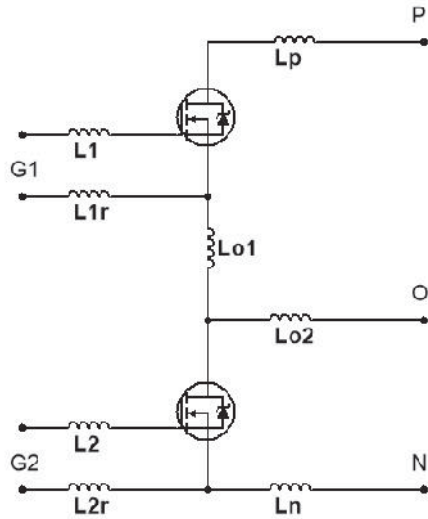


FIGURE 4.15 Partial inductances in an IPEM.

FIGURE 4.15 shows the partial inductances, L_p , L_{o1} , L_{o2} , and L_n , that we want to extract. Assuming the resistances are negligible, the following steps can be taken to extract these parameters:

Step 1. Apply gate voltage on G1 and measure the impedance between P and O to obtain $L_p + L_{o1} + L_{o2}$.

Step 2. Apply gate voltage on G2 and measure the impedance between O and N to obtain $L_{o2} + L_n$.

Step 3. Apply gate voltages on both G1 and G2 and measure the impedance between P and N to obtain $L_p + L_{o1} + L_n$.

Step 4. Measure the impedance between P and G1 to obtain $L_1 + L_p$.

Step 5. Measure the impedance between O and G1 to obtain $L_1 + L_{o1} + L_{o2}$.

From the five equations obtained in Steps 1 through 5, the values of the partial inductances in an IPEM, L_p , L_{o1} , L_{o2} , and L_n , can be calculated.

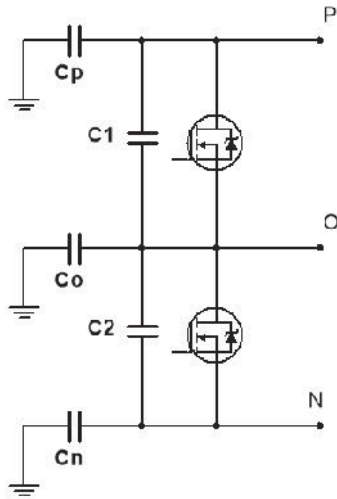


FIGURE 4.16 Parasitic capacitances in an IPEM.

Next, we will need to extract the parasitic capacitances. FIGURE 4.16 shows the parasitic capacitances C_p , C_o and C_n , between terminals P, O, N, respectively, and the IPEM chassis. The following steps can be taken to obtain C_p , C_o and C_n :

Step 1. Measure the total capacitance, $C_p + C_o + C_n$, by shorting the three terminals.

Step 2. Measure C_p using the setup shown in FIGURE 4.17(a).

Step 3. Measure C_n using the setup shown in FIGURE 4.17(b).

Step 4. Subtract measured C_p and C_n from the measured total capacitance in Step 1 to obtain C_o .

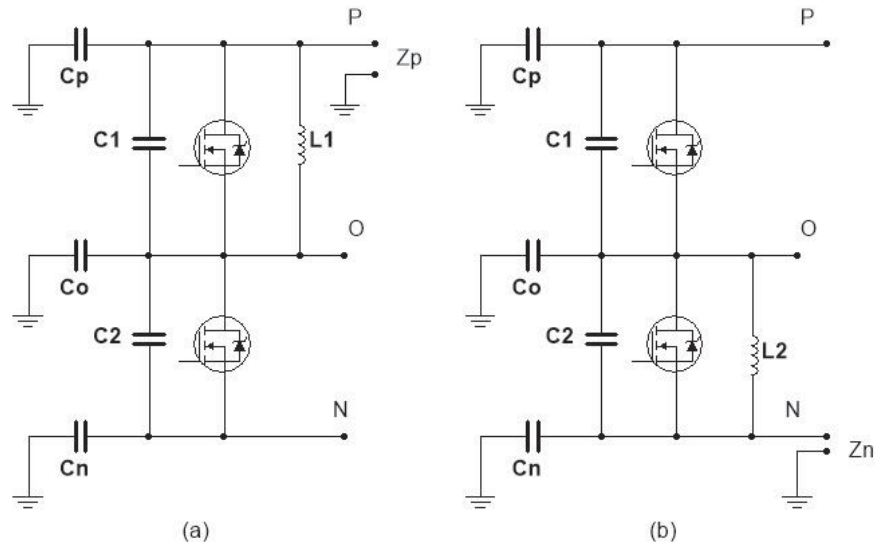


FIGURE 4.17 Setup for C_p and C_n measurements.

The setup in FIGURE 4.17(a) shows an inductor with a known value, L_1 , in parallel with C_1 , so that when L_1 and C_1 hit the resonant frequency, they can be seen as an open circuit. At this resonant frequency, the measured impedance between port P and the IPPEM chassis, Z_p , reflects only the value of C_p . In the measurement, the impedance is recorded over a frequency range and the peak value is picked to calculate C_p . The same method is used to measure C_o using the setup in FIGURE 4.17(b).

Although many steps and additional calculations are involved in this method, it provides an alternative way for the extracting the parasitic parameters when the internal structure of the power electronics module is not available.

4.5 Filter Characterization

4.5.1 Insertion Loss

To evaluate an EMI solution, such as an EMI filter, the concept of Insertion Loss (IL) is very useful. IL is defined as a ratio of the signal level without the filter to the signal level with the filter implemented, and can be expressed as,

$$IL = \frac{|V_1|}{|V_2|}, \text{ or} \quad (4.13)$$

$$IL(dB) = 20 \log_{10} \frac{|V_1|}{|V_2|}. \quad (4.14)$$

V_1 and V_2 are the noise levels without and with the filter implemented, respectively, as shown in FIGURE 4.18. The EMI solution should have its IL maximized in the EMI noise frequency range and minimized in the power frequency range of the power converter.

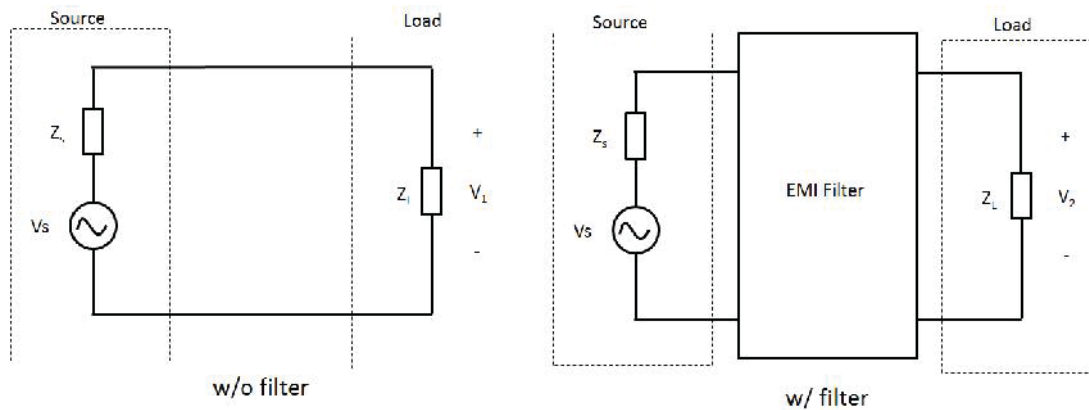


FIGURE 4.18 Insertion loss of a filter.

To measure the IL of an EMI filter, we measure the noise level of the converter with the filter installed, and compare the result with the noise level of the converter without the filter installed. For example, we can use the LISN to measure the conducted emissions of a power converter, as described in 4.1.1, with and without a filter, and apply (4.13) or (4.14) to calculate the IL of the filter.

4.5.2 Filter Characterization

For an external filter, assuming the noise source and the load impedances are already known, the IL of the filter can be obtained without installing the filter onto the converter. Using a two-port filter as an example, two steps are required to obtain the IL of a filter using this method:

Step 1. Measure the S parameters of the filter using a VNA, as shown in FIGURE 4.19.

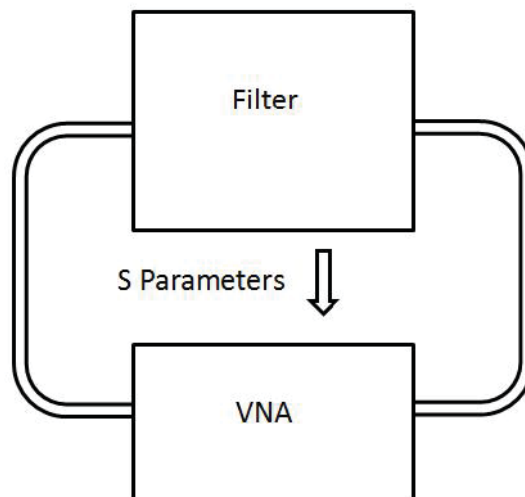


FIGURE 4.19 Filter characterization with VNA.

Step 2. Calculate the IL of the filter using the measured S parameters from Step 1 by,

$$IL = \frac{Z_L}{Z_s + Z_L} \left[\frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} + \frac{Z_0}{Z_L} \frac{(1 + S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \right. \\ \left. + \frac{Z_s}{Z_0} \frac{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} + \frac{Z_s}{Z_L} \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \right] \quad (4.15)$$

where S_{11} , S_{12} , S_{21} and S_{22} , are the S parameters of the filter, Z_s and Z_L are the source and load impedances, respectively, and Z_0 is the input impedance of the VNA, which is usually 50Ω .

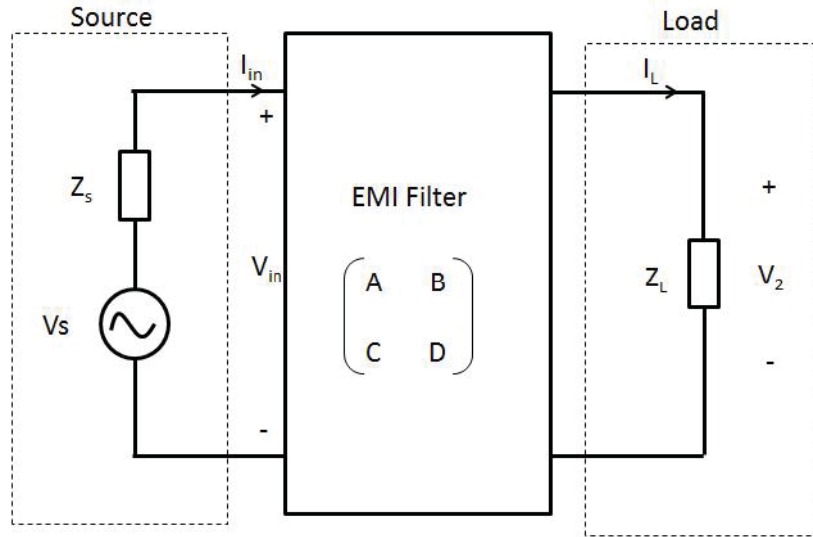


FIGURE 4.20 Noise model with the filter represented by an ABCD matrix.

S parameters are easy to measure with the VNA, thus are used for the IL measurement. For circuit analysis purposes, we will use the ABCD matrix to derive (4.15) here. FIGURE 4.20 shows the noise model with the EMI filter represented by an ABCD matrix. The input voltage and current, of the filter, V_{in} and I_{in} , can be represented by,

$$V_{in} = A \cdot V_2 + B \cdot I_L = A \cdot V_2 + B \cdot \frac{V_2}{Z_L} , \quad (4.16)$$

$$I_{in} = C \cdot V_2 + D \cdot I_L = C \cdot V_2 + D \cdot \frac{V_2}{Z_L} . \quad (4.17)$$

At the source end, applying KVL, we have,

$$V_s - I_{in} Z_s - V_{in} = 0 . \quad (4.18)$$

Combining (4.16), (4.17) and (4.18), the noise level of the DUT with the filter, V_2 , can be represented by,

$$V_2 = V_s \frac{1}{A + \frac{B}{Z_L} + CZ_s + \frac{DZ_s}{Z_L}} . \quad (4.19)$$

From FIGURE 4.18, the noise level of the DUT without the filter, V_1 , can be calculated by,

$$V_1 = V_s \frac{Z_L}{Z_s + Z_L} . \quad (4.20)$$

Combining (4.13), (4.19) and (4.20) gives,

$$IL = \frac{A \cdot Z_L + B + C \cdot Z_s Z_L + D \cdot Z_s}{Z_s + Z_L} . \quad (4.21)$$

Since the S matrix can be converted from the ABCD matrix by,

$$\begin{aligned}
A &= \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \\
B &= Z_0 \frac{(1 + S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}} \\
C &= \frac{1}{Z_0} \frac{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \\
D &= \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}}
\end{aligned} \tag{4.22}$$

we can substitute (4.22) into (4.21), to arrive at (4.15) .

(4.15) and (4.21) are very useful in filter designs. With the known source and load impedances, the filter performance can be estimated using these equations.

5. PASSIVE FILTERS

Passive filters are commonly used to help ensure EMC compliance in power converters. As the name implies, these filters use only passive components. The simple LC filters that we are familiar with, and the relatively complicated high-order Cauer-Chebyshev filters both belong to this category. Specific passive filter designs for power inverters can be found in [20] and [21]. This chapter introduces the passive filter in power converters in order to compare them to active filter technologies that will be introduced later.

5.1 Passive Filters in Power Converters

The noise source and the coupling mechanism in power converters are represented by the simple models in FIGURE 5.1. As shown in the figure, for conducted emissions, a Line Impedance Stabilization Network (LISN) is used to represent the load. Its impedance is 25Ω and 100Ω for CM and DM models, respectively. The converter output load depends on the actual application.

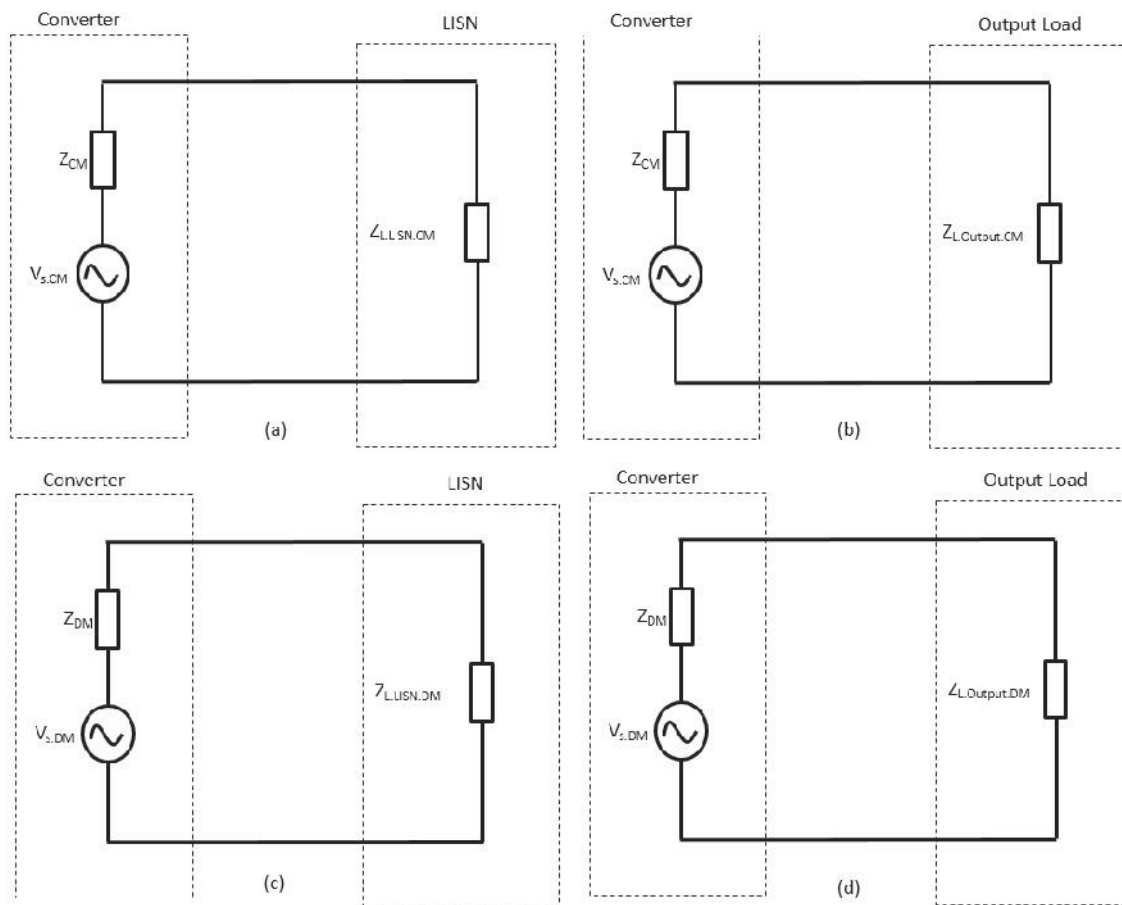


FIGURE 5.1 EMI noise models in power converters: (a) CM conducted emissions, (b) CM output noise, (c) DM conducted emissions, (d) DM output noise.

Typically, a passive filter is inserted between the noise source (converter) and the load (LISN or output load) and acts as a low-pass filter as shown in FIGURE 5.2. It should have a negligible effect at the power frequency and provide a large attenuation to the noise in the EMI frequency range. Passive filters can be integrated into the power converter to reduce size and cost and improve high frequency performance [22]. But they can also be separated from the power converter topologically to evaluate their performance.

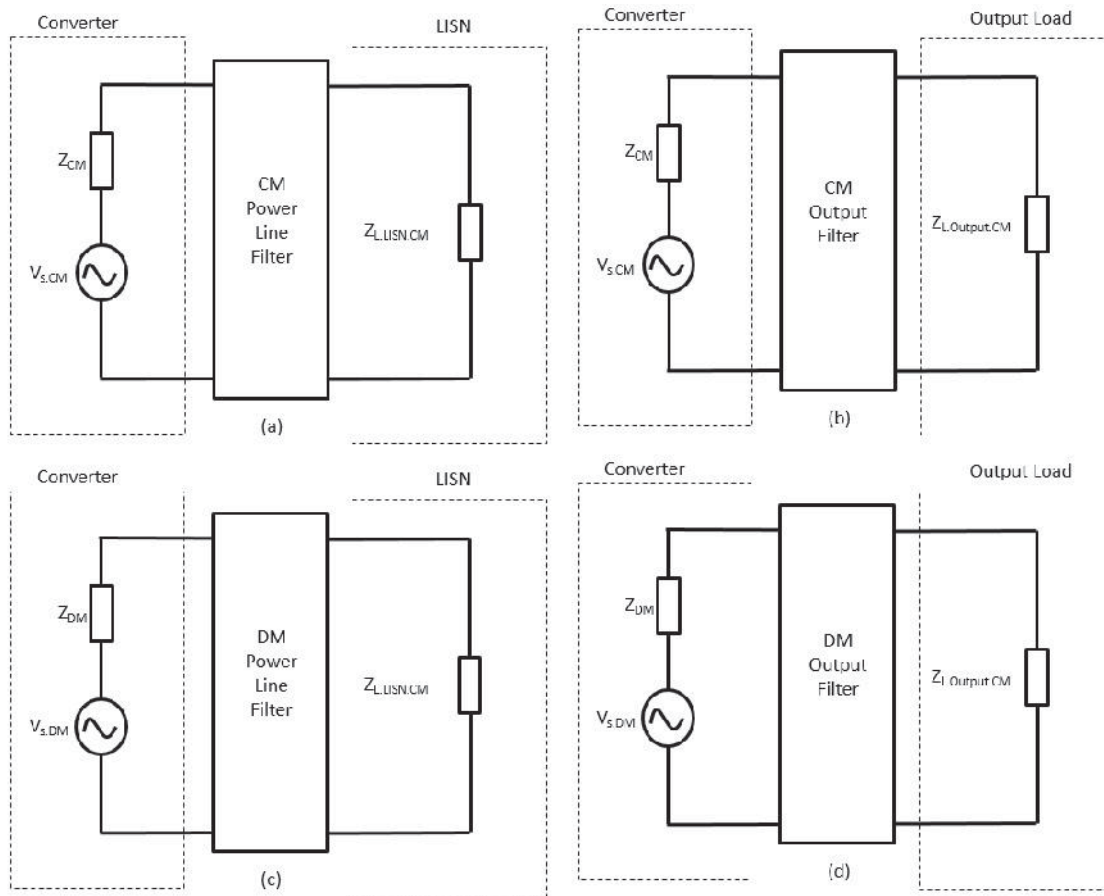


FIGURE 5.2 Filters in power converters for: (a) CM conducted emissions, (b) CM output noise, (c) DM conducted emissions, (d) DM output noise.

Information about the noise source and the load impedances are essential in order to optimize the filter design. Unlike filters in microwave applications, where the source and load impedances are usually well defined, the noise source and the load impedances in power converters varies depending on the application. As a result, the first step in the design of the filter is to estimate both the CM and DM source and load impedances. Methods to obtain this information through measurements were introduced in Chapter 4. Once the noise sources and the impedances are known, the filter topology can be chosen and filter components can be selected. Although methods of designing the passive filters without the knowledge of the source impedance or load impedance have been proposed

in the literature (e.g. [23], [24]), these methods either tend to overdesign the filter or require additional tuning.

5.2 Passive Filter Topologies

Different passive filter topologies might be used in power inverter circuits depending on the noise source and load impedances.

5.2.1 Standard Topologies

Passive filters consist of only passive components, such as capacitors, inductors and CM chokes. A single capacitor or an inductor, can provide a first-order low-pass filter as shown in FIGURE 5.3(a) and FIGURE 5.3(b). Its attenuation increases with frequency by 20 dB per decade above its cut-off frequency. The LC (or CL) filter is one of the most commonly used passive filters in power electronics. As its name implies, it consists of one inductor and one capacitor as shown in FIGURE 5.3(c) and FIGURE 5.3(d). It is a second-order low-pass filter and its attenuation increases with frequency by 40 dB per decade above its cut-off frequency. Combining a first-order C filter and a second-order CL filter forms a π -filter as shown in FIGURE 5.3(e). Similarly, combining a first-order C filter and a second-order LC filter forms a T-filter as shown in FIGURE 5.3(f). The π -filter and T-filter are third-order low-pass filters. Their attenuation increases with frequency by as much as 60 dB per decade above its cut-off frequency. Higher order filters can be formed similarly by cascading lower order filters to provide a sharper increase in the noise attenuation.

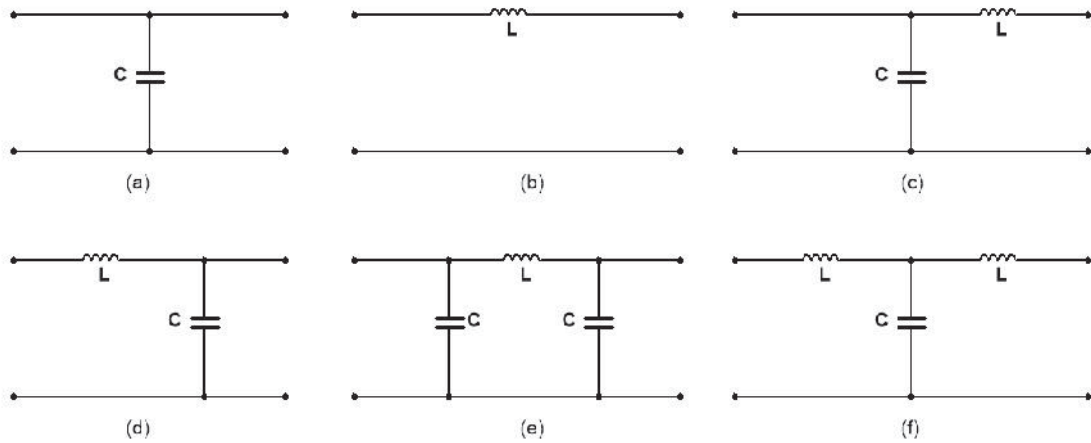


FIGURE 5.3 Passive filter topologies: (a) C filter, (b) L filter, (c) CL filter, (d) LC filter, (e) π filter, (f) T filter.

In power electronics, if the power lines are not balanced, the CM and DM noise can be coupled to each other as suggested by (4.12) and [25]. In other words, an unbalanced DM filter can increase the CM noise; and similarly, an unbalanced CM filter can increase the DM noise. Generally, this issue is addressed by dividing the DM filter inductor into two equal halves and inserting it on both power lines as shown in FIGURE 5.4. Similarly, capacitors for CM noise reduction should also be distributed equally on both power lines as shown in FIGURE 5.5.

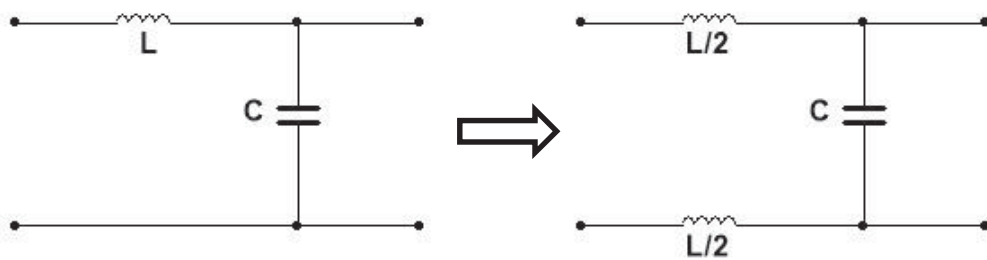


FIGURE 5.4 Balancing filter inductors.

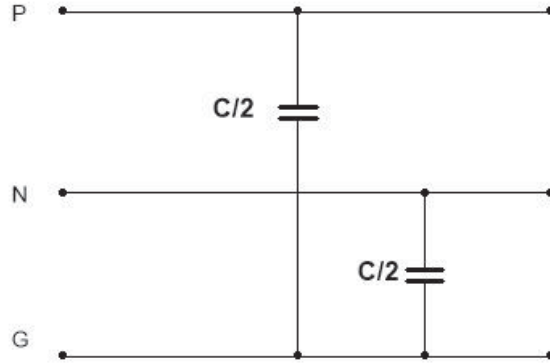


FIGURE 5.5 Balancing filter capacitors.

In practice, the leakage inductance of the CM inductor provides some DM inductance as shown in FIGURE 5.6. The total inductance presented to the DM noise is the DM inductor, L , plus the leakage inductance of the CM choke. The total capacitance is approximately equal to the capacitance of the X-capacitor, because the Y-capacitors are relatively small in order to avoid excessive leakage currents to ground. For CM noise filtering, the total inductance is the inductance of the CM choke plus the $\frac{1}{4}$ of L , because the evenly distributed DM inductances present two $L/2$ inductances in parallel to the CM noise. The total capacitance for CM filtering is the sum of the evenly distributed Y-capacitors as shown in the figure.

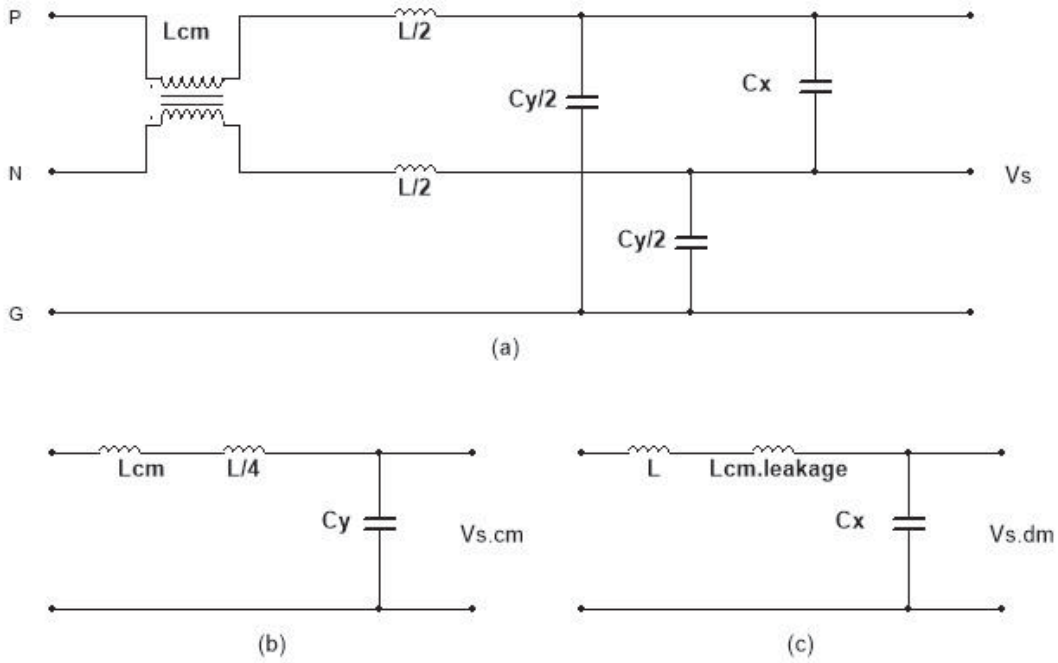


FIGURE 5.6 LC filter and its CM and DM equivalent circuits: (a) LC filter, (b) CM equivalent circuit, (c) DM equivalent circuit.

5.2.2 IL of Passive Filters

The concept of Insertion Loss (IL) introduced in 4.5.1, is very useful in designing and evaluating passive filters in power converters. The goal of the filter design in power converters is to maximize the IL of the filter in the EMI noise frequency range, and minimize the IL in the power frequency range. Using (4.21), the IL of the common filter topologies illustrated in FIGURE 5.3 can be easily calculated. From there, we can analyze the advantages and disadvantages of these filter types.

C Filter

The ABCD matrix of the C filter in FIGURE 5.3(a) can be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{C\text{-filter}} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \quad (5.1)$$

Substituting it into (4.21) gives,

$$\text{IL}_{C\text{-filter}} = \left| 1 + j \frac{\omega C}{Y_s + Y_L} \right|. \quad (5.2)$$

To maximize IL, ωC should be much greater than $Y_s + Y_L$. Thus the C filter should be chosen when both source and load impedances are high.

L Filter

The ABCD matrix of the L filter in FIGURE 5.3(a) can be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{L\text{-filter}} = \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix}. \quad (5.3)$$

Substituting it into (4.21) gives,

$$\text{IL}_{L\text{-filter}} = \left| 1 + j \frac{\omega L}{Z_s + Z_L} \right|. \quad (5.4)$$

To maximize IL, ωC should be much greater than $Z_s + Z_L$. Thus the L-filter should be chosen when both the source and load impedances are low.

CL Filter

The ABCD matrix of the CL filter in FIGURE 5.3(a) can be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CL\text{-filter}} = \begin{bmatrix} 1 & j\omega L \\ j\omega C & 1 - \omega^2 LC \end{bmatrix}. \quad (5.5)$$

Substituting it into (4.21) gives,

$$IL_{CL-filter} = \left| 1 - \frac{\omega^2 LCZ_s}{Z_s + Z_L} + j \frac{\omega(L + CZ_L Z_s)}{Z_s + Z_L} \right|. \quad (5.6)$$

As frequency increases, the term $\frac{\omega^2 LCZ_s}{Z_s + Z_L}$ will dominate. To maximize the IL, Z_s should

be much greater than Z_L . Thus the CL filter should be chosen when the source impedance is much greater than the load impedance.

LC-Filter

The ABCD matrix of the LC filter in FIGURE 5.3(a) can be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{LC-filter} = \begin{bmatrix} 1 - \omega^2 LC & j\omega L \\ j\omega C & 1 \end{bmatrix} \quad (5.7)$$

Substituting it into (4.21) gives,

$$IL_{LC-filter} = \left| 1 - \frac{\omega^2 LCZ_L}{Z_s + Z_L} + j \frac{\omega(L + CZ_L Z_s)}{Z_s + Z_L} \right|. \quad (5.8)$$

As frequency increases, the term $\frac{\omega^2 LCZ_L}{Z_s + Z_L}$ will dominate. To maximize the IL, Z_L should

be much greater than Z_s . Thus the LC filter should be chosen when the source impedance is much smaller than the load impedance.

Π -Filter

The ABCD matrix of the π filter in FIGURE 5.3(a) can be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\pi-filter} = \begin{bmatrix} 1 - \omega^2 LC & j\omega L \\ j(2\omega C - \omega^3 LC^2) & 1 - \omega^2 LC \end{bmatrix} \quad (5.9)$$

Substituting it into (4.21) gives,

$$\mathbb{I}_{\pi\text{-filter}} = \left| 1 - \omega^2 LC + j \left(\frac{\omega(L + 2CZ_L Z_s)}{Z_s + Z_L} - \frac{\omega^3 LC^2}{Y_s + Y_L} \right) \right|. \quad (5.10)$$

As frequency increases, the term $\frac{\omega^3 LC^2}{Y_s + Y_L}$ will dominate. To maximize the IL, $\omega^3 LC^2$

should be much greater than $Y_s + Y_L$. Thus the π filter should be chosen when both source and load impedances are high.

T-Filter

The ABCD matrix of the T-filter in FIGURE 5.3(a) can be easily found as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{T\text{-filter}} = \begin{bmatrix} 1 - \omega^2 LC & j(2\omega L - \omega^3 L^2 C) \\ j\omega C & 1 - \omega^2 LC \end{bmatrix} \quad (5.11)$$

Substituting it into (4.21) gives,

$$\mathbb{I}_{T\text{-filter}} = \left| 1 - \omega^2 LC + j \left(\frac{\omega(2L + CZ_L Z_s)}{Z_s + Z_L} - \frac{\omega^3 L^2 C}{Z_s + Z_L} \right) \right|. \quad (5.12)$$

As frequency increases, term $\frac{\omega^3 L^2 C}{Z_s + Z_L}$ will dominate. To maximize the IL, $\omega^3 L^2 C$ should

be much greater than $Z_s + Z_L$. Thus the T filter should be chosen when both source and load impedances are low.

5.2.3 Summary of the Passive Filter Topologies

The IL and the maximum IL conditions for the six filter types in the previous section are listed in Table 5.1 and FIGURE 5.7. From the table and figure, we can observe that in order to maximize IL, the high-impedance filter element (the inductor) should face the low-impedance source or load and the low-impedance filter element (the capacitor) should face the high-impedance source or load.

Table 5.1 Summary of the IL and maximum IL condition of the passive filters.

Passive Filter Type		Insertion Loss (IL)	Maximum IL condition
1 st order	C-filter	$IL = \left 1 + j \frac{\omega C}{Y_s + Y_L} \right $	$\omega C \gg Y_s + Y_L$
	L-filter	$IL = \left 1 + j \frac{\omega L}{Z_s + Z_L} \right $	$\omega L \gg Z_s + Z_L$
2 nd order	CL-filter	$IL = \left 1 - \frac{\omega^2 LC Z_s}{Z_s + Z_L} + j \frac{\omega(L + CZ_L Z_s)}{Z_s + Z_L} \right $	Large $\omega^2 LC$ & $Z_s \gg Z_L$
	LC-filter	$IL = \left 1 - \frac{\omega^2 LC Z_L}{Z_s + Z_L} + j \frac{\omega(L + CZ_L Z_s)}{Z_s + Z_L} \right $	Large $\omega^2 LC$ & $Z_L \gg Z_s$
3 rd order	π -filter	$IL = \left 1 - \omega^2 LC + j \left(\frac{\omega(L + 2CZ_L Z_s)}{Z_s + Z_L} - \frac{\omega^3 LC^2}{Y_s + Y_L} \right) \right $	$\omega^3 LC^2 \gg Y_s + Y_L$
	T-filter	$IL = \left 1 - \omega^2 LC + j \left(\frac{\omega(2L + CZ_L Z_s)}{Z_s + Z_L} - \frac{\omega^3 L^2 C}{Z_s + Z_L} \right) \right $	$\omega^3 L^2 C \gg Z_s + Z_L$

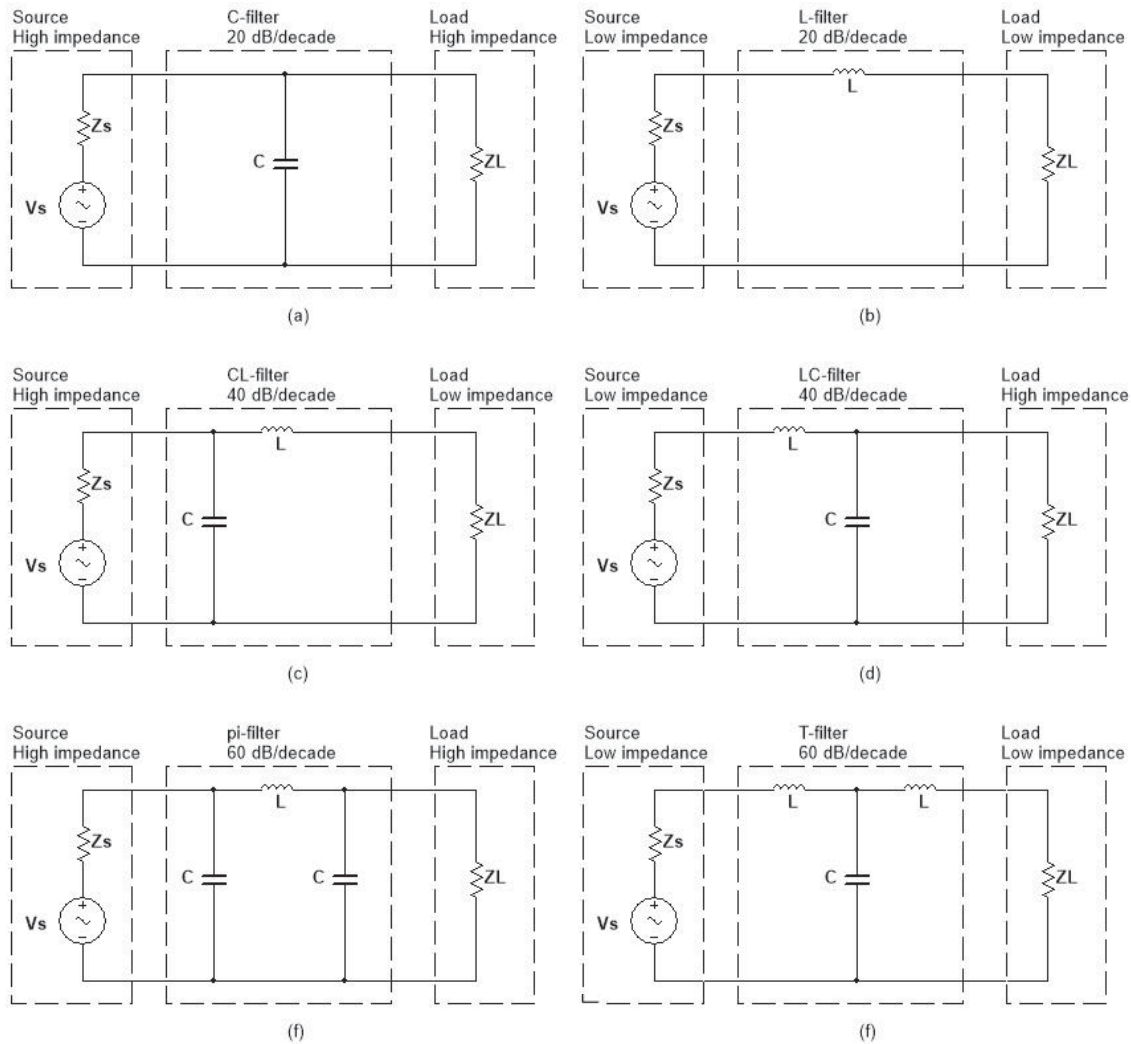


FIGURE 5.7 Maximum IL condition for EMI filters: (a) C filter, (b) L filter, (c) CL filter, (d) LC filter, (e) π filter, (f) T filter.

5.3 Passive Filter Components

After the filter topology is determined, we need to select the filter components. The passive filter mainly consists of capacitors and inductors as shown in FIGURE 5.3. The capacitors and inductors used in passive filters for power converters are discussed in this section.

5.3.1 Filter Capacitor

For DM noise filtering, capacitors are generally placed between the power lines. Capacitors connecting one power phase to another are referred to as the X-capacitors. For CM noise filtering, capacitors are placed between each power phase and the ground. These capacitors are referred to as Y-capacitors. In the previous section, the IL of the C filter was calculated assuming that the capacitors in the filter were ideal. But in reality, a capacitor will have an equivalent series resistance (ESR) and an equivalent series inductance (ESL) as indicated in FIGURE 5.8. The ESR and ESL affect the high frequency performance of passive filters, because above a certain frequency, the ESL dominates and the X-capacitor starts to act like an inductor. Extra attention must be paid when designing the layout to make sure that the effect of ESR and ESL is minimized.



FIGURE 5.8 Capacitor model.

The rated voltage of the capacitor should also be considered. As a rule of thumb, the rated voltage of the capacitor should be at least twice the maximum power line voltage.

Y-capacitors are limited by leakage current requirements imposed by many safety agencies. Excessive leakage current to ground is considered a shock hazard, and therefore is regulated. The leakage requirements vary from 0.5 mA to 5 mA depending on the application and the safety agency certification required.

For safety reasons, a resistor, typically 1 k Ω , is sometimes added in parallel with an X-capacitor to discharge the capacitor when power is removed.

5.3.2 Filter Inductor

While a filter capacitor provides a low impedance shunt path for the EMI noise, the filter inductor provides high series impedance to block EMI noise. Both the DM inductor and CM chokes typically have similar wire-wound-on-core structures. At high frequencies, the parasitic inter-winding capacitance of the inductor can significantly lower the impedance of the inductor and decrease the performance of the filter. The model of a typical inductor and its parasitics is illustrated in FIGURE 5.9. Minimizing the effect of the parasitic capacitance of the inductor during the filter design is very important.

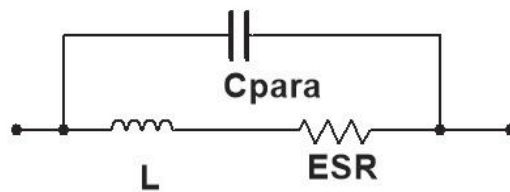


FIGURE 5.9 Inductor model.

For DM filter inductors, the power rating and the core saturation current of the inductor must be accounted for, because the DM filter inductor carries all of the power line current. DM inductors are usually wound on low permeability cores so as not to saturate.

For CM filter inductors, to prevent core saturation resulting from the large ac power line currents, the two windings of the inductor are usually wound on the same core. This coupled inductor topology is generally referred to as a CM choke. Because the power line

currents are in opposite directions, the magnetic flux produced in the core by these currents cancels. This prevents the power line currents from saturating the core. CM chokes are generally designed to have a specific value of leakage inductance, such that they also provide a certain amount of DM filtering. Typical power line chokes will have leakage inductances somewhere between 0.5 and 5% of their CM inductance.

5.4 Passive Filter Application

With the help of Table 5.1 and FIGURE 5.7, we will study some applications of passive filters in power converters.

5.4.1 CM Conducted Emissions Filtering

For CM conducted emissions, the power converter is a high-impedance source, because the parasitic capacitance between the source and the chassis is usually small. The LISN is a low-impedance load (a 25- Ω resistance). For maximum IL, the high-impedance filter element (the inductor) should face the low-impedance load (the LISN), and the low impedance filter element (the capacitor) should face the high-impedance source (the power converter). Thus, a CL-filter is generally suitable in this case. As shown in FIGURE 5.10, two line-to-ground Y-capacitors, C1 and C2, and the CM choke L1 form a low-pass CL-filter.

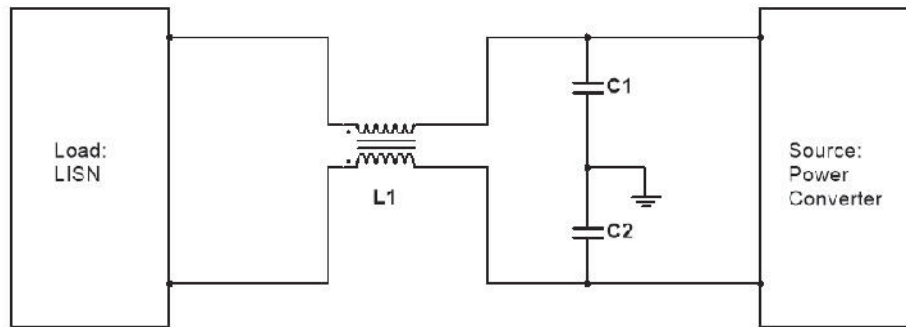


FIGURE 5.10 Passive filter for CM conducted emissions.

The value of the Y-capacitors is usually limited by the leakage current requirements and the value of the CM choke is limited by the inter-winding capacitance. For a given value of inductance, less inter-winding capacitances usually requires a bigger choke volume. If more inductance is required to achieve the necessary IL, multiple chokes can be used in series.

5.4.2 DM Conducted Emissions Filtering

For DM conducted emissions, the power converter is a low-impedance source, because of the low impedance of the filter capacitor. The LISN is a relatively high-impedance load (a 100- Ω resistance). For maximum IL, the high-impedance filter element (the inductor) should face the low-impedance source (the converter), and the low impedance filter element (the capacitor) should face the high-impedance load (the LISN). Thus, an LC-filter will be suitable in this case. As shown in FIGURE 5.11, a line-to-line X-capacitor, C3, and the two inductors, L2 and L3, form a low-pass LC- filter, where C3 is located on the LISN side of the filter.

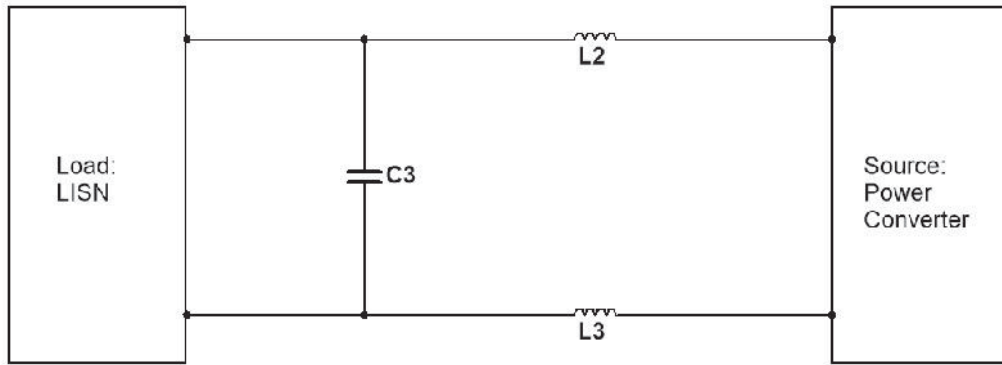


FIGURE 5.11 Passive filter for DM conducted emissions.

The value of the X-capacitor is not limited by leakage requirements. It can be on the order of several millifarads or more. As discussed in the previous section, the leakage inductance of the CM choke can provide DM inductance. If the X-capacitor is large enough, for applications where both CM and DM filtering are needed, the DM inductances, L2 and L3, can be provided by the CM choke, as shown in FIGURE 5.12. Too much leakage inductance, however, can cause the CM choke to saturate.

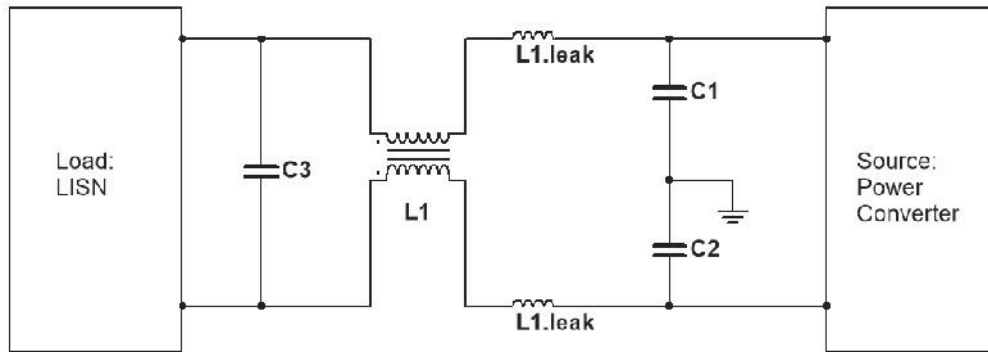


FIGURE 5.12 Passive filter for CM and DM conducted emissions.

5.4.3 Noise Filtering for an Inverter Output

For CM inverter output noise, assuming the value of Y-capacitors on the power lines is much greater than the parasitic capacitance between the load (motor) and the ground,

the power inverter is treated as a low-impedance source and the motor is treated as a high-impedance load. For maximum IL, the high-impedance filter element (the inductor) should face the low-impedance source (the inverter), and the low impedance filter element (the capacitor) should face the high-impedance load (the motor). As a result, an LC-filter will be suitable in this case. As shown in FIGURE 5.13, a CM choke, L1, and two Y-capacitors, C1 and C2, form a low-pass LC-filter where L1 is located on the inverter side. Note that C1 and C2 are limited by the leakage current requirement. This usually results in bulky CM chokes in the passive filter application. To reduce or even eliminate the CM choke, active filters and other methods will be introduced in Chapters 6-8.

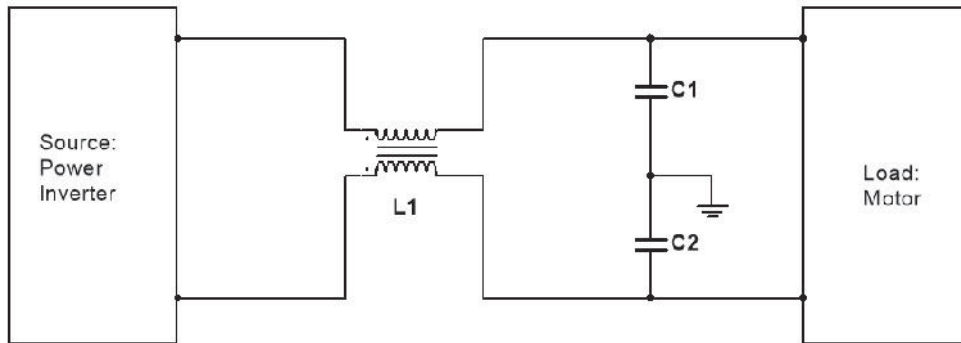


FIGURE 5.13 Passive filter for CM inverter output noise reduction.

The DM inverter output noise has the same low-impedance source and high-impedance load. Thus, the same LC-filter can be employed. When designing filters for both CM and DM noise, the leakage inductance of the CM choke can be used for DM noise filtering.

6. ACTIVE FILTERS

As the name implies, active filters use active components, such as amplifiers, to filter EMI noise. Compared to passive EMI filters, active filters can be designed to be cheaper and lighter, and they can be more effective. The bandwidth of the active filter is usually limited compared to that of a passive filter. However, because of EMI standards such as MIL-STD-461E and CISPR 11 that concern EMI noise at 10 kHz, the advantages of the active filters in size, weight and cost at those low frequencies make them a very good option for EMI noise reduction. This chapter provides general analysis and comparison of different types of active filters as well as details about active filter design and application in switched-mode power converters.

6.1 Mechanisms of Active Filters

The reason that active filters outperform passive filters at low frequencies can be explained by the following example. FIGURE 6.1 shows two passive filter topologies that were discussed in Chapter 5. The voltage across the filter inductor, V_L , and the current through the filter capacitor, I_C , can be expressed by,

$$V_L = j\omega L \cdot I_L , \quad (6.1)$$

$$I_C = j\omega C \cdot V_C . \quad (6.2)$$

V_L blocks the noise voltage, V_s , and I_C shunts the noise current, I_s . They both attenuate the noise level at the load. As shown in the equations, V_L and I_C are dependent on I_L and V_C , respectively. As a result, the filter inductor can be modeled as a current controlled voltage

source with a transfer impedance, $G_L = j\omega L$. Similarly, the filter capacitor can be seen as a current controlled voltage source with a transfer admittance, $G_C = j\omega C$. Since G_L and G_C are functions of the frequency ω , the attenuation of passive filters is also frequency dependent.

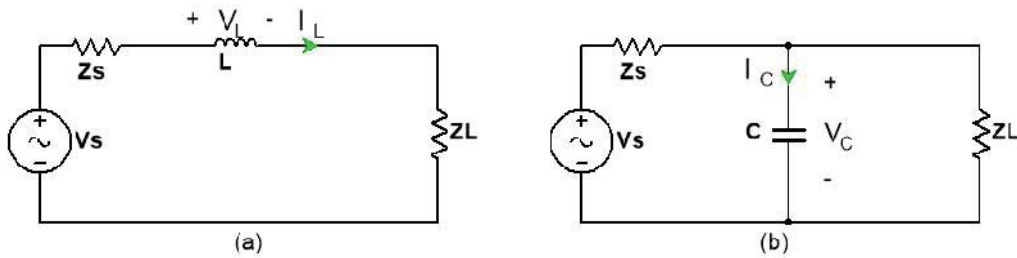


FIGURE 6.1 Example passive filters: (a) L-filter, (b) C-filter.

Applying the same concept, active filters use active components to create the current controlled voltage source and the voltage controlled current source, as shown in FIGURE 6.2. These two filters are also referred to as the current-detecting-voltage-compensating (CDVC) type active filter and voltage-detecting-current-compensating (VDCC) type active filter, respectively. The transfer impedances/admittances of the controlled sources are both denoted G in the figure. Compared to the passive filters, G of the active filters can be designed to be a large value over a certain low frequency range, independent of the frequency, as shown in FIGURE 6.3. Gains in excess of 100 at 1 MHz were demonstrated [26]. As a result, a large G , which can only be achieved by bulky passive inductors or capacitors at high frequencies, can be realized by much smaller, lighter and cheaper active components at low frequencies.

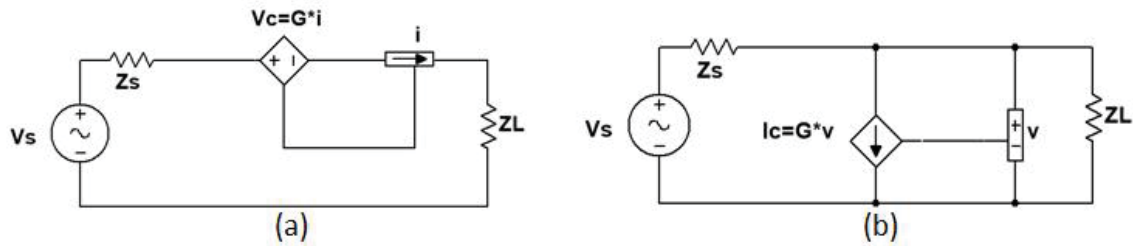


FIGURE 6.2 Type I active filters: (a) CDVC type, (b) VDCC type.

Size, weight and cost are key elements to consider when designing power converters. One reason the switching frequency keeps increasing is that higher frequencies allow for reduction in the size of the energy storage elements, such as inductors and capacitors. With the help of active filters, the size, weight and cost of power converters can be further reduced.

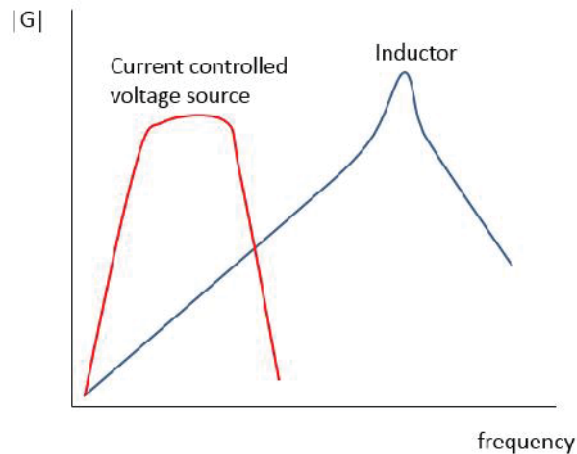


FIGURE 6.3 Typical transfer impedance of an inductor and a current controlled voltage source.

Because active filters are better for low frequency EMI noise reduction, while passive filters are more cost-effective at high frequencies. Hybrid filters using both passive and active filters can have the advantages of both. The desired IL of the hybrid filter is shown in FIGURE 6.4.

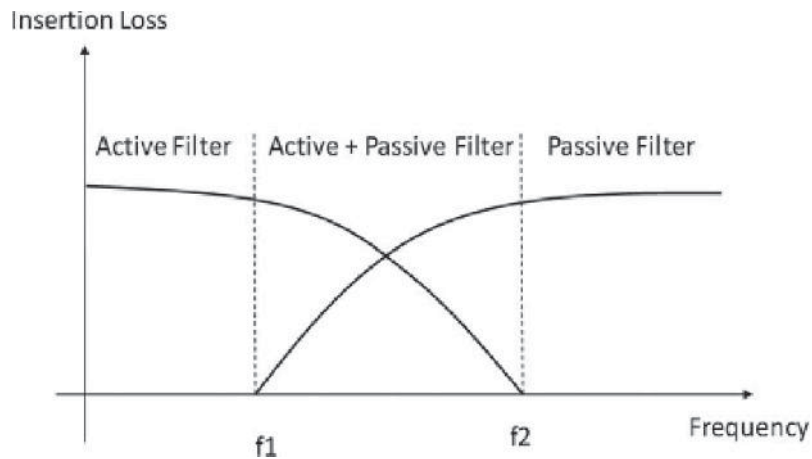


FIGURE 6.4 IL of active and passive hybrid filter.

6.2 Active Filter Topologies

Active filters can be grouped based on the characteristics of the amplification gain, G . The amplification gain of the Type I active filter represents the transfer impedance or admittance. This is similar to the C-type and L-type passive filters. Amplification gain of the Type II active filter is unit-less. This is similar to the noise cancellation method in Chapter 7.

The active filters shown in FIGURE 6.2 are referred to as Type I active filters, where the gain of the feedback loop is the transfer impedance or admittance. The active filters shown in FIGURE 6.5 are referred to as Type II active filters. These feature a unit-less gain, G . Based on the compensating method, active filters can be further grouped as feedback type and feed-forward type. FIGURE 6.5 shows all four configurations of the Type II active filters, the current-detecting-current-compensating-feedback (CDCCFB) type, the voltage-detecting-voltage-compensating-feedback (VDVCFB) type, the current-detecting-current-compensating-feed-forward (CDCCFF) type and the voltage-detecting-voltage-compensating-feed-forward (VDVCFF) type. The difference between the

feedback and feed-forward types is the locations of the detecting and compensating circuits between the load and source. Note that this difference doesn't exist in Type I active filters.

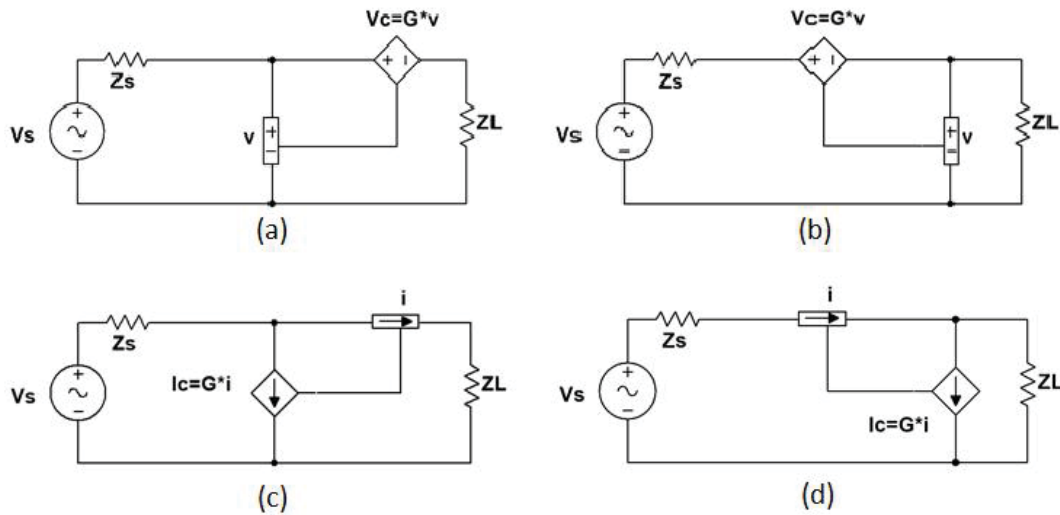


FIGURE 6.5 Type II Active filters: (a) VDVCFB type, (b) VDVCFF type, (c) CDCCFB type, (d) CDCCFF type.

Details about the different topologies will be discussed in the next section. Besides the advantages of active filters over passive filters, there are also limitations for the active filters, such as the limited bandwidth much more complicated circuits. These limitations make the active filters less attractive compared to passive filters in some applications.

6.3 Insertion Loss of Active Filters

Using the method introduced in 4.5. The insertion loss (IL) of each active filter topology can be calculated and its maximized IL condition can be found.

6.3.1 IL of Type I Active Filter

FIGURE 6.6 shows the schematic of the CDVC type active filter and its two-port-system representation. The ABCD matrix of the filter can be found as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CDVC} = \begin{bmatrix} 1 & G \\ 0 & 1 \end{bmatrix}. \quad (6.3)$$

Substituting (6.3) into (4.21) gives,

$$IL_{CDVC} = 1 + \frac{G}{Z_s + Z_L}. \quad (6.4)$$

To maximize the IL, G must be much greater than $Z_s + Z_L$. Thus this topology should be chosen when both source and load impedances are low, similar to conditions where the L-filter or T-filter should be applied.

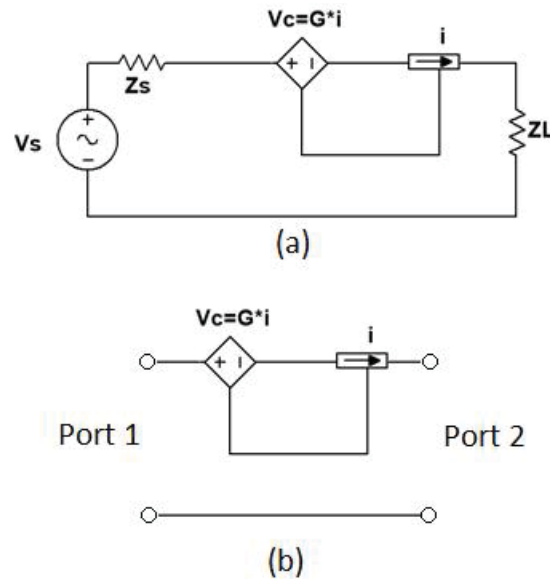


FIGURE 6.6 CDVC topology: (a) schematic, (b) two-port system.

FIGURE 6.7 shows the schematic of the VDCC type active filter and its two-port-system representation. Its ABCD matrix can be found as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{VDCC} = \begin{bmatrix} 1 & 0 \\ G & 1 \end{bmatrix}. \quad (6.5)$$

Substituting this into (4.21) gives,

$$IL_{VDCC} = 1 + \frac{GZ_s Z_L}{Z_s + Z_L} = 1 + \frac{G}{Y_s + Y_L}, \quad (6.6)$$

where Y_s and Y_L are the admittance of the source and load, respectively. To maximize the IL , G must be much greater than $Y_s + Y_L$. Thus this topology should be chosen when both source and load impedances are high, similar to conditions where the C-filter and π -filter should be applied.

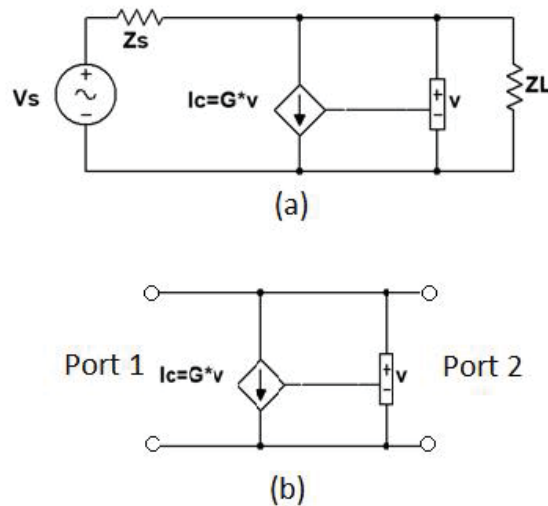


FIGURE 6.7 VDCC topology: (a) schematic, (b) two-port system.

6.3.2 IL of Type II Active Filter

FIGURE 6.8 shows the schematics of the VDVCFB and VDVCFF type active filters and their two-port-system representations. Their ABCD matrixes can be found as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{VDVCFB} = \begin{bmatrix} 1+G & 0 \\ 0 & 1 \end{bmatrix}, \text{ and} \quad (6.7)$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{VDVCFF} = \begin{bmatrix} \frac{1}{1-G} & 0 \\ 0 & 1 \end{bmatrix}. \quad (6.8)$$

Substituting these into (4.21) gives,

$$\mathbf{IL}_{VDVCFB} = 1 + \frac{GZ_L}{Z_s + Z_L}, \text{ and} \quad (6.9)$$

$$\mathbf{IL}_{VDVCFF} = \frac{1}{1-G} \left(1 - \frac{GZ_s}{Z_s + Z_L} \right). \quad (6.10)$$

To maximize the IL, Z_L must be much greater than Z_s for both topologies. Thus these types of filters should be chosen when the load impedance is much higher than the source impedance, similar to conditions where the LC-filter should be applied. Note that for the feed-forward type active filter, the gain, G , must be close as to 1 to maximize the IL according to (6.10).

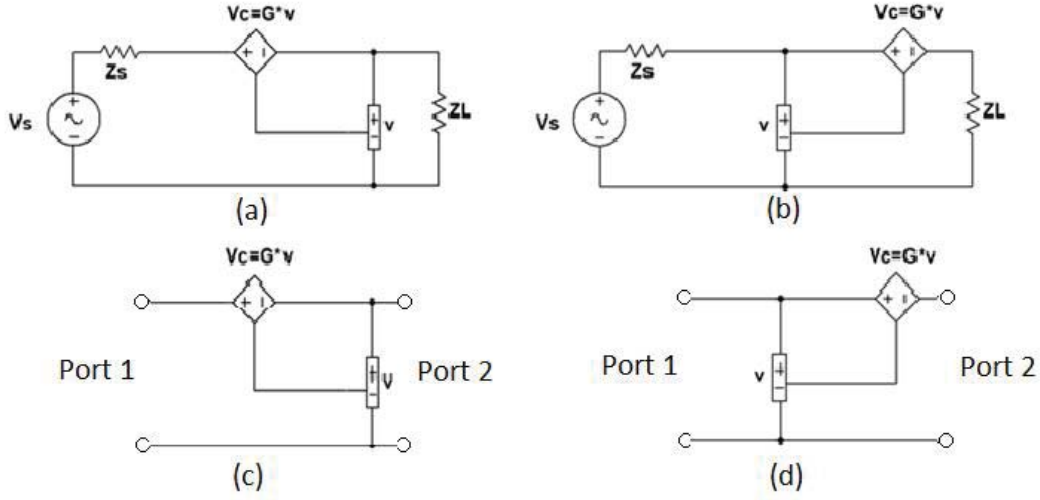


FIGURE 6.8 VDVC topologies: (a) feedback schematic, (b) feed-forward schematic, (c) feedback two-port system, (d) feed-forward two-port system.

FIGURE 6.9 shows the schematics of the CDCCFB and CDCCFF type active filters and their two-port-system representations. Their ABCD matrixes can be found as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CDCCFB} = \begin{bmatrix} 1 & 0 \\ 0 & 1+G \end{bmatrix}, \text{ and} \quad (6.11)$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CDCCFF} = \begin{bmatrix} 1 & 0 \\ 0 & \frac{1}{1-G} \end{bmatrix}. \quad (6.12)$$

Substituting these into (4.21) gives,

$$\text{IL}_{CDCCFB} = 1 + \frac{GZ_s}{Z_s + Z_L}, \text{ and} \quad (6.13)$$

$$\text{IL}_{CDCCFF} = \frac{1}{1-G} \left(1 - \frac{GZ_L}{Z_s + Z_L} \right). \quad (6.14)$$

To maximize the IL, Z_L must be much smaller than Z_s for both topologies. Thus these types of filters should be chosen when the load impedance is much lower than the source

impedance, similar to conditions where the CL-filter should be applied. Also, the gain, G of the feed-forward type active filters must be as close as to 1 to maximize the IL as suggested by (6.14).

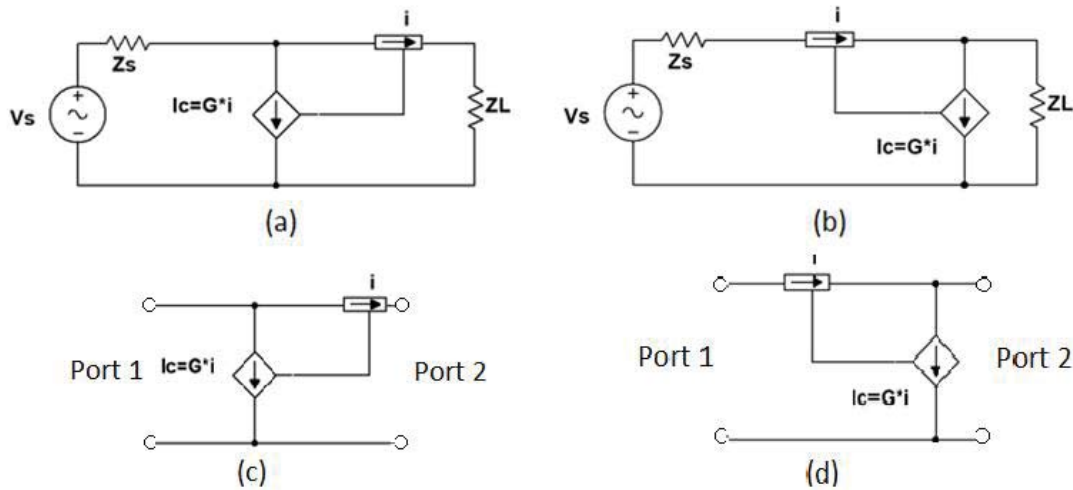


FIGURE 6.9 CDCC topologies: (a) feedback schematic, (b) feed-forward schematic, (c) feedback two-port system, (d) feed-forward two-port system.

From the calculations, we can find that, just as with passive filters, the insertion loss of active filters depends on source and load impedance. The feed-forward type active filters require the gain of the filters to be as close as possible to one. In an ideal situation, that means the compensated voltage / current is exactly the same as the detected voltage / current. As a result, this type of active filters is sometimes referred to as active cancellation. The concept of cancellation, or compensating the opposite of what's detected, can also be realized with passive components. The passive cancellation method will be introduced in Chapter 7.

6.3.3 Summary of the Active Filter Topologies

All active filter topologies and their maximum IL conditions are summarized in Table 6.1. From the table, we can observe that to maximize the IL of an active filter, voltage-detecting should be used to detect the low impedance source, while current-detecting should be used to detect the high impedance source.

Table 6.1 Summary of the IL and maximum IL condition of the active filters.

Active Filter Type		Insertion Loss (IL)	Maximum IL condition
Type I	CDVC	$IL = \left 1 + \frac{G}{Z_s + Z_L} \right $	$G \gg Z_s + Z_L$
	VDCC	$IL = \left 1 + \frac{G}{Y_s + Y_L} \right $	$G \gg Y_s + Y_L$
Type II	VDVCFB	$IL = \left 1 + \frac{GZ_L}{Z_s + Z_L} \right $	High G & $Z_L \gg Z_s$
	VDVCFE	$IL = \left \frac{1}{1-G} \left(1 - \frac{GZ_s}{Z_s + Z_L} \right) \right $	$G = 1$ & $Z_L \gg Z_s$
	CDCCFB	$IL = \left 1 + \frac{GZ_s}{Z_s + Z_L} \right $	High G & $Z_s \gg Z_L$
	CDCCFE	$IL = \left \frac{1}{1-G} \left(1 - \frac{GZ_L}{Z_s + Z_L} \right) \right $	$G = 1$ & $Z_s \gg Z_L$

The effective bandwidth is also an important factor when designing an active filter. Similar to passive filters, the differential mode (DM) IL for active filters should only block or shunt the EMI noise, not the power. Thus, in the power frequency range, the

active filter should have negligible IL to the converter. This is usually realized by implementing band control circuits in the active filters. In the next section, active filter design will be introduced.

6.4 Active Filter Components

Active filters have more components than passive filters. Active filters include both passive components, such as capacitors and inductors, and active components, such as amplifiers. As a result, designing an active filter for reducing EMI in power converters can be more challenging than designing a passive filter. This section will break down the major components of an active filter and provide insights into active filter design.

6.4.1 Detecting Circuit

Voltage detecting

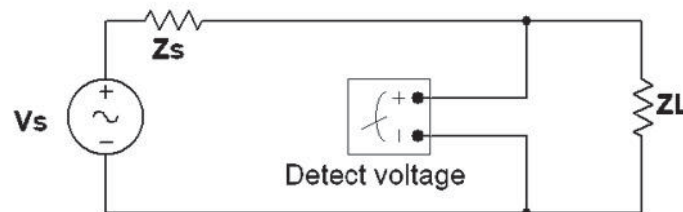


FIGURE 6.10 Voltage detecting circuit.

Like a voltage probe, voltage-detecting circuit shown in FIGURE 6.9 can detect the voltage noise by directly connecting to the power lines and feeding the signal to an amplifier, as long as the input impedance of the amplifier is high at the power frequency. Note that active filters focus on low frequency noise reduction, so impedance matching is not necessary.

When detecting the CM voltage noise, direct contact with all power cables means shorting all cables. As a result, a high impedance at the power frequency should be inserted between the detecting circuit and the power cable, as shown in FIGURE 6.11. Inductors are not suitable here because it is desired to have large impedances at the power frequency. Large resistors can provide isolation, however, in the EMI frequency range, they could significantly attenuate the detected noise signal because their values can be larger than the input impedance of the amplifier in that frequency range. (In the megahertz range, the input capacitance of an amplifier on the order of tens of picofarads has an impedance of several kilo-ohms. Thus, resistors of hundreds of ohms are desired. However, resistors of this size will cause significant power loss for high voltage power systems.) As a result, capacitors are a common choice for the voltage detecting circuit. Capacitors insulate power lines at the power frequency and provide low impedance to the detecting circuit at the EMI frequency.

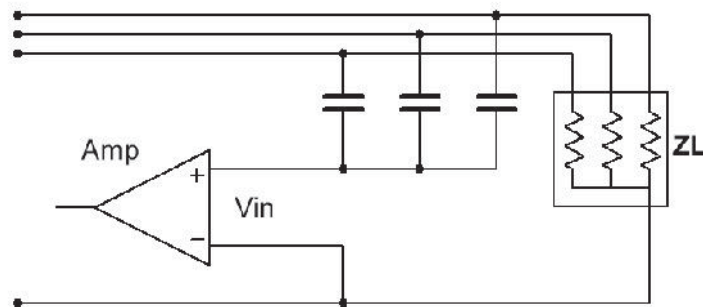


FIGURE 6.11 CM voltage detecting circuit.

Capacitors are also needed for DM noise voltage detection because they can block the power line signal from being detected, thus effectively controlling the bandwidth of the

active filter. As discussed earlier, the bandwidth of the active filter should be carefully controlled to minimize the insertion loss (IL) at the power frequency.

To detect the CM voltage, the values of the capacitors for each power cable should be identical. The equivalent CM voltage detecting circuit is shown in FIGURE 6.12(a), where the effective capacitance, C_e , of the detecting circuit is the sum of the individual capacitors connecting each power line. The model also applies for DM voltage detection where the number of power lines is one. R_{in} and C_{in} represent the input resistance and input capacitance of the amplifier, respectively. As shown in the figure, C_e and R_{in} form a high pass filter with a cut off frequency, f_L , of,

$$f_L = \frac{1}{2\pi R_{in} C_e} . \quad (6.15)$$

f_L should be designed to be between the power frequency and the switching frequency of the power converter so that only the switching frequency and its harmonics can be detected and reduced. Also C_e must be much smaller than C_{in} to avoid the detected signal being attenuated. Note that for high voltage applications, the CM voltage noise may exceed the rated value of the amplifier input. In that case, a voltage divider can be employed in the detecting circuit as shown in FIGURE 6.12(b). The voltage division factor is usually negligible compared to the amplification gain in the feed-back type active filters. However, in the feed-forward type filters, in order to achieve overall unity gain, the voltage division factor needs to be compensated either by the amplification circuit or the compensating circuit.

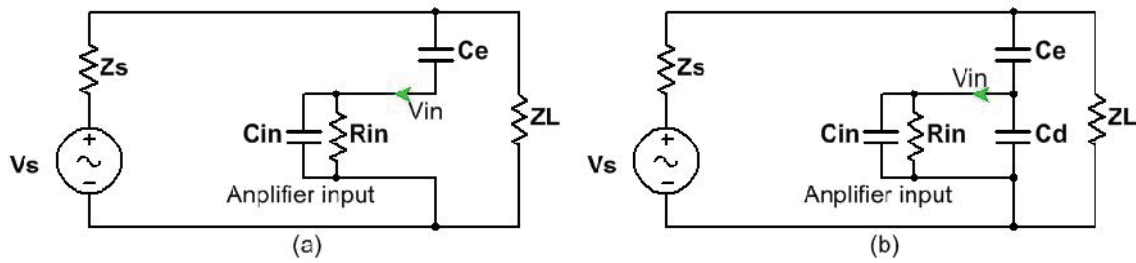


FIGURE 6.12 Low frequency voltage detecting circuit model: (a) w/o voltage divider, (b) w/ voltage divider.

FIGURE 6.13 shows the high frequency model of the voltage detecting circuit, where the equivalent series inductance (ESL) of the capacitors can no longer be neglected. Although the ESL could theoretically attenuate the signal, for a reasonable circuit layout, the ESL can be controlled within the order of nanohenries. Assuming C_e is on the order of nanofarads, the ESL will only attenuate the detected voltage when the frequency reaches tens of megahertz, which is usually not the target frequency range of the active filters. As a result, f_L of the voltage detecting circuit is usually the main concern when designing active filters.

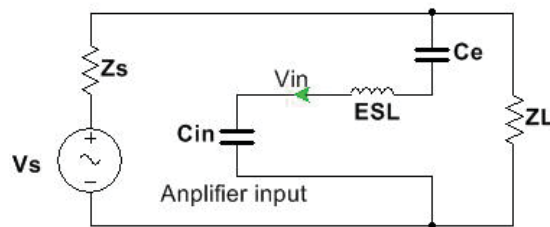


FIGURE 6.13 High frequency voltage detecting circuit model.

An example of the detecting circuit design can be found in [27]. When detecting the output CM voltage of a three phase power inverter, the inverter efficiency is also a consideration because higher valued capacitors permit more leakage current between phase wires.

Also, attention must be paid when laying out the detecting circuit to avoid EM coupling from other high speed circuits on the converter PCB.

Current Detecting

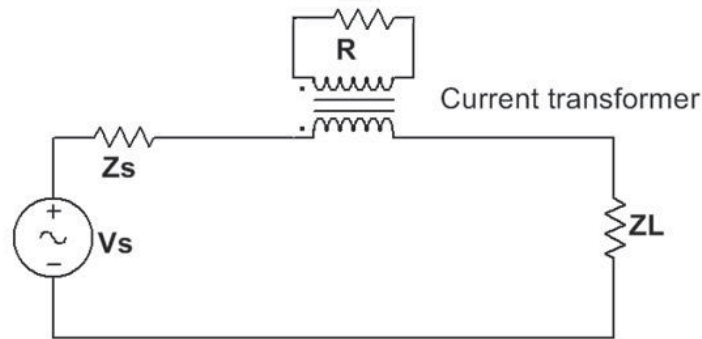


FIGURE 6.14 Current detecting circuit.

In active filter applications, transformers are often used to detect the noise current, as shown in FIGURE 6.14. The low frequency and high frequency models of the current transformer are shown in FIGURE 6.15(a) and FIGURE 6.15(b), respectively. The low frequency model consists of the primary winding magnetizing inductance, L_{mp} , an $N_p : N_s$ ideal transformer and the load, R . L_{mp} should be large enough to be considered open circuit in the noise frequency range, so that the desired relation between the output voltage, v_s , and the detected current noise, i_p , can be determined by,

$$v_s = i_s R = \frac{N_p}{N_s} R i_p \quad (6.16)$$

To find the minimum acceptable L_{mp} , the load, R , was reflected to the primary side of the transformer, as shown in FIGURE 6.16(a). In the model, i_s' , v_s' and R' are the

reflected secondary-winding current, voltage and load, respectively. Their relations to the non-reflected secondary-winding parameters are,

$$i_s' = \frac{N_s}{N_p} i_s, \quad (6.17)$$

$$v_s' = \frac{N_p}{N_s} v_s, \quad (6.18)$$

$$R' = \left(\frac{N_p}{N_s} \right)^2 R. \quad (6.19)$$

The input impedance of the detecting circuit, Z_{in} , and the reflected output voltage, v_s' , can be calculated by,

$$Z_{in} = \frac{j\omega L_{mp} R'}{R' + j\omega L_{mp}}, \text{ and} \quad (6.20)$$

$$v_s' = Z_{in} i_p = \frac{j\omega L_{mp} R'}{R' + j\omega L_{mp}} i_p. \quad (6.21)$$

Combining (6.18), (6.19) and (6.21) gives,

$$v_s = \frac{N_s}{N_p} \frac{j\omega L_{mp} \left(\frac{N_p}{N_s} \right)^2 R}{\left(\frac{N_p}{N_s} \right)^2 R + j\omega L_{mp}} i_p. \quad (6.22)$$

(6.22) suggests that at low frequencies, the transformer is like a high pass filter, and its cutoff frequency can be found by,

$$f_L = \left(\frac{N_p}{N_s} \right)^2 \frac{R}{2\pi L_{mp}} \quad (6.23)$$

The term $(N_p/N_s)^2 R$ is predetermined for a given amplification factor. L_{mp} should be tuned so that f_L is between the power frequency and the lowest noise frequency (usually the switching frequency) of the switched-mode power converters, and provide enough attenuation to the noise. Note that the load, R , is much smaller than the input impedance of the amplifier so that the increased power line impedance will be small, according to (6.20).

The primary side magnetizing inductance of the transformer, L_{mp} , can be estimated by,

$$L_{mp} = \frac{N_p^2 \mu_0 \mu_r A}{l} \quad (6.24)$$

where l , A and μ_r are the length of the primary winding, section area of the magnetic core and the relative permeability of the core material, respectively. μ_0 is the absolute permeability, and its value is $4\pi \times 10^{-7}$.

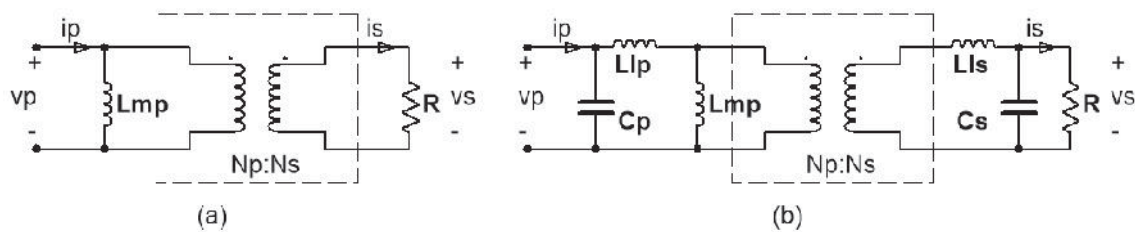


FIGURE 6.15 Current detecting transformer model: (a), low frequency model, (b), high frequency model.

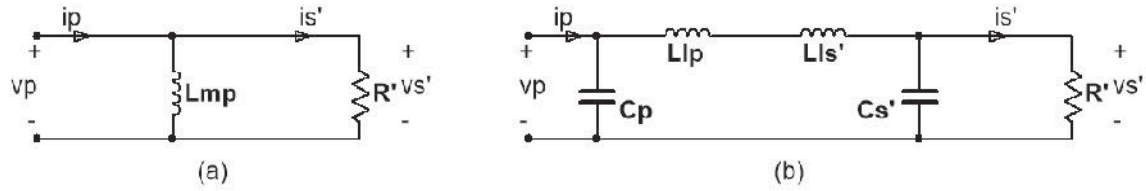


FIGURE 6.16 Current detecting transformer model with reflected secondary side circuit: (a) low frequency model, (b) high frequency model.

Transformers are not ideal. Even at frequencies where the active filter is designed to work, their leakage inductance and the inter-winding parasitic capacitance can degrade the performance of current detection. The frequency range in which these parasitic parameters start to affect the current detecting circuit will be referred to as the ‘high frequency range’ in this text, as compared to the low frequency range discussed earlier. The simplified high frequency transformer model is shown in FIGURE 6.15(b), L_p , C_p , L_s , and C_s are the primary-winding leakage inductance, primary-winding parasitic capacitance, secondary-winding leakage inductance and secondary-winding parasitic capacitance, respectively. By reflecting the secondary side circuit to the primary side, the high frequency model of the transformer can be further simplified to the circuit in FIGURE 6.16(b), where i_s' , v_s' , and R' can be calculated using (6.17), (6.18), and (6.19), respectively. L_{ls}' and C_{ls}' can be calculated by,

$$L_{ls}' = \left(\frac{N_p}{N_s} \right)^2 L_{ls} , \text{ and} \quad (6.25)$$

$$C_{ls}' = \left(\frac{N_p}{N_s} \right)^2 C_{ls} . \quad (6.26)$$

L_{mp} will be considered an open circuit at high frequencies. L_p , C_p , L_s , and C_s form a low pass π -filter with cutoff frequency,

$$f_H = \left(\frac{N_s}{N_p} \right)^2 \frac{1}{2\pi^3 \sqrt{\left(L_{pl} + \left(\frac{N_p}{N_s} \right)^2 L_{sl} \right) C_{pl} C_{sl} R}} . \quad (6.27)$$

f_L and f_H are the lower end and upper end, respectively, of the noise detecting bandwidth. This bandwidth should be designed to include the targeted noise band, but exclude the power frequency band of the converter.

One disadvantage of the transformer is its size. Thick power cables wound around a magnetic core will significantly increase the size of the core. As a result, the clamp-on-type current transformer shown in FIGURE 6.17, is desired. Since the secondary winding only carries small noise current, it can be made very thin. When clamping on all cables, the CM noise current can also be measured conveniently. The disadvantage of the clamp-on transformer is that the magnetizing inductance of the primary winding is very small, which could make the low side cut-off frequency, f_L , too high, leading to degraded performance of the active filter in low frequency range. However, from (6.23), this problem can be mitigated by increasing the number of secondary winding and the output resistance.

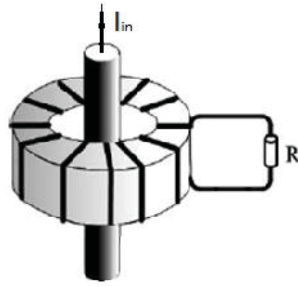


FIGURE 6.17 Clamp-on current transformer.

6.4.2 Compensating Circuit

Voltage compensating

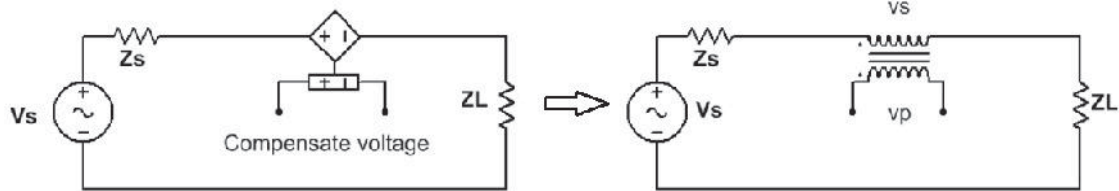


FIGURE 6.18 Voltage compensating circuit.

To compensate a voltage onto the power cables, transformers are usually employed (FIGURE 6.18). They are basically same as the current-detecting transformers, except their secondary windings are terminated by the actual load, $Z_s + Z_L$, of the power system. The low and high frequency models of the voltage transformer are shown in FIGURE 6.19. The circuit models with reflected secondary side circuit are shown in FIGURE 6.20. At low frequencies, the compensating voltage, v_s , can be expressed by,

$$v_s = \frac{N_s}{N_p} v_p . \quad (6.28)$$

It can also be expressed in terms of the amplifier output current as,

$$v_s = \frac{N_s}{N_p} Z_{in} i_p = \frac{N_s}{N_p} \frac{j\omega L_{mp} \left(\frac{N_p}{N_s}\right)^2 (Z_L + Z_s)}{\left(\frac{N_p}{N_s}\right)^2 (Z_L + Z_s) + j\omega L_{mp}} i_p \quad (6.29)$$

At low frequencies, the compensated voltage is usually limited by the output current of the amplifier. Assuming the amplifier output current is constant, the lower end of the bandwidth of the compensating voltage can be calculated from (6.29).

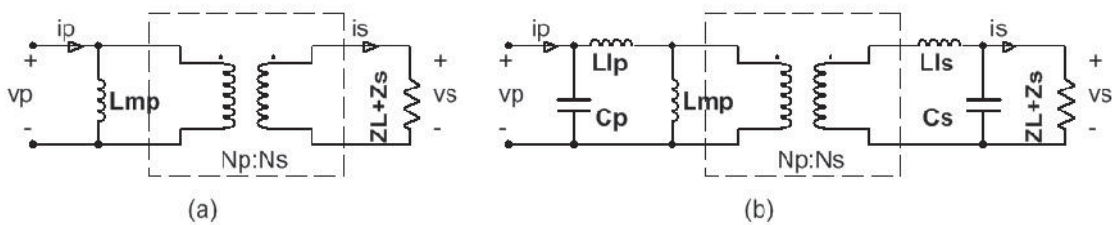


FIGURE 6.19 Voltage compensating transformer model: (a) low frequency model, (b) high frequency model.

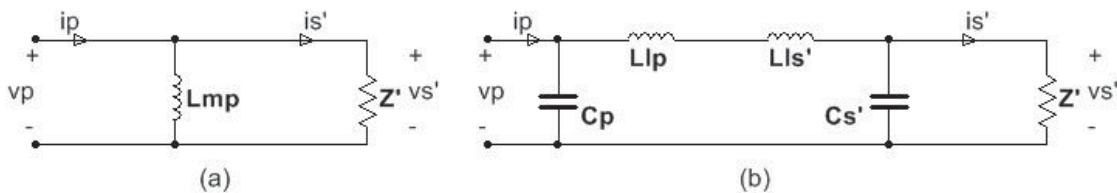


FIGURE 6.20 Voltage compensating transformer model with reflected secondary side circuit: (a) low frequency model, (b) high frequency model.

At high frequencies, due to the leakage inductance and inter-winding capacitance, the compensating voltage starts to roll off at certain frequencies, just as with the current detecting transformer. Similarly, controlling the leakage inductance and inter-winding capacitance of the transformer benefits its high frequency performance.

The clamp-on voltage compensating transformer is similar to the clamp-on current detecting transformer and is desired for the same reason; that is, it can significantly

reduce the size of the active filter for high current applications. However, for the voltage compensating transformer, the clamp-on side is the secondary winding, which significantly reduces the magnetizing inductance of the secondary winding; L_{ms} . L_{ms} is related to L_{mp} by,

$$L_{mp} = \left(\frac{N_p}{N_s} \right)^2 L_{ms} . \quad (6.30)$$

Substituting (6.30) into (6.29) gives,

$$v_s = \left(\frac{N_p}{N_s} \right) \frac{j\omega L_{ms} (Z_L + Z_s)}{(Z_L + Z_s) + j\omega L_{ms}} i_p . \quad (6.31)$$

Small L_{ms} will significantly reduce v_s . One solution is to increase N_p/N_s , which requires the output voltage of the amplifier, v_p , to be very large, according to (6.28). Increasing the output current of the amplifier, i_p , also helps. In practice, this kind of clamp-on transformer has rarely been employed in active filter applications. An example of its application is the current injection probe used in the Bulk Current Injection (BCI) test. Note the BCI probe usually requires very large amplifiers to output large v_p and i_p .

Current compensating

Current compensating is used to create a shunt current source, as shown in FIGURE 6.21(a). Since a current source is high impedance, direct contact with power lines for DM noise current compensating is allowed. However, as shown in FIGURE 6.21, capacitors are commonly employed for filtering the power frequency signals and for isolating power lines when compensating the CM current. Similar, mechanisms for voltage detecting

circuits were discussed in 6.4.1. The values of the capacitors must be identical for CM current compensation to avoid the compensated CM current being converted to DM current.

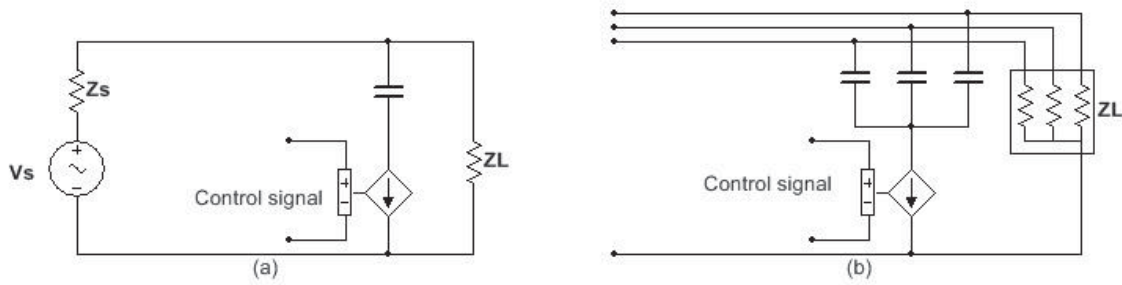


FIGURE 6.21 Current compensating circuit: (a) DM, (b) CM.

The low frequency model of the current compensating circuit is shown in FIGURE 6.22. V_{am} represents the maximum output voltage of the amplifier. The load is Z_L and Z_s in parallel. Assuming the output impedance of the amplifier is small, the compensated current can be calculated by,

$$I_c = \frac{V_{am}}{j\omega C_e + Z_L \parallel Z_s} \quad (6.32)$$

For CM conducted emissions in power converters, $Z_L \parallel Z_s$ is usually capacitive. In that case, the circuit cannot block the power frequency signal. The bandwidth control can only be done in the detecting circuit. For DM conducted emissions, $Z_L \parallel Z_s$ is mainly resistive. Letting $Z_L \parallel Z_s \approx R_L$, the cut-off frequency of the circuit can then be found as,

$$f_L = \frac{1}{2\pi R_L C_e} \quad (6.33)$$

Similarly, f_L should be between the power frequency and the noise frequency.

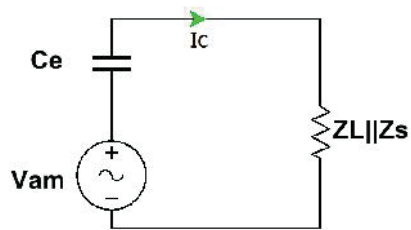


FIGURE 6.22 LF current compensating circuit model.

High frequency (megahertz range) performance of the current compensating circuit is usually not a concern, because the ESR and ESL of the small capacitors in the detecting circuit can be well controlled.

6.4.3 Amplifying Circuit

The detected noise needs to be amplified before being compensated back. As analyzed in 6.3, for active filters it is desirable to have a high gain amplifier for feedback topologies, and a unit gain amplifier for feed-forward topologies. Transistor amplifiers and operational amplifiers (op-amps) are the most commonly used amplifier types in active filters because of their small size, low cost and easy implementation. Selection and design of amplifiers for active filters is discussed in this section.

Amplifier type

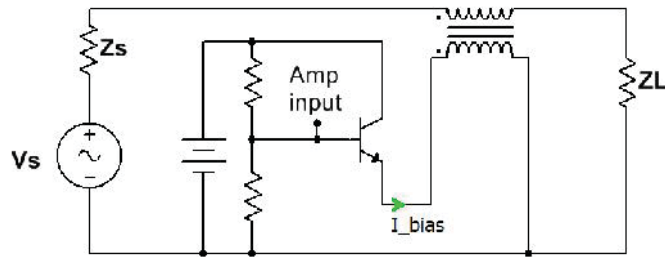


FIGURE 6.23 Class-A amplifier for voltage compensation.

A single NPN transistor can be used as an amplifier in the active filter, as shown in FIGURE 6.23. This type of amplifier is classified as a Class A amplifier in which the active element (the NPN transistor in this case) remains conducting all the time. In other words, the output stage is biased by a DC bias current, I_{bias} . Besides its higher power loss, this kind of amplifier is not suitable for active filters because it makes implementing the high pass filter on the output very difficult, if not impossible. As a result, class-B or class-AB amplifiers are commonly used in the design of active filters for power converters. FIGURE 6.24(a) and FIGURE 6.24(b) show a class-B and a class-AB push-pull amplifier being used to feed the voltage compensating circuit. FIGURE 6.25 shows a class-B push-pull amplifier being used to feed a current compensating circuit. The capacitor, C_f , in the figures is used to filter the output of the amplifier so that only the EMI noise signal is compensated.

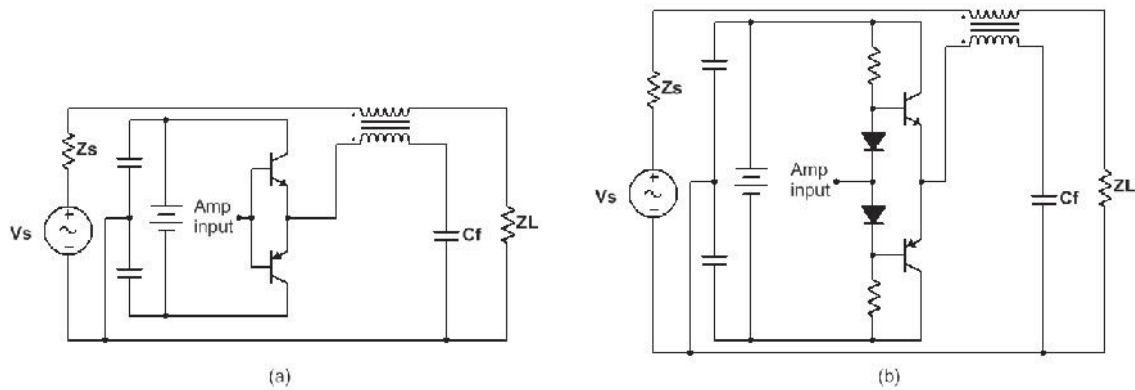


FIGURE 6.24 Push-pull amplifier for voltage compensation: (a) class-B, (b) class-AB.

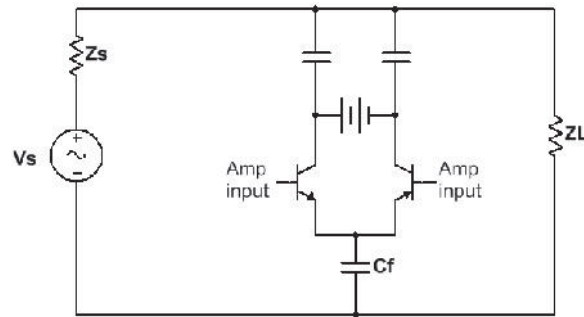


FIGURE 6.25 Class-B push-pull amplifier for current compensation.

Op-amps are also widely used in active filters. Compared to BJT transistors, off-the-shelf op-amps provide much higher bandwidth but lower output capability. Depending on the application and noise level, the op-amp can be a better choice in some cases. FIGURE 6.26(a) and FIGURE 6.26(b) show the op-amp being used to feed a voltage compensating circuit and a current compensating circuit, respectively. An example of the active filter using Texas Instruments OPA552 as the power amplifier is demonstrated in [27].

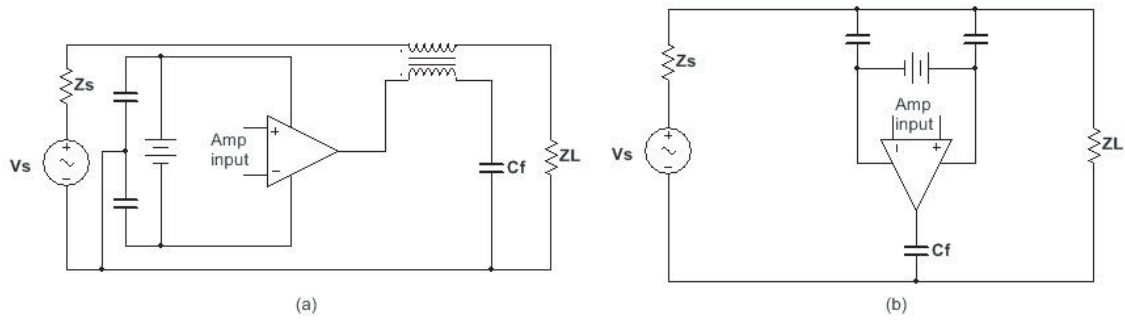


FIGURE 6.26 Op-amp in active filters: (a) voltage compensation, (b) current compensation.

Darlington configurations of BJT transistors can also be used, as demonstrated by Di Piazza and etc. [28] (FIGURE 6.27).

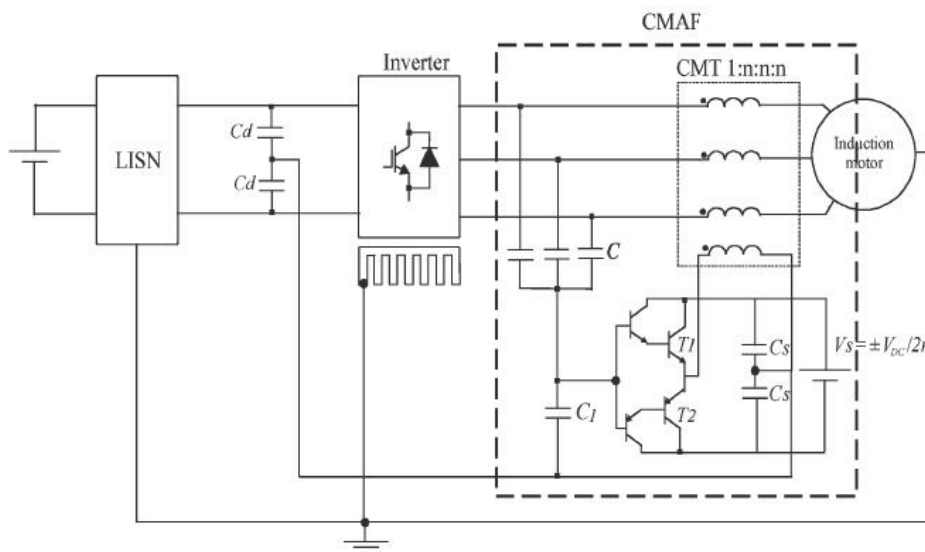


FIGURE 6.27 Active filter application with push-pull amplifier in Darlington configuration. [28]

Amplifier power supply

The active components, or the amplifiers, in active filters need power sources. They can be sources from the DC bus of the power converters or from additional voltage regulators. These voltage regulators can be switched-mode power supplies or linear

power supplies, of which the latter is usually preferred because the power required by the amplifier is small in most cases, and the linear regulator is cheaper and less noisy.

The power supply for amplifiers can be either isolated from the power lines of the power converter or not isolated. FIGURE 6.24(a) and FIGURE 6.25 show the isolated amplifier power supply for voltage compensation and current compensation, respectively, and FIGURE 6.28 shows the non-isolated version for voltage compensation. As shown in FIGURE 6.28, for the non-isolated power supply, two power sources, V_1 and V_2 , are needed. The magnitudes of V_1 and V_2 must be greater than $V_s/2$ so as not to saturate the amplifier. One advantage of the non-isolated configuration is that its power supply is usually cheaper because the isolated power supply usually requires isolation transformers. An example of the design of the non-isolated amplifier power supply for active filters used in a three phase power inverter output can be found in [27].

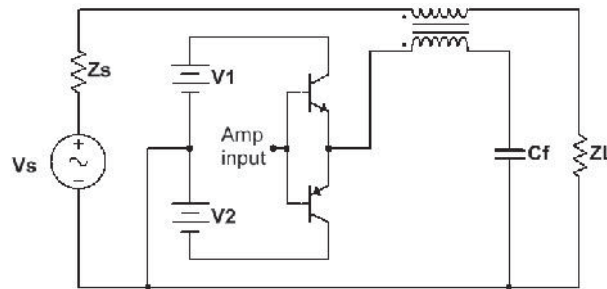


FIGURE 6.28 Non-isolated amplifier power supply.

Unity-gain active filter

In 6.3.2, the maximum insertion loss for type II active filters was discussed. For feed-forward type topologies, a unity-gain amplification factor is required. Since the detecting and compensating circuits also have their own voltage or current amplification factors,

the amplifier must compensate them to achieve the overall unity-gain amplification factor. Besides correcting the amplification factor in the compensating circuit by adjusting the turns ratio of the compensating transformer, correction can also be made in the amplification circuit, such as by adding a linear amplifier.

For the voltage-detecting-voltage-compensating-feed-forward (VDVCF) active filter, shown in FIGURE 6.29, the voltage detecting circuit has a dividing factor of $C_e/(C_e+C_d)$, and the voltage compensating circuit has a amplification factor of N_s/N_p . As a result, an op-amp with a feedback loop is employed to correct the overall gain. The resistors in the feedback loop of the op-amp should satisfy,

$$\frac{C_e}{C_e + C_d} \cdot \frac{R1 + R2}{R2} \cdot \frac{N_s}{N_p} = 1 \quad (6.34)$$

In this expression, $R1$ and $R2$ are both large-value resistors.

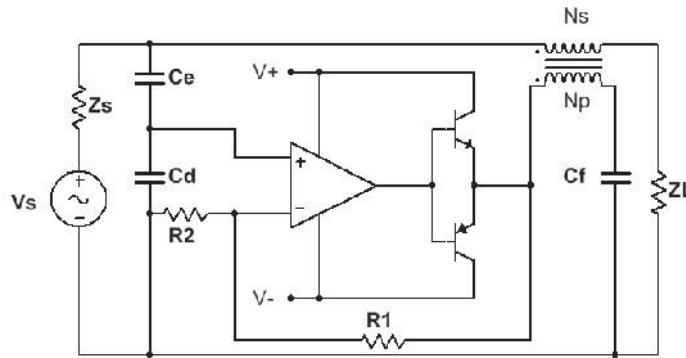


FIGURE 6.29 Unity-gain VDVCF active filter.

Amplifier selection

The bandwidth, rated voltage and output current are among the most important parameters for selecting an amplifier for active filter applications. The bandwidth of an

amplifier should be selected based on the target bandwidth of the active filter. Rated voltage and current depends on the power converter. A wideband, high voltage and high power amplifier is either hard to find or very expensive, which defeats the purpose of the active filter as a cost-effective EMI solution. It is always a compromise when selecting the amplifiers. For example, if the low voltage rate amplifier is selected, a voltage divider circuit can be added to lower the detected voltage. A multiple-stage amplifier can be cascaded to increase the output power to meet the noise reduction requirement.

6.5 Active Filter Applications

Active filter applications in power converters have been studied for many years. This section will summarize these applications and discuss the advantages and disadvantages for different types of applications.

6.5.1 DM Conducted Emissions Filtering

The differential mode (DM) conducted noise source can be modeled as a current source with a parallel bulk filter capacitor (FIGURE 3.4). The source impedance is determined by the ESR and ESL of the filter capacitor. The DM load impedance, (the LISN impedances in series) is well defined as 100Ω for the DC or single phase AC inputs. In the low frequency range up to several megahertz, the impedance of the ESL and ESR of the filter capacitor is much smaller than 100Ω . From Table 6.1, the VDVCFB and VDVCFF topologies are the best options. FIGURE 6.30 shows the schematic of the VDVCFB type active filter being applied to attenuate the DM conducted emissions.

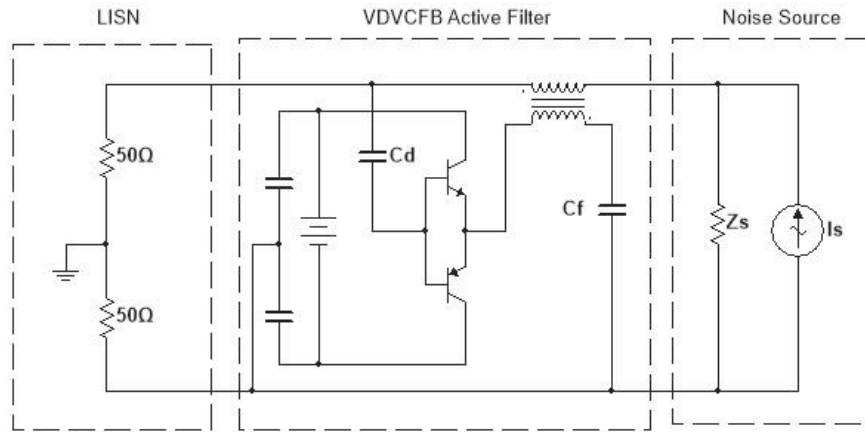


FIGURE 6.30 Schematic of the VDVCFB type active filter for DM conducted noise reduction.

Active filters for the DM conducted emissions are not very common because there is no leakage requirement for the X-capacitors. Using multiple X-capacitors that have small ESR and ESL can be more cost-effective than using the active filter.

6.5.2 CM Conducted Emissions Filtering

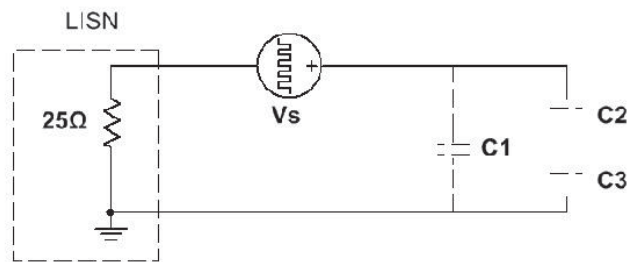


FIGURE 6.31 CM conducted emissions model.

From the CM conducted emissions model in FIGURE 6.31, we can find that the load impedance is the $25\ \Omega$ LISN impedance, and the source impedance is the stray capacitances between the power module and the converter ground. The source impedance is considered much greater than the load impedance in the conducted emissions

frequency range, 150 kHz to 30 MHz. From Table 6.1, the Type II current-detecting-current-compensating (CDCC) active filter topology provides the maximum insertion loss. An example of the CDCCFB active filter for CM conducted emission reduction is proposed in [29]. Its schematic is shown in FIGURE 6.32 and the result of the CM conducted noise reduction is shown in FIGURE 6.33.

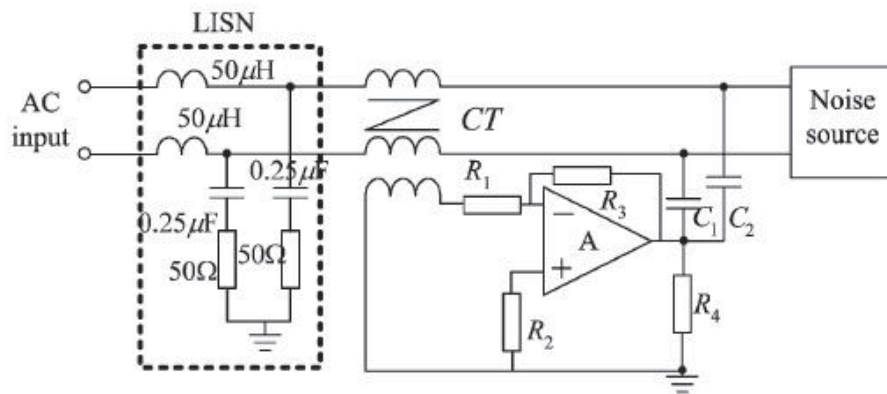


FIGURE 6.32 Schematic of the CDCCFB type active filter for CM conducted emission reduction. [29]

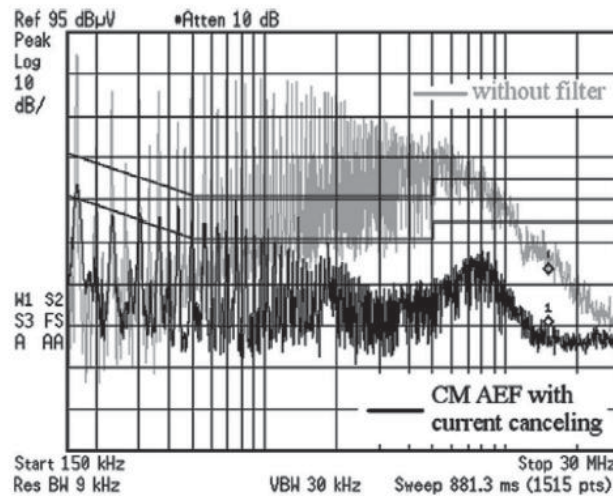


FIGURE 6.33 Comparison of the noise level w/ and w/o the CDCCFB active filter. [29]

For comparison, a CDVCFB type active filter is also designed for the same power converter in [29]. Its schematic and noise reduction result are shown in FIGURE 6.34 and

FIGURE 6.35, respectively. Comparing FIGURE 6.33 and FIGURE 6.35, it is clear that the CDCCFB type active filter works much better than the CDVCFB type active filter for this case.

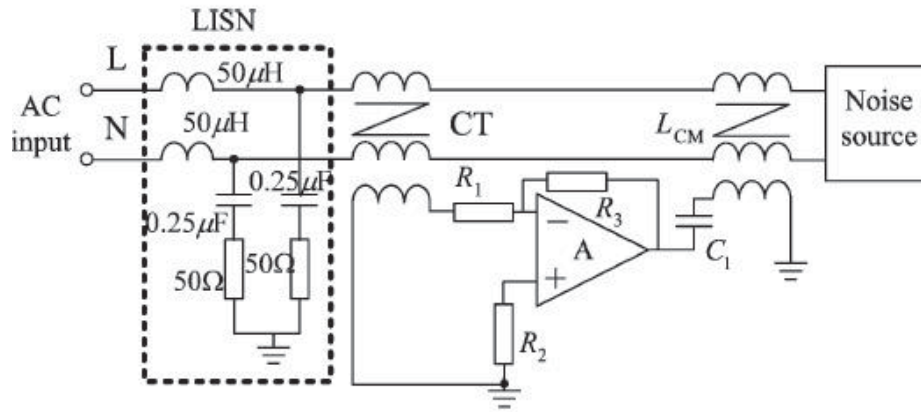


FIGURE 6.34 Schematic of the a CDVCFB type active filter for CM conducted emission reduction [29]

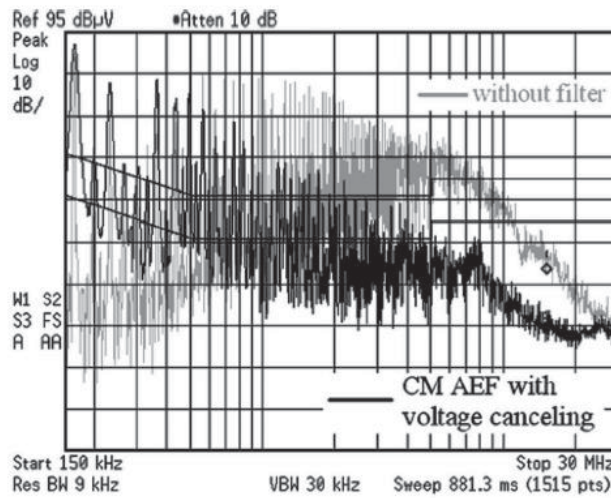


FIGURE 6.35 Compare of the noise level w/ and w/o the CDVCFB active filter. [29]

Other examples can be found in [26], [30]–[32].

6.5.3 CM Inverter Output Noise Filtering

CM noise on the inverter output is another common EMI issue in power converters. Compared to DM noise on the inverter output, CM noise is more likely to cause radiated emissions. Because of the limitation of the Y-capacitors, passive filters have to use bulky CM chokes to achieve the noise reduction requirement. As a result, the advantages of the active filter make it a very good option for the inverter output CM noise reduction.

A high voltage inverter normally has its DC bus isolated from the inverter chassis, as shown in FIGURE 6.36. As discussed in Chapter 4, the CM impedance of the motor is capacitive, and is on the order of hundreds of picofarads for medium-size electrical motors. The source impedance, which is the parasitic capacitance between the power MOSFETs / IGBTs and the inverter chassis, can be of the same order. Thus, in this case, both source and load impedances can be considered large in the active filter's targeted frequency range. As a result, the VDCC type active filter should be chosen.

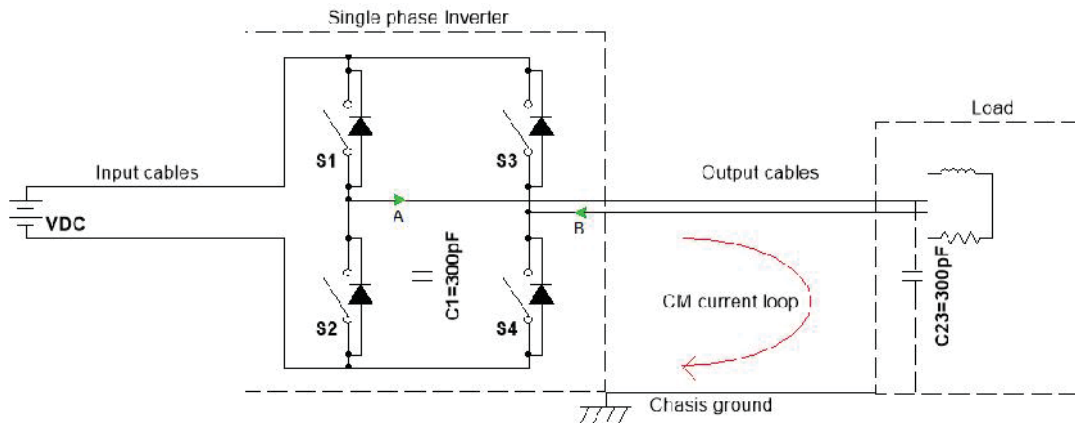


FIGURE 6.36 Inverter schematic: DC chassis isolated.

In practice, inverters normally employ Y-capacitors on the DC bus (FIGURE 6.37), with capacitance values that can be much greater than the parasitic capacitances. These Y-capacitors significantly lower the source impedance in our model and make the VDCC type active filter not a good choice anymore. Instead, VDVC type active filters should be chosen for this situation, according to Table 6.1. FIGURE 6.38 shows an application of the VDVCFF type active filter designed for a three-phase power inverter [33]. As shown in the figure, a class B push-pull amplifier is used. Other similar applications can be found in [28], [33]–[36].

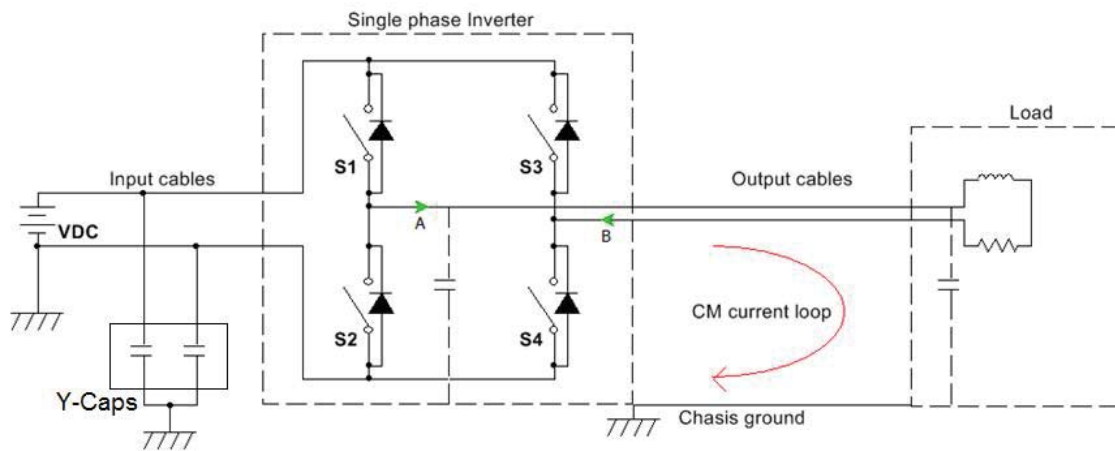


FIGURE 6.37 Inverter schematic: with Y capacitors.

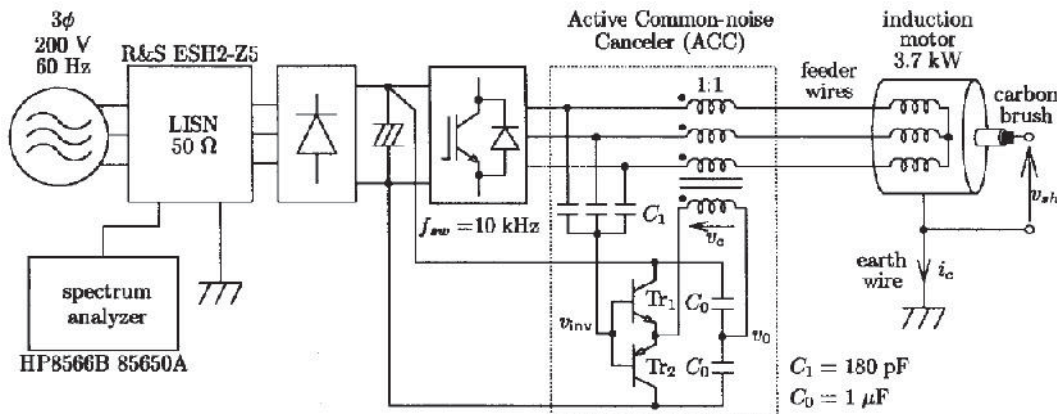


FIGURE 6.38 VDVC type active filter for inverter output CM noise reduction. [33]

7. NOISE CANCELLATION

This chapter will introduce a new method for EMI mitigation in power converters called the noise cancellation method. Depending on whether active devices are used, the noise cancellation method can be classified as either passive cancellation or active cancellation.

7.1 Cancellation Mechanism

Several approaches similar to the Noise Cancellation Method have appeared in the literature [37]–[44], some of which are classified as internal filters and others topological solutions. These approaches are similar to the new method in that the EMI noise is reduced by duplicating the EMI noise source, inverting the duplicated the source, and then compensating it back to the power system. These steps characterize a feed-forward type active filter, which detects the noise source and compensates a complementary signal (same magnitude, opposite polarity) back into the circuit. The difference between the two is the way they compensate the signal. Active filters electrically or magnetically couple the signal back into the circuit through capacitors or transformers. That's why they usually don't affect the converter topology and can be seen as external to the converter. The noise cancellation method, on the other hand, duplicates the noise coupling path of the converter to couple the signal back. It is often considered an integrated part of the power converter.

7.1.1 Ideal Cancellation

We will use the simple source-load model shown in FIGURE 7.1 as an example to explain the mechanism of how the noise cancellation method works. V_s , Z_s and Z_L are the noise source, source impedance and load impedance, respectively. V_1 is the voltage across the load, which is used to represent the EMI noise at the victim. The noise cancellation method creates a signal, V_s' , which has the same magnitude but opposite polarity of V_s , and the same coupling path ($Z_s' = Z_s$), as shown in FIGURE 7.2. Now the voltage across the load becomes V_2 . The noise reduction performance of this method can be evaluated by the insertion loss (IL), or V_1/V_2 .

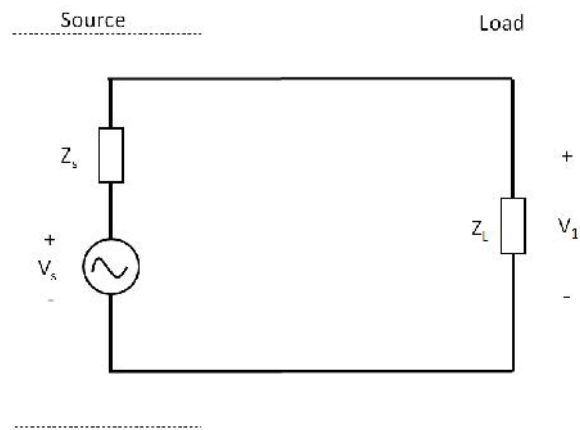


FIGURE 7.1 Noise source-load model.

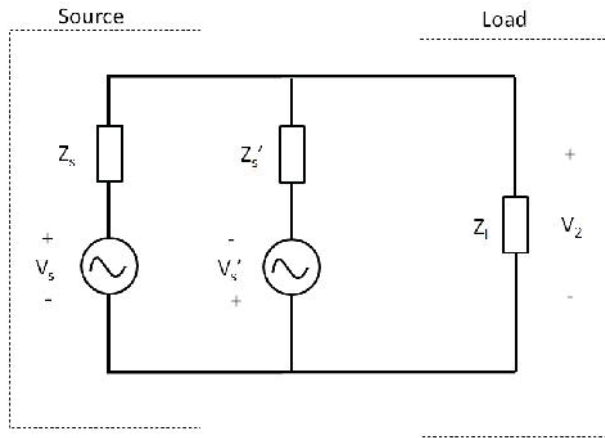


FIGURE 7.2 Noise cancellation model.

Using the voltage division and the superposition theorem, we have,

$$V_1 = \frac{Z_L}{Z_s + Z_L} V_s \quad (7.1)$$

$$V_2 = \frac{Z_L}{Z_s + Z_L} V_s - \frac{Z_L}{Z_s' + Z_L} V_s' \quad (7.2)$$

Ideally, if we have $V_s' = V_s$ and $Z_s' = Z_s$, V_2 becomes zero. This means IL is infinite and the noise cancellation is perfect. The noise current only circulates in the Z_s - Z_s' loop. This is the mechanism of the noise cancellation method.

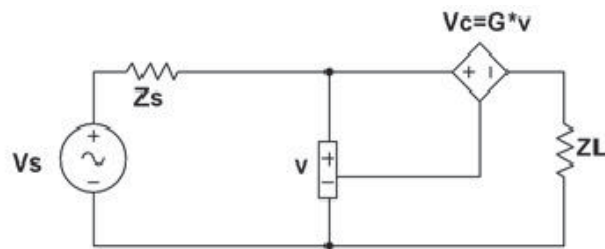


FIGURE 7.3 Type II feed-forward active filter model.

Comparing the noise cancellation model in FIGURE 7.2 with the Type II feed-forward active filter model in FIGURE 7.3, we can see that the active filter only duplicates the noise source.

7.1.2 Practical Cancellation

In practice, V_s and Z_s can't be perfectly duplicated. Assuming we have

$$V_s' = GV_s, \quad (7.3)$$

combining (7.1), (7.2) and (7.3), the IL of the cancellation circuit can be obtained by,

$$IL = \left| \frac{V_1}{V_2} \right| = \left| \frac{(2Z_L + Z_s')(2Z_L + Z_s)}{2Z_L(1-G)(Z_L + Z_s) + Z_s - GZ_s'} \right|, \quad (7.4)$$

where G represents the imperfect duplication factor of the noise source. If $Z_s = Z_s'$, (7.4) can be rewritten as,

$$IL_{Z_s=Z_s'} = \left| \frac{1}{1-G} \left(\frac{2Z_L + Z_s}{Z_s + Z_L} \right) \right|. \quad (7.5)$$

The IL of the VDVCFF type active filter discussed in Chapter 6 is,

$$IL_{VDVCFF} = \left| \frac{1}{1-G} \left(1 - \frac{GZ_s}{Z_s + Z_L} \right) \right| \quad (7.6)$$

where G is the gain of the compensated voltage relative to the source voltage, the same as the imperfect duplication factor. Comparing (7.5) and (7.6), we can see that the IL of the noise cancellation method is less dependent on the source and load impedance because,

$$1 \leq \left| \frac{2Z_L + Z_s}{Z_s + Z_L} \right| \leq 2 \quad (7.7)$$

(7.5) also suggests that the IL of the noise cancellation method depends on the quality of the duplicated noise. The closer G is to 1, the larger the IL will be.

Similarly, substituting $G = 1$ into (7.4), we have

$$\text{IL}_{G=1} = \left| \frac{(2Z_L + Z_s')(2Z_L + Z_s)}{Z_s - Z_s'} \right| \quad (7.8)$$

(7.8) suggests that the IL of the noise cancellation method also depends on the quality of the duplicated noise coupling path. The closer Z_s' is to Z_s , the larger the IL that can be achieved.

7.1.3 Noise Source and Coupling Path Duplication

Noise source duplication

In passive cancellation circuits, a transformer with opposite winding direction is used to duplicate the noise source and change its polarity, as shown in FIGURE 7.4. As a result, G in (7.4) and (7.5) is dependent on the chosen transformers. Just as in feed-forward type active filters, G should be designed to be close to one in the EMI noise band, and be close to zero in the power frequency range. Generally, the leakage inductance determines the lower end of the bandwidth of G , and the inter-winding parasitic capacitance affects the upper end of the bandwidth of G . The transformer model in FIGURE 6.19 also applies here.

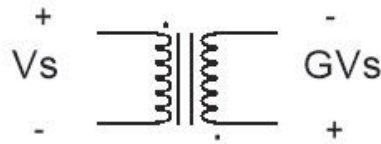


FIGURE 7.4 Passive noise source duplication example.

In active cancellation circuits, the noise source is often duplicated by adding additional MOSFET/IGBT legs that switch complementarily to the existing switches. Using the MOSFET bridge in FIGURE 7.5(a) as an example, the noise source is the pulse generated by the MOSFET switching. The noise source can be duplicated by adding another identical MOSFET leg and making it switch complementarily to the existing leg, as shown in FIGURE 7.5(b). The pulse generated by the added leg has the same magnitude but opposite polarity compared to the pulse from the existing leg.

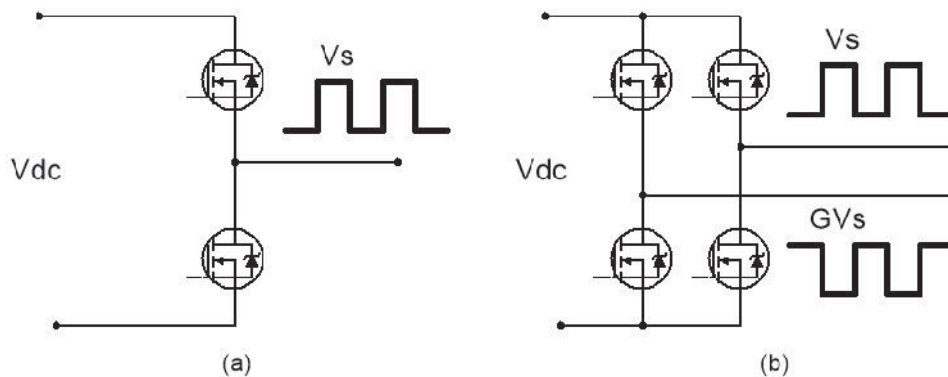


FIGURE 7.5 Active noise source duplication example: (a) MOSFET leg, (b) active noise duplication.

The difficulty in the active method is the switch control. A perfect match of the rising and falling edges is usually very difficult to achieve. (FIGURE 7.6)

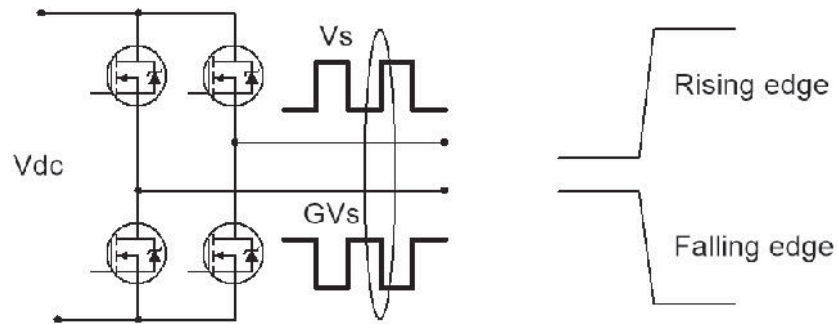


FIGURE 7.6 Switch control.

Coupling path duplication

To duplicate the coupling path, we need to characterize the coupling path first. For example, the common mode (CM) noise goes through the parasitic capacitances, C1 through C3, in the buck converter as shown in FIGURE 7.7. The parasitic capacitances and their associated loop inductances and resistances comprise the coupling path we need to duplicate. These parasitic parameters can be extracted using the measuring techniques introduced in Chapter 4. They can also be obtained by numerical simulation tools if the detailed converter model is available.

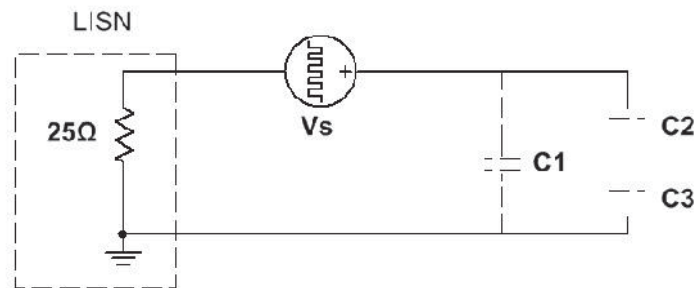


FIGURE 7.7 Coupling path for CM conducted emission in buck converters.

Since the parasitic parameters vary from device to device, it's very hard to achieve $Z_s = Z_s'$. From (7.8), we know the phase information of Z_s is a very sensitive factor. In the

above example, we know the parasitic capacitance dominates Z_s , in the frequency range of interest. If the variation of the parasitic capacitance is small, a lumped capacitor with approximately the same value could make the noise cancellation circuit work.

7.2 Passive Noise Cancellation

The passive cancellation method can be cost-effective for CM noise reduction in power converters. Applications of passive noise cancellation for CM conducted emissions reduction in DC-DC converter and CM output noise reduction in DC-AC inverters will be discussed here.

7.2.1 CM Conducted Emissions Reduction in non-isolated DC-DC Converters

Buck converter

FIGURE 7.8 shows the passive noise cancellation method applied in the synchronous buck converter. The dotted capacitor Z_s represents the parasitic capacitance between the low side MOSFET drain and the heatsink/converter chassis, which is the main coupling path for the CM conducted emissions. The circuit in the dotted box in the middle is the added noise cancellation circuit. A transformer is used to duplicate the noise source (voltage across the low side MOSFET). A lumped capacitor Z_s' is added to match Z_s . The load is the 25Ω LISN impedance in this case. Just as in the active filter, a filter capacitor, C_f , is used to isolate the power frequency current. If the noise current that flows through Z_s to the converter chassis, and the compensating current that flows from the chassis through Z_s' to the source are equal to each other, $I_{cm} = I_{comp}$, then the noise current only circulates within the converter and results in no CM conducted emissions.

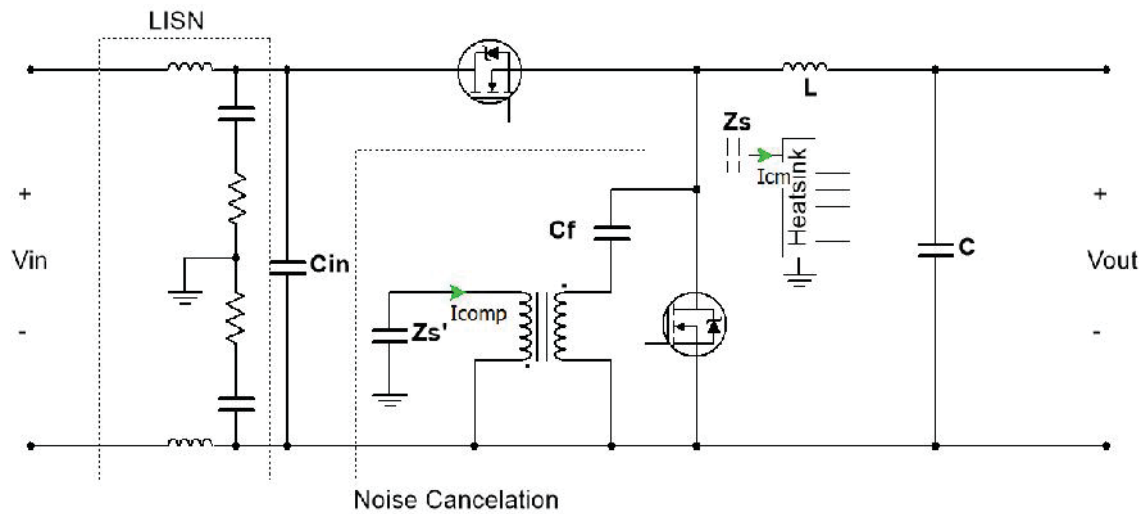


FIGURE 7.8 Passive noise cancellation in a synchronous buck converter with added transformer.

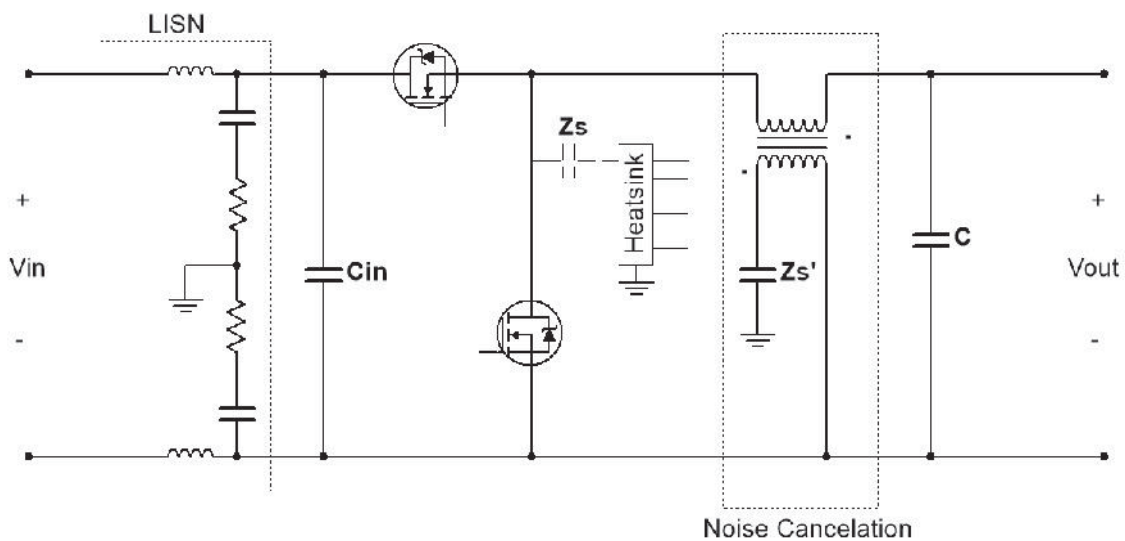


FIGURE 7.9 Passive noise cancellation in a synchronous buck converter with added winding.

Another way to duplicate the noise source in the buck converter without adding a transformer is to utilize the existing inductor, L , by just adding an anti-phase winding, as shown in FIGURE 7.9. This approach could potentially save money and PCB space. As shown in the figure, at the EMI frequency, the output capacitor, C , is considered a short circuit, thus the voltage across the primary winding of the inductor / transformer is the

noise source. Since the power frequency doesn't need to be isolated in this case, C_f can also be saved. (Z_s is large at the power frequency.)

Boost converter

Similarly, the boost converter can also use the passive noise cancellation method to mitigate CM conducted emissions. Two schemes using an additional transformer and added anti-phase winding are shown in FIGURE 7.10 and FIGURE 7.11, respectively.

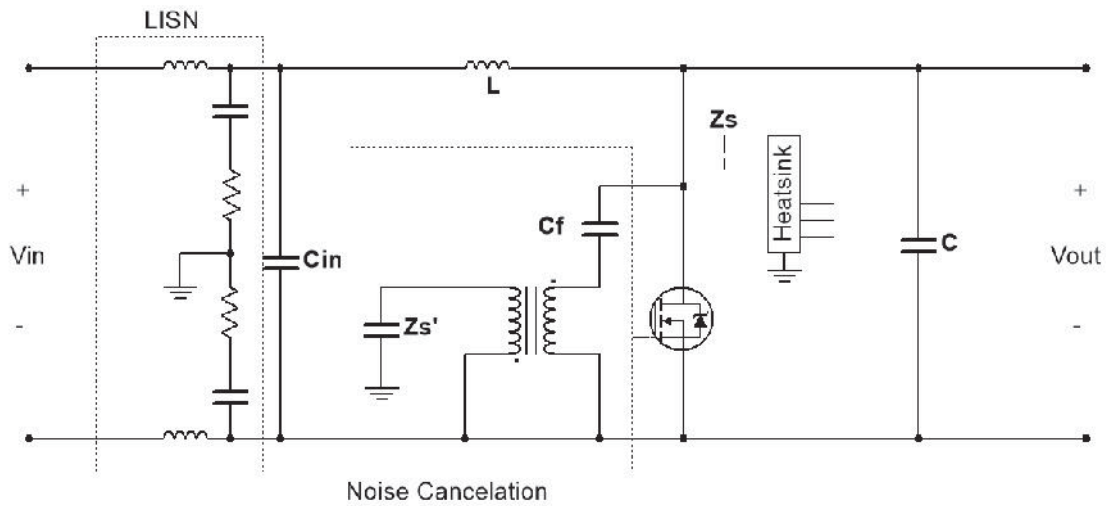


FIGURE 7.10 Passive noise cancellation in a boost converter with added transformer.

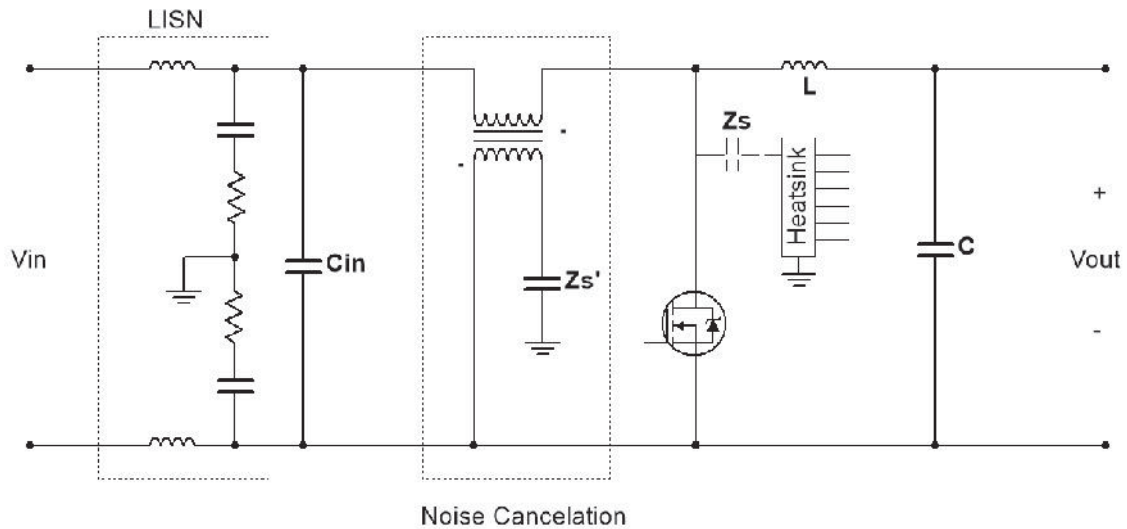


FIGURE 7.11 Passive noise cancellation in a boost converter with added winding.

Although utilizing an existing inductor to duplicate the noise source is cost-saving, the inductor has to operate in the power frequency band and may not be optimized for EMI noise duplication. For better control of the bandwidth of the noise cancellation, it is recommended that a new transformer be used to duplicate the noise source. Note that the added transformer can also be replaced by a unity gain amplifier with inverted output.

7.2.2 CM Conducted Emissions Reduction in Isolated DC-DC Converters

The passive noise cancellation application for CM conducted emissions reduction in isolated DC-DC converters is similar to the non-isolated case, because the noise source and the coupling path are very similar. FIGURE 7.12 and FIGURE 7.13 show the passive noise cancellation method used in a flyback DC-DC converter with an added transformer and added winding, respectively. As shown in the figures, the noise source is the voltage across the low side MOSFET and the coupling path is the parasitic capacitance between the MOSFET drain and the converter chassis, just as in the non-isolated converters.

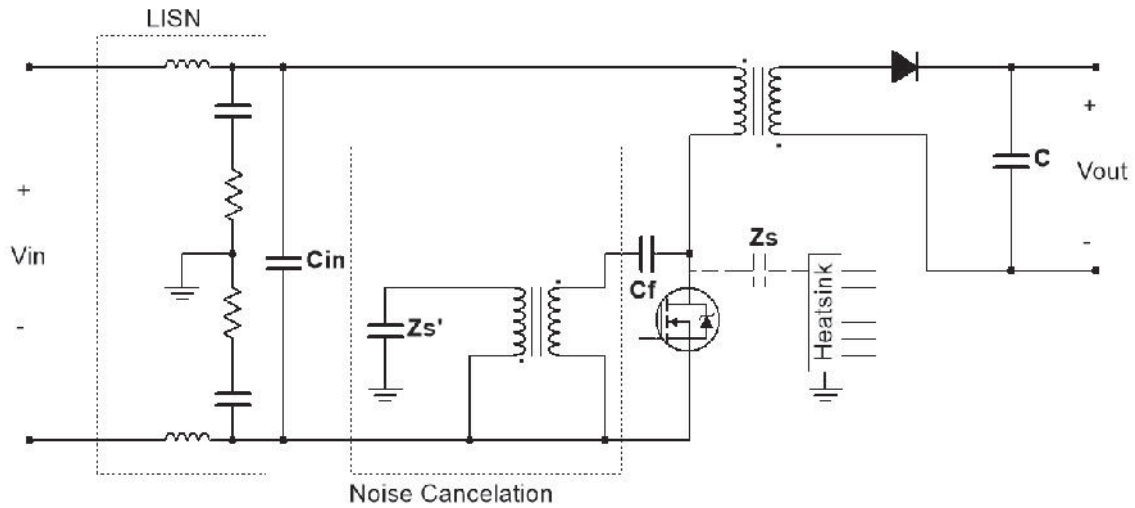


FIGURE 7.12 Passive noise cancellation in a flyback converter with added transformer.

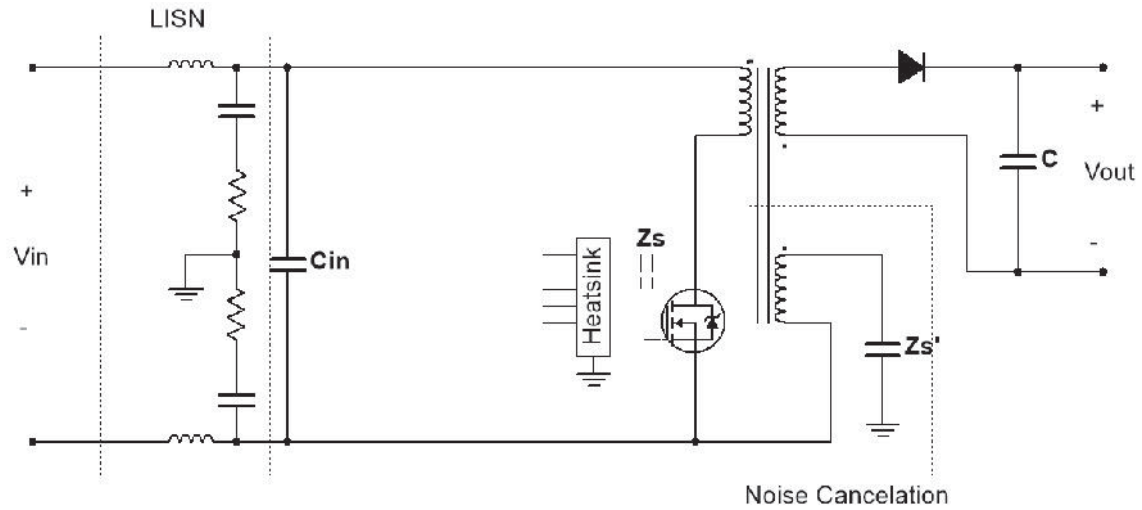


FIGURE 7.13 Passive noise cancellation in a flyback converter with added winding.

7.2.3 CM Noise Reduction in DC-AC Inverters

The DC-AC inverter has the same MOSFET / IGBT legs as the synchronous DC-DC converter, thus the CM conducted emissions can be reduced by the passive noise cancellation method in a similar way, as shown in FIGURE 7.14. The CM noise voltage is detected by the capacitor network, similar to the approach used with active filters. It is

then duplicated by a transformer. Since there are no inductors in the inverter topology, the anti-phase winding option no longer applies here.

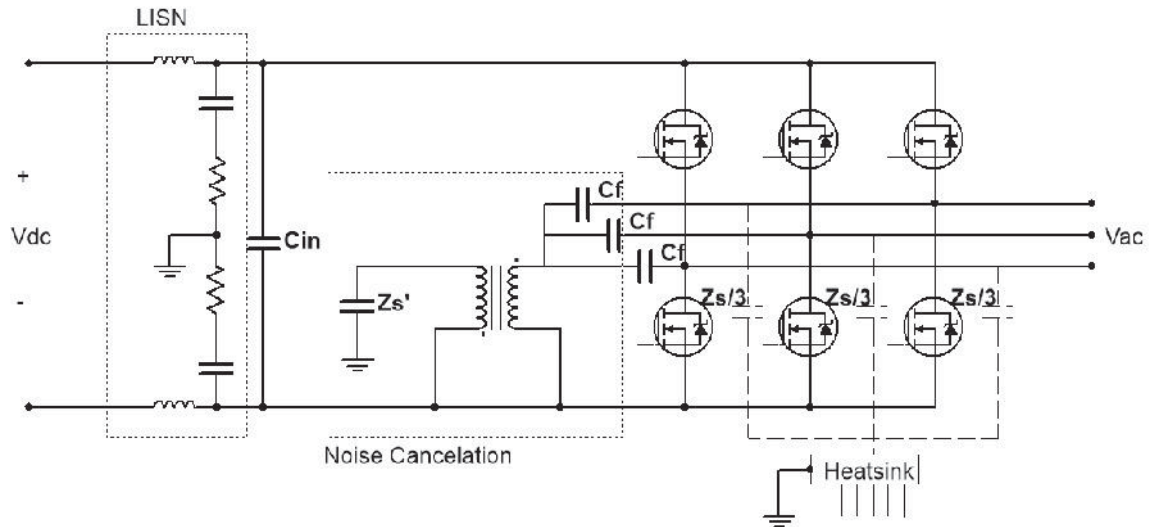


FIGURE 7.14 Passive noise cancellation for CM conducted emissions reduction in a three phase inverter.

For inverters, we are also interested in reducing the CM noise on the output phase cables, which may cause radiated emissions and other issues. The CM output noise source is the same as the CM conducted emissions source, which is the CM phase voltage relative to the inverter chassis. The coupling path, however, is different. As shown in FIGURE 7.15, assuming the DC bus is isolated from the inverter chassis, the CM current flows through the parasitic capacitance between the load and the chassis, Z_L , to the chassis, and through the parasitic capacitance between the DC bus and the chassis, Z_s ($3 \times Z_s/3$), back to the source. According to the noise cancellation mechanism, we need to duplicate the source and one of the impedances, Z_s or Z_L . The reason that we have two options here for coupling path duplication is illustrated in FIGURE 7.16, which shows an alternative way to cancel the noise current, I_s . This model treats the load Z_L as the

coupling path and cancels the noise current by making the noise current circulate inside the $Z_L' - Z_L$ loop, which is different from the passive cancellation model in FIGURE 7.2. For conducted emissions reduction this is not an option because this alternative method does not cancel the voltage, V_2 , appearing on the load (LISN).

FIGURE 7.15 and FIGURE 7.17 show the passive noise cancellation schematic for phase noise reduction in a three-phase power inverter with Z_s and Z_L duplicated. In the case when Z_L is duplicated, the cancellation circuit makes the noise current circulate in the Z_L-Z_L' loop in an ideal situation. As a result, we need to extend the wire that connects the source and Z_L' to minimize the Z_L-Z_L' loop. In other word, by duplicating Z_L , we cannot reduce the CM current on the three phase cables. We are adding another cable in parallel with the three phase cables so that the CM current on all four cables can be canceled out. Compared to the duplication of Z_s , this requires more modifications to the system, such as the additional output cable.

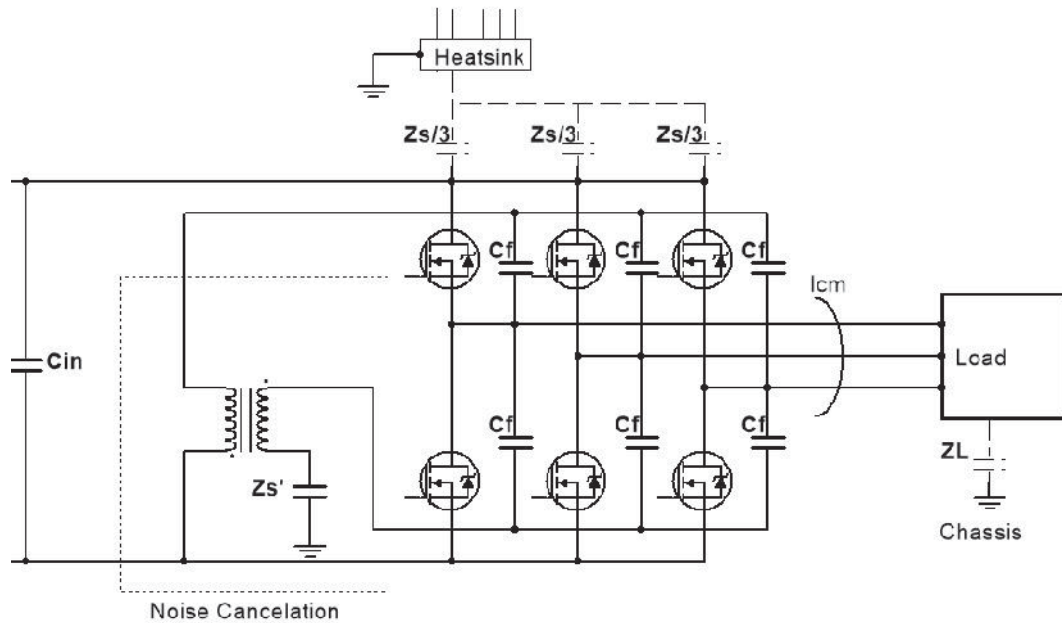


FIGURE 7.15 Passive noise cancellation for CM output noise reduction in a three phase inverter with Z_s duplicated.

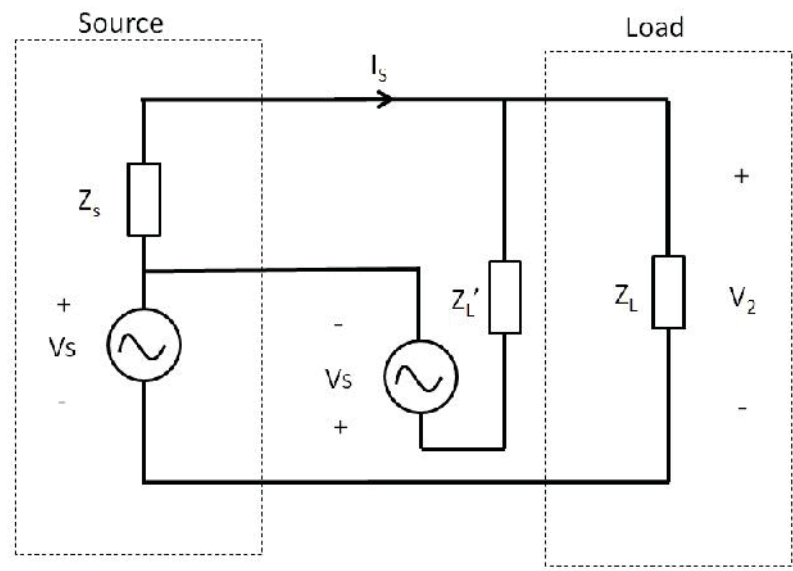


FIGURE 7.16 Alternative passive cancellation model.

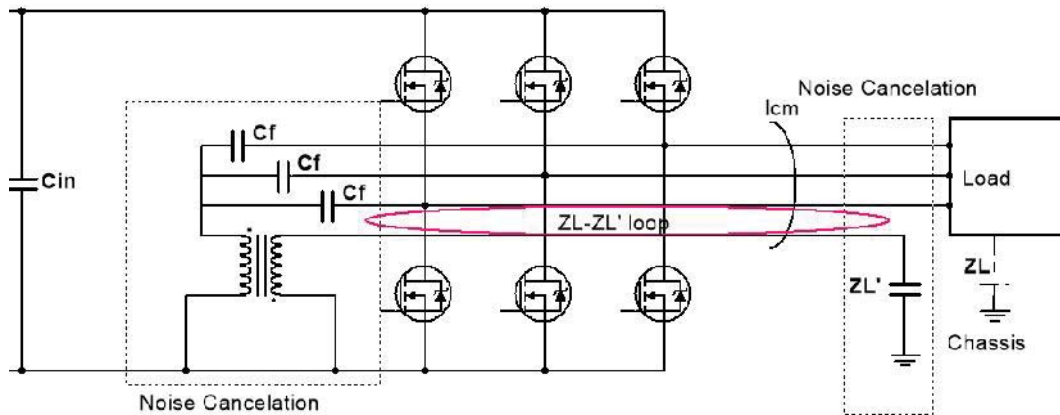


FIGURE 7.17 Passive noise cancellation for CM phase noise reduction in a three phase inverter with Z_L duplicated.

7.3 Active Noise Cancellation

The active cancellation method can also be used for CM noise reduction in power converters. We will discuss several active cancellation topologies here.

7.3.1 Complementary Switching Topology

To duplicate the noise source, an identical switch leg with a complimentary switching pattern can be employed. An example of the synchronous buck converter is shown in FIGURE 7.18. An identical MOSFET leg is added to the existing one. The voltage across the low side MOSFET of the added leg has the same magnitude and opposite polarity as the noise source resulting from the complementary switching. For the coupling path, as shown in the figure, the parasitic capacitance Z_s' of the added leg should be close to Z_s with a good layout.

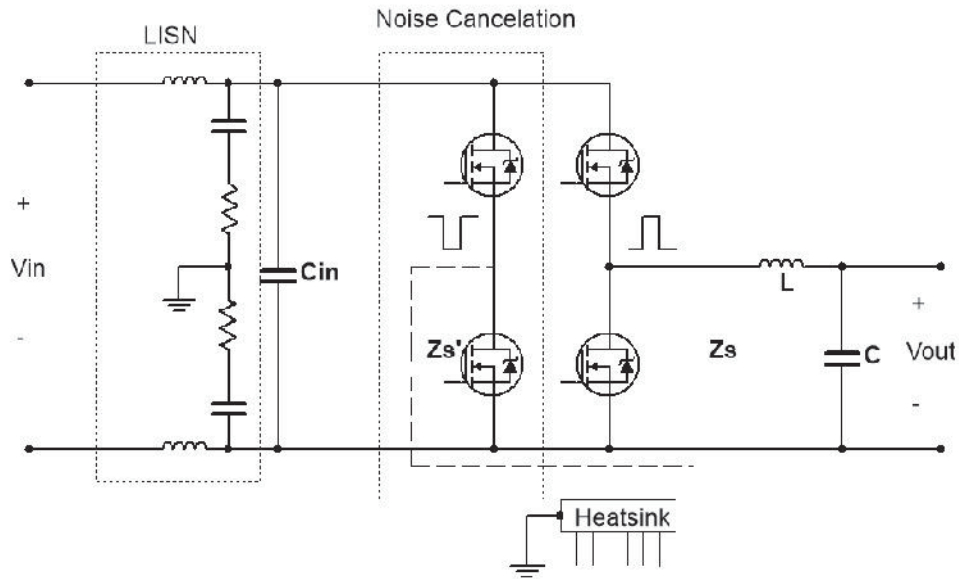


FIGURE 7.18 Active noise cancellation for CM conducted emissions reduction in synchronous buck converter.

For canceling the CM noise on inverter output phase cables, the complementary switching method can also be used. Just as with the passive cancellation method, either Z_s or Z_L must be duplicated, as shown in FIGURE 7.19 and FIGURE 7.20, respectively. When duplicating Z_L , the fourth cable is also required. This topology is referred to as the fourth-leg topology in [38]. As shown in FIGURE 7.19 and FIGURE 7.20, besides the simultaneous switching challenge, the added leg must be switched complementary to all the other three bridges. For example, if phase A ties high and generates a rising edge in the CM noise voltage, the added leg needs to be tied low to generate a falling edge canceling signal. If phase B ties high next in the sequence, the added leg which is already tied low can't be tied low again. As a result, this method restricts the driving scheme of the converter. Details of the driving scheme will be discussed in Chapter 8.

Also, adding a leg is more expensive than adding a small transformer or an amplifier.

With respect to cost, this is not as good an option as passive cancellation.

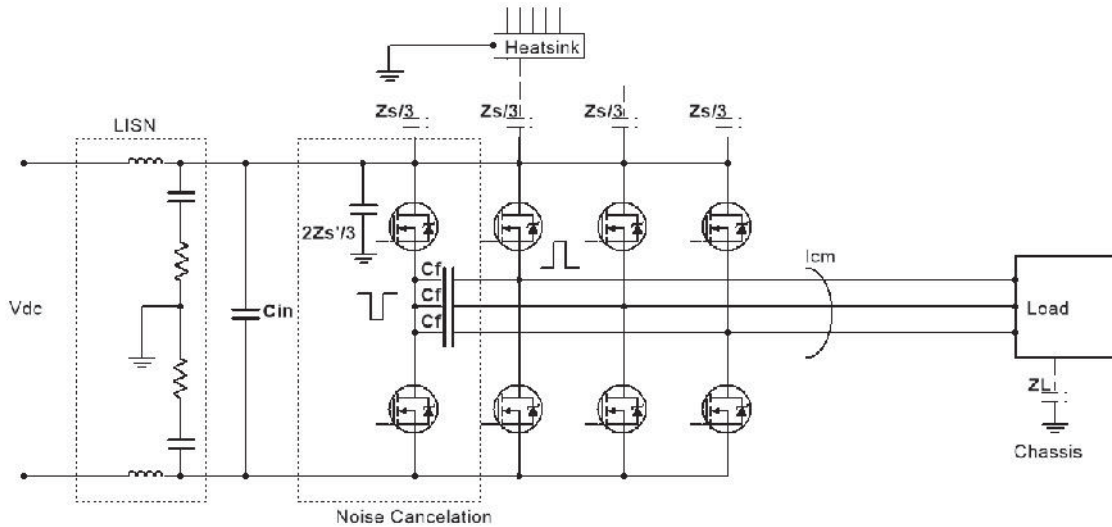


FIGURE 7.19 Active noise cancellation for CM phase noise reduction in a three phase inverter with Z_s duplicated.

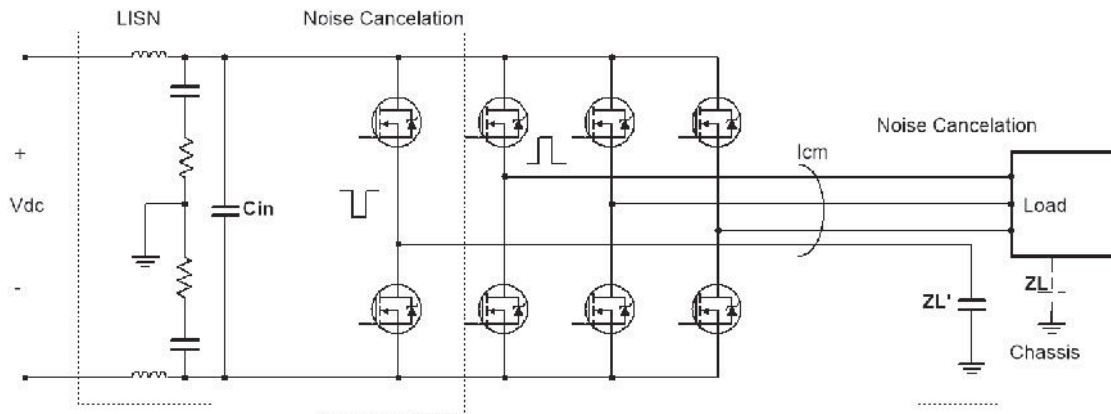


FIGURE 7.20 Active noise cancellation for CM phase noise reduction in a three phase inverter with Z_L duplicated.

7.3.2 Dual-Fed Topology

Dual-fed topology also utilizes complementary switching to duplicate the noise source. It solves the driving scheme restriction issue with the fourth-leg topology at a cost

of two additional switch legs and a dual-winding motor. As shown in FIGURE 7.21, the dual-fed topology is designed to cancel the CM output noise in the three phase motor drive. The mechanism of the cancellation method is to duplicate the CM noise source with the three additional switch legs, and to duplicate Z_L by using the dual-winding motor. Since there are three additional legs, any combination of the switching can be complementarily compensated. The result is the CM noise is reduced on all six phase cables. Compared to the fourth-leg topology, although it has two additional bridges, all the power MOSFETs are used to drive the motor. In other words, for a given power output, the required power rate for each MOSFET is lowered. However, the dual-winding motor is not as common as the single winding motor, and thus may result in increased system cost.

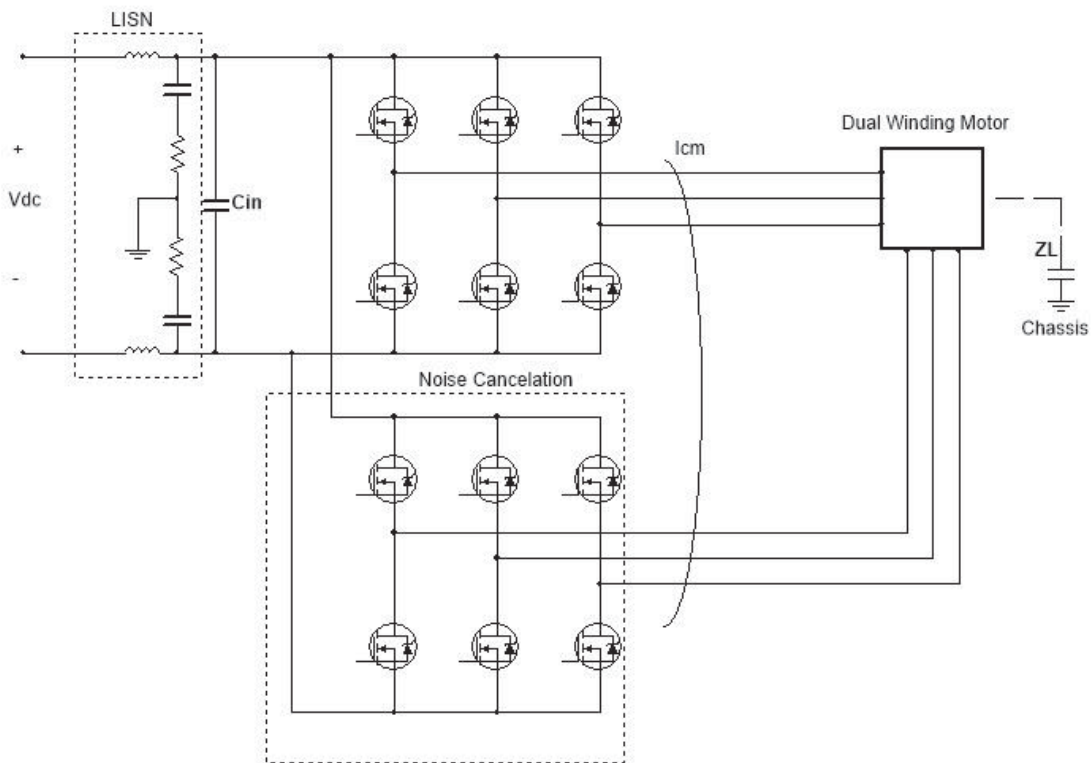


FIGURE 7.21 Dual-fed noise cancellation topology for CM phase noise reduction in a three phase inverter.

A multilevel inverter also adds MOSFET bridges, and thus offers more switching combinations and can reduce the CM noise on the inverter output [45]. However, it doesn't duplicate the coupling path, thus is not classified as an active noise cancellation method.

8. COMMON MODE NOISE SOURCE REDUCTION

The common mode (CM) noise source reduction method is based solely on the switching pattern modification to cancel or reduce the CM noise source. Compared to the filtering and topological cancellation solutions, it requires neither additional components nor topological modifications to the power converter, thus is the most cost-effective solution among the all. This chapter will introduce its mechanism and its application in the three-level-three-phase voltage source power inverters.

8.1 Noise Source Reduction Mechanism

As its name implies, the CM noise source reduction method reduce the CM noise source only. It modifies the switching sequence in a PWM cycle to cancel or reduce the CM noise. Compared to the other hardware based modification, this solution is all about the software.

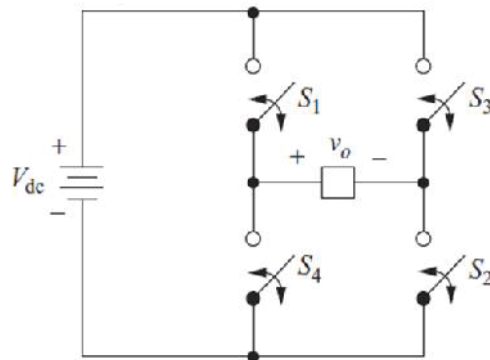


FIGURE 8.1 Full-bridge inverter.

The full-bridge DC-AC inverter shown in FIGURE 8.1 will be used as an example to show how the CM noise source is reduced. To output a sinusoidal waveform, one period of the sine wave is divided into many PWM cycles, as shown in FIGURE 8.2. In each

PWM cycle, an average voltage, referred to as the reference voltage, will be generated by the inverter as shown in the figure. For example, to generate a reference voltage, DV_{dc} , in one PWM cycle, S_1 will be on and S_4 will be off for a time of DT as shown in FIGURE 8.3(a). When S_1 and S_2 are both closed, the output differential mode (DM) voltage, V_o , equals V_{dc} . When S_2 and S_4 are both closed, $V_o = 0$. As a result the average output voltage can be found by,

$$\begin{aligned} V_{o.avg} &= \frac{V_{dc} \cdot DT}{T} \\ &= DV_{dc} \quad . \\ &= V_{ref} \end{aligned} \quad (8.1)$$

The CM voltages are also plotted in FIGURE 8.3(a). Similarly, to generate the reference voltage, $-DV_{dc}$, the switching pattern in FIGURE 8.3(b) can be used, and the DM and CM output voltages are plotted in the same figure.

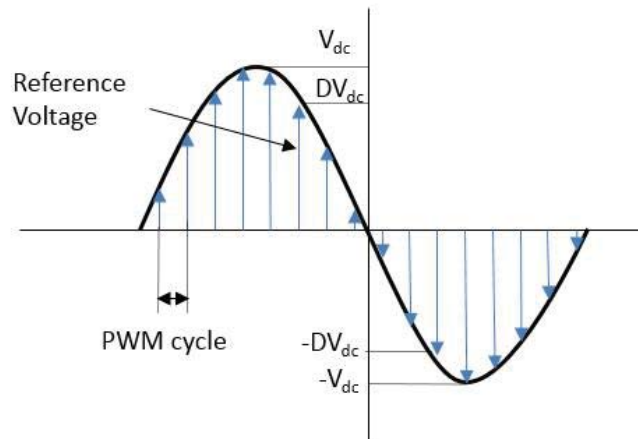


FIGURE 8.2 PWM scheme for sinusoidal waveform output.

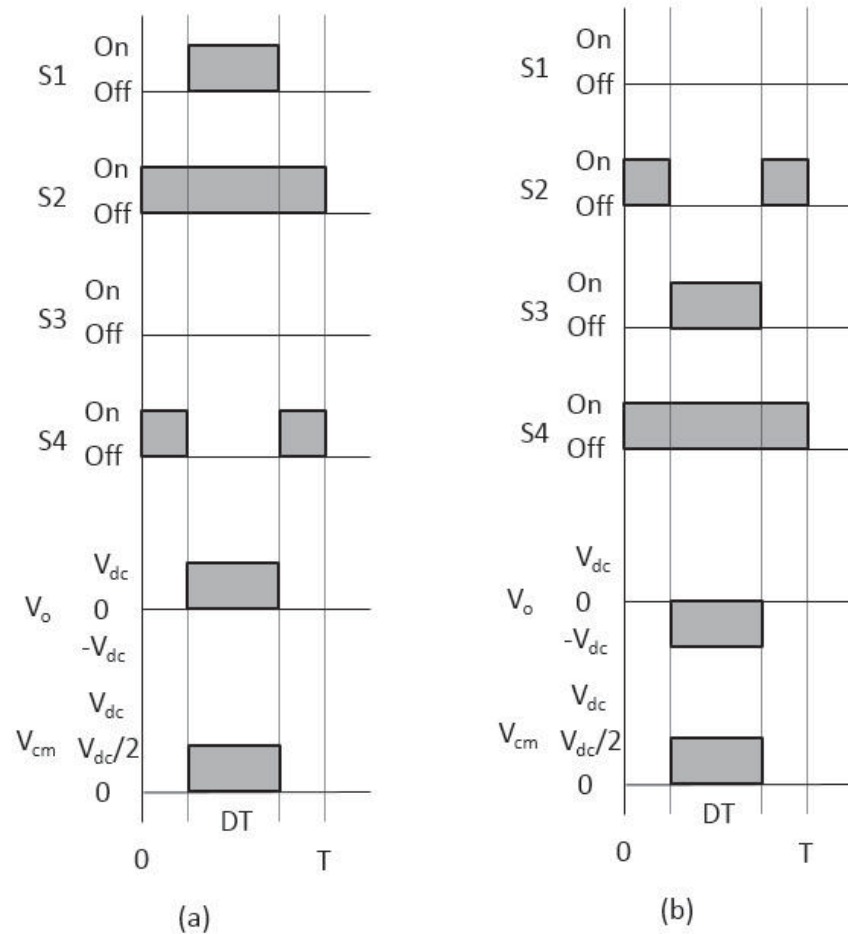


FIGURE 8.3 Switching schemes in one PWM cycle: (a) $V_{ref} = DV_{dc}$, (b) $V_{ref} = -DV_{dc}$.

As discussed in Chapter 3, the CM voltage at the inverter output couples noise to the power lines (or LISN) through the parasitic capacitances between the power switches and the inverter chassis. It also generates CM current flowing through the parasitic capacitances between the load to the chassis ground.

Unlike the noise cancellation method, which duplicates both the noise source and the coupling path, the CM noise source reduction method only modifies the switching pattern to reduce the CM noise source. Because there are no topological changes in the inverter, any passive or active filter can be added for additional noise attenuation. As shown in

FIGURE 8.3, the traditional switching pattern only closes one switch at a time. If simultaneous switching is allowed, the switching pattern can be modified so that S1 and S2 are turned on and off at the same time to output V_{dc} , as shown in FIGURE 8.4(a). The duty cycle is changed to $(1+D)T/2$, so that the average output voltage in the PWM cycle is,

$$\begin{aligned}
 V_{o.avg} &= \frac{\frac{(1+D)}{2}TV_{dc} + \frac{(1-D)}{2}T(-V_{dc})}{T} \\
 &= DV_{dc} \\
 &= V_{ref}
 \end{aligned} \tag{8.2}$$

The modified switching pattern results in a constant CM voltage of $V_{dc}/2$ relative to the DC negative. It theoretically eliminates the CM noise source. Similarly, the switching pattern can be modified to output $-DV_{dc}$ with CM noise eliminated as shown in FIGURE 8.4(b).

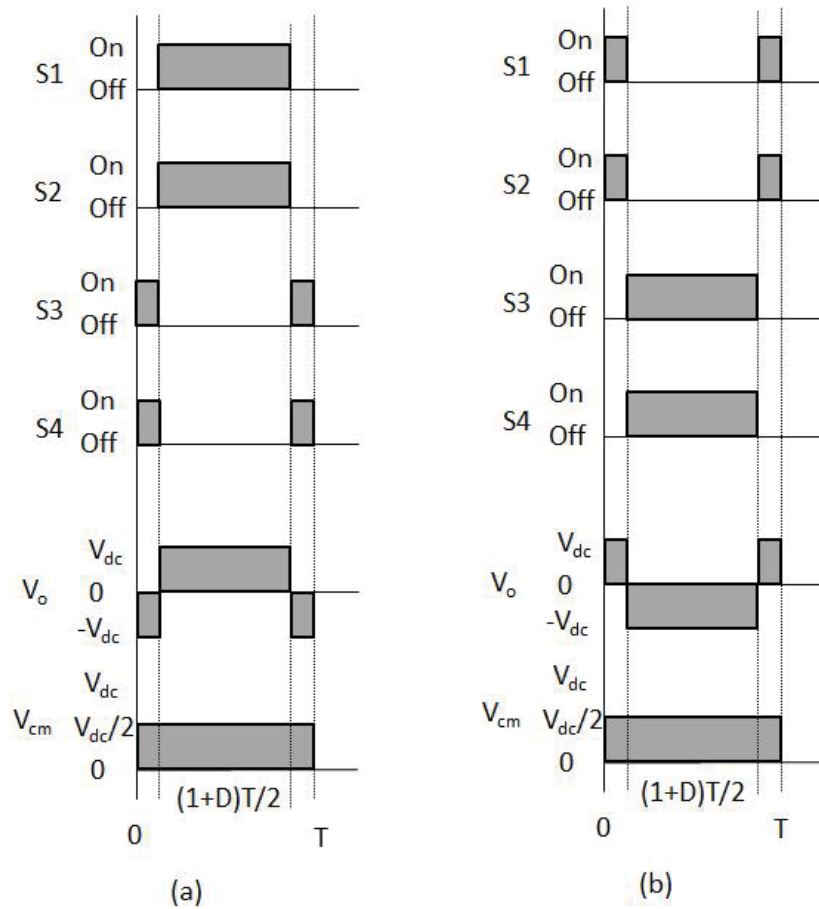


FIGURE 8.4 Modified switching schemes in one PWM cycle: (a) $V_{ref} = DV_{dc}$, (b) $V_{ref} = -DV_{dc}$.

The vector approach can also be used to analyze the PWM scheme. As shown in FIGURE 8.5(a), \mathbf{V}_0 , \mathbf{V}_1 , \mathbf{V}_2 and \mathbf{V}_3 , denote the inverter output voltage vectors. When S1 and S3 are closed, the output voltage is denoted \mathbf{V}_0 . When S1 and S2 are closed, the output is \mathbf{V}_1 . When S3 and S4 are closed, the output is \mathbf{V}_2 . When S3 and S4 are closed, the output is \mathbf{V}_3 . Both \mathbf{V}_1 and \mathbf{V}_2 have a magnitude of V_{dc} but are 180 degrees out of phase, and \mathbf{V}_0 and \mathbf{V}_3 are zero vectors, as shown in FIGURE 8.5(a). To generate the reference voltage, \mathbf{V}_{ref} , different combinations of these inverter output vectors can be used. For example, the traditional switching pattern in FIGURE 8.3(a) uses \mathbf{V}_0 and \mathbf{V}_1 to

generate the reference voltage, V_{ref} , while the modified switching pattern in FIGURE 8.4(a) uses V_1 and V_2 to generate V_{ref} , as shown in FIGURE 8.6. The two different switching patterns both output an average voltage of V_{ref} in the PWM cycle, however, result in different CM voltages.

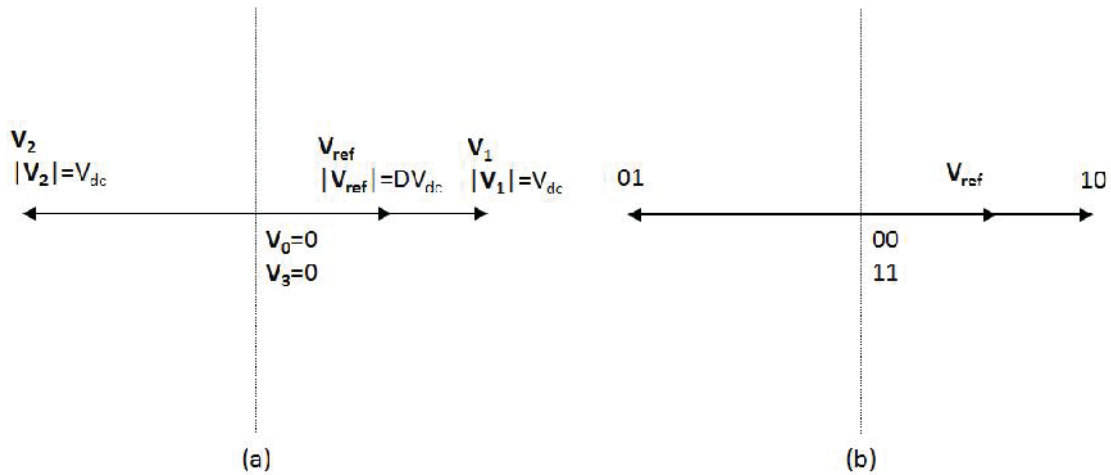


FIGURE 8.5 Vector representations of the full-bridge inverter output: (a), by the vector name, (b), by the ‘0-1’ notation.

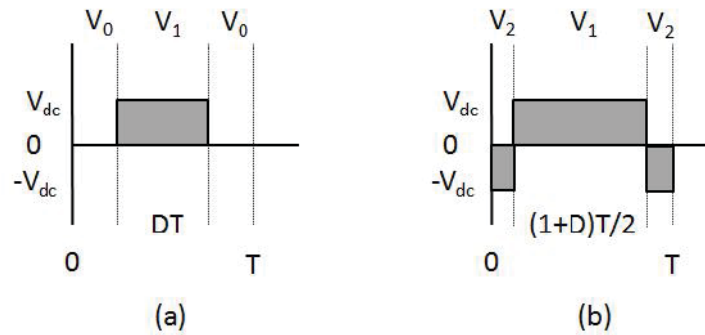


FIGURE 8.6 Vectors used to generate the reference voltage: (a) traditional scheme, (b) modified scheme.

The voltage vectors, V_0 , V_1 , V_2 and V_3 , can also be represented by the states of each inverter leg. We use ‘1’ to represent a high output (high side switch on and low side switch off) and ‘0’ to represent a low output (high side switch off and low side switch on).

For example, V_1 can be represented by 10 because the left leg of the inverter is high and the right leg is low. Similarly, V_2 can be represented by 01 and V_0, V_3 are 00 and 11, respectively, as shown in FIGURE 8.6(b). The CM voltage can be found by averaging the two numbers in the '0-1' denotation of the voltage vector and multiply it with the DC input voltage. For example, the traditional switching scheme in FIGURE 8.3(a) used 00-10-00 to generate V_{ref} . We would expect that the CM voltage changes from 0 to $V_{dc}/2$ and then to 0. The modified switching scheme in FIGURE 8.4(a) only uses 10 and 01 to generate the V_{ref} . We would expect the CM voltage to be at constant $V_{dc}/2$.

Note the above CM voltage analysis used the DC negative as the reference. If the inverter has balanced Y-capacitors at the power line, the chassis voltage should be $V_{dc}/2$. The CM noise source reduction method is based solely on the modification of the PWM switching patterns, thus doesn't have any additional cost to the product. We will explore its application in the most popular three-phase motor drives next and discuss the disadvantages of this method.

8.2 Application in the Three-Phase Power Inverter

The application of the noise source reduction method in the three-phase motor drives is based on the modification of the PWM driving schemes. Different modified schemes will be introduced here.

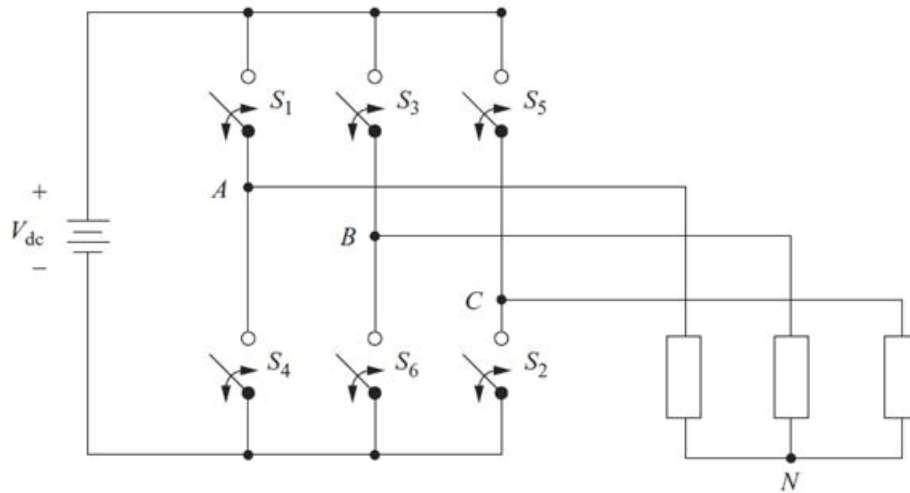


FIGURE 8.7 Three-phase inverter.

8.2.1 PWM Driving Schemes

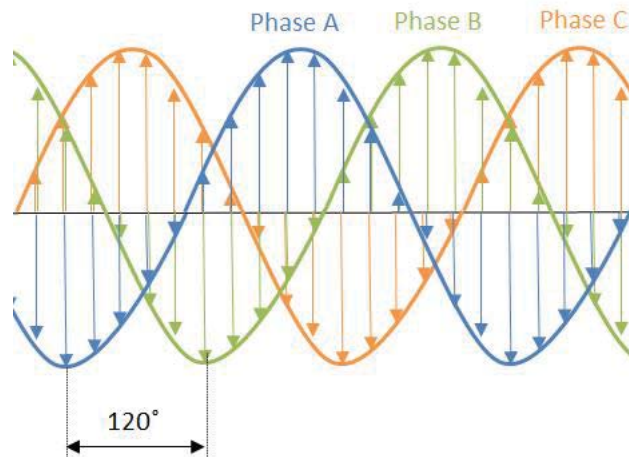


FIGURE 8.8 Three-phase inverter output.

Similar vector approaches can be applied to the three-phase power inverter. For example, an inverter drives a motor at a constant speed, by outputting three sinusoidal waveforms with the same magnitude and 120 degrees apart from each other, as shown in FIGURE 8.8. In each PWM cycle, although the reference voltages of each inverter leg varies in magnitudes and phases, the vector sum of the three reference voltages is a space vector with its tip on a circular locus that rotates at the same frequency as the sinusoidal

inverter outputs, as shown in FIGURE 8.9. The vector, V_1 , representing only phase A has a high output (phase A is tied high, phase B and C are tied low), is at 0° position. V_3 and V_5 , representing only phase B and only phase C has a high output, respectively, are 120° and 240° apart from V_1 , respectively. The eight different inverter outputs are $V_0(000)$, $V_1(100)$, $V_2(110)$, $V_3(010)$, $V_4(011)$, $V_5(001)$, $V_6(101)$ and $V_7(111)$. Vectors, V_2 , V_4 and V_6 , are the opposite switching combinations to the vectors, V_1 , V_3 and V_5 , respectively. V_0 , V_7 are zero vectors. The six active vectors and the two zero vectors divide the space into six segments as shown in FIGURE 8.9.

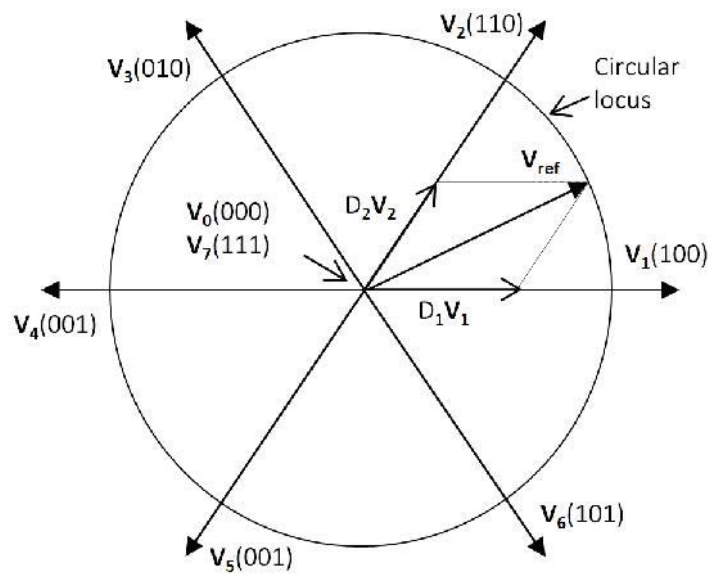


FIGURE 8.9 Generation of the reference voltage by SVPWM.

SVPWM

The Space-Vector-Pulse-Width-Modulation (SVPWM) generates the reference voltage, V_{ref} , by using its two adjacent vectors and the two zero vectors. For example, to generate the V_{ref} between 0° and 60° , V_0 , V_1 , V_2 and V_7 are used as shown in FIGURE

8.9. The sequence of the switching is V_7 - V_2 - V_1 - V_0 - V_1 - V_2 - V_7 , as shown in FIGURE 8.10. The duty cycles for V_1 and V_2 are D_1 and D_2 , respectively. The average output voltage of the PWM cycle can be found by summing the four inverters,

$$\begin{aligned} \overline{V_{o.avg}} &= \frac{1-D_1-D_2}{2} \overline{V_0} + D_1 \overline{V_1} + D_2 \overline{V_2} + \frac{1-D_1-D_2}{2} \overline{V_7} \\ &= D_1 \overline{V_1} + D_2 \overline{V_2} \\ &= \overline{V_{ref}} \end{aligned} \quad , \quad (8.3)$$

as shown in FIGURE 8.9. Reference voltages at other sections of the space can be generated in a similar way.

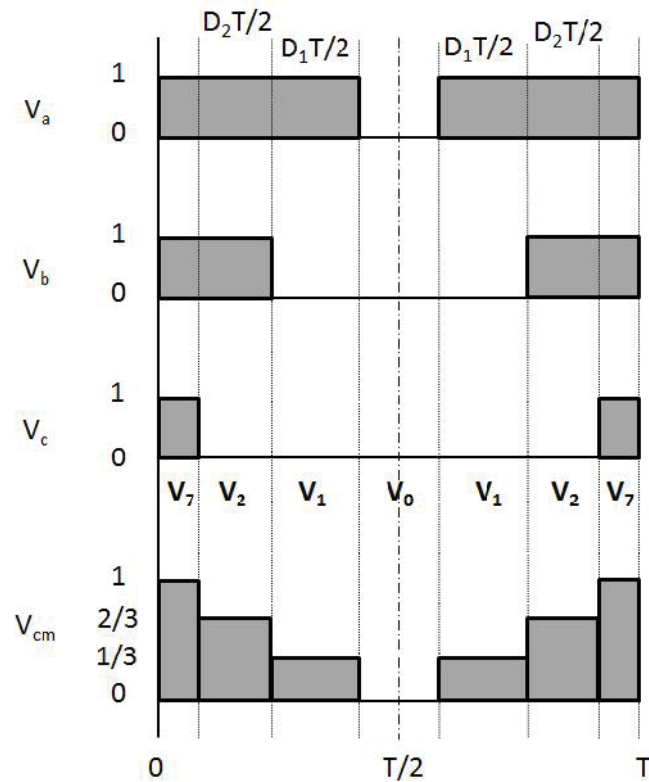


FIGURE 8.10 Switching pattern of SVPWM.

The CM output voltage relative to the DC negative in this PWM cycle changes between 0 and 1, as shown in FIGURE 8.10, where ‘1’ represents V_{dc} . Next, we will introduce other PWM driving schemes that can reduce the CM voltage.

AZSPWM I

The Active-Zero-State-Pulse-Width-Modulation (AZSPWM) scheme generates the reference voltage, V_{ref} , by using its two adjacent vectors and another two opposite active (non-zero) vectors. Compared to the SVPWM, AZSPWM uses two opposite active vectors of the same magnitude (same duty cycle) to replace the zero vectors (as its name implies). Depending on the selection of the opposite active vectors, different types of AZSPWM schemes were proposed in [46]–[49]. As shown in FIGURE 8.11(a), the Type I AZSPWM generates V_{ref} by using V_0 , V_1 , V_3 and V_6 . The sequence of the switching is V_3 - V_2 - V_1 - V_6 - V_1 - V_2 - V_3 , as shown in FIGURE 8.11(b). The duty cycles for V_1 and V_2 are D_1 and D_2 , respectively and the duty cycles for V_3 and V_6 are both $(1-D_1-D_2)/2$. Because V_3 and V_6 are opposite vectors, the average output voltage in this PWM cycle can be found by,

$$\begin{aligned}\overline{V_{o.avg}} &= D_1\overline{V_1} + D_2\overline{V_2} + \frac{1-D_1-D_2}{2}\overline{V_3} + \frac{1-D_1-D_2}{2}\overline{V_6} \\ &= D_1\overline{V_1} + D_2\overline{V_2} \quad , \quad (8.4) \\ &= \overline{V_{ref}}\end{aligned}$$

as shown in FIGURE 8.11(a).

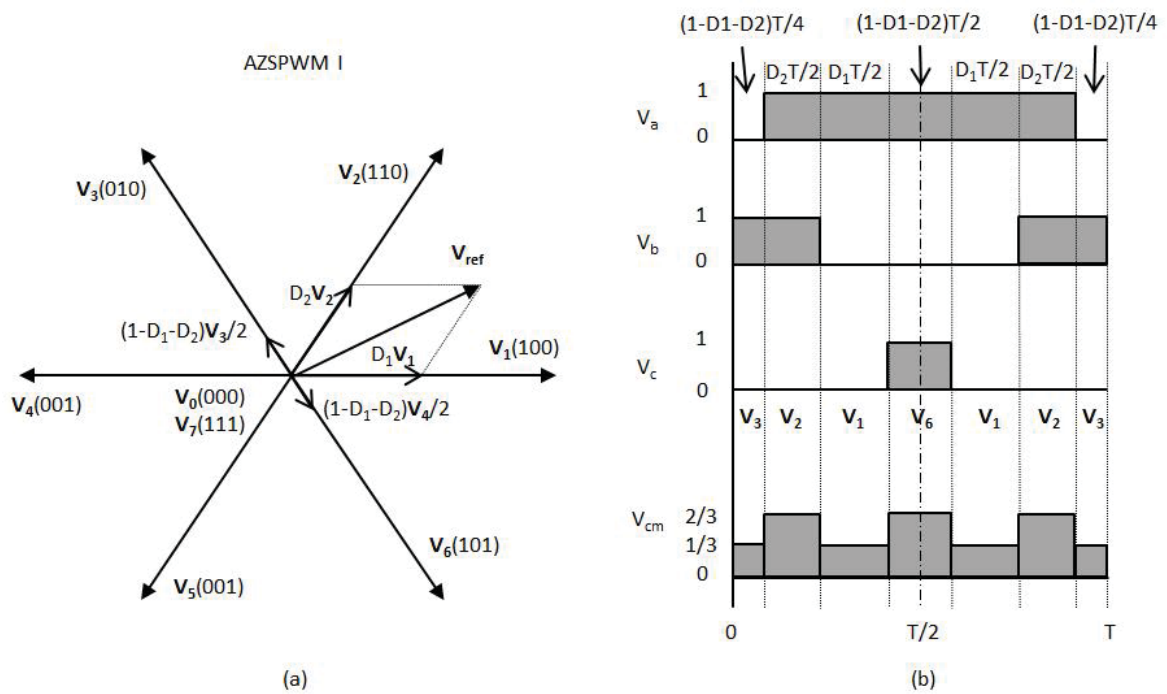


FIGURE 8.11 AZSPWM I: (a) generation of the reference voltage, (b) switching pattern.

The CM voltage of the Type I AZSPWM in a PWM cycle varies from $1/3$ to $2/3$, as shown in FIGURE 8.11(b). As a result, the CM noise magnitude of AZSPWM I is only $1/3$ of that of the SVPWM.

AZSPWM II

Type II AZSPWM uses one of the adjacent vectors as one of the opposite active vector as shown in FIGURE 8.12(a). As a result, the total number of the used vectors to generate V_{ref} is only three. The duty cycles of the V_1 and V_4 are $(1+D_1-D_2)/2$ and $(1-D_1-D_2)/2$, respectively. Since $V_4 = -V_1$, the average output voltage in this PWM cycle can be found by,

$$\begin{aligned}
\overline{V_{o,avg}} &= \frac{1+D_1-D_2}{2} \overline{V_1} + D_2 \overline{V_2} + \frac{1-D_1-D_2}{2} \overline{V_4} \\
&= \frac{1+D_1-D_2}{2} \overline{V_1} + D_2 \overline{V_2} - \frac{1-D_1-D_2}{2} \overline{V_1} , \\
&= D_1 \overline{V_1} + D_2 \overline{V_2} \\
&= \overline{V_{ref}}
\end{aligned} \tag{8.5}$$

as shown in FIGURE 8.12(a). The sequence of the switching is V_1 - V_2 - V_4 - V_2 - V_1 , as shown in FIGURE 8.12(b).

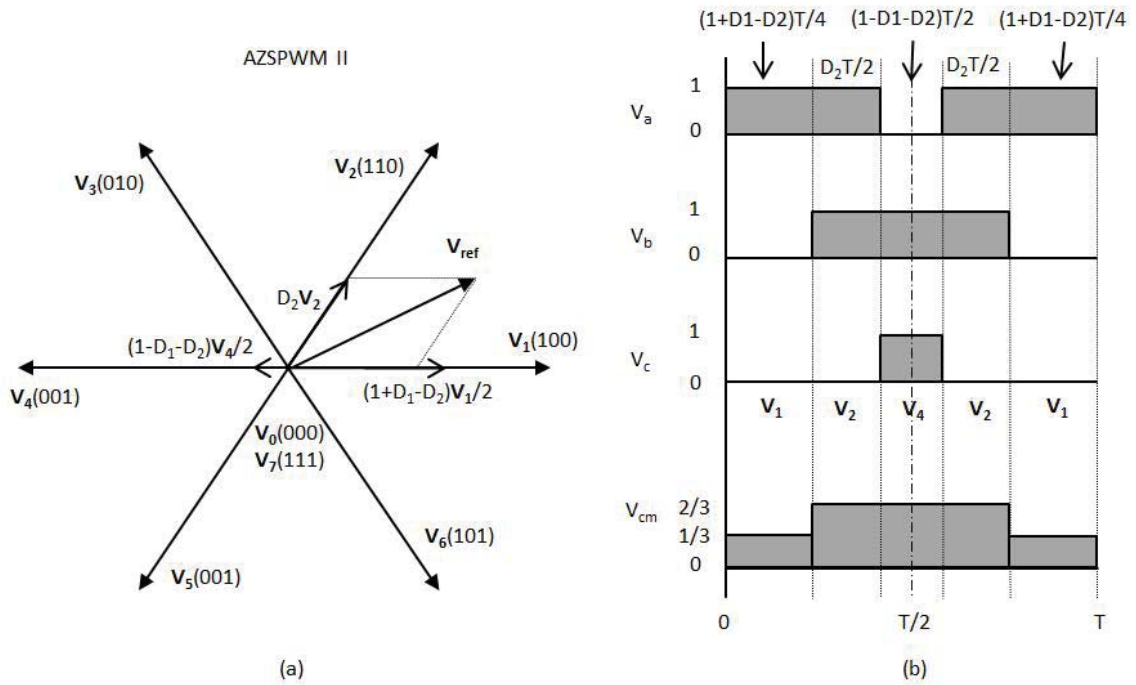


FIGURE 8.12 AZSPWM II: (a) generation of the reference voltage, (b) switching pattern.

The CM voltage of the Type II AZSPWM in each PWM cycle varies from $1/3$ to $2/3$, as shown in FIGURE 8.12(b). The CM voltage magnitude of AZSPWM II is only $1/3$ of the CM voltage generated by the SVPWM.

NSPWM

The Near-State-Pulse-Width-Modulation (NSPWM) scheme proposed in [50]–[52] generates the reference voltage, \mathbf{V}_{ref} , by using its two adjacent vectors and another active vector that is closest to the reference voltage. For example, as shown in FIGURE 8.13(a), \mathbf{V}_{ref} is generated by two adjacent vectors, \mathbf{V}_1 and \mathbf{V}_2 , and another vector \mathbf{V}_6 , if the angle between \mathbf{V}_{ref} and \mathbf{V}_1 is smaller than 30° . The sequence of the switching is \mathbf{V}_2 - \mathbf{V}_1 - \mathbf{V}_6 - \mathbf{V}_1 - \mathbf{V}_2 , as shown in FIGURE 8.13(b). The duty cycles for \mathbf{V}_1 , \mathbf{V}_2 and \mathbf{V}_6 are $2D_1+D_2-1$, $1-D_1$ and $1-D_1-D_2$, respectively. The average output voltage in this PWM cycle can be found by,

$$\begin{aligned}
 V_{o.avg} &= (2D_1 + D_2 - 1)\overline{V}_1 + (1 - D_1)\overline{V}_2 + (1 - D_1 - D_2)\overline{V}_6 \\
 &= (2D_1 + D_2 - 1)\overline{V}_1 + (1 - D_1)\overline{V}_2 + (1 - D_1 - D_2)\overline{V}_1 + (1 - D_1 - D_2)\overline{V}_5 \\
 &= (2D_1 + D_2 - 1)\overline{V}_1 + (1 - D_1)\overline{V}_2 + (1 - D_1 - D_2)\overline{V}_1 - (1 - D_1 - D_2)\overline{V}_2, \quad (8.6) \\
 &= D_1\overline{V}_1 + D_2\overline{V}_2 \\
 &= \overline{V}_{ref}
 \end{aligned}$$

as shown in FIGURE 8.13(a).

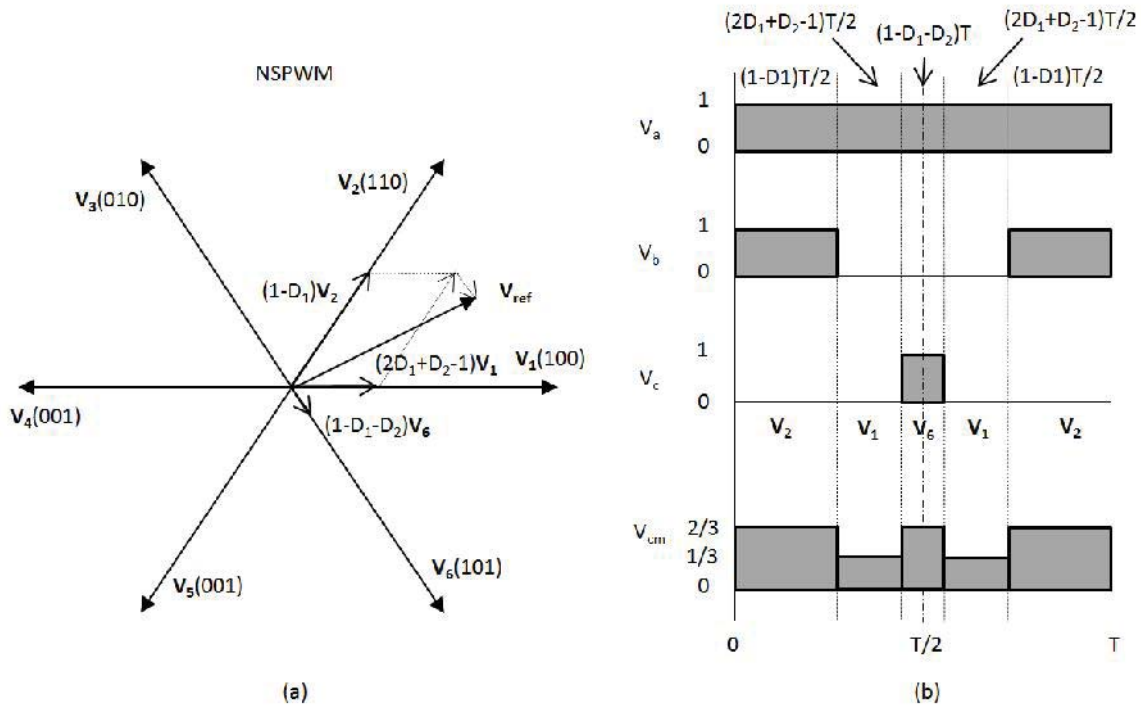


FIGURE 8.13 NSPWM: (a) generation of the reference voltage, (b) switching pattern.

The CM voltage of the NSPWM in each PWM cycle varies from $1/3$ to $2/3$, as shown in FIGURE 8.13(b). The CM voltage magnitude of NSPWM is only $1/3$ of the CM voltage generated by the SVPWM.

RSPWM

The Remote-State-Pulse-Width-Modulation (RSPWM) scheme proposed in [49], [53] generates the reference voltage, V_{ref} , by using three remote active vectors, either V_1 , V_3 , and V_5 , or V_2 , V_4 , and V_6 . FIGURE 8.14(a) shows an example of the RSPWM where, V_{ref} is generated by V_1 , V_3 , and V_5 . The sequence of the switching is V_3 - V_1 - V_5 - V_1 - V_3 , as shown in FIGURE 8.14(b). The duty cycles for V_1 , V_3 and V_5 are $1-D_2$, $1-D_1-D_2$ and $1-D_1-2D_2$, respectively. The sum of the three vectors can be found by,

$$\begin{aligned}
V_{o.avg} &= (1-D_2)\bar{V}_1 + (1-D_1-D_2)\bar{V}_3 + (1-D_1-2D_2)\bar{V}_5 \\
&= (1-D_2)\bar{V}_1 + (1-D_1-D_2)\bar{V}_2 + (1-D_1-D_2)\bar{V}_4 + (1-D_1-2D_2)\bar{V}_5 \\
&= (1-D_2)\bar{V}_1 + (1-D_1-D_2)\bar{V}_2 - (1-D_1-D_2)\bar{V}_1 - (1-D_1-2D_2)\bar{V}_2 \quad (8.7) \\
&= D_1\bar{V}_1 + D_2\bar{V}_2 \\
&= \bar{V}_{ref}
\end{aligned}$$

as shown in FIGURE 8.14(a).

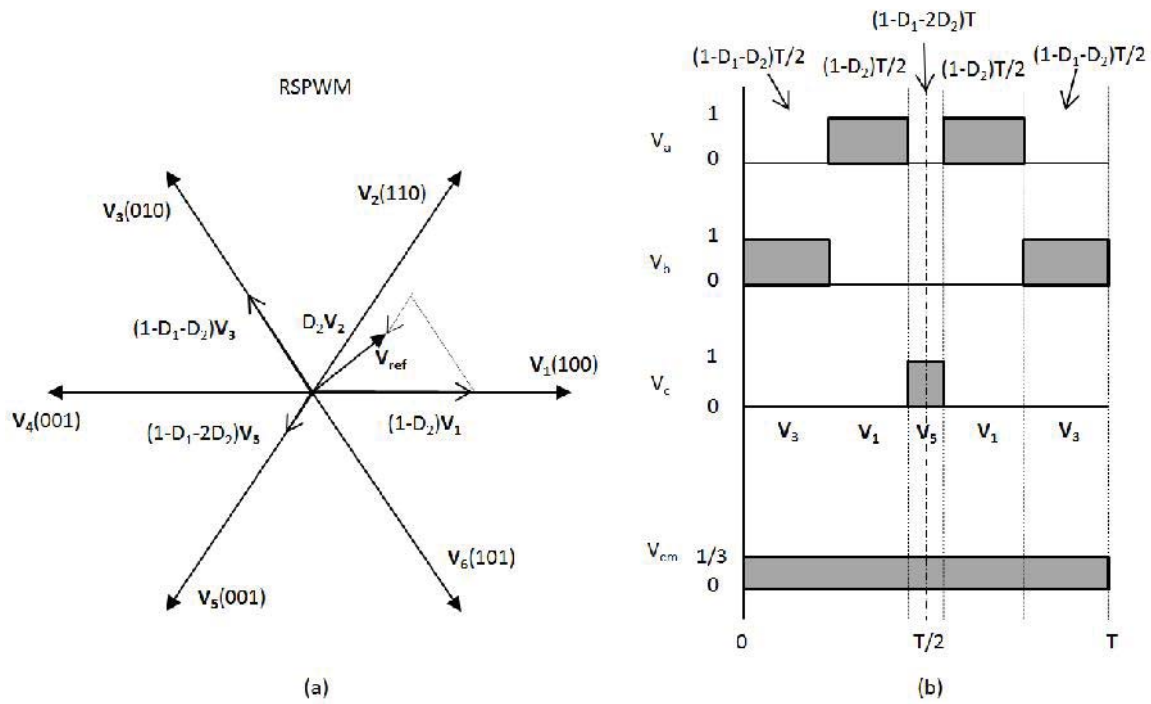


FIGURE 8.14 RSPWM: (a) generation of the reference voltage, (b) switching pattern.

The CM voltage of the RSPWM in each PWM cycle is constant in an ideal situation, as shown in FIGURE 8.14(b). As a result, the CM voltage of the RSPWM scheme can be eliminated theoretically.

8.2.2 Performance Analysis

CM voltage reduction

As analyzed above, the theoretical CM voltage source reduction of the AZSPWM, NSPWM and RSPWM schemes are listed in Table 8.1. For the three phase inverter, the CM voltage relative to the DC negative rail is the average of the numbers in the ‘0-1’ notation of the inverter output voltage times V_{dc} . For example, $\mathbf{V}_1(100)$ has a CM voltage relative to the DC negative of $V_{dc} / 3$ and $\mathbf{V}_7(111)$ has a CM voltage of V_{dc} . Both AZSPWM and NSPWM avoid using zero vectors, $\mathbf{V}_0(000)$ or $\mathbf{V}_7(111)$, when generating the reference voltage, thus, reduce the variation of the CM voltage in one PWM cycle from V_{dc} to $V_{dc}/3$, which is 10dB reduction. The RSPWM produces a constant CM voltage by using only odd-number or even-number active vectors to generate the reference voltage. Theoretically, it eliminates the CM noise source. Although these methods reduce the CM voltages of the power inverter, practically, they have several disadvantages compared to the traditional SVPWM scheme, such as limited voltage linearity region, increased harmonic distortion and simultaneous switching issues.

Table 8.1 CM voltage source reduction comparison.

	AZSPWM I	AZSPWM II	NSPWM	RSPWM
CM voltage source reduction	10dB	10dB	10dB	∞

Linearity region

Note that the duty cycles of all the voltage vectors used to generate the reference voltage always add up to one. As a result, the range of the reference voltage that can be

generated by the inverter output voltages is limited. Such range of the reference voltage is referred to as the voltage linearity region. Take the SVPWM for example, its voltage linearity region is the grey hexagon region shown in FIGURE 8.15. As discussed above, to output three sinusoidal waveforms in FIGURE 8.8, the reference voltage vector rotates around the hexagon center. As a result, the real useful region, or the fundamental linearity region, is the area inside the circle shown in FIGURE 8.15. The modulation index of the PWM driving scheme can be found by,

$$M_i = \frac{4}{3} \frac{|V_{ref}|}{|V_1|} . \quad (8.8)$$

As a result, the SVPWM can have a M_i up to 1.15 in its fundamental linearity region.

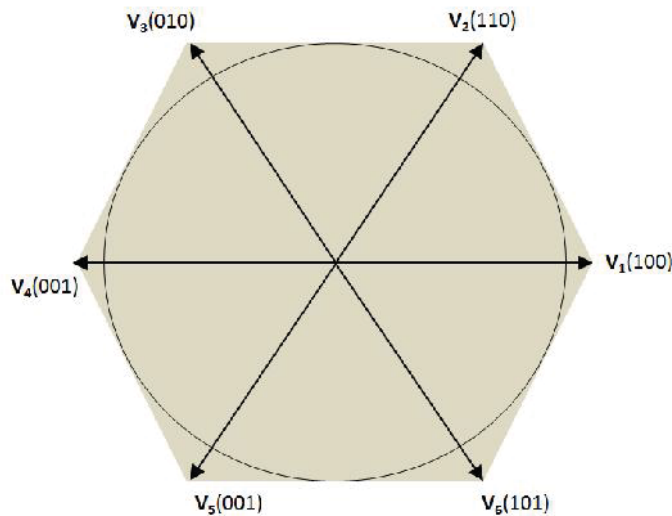


FIGURE 8.15 Voltage linearity region of SVPWM.

The linearity region of the AZSPWM scheme is the same as that of the SVPWM scheme. But the linearity regions of the NSPWM and RSPWM schemes are very limited compared to the SVPWM scheme, as shown in FIGURE 1.16 (grey area). The

fundamental linearity region of the NSPWM is contained in a ring area, which corresponds to a modulation index from 0.77 to 1.15. The fundamental linearity region of the RSPWM is the circle inside a triangular, which corresponds to a modulation index from 0 to 0.67. It can be improved by employing both V_1, V_3, V_5 , and V_2, V_4, V_6 , to generate the reference voltage. For example, when the angle of reference voltage is between -30° and 30° , V_1, V_3, V_5 are used. When its angle is between 30° and 90° , V_2, V_4, V_6 are used. The result is the increased linearity region and maximum modulation index of 0.77, as shown in the figure.

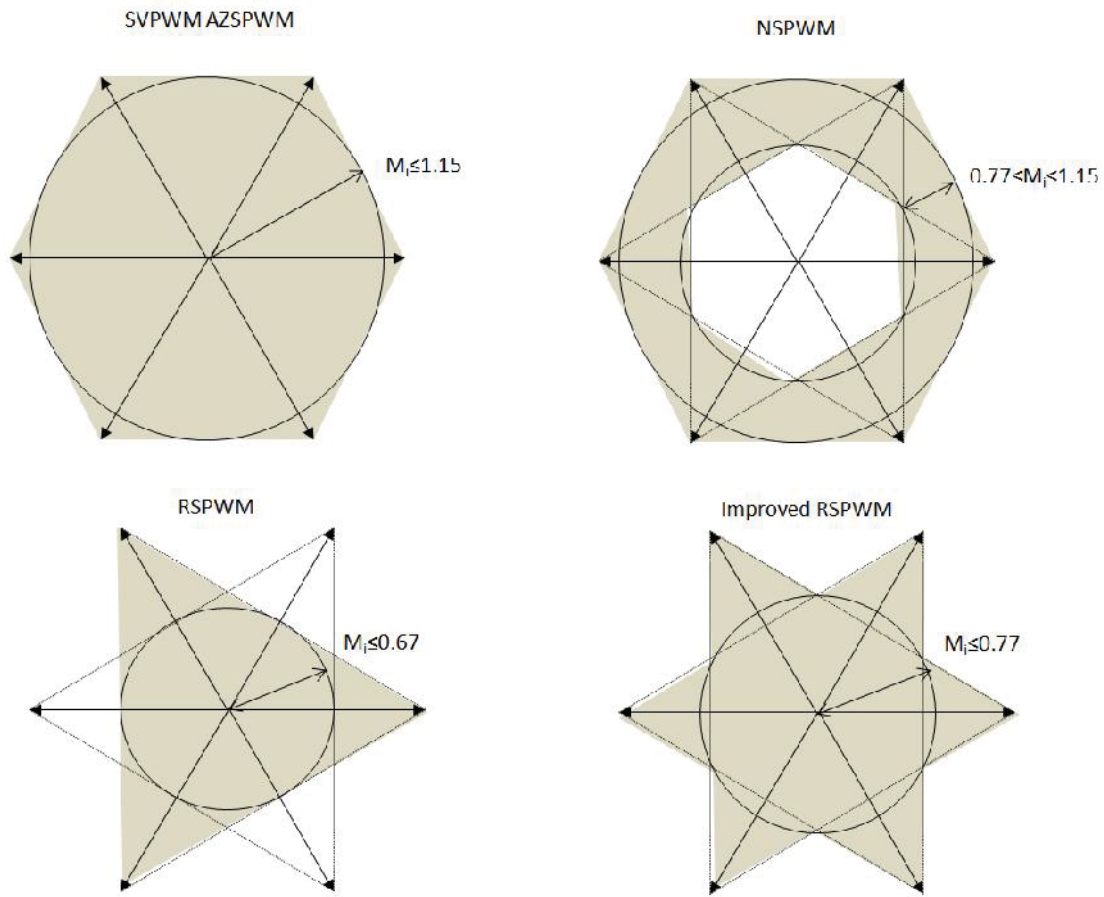


FIGURE 8.16 Voltage linearity regions of the CM-voltage-source-reduction schemes.

Output quality

Besides the linearity region, the actual inverter output quality is also a concern when selecting the PWM schemes. The sinusoidal waveforms in FIGURE 8.8 are never perfect in reality. The harmonics of the PWM carrier frequency distort the waveform and cause current and torque ripples at the motor it is driving. Criteria, such as the Total Harmonic Distortion (THD) factor, are used to evaluate such distortion. THD depends on the modulation index, but in general, the closer the active vectors used to generate the reference voltage are to each other, the smaller the THD is. The SVPWM uses two

adjacent active vectors to generate reference vector. Its THD is the smallest among the all. The NSPWM uses three adjacent vectors, so its THD is larger than SVPWM. The AZSPWM has two opposite active vector thus, high THD is expected. The RSPWM uses three remote active vectors. Its THD could be the highest among the all.

Simultaneous switching

Observe the switching patterns, SVPWM, AZSPWM I and NSPWM switch one inverter leg at a time, while AZSPWM II and RSPWM involve switching two inverter legs at the same time. In practice, simultaneous switching doesn't happen due to the difference in the power components and the dead time. Also instantaneous line-to-line voltage reversal caused by the simultaneous switching could result in significant over voltage at the motor terminals. [54]

8.2.3 Summary of Noise Source Reduction Schemes

Table 8.2 listed the PWM schemes that reduce the CM noise source in the three-phase power inverter for comparison. The traditional SVPWM has the largest CM output noise source. However, it performs very well by other criteria, which is why it is favored and employed in many of the today's three-phase motor drives. The CM-voltage-reducing PWM schemes are favored from the EMC standpoint of view, especially for those without the simultaneous switching problem.

Table 8.2 Noise source reduction schemes comparison.

	CM voltage reduction	Linearity Region	Output Quality	Simultaneous Switching
SVPWM	0 dB	$M_i \leq 1.15$	Good	No
AZSPWM I	10 dB	$M_i \leq 1.15$	Poor	No
AZSPWM II	10 dB	$M_i \leq 1.15$	Poor	Yes
NSPWM	10 dB	$0.77 \leq M_i \leq 1.15$	Moderate	No
RSPWM	∞	$M_i \leq 0.77$	Poor	Yes

8.3 Other Noise Source Reduction method

This chapter reviewed the methods for CM noise source reduction. Although the AZSPWM, NSPWM and RSPWM reduce the CM noise compared to the standard SVPWM method, they have many disadvantages, such as smaller linearity region, poor output quality and simultaneous switching issues, which are not favored in practical applications.

Compared to the three-level inverter example, multilevel inverters have advantages for applying the CM-source-reduction method because they offer more switching combinations. Better performance of such applications were reported in [55], [56].

Other methods such as the Random PWM (RPWM) proposed in [57]–[59] can also improve the EMC performance of the motor drive. It uses a non-constant PWM carrier frequency to spread the noise energy in a wide frequency range so that the peak noise in the switching frequency harmonics can be reduced.

PART II

9. INTRODUCTION TO MREMC

The Maximum Radiated Electromagnetic Emissions Calculator (MREMC) is a software tool that allows the user to calculate the maximum possible radiated emissions that could occur due to specific source geometries on a printed circuit board. The *I/O coupling EMI* algorithm determines the maximum possible radiated emissions that could occur due to coupling from a source signal on one trace to another (I/O) trace that could carry the coupled signal off the board. The *Common-mode EMI* algorithm determines the maximum possible radiated emissions that could occur when a signal on a microstrip trace induces CM currents on the cables attached to the circuit board. The *Power Bus EMI* algorithm determines the maximum possible radiated emissions that could occur from a rectangular power bus structure. The *Differential-Mode EMI* algorithm determines the maximum possible radiated emissions that could occur due to direct radiation from the differential currents flowing on circuit board traces. The methods used, calculations made, and implementation details are described.

10. IO COUPLING EMI ALGORITHM

10.1 Introduction

High frequency signals on one circuit board trace can couple to input/output (I/O) traces that carry the coupled energy away from the board. The common-mode currents induced on cables attached to I/O nets can result in significant radiated emissions. The I/O coupling EMI calculator was developed to calculate the maximum possible radiated emissions from structures like this. The calculator utilizes formulas for crosstalk between PCB traces described by Gupta [60] and expressions for the maximum radiated emissions from PCB-cable structures developed by Deng [61]. This report is an extension of the method described by Su [62] and is intended to provide details of the implementation sufficient to allow others to develop their own version of this calculator.

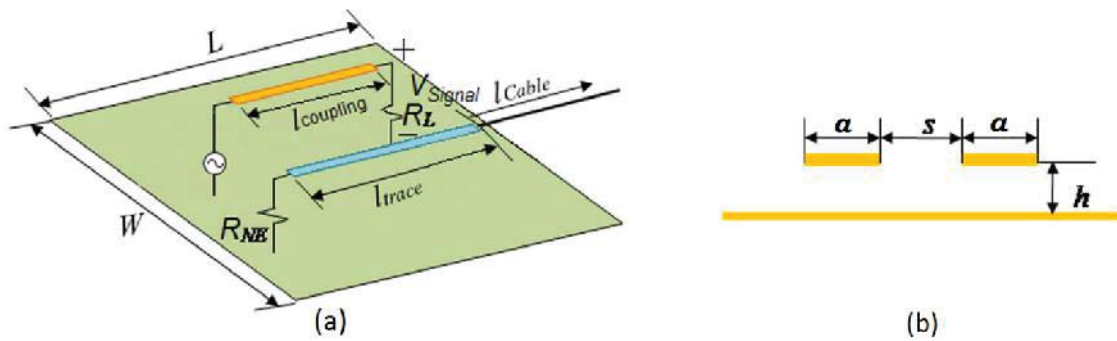


FIGURE 10.1 I/O Coupling model: (a) top view, (b) section view.

Two parallel sections of microstrip circuit board traces are illustrated in FIGURE 10.1. The cross-sectional view in FIGURE 10.1(b) shows that both traces have a width, a , a height, h , and edge-to-edge separation, s . The board length, L , board width, W , relative dielectric constant, ϵ_r , coupling length, $l_{coupling}$, and I/O trace length, l_{trace} , are the other geometrical parameters required for this calculation. V_{Signal} and R_L represent the signal

source voltage and the load resistance of the signal trace respectively. R_{NE} is the near end resistance of the I/O trace. The I/O cable length is unspecified, but board is assumed to be 1 meter over a ground plane, as it would be in most radiated emissions tests[61].

The calculator calculates the maximum radiated electric field at a distance of 3 meters from the board and plots the results in $dB\mu V/m$ from 0 to 100 MHz as shown in FIGURE 10.2.

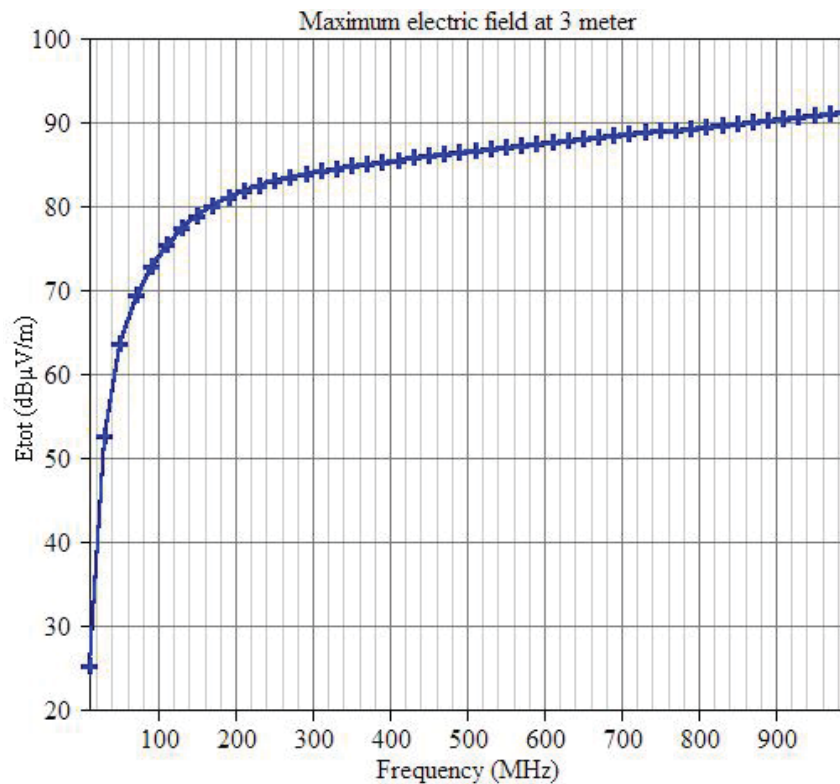


FIGURE 10.2 MREMC plot example.

10.2 Description of Algorithm

The algorithm used by the calculator can be broken into two main parts. The first is to determine the equivalent common-mode (CM) source based on the trace geometry. The second is to determine the maximum radiated emissions based on the CM source and

cable-board geometry. To determine the CM source, the total voltage coupled to the victim circuit is determined by the *coupling* algorithm and the *Thevenin equivalent* algorithm. After the CM source is obtained, the maximum radiated emissions are then estimated by the *estimation* algorithm.

10.2.1 The Coupling Algorithm

I/O coupling model

FIGURE 10.3(a) shows the coupling model, which can be represented more simply as shown in FIGURE 10.3(b). V_S , Z_L and Z_{NE} are the same as V_S , R_L and R_{NE} indicated in FIGURE 10.1. Note that in this calculator, Z_L and Z_{NE} only support resistive input. Z_{FE} is the far-end load of the I/O trace, representing the input impedance of the antenna formed by the I/O cable being driven against the wide PCB ground plane. L_m represents the mutual inductance between the two trace-ground loops. C_m represents the mutual capacitance between the two traces. Inductive coupling occurs when changing current in the signal trace induces a voltage on the I/O trace through L_m . Similarly, the capacitive coupling occurs when a changing voltage on the signal trace induces a current on the I/O trace through C_m .

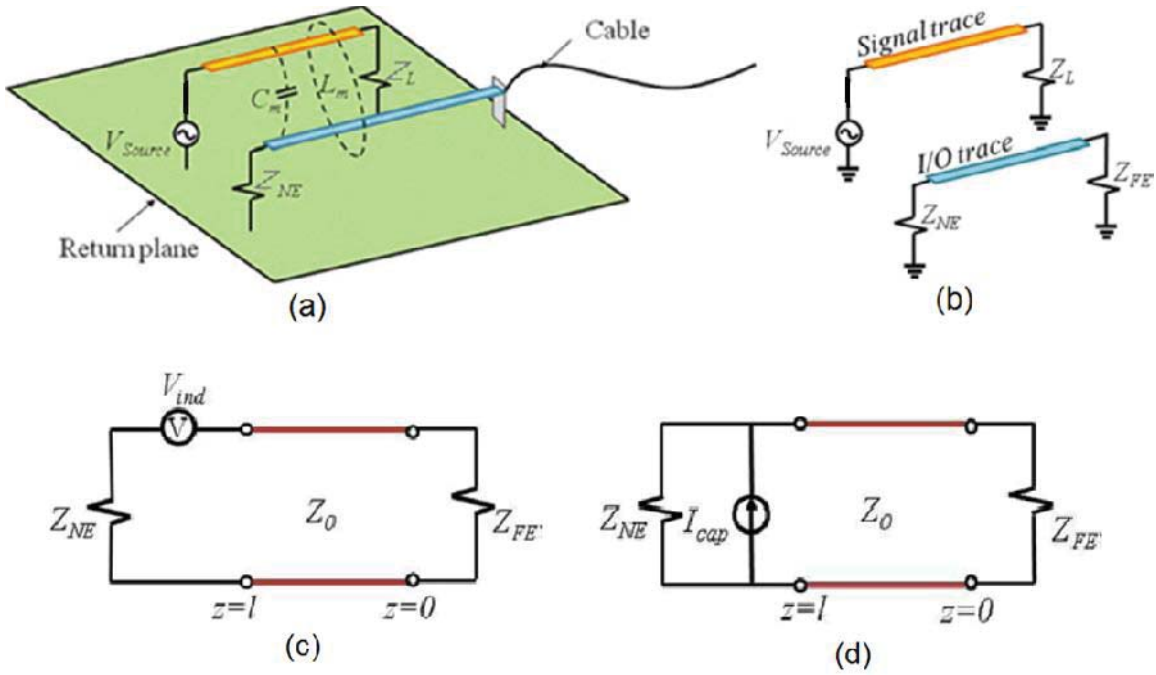


FIGURE 10.3 Coupling algorithm: (a) coupling model, (b) simplified model, (c) inductive coupling schematic, (d) capacitive coupling schematic.

Inductive Coupling

FIGURE 10.3(c) is the lumped-element circuit model for the inductive coupling. The I/O trace and return plane are represented as a transmission line of length l . V_{ind} represents the induced electromotive force due to inductive coupling, which is given by

$$V_{ind} = -j\omega L_m I_{source} \quad (10.1)$$

where I_{source} is the current on the signal which can be obtained by V_{Signal} / Z_L . Note that the self inductance of the signal trace loop is ignored since at a frequency where the loop inductance matters, the trace usually has a matched load. In the algorithm, only the magnitude of the V_{ind} is calculated,

$$|V_{ind}| = 2\pi f L_m I_{source} \quad (10.2)$$

Capacitive Coupling

FIGURE 10.3(d) is the lumped-element circuit model for the capacitive coupling. An independent current source, I_{cap} , represents the induced current due to capacitive coupling, which is given by

$$I_{cap} = j\omega C_m V_{\text{signal}} \approx j\omega C_m Z_L I_{\text{source}}. \quad (10.3)$$

In the algorithm, only the magnitude of the I_{cap} is calculated. Then magnitude of V_{cap} is obtained by

$$|V_{cap}| = |I_{cap}| \cdot Z_{NE} = 2\pi f C_m Z_L Z_{NE} I_{\text{source}}. \quad (10.4)$$

Total Coupling

Assuming the lines are weakly coupled, the maximum possible coupling is a linear combination of contributions due to the inductive and capacitive coupling [63]. The maximum voltage induced in the victim circuit is the sum of the two coupled voltages,

$$|V_{\text{total}}| = |V_{\text{ind}} + V_{\text{cap}}| = |j\omega [-L_m + C_m Z_L Z_{NE}] I_{\text{source}}| = \left| |V_{\text{ind}}| + |V_{\text{cap}}| \right|. \quad (10.5)$$

Mutual Inductance and Capacitance

The mutual inductance L_m and mutual capacitance C_m are required to calculate the induced voltages. The algorithm calculates L_m and C_m by [60]

$$C_m = \frac{1}{2} [C_o(\epsilon_r) - C_e(\epsilon_r)] \cdot I_{\text{coupling}} \quad (10.6)$$

$$L_m = \frac{\mu_0 \epsilon_0}{2} \left[\frac{1}{C_e(\epsilon_r = 1)} - \frac{1}{C_o(\epsilon_r = 1)} \right] \cdot I_{\text{coupling}} \quad (10.7)$$

where C_o and C_e are even and odd mode capacitances per unit length respectively. $l_{coupling}$ is the coupling length for user input. (10.6) and (10.7) only apply to symmetrical traces (traces with same width) [60]. For coupled microstrip lines, the components of the line capacitance are illustrated in FIGURE 10.4. The algorithms to calculate C_o and C_e are included in the subroutine *calcCeCo(epsr)*.

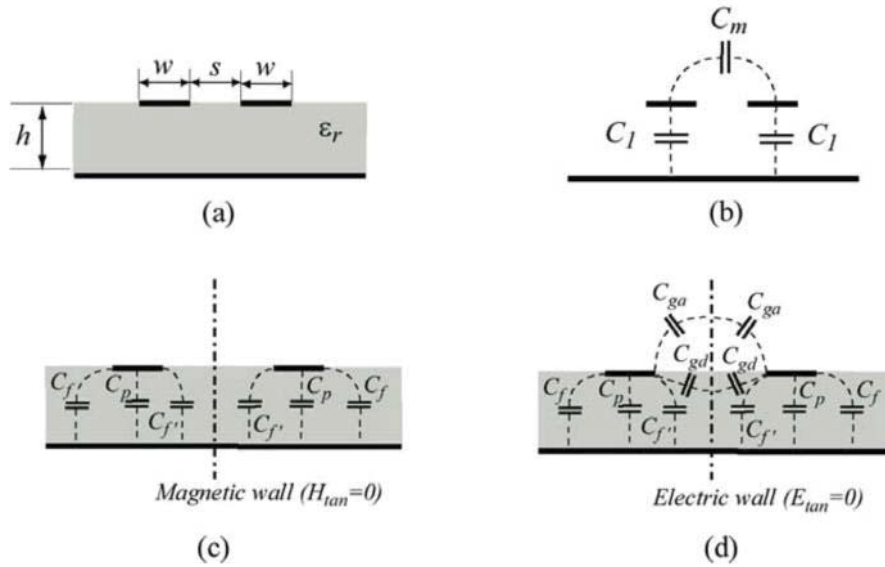


FIGURE 10.4 Configuration of coupled microstrip line (a) general equivalent circuit (b) and breakup of even mode (c) and odd mode (d) capacitance

For the even mode, the capacitance C_e is given as [60],

$$C_e(\epsilon_r) = C_p + C_f + C_{f'} \quad (10.8)$$

where,

$$C_p = \frac{\epsilon_0 \epsilon_r w}{h} \quad (10.9)$$

$$C_f = \frac{1}{2} \left[\frac{\sqrt{\epsilon_r}}{cZ_0} - C_p \right] \quad (10.10)$$

$$C_{f'} = \frac{C_f \cdot \sqrt[4]{\epsilon_r / \epsilon_{re}}}{1 + A(h/s) \tanh(10s/h)} \quad (10.11)$$

where,

$$A = \exp[-0.1 \exp(2.33 - 1.5w/h)] \quad (10.12)$$

$$Z_0 = \begin{cases} \frac{120\pi}{2\pi\sqrt{\epsilon_{re}}} \ln(8h/w + 0.25w/h) & w/h \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_{re}}} [w/h + 1.393 + 0.667 \ln(w/h + 1.444)]^{-1} & w/h > 1 \end{cases} \quad (10.13)$$

where ϵ_{re} is effective relative permittivity, which can be found by [64],

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/a}}. \quad (10.14)$$

The values are found to be accurate to within 3 percent, compared with the values obtained from [6], over the following range of parameters [60],

$$0.1 \leq w/h \leq 10 \quad 0.1 \leq s/h \leq 5 \quad 1 \leq \epsilon_r \leq 18$$

For the odd mode, the capacitance C_o is found by [60],

$$C_e(\epsilon_r) = C_p + C_f + C_{f'} + C_{ga} + C_{gd} = 0.5C_{os} + C_{cps} \quad (10.15)$$

where,

$$C_{cps} = \epsilon_0 \frac{K(k')}{K(k)} \quad (10.16)$$

$$C_{os} = 4\epsilon_0\epsilon_r \frac{K(k_0)}{K(k_0')} \quad (10.17)$$

where,

$$k = \frac{s}{s+2w} \quad (10.18)$$

$$k' = \sqrt{1-k^2} \quad (10.19)$$

$$k_0 = \tanh\left(\frac{\pi w}{4h}\right) \coth\left[\frac{\pi}{4}\left(\frac{w+s}{h}\right)\right] \quad (10.20)$$

$$k_0' = \sqrt{1-k_0^2}. \quad (10.21)$$

The function $K(k)$ and $K(k')$ are the complete elliptic function and its complement and their ratio is given by

$$\frac{K(k')}{K(k)} = \begin{cases} \frac{1}{\pi} \ln\left(2 \frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right) & 0 \leq k \leq \frac{1}{\sqrt{2}} \\ \pi / \ln\left(2 \frac{1+\sqrt{k}}{1-\sqrt{k}}\right) & \frac{1}{\sqrt{2}} \leq k \leq 1 \end{cases}. \quad (10.22)$$

Same applies to $K(k_0) / K(k_0')$

The capacitances obtained by using the above equations are accurate within 3 percent, compared with values obtained from [65], over the range of parameters [60],

$$0.1 \leq w/h \leq 10 \quad 0.1 \leq s/h \leq 4 \quad 2 \leq \epsilon_r \leq 18$$

10.2.2 Thevenin Equivalent Algorithm

A Thevenin equivalent source model was derived to account for all of the coupling without requiring the input impedance of the attached cable to be known. The I/O trace may or may not be electrically short and is modeled as a transmission line as indicated in FIGURE 10.5(a). The open-circuit voltage at the far end (i.e., the connector) V_{eq} , and the equivalent impedance looking back toward the near end from the connector Z_{eq} , can be readily calculated from transmission line theory yielding the Thevenin equivalent circuit in FIGURE 10.5(b).

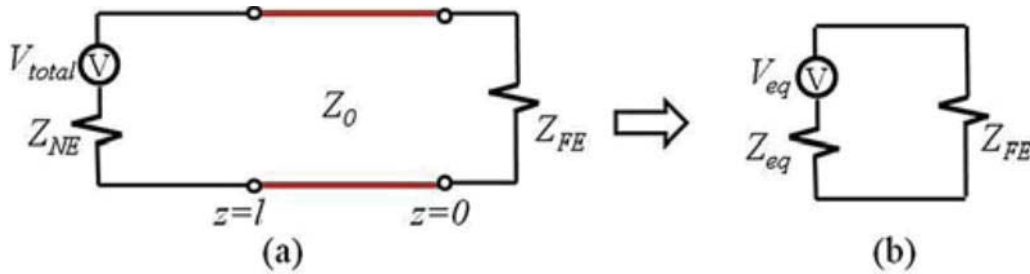


FIGURE 10.5 Thevenin equivalent model

V_{eq} and Z_{eq} can be found by [62]

$$V_{eq} = 2 \left(\frac{Z_0}{Z_0 + jZ_{NE} \tan \beta l} \right) \left(\frac{V_{total}}{e^{j\beta l} + e^{-j\beta l}} \right) \quad (10.23)$$

$$Z_{eq} = Z_0 \left(\frac{Z_{NE} + jZ_0 \tan \beta l}{Z_0 + jZ_{NE} \tan \beta l} \right) \quad (10.24)$$

where Z_0 is the characteristic impedance of the transmission line, which is given in

(10.13) and βl is the wavenumber, which is given by

$$\beta l = \frac{2\pi f l_{trace} \sqrt{\epsilon_r}}{c_0} . \quad (10.25)$$

In the algorithm, the magnitude of V_{eq} , the real part of Z_{eq} and the imaginary part of Z_{eq} are calculated separately by

$$|V_{eq}| = \left(\frac{Z_0}{\sqrt{Z_0^2 + (Z_{NE} \tan \beta l)^2}} \right) \left(\frac{V_{total}}{|\cos \beta l|} \right) \quad (10.26)$$

$$Z_{eq,real} = \frac{Z_0^2 Z_{NE} + Z_0^2 Z_{NE} (\tan \beta l)^2}{Z_0^2 + (Z_{NE} \tan \beta l)^2} \quad (10.27)$$

$$Z_{eq,imag} = \frac{Z_0^3 \tan \beta l - Z_0 Z_{NE}^2 \tan \beta l}{Z_0^2 + (Z_{NE} \tan \beta l)^2} \quad (10.28)$$

FIGURE 10.3(a) can then be replaced by the model in FIGURE 10.6 with the Thevenin equivalent source voltage and impedance. The new model is ready for use in the radiated emission estimation.

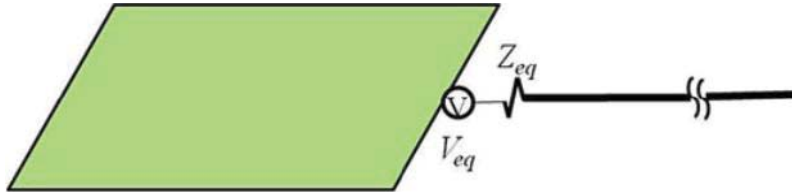


FIGURE 10.6 I/O coupling model with CM source and impedance

10.2.3 Maximum Radiated Emission Estimation Algorithm

Board-source-cable geometry

A simplified geometry representing a typical EMC test environment is shown in FIGURE 10.7, where the PCB board is 1m above the ground. Study in [61] suggests that the peak emissions from such geometry are relatively independent of the connection point to the board and relatively insensitive to the total cable length or orientation. The

parameters that matter are the vertical distance traversed by the cable and the maximum current. Also the maximum radiated electric field for this geometry can be estimated by comparing the emissions from this structure to the emissions from a thin-wire monopole above an infinite ground plane. In [61], a closed-form formula was developed to estimate the maximum radiated emissions from the antenna model in FIGURE 10.7. This formula was enhanced in [66] to be more accurate over the larger frequency ranges.

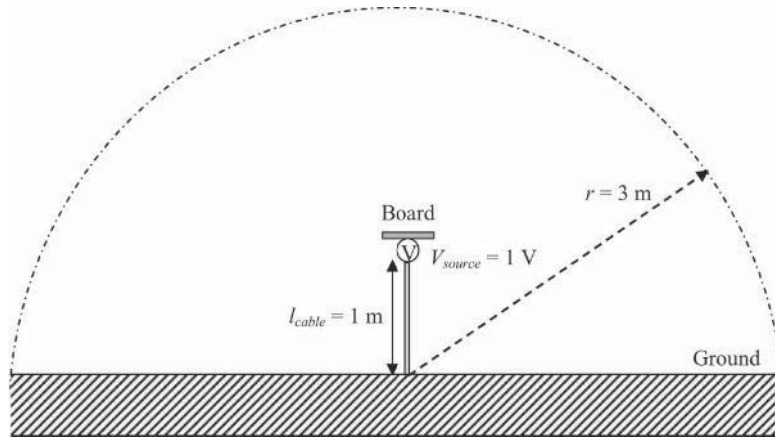


FIGURE 10.7 Board-source-cable geometry

Maximum Radiated Emission Estimation

The maximum electric field at 3m as shown in FIGURE 10.6 is calculated by [61],

$$|E|_{\max} = 20 \times I_{\text{peak}} \times f(\theta, k, l_{\text{cable}}) \quad (10.29)$$

where $f(\theta, k, l_{\text{cable}})$ can be obtained by [66],

$$f(\theta, k, l_{\text{cable}}) = \begin{cases} \frac{2}{\sin(\sqrt{2})} & f \leq \frac{c_0}{2l_{\text{cable}}} \\ \frac{2}{\sin\left(\sqrt{\frac{c_0}{fl_{\text{cable}}}}\right)} & f > \frac{c_0}{2l_{\text{cable}}} \end{cases} \quad (10.30)$$

where l_{cable} is the length of the attached cable, which is set to 1m in the calculator. f is the frequency, and c_0 is the propagation velocity in free space. I_{peak} is the highest current that actually exists on the cable and is given by

$$I_{peak} = \frac{V_{eq}}{\left| Z_{eq} + \frac{R_{min}}{board_factor \times cable_factor} \right|} \quad (10.31)$$

where R_{min} is the input resistance (about 37 Ω) of a resonant quarter-wave monopole. Two factors account for the effect that the finite cable length and the small board size have on this minimum resistance, which are given by,

$$board_factor = \begin{cases} \sin(2\pi l_{board}/\lambda) & \text{when } l_{board} \leq \frac{\lambda}{4} \\ 1.0 & \text{otherwise} \end{cases} \quad (10.32)$$

$$cable_factor = \begin{cases} \sin(2\pi l_{cable}/\lambda) & \text{when } l_{cable} \leq \frac{\lambda}{4} \\ 1.0 & \text{otherwise} \end{cases} \quad (10.33)$$

where l_{board} is the effective length of a rectangular board. It can be approximated as,

$$l_{board} = \frac{1 + 2L/W}{2L/W} \times \sqrt{L^2 + W^2} \quad (10.34)$$

where L and W denote the board length and width, respectively as shown in FIGURE 10.1. (10.31) is then calculated as,

$$I_{peak} = \frac{V_{eq}}{\sqrt{\left(Z_{eq,real} + \frac{37}{board_factor \times cable_factor} \right)^2 + Z_{eq,imag}^2}} \quad (10.35)$$

10.2.4 Assumptions Made in this Derivation

1. Signal trace and I/O trace are weakly coupled.

The induced currents and voltages in the victim circuit will induce currents and voltages back into the generator circuit. By assuming weak coupling, the currents and voltages coupled back into the generator circuit are ignored. [63]

2. Portion of the signal trace coupling to the I/O line is electrically short with a self-capacitance and self-inductance that are negligible compared to the source and load impedances. This is frequently the case, but similar equations that do not depend on the value of Z_{FE} could be readily derived for longer signal traces. [62]
3. The I/O trace can be model as a lossless transmission line, which is a reasonable approximation.
4. The attached cable has negligible diameter, which is a good approximation when the cable diameter is considerably smaller than the wavelength.

10.2.5 Limitations due to Implementation

1. These calculations are designed for symmetric microstrip lines.
2. The coupling algorithm provides reasonably accurate values in the following range, $0.1 \leq w/h \leq 10$ $0.1 \leq s/h \leq 4$ $2 \leq \epsilon_r \leq 18$
3. The Estimation algorithm currently calculates emissions for a typical EMC test environment with the EUT set 1 meter above the ground and the measuring antenna located at 3 meters away.

10.3 Conclusion

This calculator determines the maximum possible radiated emissions due to coupling from a signal trace to an I/O trace on a circuit board. It is limited to symmetric microstrip lines and assumes that the length of the coupled section is small relative to a wavelength at the highest frequency of the analysis. Applied to longer coupled sections, the calculator will overestimate the possible radiated emissions.

11. COMMON-MODE EMI ALGORITHM

11.1 Introduction

A very common source of unwanted radiated emissions from electronic devices is the common-mode current induced on attached cables. Energy from signal currents can be coupled to attached cables through electric or magnetic fields. High frequency signals on a circuit board trace can couple energy to the cables attached to the ground plane directly through their electric field. They can also couple energy to the cables through the magnetic field wrapping around the ground plane generated by the signal currents returning through the finite-impedance ground plane. Both mechanisms can induce CM currents on the cables resulting in radiated emissions. The first source mechanism is referred to as *electric-field coupling*, by which, the magnitude of the induced CM current is proportional to the signal voltage, but independent of the signal current. The second source mechanism is referred to as *magnetic-field coupling*, by which the magnitude of the induced CM current is proportional to the signal current, but independent of the signal voltage. The CM EMI calculator was developed to calculate the maximum possible radiated emissions from structures like this due to the two coupling mechanisms. The calculator utilizes models for equivalent noise source calculations described by Su [7] and expressions for the maximum radiated emissions from PCB-cable structures developed by Deng [61] and Su [66]. This report is an extension of the method described above and is intended to provide details of the implementation sufficient to allow others to develop their own version of this calculator.

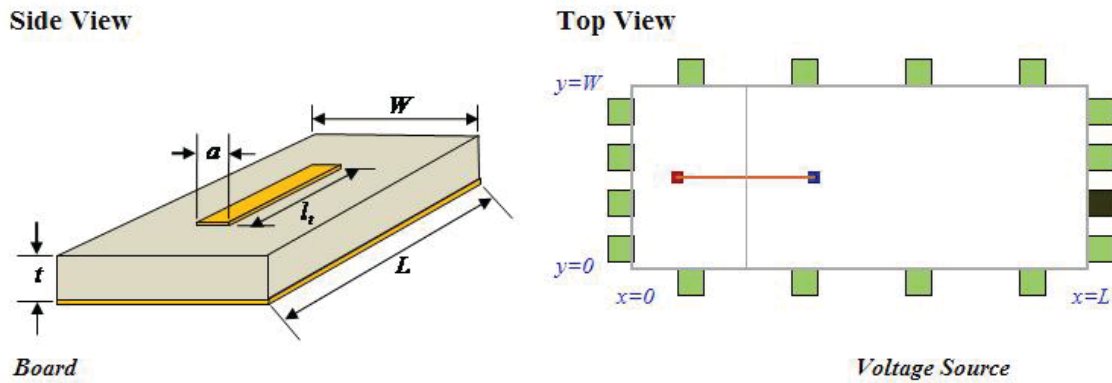


FIGURE 11.1 CM EMI model: (a) side view, (b) top view.

A simple circuit board with a microstrip trace and a ground plane is illustrated in FIGURE 11.1. The circuit board has a length, L , a width, W , and a dielectric layer thickness, t . The signal trace has a width, a , and a length, l_t . The positions of the trace and the attached cables are other geometrical parameters required for this calculation. The coordinates of the two end points of the trace are entered into the calculator manually. Cable attachment points (connector positions) are to be chosen from the 16 position options around the perimeter of the circuit board indicated by the green squares in FIGURE 11.1(b). R_L and C_L represent the load resistance and capacitance, respectively. The user can choose one of them depending on whether the signal terminates in a CMOS component or a matched load.

The calculator calculates the maximum radiated electric field due to both coupling mechanisms at a distance of 3 meters from the board. It plots the results in $dB\mu V / m$ from 0 to 500 MHz if the “*Digital Signal*” source type is chosen; or from f_0 to f_1 if the “*Swept Frequency*” source type is chosen. A representative output plot is shown in FIGURE 11.2. f_0 and f_1 are the lower and the upper limits for the frequency sweep respectively.

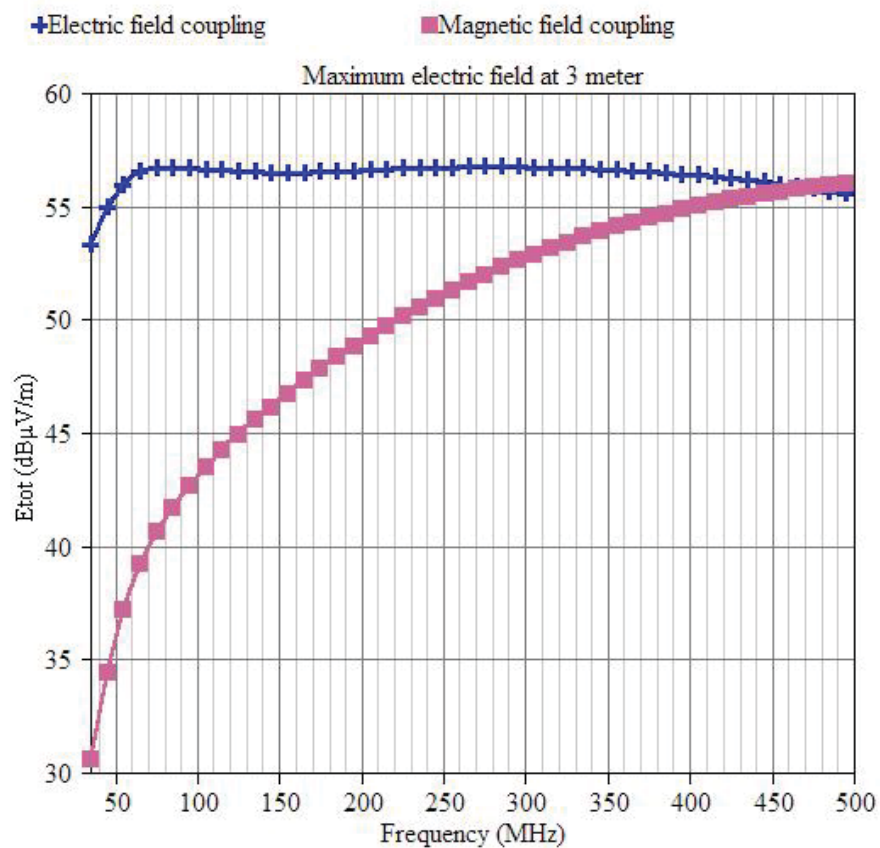


FIGURE 11.2 MREMC plot example.

11.2 Description of Algorithm

The algorithm used by the calculator can be broken into two main parts. The first part determines the equivalent CM source based on the source geometry using the *CM Source* algorithm. The second part determines the maximum radiated emissions based on the CM source and the cable-board geometry using the *Radiated Emission Estimation* algorithm. Both parts can be further broken into two subparts: the *Electrical Coupling* algorithm and the *Magnetic Coupling* algorithm.

11.2.1 The CM Source Algorithm

In [7], Su described a method called the Imbalance Difference Method to model the differential-mode (DM) to CM conversion of a signal routed on a trace over a solid ground plane with cables attached to both sides of the ground plane, as shown in FIGURE 11.3(a). The equivalent model is shown in FIGURE 11.3(b), where the trace and the loads are replaced by two CM voltages on the ground plane. h_1 , h_2 , h_3 are the imbalance factors, which can be defined for any transmission line geometry and are used to calculate the magnitude of the CM voltages. They can be calculated using the equation,

$$h = \frac{C_{trace}}{C_{trace} + C_{board}} \quad (11.1)$$

where, C_{trace} and C_{board} are the stray capacitances per unit length of the signal trace and ground plane. Note that the imbalance factor h is always between 0 and 0.5.

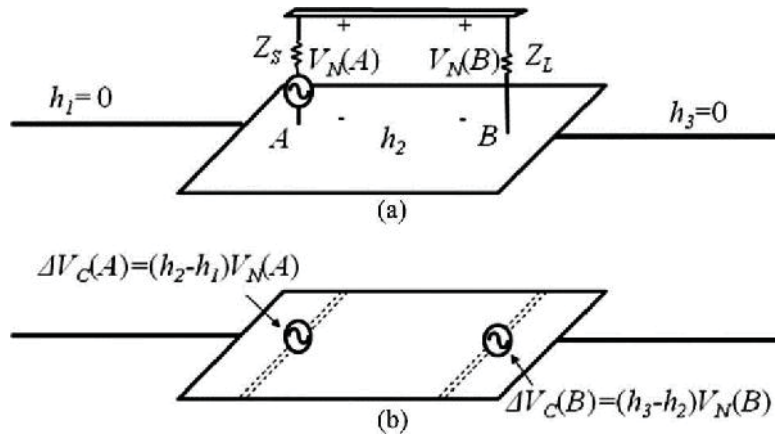


FIGURE 11.3 Imbalance difference model (a) Trace-and-board configuration. (b) Equivalent model.

In FIGURE 11.3, there is a change in the imbalance factor h at both ends of the microstrip. As a result, voltages are generated that drive common-mode currents in the ground plane. These voltages have amplitudes

$$\Delta V_C(A) = (h_2 - h_1)V_N(A) \quad (11.2)$$

$$\Delta V_C(B) = (h_3 - h_2)V_N(B) . \quad (11.3)$$

Since h_1 and h_3 are both zero (there is no trace, so $C_{\text{trace}}=0$), (11.2) and (11.3) can be rewritten as,

$$\Delta V_C(A) = h_2 V_N(A) \quad (11.4)$$

$$\Delta V_C(B) = -h_2 V_N(B) . \quad (11.5)$$

If $V_N(B)$ is the signal on the load end of the circuit, $V_N(A)$ can be expressed in terms of $V_N(B)$ as,

$$V_N(A) = V_N(B) + j2\pi f(L_{\text{trace}} + L_{\text{return}})I_{DM} \quad (11.6)$$

where L_{trace} and L_{return} are the partial inductance of the trace and the board respectively.

Combining (11.4) and (11.6), we have,

$$\Delta V_C(A) = h_2 V_N(B) + j2\pi f(L_{\text{trace}} + L_{\text{return}})I_{DM} . \quad (11.7)$$

The two CM source amplitudes obtained from (11.5) and (11.7) drive the common-mode currents on the structure. Their magnitudes and phases depend on $V_N(B)$ and I_{DM} given the imbalance factor h_2 is a constant. As a result, we can further decompose the

radiated emissions source into two parts. One part depends on the signal voltage, $V_N(B)$, and is the electric-field coupled component. The other part depends on the signal current, I_{DM} , is the magnetic-field coupled component. Separating the two coupling mechanisms allows users to better understand the cause of the radiated emissions from the circuit board.

Electric-Field Coupling

The source components representing the electric-field coupling can be derived by making the circuit in FIGURE 11.3(a) an open circuit as shown in FIGURE 11.4(a), so that the DM current, I_{DM} , becomes zero. This configuration results when the two CM voltages have the same magnitude and are 180° out of phase. In this case, the sources drive the attached cables against the board and the induced CM currents flow in opposite directions on cables attached to each side of the board, as shown in FIGURE 11.4(b). The magnitudes of the electric-field component of the CM voltages can be calculated by,

$$V_{CM} = hV_{DM} \quad (11.8)$$

where h and V_{DM} are the same as h_2 and $V_N(B)$ in Equation (11.7), (i.e. the imbalance factor of the trace-board geometry and the signal voltage at the load, respectively).

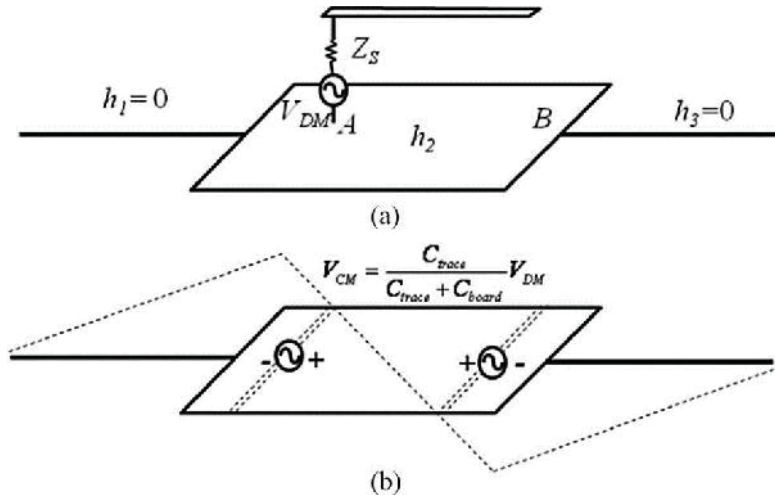


FIGURE 11.4 Imbalance difference model for the open circuit structure.

Magnetic-Field Coupling

The sources representing the magnetic-field coupling can be derived by making the circuit in FIGURE 11.3(a) a short circuit as shown in FIGURE 11.5(a). This makes the DM signal voltage, V_{DM} , zero. The load-end CM voltage is also zero, as shown in FIGURE 11.5(b), leaving only the source end CM voltage with an amplitude that is given by,

$$V_{CM} = h \cdot 2\pi f (L_{trace} + L_{return}) I_{DM} . \quad (11.9)$$

Since h can also be expressed as,

$$h = \frac{L_{return}}{L_{return} + L_{trace}} . \quad (11.10)$$

Combining (11.9) and (11.10), we have,

$$V_{CM} = 2\pi f L_{return} I_{DM} . \quad (11.11)$$

I_{DM} can be found by,

$$I_{DM} = V_{DM} / Z_L \quad (11.12)$$

where Z_L is the load impedance. Note that the calculator doesn't allow Z_L to be zero, because this would cause the signal voltage to also be zero.

The CM voltage obtained from (11.11) drives one cable relative to another if cables are attached to opposite sides of the board. It drives the cables relative to the board if all cables are attached to the same side of the board. The induced CM currents flow in the same directions on the cables attached to opposite sides of the board, as shown in FIGURE 11.5(b).

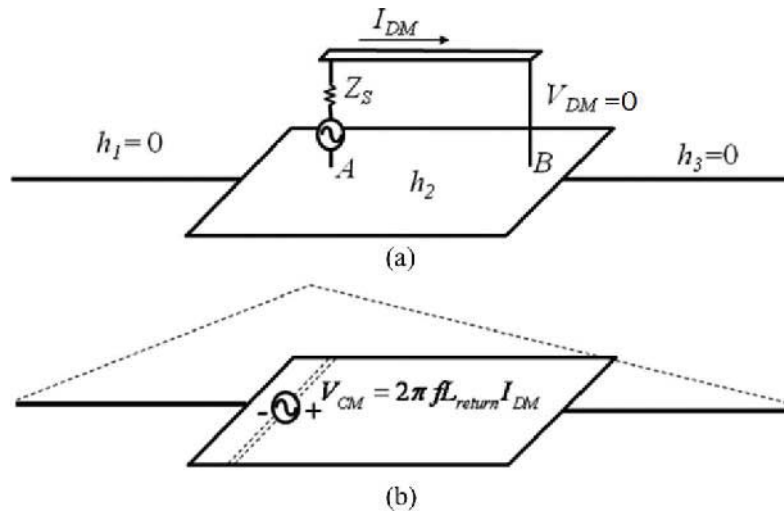


FIGURE 11.5 Imbalance difference model for the shorted trace structure. [7]

Calculating the Imbalance Factor

The calculator calculates the imbalance factor, h , using (11.10). L_{trace} is obtained by [64],

$$L_{trace} = \begin{cases} \frac{\mu_0}{2\pi} \ln\left(\frac{8t}{a} + \frac{a}{4t}\right) l_t & a/t \leq 1 \\ \frac{\mu_0}{a/t + 1.393 + 0.667 \ln(a/t + 1.444)} l_t & a/t > 1 \end{cases}, \quad (11.13)$$

where μ_0 is the permeability of free space and t and l_t are the dielectric thickness and trace length, respectively. L_{return} is calculated by [67],

$$L_{return} = \frac{\mu_0}{\pi} \frac{t l_t}{W} \frac{1}{\sqrt{1 - 4(1 - 2t/W)(s/W)^2}}, \quad (11.14)$$

where s is the offset of the trace from the center of the board and W is the board width as shown in FIGURE 11.6. The algorithm will calculate the coordinates of the trace center, C , and obtain the offset, s , by,

$$s = \frac{|W - 2C_y|}{2} \quad (11.15)$$

where C_y is the y coordinate of point C . Note that when the trace is at the corner of the board as shown in FIGURE 11.7, the magnetic field generated by the returning current can wrap around the board's corner instead of the whole width of the board and thus, make L_{return} larger. To avoid underestimating L_{return} , the algorithm will replace W in (11.14) by $dist1 + dist2$, the sum of the distances from the trace center to the two nearest board edges, when the trace is located at the corner of the board as shown in FIGURE 11.7. Offset, s , is correspondingly replaced by,

$$s = \frac{|dist1 - dist2|}{2}. \quad (11.16)$$

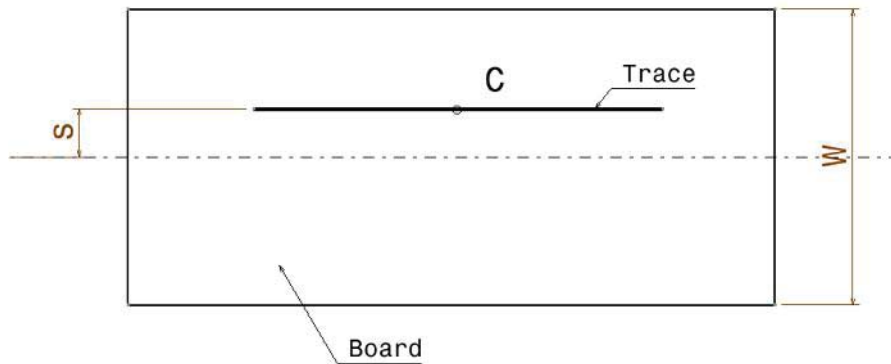


FIGURE 11.6 Trace position relative to the board.

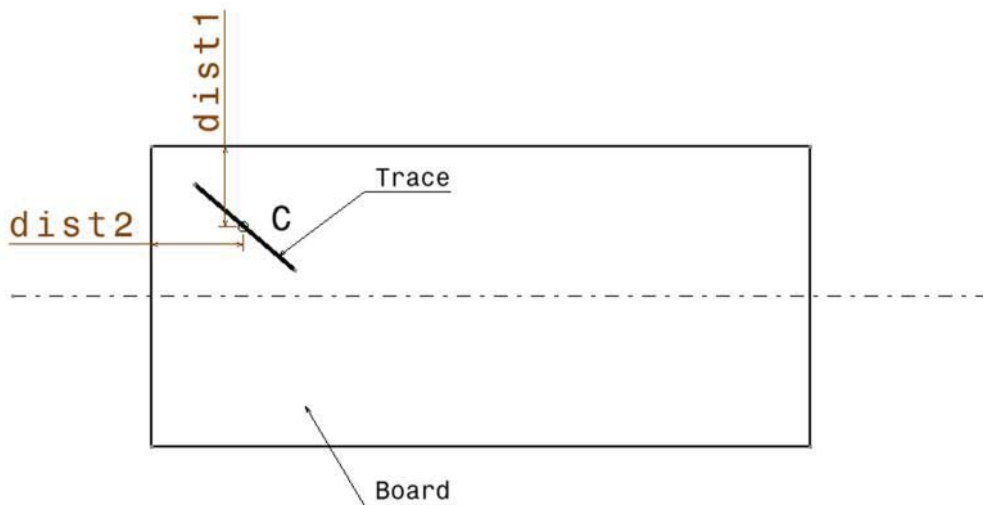


FIGURE 11.7 Trace at the corner of the board.

11.2.2 Radiated Emissions Estimation Algorithm

A detailed description of the radiated emissions estimation algorithm is provided in 10.2.3. The CM emissions calculator supports multiple-cable geometries. It also separates the emissions due to electric-field coupling from the emissions due to magnetic-field coupling. Both components are calculated by the same estimation algorithm in 10.2.3 using different effective board lengths for the different coupling mechanisms.

Electric-Field Coupling

As shown in FIGURE 11.4(b), the out-of-phase components of the two CM noise sources are responsible for electric-field coupling. These source components drive the attached cables relative to the board. Different board-cable configurations are treated individually by the algorithm to calculate the effective board length. FIGURE 11.8 shows a PCB layout with horizontally and vertically oriented traces. The angle between the trace and the board centerline is β . If β is smaller than 45 degrees, the trace is considered horizontally oriented. Otherwise, it is considered to be vertically oriented. As discussed in 10.2.3, when a cable is driven relative to the board, an estimate of the effective board length is required to calculate the radiated emissions. The effective board length is determined by assigning the trace-board-cable configurations to one of four cases.

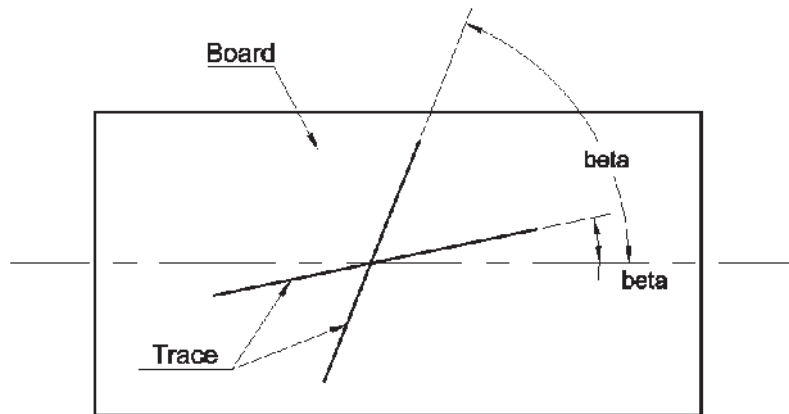


FIGURE 11.8 Trace orientation.

Case 1: Horizontal trace with cables attached to one side. (FIGURE 11.9)

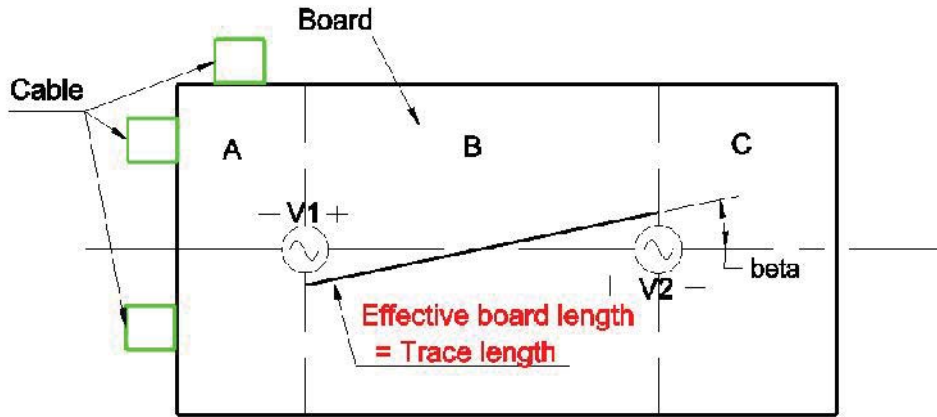


FIGURE 11.9 Electric field coupling: Horizontal trace with cables attached to one side.

This is equivalent to the single-source-single-cable case in 10.2.3, except that the effective board length used to calculate the board factor is different. In this case, the CM source, V_1 , is driving board region A and attached cables against board region B as shown in FIGURE 11.9, so the algorithm sets the effective board length equal to the trace length.

Case 2: Horizontal trace with cables attached to both sides. (FIGURE 11.10)

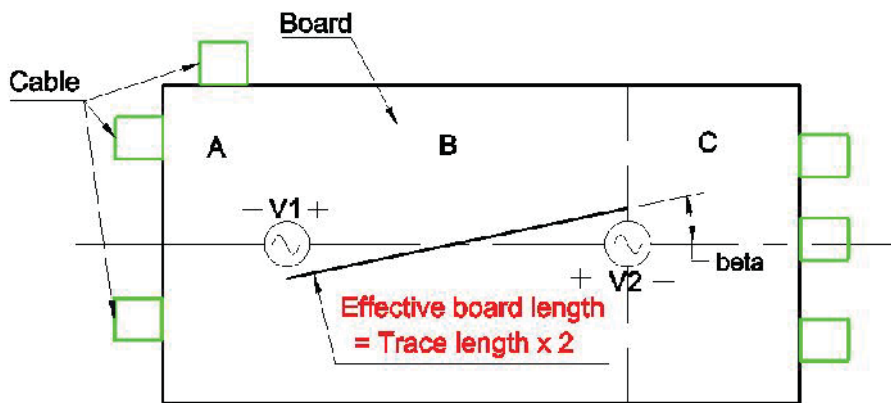


FIGURE 11.10 Electric field coupling: Horizontal trace with cables attached to both sides.

If the cables are attached to opposite ends of the board as shown in FIGURE 11.10, the CM source V1 will drive the cables attached to area A against the board area B and the source V2 will drive the cables attached to the area C against the board area B. The algorithm handles this case by setting the effective board length equal to twice the trace length. While this is not an exact solution, it is a reasonable worst-case approximation for electrically small boards.

Cables attached to board area B are treated as though they were attached to one side of the board. In other words, if there are already cables attached to area A and C of the board, cables attached to B will have no effect on the effective board length.

Case 3: Vertical trace with cables attached to one side. (FIGURE 11.11)

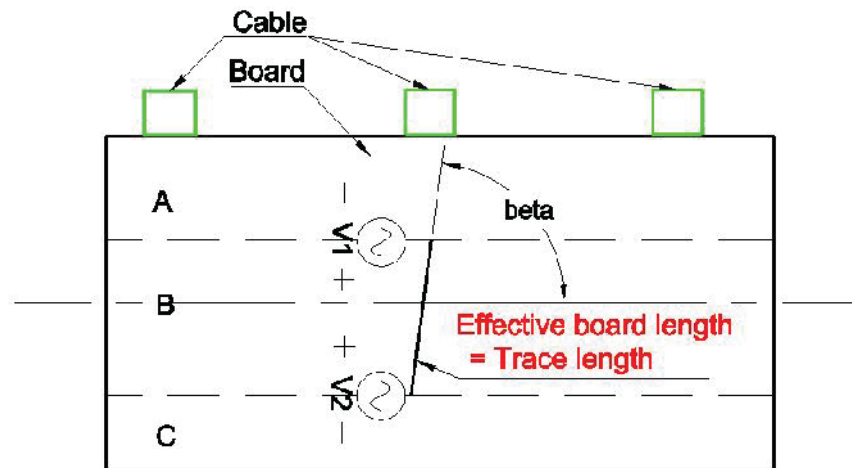


FIGURE 11.11 Electric field coupling: vertical trace with cables attached to one side.

When the angle between the trace and the board center line exceeds 45 degrees, the algorithm considers the trace to be vertically oriented and arranges the board areas A, B and C as shown in FIGURE 11.11. Calculation of the effective board length

corresponding to the different cable positions is same as the cases where the trace is horizontally oriented.

In Case 3, all cables are attached to one side of the board (area A or C), so the algorithm uses the trace length for the effective board length.

Case 4: Vertical trace with cables attached to both sides. (FIGURE 11.12)

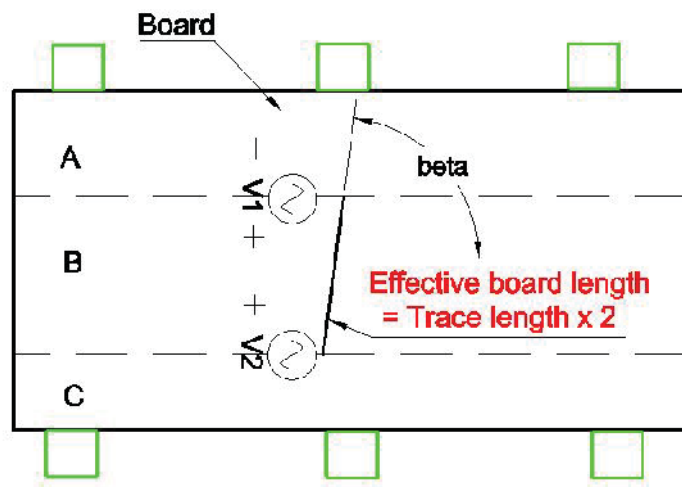


FIGURE 11.12 Electric field coupling: vertical trace with cables attached to one side.

In Case 4, the cables are attached to both sides of the board, so the algorithm makes the effective board length equal to twice the length of the trace.

Magnetic-Field Coupling

As shown in FIGURE 11.5 (b), the magnetic-field coupled component is modeled using only one CM noise source. As a result, the CM source will drive the attached cables against the board, if all cables are attached to one side of the board, and will drive some attached cables against others if they are attached to both sides of the board.

Case 5: Horizontal trace with cables attached to one side. (FIGURE 11.13)

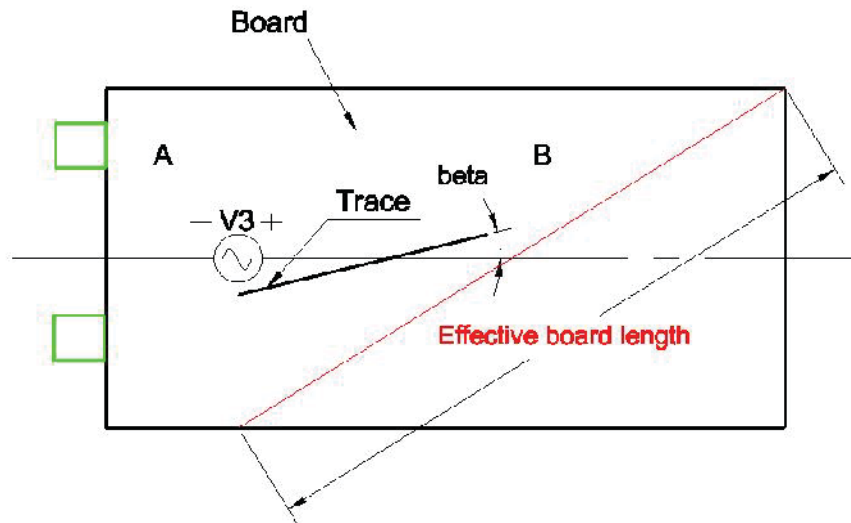


FIGURE 11.13 Magnetic field coupling: Horizontal trace with cables attached to one side.

As shown in FIGURE 11.13, the CM source, V_3 , drives board area A and the cables against board area B. The algorithm uses the diagonal length of the board area B for the effective board length. If the cables are attached to area B instead of A, the diagonal length of board area A will be used as the effective board length.

Case 6: Horizontal trace with cables attached to both sides. (FIGURE 11.14)

In this case, since the CM voltage is driving cables against cables, the algorithm ignores the effective board length and sets the board factor equal to 1.

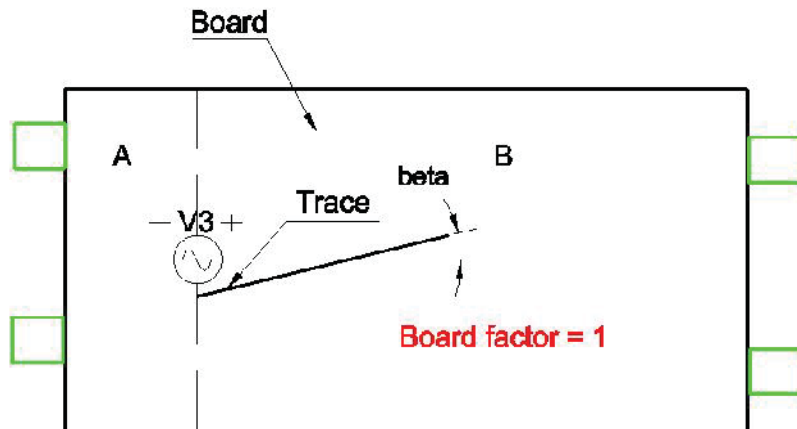


FIGURE 11.14 Magnetic field coupling: Horizontal trace with cables attached to both sides.

Case 7: Vertical trace with cables attached to one side. (FIGURE 11.15)

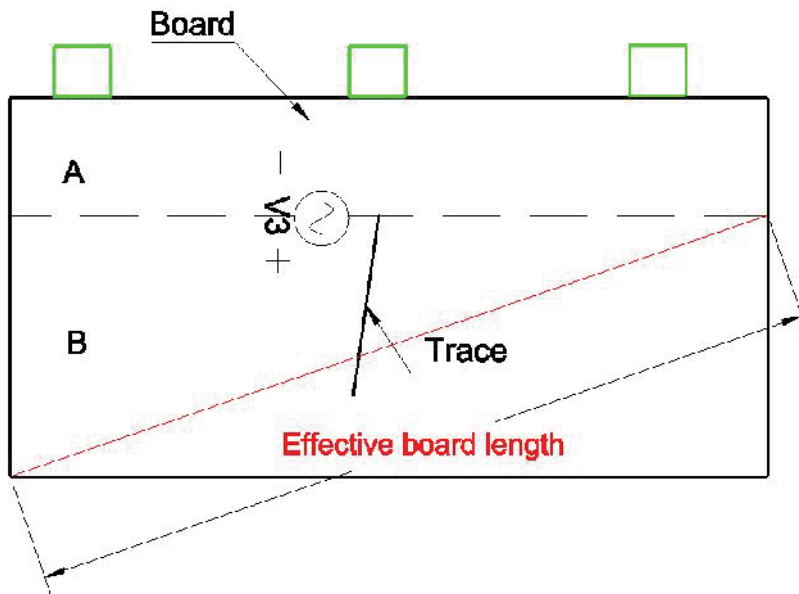


FIGURE 11.15 Magnetic field coupling: Vertical trace with cables attached to one side.

When the trace is vertically oriented, the algorithm arranges the board areas A and B as shown in FIGURE 11.15. Calculation of the effective board length corresponding to the different attached cables positions is same as it is for horizontally oriented traces.

In Case 7, all cables are attached to one side of the board (area A or B), so the algorithm uses the diagonal length of the opposite board area as the effective board length.

Case 8: Vertical trace with cables attached to both sides. (FIGURE 11.16)

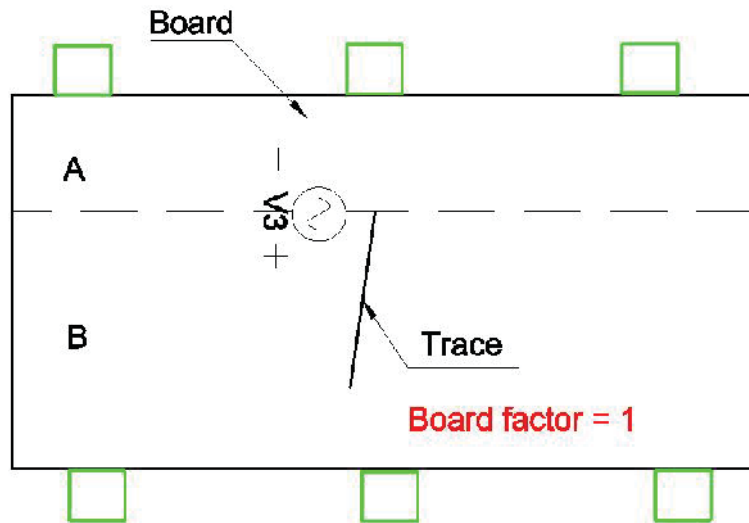


FIGURE 11.16 Magnetic field coupling: Vertical trace with cables attached to both sides.

In Case 8, the cables are attached to both sides of the board, so the algorithm sets the board factor to 1.

11.2.3 Assumptions Made in the Derivation and Implementation of These Algorithms

The width of the microstrip trace and the thickness of the dielectric layer are small relative to a wavelength. This ensures the propagation on the trace is quasi-TEM. This assumption was made in order to calculate and apply the imbalance difference method in (11.10), (11.13) and (11.14).

The signals are in phase on both ends of the trace. The algorithm does not currently account for any phase shift between the signal at the source end and the signal at the load end.

11.3 Conclusion

This calculator determines the maximum possible radiated emissions due to common-mode currents induced on cables attached to a PCB with a microstrip trace. The current implementation is limited to microstrip traces that are short relative to a wavelength at the highest frequency of the analysis. The algorithm could be extended by using complex values for the differential-mode voltages and equivalent common-mode voltage sources at each end of the trace.

12. POWER BUS EMI ALGORITHM

12.1 Introduction

High frequency noise on the power bus can result in significant radiated emissions. The Power Bus EMI calculator was developed to calculate the maximum possible radiated emissions from printed circuit board power plane structures. The calculator utilizes simple closed-form expressions developed by Leone [68], Shim [69] and Zeng [70].

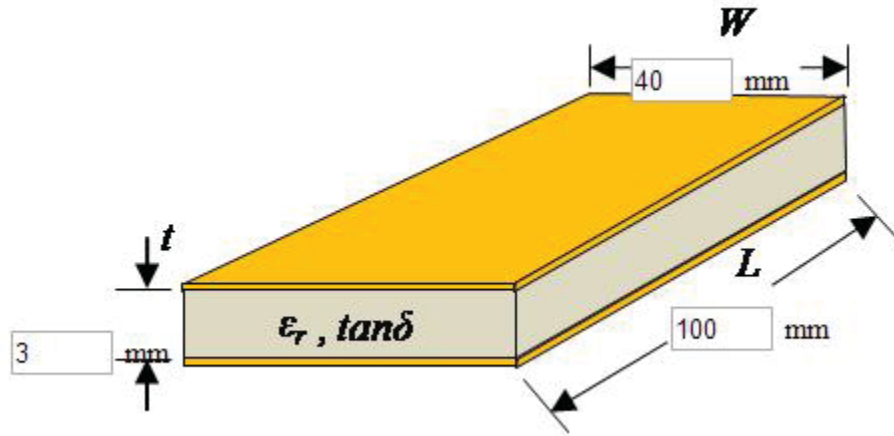


FIGURE 12.1 Power plane structure.

The power bus structure is illustrated in FIGURE 12.1. The power planes have a length, L , a width, W , and a conductivity, σ . The dielectric layer has a thickness, t , a relative dielectric constant, ϵ_r , and a loss tangent, $\tan\delta$. The noise source can be expressed as the maximum current drawn from the planes by the active devices, I_i , or the maximum voltage fluctuation at the board edge, V_{max} . For the current source, parameters of the components on the board are needed to estimate the voltage fluctuations that will appear on the planes. These parameters include the number of active and passive

component connections to the power bus, N_c , the equivalent series resistance of these components, R_c , and the connection inductance of these components, L_c [69].

The calculator calculates the maximum radiated electric field at a distance of 3 meters from the board and plots the results in $dB\mu V / m$ from a specified minimum frequency, f_1 , to a specified maximum frequency, f_2 , as shown in FIGURE 12.2.

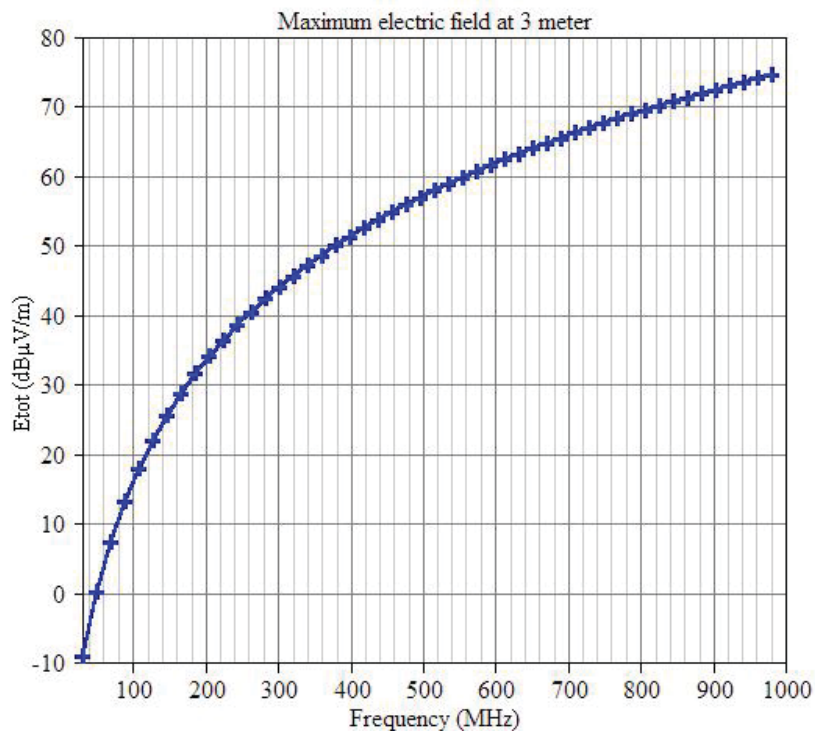


FIGURE 12.2 Example of output from Power Bus EMI calculator.

12.2 Description of Algorithm

The calculator uses one of two separate algorithms depending on the type of noise source specified. The *Components on Board* algorithm determines the maximum radiated emissions based on the maximum noise current drawn from the power planes and information about the components on the board. The *Maximum Voltage at Board Edge*

algorithm determines the maximum radiated emissions based the maximum voltage fluctuation at the board edge.

12.2.1 Components on Board Algorithm

The derivation of the closed-form expression used by the algorithm is well documented in [69]. For relatively high-Q resonances, the maximum radiated field from a populated rectangular board can be expressed as,

$$|E| \leq \frac{120I_i}{\epsilon_r \cdot \min(W, L)} \cdot \frac{t}{r} \cdot \left(\tan \sigma + \frac{\delta_s}{t} + \frac{N_c R_c}{\omega C_0 (R_c^2 + \omega^2 L_c^2)} \right)^{-1} \quad (12.1)$$

where r is the distance from the board, δ_s is the skin depth of the plane conductors, and C_0 is the capacitance between the power planes. r is set to three meters in the calculator, δ_s and C_0 can be found by,

$$\delta_s = \sqrt{\frac{2}{\omega \mu_0 \sigma}} \quad (12.2)$$

$$C_0 = \epsilon_r \epsilon_0 \frac{W \cdot L}{t} \quad (12.3)$$

The calculator returns an error if the input value of the board width, W , is greater than the input value for the board length, L . As a result, the term, $\min (W, L)$, in (12.1) is equivalent to W .

12.2.2 Maximum Voltage at Board Edge Algorithm

The noise current drawn from the power planes causes voltage fluctuations. For boards that have already been built, it is usually easier and more accurate to measure the power bus voltage instead of estimating it based on the current drawn by the active components. The *Maximum Voltage at Board Edge* algorithm is based on the closed-form equation in [70], which calculates the maximum radiated emissions from a rectangular power bus with a given maximum voltage along the board edge. The maximum radiated electric field strength is expressed as,

$$|E_{\max}| = \begin{cases} \frac{f\sqrt{\mu\epsilon_0}V_{\max}W}{r} & f < f_{t1} \\ \frac{f\sqrt{\mu\epsilon_0}V_{\max}L}{r} & f_{t1} \leq f < f_{c2} \\ \frac{f\sqrt{\mu\epsilon_0}V_{\max}\sqrt{L^2+W^2}}{r} & f \geq f_{c2} \end{cases} \quad (12.4)$$

where f_{t1} is a transition frequency that occurs midway between adjacent resonances just below the cutoff frequency of the TM_{01} mode and f_{c2} is the cutoff frequency of the TM_{11} mode. They can be found by [70],

$$f_{t1} = \frac{1}{2} \left(\frac{1}{2\sqrt{\mu\epsilon_r\epsilon_0}} \frac{1}{W} + \frac{1}{2\sqrt{\mu\epsilon_r\epsilon_0}} \frac{m}{L} \right) \quad (12.5)$$

$$f_{c2} = \frac{1}{2\sqrt{\mu\epsilon_r\epsilon_0}} \sqrt{\left(\frac{1}{L}\right)^2 + \left(\frac{1}{W}\right)^2} . \quad (12.6)$$

The term $\frac{1}{2\sqrt{\mu\epsilon_r\epsilon_0}} \frac{m}{L}$ in (12.5) is the cutoff frequency of the TM_{m0} mode that occurs at the mode frequency closest to, but lower than, the TM_{01} mode.

12.2.3 Assumptions Made in this Derivation

The closed-form equations in both algorithms are developed based on a resonant cavity model that assumes the spacing between the two planes is electrically small and much smaller than the length and width of the board. Also, the shape of the planes must be rectangular (or nearly rectangular).

The Components on Board algorithm makes additional assumptions in order to estimate the voltage fluctuations caused by the active components on the board. This algorithm assumes that the active and passive components are distributed fairly uniformly over the board. It also assumes that a worst-case equivalent series resistance and connection inductance can be defined that adequately represents the majority of the board components. For boards with large numbers of decoupling capacitors, the ESR and connection inductance of these capacitors should be used. The decoupling capacitor capacitances are not relevant, since the inductance will typically dominate at board resonance frequencies.

12.3 Conclusion

This calculator determines the maximum possible radiated emissions from a rectangular power bus structure based on equations derived and validated in [68], [69] and [70]. It can be applied to power buses consisting of two nearly rectangular planes

with a small spacing relative to the length and width of the planes. It calculates the maximum radiated fields for a board in free space and does not model near-field interactions with cables or enclosures that might also contribute to a radiated emissions problem.

13. DIFFERENTIAL-MODE EMI ALGORITHM

13.1 Introduction

Differential-mode (DM) currents are currents that travel from the source to the load on one trace and return on another trace or plane along a path that is parallel and very near to the out-going path. Because the fields from the out-going current are nearly canceled by the fields from the returning current, differential-mode currents are inefficient radiation sources. They are much less likely to radiate significant amounts of electromagnetic energy when compared to common-mode currents that flow in one direction on one or more conductors with no near-by return path. Nevertheless, large differential-mode signal currents on circuit board traces are capable of causing radiated emission problems. The differential-mode EMI calculator was developed to calculate the maximum possible radiated emissions due to the DM currents on PCB traces. The calculator utilizes simple closed-form expressions described by Paul [71]. This report is intended to provide details of the implementation sufficient to allow others to develop their own version of this calculator.

The circuit board trace configuration to be analyzed is illustrated in FIGURE 13.1. The trace with a length, l , is located above a plane that carries the return current. The dielectric layer has a thickness of t . The differential-mode signal on the trace is terminated with a capacitive or resistive load. The calculator determines the maximum radiated electric field from this configuration at a distance of 3 meters and plots the results in $dB\mu V / m$ up to 500 MHz, as shown in FIGURE 13.2.

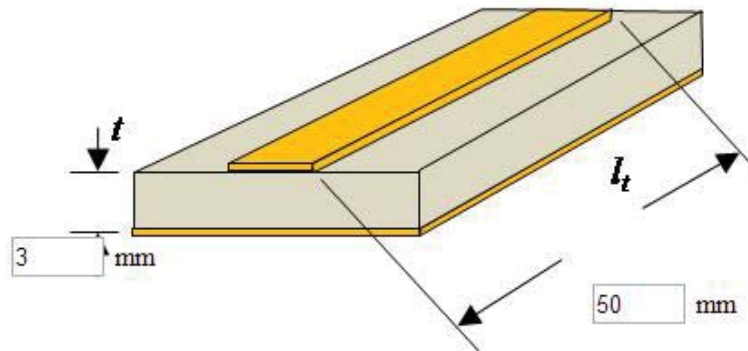


FIGURE 13.1 Printed circuit board trace above a plane.

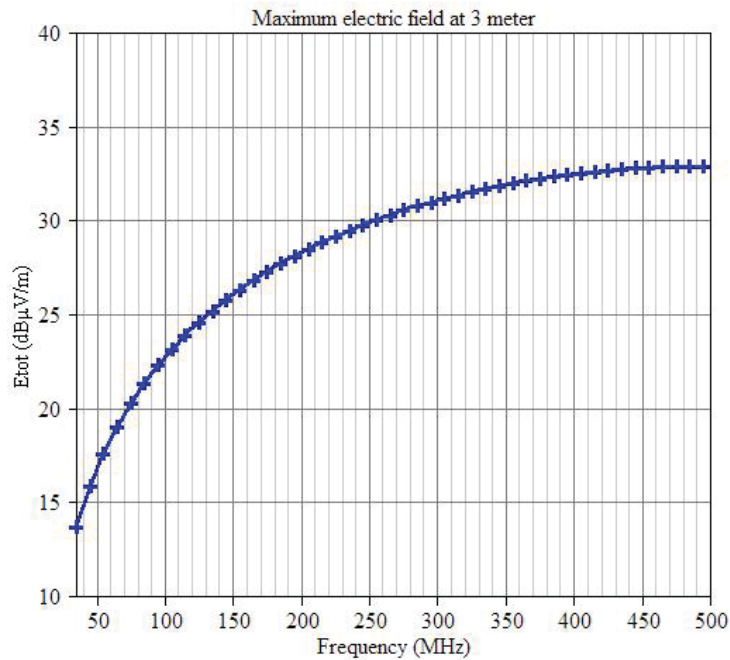


FIGURE 13.2 Example of output from the Differential-Mode EMI calculator.

13.2 Description of Algorithm

To calculate the maximum possible radiated electric field above the PCB, image theory is applied. The ground plane is replaced by an image trace on the other side of the ground plane carrying the same current as the original trace flowing in the opposite

direction. For electrically short sections, the trace and its image can be treated as two Hertzian dipoles and their radiated electric field strength can be calculated using the closed-form expression in [72].

$$|E_{\max}| = 1.316 \times 10^{-14} \frac{I_{DM} f^2 l_t \cdot 2t}{r} . \quad (13.1)$$

In this implementation the distance from the board, r , is set to three meters; so (12.1) can be further simplified to,

$$|E_{\max}| = 8.8 \times 10^{-15} I_{DM} f^2 l_t t . \quad (13.2)$$

The magnitude of the differential-mode current flowing on the trace is,

$$I_{DM} = \left| \frac{V_{Signal}}{Z_{load}} \right| . \quad (13.3)$$

The algorithm caps the trace length, l_t , at one sixth of a wavelength because above that, the assumption of a uniform current along the trace will be inaccurate. As long as the trace is less than about one wavelength, (2) provides a reasonable upper-bound when l_t is capped at $\lambda/6$. For trace lengths greater than one wavelength, the traveling wave antenna model described in [73] is recommended. The expression for the maximum possible radiated emissions from a traveling wave antenna is similar to (2) with no limitation on the trace length, l_t ; however this has not been implemented in the algorithm. Electrically long microstrip traces are capable of producing significant radiated emissions due to differential-mode currents, but they usually don't. Losses in the structure and details of the routing generally prevent DM radiation from these traces from being an

issue. For this reason, electrically long microstrip traces should generally be modeled using full-wave analysis techniques when one suspects that radiation from these traces may be a problem.

This algorithm provides a reasonably accurate estimate of the maximum possible emissions due to radiation directly from the trace/return structure provided that:

5. The length of the trace and the thickness of the dielectric layer are electrically small.
6. The ground plane width is much greater than the trace width and the dielectric thickness.
7. The trace length is limited to one wavelength. At the maximum frequency, 500 MHz, that this calculator supports, the wavelength is 60 cm.

13.3 Conclusion

This calculator determines the maximum possible radiated emissions due to differential-mode currents flowing on PCB traces. It is limited to traces with lengths that are smaller than a wavelength. For longer traces, the travelling wave antenna model in [73] could be used.

It is important to note that for most realistic circuit board trace structures and currents, the differential-mode radiation should be well below the FCC or CISPR radiated emission limits. Any circuit that has loop areas sufficient to cause excessive differential-mode radiation is likely to have other EMC problems as well.

Differential-mode radiation is rarely, if ever, the dominant source of a radiated emissions problem. For that reason, the relatively simple closed-form equation provided in [63] is accurate enough to flag a significant problem. Precise calculations of the

radiation from differential signal currents on a printed circuit board are not helpful when common-mode currents are the dominant EMI source.

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