The DEPFET Mini-matrix Particle Detector

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Abstract

The DEPFET is new type of active pixel particle detector. A MOSFET is integrated in each pixel, providing the first amplification stage of the readout electronics. Excellent noise parameters are obtained with this layout. The DEPFET detector will be integrated as an inner detector in the BELLE II and ILC experiment. A flexible measuring system with a wide control cycle range and minimal noise was designed for testing small detector prototypes.

Noise of 60 electrons of the equivalent input charge was achieved during the first measurements on the system.

Keywords: DEPFET, BELLE II, ILC, silicon pixel detector.

1 Introduction

Accelerator physics experiments use linear or cyclic accelerators to accelerate charged particles. The particles are collided at an interaction point surrounded by various types of particle detectors that track the newly-originated particles. The pixel semiconductor detector near to the interaction point is called an inner detector. The DEPFET Collaboration is an international organization developing a new type of pixel semiconductor inner detector for the International Linear Collider and BELLE II, an upgrade of the BELLE experiment in Japan. DEPFET is an abbreviation of 'DEPleeted Field Effect Transistor'. A new system has been developed for measuring and characterizing small samples of the DEPFET detector. This system enables precise charge measurements and a flexible high resolution configuration of searing signals.

2 The DEPFET detector

2.1 Active pixel structure

The DEPFET detector itself consists of a high-resistivity depleted n-substrate and two p-regions, creating a pnp-sandwich structure (p frontside-implantation, n-substrate, p-rearside). The n-substrate is depleted sidewards.

The principle of sideward depletion [1, 3] is shown in Fig. 1. The n-substrate (bulk) is depleted from both sides by applying negative voltages to both p-implantations with respect to the bulk. The minimum of the electron potential is in a plane parallel to the front surface. The minimum of the electron's potential is at depth $x_{\min}$ given by [1]

$$x_{\min} = \frac{d}{2} + \frac{\varepsilon_s}{qN_D d}\left(V_d - V_u\right) \qquad (1)$$

where $x_{\min}$ is the depth of the potential minimum in the detector substrate, q is the elementary charge, N_D is the doping concentration of the substrate, d is the total wafer thickness, ε_s is the dielectric constant of the semiconductor, and V_d, V_u are the voltages applied to the rear and front sides. If $V_u = V_d$ the potential minimum is in the middle. Asymmetric voltages are applied in the DEPFET pixel to shift the electron potential minimum close to the front surface, where the MOSFET is located. Additional n-implants hinder electron lateral diffusion and the electrons are concentrated in a small region under the MOSFET channel. This region is called an internal gate.
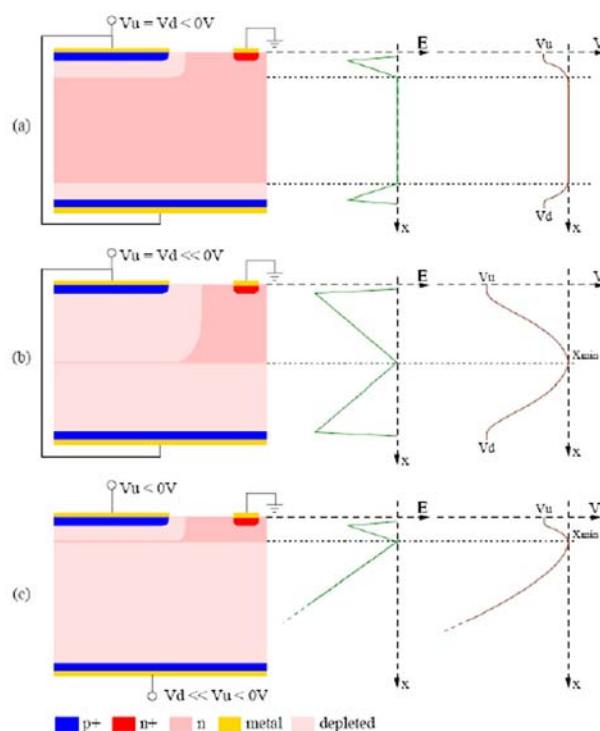

Fig. 1: The Principle of Sideward Depletion

An impinging radiation generates electron-hole pairs in the depleted n-substrate (bulk), the holes drift to the rearside contact, and the electrons are trapped in the internal gate. The internal gate is located directly under the MOSFET channel below the external

gate contact, so the charge stored in the internal gate affects the MOSFET channel. For a fixed drain to source voltage V_{DS} and a constant external gate voltage V_{GS}, the drain current I_D is proportional to the stored charge in the internal gate. The amplification g_q is given by the change of the transistor current δI_D due to the collected charge δQ [1]

$$g_q = \left. \frac{\delta I_D}{\delta Q} \right|_{V_{GS}, V_{DS}}. \qquad (2)$$

Amplification 300–600 pA/e$^-$ is obtained for mini-matrices with channel effective length 4 μm.
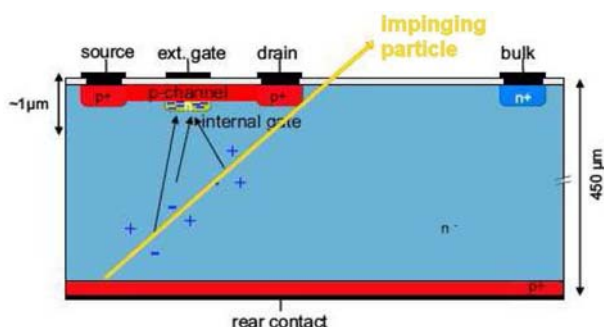

Fig. 2: The DEPFET Pixel Cross-section

2.2 Clearing process

When new charge collection is needed, it is necessary to empty the internal gate. For clearing out the internal gate, there is a clear contact next to the MOSFET transistor. Fig. 3. shows a Cleargate cross-section, and a detailed description of the clearing process is given in [4, 5] and [6]. The electrons are extracted from the internal gate by applying a high positive voltage to the clear contact. This causes the electrons drift to the clear contact, where they are taken away. To prevent losses during charge accumulation, the n$^+$-region below the clear contact is surrounded by the p-well. The n$^+$-region provides an ohmic contact to the clear electrode and with the p-well it provides a reverse biased PN junction that represents a potential barrier for the electrons in the internal gate. When the voltage applied to the clear electrode is high enough, the depleted region in the p-well is able to pass through the p-well and touches the p-well boundary (punch-through effect [2]). In this moment there is no barrier for electrons in the internal gate and they are extracted.
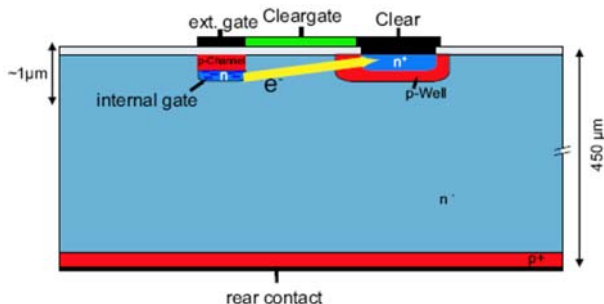

Fig. 3: The Cleargate Cross-section

In order to control the potential barrier between the internal gate and the clear contact, an additional MOS structure cleargate is added. If the cleargate is on a positive potential during the clear process, it helps to form an n-channel in the p-well. But whereas the n-channel is situated at the surface, the punch-through effect is also effective in the depths of the internal gate.

3 Measuring system

3.1 Conception

The Mini-matrix Measuring System is able to measure and characterize a small (3.5×3.5 mm) prototype of a DEPFET (see Fig. 4). The small sensor has 4×12 active pixels, allowing studies of the DEPFET structure behavior and processes during operation of the sensor. The Mini-matrix readout setup allows us to make a precise collected charge measurement in each pixel with low noise, charge shearing among multiple pixels, clustering, charge-loss measurement, trimming steering voltage values and timing of driving signals.
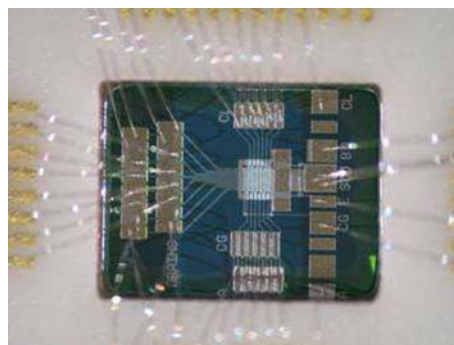

Fig. 4: Photo of the DEPFET Mini-matrix

The system is made of commercial and custom-made blocks as a PC with an 8-channel 14-bit 125 Msps PCI data acquisition card, an FPGA control card, a current readout and a switching circuit. The custom-made current readout circuit is made of 8 low noise trans-impedance readout amplifiers and the switching circuit with 12 individual analog switches that are necessary for controlling the gate and clear electrodes of the DEPFET Mini-matrix sensor.
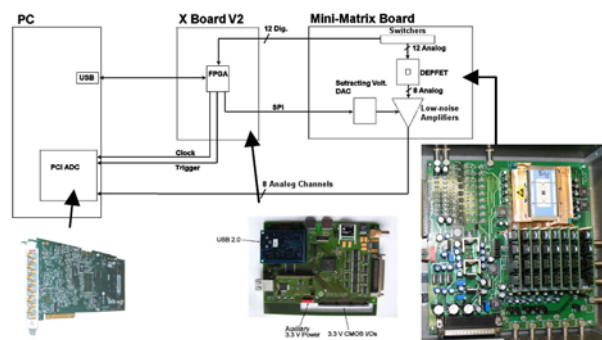

Fig. 5: Conception of the Measuring System

The switching circuit can perform gate voltage timing with resolution of 7.5 ns. A voltage for a pedestal current subtraction is reconfigurable. The measuring system is controlled and configured by the PC. All 8 channels are digitized by 14-bit ADCs with 125 Msps for each channels in parallel with frame readout time 26 us.

3.2 Processing the signals from the detector

The readout signals from the DEPFET detector are the current base. The source of the MOSFET pixel is kept at the ground potential and the MOSFET's drain is at -5 V. The output signal has two components, constant pedestal current and signal current proportional to the charge in the internal gate. The pedestal current is subtracted at the analog level at the inputs of the low noise readout amplifiers. The drain signal currents are read out by 8 amplifiers in parallel and digitized by a GaGe Octopus data acquisition card with 8 14-bit/125 Msps inputs.
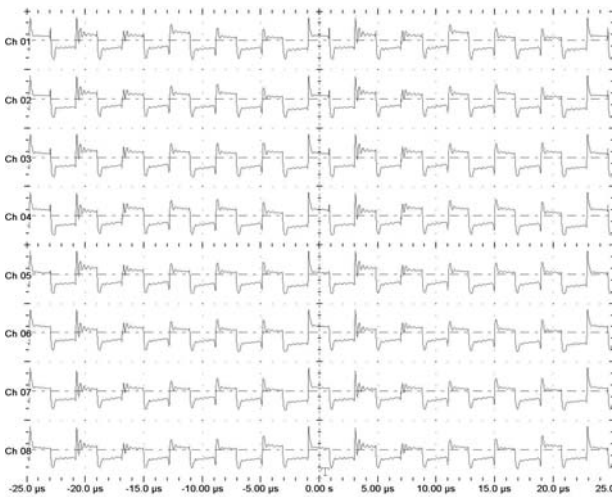

Fig. 6: The Stream of 8 Drain Signal Currents

Fig. 6 shows the typical digitized stream of illuminated DEPFET matrix. The signal stream is recorded and acquired by the data acquisition system (DAQ).

3.3 Low-noise current readout amplifiers

The system has 8 parallel current readout amplifiers that consist of 3 parts: TIA, the non-inverting operational amplifier (EL2126), and the fully differential output buffer (AD8139), which can be configured as differential or single-ended.

The measured input-referred equivalent noise current of the readout amplifiers is 18 nA RMS. The noise is reduced to 8.1 nA RMS by using a 4-sample averaging method, and to 3.2 by 10-sample averaging. Aver-

aging of 90 samples is used in the DAQ system. The noise contribution of the amplifiers is less than 3.6 nA, which is 1 ADU of the 14-bit digitizing system.
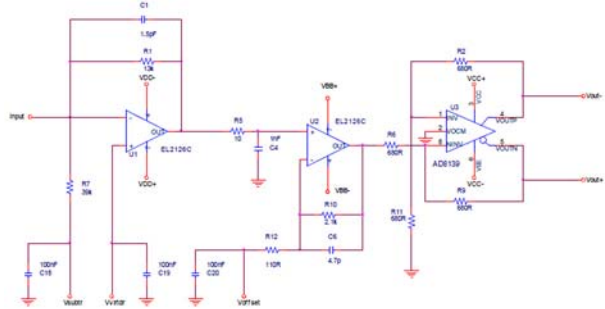

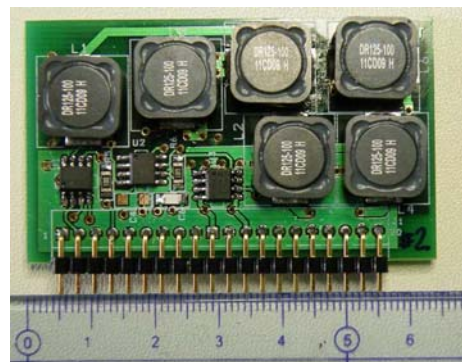Fig. 7: Scheme of the Current Readout Amplifier

Fig. 8: Photo of the Current Readout Amplifier Board

3.4 DEPFET matrix steering

The Mini-matrix DEPFET sensor requires 6 external gate channels and 6 clear switching channels that are controlled by the FPGA card and configured via a PC program with time resolution of 7.5 ns. Three additional trigger channels are available for ADC card synchronization. The external gate electrodes are used for addressing the rows of the matrix. The clear electrode is used to clear one row of pixels.
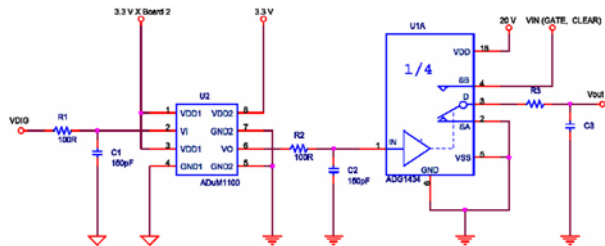

Fig. 9: Scheme of the Double-throw Switch

Fig. 9 shows a one channel scheme of the switch. Each channel consists of 1/4 of the ADG1434 analog switch and galvanic separator ADuM1100 insulating FPGA card digital control inputs.

The readout frame scheme is very flexible and can be configured to fit current requirements. The FPGA

generates driving pulses according to the configuration software.

Fig. 10 shows the structure of the whole matrix readout frame configured in the control program, and Fig. 11 shows the real control channel scope plots. The frame length is approx. 26 μs. The GATE_ON signals are approx. 100 ns overlapping for each matrix row to make a continuous drain current flow. This prevents saturation of the amplifiers.
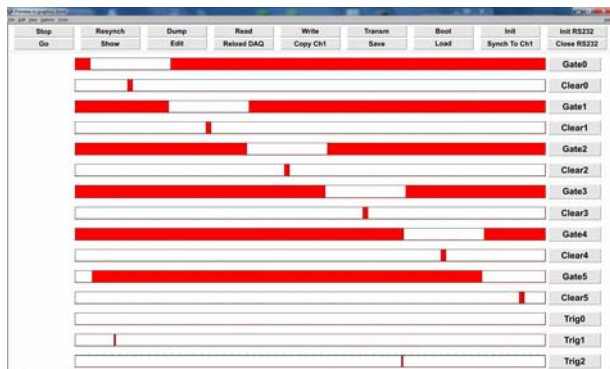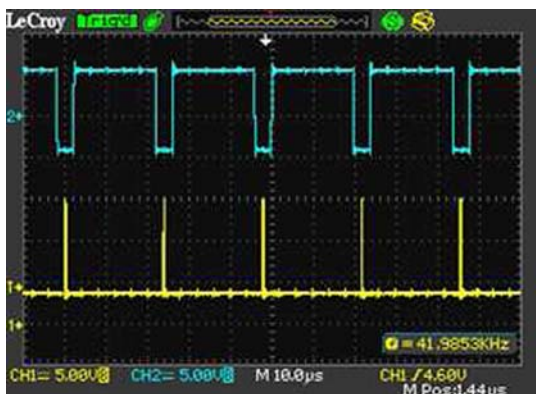

Fig. 10: Sequencer Configuration Software

Fig. 11: Scope Plots of the External Gate Channel (above) and Clear Channel (below)

3.5 DAQ Control Monitor

Fig. 12 displays the results of the DAQ control monitor. The frame is triggered by a hardware trigger generated by the sequencer. The whole frame is recorded and the signals for each row are software-triggered. Samples are taken before and after the clear signal. The evaluated areas are indicated by blue stripes in the 'Full monitor with soft triggers' top left window in Fig. 12. Complete data set can be saved in ASCII format with: ADU, hexadecimal or mV float formats. The top middle window is the signal histogram and the top right window indicates the distance between the hardware triggers. The bottom row of windows contains, from the left: real acquired signals in mV, the histogram of the evaluated areas and the evaluated parts of the signals. The DAQ control monitor helps to set the software triggers.
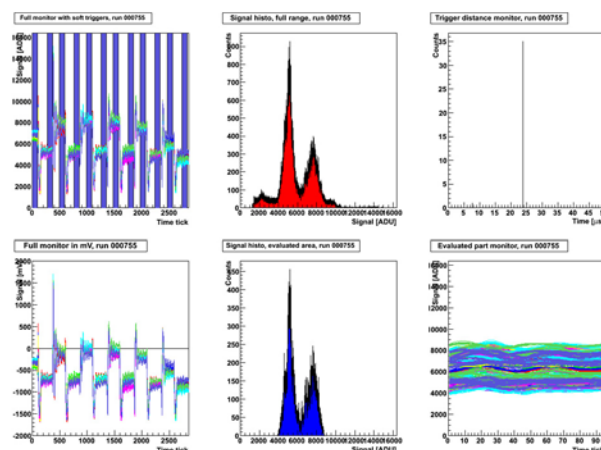

Fig. 12: The DAQ Control Monitor

A visualization tool also forms part of the DAQ Control Monitor. The window in Fig. 13 left shows the real pixel layout and the signal response in ADU units of the 14-bit resolution ADC. 1 ADU corresponds approximately to a charge of 6 electrons. The noise of each pixel is indicated in the right window. The noise of the matrix in the dark expresses the total system noise. The total noise of all pixels is less than 10 ADU, which is a charge of 60 electrons.
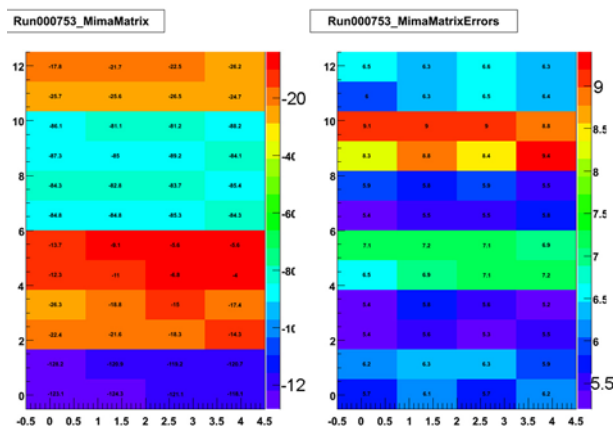

Fig. 13: The Matrix Signal Response and Noise Visualization

Fig. 14: A Photo of the Measuring System

4 Conclusions

A measuring system has been designed for the DEPFET Mini-matrix particle detector. The matrix of the detector with 4×12 pixels can be repeatedly read out with frame frequency of 38 kHz and noise lower than 60 electrons. The steering pulses can by configured with high resolution of 7.5 ns. These parameters are efficient enough to start testing and characterizing the prototypes of the DEPFET particle detector. The development of the second measuring system has already started. Noise below 20 electros should be achieved with the new measuring system.

Acknowledgement

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