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2.45 GHz Class E Power Amplifier for a Transmitter Combining LINC and EER

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A 10 W class-E RF power amplifier (PA) is designed and fabricated using a Cree GaN HEMT. The proposed PA uses an innovative input circuit to optimize band with. At 2.45 GHz the PA achieves a PAE of 60 % at an outputpower of 40 dBm. The resulting amplifier is simulated and constructed using a transmissionline topology. Two of these amplifiers are fabricated on a single board for outphasing application. Their suitability for outphasing application and supply modulation is investigated.

Keywords: Class E, power amplifier, CLIER.

1 Introduction

Efficiency is a more and more critical issue when designing transmitters, both to save energy costs at the base station and to reduce the power consumption of mobile terminals to increase battery life. Efficiency boosting techniques tend to rely on switch-mode amplifiers (SMA). Conventional amplifier classes like A, AB, which offer high linearity at the cost of efficiency are avoided. The non-linearities caused by these amplifiers are compensated using envelope elimination and restoration (EER)[2] or vector addition (LINC) [1] techniques or both (CLIER) [5].

For implementation of a CLIER amplifier architecture a Class E amplifier is well suited both for the LINC and for the EER part. LINC consists of two non-linear amplifiers. The input signal, containing both amplitude $a(t)$ and phase $\varphi(t)$ is transformed into two solely phase modulated signals with constant envelopes. Both non-linear amplified signals are vector combined at the output, resulting in an amplified replica of the original time varying envelope signal. Additionally, the supply of the amplifiers is modulated with a slowly varying signal. This reduces the dynamics of the LINC signal and thereby increases the efficiency of the entire system. This paper focuses on the implementation of class E amplifiers.

2 Theory

For lossless operation of the Class E amplifier there are two criteria that have to be met: First, zero voltage across the transistor terminals when the switch closes [4]

$$u_s(\omega t = \omega t_c) = 0. \tag{1}$$

And, second, no voltage building across the transistor terminals while the switch is closed

$$\frac{\mathrm{d}u_s}{\mathrm{d}t}(\omega t = \omega t_c) = 0. \tag{2}$$

To obtain this non overlapping between voltage and current a complex load impedance is imposed on the switch output terminals, which results in a phase shift between current and voltage of the output signal.

Fig. 1 shows a typical Class E circuit. The transistor is ideally replaced with a switch. The load network consists of a parallel capacitor C and an inductance L in series with a tuned output network L_0C_0 and load resistance R. When using a real transistor the capacitor C can comprise the intrinsic transistor capacitance C_{ds} and an external capacitance. An RF choke at the supply voltage enforces a DC supply current.

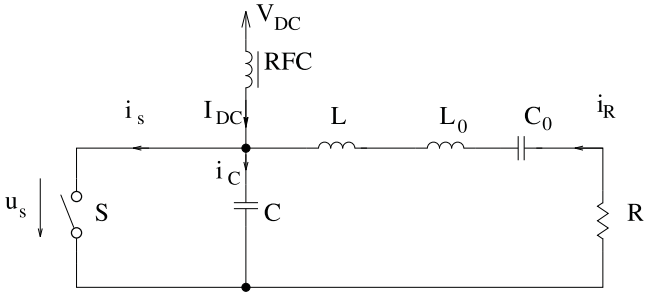

Fig. 1: Class E circuit with lumped elements

The output tuning network L_0C_0 forces the current through the load resistance R to be a sinusoidal function of ωt angular time and phase shift φ. The current can be described as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi). \tag{3}$$

Because the RF choke enforces a DC current I_{DC}, the difference between output- and DC current flows into the switch-capacitance network. Initially, when the switch S is closed, the switch current is zero $i_s(\omega t = 0) = 0$. With (3), the DC current can then be described as

$$I_{DC} = -I_R \sin(\varphi). \tag{4}$$

While the switch S is closed the capacitor C has zero voltage across and consequently all current starts flowing through S for $\omega t > 0$. The current flowing the switch S $i_s(\omega t)$ can be described as

$$i_s(\omega t) = I_{DC} + I_R \sin(\omega t + \varphi) = I_R\left[\sin(\omega t + \varphi) - \sin(\varphi)\right]. \tag{5}$$

At the time $\omega t = \omega t_0 = \pi + k\,2\pi$ the switch S opens and the difference current $i_c(\omega t - \omega t_0) = i_s(\omega t + \omega t_0)$ flows into capacitor C which starts charging. The build up of the voltage $u_s(\omega t)$ across the switch S is determined by the charging of capacitor C, which can be described as

$$u_s(\omega t) = \frac{1}{\omega C}\int_{\omega t_0}^{\omega t} i_c(\omega t)\,\mathrm{d}\omega t. \tag{6}$$

With (5) it follows that

$$u_s(\omega t) = -\frac{I_R}{\omega C}\left[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi\right]. \quad (7)$$

With the first criteria for Class E operation Eq. (1) and Eq. (7) it follows that for optimal operation the phase angle φ can be defined as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482 \text{ deg}. \quad (8)$$

With these equations the resulting normalized voltage can easily be obtained. The normalized voltage and current transients are shown in Fig. 2. As can be seen, there is no overlap between switch current and voltage waveforms, resulting in 100 % switch efficiency.

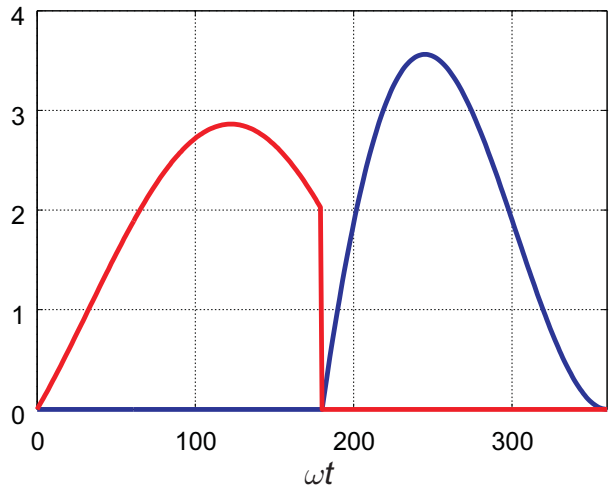

Fig. 2: Switch current (light) and voltage (dark) transient

A common design approach for high frequency Class E PAs is to design a lumped element amplifier [4] and then replace each component with an equivalent transmission line.

This however makes the design and optimization both tedious and time-consuming because only the slightest change in a transmission line parameter will change the load network radically, losing Class E operating conditions.

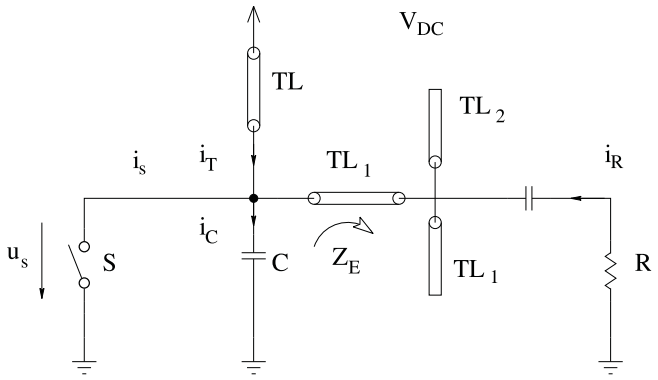

Fig. 3: Class E circuit with transmission lines

A better approach is found in [3]. Consider Fig. 3. Class E operation in this circuit depends on the load network providing a phase angle $\varphi = 49.05$ deg. This complex output impedance, using $\tan\phi = X/R$, can be written as

$$Z_E = \begin{cases} R_E(1 + j1.152) & \text{at } f_0 \\ \infty & \text{at } nf_0, n > 1. \end{cases} \quad (9)$$

The optimum value for the load resistance R_E at the fundamental frequency f_0 is given by

$$R_E = \frac{1}{34.225 f_0 C_s}. \quad (10)$$

By choosing a moderate to high impedance for transmission lines Z_{TL1} and Z_{TL2} and defined output load impedance R_L, circuit parameters can be further obtained by keeping the absolute value of the reflection parameter on both sides of $TL1$ equal $|\Gamma_E| = |\Gamma_G|$. The total admittance combining the load admittance G_L and transmission lines $TL2$ and $TL3$ can be written as

$$Y_G = G_L + jB, \quad (11)$$

where B is

$$B = \sqrt{\frac{|\Gamma_E|^2 \cdot (Y_{TL1} + G_L)^2 - (Y_{TL1} - G_L)^2}{1 - |\Gamma_E|^2}} \quad (12)$$

Because the load resistance is real, the imaginary part of Y_G has to comprise both transmission lines $TL2$ and $TL3$. With the already chosen parameter Z_{TL2}, Z_{TL3} can be obtained with

$$Z_{TL3} = \frac{1}{B - \frac{1}{Z_{TL2}}} \cdot \tan(30\,\text{deg}). \quad (13)$$

With Γ_E being the reflection factor at the transistor output terminals

$$\Gamma_E = \frac{Z_E - Z_{TL1}}{Z_E + Z_{TL1}} \quad (14)$$

and Γ_G the reflection factor at the end of transmission line TL_1

$$\Gamma_G = \frac{\frac{1}{Y_G} - Z_{TL1}}{\frac{1}{Y_G} + Z_{TL1}} \quad (15)$$

the electrical length of Z_{TL1} can be calculated with

$$\frac{l_{TL1}}{\lambda} = \frac{\ln\left(\frac{\Gamma_E}{\Gamma_G}\right)}{-j4\pi}. \quad (16)$$

Because this implementation only provides a high impedance at the second and third harmonics across the transistor output terminals, output current and voltage waveforms are not completely separated resulting in less than 100 % maximum efficiency. Hence the transmissionline circuit should only be used for applications where it is not possible to use

lumped elements, or the insertion losses are greater than the efficiency restraints due to harmonic termination problems.

2.1 Input network

To meet the demands that Class E imposes on the used transistor for this project a GaAS HEMT transistor of type CREE CGH4010F is chosen. This transistor allows for a maximum collector voltage of 120 V . The input impedance for this transistor is $4-j\,4\,\Omega$ at 2.4 GHz which needs to be adapted to the 50 Ω output of the pre-amplifier. While this can be easily be achieved using a $\lambda/4$ transmission line limiting bandwidth, a binomial input filter is chosen. The main advantage of using a binomial matching transformer is that the passband response is maximally flat near the design frequency. The order N also determines the number of sections in the transformer [7].

2.2 Simulation and Measurement Results

In this section, the Class E amplifier structure is modeled and simulated in the Agilent Advanced Design System (ADS). Then simulation results are compared to measurement of the implemented amplifier. The Cree CGH4010F GaN HEMT has an output capacitance C_{GS} of typically 1.3 pF [6]. Using Eqs. (10) and (9) the required load impedance Z_E can be calculated. Further following the advice of [3] a medium to high characteristic impedance has been chosen for $TL_1 = 75\ \Omega$ and $TL_2 = 50\ \Omega$. Further parameters can easily be attained using equations presented in Section 2.

First, the circuit output network is simulated using two real ports, to review the location of the second and third harmonic in a Smith chart. As already mentioned, the output network should impose a 40.5 deg phase shift on the transistor output terminals for the target frequency and impose a high impedance at the second and third harmonic. Fig. 4 shows the frequency response of the output network as seen by the transistor output terminals.

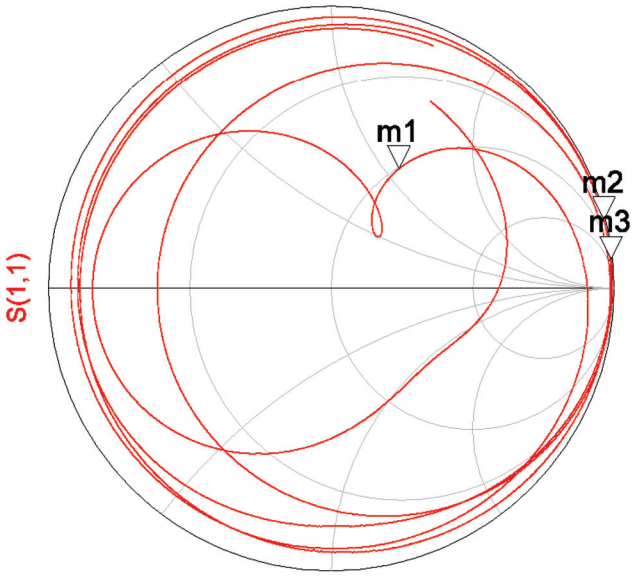

Fig. 4: Smithchart of the output load network

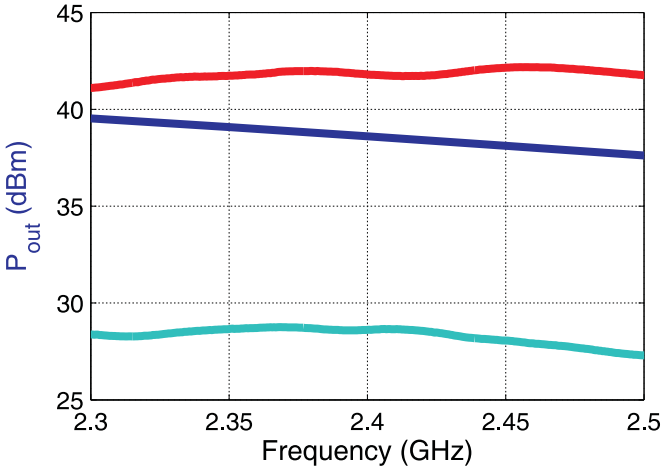

Fig. 5: Frequency response of the measured and simulated amplifier, and pre-amplifier using a 20 V DC supply voltage

Fig. 5 shows the frequency response of the amplifier. In red the measurement, and in blue the simulated values. Remarkable for this amplifier is that the measurement results are well above the simulation results. In addition, the real amplifier performs best with 28 dBm input power, while the simulation is carried out with 30 dBm input power. These differences can be explained given that the simulation model of the transistor is optimized for Class AB operation. The output frequency response of the pre-amplifier is shown in turquoise.

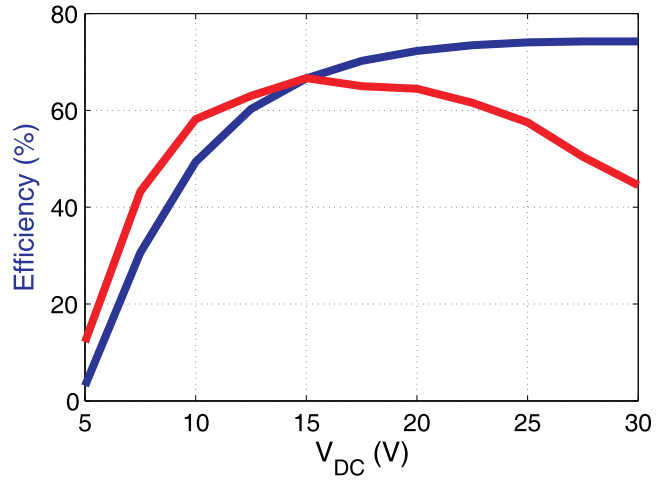

Fig. 6: Power added efficiency

Fig. 6 shows the resulting amplifier efficiency.

Fig. 7 shows that the two amplifiers, Yellow and Blue, are put together on a single circuit board for implementation in

the CLIER system. In the following figures the two amplifiers can be compared.

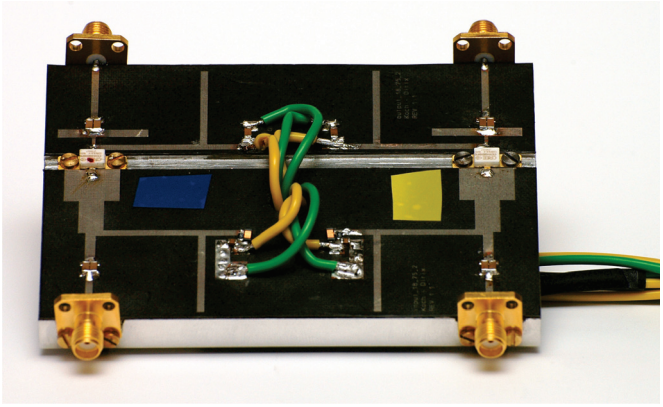

Fig. 7: The two Linc Class E amplifiers on a circuitboard

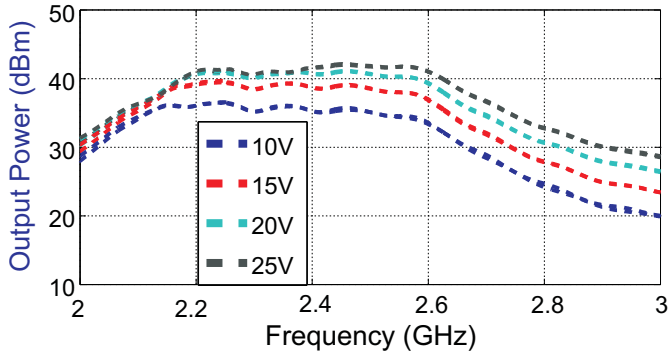

Fig. 8: Frequency response of the blue and the yellow amplifier with 10, 15, 20 and 25 V supply voltage, DC supply

Figs. 8 and 9 show that the differences between the two amplifiers are small. This makes them ideally suited for further implementation in the LINC part of the CLIER amplifier architecture, as a LINC transmitter requirers a small phase and amplitude imbalance between the two paths. Figure 10 depicts the linearity between the DC supply voltage and the output voltage. As can be seen good linearity is delivered up to 20 V DC. The non-linearity in the higher voltage range must be compensated using pre-distorting or with the LINC part of the architecture.

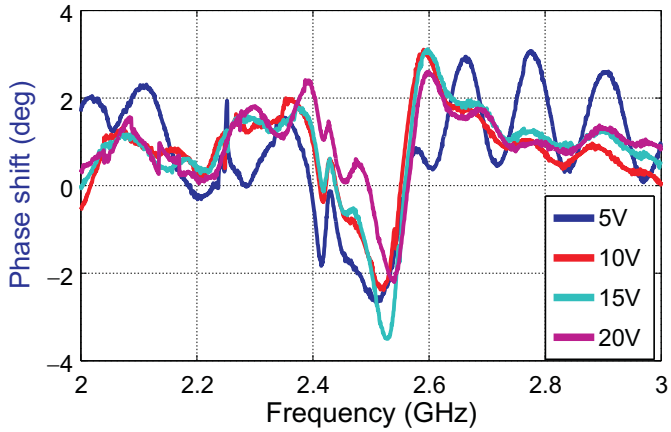

Fig. 9: Phase difference of the two ouput signals B21-Y21

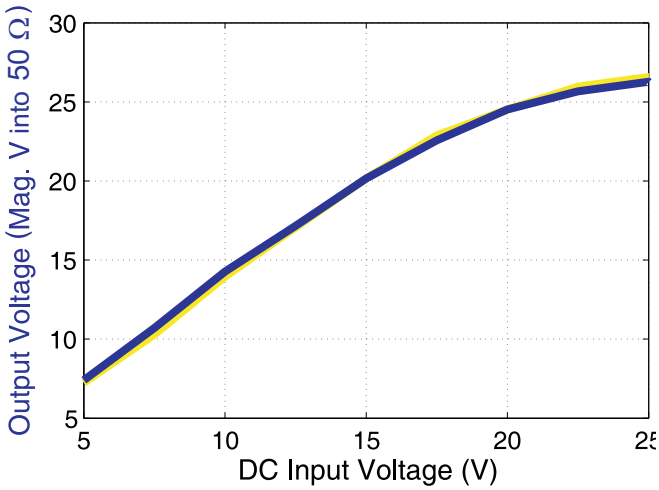

Fig. 10: Comparison of the output voltage of the yellow (light) and the blue (dark) amplifier

3 Conclusion

A Class E Power Amplifier has been presented and its efficiency simulated and measured. Its suitability for a CLIER transmitter has been demonstrated.

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