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All-Optical Sigma-Delta Modulator for Analog-to-Digital Conversion

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All-Optical Sigma-Delta Modulator for Analog-to-Digital Conversion

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ABSTRACT

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In this thesis, an all-optical sigma-delta (ΣΔ) modulator for analog-to-digital conversion (ADC) using a novel optical bistable switch, the SOA-PD device, is demonstrated. The presented all-optical ΣΔ modulator consists of a photonic leaky integrator, the SOA-PD optical comparator, and a positive feedback loop. The switching properties of the SOA-PD device are studied and experimentally tested to confirm its performance. Then the all-optical ΣΔ modulator is designed according to the switching performance of the SOA-PD device. It is demonstrated that the all-optical ΣΔ modulator is capable of producing an inverted non-return-to-zero (NRZ) type binary output for frequencies in the range of dozens of kilohertz. The limit cycle frequency of the ADC system is about 250 kHz, which is limited by the maximum switching speed of the SOA-PD device. Through noise analysis of the system, SNR and ENOB of the system are calculated to be 25.3 dB and 3.93 bits respectively.

ACKNOWLEDGEMENTS

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1. INTRODUCTION

For decades, the analog-to-digital (A/D) conversion has always been a critical technology in the electronic industry for its broad applications from daily consumer electronics to military radars and aerospace satellites. Electronic A/D converters have experienced fast evolution since 1970s. However, they still lag behind the development of digital electronics that process, store and transmit digital signals at much higher speed. The limited performance of traditional electronic A/D converters is mainly due to quantization accuracy, timing accuracy, and the sampling rate which ultimately govern the conversion speed and resolution [1]. More recently, optical and photonic technologies are investigated to improve the performance of A/D converters for their advantages of high speed, high resolution and immunity of electromagnetic interference over the electronic counterparts.

This thesis presents an all-optical A/D converter based on sigma-delta (ΣΔ, or delta-sigma, ΔΣ) modulation, implemented with photonic leaky integrator and an optical bistable comparator. The first chapter covers an introduction to A/D conversion, ΣΔ modulation and the research motivation. Chapter 2 provides a mathematical description of the proposed all-optical ΣΔ modulator followed by the simulations. Chapter 3 focuses on optical bistable switches, especially, on SOA-BJT device and SOA-PD device. Since the significance of this research is to demonstrate all-optical ΣΔ modulation with a novel optical quantizer, SOA-PD device, design and testing of this device takes a considerable part of this chapter. Another important component of the system, optical leaky integrator, is demonstrated in Chapter 4. The design of the ΣΔ modulator is covered in Chapter 5, followed by the experimental results. To confirm A/D

conversion, the binary output of the system is demodulated through a Matlab-based program and the input signal is reconstructed. In Chapter 6, a noise model of the open-loop system (feedback loop is disconnected from summing junction) is built and simulated in order to characterize the significant performance of the system. Finally, conclusion and recommendations for future work are highlighted in Chapter 7.

1.1 Introduction to A/D Conversion

Analog-to-digital conversion is the process which converts a continuous-time, continuous-amplitude signal into a discrete-time, discrete-amplitude signal –digital signal. This conversion process can be generally described by four distinct functions shown in Figure 1.1.

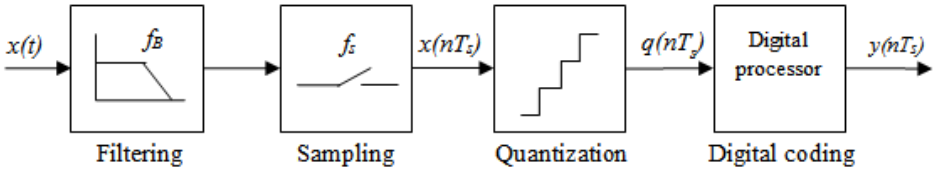

Figure 1.1 Generalized Block Diagram of A/D Converter

The operation of this generic A/D converter can be described by following a signal as it progresses through each element shown in Figure 1.1. The analog signal *x(t)* is first bandlimited to the range $0 \leq f_x \leq f_B$ (Hz) by an analog filter to ensure protection against aliasing that could occur during the subsequent sampling operation. Then a proper sampling operation is chosen to satisfy the minimum Nyquist criterion: $fs = f_N = 2f_B$, where *fs* is the sampling frequency, f_N is the Nyquist frequency, and f_B is the constrained signal bandwidth after the filtering operation. There are also other sampling schemes depending on the specific applications, such as subsampling ($fs << f_N$) and oversampling ($fs >> f_N$). Quantization is the next step in the analog-to-digital

conversion. There are several different quantization approaches which are typically associated with the quantization step size. Amongst them, uniform quantization is the most preferred and used technique in industry for its optimal performance in high-rate applications. A uniform quantizer accomplishes the quantization process using 2^N equal quantization steps to achieve N-bits of resolution. Other types of quantizers attempt to modify the step size as a function of signal information such as pulse width [2]. The last operation of analog-to-digital conversion is digital coding. A/D converters generally use an internal coding scheme which supports the specific quantization approach, enables fast look-up for output coding, or helps to ensure data integrity. Three common types of internal coding schemes in use today are the thermometer code, Gray code, and the circular code [3].

1.2 ΣΔ A/D Converter

ΣΔ A/D converters are A/D converters utilizing sigma-delta technique which sums (Σ) the difference (Δ) between the input signal and system feedback to improve the resolution of the system. A simple block diagram of a typical electronic first-order ΣΔ A/D converter can be described with two primary internal cells: the ΣΔ modulator and the digital/decimation filter (as shown in Figure 1.2). The internal ΣΔ modulator coarsely samples the input signal at a very high rate into a 1-bit stream. The digital/decimation filter then takes this sampled data and converts it into a high-resolution, slower digital code. While most converters have one sampling rate, the ΣΔ converter has two—the input sampling rate (f_S) and the output data rate (f_D). ΣΔ A/D converters are largely used for analog-to-digital conversion in high-fidelity audio and communication equipment.

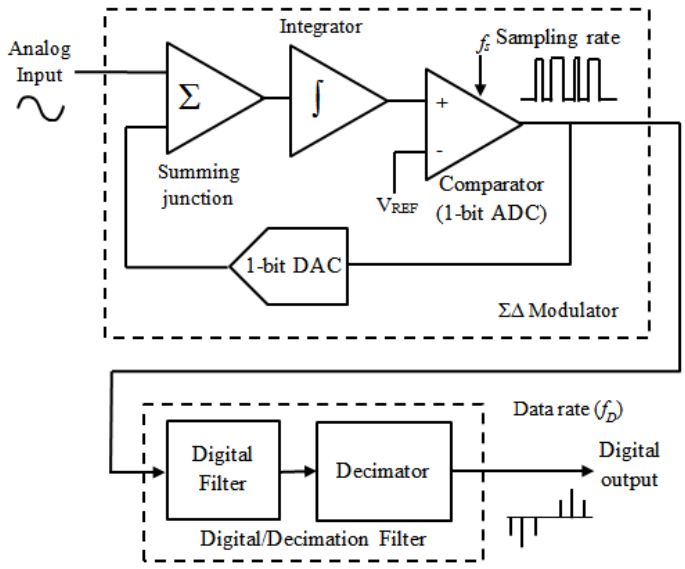

Figure 1.2 Block Diagram of 1st Order ΣΔ A/D Converter

1.2.1 Sigma-Delta Modulator

The ΣΔ modulator is the heart of the ΣΔ A/D converter. It is responsible for encoding analog signals into binary signals or higher-resolution digital signals into lower-resolution digital signals. The conversion is accomplished by using error feedback, where the difference between the input and output is measured and used to improve conversion. The converter generates an output that can be easily reconstructed to the input signal by applying low-pass filtering. The ΣΔ modulator shown in Figure 1.2 contains a summing junction, an integrator, and a one-bit comparator. The input signal comes into the modulator via a summing junction. It then passes through the integrator which feeds a comparator that acts as a one-bit analog-to-digital converter (ADC). The comparator output is fed back to the input summing junction via a one-bit digital-to-analog converter (DAC), and it also sent to the digital/decimation filter and emerges at the output of the converter.

The ΣΔ modulator (encoder) acquires many samples of the input signal to produce a stream of 1-bit codes. The system clock implements the sampling speed, f_S, in conjunction with the modulator's one-bit comparator. In this manner, the quantizing action of the ΣΔ modulator is produced at a high sample rate that is equal to that of the system clock. ΣΔ modulation converts the analog signal into a pulse frequency and is alternatively known as Pulse Density Modulation (PDM) or Pulse Frequency Modulation (PFM). This output is a pulse stream in which the frequency of pulses in the stream is proportional to the analog voltage input. Typical signals through a ΣΔ modulator are shown in Figure 1.3. If the input signal is a sine wave, on which the output signal is subtracted to form the error signal. This error is integrated, and when the integral of the error exceeds the limits, the output changes state. As observed, when sinusoidal input is near its maximum, the duty cycle of the output signal approaches 100% and the output stays positive most of the time. Similarly, when the input signal is at its minimum value, the duty cycle of the output signal is close to 0% and the output is predominately negative. As the input signal transits between the maximum and minimum values, the output signal has an approximate 50% duty cycle.

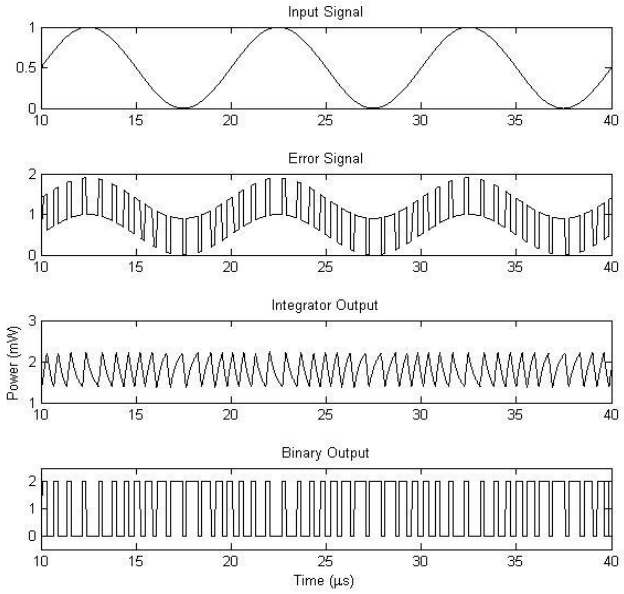

Figure 1.3 Input Signal, Error Signal, Integrator Output and Binary Output of a ΣΔ Modulator.

The biggest merit of ΣΔ modulators is that it reduces noise at lower frequencies. In this stage, the combination of the integrator (noise shaping filter) and oversampling strategy implements a function called noise shaping that pushes low-frequency noise up to higher frequencies where it is outside the band of interest. Noise shaping is one of the reasons that ΣΔ converters are well suited for low-frequency, high accuracy measurements. Figure 1.4 shows the input signal and the quantization noise for a first-order ΣΔ modulator. The input signal appears as a spur in the spectrum of the digital output, while the quantization noise starts low at zero hertz, rises rapidly, and then levels off at a maximum value at the modulator's sampling frequency (f_S).

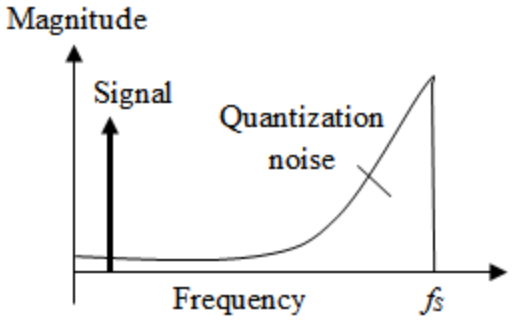

Figure 1.4 Spectrum of Binary Output of ΣΔ Modulator

1.2.2 Digital Filtering and Decimation

Once the signal resides in the digital domain, a low-pass digital filter can be used to attenuate the high-frequency noise, and a decimator can be used to slow down the output-data rate. Here, the two components are described independently, however, real-world designs intertwine them in the same chip.

The digital filter is functioning as a low-pass filter by first sampling the modulator stream of the 1-bit code. The output rate of a digital filter is the same as the sampling rate. In the time domain, the digital filter is responsible for the high resolution of the ΣΔ converter. However, in the frequency domain, the digital filter applies only a low-pass filter to the signal. In doing so, it attenuates the modulator's quantization noise; but it also reduces the frequency bandwidth, as any good low-pass filter will.

The second function of the digital/decimation filter is the decimator. The word "decimate" was originally used by the Roman army to mean the killing of every tenth man of a group that was guilty of mutiny. In the case of the digital/decimation filter, the digital signal's output rate is reduced by throwing away or "killing" portions of the output data. The way to do this is to discard some of the samples. This may seem a bit distressing. In fact, according to the Nyquist

theorem, the decimated signal has exactly the same informational content as the previous waveform, but now at a much more manageable data rate.

1.3 Motivation

The A/D converter is a key element in any electronic or photonic system which senses the natural environment and processes, stores, or displays the information using digital representation or processing. Since the vast majority of signals in nature are analog and the preferred method of processing, storing, and transmitting signals is digital, this interface is critical to the success of the overall system. A/D converters are ubiquitous, being used in a wide variety of applications such as consumer electronics, high-fidelity audio system, precision instrumentation, military radar and aerospace communication satellites [4].

The use of photonic component to make or improve an analog-to-digital converter has attracted interests since 1970s. During this period, laser and optical components have improved and matured remarkably, but photonics is still not used in any commercial or special purpose analog-to-digital converters. Not until 2005, the scheme of all-optical ΣΔ A/D converter was first proposed by M. Sayeh and A. Siahmakoun [5]. The latest work demonstrated a photonic asynchronous ΣΔ modulator operating at several megahertz [6]. However, the system is the implemented an electronic comparator which inherently limits the optimum performance because of the existence of electrical-to-optical conversions in the system.

Optics has many attractive features for switching and signal processing applications. It has the potential to solve many of the communications problems within the existent processing machines. A good example of optical switching device is the quantum-well self-electro-optic effect device (SEED), whose concept was first proposed by D. Miller in 1990s. [7] It uses the

very strong electro-absorptive effects in quantum-confined system to achieve nonlinear-optical applications such optical bistable switching. This technology is very promising in the application of all-optical A/D converters, since it provides a possibility of high-speed optical quantization. More recently, two derivations of the SEED are demonstrated by utilizing commercialized semiconductor optical amplifier (SOA) and bipolar junction transistors (BJTs) [8, 9]. This discovery greatly expedites the exploration in all-optical A/D converters. This research will start with the study of optical switching properties in SOA-BJT and SOA-PD devices for all-optical A/D conversion, then move to the architecture of an optical ΣΔ A/D converter. At last, a noise analyzing model will be developed and the conversion performance, such as dynamic range (SNR) and resolution (ENOB), will be evaluated in comparison with the experimental results.

2. THEORY

2.1 Overview of All-Optical ΣΔ Modulator

The generic architecture of all-optical ΣΔ modulator can be described as a first-order ΣΔ modulator as shown in Figure 2.1. It contains a summing junction, a leaky integrator and a bistable quantizer connected by optical fibers. The summing junction is the simplest component in the system. As a real example, it can be an optical coupler which serves to add the feedback signals into the input signals. The leaky integrator is a linear system whose function is accumulating input signals while leaking out a certain amount of output signals at the same time. Unlike traditional electronic quantizer, the bistable quantizer, in this case, is an optical switching device which generates on-level outputs when the inputs vary from the minimum to maximum, and off-level outputs when the inputs vary from the maximum to minimum. A detailed description of the operating principles of the leaky integrator and the bistable quantizer are presented in Chapter 4 and Chapter 5 respectively.

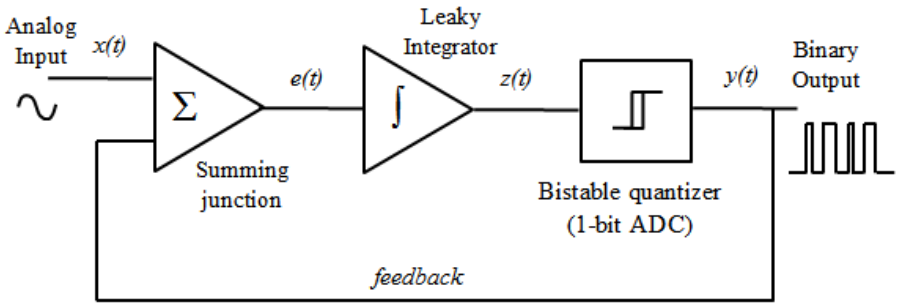

Figure 2.1 First-Order ΣΔ Modulator

The operation of the system can be described in three steps. First, the input signal *x(t)* adds to the output of the modulator, *y(t)*, generating an error signal *e(t)*. Then this error signal enters into the integrator which basically works as a low-pass filter. Finally, the output of the integrator *z(t)* is sent into the bistable quantizer which generates the binary output, *y(t)*. To better understand the operation conditions and find out the power boundaries of the optical signals, a mathematical model of the all-optical ΣΔ modulator is established and examined by Matlab-based simulations in the next two sections.

2.2 Mathematical Model of All-Optical ΣΔ Modulator

The mathematical modeling of the all-optical ΣΔ modulator is based on the work ‘‘Asynchronous first-order fiber-optic delta-sigma modulator’’ by E. Reeves and P. Costanzo-Caso [6]. The conceptual model of the all-optical ΣΔ modulator contains a summing junction, a leaky integrator, a bistable quantizer and a feedback loop as shown in Figure 2.2 (a). Before the conduction of any mathematics, several assumptions must be stated in advanced: the first is the leaky integrator is a linear system whose transfer function is given by $H(\omega)=g/(j\omega+1/\tau)$ where g and τ are constant [5], and the second is the bistable quantizer has ON-level outputs when input is greater than the threshold and OFF-level output when input is smaller than the threshold. Those two assumptions are made at the best approximation of the two devices, and it can be demonstrated in the later text that the theoretical model based on the two assumptions agrees with the experimental results.

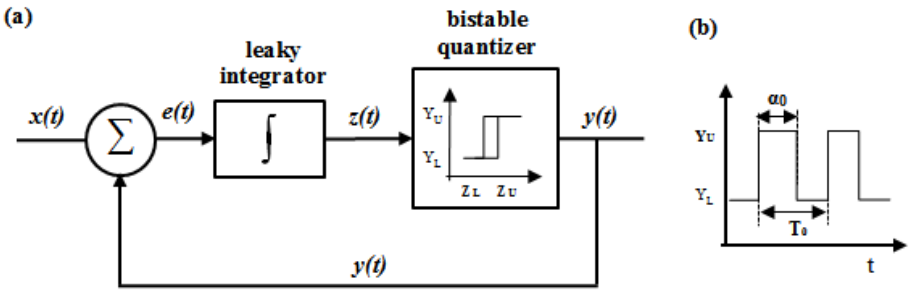

Figure 2.2 Diagram of (a) All-Optical ΣΔ Modulator. (b) Output Waveform

Let's first consider the output of the modulator, *y(t)*. The output of the modulator is an inverted non-return-to-zero (NRZ) pulse stream whose duty cycle contains information of the input signal. The duty cycle, *D*, is defined as $D=\alpha_0/T_0$, where α_0 is the pulse width and T_0 is the period [see Figure2.2 (b)]. The output of the modulator is written as

$$y(t) = Y_M + \Delta Y sgn[z(t) - Z_M] \tag{2.1}$$

where ΔY is the amplitude of output signal, $\Delta Y = (Y_U - Y_L)/2$, and *sgn ( )* is the sign function. The subscripts *U, L, M* denote the upper, lower and mean value of signals. The positive sign '+' in Equation (2.1) indicates that the output of the bistable quantizer, *y(t)*, 'tracks' the output of the leaky integrator. That is to say *y(t)* will be Y_U when the integrator output $z(t) > Z_M$, and Y_L when $z(t) < Z_M$.

If a constant input signal, $x(t)=X$, is sent into the system, the integrator output *z(t)* is described as

$$\begin{aligned} z(t) &= \{x(t) + y(t)\} * h(t) \\ &= \{X + Y_M + \Delta Y sgn[z(t) - Z_M]\} * h(t) \end{aligned} \tag{2.2}$$

where *h(t)* is the impulse response of the leaky integrator and '*' denotes the convolution operation. In order to better understand the integrator output *z(t)*, we can expand the second term of *y(t)* as a Fourier series

$$\Delta Y sgn[z(t) - Z_M] = \frac{a_0}{2} + \sum_{n=-\infty}^{\infty}[a_n \cos(n\omega t) + b_n \sin(n\omega\, t)] \quad (2.3)$$

where ω is the frequency of output signal and equals to $2\pi/T_0$. T_0 is the period of one sample of $y(t)$. Solving the Fourier coefficients a and b over period T_0 and substituting the Fourier coefficients into $y(t)$, we derive

$$y(t) = Y_M + \frac{\Delta Y}{2}(2D - 1) + \frac{2\Delta Y}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\sin(n\pi D)\cos\left(\frac{2n\pi t}{T_0}\right)\right] \quad (2.4)$$

Then we find the integrator output to be

$$z(t) = \left\{X + Y_M + \frac{\Delta Y}{2}(2D - 1) + \frac{2\Delta Y}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\sin(n\pi D)\cos\left(\frac{2n\pi t}{T_0}\right)\right]\right\} * h(t)$$

$$= \left\{X + Y_M + \frac{\Delta Y}{2}(2D - 1)\right\}H(0) + \frac{\Delta Y}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\sin(n\pi D)\left(e^{\frac{j2\pi nt}{T_0}}H\left(\frac{n}{T_0}\right) + e^{-\frac{j2\pi nt}{T_0}}H\left(-\frac{n}{T_0}\right)\right)\right] \quad (2.5)$$

Details of solving for Fourier coefficients and convolution operation can be found in [10]. If only three significant duty cycles are considered, *D=0%, 50%, 100%,* then it can be seen that the second term in Equation (2.5) equals to zero, resulting a simple solution for $z(t)$,

$$Z = \left\{X + Y_M + \frac{\Delta Y}{2}(2D - 1)\right\} g\tau \quad (2.6)$$

The operating conditions of the all-optical ΣΔ modulator can be found by analyzing integrator output when the duty cycle is 0%, 50%, and 100%. Even though the input signal is constant, a high input results with a 0% duty cycle, a moderate input with 50% duty cycle, and low input with 100% duty cycle. Since the output of the integrator is inverted from the input signal, $z(t)$ is Z_U when $x(t)=X_L$ while $z(t)$ is Z_L when $x(t)=X_U$. Summarize above we derive,

$$D = 0 \xrightarrow{yields} Z_L = \left\{X_U + Y_M - \frac{\Delta Y}{2}\right\} g\tau \quad (2.7\text{ a})$$

$$D = 0.5 \xrightarrow{yields} Z_M = \{X_M + Y_M\} g\tau \quad (2.7\text{ b})$$

$$D = 1 \xrightarrow{yields} Z_U = \left\{X_L + Y_M + \frac{\Delta Y}{2}\right\} g\tau \quad (2.7\text{ c})$$

Equation (2.7a) to (2.7c) are used to determine the mean value and contrast of the integrator output and provide boundaries for the operation of the bistable quantizer. Because the quantizer window size must be smaller than the contrast of the integrator output, this boundary condition is derived by subtracting (2.7 a) from (2.7 c).

$$|\Delta Z| < |\{\Delta X + \Delta Y\} g\tau| \qquad (2.8)$$

where $|\Delta Z|$ stands for the quantizer window size (see Figure 2.2 a), and $|\{\Delta X + \Delta Y\} g\tau|$ is the contrast of integrator output. This is the most important requirement to ensure successful optical ΣΔ A/D conversion. It will be demonstrated later that the quantizer window size is the main limitation to the maximum operating frequency of the all-optical ΣΔ modulator, since the window of the optical quantizer is frequency dependent.

Equation (2.7 b) illustrates another operating condition of the all-optical ΣΔ modulator. It states that the mean value of integrator output has to be equal to the center of the quantizer window. In this case, this condition can be achieved by adjusting the optical quantizer threshold.

2.3 Simulation of All-Optical ΣΔ Modulator

The summarized simulation is based on the relations between *x(t), y(t)* and *z(t),* derived in the previous section. In this thesis, we adopted a Matlab-based simulation, which is based only on the conceptual model without considering the noise in the actual system. Consider a sinusoidal input signal with amplitude 0.5 mW and offset 0.5 mW at frequency 100 kHz, and the ON- and OFF-level outputs of the bistable quantizer are 2.0mW and 0 mW respectively. Let's also assume that the gain and the time constant of the integrator are: $g=3$ and $\tau=0.4$. By applying equation (2.7 b) and (2.8), we can derive the system requirements:

$$Z_M = \{X_M + Y_M\}g\tau = 1.8mW$$

$$|\Delta Z| < |\{\Delta X + \Delta Y\}g\tau| = 3.6mW$$

where *1.8 mW* is the mean value of integrator output and *3.6 mW* is the contrast of integrator output.

In order to investigate the impact of quantizer window size *(|ΔZ|)* on the binary output, *y(t),* the quantizer window size will be manually chosen as 0.6 mW, 1.2 mW and 3.4 mW with a center of 1.8 mW, such that different binary outputs can be compared. In addition, a 3rd order low-pass Butterworth filter with cutoff frequency ω_c= 120kHz is used to demodulate the binary outputs and compare the reconstructed signals, *x'(t),* with the input signals, *x(t),* to demonstrated the performance of the modulator. Moreover, the waveforms of the error signal, *e(t),* and the integrator output, *z(t),* are given by the simulation program for better understanding the operation of the all-optical ΣΔ modulator.

Figure 2.3 to 2.5 illustrate simulation results when the quantizer window size |*ΔZ*| equals 0.6 mW , 1.2 mW and 3.4 mW. One conclusion we can draw from the simulation results is that the density of the binary pulses decreases as the quantizer window size is increased. This principle is essential in controlling the sampling rate of the all-optical ΣΔ modulator. In other word, a small quantizer window size gives out a high sampling rate, while a relatively larger quantizer size degrades the sampling rate. Since the sampling rate determines the maximum operating speed of the A/D conversion, the quantizer window size is a critical factor in the design of the all-optical ΣΔ modulator.

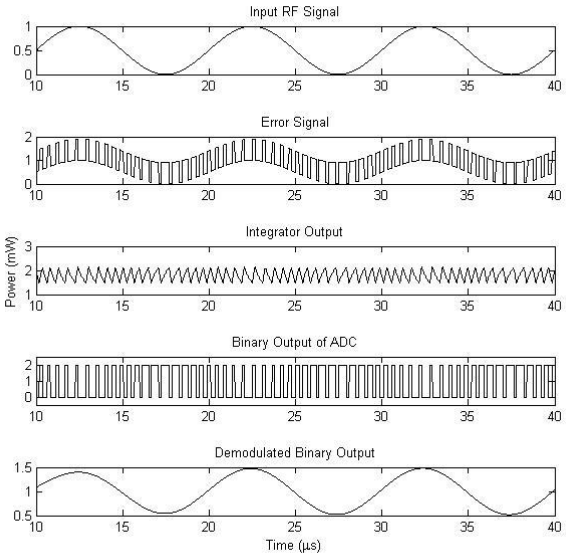

Figure 2.3 Simulation Signals of All-Optical ΣΔ Modulator When |ΔZ|=0.6 mW.

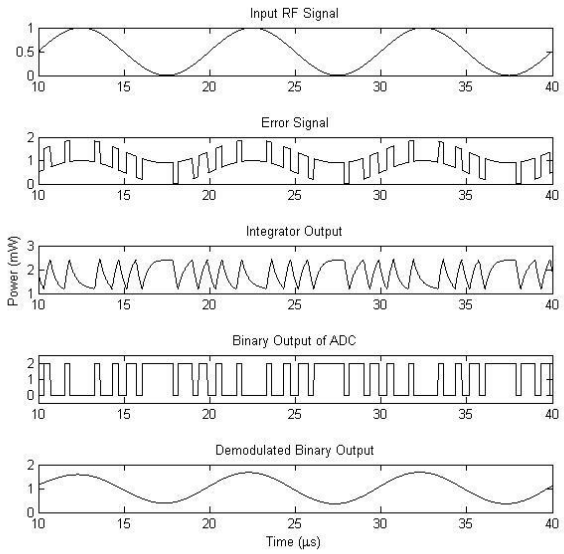

Figure 2.4 Simulation Signals of All-Optical ΣΔ Modulator When |ΔZ|=1.2 mW.

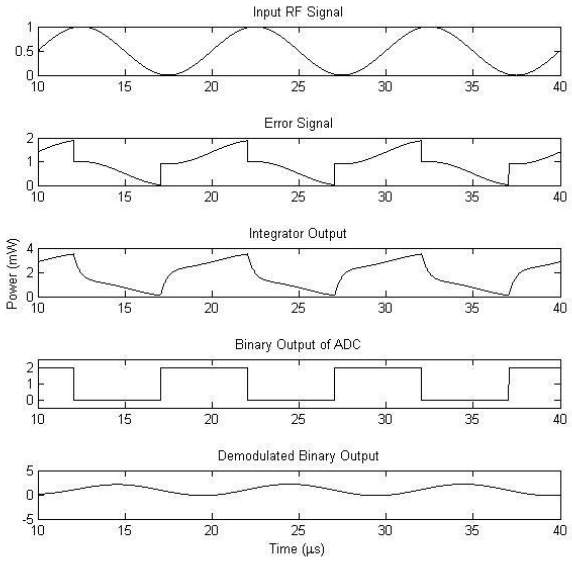

Figure 2.5 Simulation Signals of All-Optical ΣΔ Modulator When $|\Delta Z|$=3.4 mW.

3. OPITCAL BISTABLE SWITCHES

3.1 Introduction to Optical Bistability

Optical bistability is an attribute of certain optical devices in which two output states occur for the same input intensity over a given range of input values [11]. The two output states associated with the high and low transmitting levels (ON-level and OFF-level) appear when the input rapidly transits from maximum to minimum and vice versa. As a result, the optical bistable device has a transmittance curve as Figure 3.1.

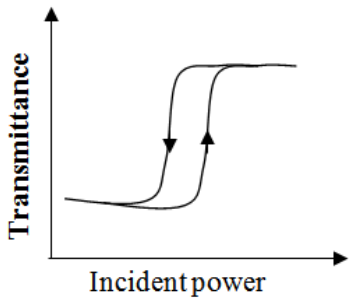

Figure 3.1 Hysteresis Curve of Optical Bistable Device

Optical bistable devices attract considerable attention in recent years due to their broad applications in wavelength conversion, optical storage, optical switches, routers, optical neural networks and optical logic circuits. There are several approaches to generate optical bistability involving nonlinear systems and feedback mechanisms. Reported optical bistable devices associated with nonlinear effects such as cross-gain modulation (XGM) and cross-phase modulation (XPM) are commonly seen in semiconductor optical amplifiers (SOA) [12, 13], erbium doped fiber amplifiers (EDFA) [14], saturable absorbers [15, 16, 17] and quantum well self electro-optic effect devices (SEEDs) [18, 19]. Because of compactness and integration possibility of SOAs and SEEDs, they are good candidates to be used in design of bistable

switching elements on optical integrated circuits. The optical feedback, which leads to field enhancement, can be provided by lumped or distributed optical resonators such as Fabry-Perot (PF) cavities [15], fiber Bragg grating (FBG) resonators [20], and photonic crystal (PhC) nanocavities [21]. Microcavities and nanocavities are possibly employed on the optical integrated circuits while FBG resonators can be exploited in the lumped bistable devices. Optical bistability in SEEDs has drawn great interest since the 1990s for its potential use in optical switching and computing. This device is composed of a p-i-n diode which is a multiple quantum-well (MQW) structure within its intrinsic region. When the diode is reverse-biased, the quantum-confined Stark effect (QCSE) causes the absorption coefficient (or transmission) to change nonlinearly with the voltage across the MQW. Consequently, a bistable behavior is observed as a result of the feedback mechanism introduced by the electrical circuit containing the SEED. The Symmetrical-SEED (S-SEED) [8], formed by connecting two SEEDs in series, leads to improved bistable characteristics. In this case, however, the switching point depends on the ratio of the input optical powers.

After the proposal of S-SEEDs, many variations on the S-SEEDs have been demonstrated. One example is the symmetric SOA device (S-SOAD). The S-SOAD exhibits both electrical and optical bistability on the basis of two opto-electric effects: electric bistability results from the connection of two p-i-n structures in series, and optical bistability is obtained from the QCSE in the WQW region of SOA. This effect results in the absorption coefficient changing with the voltage across the p-i-n region. The principal advantages of the S-SOAD are: availability of SOA; the simplicity of implementation, noninterferometric device and integration feasibility. Nevertheless, S-SOAD suffers from a large capacitance in SOAs which ultimately limits its switching speed. The fastest switching speed reported is 100 kHz [8].

In order to overcome the capacitance limitation of the S-SOAD, the SOA-BJT device and the SOA-PD device are proposed. These two devices will be discussed in details in the next two sections.

3.2 SOA-BJT Device

3.2.1 Operation Principles SOA-BJT Device

Bipolar junction transistor (BJT) is a type of transistor that is commonly used in the electric circuits to amplify and switch electronic signals and electric power. BJT consists of two types of semiconductor in contact and three terminals labeled as base, collector and emitter. A small current flowing between base and emitter can control or switch a much larger current between the collector and emitter terminals.

SOA-BJT device adopts the base-collector junction of BJT to replace one SOA in the S-SOAD device. The electrical circuit creates a bistable system which can be switched by controlling the optical input to the SOA. Furthermore, as the voltage across the SOA switches, the transmittance is modified by the QCSE as a result of the MQW structure within the SOA. In this case, the absorption spectrum of SOA shifts to longer wavelength as the voltage across it increases, resulting the transmittance (at 1550 nm) of SOA increases with an increasing voltage and vice versa.

Figure 3.2 (a) shows a schematic of the SOA-BJT device. The anode of the SOA is connected to the collector terminal of BJT, while a positive bias voltage V_1 is applied to the cathode of the SOA such that the SOA and the collector-base junction of the BJT are in reverse bias. The base-emitter junction of BJT along with a potentiometer is used to control the current of collector terminal which consequently adjusts the switching point of SOA-BJT device.

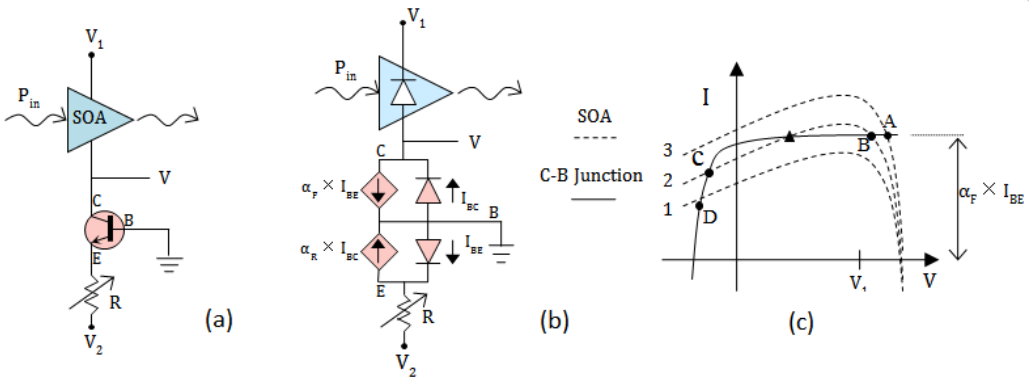

Figure 3.2 Schematic Diagram of (a) SOA-BJT Device (b) Equivalent Circuit Using the Ebers-Moll Model for the BJT (c) Load Lines of SOA and C-B Junction of BJT: Dashed Line 1 to 3 Shows the Load of PD as P_1 Increases.

The electrical bistability of this device is easier to understand by replacing the BJT with the Ebers-Moll model which approximates the operation of a BJT in active mode (shown in Figure 3.2(b)). The BJT is now acting as a reverse-biased diode (collector-base junction) with a current-controlled source (base-emitter junction along with the potentiometer and bias voltage V_2). The current through this source is equal to the current flowing through the base-emitter junction times the coefficient α_F. Since V_2 is negative, the base-emitter diode is forward biased and the current is controlled by adjusting the value of V_2 and the potentiometer.

Using this model, the load lines of both the collector-base junction and the SOA can be described in terms of V, the voltage between the two devices, as seen by Figure 3. 2(c). Since the two components are in series and share the same current, the device will operate at points where the load lines intersect. The load line for the collector-base junction (shown in solid line) is just that of a reverse biased diode, shifted up by the current $\alpha_F \times I_{BE}$. The load line of the SOA (dashed lines) has been added for several different optical input powers. The load line of the SOA is also similar to that of a reverse biased diode, shifted up by the photocurrent. Line 1 represents a low optical input, which is displaced to line 2 and line 3 as the optical input is increased. As the

voltage across the SOA increases (for V decreasing), the absorption of the SOA decreases and so the photocurrent also decreases. As a result of this drop off, the load line of collector-base junction and SOA's line 2 intersect at three different points. While the center intersection (triangle) is unstable, the left and right intersections are both stable. Therefore the point at which the device actually operates is determined by the direction in which the optical power is changing.

Starting with a low optical input as represented by line 1, the voltage (V) will be close to zero (point D). As the power is increased continuously, to line 2, the device will remain at a voltage close to zero (point C). As the power is further increased, the intersection point C will move to point B and eventually will disappear from the left side. At this power level the voltage will switch to a new value close to V_1 (point A). As the power decreases continuously back to line 2, the voltage will now remain close to V_1 at point B. The device is clearly bistable, with one operating point near zero (point C), and another near V_1 (point B). Additionally, it can be seen that the device switches at different optical inputs depending on whether the optical power is increasing or decreasing, meaning that the device exhibits hysteresis.

3.2.2 Simulation of SOA-BJT Device

In this section, a PSPICE simulation is developed to predict the performance of the SOA-BJT device. For modeling the SOA-BJT device, the equivalent circuit of SOA is modeled and the impedance of each component is computed using measurements from electrochemical impedance spectroscopy (EIS). The impedance analysis of SOA with EIS can be found in Appendix A.

Figure 3.3 shows the equivalent circuit of SOA-BJT device in PSPICE. The model for the SOA consists of a diode, a capacitor (500 pF), a parallel resistor (3.15 MΩ), and a serial resistor (75.5 Ω). The diode is used to simulate the p-i-n structure in the SOA. Upper bias (V_1=1.3V) and lower bias (V_2= -3V) are provided by two DC sources. Since PSPICE can only simulate electric circuits running voltage or current signals, the optical source in the simulation are substituted by a sinusoidal current source (f=300kHz, V_{amp}=3mV). This substitution is reasonable because the photo current is generated when optical signal is incident on the SOA.

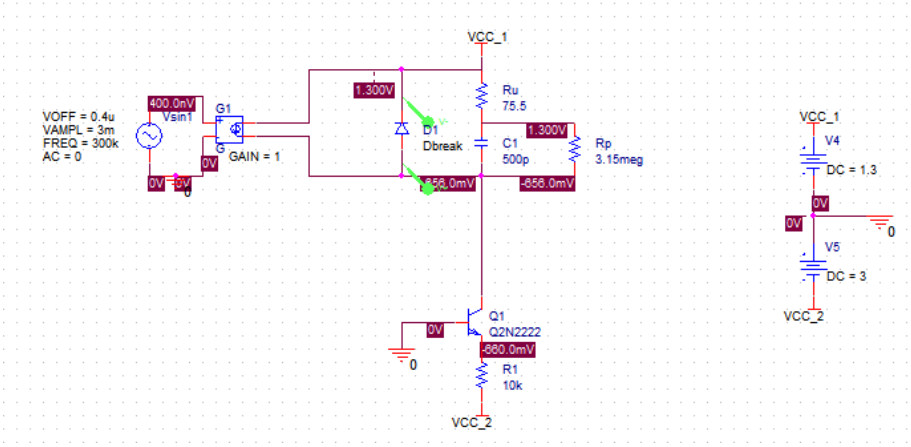

Figure 3.3 PSPICE Simulation Circuit of SOA-BJT Device

Since optical signals cannot be observed in the PSPICE simulation, only the voltage across SOA is observed. The voltage across SOA is defined as the potential drop from the anode to the cathode of SOA, and measured with two electric probes that one is connected to the anode of SOA and the other to its cathode. The voltage across SOA represents the optical output of SOA to some extent since the SOA transmittance vs. voltage can be experimentally determined.

Figure 3.4 shows the simulation results of SOA-BJT device. With a sinusoidal input signal into SOA, the voltage across SOA exhibits two states: one is at 0.6 V and the other is at -2.0V. The transition time between the two states is evaluated using the software: the voltage rise

time is 508.2 ns and fall time is 496.6 ns. Voltage across SOA vs. input signal is shown in Figure 3.4 (b).

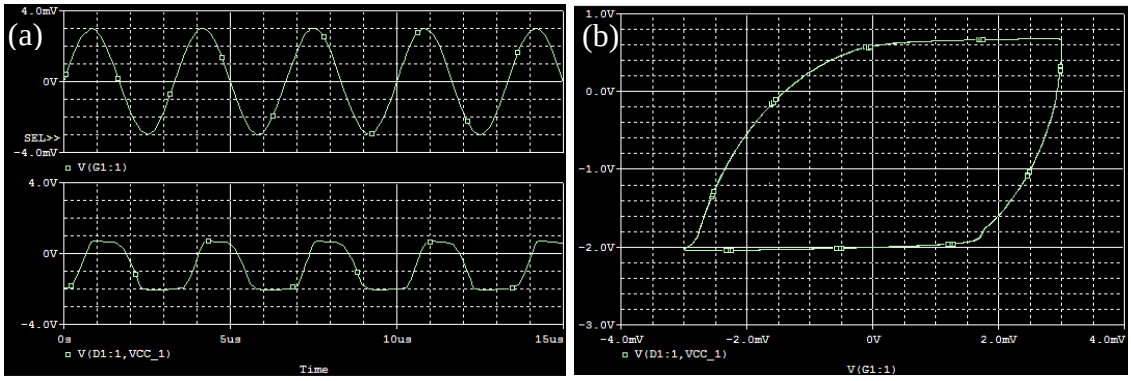

Figure 3.4 PSPICE Simulation Results: (a) the Input Signal (Upper Trance) and the Voltage across SOA (Lower Trace) at 300 kHz; (b) the Electric Bistability of SOA-BJT Device.

3.2.3 Experimental Demonstration of the SOA-BJT Device

The device shown in Figure 3.2 is constructed using a commercial SOA (Covega SOA-1117) and a standard BJT (model 2N2222A - NPN). Figure 3.5 shows the schematic diagram of the experimental setup. The bias V_1 is chosen to be 1.3 V according to the maximum reverse-bias of the Covega SOA. The control voltage V_2 is held at -3.0 V and a 5 KΩ potentiometer is used to control the current through the base-emitter diode, which in turn controls the switching threshold of the device. A DFB laser (Fujitsu FLD5F10NP) with integrated electro-absorption modulator (EAM) is used to produce a sinusoidal optical signal with an average power of 6 dBm. This signal is sent through the SOA and the output of the SOA is detected by a photo detector (EOT ET3500F) of 15 GHz bandwidth.

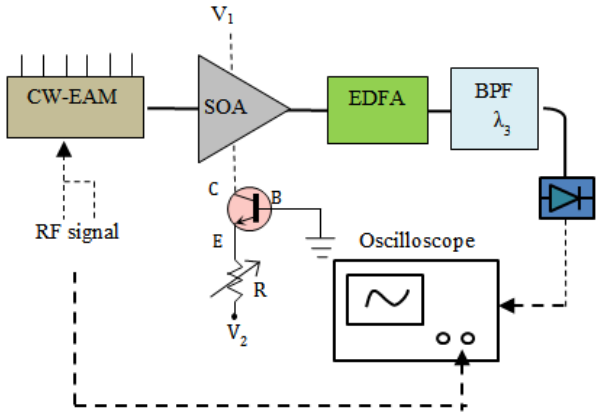

Figure 3.5 Schematic Diagram of Experimental Setup for SOA-BJT Device

In order to understand the optical bistability of SOA-BJT device, the behavior of the voltage across SOA in response to the input optical signal is first studied, and then compared with the transmittance curve of the SOA to predict its performance. The plot of voltage across SOA vs. input signal at 300 kHz is shown in Figure 3.6. This is also called the electrical bistability in which the two stable states occur at voltages of approximately 0.5 V and -2.0 V and the hysteresis behavior is clearly visible. The maximum switching frequency of the SOA-BJT device is at 300 kHz, which is mainly limited by the capacitances of the SOA (~500 pF) and BJT (~30 pF), and by the parasitic inductances of the components and cables involved in the circuit (about one meter long) [9].

As a result of QCSE, the transmittance of SOA changes with the voltage across it. This relation is depicted by Figure 3.7: over the voltage range of interest (between –2V and 0.5V), the transmittance of SOA decreases when the voltage varies from -2V to 0V and increases when the voltage varies from 0V to 0.5 V. The transmittance corresponding to the two voltage state, -2V and 0.5 V, is 0.022% and 0.016% respectively for an input power of 0.7 mW. Hence, for a

certain input power, the output power of the SOA is high when the voltage is -2V and low when the voltage is 0.5V.

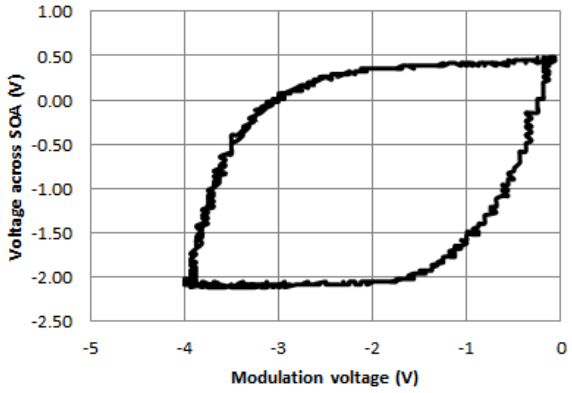

Figure 3.6 Bistability for the Voltage across the SOA

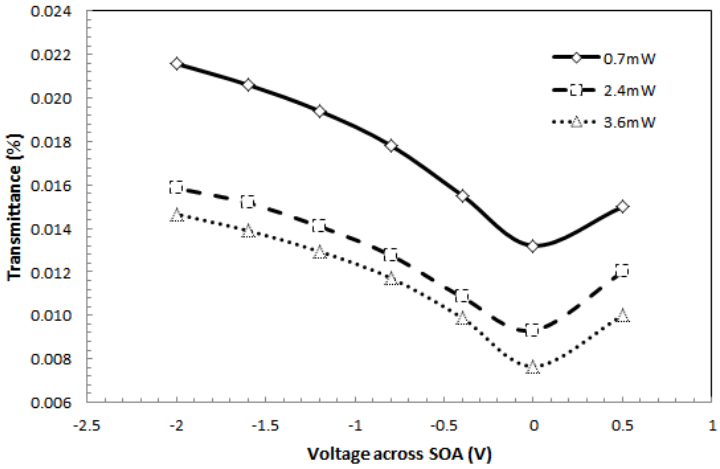

Figure 3.7 Transmittance of SOA vs. Voltage at Different Input Power.

For the SOA-BJT device, the quality of the binary optical output is greatly subject to the variation of the input signal. This impact on the optical output of the SOA-BJT device is depicted by Figure 3.8. Figure 3.8 (a) shows the voltage across SOA as a function of time, while Figure 3.8 (b)-(d) show the optical outputs generated by sinusoidal input optical signals at modulation voltage of 0.1V, 0.3V and 0.6V. Different modulation voltages correspond to different contrast of the optical input signals which share the same average power (about 0.7

mW). Because of the low contrast power of the input signal, binary optical outputs of the SOA-BJT device can only be observed under 1 kHz. What is more, the larger contrast of the optical input signal is, the worse binary output is generated after the SOA. This is due to the optical output of the SOA-BJT device is simply the product of the input signal and the transmittance of the SOA. As the contrast of the input signal increases [as shown in Figure 3.8 (b) to (d)], a clearer profile of the input sinusoidal is shown on top of the binary output signal. In other words, if the contrast of the input signal is too large, the binary output will be degraded by the wave form of the input signal.

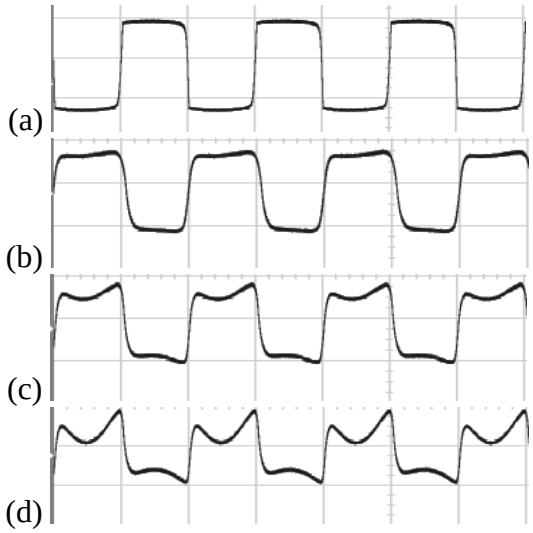

Figure 3.8 Voltage and Optical Signals: (a) Voltage across SOA as a Function of Time. (b), (c) and (d) Are Optical Outputs When Modulation Voltage to the Laser Are 0.1V, 0.3V and 0.6V.

This result leads to a dilemma where switching speed of the SOA-BJT device conflicts with the quality of the binary output. Because the switching speed of the SOA-BJT device is improved by increasing the contrast of the input signals, while the large-contrast input signals degrade the quality of the binary outputs. The best optical bistability observed in the SOA-BJT device is measured at 0.1V and 1 kHz modulation signal as shown in Figure 3.9.

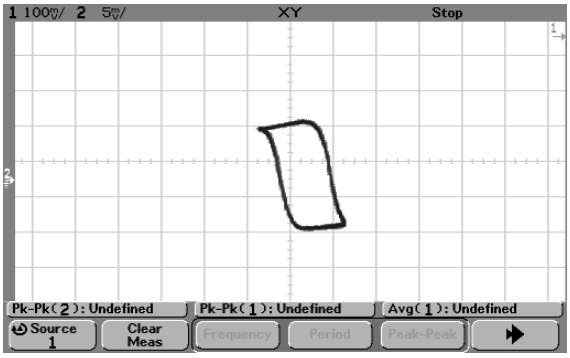

Figure 3.9 Bistability Is Exhibited for Optical Output of SOA-BJT Device at 1kHz.

3.3 SOA-PD Device

3.3.1 Operation Principles of SOA-PD Device

Another variation of S-SOAD is the SOA-PD device as shown in Figure 3.10 (a). The anode of the SOA (Covega SOA-1117) is connected to the cathode of the photo diode (PD, Eudyna FIX3Z1KX), while the cathode of SOA is grounded. Unlike the SOA-BJT device that uses a positive bias voltage at the cathode of SOA, the SOA-PD device adopts a negative bias voltage at anode of the PD. In doing so, the voltage across SOA can be monitored by an electrical probe at the connection of SOA and PD. The operation of SOA-PD device is very similar to that of SOA-BJT device: the electrical bistability is a result of the connection of two p-i-n structures in the SOA and PD, and optical bistability is a consequence of QCSE in MQW structure in the SOA. Figure 3.9 (b) shows the load lines of the SOA (solid line) and the PD (dashed line). The x-axis indicates the voltage across SOA while the y-axis represents the current shared by SOA and PD. The dashed line 1 indicates a small optical input power, P_1, is sent into the PD. At this moment, the voltage across SOA is close to zero (point A). As P_1 increases, the load line of PD shifts up from line 1 to line 2 to line 3, the intersection between the load lines of

SOA and PD moves from A to B to C. When the input power, P_1, decreases, the load line of PD moves down (from line 3 to line 2 to line 1), causing the intersection moves from C to D to A.

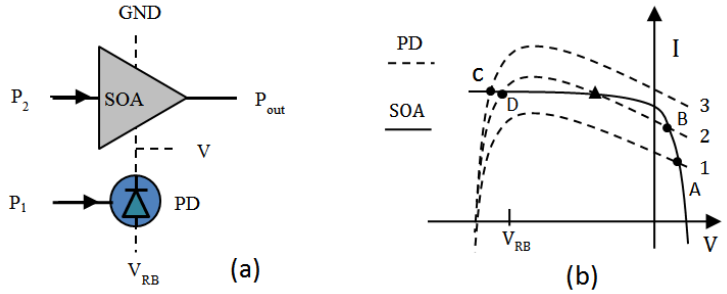

Figure 3.10 Schematic Diagram of (a) SOA-PD Device Comprising One SOA and One Photo Diode Electrically Connected in a Reverse Bias Mode and (b) Load Lines of SOA and PD: Dashed Line 1 to 3 Shows the Load of PD as P_1 Increases

3.3.2 Simulation of SOA-PD Device

PSPICE simulation is designed to predict the performance of the SOA-PD device as shown in Figure 3.11. For modeling the SOA-PD device, the equivalent circuits of SOA and PD are developed to compute the impedance of both the components using EIS measurements. Information regarding EIS analysis is described in Appendix A. Figure 3.11 shows the equivalent circuit of SOA-PD device. Two diodes are used to simulate the p-i-n structures in the SOA and PD. The SOA contains a capacitor (500 pF), a parallel resistor (3.15 MΩ), and a serial resistor (75.5 Ω), and the PD has capacitance of 30 pF. The anode of the PD is biased with a direct current (DC) source of -2V.

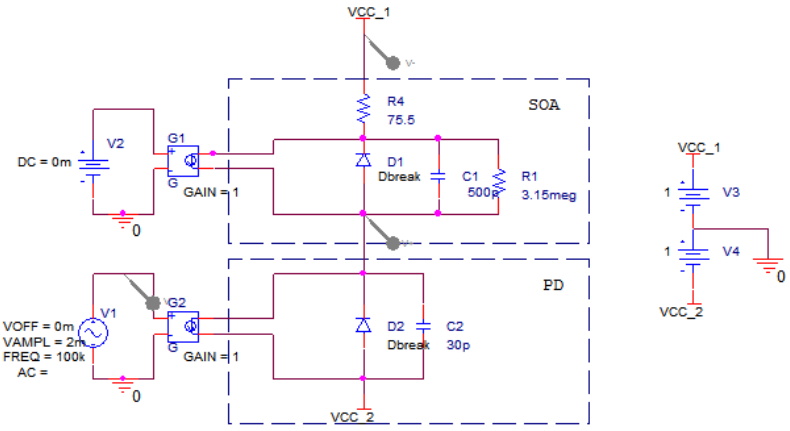

Figure 3.11 PSPICE Simulation Circuit of SOA-PD Device

Since PSPICE can only simulate electric circuits running voltage or current signals, the optical sources in the real case are substituted by current sources. This substitution is reasonable because photo current is generated when optical signal is incident on the SOA and PD. Simulation results shows that the SOA-PD device can generate a binary output when sinusoidal input signal with 2 mV amplitude and 100 kHz frequency is sent into the PD as shown in Figure 3.12 (a). The electric hysteretic curve is shown in Figure 3.12 (b).

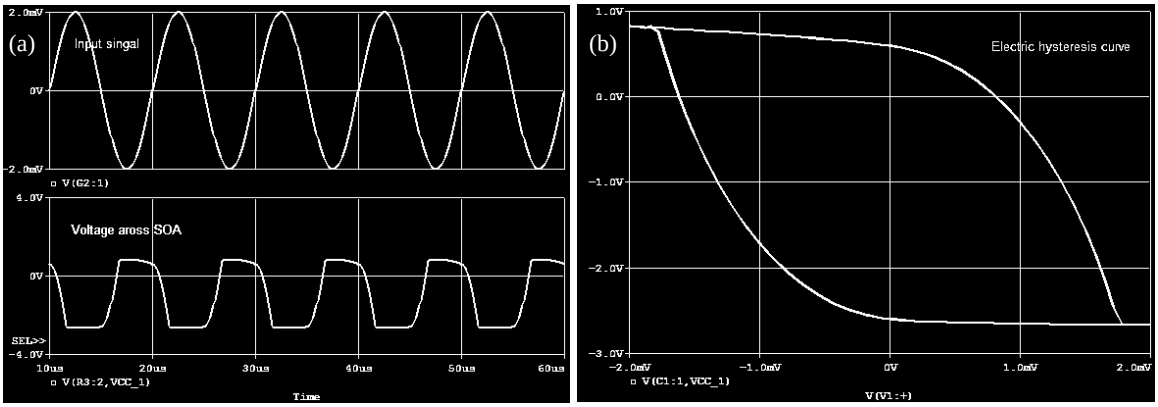

Figure 3.12 PSPICE Simulation Results: (a) the Input Signal, P_1, (Upper Trance) and the Voltage Output between SOA and PD (Lower Trace) at 100 kHz; (b) the Electrical Bistability of SOA-PD Device.

3.3.3 Experimental Demonstration of SOA-PD Device

The experimental setup for testing the SOA-PD device is shown in Figure 3.13. An EAM laser (Fujitsu FLD5F10NP) at wavelength λ_1=1553.3 nm is driven by a 130 mA current and a 2.4V_{pp}, -1.2V_{off} modulation voltage, generating a sinusoidal optical signal with an average power of 2.55 dBm and contrast of 10.41 dB (maximum value of the sinusoidal signal is 5.19 dBm and minimum is -5.22 dBm). This optical signal, P_1, is received by the PD (Eudyna FID3Z1KX) which is electrically connected to the SOA (Covega SOA-1117), while another continuous-wave (CW) laser (ALCATEL A1905) generates a CW signal, P_2, at wavelength λ_3=1551.7 nm to the SOA. A reverse bias is applied to the SOA-PD device at the anode of the PD, V_{RB}= -2V. A binary optical output can be produced at the output of the SOA if a proper power of P_2 is chosen (P_2 =2.14 dBm in this case). However, this output power is so small (-31.02 dBm) that it is impossible to be used for a sufficient feedback. In order to generate enough output power, a post-amplifier such as an EDFA (considering the gain has to be > 33 dB) has to be used after the SOA. As the EDFA greatly enhances the output power of the binary signal, an amplified-spontaneous-emission (ASE) noise is also added to the output signal. To remove this noise, a band pass filter (Dicon 30A14G000300) with a center wavelength of 1551.7 nm and a bandwidth of ±0.35 nm is placed after the EDFA. Finally a photo detector (EOT ET-3500) is connected to the output of band pass filter to observe the output on a digital oscilloscope.

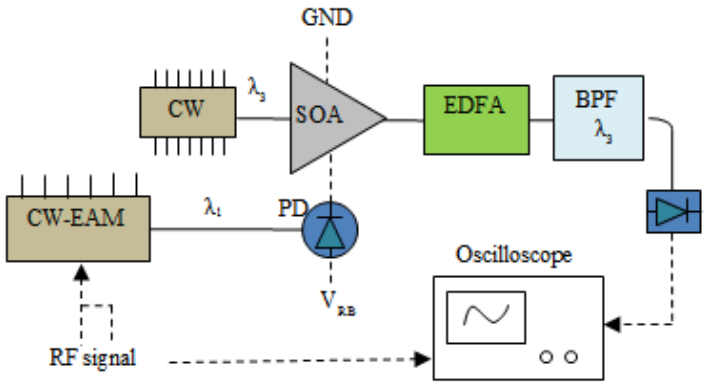

Figure 3.13 Schematic Diagram of Experimental Setups for SOA-PD Device

In order to compare with the simulation results, the voltage across SOA as a function of time is observed using an electrical probe. This voltage signal can be used to predict the optical output of SOA based on the transmittance curve of SOA shown in Figure 3.7. Figure 3.14 shows the input sinusoidal signal, the voltage across SOA and electrical hysteresis curve. The results are in great accordance with the simulation results shown in Figure 3.12.

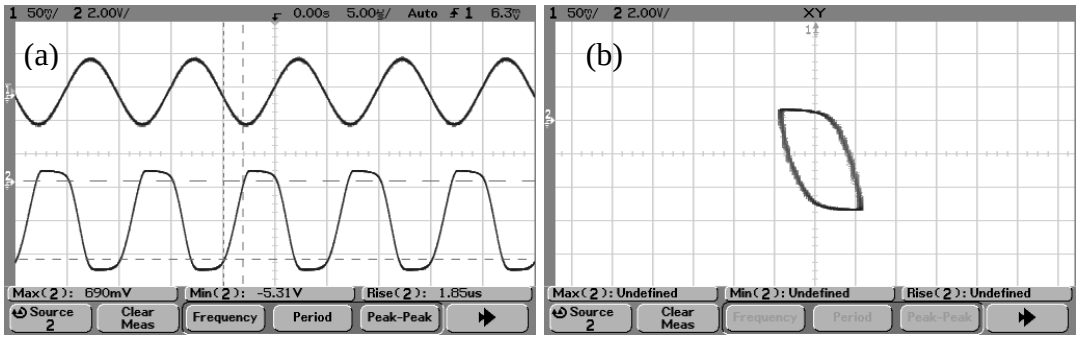

Figure 3.14 Voltage Signals: (a) Input Sinusoidal Signal (Upper Trace) and the Voltage Output between SOA and PD (Lower Trace) at 100 kHz; and (b) the Electric Bistability.

Optical bistability of the SOA-PD device is a study focus, since electrical bistability has been well reported by many articles [8, 9, 22], and achieving optical quantization is the most critical and challenging task of achieving all-optical A/D conversion. The performance of the SOA-PD device has several limitations: the first one is the switching speed is limited by the total capacitance of the device. The total capacitance means the summation of the capacitances in both

SOA and PD, instead of the capacitance of two components in series. To better understand this, I recommend references [1, 7, 9]. The second limitation is the width of hysteresis window is dependent on the frequency of input signal. The width of hysteresis window gives the minimum contrast of the input signal which the SOA-PD device can convert into a binary output. In other words, the contrast of the input signal has to be larger than the width of hysteresis window to ensure the SOA-PD device can switch between its On- and OFF-levels. This property will be discussed in the following text.

Figure 3.15 shows the binary optical outputs of the SOA-PD device and the optical hysteresis curves at 10 kHz, 50 kHz and 100 kHz. Unlike the electrical hysteresis curve, the optical hysteresis curves are non-inverted: this means device switches to ON- level when the input signal varies from its minimum to maximum values and OFF-level when the input signal varies from its maximum to minimum values. In addition, the width of the hysteresis window is directly correlated to the frequency of input signal. As the frequency of the input signal increases, the width of the hysteresis window also increases as shown in Figure 3.15 (d) - (f). In other words, as the frequency of the input signal is increased, the switching threshold of the SOA-PD device is increased. In the experiment, the hysteresis window size, $|\Delta Z|$, is measured as 10.3 mV, 18.1 mV and 22.0 mV on the oscilloscope when the input frequency is 10 kHz, 50 kHz and 100 kHz.

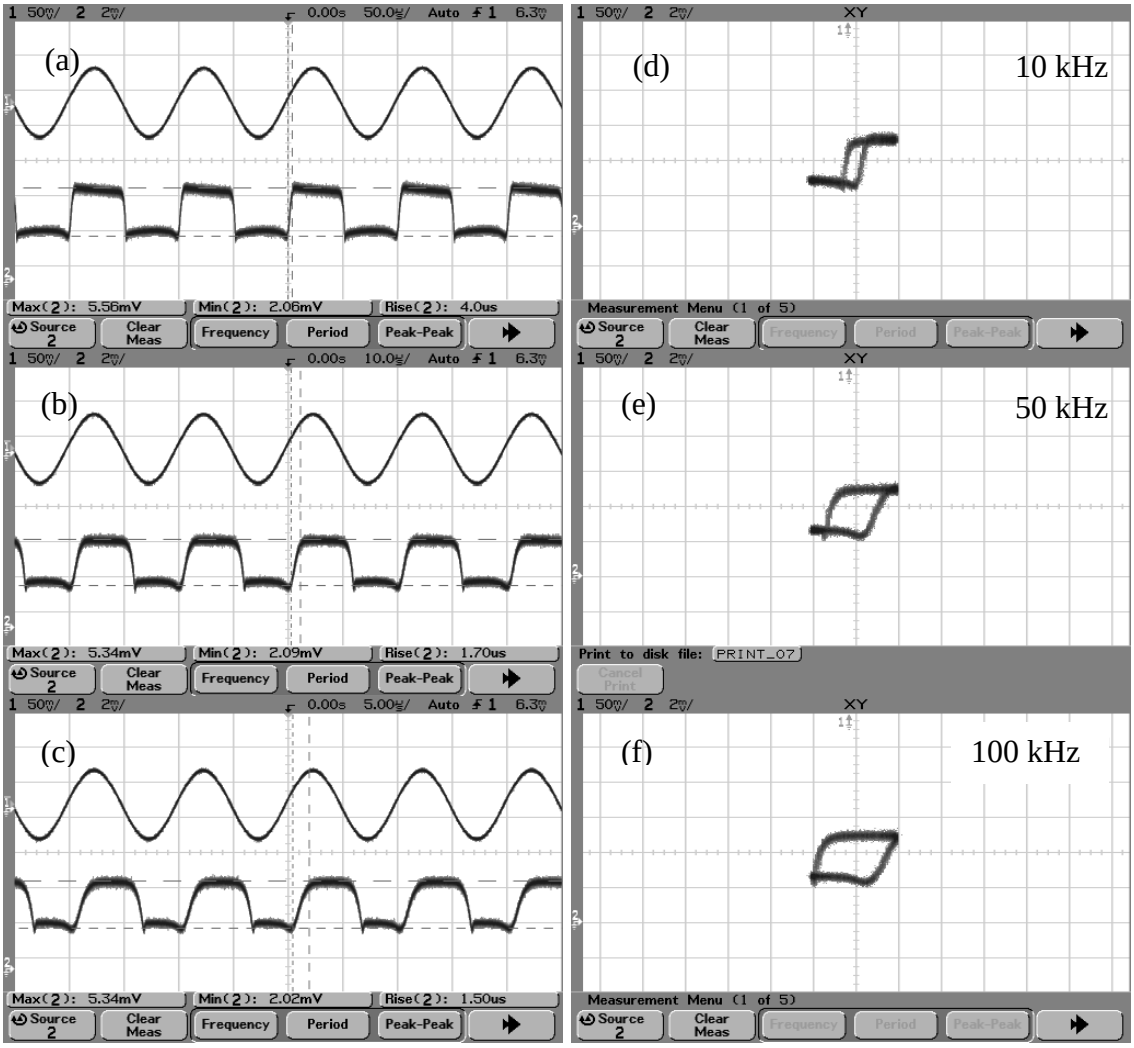

Figure 3.15 Sinusoidal Input Signals (Upper Trance) and Binary Optical Outputs (Lower Trace) at (a) 10 kHz, (b) 50 kHz and (c) 100 kHz; and Optical Hysteresis Curves at (d) 10 kHz, (e) 50 kHz and (f) 100 kHz.

4. OPTICAL LEAKY INTEGRATOR

The optical leaky integrator consists of a SOA (COVEGA SOA-1117), a band pass filter (JDS TB45BT1SC) and an optical isolator (ISO-D-A-1550-0-0) connected together by two optical fiber couplers as shown in Figure 4.1. The so-called leaky integration is realized by circulating optical signals within the closed loop while leaks out a portion of the signals in each round trip. The length of the integration loop (about 12.5 meters) determines the time that light travels through the loop for one round trip, which ultimately determines the resolution of the integrator, called free spectrum range (FSR, about 16 MHz). The operation of the optical leaky integrator involves a wavelength conversion process called cross gain modulation (XGM). The reason for doing this is to avoid the interference that can take place between input signals and accumulating signals. As a result of XGM, the optical leaky integrator has an inverter output. An optical isolator is also used in the integration loop to avoid accumulation of optical signals in the opposite direction.

There are two important parameters in the operation of the optical leaky integrator, the gain and the delay time, both of which are controlled by the gain of the SOA and related to the power of the input signals. The impact of SOA gain on the delay time and the overall gain of the integrator will be discussed in the section 4.3.

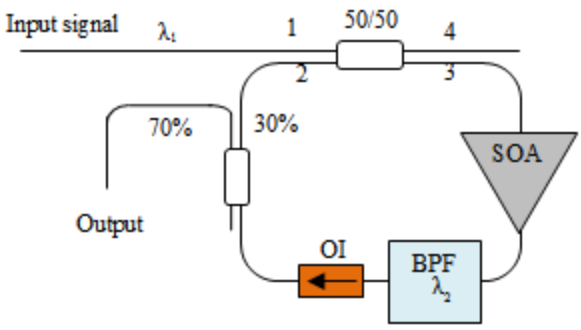

Figure 4.1 Schematic Diagram of Optical Leaky Integrator

4.1 Mathematical Modeling of Optical Leaky Integrator

Consider that the input power sent into the optical leaky integrator is a square wave, expressed as

$$P_1(t) = A \cdot square(\omega t) + C \qquad (4.1)$$

where A is the amplitude and C is the offset power. If Δt is the round trip time for the light traveling through the integration loop (also known as sampling period, which is the reciprocal of free spectrum range, *FSR, FSR=1/ Δt*), then signal power at port 3 (P_3) and port 4 (P_4) can be written as [23, 24, 25]

$$P_3(t + \Delta t) = k \cdot P_1(t + \Delta t) + (1 - k) \cdot P_{loop}(t) \qquad (4.2)$$

$$P_4(t + \Delta t) = (1 - k) \cdot P_1(t + \Delta t) + k \cdot P_{loop}(t) \qquad (4.3)$$

where k is the coupling coefficient of the 50/50 coupler ($k=0.5$), and P_{loop} is the power at port 2. The gain of SOA is dependent on the input power and the driving current and is given by

$$G(t + \Delta t) = 10^{(\frac{G_0}{10})/[1+\frac{P_3(t+\Delta t)}{P_{sat}}]} \qquad (4.4)$$

where G_0 is small signal gain (unit: dB) and P_{sat} is SOA saturation power. Hence, the power after SOA is

$$P_{SOA}(t + \Delta t) = k \cdot G(t + \Delta t) \cdot P_1(t + \Delta t)$$

$$= k \cdot G(t + \Delta t) \cdot P_1(t + \Delta t) + (1 - k) \cdot G(t + \Delta t) \cdot P_{loop}(t) \qquad (4.5)$$

Notice that the first term of this equation is related to wavelength λ_1, while the second term is related to wavelength λ_2. Thus, signal power after band-pass filter (P_2) is

$$P_2(t + \Delta t) = (1 - k) \cdot G(t + \Delta t) \cdot P_{loop}(t) \qquad (4.6)$$

Finally, the integrator output power and the loop power are derived. They are

$$P_{out}(t + \Delta t) = 0.7 \cdot (1 - k) \cdot G(t + \Delta t) \cdot P_{loop}(t) \qquad (4.7)$$

$$P_{loop}(t + \Delta t) = 0.3 \cdot (1 - k) \cdot G(t + \Delta t) \cdot P_{loop}(t) \qquad (4.8)$$

.

4.2 Simulation of Optical Leaky Integrator

Based on the mathematical model that is derived in the previous section, a Matlab-based simulation can be conducted to predict the performance of the optical leaky integrator. A square wave with 100 kHz frequency and 0.15 mW amplitude is used as the input signal in the simulation. The gain of the SOA is manually chosen at 16.9 dB, 17.0 dB and 17.1 dB to demonstrate the changes in the output signals. Figure 4.2 shows the same input signal and the simulated integrator outputs when the gain of the SOA is (a) G_0=16.9 dB, (b) 17.0 dB, and (c) 17.1 dB. The simulation results demonstrate that as the gain of the SOA increases, the average output power and the contrast of this output are also increased. It can also be noted that the time during which the integrator outputs vary from their maximum values to minimum values (the delay time as described earlier) is decrease as the gain of the SOA increases.

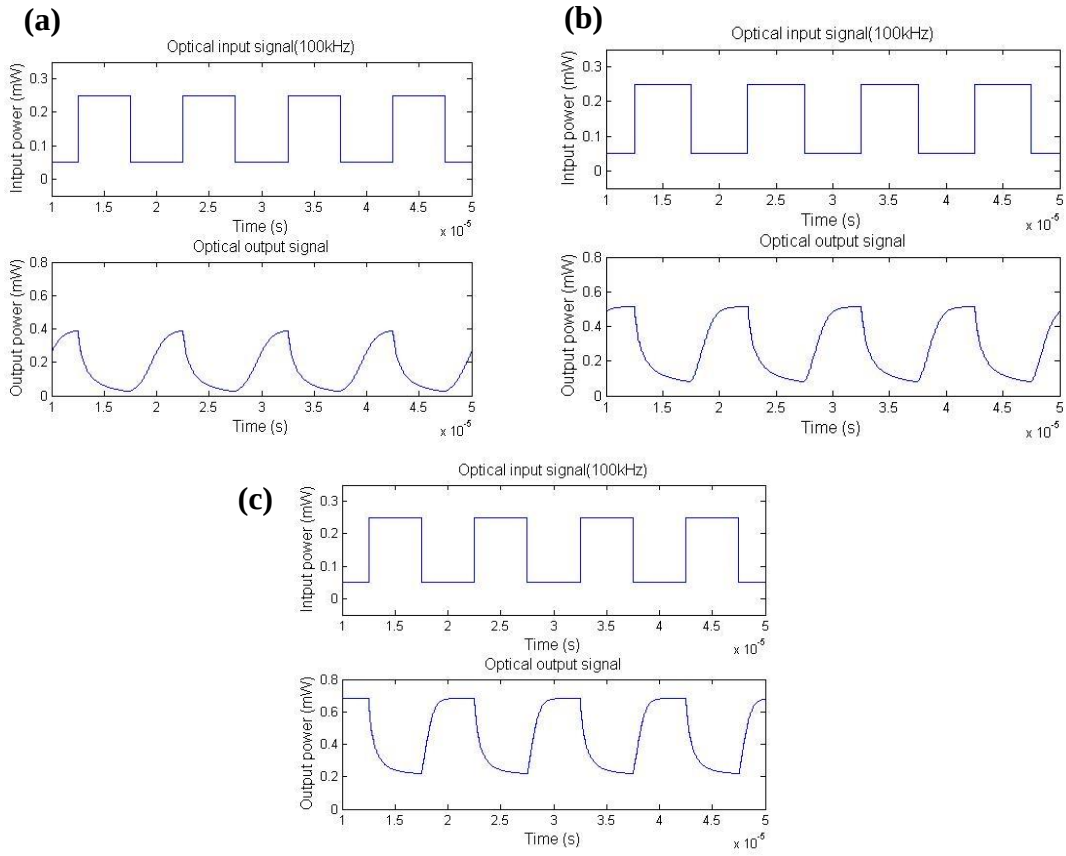

Figure 4.2 Matlab Simulation of Optical Leaky Integrator When Small Signal Gain Is (a) 16.9 dB, (b) 17.0 dB and (c) 17.1 dB

4.3 Experiment of Optical Leaky Integrator

Figure 4.3 illustrates the experimental setup of the optical leaky integrator. An EAM laser (Fujistu FLD5F10NP) is driven by a 13 mA current and a -1.0V_{off}, 2.0V_{pp} modulation voltage, generating a square-wave input signal at 100 kHz. The square-wave signal has an average power of -11.46 dBm and a contrast of 1.40 dB (corresponding to maximum value of -11.33 dBm and minimum value -12.73 dBm). In order to demonstrate the impact of the SOA gain on the operation of the optical leaky integrator, the driving current of SOA is chosen at 248.0 mA, 249.0 mA and 250.0 mA and corresponding outputs of the integrator are compared. Two photo detectors, PD_1 and PD_2, are used for monitoring the input signal and output signal respectively.

The wavelength of input signal and is λ_1=1553.3nm, while the wavelength of the accumulating signal is λ_2=1551.7nm.

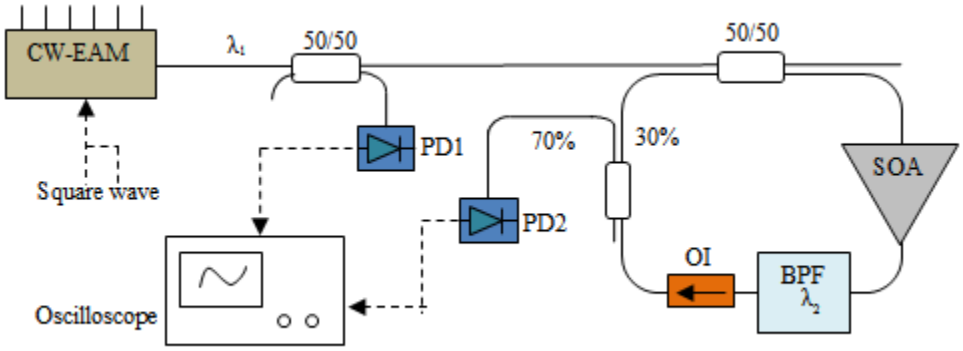

Figure 4.3 Schematic Diagram of Experiment Setup of Optical Leaky Integrator

The input signals and output signals of the optical leaky integrator are shown in Figure 4.4. The delay time of the output signals is represented by their rise times which are automatically measured on the digital oscilloscope. Figure 4.4 demonstrates that with the same input signal, the contrast of the output signals is increased as the driving current of SOA is increased, while the delay time of the output signals is decreased with the increment of the SOA current. To better demonstrate these relations, the average power of the integrator outputs is measured when the driving current of the SOA is 248.0 mA, 249.0 mA and 250.0 mA. The corresponding output powers are -8.4 dBm, -7.0 dBm and -6.2 dBm. Hence, the gain of the optical leaky integrator and the delay time of the integrator outputs can be described as a function of the SOA current as shown in Figure 4.5. These results agree with the prediction of the simulation in Section 4.2.

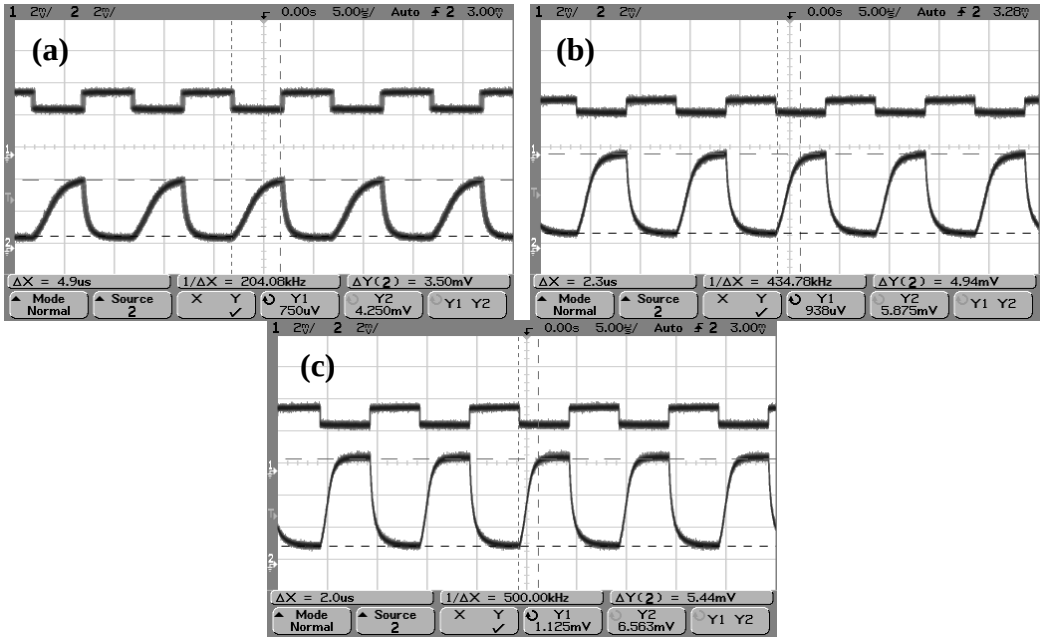

Figure 4.4 Input Signal (Upper Trace) and Leaky Integrator Output (Lower Trace) When Driving Current of SOA Is (a) 248.0mA, (b) 249.0mA and (c) 250.0mA.

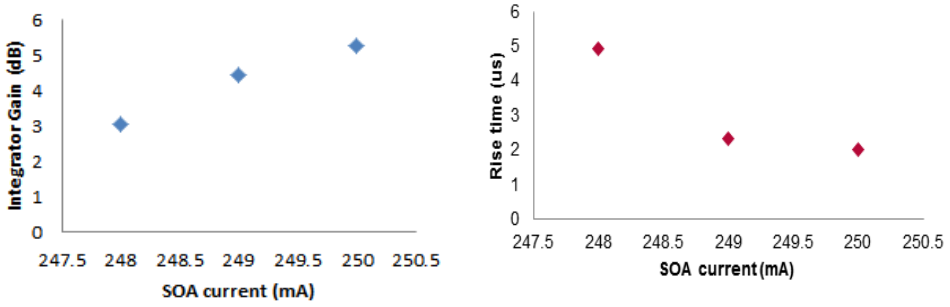

Figure 4.5 Integrator parameters: (a) Gain and (b) Rise Time of Integrator Output vs. SOA Current

5. DESIGN AND EXPERIMENT

In designing the architecture of the all-optical ΣΔ modulator, amplification of the integrator output signals becomes a critical issue, since switching speed of the SOA-PD device is subject to the contrast of its input signals. The method to amplify the integrator output can be various. In this chapter, two architectures of the all-optical ΣΔ modulator are presented. The first one utilizes an EDFA as a post-amplifier of the optical leaky integrator, while the second one replaces the EDFA with a SOA for circuit integration in the future. The optical binary outputs of both architectures are examined and then demodulated through a Matlab-based low pass filter to test the performance of the conversion.

5.1 Architecture of the All-Optical ΣΔ Modulator

The architecture of all-optical ΣΔ modulator is based on an asynchronous first-order fiber-optic ΣΔ modulator demonstrated in [6, 5]. The system consists of an optical leaky integrator, an optical comparator and a feedback loop. Figure 5.1 illustrates the experimental setup of the all-optical ΣΔ modulator. A function generator is used to modulate an EAM laser (Fujitsu FLD510NP) generating an optical sinusoidal signal to the system. This signal is added to the feedback signal of the modulator via a 50/50 fiber-optic coupler, and then enters the optical leaky integrator. The output signal of the optical leaky integrator is amplified by an EDFA before it enters the SOA-PD device for comparison. To achieve the maximum switching speed in the SOA-PD device, the amplified integrator output has an average power around 10 dBm. Finally, the output of the SOA-PD device is divided into two portions: 90% of the power is fed back to

the circulating loop, while 10 % is used as the output of the modulator and analyzed using a photo detector (EOT ET3500F) and an oscilloscope. Three different wavelengths are used in the system: the input signal wavelength λ_1 = 1553.3 nm, integration signal wavelength λ_2 = 1555.6 nm, and feedback signal wavelength λ_1 = 1551.7 nm.

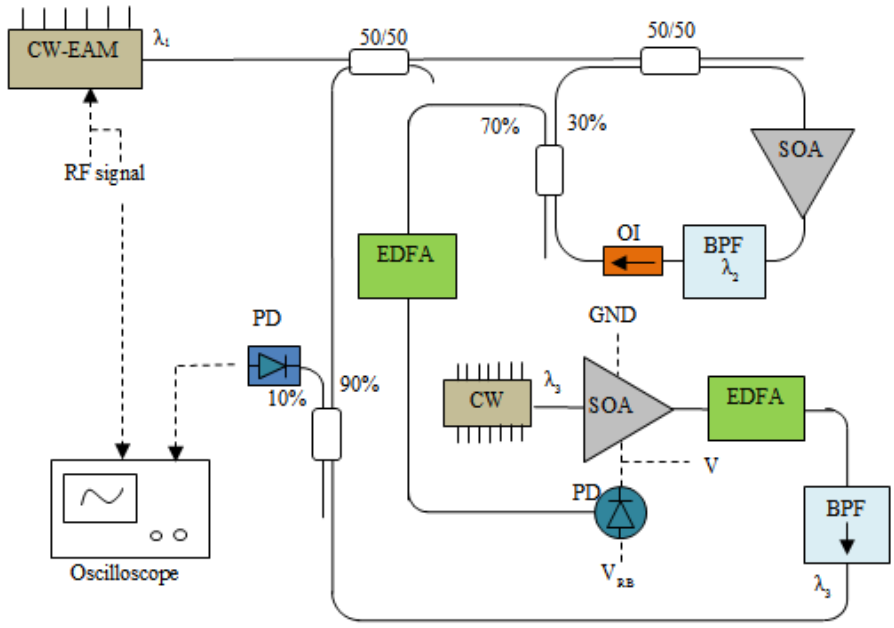

Figure 5.1 Schematic Diagram of All-Optical ΣΔ Modulator

5.1.1 Limit Cycle Frequency

The sampling frequency of the optical ΣΔ ADC is the frequency of which the modulator oscillates when the input is a DC signal. This frequency is also called the limit cycle frequency because it sets the limit for the oversampling of the signal to be converted. This frequency should be over twice of the cutoff frequency of the input signal (Nyquist frequency). The limit cycle frequency of the all-optical ΣΔ modulator is determined by the width of the hysteresis window in the quantizer as it is demonstrated in Chapter 3. Therefore, the maximum switching speed of the SOA-PD device is what determines the maximum sampling frequency of the system.

The sampling frequency for the all-optical ΣΔ modulator is found by sending a DC signal into the system. As expected, a one-bit signal stream with an approximate duty cycle of 50 % is observed on the oscilloscope where the signal frequency could be measured. Figure 5.3 shows the DC input (top) and the unforced output oscillation (bottom). The sampling frequency is found to be about 220 kHz.

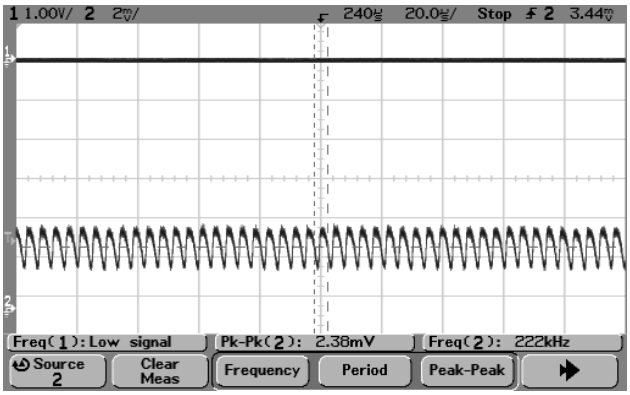

Figure 5.2 DC Input (Top) and Unforced Binary Output (Bottom)

The all-optical ΣΔ ADC system has a self-set limit cycle frequency. This is due to the quantizer window width of the SOA-PD device is determined by the frequency of the input signal (to the PD). In this case the frequency equals the oscillation frequency of the modulator (which is the limit cycle frequency). That is to say, no matter what frequency the input signal is, oscillation frequency within the system will remain the same. This does not always hold true, however, the sampling frequency does change under some adjustments to the system parameters. One adjustment is to change the output power of the CW laser which consequently changes the switching thresholds of the optical quantizer. Figures 5.4 (a) to (c) show the limit cycle frequency changing from 250 kHz to 222 kHz when the driving current of the CW laser is decreased from 16.9 mA to 14.8mA. This operation changes the limit cycle frequency because the hysteresis window of the SOA-PD device is subject to the optical power sent into both SOA

and PD. When the optical power sent into the SOA decreases, the hysteresis window is increased in size. So the oscillation frequency of the modulator is decreased as a result of the drop of the switching speed in the SOA-PD device. However, this change in the sampling frequency is very small (about 200 kHz to 250 kHz).

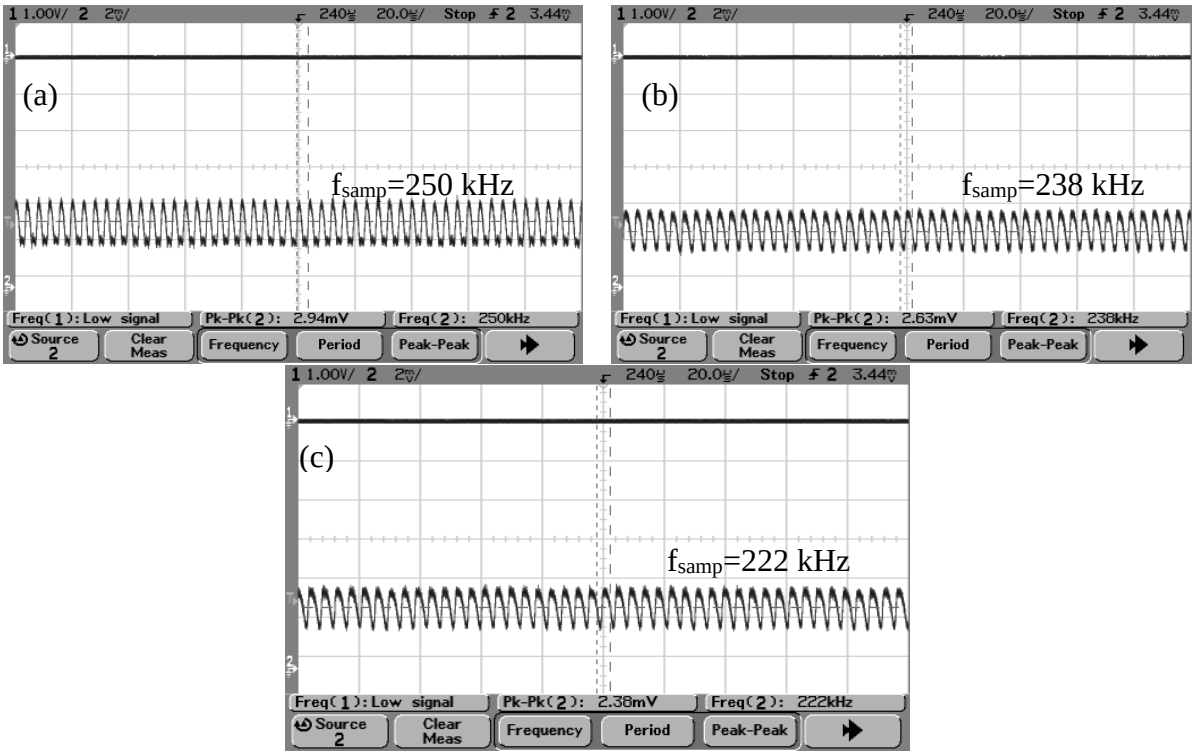

Figure 5.3 DC Input (Top) and Unforced Binary Output (Bottom) When Driving Current of CW Laser Is (a) 16.9 mA, (b) 15.3 mA and (c) 14.8 mA

As it is shown in Chapter 3 the limit switching speed of the SOA-PD device is about 200 kHz. This proves that the limit cycle frequency of the all-optical ΣΔ modulator is restrained by the switching speed of the optical quantizer, since the FSR (16 MHz) of the integration loop is significantly greater than 200 kHz.

5.1.2 Oversampling Ratio

The oversampling ratio is one of the most important parameters of any ΣΔ A/D converters since it related to the resolution of the binary output of the system. If the optical power through the system remains the same while the frequency of input signal is increased, the oversampling ratio, *M* (ratio of the limit cycle frequency to twice the input frequency, $f_s/2f_0$), will decrease. This trend is illustrated by Figure 5.5. When input signal varies from 10 kHz to 100 kHz with a step of 10 kHz, the limit cycle frequency of the modulator stays constant at 200 kHz, hence, the oversampling ratio decreases from 20 to 2. When sampling frequency equals to twice of input frequency (Nyquist frequency), oversampling ends.

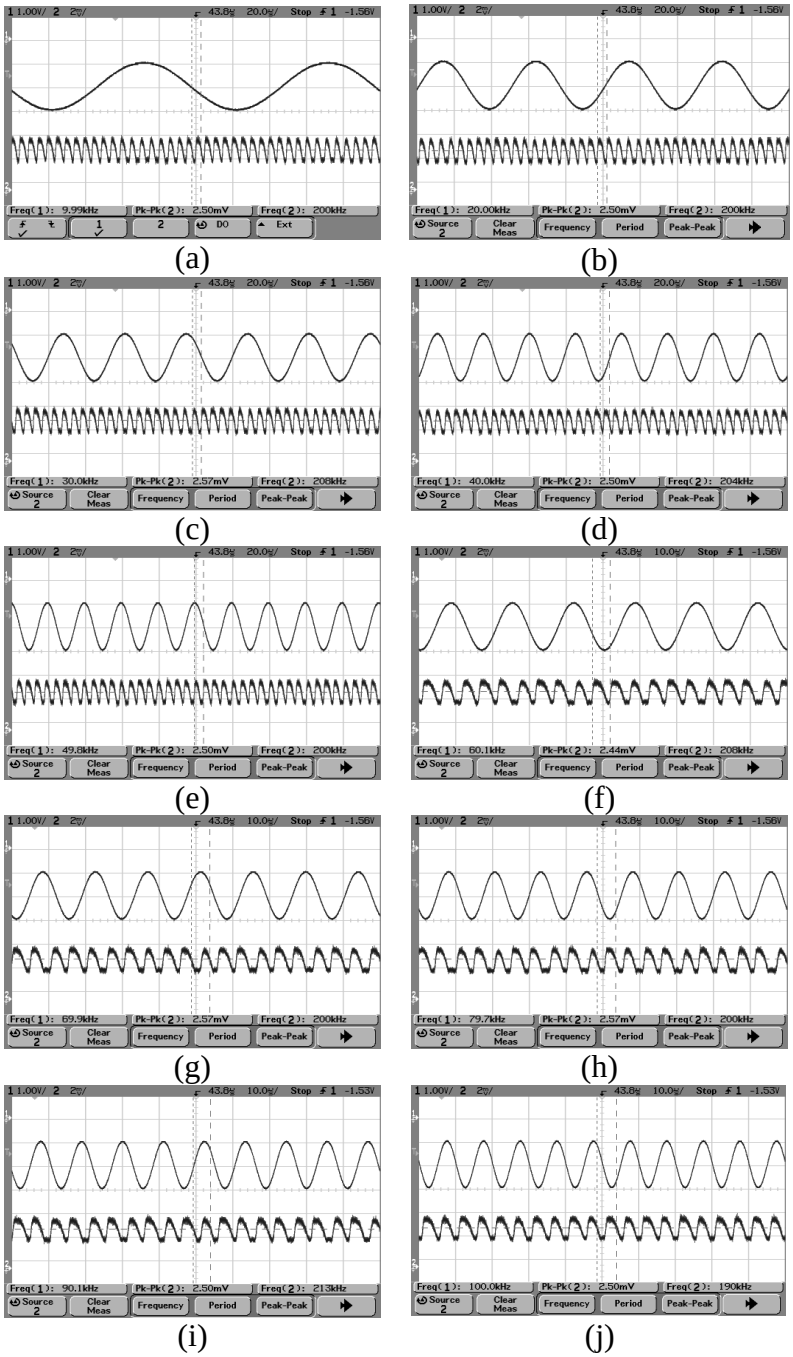

Figure 5.4 Input Analog Signal (Upper Trace) at (a) 10 kHz, (b) 20 kHz, (c) 30 kHz, (d) 40kHz, (e) 50 kHz, (f) 60 kHz, (g) 70 kHz, (h) 80 kHz, (i) 90 kHz, (j) 100 kHz and Corresponding Binary Outputs (Lower Trace).

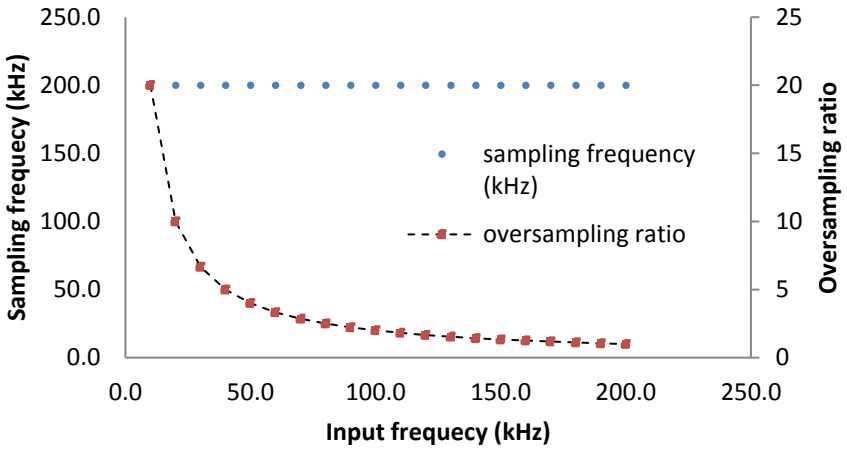

Figure 5.5 Sampling Frequency and Oversampling Ratio vs. Input Frequency

5.1.3 Binary Output and Demodulation

The function of the all-optical ΣΔ modulator is to convert an analog signal to a binary bit stream. Figure 5.6 illustrates sinusoidal input signals (upper) at 10 kHz, 20 kHz and 30 kHz and their binary output signals (middle). The binary outputs have their maximum duty cycle when the input signals have the minimum values, and minimum duty cycle when input signals have the maximum values. As a result, the binary output of the all-optical ΣΔ modulator is an inverted NRZ bit stream. However, this binary signal suffers from a relatively long transition time (the time that signal transits between ON-level and OFF-level), which is mainly due to the switching speed of the SOA-PD device.

Perhaps the easiest way to examine the A/D conversion is to demodulate the binary output of the system with a low pass filter. If the cutoff frequency is properly chosen, the filtered binary output should be similar to the initial input signal. Here a 3rd order butterworth filter is demonstrated in the Matlab simulation workspace. The output of ΣΔ modulator is detected with the oscilloscope and the trace is saved as a CSV file. The file is then processed in Matlab. The

cut-off frequencies for the sinusoidal input signals at 10 kHz, 20 kHz and 30 kHz are set at 12 kHz, 2.4 kHz and 3.6 kHz respectively. Demodulation program can be found in Appendix D.

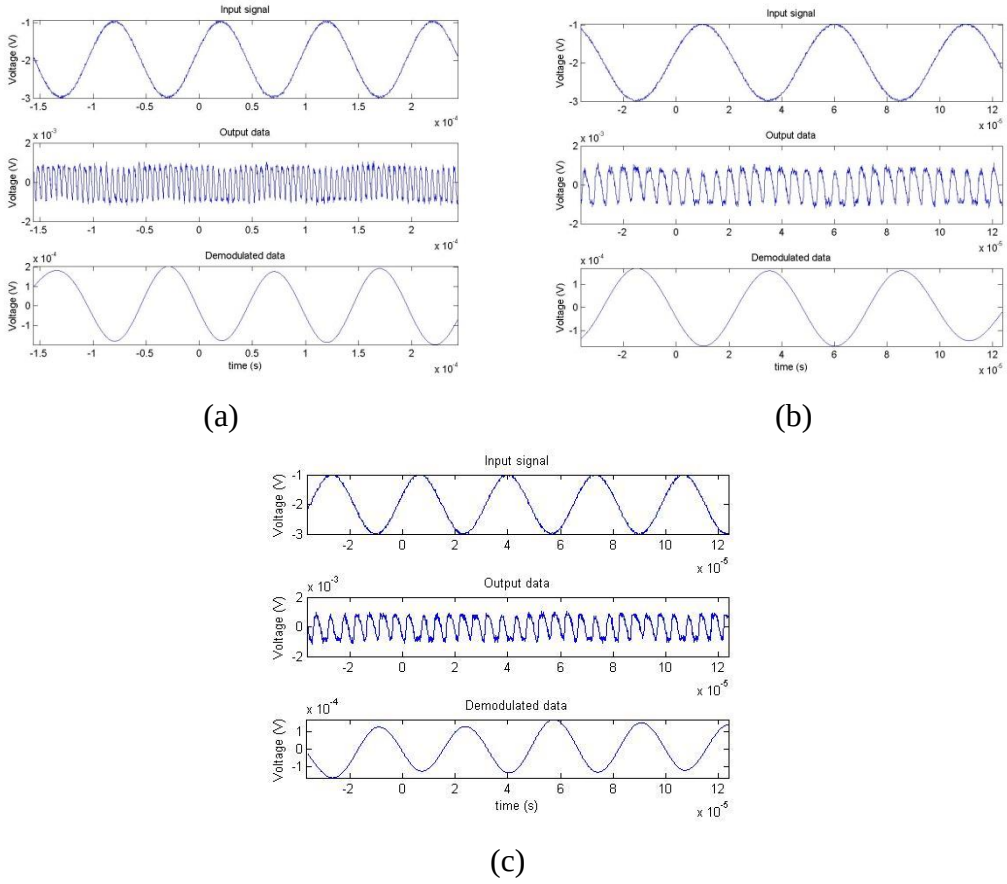

Figure 5.6 Sinusoidal Input (Top), Binary Optical Output (Middle) and Demodulated Signal (Bottom) When Input Freuqncy Is at (a) 10 kHz, (b) 20 kHz and (c) 30 kHz.

Other input waveforms, such as triangle wave, and ramp signal, are also tested to demonstrate the performance of the all-optical ΣΔ modulator. Comparing to a sinusoidal wave, these two waveforms contain more frequency components in their frequency domain. Thus, the cut-off frequencies for a 10 kHz triangle wave and a 10 kHz ramp signal are set at 80 kHz. The reconstructed signals have inverted waveforms with respect to the initial input signals and smoothed edges resulted from low pass filtering.

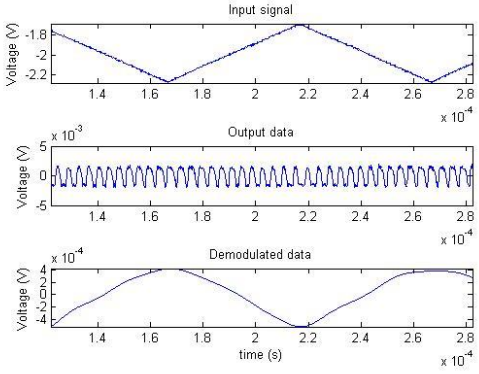

Figure 5.7 Triangular Input Signal (Top) at 10 kHz, Digital Optical Output (Middle) and Demodulated Signal (Bottom)

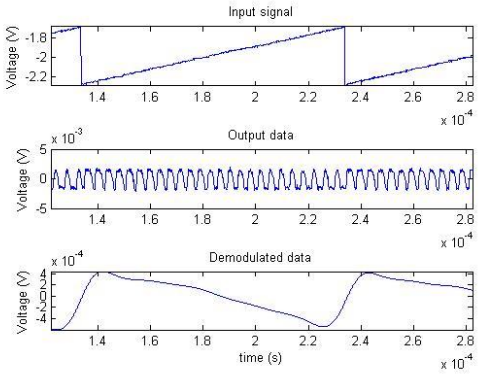

Figure 5.8 Ramp Input Signal (Top) at 10 kHz, Digital Optical Output (Middle) and Demodulated Signal (Bottom)

5.2 Improved Architecture

An improved architecture of the all-optical ΣΔ modulator is shown in Figure 5.9. The EDFA after the optical leaky integrator is substituted with a SOA for the purpose of circuit integration in the future. In order to remove the ASE noise of the SOA, a band pass filter (Dicon TF-1500-0.8-9/TB-FC/A-1) with center wavelength of λ_2 = 1555.6 nm and bandwidth of ±0.65 nm is place after the SOA, since the ASE noise of SOA is much higher noise than that of the EDFA with respect to the same amplified output power. For easier understanding, the SOA and band pass filter can be regarded as a post-amplification unit where its average output power is set

to be 10 dBm (the maximum safe power for the photo diode) for achieving maximum switching speed of SOA-PD device.

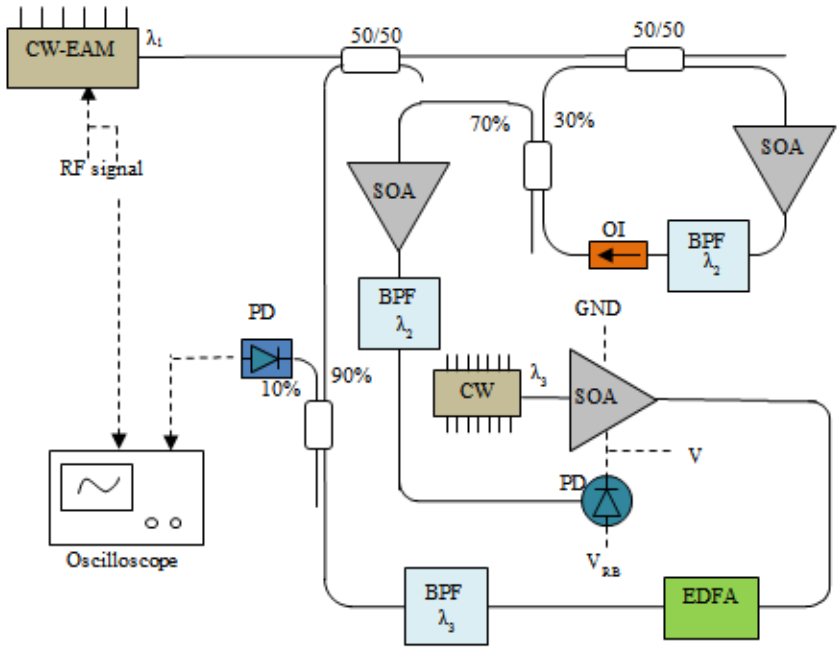

Figure 5.9 Schematic Diagram of the Improved All-Optical ΣΔ Modulator

5.2.1 Binary Output and Demodulation

Figure 5.10 shows the analog input signals, binary outputs and the reconstructed signals for the modified modulator. Experimental results show a success of replacing EDFA with the SOA and band pass filter. The binary output of the system has a sampling frequency of 300 kHz regardless of input frequency (10 kHz, 20 kHz and 30 kHz).

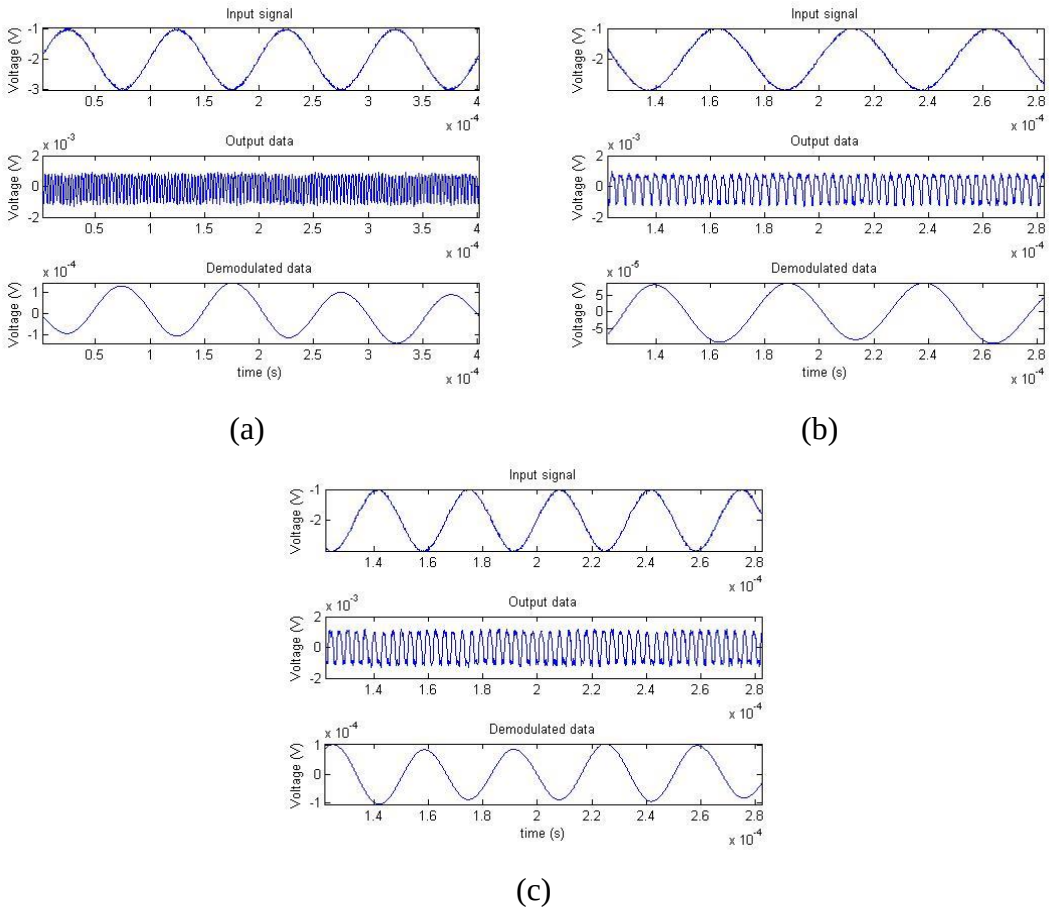

Figure 5.10 Sinusoidal Input (Top), Digital Optical Output (Middle) and Demodulated Signal (Bottom) When Input Freuqncy Is at (a) 10 kHz, (b) 20 kHz and (c) 30 kHz.

Perhaps one could come up with the question -- why not replace the EDFA after the SOA-PD device with a SOA? This has to contribute to the low transmittance of SOA in reverse bias. It has been demonstrated in Chapter 3 that the gain of the SOA in the SOA-PD device is less than -30 dB since the SOA is reverse biased, and a sufficient feedback power to the system demands at least 3 dBm in the feedback loop. That is to say the post amplifier of the SOA-PD device needs at least 33 dB gain. However, the gain of a commercialized SOA is usually around 20 dB which is far away from the requirement.

5.2.2 Frequency Domain Analysis

One simple way to analyze the binary output of the all-optical ΣΔ modulator is to convert the binary output from a time domain signal to a frequency domain signal, and the best way to do this is to apply a Fast Fourier Transform (FFT) [26]. A Matlab based program has been developed to calculate the SNR and ENOB in the spectra of the binary outputs. FFT analysis program can be found in Appendix E. The calculated results of SNR, signal-to-noise and distortion ratio (SINAD), ENOB, and spurious-free dynamic range (SFDR) are listed in the Table 5.1.

Table 5.1 FFT Analysis of All-Optical ΣΔ ADC System

frequency	SNR (dB)	SINAD (dB)	ENOB (bits)	SFDR (dB)
10kHz	29.449	27.074	4.205	13.840
20kHz	27.992	26.374	4.071	14.126
30kHz	26.381	25.538	3.950	14.500

6. PERFORMANCE CHARACTERIZATION

Methods to characterize and analyze the performance of a specific A/D converter can vary [27, 28]. However, there are some standard measures that are commonly used for all. The signal-to-noise ratio (SNR) is the most common measurement in engineering to quantify how much a signal has been corrupted by noise. Other performance parameters, such as the effective number of bits (ENOB), are commonly used in oversampled ADC systems. In this chapter, performance characterization of the all-optical ΣΔ modulator will be conducted by analyzing the noise throughout the open-loop system (feedback loop is disconnected from the summing junction). In doing so, the optical link is first divided into five subsystems: optical source (OS), integrator, integrator amplifier (IA), comparator and comparator amplifier (CA) as shown in Figure 6.1. Then the noise after each component is theoretically modeled, and therefore, the SNR and ENOB of the system are calculated.

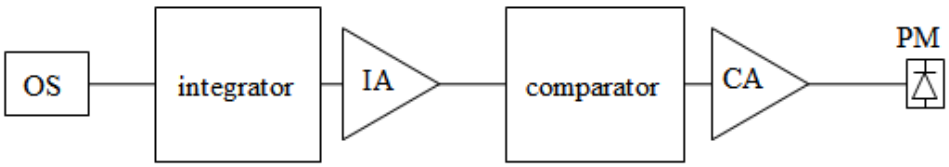

Figure 6.1 Block Diagram of Open-Loop All-Optical ΣΔ Modulator. OS: Optical Source, IA: Integrator Amplifier, CA: Comparator Amplifier, PM: Power Meter

6.1 Gain Measurement

The binary output of the all-optical ΣΔ modulator is first examined, and then the feedback loop is disconnected from the summing junction to measure the power before and after

each subsystem as shown in Figure 6.1. Table 6.1 presents the input and output power and the gain of the integrator, IA, comparator and CA. The gain of each component will be used to evaluate the noises in the disconnected system and finally to calculate the dynamic range (SNR) and resolution (ENOB) of the system.

Table 6.1: Power throughout System and Gain of Each Component

	integrator	IA	comparator	CA
Input(dBm)	-13.60	-2.10	2.60	-31.07
error (dB)	0.05	0.01	0.05	0.01
Output(dBm)	-2.10	9.50	-31.07	2.60
error (dB)	0.01	0.02	0.01	0.05
Gain (dB)	**11.5**	**11.6**	**-33.67**	**33.67**

6.2 Noise Analysis

To better understand the noise model of the open-loop system, a detailed block diagram is presented in Figure 6.2. The optical source (OS) is the EAM laser modulated by a RF generator. The major noise in the OS is the relative intensity noise (RIN) of the laser. This noise then passes through the integrator in conjunction with the noise generated by the SOA in the integrator. Since a narrow band pass filter is used after the SOA in the integrator, the major noise power, in this case, is modeled as the noise power through a data link [29]. Similarly, the noise power of the integrator amplifier (IA) and comparator amplifier (CA) is also model as the same way. The noise in the SOA-PD device consists of the mean-square noise current contributed by the optical noise from the former components, the shot noise, the thermal noise and the dark current. Then the noise power of the SOA-PD device is derived by multiplying the gain of the SOA, the total noise current and the bias voltage.

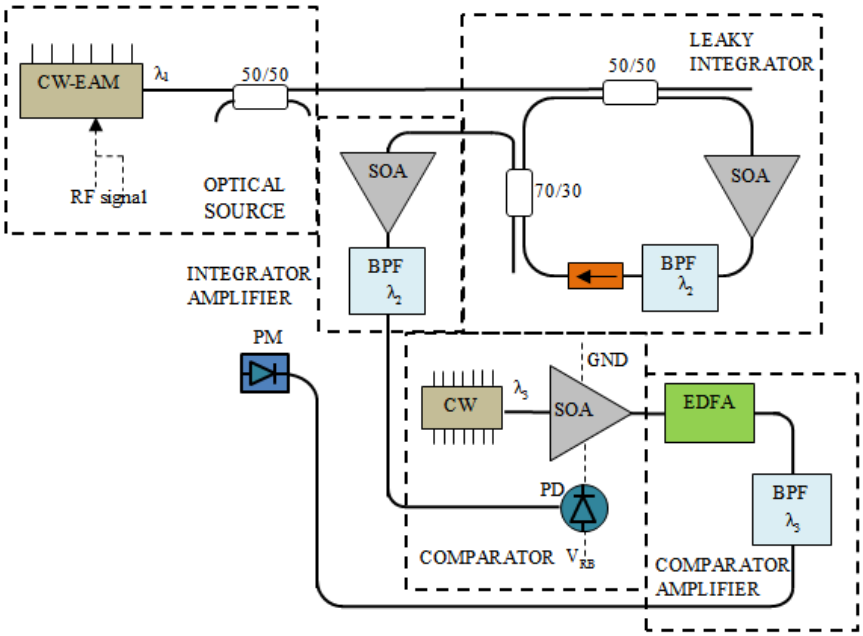

Figure 6.2 Block Diagram of Open-Loop All-Optical ΣΔ Modulator

6.2.1 Relative Intensity Noise of Optical Source

Relative intensity noise (*RIN*) describes fluctuation in the optical power of a laser, which mainly stem from intrinsic optical phase and frequency fluctuations caused by spontaneous emission [30]. The *RIN* is defined as

$$RIN = \frac{\langle \Delta P(t)^2 \rangle}{P_1^2} \qquad (6.1)$$

where $\Delta P(t)$ represents the fluctuations of optical power and P_1 *is* the average optical power. Optical analog signal generated by the EAM laser (Fujistu FLD5F10NP) has *RIN* value of -120 dB/Hz according to its specification (in Appendix D). Since the *RIN* is frequency dependent, the optical fluctuation power is written as

$$\langle \Delta P(t) \rangle = \sqrt{RIN \cdot B} \cdot P_1 \qquad (6.2)$$

where *B* is the signal bandwidth and *RIN* is in unit of Hz^{-1}.

6.2.2 Integrator Noise

The integrator consists of a SOA (Covega SOA 1117) and a band pass filter (JDS TB45BT1SC). The output power of the integrator, $P_{2,out}$, is presented as equation (6.3), and it can be written as two components: signal power and noise power. The noise power at the output of a data link is given by equation (6.4) [29].

$$P_{2,out} = G_1 \cdot P_1 = P_{2,signal} + P_{2,noise} \quad (6.3)$$

$$P_{2,noise} = k \cdot T \cdot G_1 \cdot B \cdot F_1 + G_1 \cdot \langle \Delta P(t) \rangle \quad (6.4)$$

where k is the Boltzmann constant ($k=1.38 \times 10^{-23}$ *J/K*), T is the room temperature (293 K), G_1 is the gain of integrator in Table 6.1, and F_1 is the noise figure of the SOA. $F_1 = 9$ *dB* can be found in Appendix D.

6.2.3 Integrator Amplifier Noise

The two components of the IA are a SOA (Kamelian OPA-10-N-C-FP) and a band pass filter (Dicon TF-1500-0.8-9/TB-FC/A-1). The output power and the noise power of the integrator amplifier are written as

$$P_{3,out} = G_2 \cdot P_{2,out} \quad (6.5)$$

$$P_{3,noise} = k \cdot T \cdot G_2 \cdot B \cdot F_2 + G_2 \cdot P_{2,noise} \quad (6.6)$$

where G_2 is the gain of IA in Table 6.1, and F_2 =6.5 dB is the noise figure of the SOA on the specification.

6.2.4 Comparator Noise

The optical comparator is a novel SOA-PD bistable switch where input signal enters PD generating a modulating electric field across SOA connected in series. This electric field

consequently changes the absorption of the SOA and its output power by the QCSE. The calculation of the noise power of SOA-PD device will be based on the operating principle which has been described in Chapter 3. To better understand this calculation, we need to keep in mind that the electro-optic effect is involved in the operational process.

Shot noise appears at the PD and is result of the photo current generated by optical power of IA. The photo current is described as

$$I_p = R \cdot P_{3,out} \tag{6.7}$$

where *R* is the responsivity of the PD and can be found in the data sheet. The mean-square shot noise current in the PD is proportional to the photo current and is expressed as equation (6.8) [31]. Since SOA and PD are connected in series, this current will be the same for both of them.

$$\langle i_{shot}^2 \rangle = 2 \cdot q \cdot I_p \cdot B_e \tag{6.8}$$

Where *q* is electron charge ($q=1.6 \times 10^{-19}$ *C)* and B_e *is the bandwidth of PD.* There will also be photo current generated by optical noise power described by equation (6.6). This noise photo current is written as

$$i_n = R \cdot P_{3,noise} \tag{6.9}$$

In addition, the mean-square dark current in photo diode is described as

$$\langle i_D^2 \rangle = 2 \cdot q \cdot I_D \cdot B_e \tag{6.10}$$

Where I_D is the dark current for the photo diode and is found in the data sheet.

The thermal noise in the SOA-PD device is mainly contributed by the impedance in SOA whose resistance (R_L) is about 3.15 MΩ. The thermal noise current is written as

$$\langle i_T^2 \rangle = \frac{4kT}{R_L} B_e \tag{6.11}$$

Therefore, the total noise current of the optical comparator is summarized as

$$i_{total} = \sqrt{\langle i_{shot}^2 \rangle + i_n^2 + \langle i_D^2 \rangle + \langle i_T^2 \rangle} \tag{6.12}$$

The output of the SOA-PD device is generated by a CW laser beam passing through the SOA with gain G_3. This output power is expressed as equation (6.13). The noise in the output is the product of the gain, the total noise current in the comparator and the reverse bias voltage (V_R), as described in equation (6.14).

$$P_{4,out} = G_3 \cdot P_4 \quad (6.13)$$

$$P_{4,noise} = G_3 \cdot i_{total} \cdot V_R \quad (6.14)$$

$$P_{4,signal} = P_{4,out} - P_{4,noise} \quad (6.15)$$

6.2.5 Comparator Amplifier Noise

The comparator amplifier (CA) consists of an EDFA (IPG EAD-500-CL) and a band pass filter (Dicon 30A14G000300). Like the IA, the average output power and noise power of the CA are expressed as equation (6.16) and (6.17).

$$P_{5,out} = G_4 \cdot P_{4,out} \quad (6.16)$$

$$P_{5,noise} = k \cdot T \cdot G_4 \cdot B \cdot F_4 + G_4 \cdot P_{4,noise} \quad (6.17)$$

$$P_{5,signal} = P_{5,out} - P_{5,noise} \quad (6.18)$$

Substitute (6.15) and (6.16) into (6.18), the ultimate signal power and the noise power of the disconnected system are express as equation (6.19) and (6.20).

$$P_{out,singal} = P_{5,singal} = G_4 \cdot P_{4,signal} - k \cdot T \cdot G_4 \cdot B \cdot F_4 \quad (6.19)$$

$$P_{out,noise} = P_{5,noise} = G_4 \cdot P_{4,noise} + k \cdot T \cdot G_4 \cdot B \cdot F_4 \quad (6.20)$$

6.3 SNR and ENOB

Signal-to-noise ratio (SNR) is a standard measure of the dynamic range of a system. It is defined as the power ratio between signal (useful information) and an unwanted signal (background noise) in the frequency band of interest, as expressed as

$$\text{SNR} = 10 \cdot \log\left(\frac{P_{out,signal}}{P_{out,noise}}\right) = P_{out,signal}(dB) - P_{out,noise}(dB) \qquad (6.21)$$

Where P_{signal} and P_{noise} are the average power of signal and noise respectively. Because of large dynamic range, SNR is often written in logarithmic decibel scale.

Effective number of bits (ENOB) is a measure of the resolution of a digitized signal defining how close an A/D converter resembles to the theoretical mathematical model [1]. It specifies the number of bits in the digital signal above the noise floor. The definition of ENOB is written as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \qquad (6.22)$$

Where SNR is in unit of dB.

The SNR and ENOB of the all-optical ΣΔ modulator can be calculated based on Equation (6.1) to (6.22), where the gain of each subsystem can be found in Table 6.1, and the noise figure of optical amplifiers (SOAs and EDFA) are given in their datasheets which are summarized in Appendix D. Table 6.2 provides us two main information about the all-optical ΣΔ modulator: the overall performance and the signal degradation in the system. The overall performance of the system is given by SNR and ENOB. The SNR is around 25.4 dB and the ENOB around 3.93 bits.

Table 6.2 Noise, Output Power, SNR and ENOB

frequency		OS	Integrator	IA	comparator	CA
10 kHz	noise (mW)	4.37E-06	6.17E-05	8.91E-04	2.40E-06	5.60E-03
	output (mW)	4.37E-02	6.17E-01	8.91E+00	8.78E-04	2.04E+00
	SNR (dB)	39.999566	39.999565	39.999565	25.611493	**25.611493**
	ENOB	**3.96**				
20 kHz	noise (mW)	6.17E-06	8.72E-05	1.26E-03	2.50E-06	5.82E-03
	output (mW)	4.37E-02	6.17E-01	8.91E+00	8.78E-04	2.04E+00
	SNR (dB)	38.494236	38.494235	38.494235	25.440216	**25.440215**
	ENOB	**3.93**				
30 kHz	noise (mW)	7.56E-06	1.07E-04	1.54E-03	2.59E-06	6.04E-03
	output (mW)	4.37E-02	6.17E-01	8.91E+00	8.78E-04	2.04E+00
	SNR (dB)	37.6136414	37.6136409	37.6136409	25.2814169	**25.2814160**
	ENOB	**3.91**				

The signal degradation in the system can be analyzed by looking at the SNR after each subsystem. There is an evident SNR drop at the optical comparator, indicating noise is mainly introduced in the quantization step. Furthermore, close scrutiny of current noises in the SOA-PD device (in Table 6.3) reveals that the majority of the noise current in the SOA-PD device is the shot noise of photo detector which covers about 92% of the total noise current. The second biggest noise associated with quantization process is the noise current produced by former optical noise.

Table 6.3 Mean-Square Current Noises in the SOA-PD Device at 10 kHz

	optical noise	shot noise	dark current	thermal noise	total
mean-square current (A2)	5.08E-13	5.70E-12	8.00E-19	1.28E-17	6.21E-12
percentage	8.18%	91.82%	0.00%	0.00%	

7. CONCLUSION AND DISCUSSION

In developing the all-optical ADC system, optical quantization has become the most challenging work at hand [2, 4, 10]. Even though optical bistability has been enormously reported since 1980s [11] and several promising devices such as S-SEEDs [32, 19] and S-SOA devices [8] have been demonstrated, optical bistable switches are still not implemented in the ADCs according the best of author's knowledge.

In this thesis, two novel optical bistable switches, SOA-BJT device and SOA-PD device, are successfully designed and tested for the purpose of all-optical A/D conversion. Equivalent circuit model of SOA, BJT and PD are subtracted using EIS Potentiostat analysis such that simulations based on the equivalent circuit can be completed in the PSPICE software to predict the performance of SOA-BJT and SOA-PD devices. Then optical bistability of SOA-BJT device and SOA-PD device are observed. Experimental results show that optical binary output of SOA-BJT device is limited by the contrast of input signal since the input signal is actually added onto the output. Therefore, optical bistability of SOA-BJT device is only observed with low-contrast optical input signal at 1kHz. Unlike SOA-BJT device, SOA-PD device utilizes a different scheme: input signal is received by a PD while another CW optical signal passes through the SOA. In such a way, input signal is no longer mixed with the optical binary output. The maximum optical bistability of SOA-PD device is measured at 200 kHz.

Then, an all-optical ΣΔ modulator for A/D conversion is successfully constructed and demonstrated. The system consists of a photonic leaky integrator, the SOA-PD device (quantizer) and a positive feedback loop. The limit cycle frequency of the system is first measured around 250 kHz depends on the power through the system implying the limited conversion rate of the all-optical ΣΔ modulator is due to the optical comparator. Two architectures are proposed and tested in this thesis. The first architecture involves two EDFAs before and after the SOA-PD device: the former EDFA is to amply integrator output to achieve maximum switching speed while the latter EDFA is to amply the binary output power for sufficient feedback. The revised architecture replacing the former EDFA with a SOA and a band pass filter for future integration design. It is demonstrated that the revised all-optical ΣΔ modulator is capable of producing an accurate bit-stream that can be demodulated to recover the input analog signal.

Finally, the system performance is characterized by calculating SNR and ENOB of the disconnected loop. In doing so, the disconnected system is divided into five subsystems: OS, integrator, IA, comparator and CA. Then, the gain of each subsystem is measured to predict the noise power after each subsystem and consequently the SNR and ENOB. The system performs with a SNR of 25.4 dB and has an ENOB of 3.93.

8. REFERENCE

[1] Shoop, B. L. *Photonic Analog-to-Digital Conversion.* New York: Springer, 2001. Print.

[2] Valley, G. C. "Photonic Analog-to-Digital Converters." *Optics Express* 15.5 (2007): 1955-1982. Print.

[3] Shoop, B. L. "A/D Converter Coding Schemes." *Photonic Analog-to-Digital Conversion*. Berlin: Springer, 2001. 29-31. Print.

[4] Shoop, B. L., and J. W. Goodman. "Optical Oversampled Analog-to-Digital Conversion." *Applied Optics* 31.26 (1992): 5654-5660. Print.

[5] Sayeh, M. R., and A. Siahmakoun. "All Optical Binary Delta-Sigma Modulator." Proceedings of SPIE 5970: *Photonic Applications in Devices and Communication System.* Bellingham, WA: SPIE, 2005. Print.

[6] Reeves, E., P. Costanzo-Caso, and A. Siahmakoun. "Photonic Asynchronous First-Order Fiber-Optic Delta-Sigma Modulator." *Microwave and Optical Technology Letters* 54.5 (2012): 1287-1292. Print.

[7] Miller, D. A. B. "Quantum-Well Self-Electro-Optic Effect Devices." *Optical and Quantum Electronics* 22 (1990): S61-S98. Print.

[8] Costanzo-Caso, P., et al. "Optical Bistable Switching with Symmetrically-Configured SOAs in Reverse Bias." *Conference on Lasers and Electro-Optics.* Piscataway, NJ: Institute of Electrical and Electronics Engineers, 2010. Print.

[9] Costanzo-Caso, P., et al. "Optical Bistability in Electrically Coupled SOA-BJT Devices." Proceedings of SPIE 7750: *Photonics North 2010*. Bellingham. WA: SPIE, 2010. Print.

[10] Reeves, E., et al. "Optical A/D Using Oversampling by Second-Order DSM." *Frontiers in Optics 2011*. Washington, D.C.: Optical Society of America, 2011. Print.

[11] Gibbs, H. M. *Optical Bistability: Controlling Light with Light*. Orlando: Academic Press, 1985. Print.

[12] Hoghooghi, N., S. Granieri, and A. Siahmakoun. "Fiber-Optic Hysteretic Quantizer for A/D Conversion." *Frontiers in Optics* . Washington, D.C.: Optical Society of America, 2007. Print.

[13] Maywar, D. N., G. P. Agrawal, and Y. Nakano. "All-Optical Hysteresis Control by Means of Cross-Phase Modulation in Semiconductor Optical Amplifiers." *Journal Optical Society of America B* 18.7 (2001): 1003-1013. Print.

[14] Toifghi, S., et al. "Optical Bistability in Fiber Ring Resonator Containing an Erbium Doped Fiber Amplifier and Quantum Dot Doped Fiber Saturable Absorber." *Applied Optics* 51.29 (2012): 7016-7024. Print.

[15] Siahmakoun, A., Y. Tang, and S. Granieri. "Optical Tunability of Resonant Fabry-Perot Saturable Absorders with Application to Optical Switching." *Topical Meeting on Controlling Light with Light*. Washington, D.C.: Optical Society of America, 2007. Print.

[16] Gibbs, H. M., S. L. MaCall, and T. N. Venkatesan. "Differential Gain and Bistability Using a Sodium-Filled Fabry-Perot Interferometer." *Physical Review Letters* 36.19 (1976): 1135-1137. Print.

[17] Tang, Y, et al. "Optical Bistability in Fabry-Perot Quantum-Well Saturable Absorber." *Frontiers in Optics 2005*. Washington, D.C.: Optical Society of America, 2005. Print.

[18] Miller, D. A. B., D. S. Chemla, and T. C. Damen, "Novel Hybrid Optically Bistable Switch: The Quantum Well Self-Electro-Optic Effect Device. " *Applied Physics* 45.1 (1984): 13-15. Print.

[19] Miller, D. A. B., et al. "Field-Effect Transistor Self-Electro-Optic Effect Device: Integrated Photodiode, Quantum Wel Modulator and Transistor." *IEEE Photonics Technology Letters* 1.3 (1989): 62-64. Print.

[20] Zang, Z. "Numerical Analysis of Optical Bistability Based on Fiber Bragg Grating Cavity Containing a High Nonlinearity Doped-Fiber." *Optics Communications* 285.5 (2012): 521-526. Print.

[21] Notomi, M., et al. "Optical Bistable Switching Action of Si High-Q Photonic-Crystal Nanocavities." *Optics Express* 13.7 (2005): 2678-2687. Print.

[22] Costanzo-Caso, P., et al. "Hybrid Optoelectronic Device with Multiple Bistable Outputs." *Journal of Pysics: Conference Series* 274.1 (2011): 1-11. Print.

[23] Cole, A., et al. "Optical Accumulator for Signal Processing." *OSA Topical Meeting on Information Photonics.* Piscataway, NJ: Optical Society of America, 2005. Print.

[24] Costanzo-Caso, P., A. Siahmakoun, and S. Granieri. "Optical Leaky Integrator with Inverted and Noninverted Accumulation." *Microwave and Optical Technology Letters* 53.9 (2011): 2034-2037. Print.

[25] Jin, Y, et al. "Photonic Inegrator for A/D Conversion." Proceedings of SPIE 7797, *Optics and Photonics for Information Processing IV*. Bellingham, WA: SPIE, 2010. Print.

[26] Carver, S., et al. "Photonic Analog-to-Digital Converter via Asynchronous Oversampling." *Proceedings of SPIE 8397: Enabling Photonics Technologies for Defense, Secuirty, and Aeorspace Applications VIIII*. Bellingham, WA: SPIE, 2012. Print.

[27] Walden, R. "Analog-to-Digital Converter Survey and Analysis." *IEEE Journal on Selected Areas in Communications* 17.4 (1999): 539-550. Print.

[28] Ouzounov, S., et al. "Analysis and Design of High-Performance Asynchronous Sigma-Delta Modulators with a Binary Quantizer." *IEEE. Journal of Solid-State Circuits* 41.3 (2006): 588-596. Print.

[29] Black, B. *Noise and Noise Figure Measurement*. Terre Haute, IN: Rose-Hulman Institute of Technology, 2001. Web. 17 Apl. 2013. <http://www.rose-hulman.edu/~black/Noise/ppframe.htm.>.

[30] *Application Note: Relative Intensity Noise of Distributed Feedback Lasers.* Berlin: Eagleyard Photonics GmbH. Web. 17 Apl. 2013. <http://www.eagleyard.com/fileadmin/downloads/app_notes/App_Note_RIN_1-5.pdf>.

[31] Keiser, G. "Photodetectors." *Optical Fiber Communications*. New York, McGraw-Hill Education, 2008. 231-234. Print.

[32] Lentine, A. L., et al. "Symmetric Self-Electrooptic Effect Device: Optical Setreset Latch, Differential Logic Gate, and Differential Modulator/Detector." *IEEE Journal of Quantum Electronics* 25.8 (1989):1928-1936. Print.

APPENDICES

Appendix A: EIS Potentiostat Analysis

The equivalent circuits of SOA and photo diode are extracted by measuring their impedance. The equipment involved in this measurement is Gamry Reference 600 whose function is to probe the frequency response of the system under test based on Electrochemical Impedance Spectroscopy (EIS) theory. Data extracted from the system is then fitted with an electric model and the impedance of each component is then calculated. Figure A.1 is the Bode plot of measurement of SOA. By fitting an empirical electric model shown in Figure A.2 into these data points, we derived the values of each component:

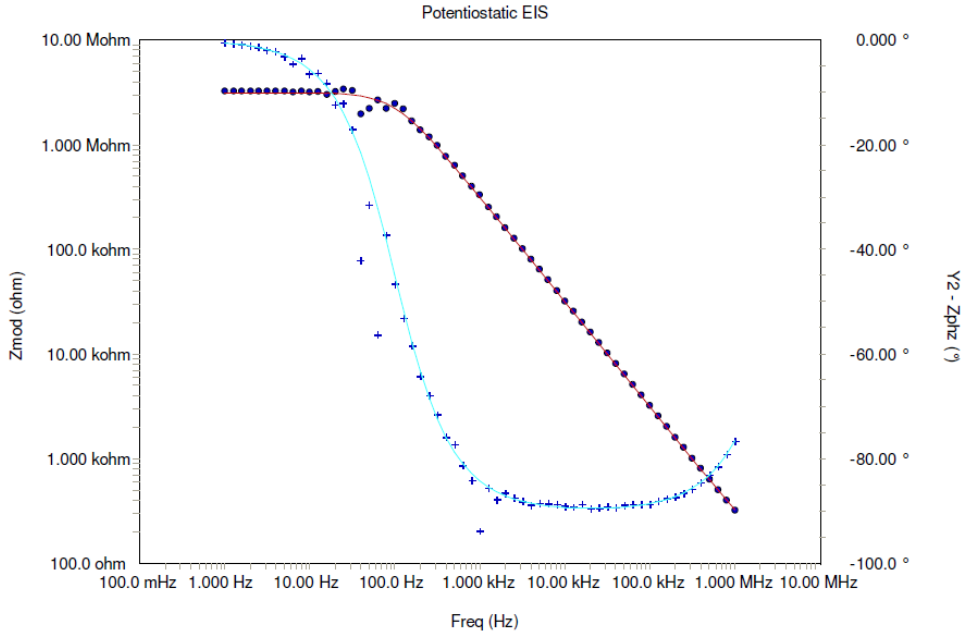

Figure A. 1 Bode Plot of Semiconductor Optical Amplifier (COVEGA SOA 1117), Tested with Gamry Reference 600

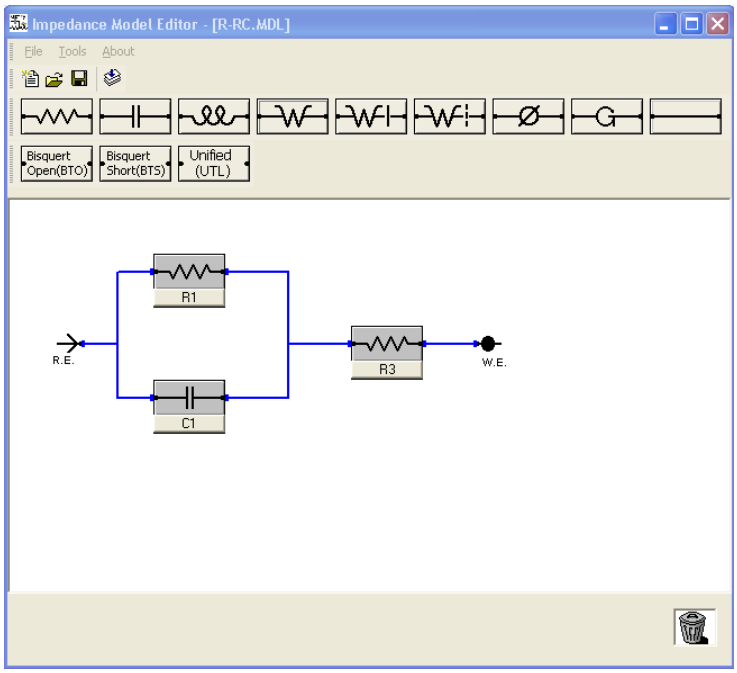

Figure A. 2 Equivalent Circuit of SOA

Results:

Capacitance	C=503.2 ± 2.0 pF
Parallel resistance	R_p=3.15 ± 0.02 MΩ
Series resistance	R_u=75.5 ± 4.9 Ω

Similarly, the impedance of photo diode is also measured. Figure A.3 is the Bode plot of measurement of PD. By fitting an empirical electric model shown in Figure A.4 into these data points.

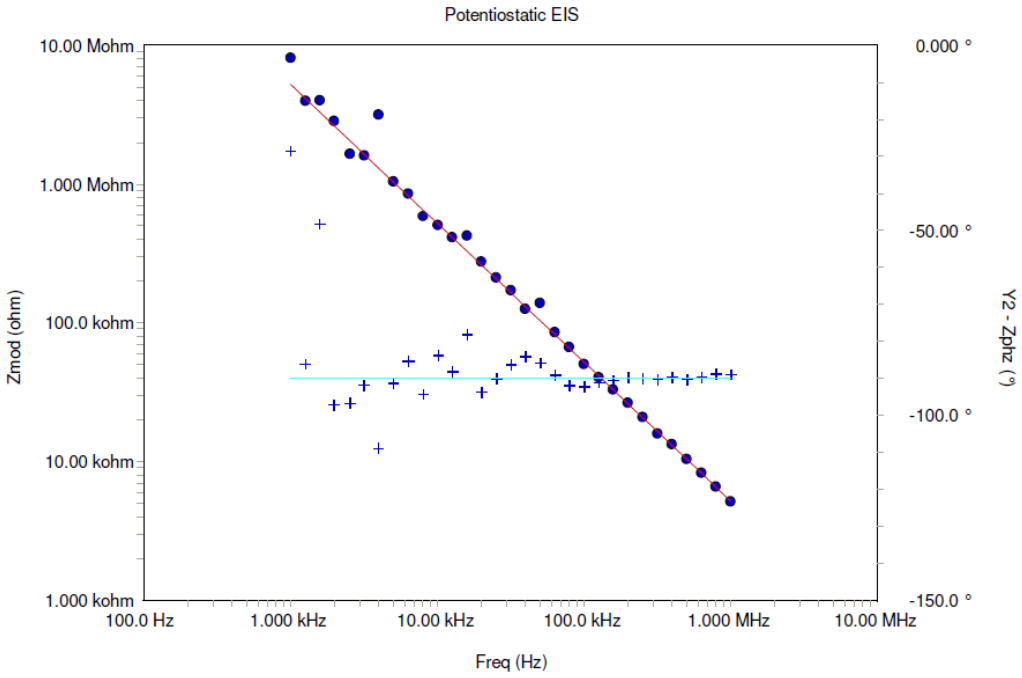

Figure A. 3 Bode Plot of Photo Diode (FID3Z1KX) Tested with Gamry Reference 600

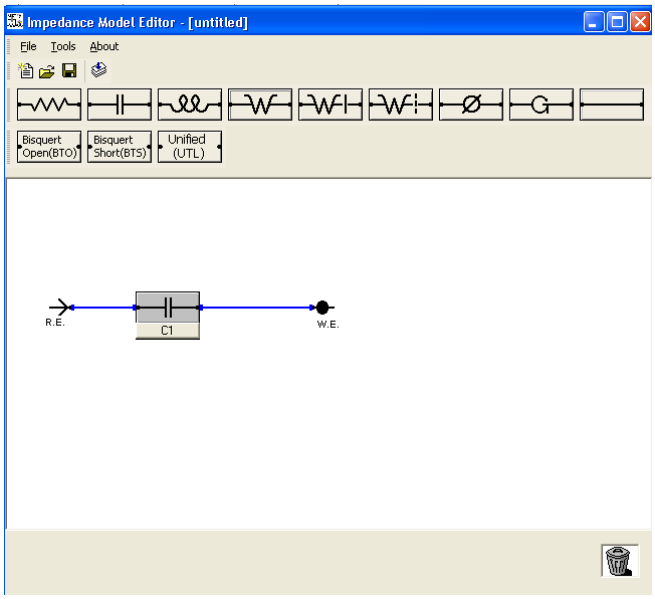

Figure A. 4 Equivalent Circuit of Photo Diode

Results:

Capacitance C=30.4 ± 0.2 pF

Appendix B: Matlab Program for Optical Leaky Integrator

```
%03 21, 2011
%Leaky integrator Implementation - Attempt to Gen. Simulink System
%Edited by B. Zhang

clear
clc
close all

%set sample time and signal frequency
t = (0:0.1:40); %microsecond
f = 0.1; %MHz

%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%define variable parameters%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%
RF_signal_amplitude=0.1;    % g=gain, t=time constant, c=DC offset
RF_signal_offset=0.15;      % applied to signal after integrator,
g1=1;                       % controlled by SOA current
t1=1;                       % microsecond (given by loop length)

%input RF signal
RF_in = RF_signal_amplitude*square(2*pi*f*t) + RF_signal_offset;

%setup integrator and output signal arrangement
int1_out = zeros(size(t));

%integrator transfer function
f1=1/t1;
n1=g1;
d1=[1 f1];
[A,B,C,D] = tf2ss(n1,d1);
syst_ss1=ss(A,B,C,D);

%%%%%%%%%%%%%%%%%%%%%%
%simulate ADC system%
%%%%%%%%%%%%%%%%%%%%%%
for i=1:length(t)-1
   %signal through integrator
   [z1] = lsim(syst_ss1,RF_in,t);
```

```
    %save data point
    int1_out(i) = z1(i);

end


%%%%%%%%%%
%PLOTTING%
%%%%%%%%%%
subplot(2,1,1); plot(t,RF_in,'k')
title ('Input RF Signal','Fontsize',12)
xlabel('Time (\mus)','Fontsize',12)
ylabel('Power (mW)','Fontsize',12)
xlim([0 40])
ylim([-0.09 0.351])

subplot(2,1,2); plot(t(1:end-1), int1_out(1:end-1), 'k')
title('Integrator Output','Fontsize',12)
xlabel('Time (\mus)','Fontsize',12)
ylabel('Power (mW)','Fontsize',12)
xlim([0 40])
```

Appendix C: Matlab Program for All-Optical ΣΔ Modulator

```
%March 21, 2011
%ADC Implementation - Attempt to Gen. Simulink System
%Edited by B. Zhang

clear
clc
close all

%set sample time and signal frequency
t = (0:0.01:40);    %microseond
f = 0.1;            %MHz

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%define variable parameters%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
RF_signal_amplitude=0.5;    % g=gain, t=time constant, c=DC offset
RF_signal_offset=0.5;       % applied to signal after integrator,
g1= 3;                      % number indicates integrator param.
t1=0.4;                     % zh=quantizer on, z1=quantizer off,
zh=1.8;                     % yh=output high, y1=output low
zl=1.2;
yh=2;
yl=0;

%input RF signal
RF_in = RF_signal_amplitude*sin(2*pi*f*t) + RF_signal_offset;

%setup integrator and output signal arrangement
bit_out = ones(size(t));
int1_out = zeros(size(t));

%integrator transfer function
f1=1/t1;
n1=g1;
d1=[1 f1];
[A,B,C,D] = tf2ss(n1,d1);
syst_ss1=ss(A,B,C,D);

%%%%%%%%%%%%%%%%%%%%%
%simulate ADC system%
```

```
%%%%%%%%%%%%%%%%%%%%
for i=1:length(t)-1
   %signal through integrator
   [z1] = lsim(syst_ss1,RF_in+bit_out,t);

   %save data point
   int1_out(i) = z1(i);

   %signal into quantizer
   if z1(i)>=zh
      bit_out(i+1)=yl;    % NEW BOUNDS?
   elseif z1(i) <= zl
      bit_out(i+1)=yh;
   else
      bit_out(i+1)=bit_out(i);
   end
end

% create a 3rd-order LP filter
fs=1/(0.01);
f_cutoff=0.12;
f_norm=f_cutoff/(fs/2);
[b,a] = butter(5, f_norm, 'low');

%filter binary output
demod=filter(b,a,bit_out);

%%%%%%%%%%
%PLOTTING%
%%%%%%%%%%
subplot(5,1,1); plot(t,RF_in,'k')
title ('Input RF Signal')
xlim([10 40])
subplot(5,1,2); plot(t, RF_in+0.45*bit_out, 'k')
title('Error Signal')
xlim([10 40])
subplot(5,1,3); plot(t(1:end-1), int1_out(1:end-1), 'k')
title('Integrator Output')
xlim([10 40])
ylabel('Power (mW)')
subplot(5,1,4); plot(t,bit_out, 'k')
title('Binary Output of ADC')
xlim([10 40])
ylim([-0.5 2.5])
subplot(5,1,5); plot(t, demod, 'k')
title('Demodulated Binary Output')
```

```
xlim([10 40])
xlabel('Time (\mus)')
```

Appendix D— Component

1. Fujistu FLD5F10NP 5mW EAM-Laser

Parameter	Symbol	Value	Unit
Peak Oscillation wavelength (at 20°C)	λ_p	1553.3	nm
Threshold current	I_{th}	15	mA
Side mode suppression ratio	SMSR	>35	dB
Cutoff frequency	fc	>10	GHz
Relative Intensity Noise	RIN	< -120	dB/Hz

2. Alcatel 1905 LMI CW-Laser

Parameter	Symbol	Value	Unit
Peak Oscillation wavelength (at 10kΩ)	λ_p	1551.7	nm
Threshold current	I_{th}	6	mA
Side mode suppression ratio	SMSR	>40	dB
Spectral width	$\Delta\lambda$	3	MHz
Relative Intensity Noise	RIN	< -140	dB/Hz

3. Covega SOA 1117 (Series No. 5901 and 5902)

Parameter	Symbol	Min	Typ	Max	Unit
Operating current	I_{op}		500	600	mA
Operating Wavelength	λ	1528		1562	nm
Saturation output power	Psat	6	9		dBm
Small signal gain	G	15	20		dB
Gain ripple	ΔG		0.2	0.5	dB
Noise Figure	NF		9	11	dB

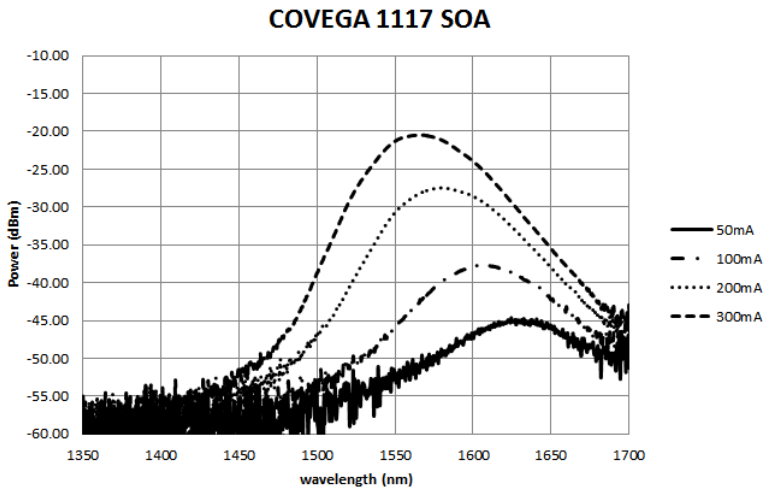

Figure A. 5 Spontaneous Emission Spectra of COVEGA 1117 SOA Changing with Driving Current

4. Kamelian SOA OPA-10-N-C-FP

Parameter	Symbol	Min	Typ	Max	Unit
Operating current	I_{op}		200	250	mA
Saturation output power	P_{sat}	10	11		dBm
Small signal gain	G	20			dB
Gain ripple	ΔG		0.3	0.5	dB
Noise Figure	NF		6	7	dB

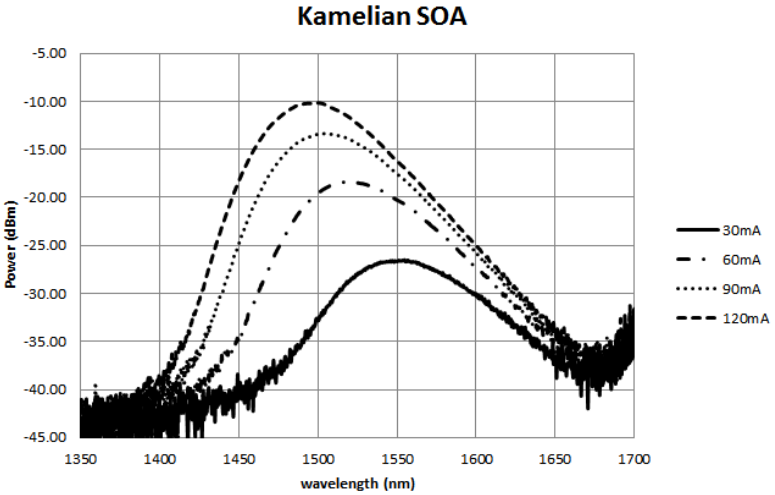

Figure A. 6 Spontaneous Emission Spectra of Kamelian SOA Changing with Driving Current

5. IPG Photonics EDFA EAD-500-CL

Parameter	Symbol	Value	Unit
Output Bandwidth	B	1540-1605	nm
Nominal saturated power (Pin=3dB, 1590nm)	P_{sat}	27	dBm
Output power instability	-	<0.3	%
Noise figure	F	6.5	dB
Pump wavelength	λp	965	nm

6. Eudyna FID3Z1KX Photo Diode

Parameter	Symbol	Min	Max	Unit
Responsivity (at 1500nm)	R	0.8	-	A/W
Variation of responsivity	ΔR		±3	%
Dark current (VR=5V, T=25°C)	I_d	-	1	nA
Cut-off frequency	f_c	2.5		GHz
Capacitance (f=1MHz, VR=5V)	C		0.9	pF

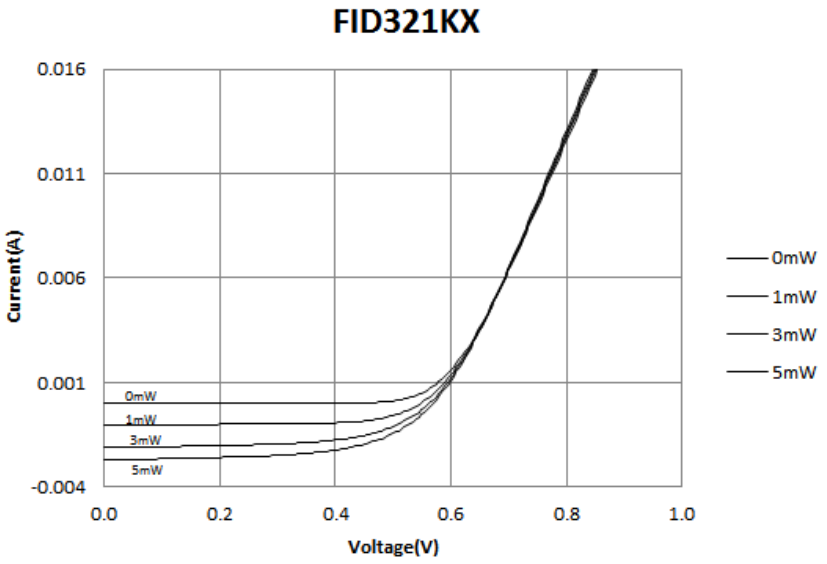

Figure A. 7 V-I Curves at Different Input Powers

7. Tunable Band Pass Filter (JDS TB45BT1SC)

Parameter	Symbol	Value	Unit
Center wavelength	λc	1555.6	nm
3 dB bandwidth	FWHM	±0.20	nm

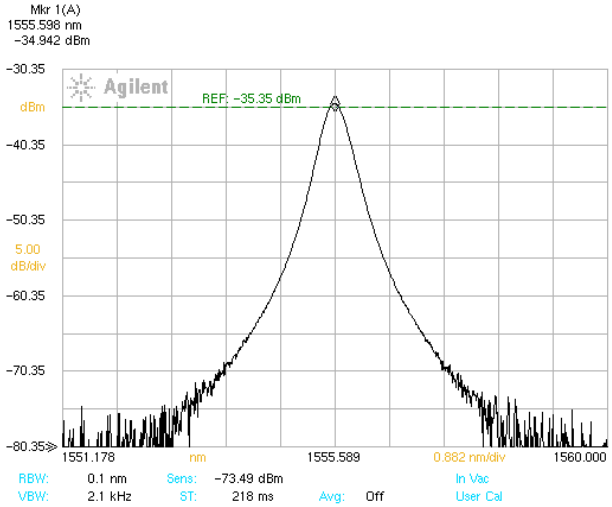

Figure A. 8 Spectrum of JDS TB45BT1SC

8. Tunable Band Pass Filter (Dicon TF-1500-0.8-9/TB-FC/A-1)

Parameter	Symbol	Value	Unit
Center wavelength	λc	1555.6	nm
3 dB bandwidth	FWHM	±0.65	nm

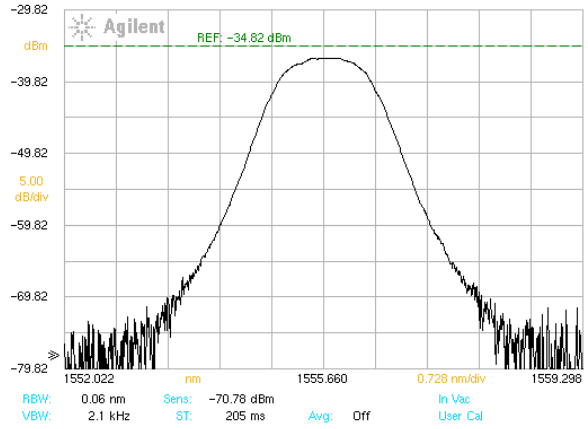

Figure A. 9 Spectrum of JDS Dicon TF-1500-0.8-9/TB-FC/A-1

9. Band Pass Filter (Dicon 30A14G000300)

Parameter	Symbol	Value	Unit
Center wavelength	λc	1551.7	nm
3 dB bandwidth	FWHM	±0.35	nm

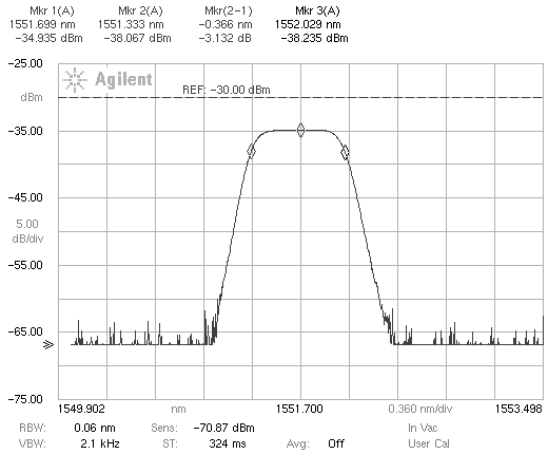

Figure A. 10 Spectrum of JDS Dicon 30A14G000300

Appendix E: FTT Analysis of Binary Output

```
 % Photonic ADC Performance Characteristic Solver
% By Bin Zhang
% Based off work done by Spencer Carver

clear all
clc
close all

%%%%%%%%%%%%%
% SET VALUES %
%%%%%%%%%%%%%

file_name = 'data_analysis/print_01.csv';

frequency = 1.0*10^4;  % The frequency the trial was run with.
% If the trial uses a combined waveform, this is the frequency
% of the largest component

filter_order = 3;  % Do not change

cutoff_frequency = 8*10^4;
% cutoff frequency must be 6.9*10^6 for breadboard comparator
% cutoff frequency must be ___*10^6 for PCB comparator
% cutoff frequency must be 8.33*10^6 for high-gain low-bandwidth comparator

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% DO NOT MODIFY THIS PORTION %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

read_data=csvread(file_name, 2, 0);
input_data=read_data(:,[1,2,3]);

Time=(input_data(:,1));
sine = (input_data(:,2));
input=(input_data(:,3));

avgin = mean(input);
for i=1:length(input)
   input(i) = input(i)-avgin;
end
```

```
Ts=Time(2)-Time(1);
Fs=(1/Ts);
L=length(input_data);

f_cutoff_demod= frequency + 0.2*10^4; % Demodulation frequency can be close to actual
f_cutoff=cutoff_frequency;
f_norm_demod=f_cutoff_demod/(Fs/2);
f_norm=f_cutoff/(Fs/2); % normalized cutoff frequency
[d,c]=butter(filter_order,f_norm_demod,'low');
[b,a]=butter(filter_order,f_norm,'low'); % low pass Butterworth filter of order
filter_data=filtfilt(b,a,input); % filtering
filter_data_demod=filtfilt(d,c,input);

f_nyquist=Fs/2;
x=f_nyquist*linspace(0,1,L/2+1)/1000000;

y=(fft(filter_data))/(L);

y=abs(y(1:end));y(2:end)=sqrt(2)*y(2:end);
y2 = 20*log10(y);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Truncate data based on cutoff frequency%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
indmax = 0;
for i=1:length(x)
    if x(i)*1000000 >= f_cutoff
        indmax = i;
        break
    end
end

%%%%%%%%%%%%%%%%%%%%%%%%%
%Evaluate Vsig & Vspur%
%%%%%%%%%%%%%%%%%%%%%%%%%
Vsig = realmin;
indVsig = 0;
Vspur = realmin;
indVspur = 0;
for i=1:indmax
    val = y(i);
    if val > Vspur
        if val > Vsig
            Vspur = Vsig;
            Vsig = val;
```

```
            indVspur = indVsig;
            indVsig = i;
        else
            Vspur = val;
            indVspur = i;
        end
    end
end

%%%%%%%%%%%%%
%Convert to dB%
%%%%%%%%%%%%%
Vsig = 20*log10(Vsig);
Vspur = 20*log10(Vspur);

%%%%%%%%%%%%%%%%%%%%%%%%
%Evaluate Vnoise & Vn+d%
%%%%%%%%%%%%%%%%%%%%%%%%
Vnoise = 0;
Vnd = 0;
lengthVnoise = 0;
lengthVnd = 0;
for i=2:indmax
    val = y(i);
    if i == indVsig
        % do nothing
    elseif x(i) == 3*x(indVsig)
        V3 = y(i);
    elseif rem(x(i),x(indVsig)) == 0
        Vnd = Vnd + val;
        lengthVnd = lengthVnd + 1;
    else
        Vnoise = Vnoise + val;
        Vnd = Vnd + val;
        lengthVnd = lengthVnd + 1;
        lengthVnoise = lengthVnoise + 1;
    end
end

Vnoise = Vnoise / lengthVnoise;
Vnd = Vnd / lengthVnd;

%%%%%%%%%%%%%
%Convert to dB%
%%%%%%%%%%%%%
Vnoise = 20*log10(Vnoise);
```

```
Vnd = 20*log10(Vnd);
% V3 = 20*log10(V3);
% IP3 = (3*Vsig - V3)/2;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Evaluate SNR, SINAD, ENOB, & SFDR%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
SNR = Vsig - Vnoise;
SINAD = Vsig - Vnd;
ENOB = (SINAD - 1.76)/6.02;
SFDR = Vsig - Vspur;

%%%%%%%%%%%%%%%%%
%Display Results%
%%%%%%%%%%%%%%%%%
figure          % Demodulation
subplot(3,1,1),plot(Time,sine),title('Input');
xlim([Time(200) Time(1800)])
ylim([min(sine) max(sine)])
subplot(3,1,2),plot(Time,input),title('Output data');
xlim([Time(200) Time(1800)])
subplot(3,1,3),plot(Time,filter_data_demod),title('Demodulated data');
xlim([Time(200) Time(1800)])
ylim([min(filter_data_demod(200:1800)) max(filter_data_demod(200:1800))])

figure          % FFT Analysis
subplot(2,1,1),plot(x(1:100),y(1:100)),title('Filtered Output (mV)');
xlim([0 0.2])
subplot(2,1,2),plot(x(1:100),y2(1:100)),title('Filtered Output (dB)');
xlim([0 0.2])

disp(['Vsig = ', num2str(Vsig), ' dB']);
disp(['Vspur = ', num2str(Vspur), ' dB']);
disp(['Vn+d = ', num2str(Vnd), ' dB']);
disp(['Vnoise = ', num2str(Vnoise), ' dB']);
disp(' ')
disp(['SNR = ', num2str(SNR), ' dB']);
disp(['SINAD = ', num2str(SINAD), ' dB']);
disp(['ENOB = ', num2str(ENOB), ' bits']);
disp(['SFDR = ', num2str(SFDR), ' dB']);
disp(' ')
disp(['IP3 = ', num2str(IP3), ' dB']);
disp(' ')
disp('NOTE: All final values are approximate and dependant upon errors');
disp('      which stem from the first set of calculated values');
```

Appendix F: Program for Noise Analysis

Input signal power P1 is in dB, P11 is in mW

> *restart*

> $k := 1.38 \cdot 10^{-23}$

$$k := 1.380000000\,10^{-23}$$

> $T := 293$

$$T := 293$$

> $q := 1.6 \cdot 10^{-19}$

$$q := 1.600000000\,10^{-19}$$

EAM-Laser RIN

> $B := 10000$

$$B := 10000$$

Hz

> $P1 := -13.6$

$$P1 := -13.6$$

dBm

> $P11 := 10^{\left(\frac{P1}{10}\right)}$

$$P11 := 0.04365158322$$

mW

> $RIN1 := -120$

$$RIN1 := -120$$

dB/Hz

> $RIN11 := 10^{\frac{RIN1}{10}}$

$$RIN11 := \frac{1}{1000000000000}$$

Hz^-1

> $RIN11 := RIN11 \cdot B$

$$RIN11 := \frac{1}{100000000}$$

unit

> $fluctuation1 := evalf(\mathrm{sqrt}(RIN11) \cdot P11)$

$$fluctuation1 := 0.000004365158322$$

in mW

Integrator

Gain: 11.5 dB

Noise figure: 9 dB

> $G1 := 11.5$

$$G1 := 11.5$$

> $G11 := 10^{\left(\frac{G1}{10}\right)}$

$$G11 := 14.12537545$$

> $F1 := 9$

$$F1 := 9$$

> $F11 := 10^{\left(\frac{F1}{10}\right)}$

$$F11 := 10^{9/10}$$

> $P2[2, out] := G11 \cdot P11$

$$P2_{2,\,out} := 0.6165950020$$

mW

> $P2[2, noise] := evalf(k \cdot T \cdot G11 \cdot B \cdot F11 + 0.001 \cdot G11 \cdot fluctuation1)$

$$P2_{2,\,noise} := 6.165950474\,10^{-8}$$

W

> $P[2, out] := evalf(10 \cdot \log[10](P2[2, out]))$

$$P_{2,\,out} := -2.099999999$$

dBm

Integrator amplifier

Gain: 11.6dB

Noise figure : 6 dB

> $G2 := 11.6$

$$G2 := 11.6$$

dB

> $G22 := 10^{\frac{G2}{10}}$

$$G22 := 14.45439771$$

> $F2 := 6$

$$F2 := 6$$

dB

> $F22 := 10^{\frac{F2}{10}}$

$$F22 := 10^{3/5}$$

> $P3[3, out] := \text{evalf}(\text{G22} \cdot \text{P2}[2, out])$

$$P3_{3,\,out} := 8.912509385$$

mW

> $P3[3, noise] := evalf(k \cdot T \cdot G22 \cdot B \cdot F22 + G22 \cdot P2[2, noise])$

$$P3_{3,\,noise} := 8.91251006\,4\,10^{-7}$$

W

> $P[3, out] := evalf(10 \cdot \log[10](P3[3, out]))$

$$P_{3,\,out} := 9.500000002$$

dBm

Comparator

Responsivity: 0.8 A/W

reciever bandwidth: 2.5 GHz

dark current: 1 nA

Resistance: 3.15 Mohm

> $R := 0.8$

$$R := 0.8$$

> $Be := 2.5 \cdot 10^{9}$

$$Be := 2.500000000\,10^{9}$$

> $Ip := R \cdot 0.001 \cdot P3[3, out]$

$$Ip := 0.007130007508$$

A

> $shotnoise := 2 \cdot q \cdot Ip \cdot Be$

$$shotnoise := 5.704006004\,10^{-12}$$

A^2

> $inoise := R \cdot P3[3, noise]$

$$inoise := 7.130008051\,10^{-7}$$

A

> $Id := 10^{-9}$

$$Id := \frac{1}{1000000000}$$

A

> $idark := 2 \cdot q \cdot Id \cdot Be$

$$idark := 8.000000000\,10^{-19}$$

in A^2

> $Rl := 3.15 \cdot 10^{6}$

$$Rl := 3.15000000\,10^{6}$$

> $thermalnoise := \frac{4 \cdot k \cdot T \cdot Be}{Rl}$

$$thermalnoise := 1.283619048\,10^{-17}$$

A^2

> $itotal := \mathrm{sqrt}(shotnoise + inoise^{2} + idark + thermalnoise)$

$$itotal := 0.000002492466607$$

in A

P4 is CW laser power

Vr=-2V

SOA Gain: -33.67dB

> $G3 := -33.167$

$$G3 := -33.167$$

dB

> $G33 := 10^{\frac{G3}{10}}$

$$G33 := 0.0004822808304$$

> $Vr := 2$

$$Vr := 2$$

V

> $P4 := 2.6$

$$P4 := 2.6$$

dBm

> $P44 := evalf\left(10^{\frac{P4}{10}}\right)$

$$P44 := 1.819700859$$

mW

> $P4[4, out] := G33 \cdot P44$

$$P4_{4,\,out} := 0.0008776068414$$

mW

> $P4[4, noise] := G33 \cdot itotal \cdot Vr$

$$P4_{4,\,noise} := 2.404137730\,10^{-9}$$

W

> $P4[4, signal] := P4[4, out] - 1000 \cdot P4[4, noise]$

$$P4_{4,\,signal} := 0.0008752027037$$

mW

> $P[4, out] := 10 \cdot \log[10](P4[4, out])$

$$P_{4,\,out} := -30.56700000$$

Comparator amplifier EDFA

> $G4 := 33.67$

$$G4 := 33.67$$

dB

> $G44 := 10^{\frac{G4}{10}}$

$$G44 := 2328.091258$$

> $F4 := 6.5$

$$F4 := 6.5$$

in dB

> $F44 := 10^{\frac{F4}{10}}$

$$F44 := 4.466835922$$

> $P5[5, out] := \text{evalf}(G44 \cdot P4[4, out])$

$$P5_{5,\,out} := 2.043148815$$

in mW

>

> $P5[5, noise] := 1000 \cdot evalf(k \cdot T \cdot G44 \cdot B \cdot F44 + G44 \cdot P4[4, noise])$

$$P5_{5,\,noise} := 0.005597052452$$

in mW

> $P[5, out] := evalf(10 \cdot \log[10](P5[5, out]))$

$$P_{5,\,out} := 3.103000001$$

in dBm

> $P[5, noise] := 10 \cdot \log[10](P5[5, noise])$

$$P_{5,\,noise} := -22.52040623$$

in dBm

> $P5[5, signal] := P5[5, out] - P5[5, noise]$

$$P5_{5,\,signal} := 2.037551763$$

in mW

> $P[5, signal] := 10 \cdot \log[10](P5[5, signal])$

$$P_{5,\,signal} := 3.091086506$$

SNR and ENOB

> $SNR := P[5, signal] - P[5, noise]$

$$SNR := 25.61149274$$

in dB

> $ENOB := \frac{(SNR - 1.76)}{6.02}$

$$ENOB := 3.962041983$$

bits