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# Fabrication and Characterization of Edge-Emitting Semiconductor Lasers

A Thesis

Submitted to the Faculty

of

Rose-Hulman Institute of Technology

by

Junyeob Song

In Partial Fulfillment of the Requirements for the Degree

of

Master of Science in Optical Engineering

May 2014

**ROSE-HULMAN INSTITUTE OF TECHNOLOGY**

**Final Examination Report**

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# ABSTRACT

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May 2014

Fabrication and Characterization of Edge-Emitting Semiconductor Lasers

Dr. Paul O. Leisher

The semiconductor laser was invented in 1962, and has recently become ubiquitous in modern life. This thesis focuses on the development of a semiconductor laser fabricating process which utilizes semiconductor manufacturing technology in a cleanroom environment including photolithography, etching, deposition, and bonding processes. A photomask for patterning is designed, recipes of photolithography process and etching process are developed with experiments. This work gives how to develop the process of fabrication and determine the parameters for each processes. A series of semiconductor laser devices are then fabricated using the developed process and characterization is performed to assess device performance with industrial standard methods. A fabricated device has 18W power and 11% conversion efficiency.

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# 1. INTRODUCTION

## 1.1 Motivation

The semiconductor laser was invented in 1962, and has recently become ubiquitous in modern life. This laser has many benefits, including simple fabrication, small physical size, high efficiency, high-speed output, compatibility with high-speed modulation, stable operation, and a long lifetime. Because of these properties, it has numerous applications in the areas of optical communications, laser printing, laser pointers, spectroscopy, laser video and other types of display, and medicine. These advantages make edge-emitting lasers the standard for the telecommunications industry, which demands these properties for high speed data transmission.

At its core, the semiconductor laser is a Light Amplifier by Simulated Emission of Radiation (LASER) in a semiconductor pn junction diode. The semiconductor laser is the most compact of all kinds of lasers and can be mass-produced using standard semiconductor wafer manufacturing process at low cost. Most modern communication systems are based on optical fiber communication utilizing semiconductor lasers as the source. Other applications include laser mice, laser printers, displays, and medical equipment.

There are two fundamental classes of semiconductor lasers: edge-emitting lasers (horizontally-emitting lasers), and surface-emitting lasers (vertical-emitting lasers) [1]. Edge-emitting lasers were the first to be developed and are, therefore, the most mature form of the technology. In edge-emitting lasers, the light propagates parallel to the semiconductor wafer surface (in-plane with vertical-grown of epitaxial layers). The edge-

emitting laser has several advantages including simple fabrication, high output power, high efficiency, and compatibility with high speed modulation. These advantages make edge-emitting lasers the standard for the telecommunication industry which demands these properties for high speed data transmission. Other applications which leverage these properties include diode-pumped solid-state and fiber lasers, optical sensing, and free space (point-to-point) communication.

## 1.2 Semiconductor Laser Diodes

Electrically, the semiconductor laser diode is a pn junction diode. Figure 1 shows a cross-sectional view of the laser diode having an anode and cathode to allow injection of current into the intrinsic layer (i-layer) active region [2]. The current blocking layer confines the injected current to maximize stimulated emission. The longitudinal cross-section of the laser diode is shown in Figure 2. Optical gain is provided by radiate recombination of electrons and holes in the i-layer, and the light wave is amplified as it travels back and forth in the resonator. Cavity resonance is provided by cleaved facets at the ends of the chip, and this structure is called a Fabry-Perot resonator [3].

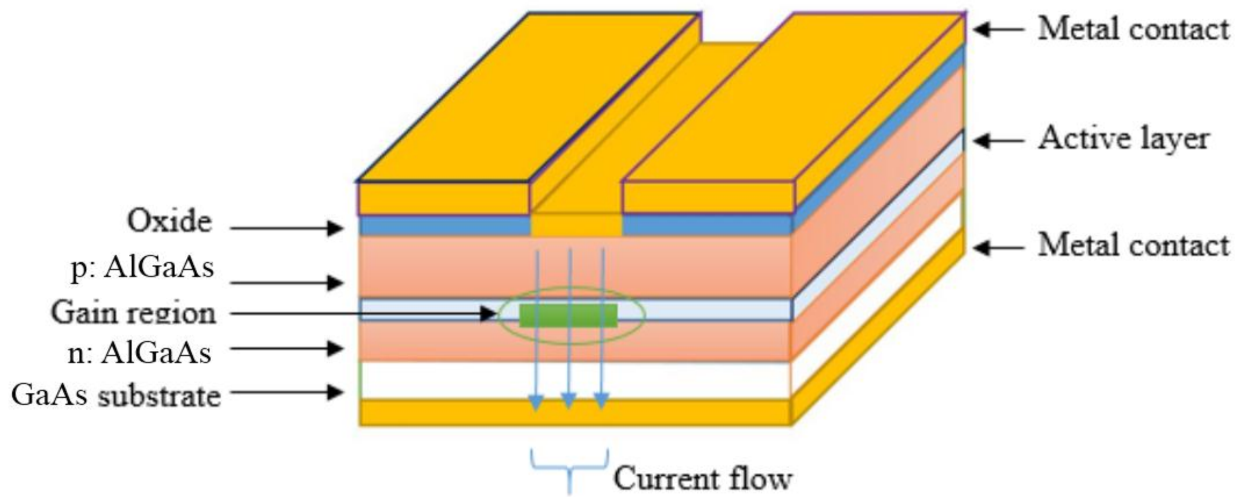



**Figure 1 Schematic cross-sectional views of a semiconductor laser diode along the lateral direction**

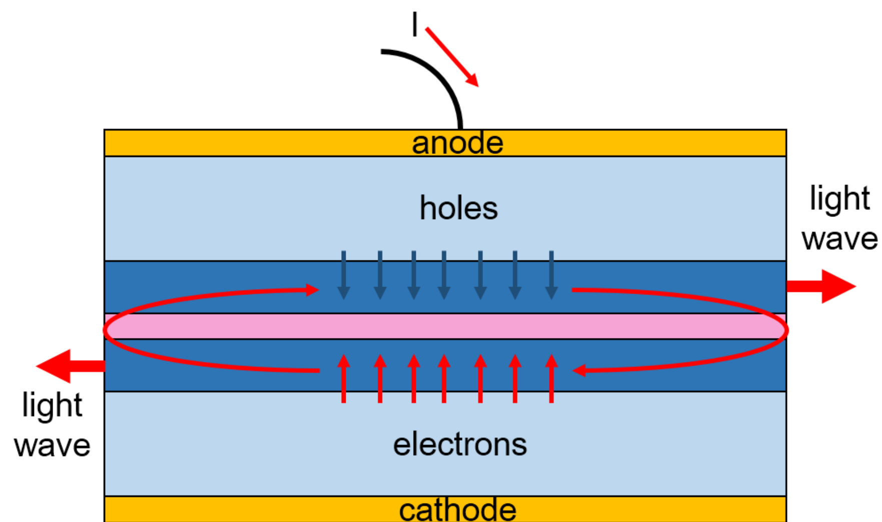



**Figure 2 Schematic cross-sectional views of a semiconductor laser diode along the longitudinal direction**

In the active region of the laser, three important interactions between photons and electrons can occur – absorption, spontaneous emission, and stimulated emission [4][5].

To achieve optical gain, the probability of stimulated emission must be greater than probability of absorption, which is called population inversion. To achieve population inversion, a forward bias voltage greater than the band gap energy of the active region is applied to the pn junction. When optical gain is greater than optical absorption, light wave in the resonator is amplified [6].

In order to describe the onset of laser action, all optical loss in the cavity should be considered. The light wave traveling in the resonator has several possible ways to lose photons. At the threshold point, the number of photons lost in one complete roundtrip from the facets or due to the waveguide loss equals the roundtrip gain.

The laser beam of an edge-emitting laser is guided in the growth direction by a waveguide structure. Normally, this uses a double hetero (DH) structure which is formed by sandwiching a narrow bandgap material between a wider band gap material [7]. The semiconductor laser has a p-i-n diode structure. An intrinsic semiconductor is added between p-type and n-type semiconductor materials. This confines injected carriers to a narrow region and at the same time serves as a waveguide for the optical mode.

The adoption of the DH structure made a significant contribution to the improvement in semiconductor laser efficiency. Referring to Figure 3, when a forward bias is applied to this structure, the electrons from the n-type semiconductor move into the intrinsic semiconductor section where the energy bandgap is low [8][9]. Holes from the p-type semiconductor move into the intrinsic semiconductor as well [10]. This structure improves quantum efficiency by localizing the electrons and holes in the intrinsic region, increasing the probability that they will find one another and recombine radiatively. The refractive index of the DH structure in the active region is also greater,

which causes the optical mode to localize in the same vicinity. The active region in the DH structure thus serves as a waveguide and maximizes stimulated emission. Further improvement is made by inserting a thin quantum well or multiple quantum well structures into the waveguide [11]. The quantum well improves the performance of the device by reducing the transparency current which lowers threshold current and improves temperature performance, and modulation [12]. Multiple epitaxial layers composed of materials having different band gaps are used to form the DH structure. Semiconductor materials can be epitaxial grown on top of one another, provided the lattice constants are similar. The epitaxial design of laser diodes is critical to the performance of such devices. The detail of epitaxial design however, lie beyond the scope of this thesis.

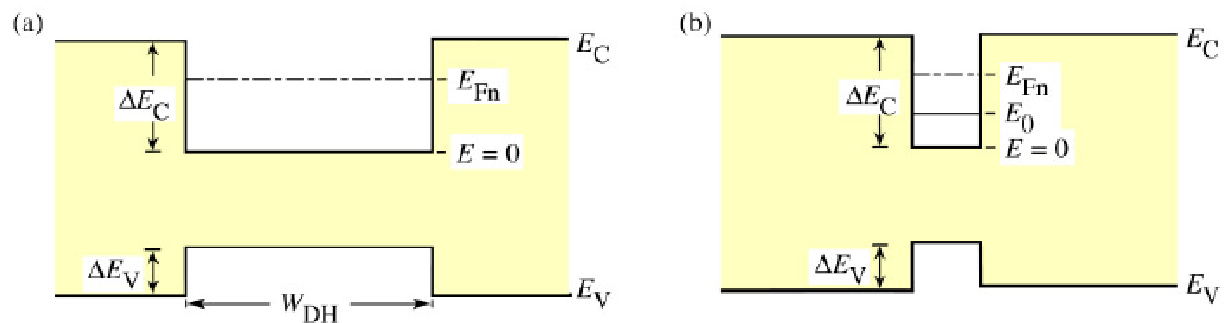



**Figure 3 Illustration of energy diagram of (a) double hetero structure and (b) a quantum well structure**

To improve the efficiency of semiconductor lasers, several structures have been researched. The separate confinement heterostructure (SCH) is one method to achieve better efficiency [13]. Figure 4 shows the development of active region structure of laser diode [14]. This design allows to confine carriers by adjusting the thicknesses and index of refractions with inner layers and outer cladding layers [15].

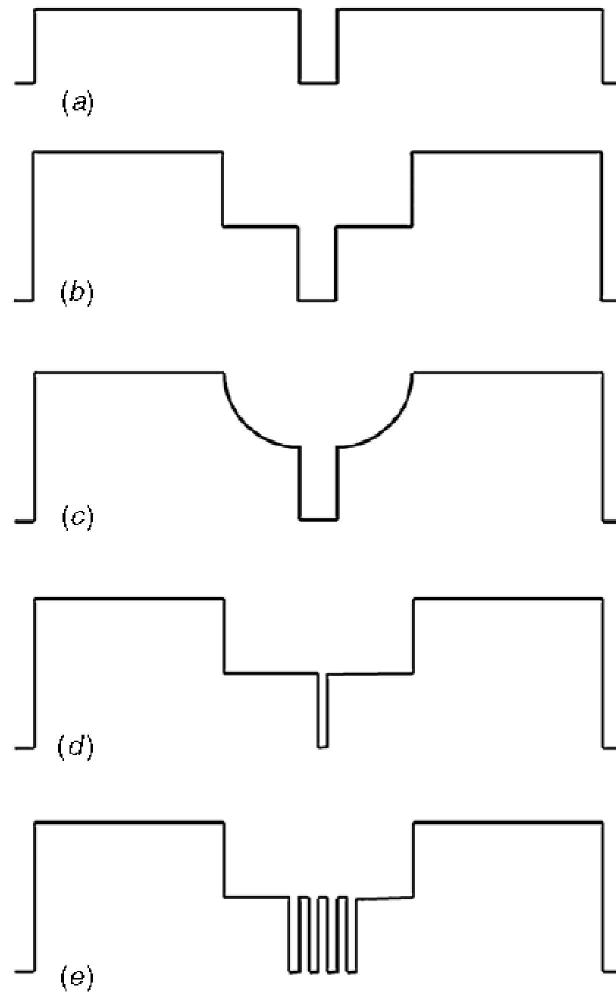



**Figure 4 Schematic diagrams depicting the evolution of the conduction band structure in the transverse direction: (a) double heterostructure, (b) separate confinement heterostructure (SCH), (c) graded-index separate confinement hetero structure(GRIN-SCH), (d) single quantum well hetrostructure (QWH), and (e) multiple quantum well (MQW)**

1.3 Semiconductor Fabrication Device Structure

In general, the first step of the fabrication of a semiconductor laser is growth of the epitaxial layer. Epitaxy means the growth of a single crystal film on top of a crystalline substrate. The design of epitaxial layer depends on the conduction band structure mentioned in the previous chapter. Appendix A shows the epitaxial design used for this thesis work. It is grown by Metal Organic Chemical Vapor System (MOCVD) equipment.

To limit the stripe width of a laser, a structure like Figure 5 is used. [14] The thin film of $SiO_2$ is deposited on a laser structure and it is etched as a narrow stripe. A metallic contact is deposited on the film and the film insulates and confines the current within the stripe width. Injection current is easily confined by changing the stripe width.

There are two categories to define lateral electrical and optical confinement. One is a 'gain guided' structure as shown in Figure 6. It only confines charge carriers, not photons. Advantages of this structure are simple fabrication and achievement of very high power. Disadvantages are many modes and filamentation.

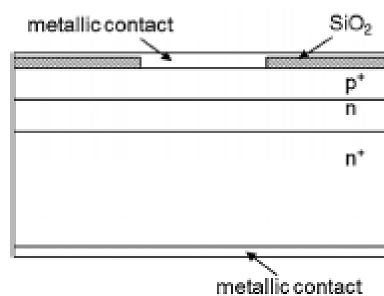



**Figure 5 Schematic diagram of an oxide defined stripe geometry**

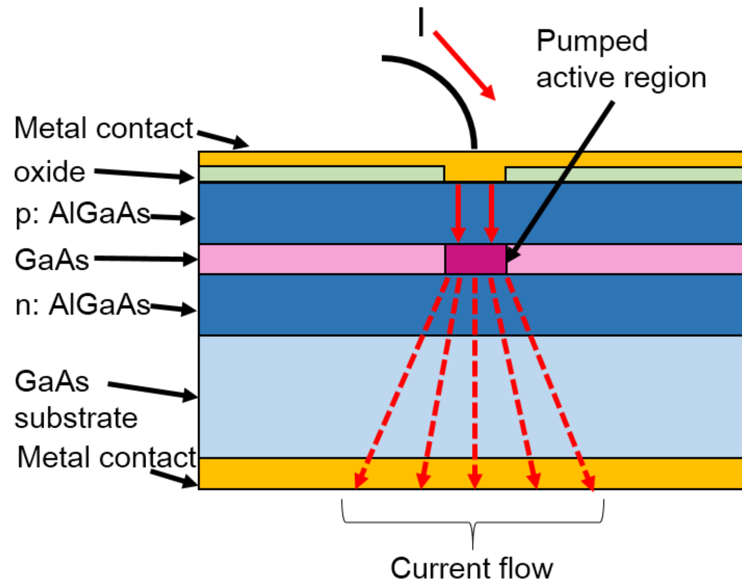



**Figure 6 Illustration of an edge-emitting diode structure**

The other is a 'index guided' structure. It confines photon via refractive index variation; surround cavity with lower index. It can be designed index contrast such that only a single transverse/lateral mode propagation. A disadvantage of this structure is difficult fabrication complexity. To design these lateral wave guide structure, two specific index guided designs are widely used in the commercial market for a laser diode. Figure 7(a) shows one design called buried hetero structure (BH) laser. After the stripe is etched, another layer, having lower refractive index and higher bandgap energy, is grown to bury the active layer. The injection current is effectively confined to the central stripe. Figure 7(b) shows the ridge waveguide laser. Lowering transverse index profile outside the stripe, the lateral index reduction is occurred. [14] These structures are formed by photolithography processes and etching processes in this work. Figure 8 shows a sample of scanning electron microscope picture of these structures [12] [17].

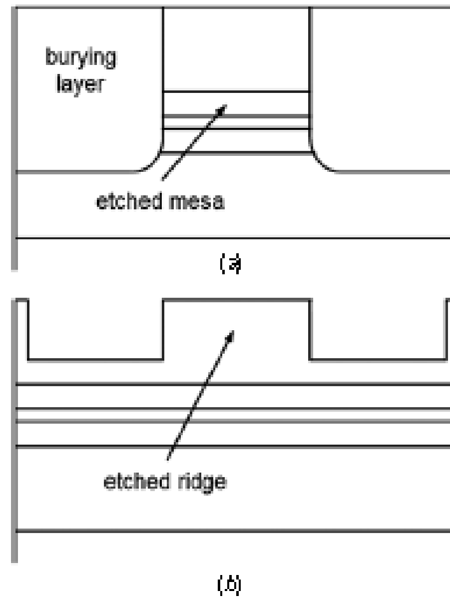



**Figure 7 Schematic drawings of (a) the buried heterostructure (BH) laser and (b) the ridge waveguide laser**

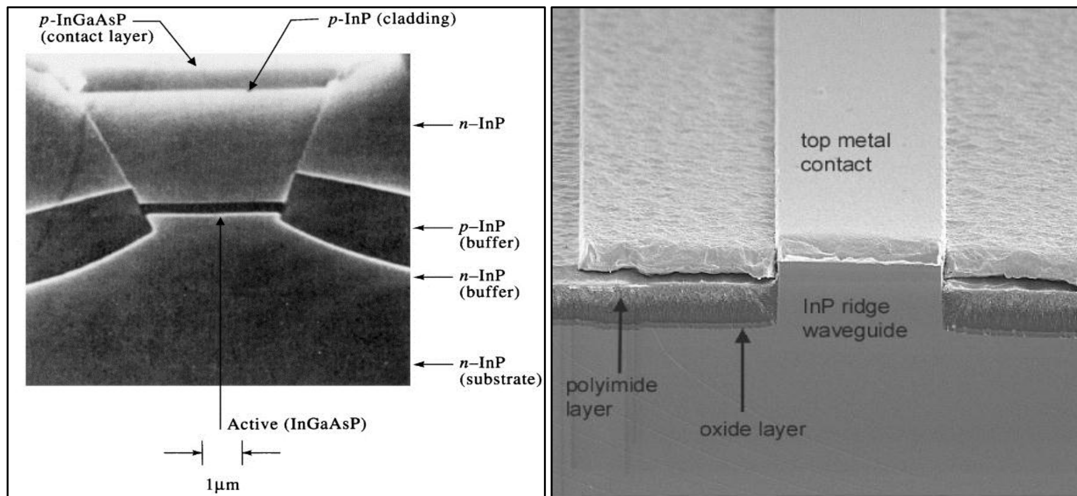



**Figure 8 Sample SEM picture buried heterostructure laser (left) and ridge waveguide laser (right)**

In addition to this, thinning of the substrate wafer is needed for reducing series resistance. All gold deposited for contact and bonding.

1.4 Epitaxial layer

The standard structure for high power semiconductor lasers requires a quantum well, waveguide, and cladding as shown in Figure 9.

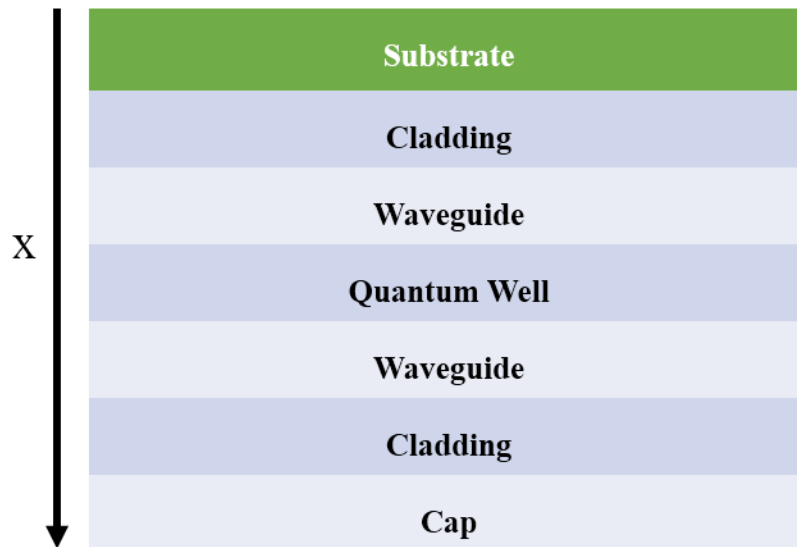



**Figure 9 The epitaxial structure for high power semiconductor laser**

The Figure 10 shows the energy band diagram and refractive index of each layer as function of x. In the figure, the cladding has a high and wide band gap, the waveguide is a lower energy bandgap and the quantum well is energy bandgap is even lower. The purpose of the waveguide and cladding layers is to control the optical mode. This occurs because refractive indices of each layer is related to 1/Eg, and the index profile is illustrated in Figure 10. Electrons enter the active region from the n-side and holes from the p-side. These carriers get trapped in the quantum well and recombined.

In an electrical (Si or GE) diode, diffusion current is primarily responsible for current flow in the biased pn junction. In a LED of laser diode, recombination current dominates. This recombination occurs in the active region and is responsible for light generation. The waveguide is not strictly necessarily for laser operation. The dotted trend

in the refractive index profile shows that the quantum well alone can serve to confine light. In such a device however, a difficulty arises in separately engineering the carrier and light confinement. In other words, changing the quantum well thickness changes both the electronic and photonic confinement. By separating the electron and photon confined, an SCH structure provides independent parameters in the form of the waveguide and quantum well, giving us additional design degrees of freedom. The cladding serves the same purpose as that in a fiber optic cable, it is required for optical confinement due to total internal reflection.

The purpose of the cap is to prevent oxidation of the surface, and the purpose of the substrate is to have a semiconductor structure to grow on it.

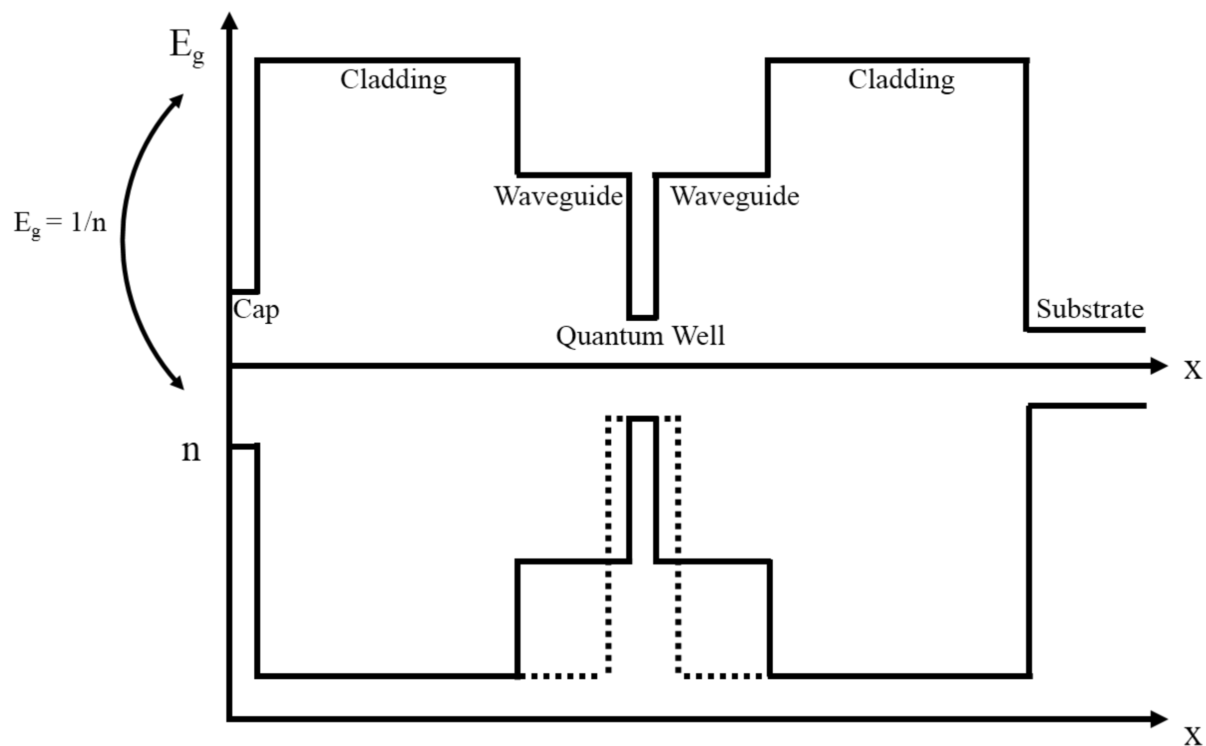



**Figure 10 The diagram of energy bandgap and refractive index for the epitaxial structure**

## 1.5 Rate equations

In this section, the rate equations which describe the physical operation of semiconductor lasers will be discussed. The two coupled equations are the standard rate equations for the photon density and the carrier density as shown in Equations 1.1 and 1.2 [16]. These show the dynamic relation of carrier density, photon density, and optical gain in the cavity.

$$\frac{dN_p}{dt} = \Gamma(v_g g N_p) - \frac{N_p}{\tau_p} + \Gamma g \beta_{sp} v_g N_p \quad (1.1)$$

$$\frac{dN}{dt} = \frac{\eta_i I}{qV} - \frac{N}{\tau} - v_g g N_p \quad (1.2)$$

$$g \approx g_0 \ln\left(\frac{N}{N_{tr}}\right) \quad (1.3)$$

Equation 1.1 shows the rate of change of photon density. $\Gamma g$ is equal to the ratio of mode energy in the active region called the modal overlap parameter. The first term on the right side describes optical gain and the second term describes optical loss. $\tau_p$ is the photon life time. The lasing phenomenon needs a condition to lase so that the rate of increase of photon density due to stimulated emission is equal to the rate of decrease of photon density due to loss. The last term describes for spontaneous emission that the spontaneous emission rate equals the stimulated emission rate assuming one photon in the optical mode. The $\beta_{sp}$ is the spontaneous emission factor which is needed for $g$ which is related to the total stimulated rate.

Equation 1.2 describes the carrier density rate. The first tem on the right side describes the injection rate of carriers, the second term describes the recombination rate of consuming carriers, and the last term describes the stimulated emission rate. $\eta_i$ is

intrinsic efficiency that is the ratio of electrons making the radiative transition to total electrons. I is injection current, q is electron charge, $V$ is volume of active region and $\tau$ is carrier life time. The gain is also a function of the carrier density rate and this dependence is approximated by a logarithmic function as shown in Equation 1.3. $N_{tr}$ expresses carrier density at transparency in which gain equals loss.

To obtain analytic solutions, the steady state is implied. The left side of Equation 1.1 and 1.2 are set to zero. $\beta_{sp}$ is also set to zero due to photon density by spontaneous emission is much smaller than by stimulated emission. Figure 11 shows trends of photon density, carrier density, and gain as injection current increases. Using the rate equations, the operation of semiconductor lasers can be described.

When the injection current is just applied under the threshold, the gain is negative ($n<n_{tr}$). Photons from spontaneous emission will disappear due to mirror loss, waveguide loss, and loss from the active region. As a result, photon density inside the cavity will be very low, so there will be no photon generation. As injection current is increased, the carrier density will increase as shown in Equation 1.2 and gain will be turned from negative to positive($n_{tr}<n<<n_{th}$). Since carrier density is still much smaller than threshold current density and gain also smaller than threshold gain, the photon generation rate from spontaneous and stimulated emission inside the cavity is not much enough to overcome the photon loss rate. Therefore, photon density in the cavity is small as described in Equation 1.1. As injection current is increased further, the carrier density $N$ approaches the threshold carrier density $N_{th}$, and the gain $g$ approaches the threshold gain $g_{th}$ as shown in Figure 11. As the gain increases, the stimulated emission rate increases and balances the photon loss from the cavity, so there is lasing. According to Equation 1.2, as

the photon density increases further, the stimulated emission rate also increases and keeps carrier density. Therefore the gain is saturated which is needed to stabilize the photon density inside the cavity. This is the reason why there would be steady state that the photon density generated by spontaneous emission is smaller than the stimulated emission.

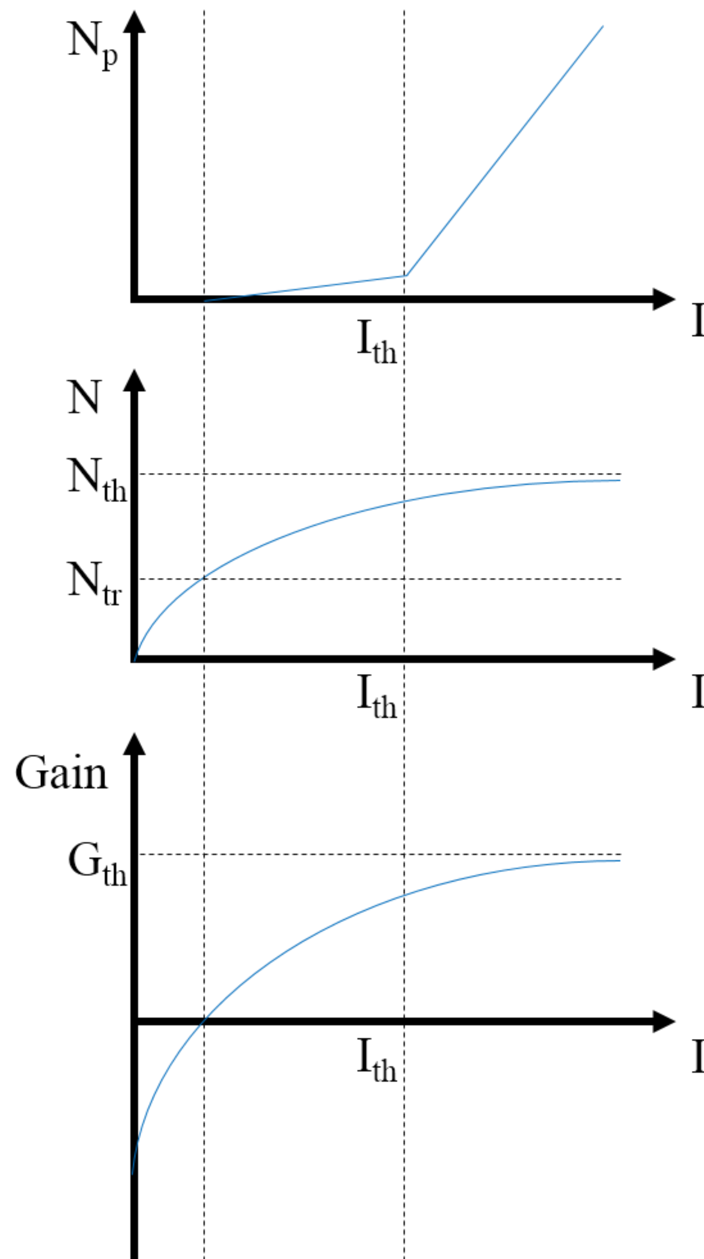



**Figure 11 The carrier density and the photon density vs. the injection current**

## 1.6 Scope of Work

This work focuses on a fabrication of GaAs-based edge-emitting semiconductor lasers. The fabrication process has been developed from scratch and is suitable for use in a wide variety of epitaxially-grown wafers. Front-end processing takes place in a cleanroom environment using standard wafer processing techniques. Back-end processing (wafer cleaving, die bond, wire bond) occur outside of the cleanroom. Chapter 2 provides an overview and development of each process step that is discussed in detail. The designed recipe is presented and the equipment used are shown. Photolithography is explained in detail and the mask layouts designed for use are given. Finally, a detailed account of the final fabrication procedure is discussed. In Chapter 3, the device characteristics are studied. Injected current versus output power and voltage are presented. The spectra at several current values are also presented. Additionally, the laser emission near field and far-field profile are measured. Chapter 4 summarizes this work and gives a prospective view on future work.

# 2. PROCESS DEVELOPMENT

## 2.1 Overview of Fabrication Process

The photolithography fabrication process for the edge-emitting semiconductor laser will be shown as a series of process steps. Most process steps are performed in a cleanroom facility under contamination control because this laser deals with micro-size features and minor contaminants can be a critical risk. A GaAs wafer is a more fragile substrate than those made of silicon and, therefore, needs to be treated carefully. In dealing with a piece of wafer instead of using a whole wafer, more attention is required. Because whole wafers are expensive, a piece of wafer is suitable to develop the process. To meet the size standard for wafers imposed by most processing tools, which is a whole wafer, the piece of wafer is taped to a dummy wafer for resizing as shown in Figure 12. In this development, a dummy wafer with 4 inch diameter is used.

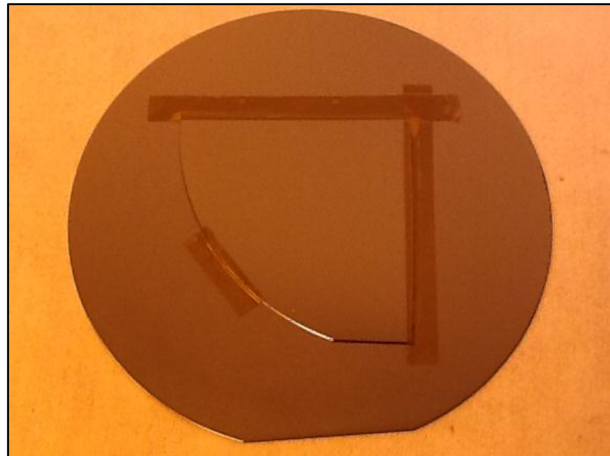


**Figure 12 Photograph of a piece of wafer attached on the dummy wafer**

### 2.1.1 Epitaxial Growth

GaAs is used as the substrate material because of lattice match to AlGaAs and InGaAsP, the direct bandgap materials from which the epitaxial structure is engineered. In this fabrication process, a Si-doped GaAs substrate is used for n-side contact as shown in Figure 13. The choice of n-type substrate is due to it having higher mobility than p-type, which provides lower resistivity in the substrate (which is the thickest part of the structure) [18].

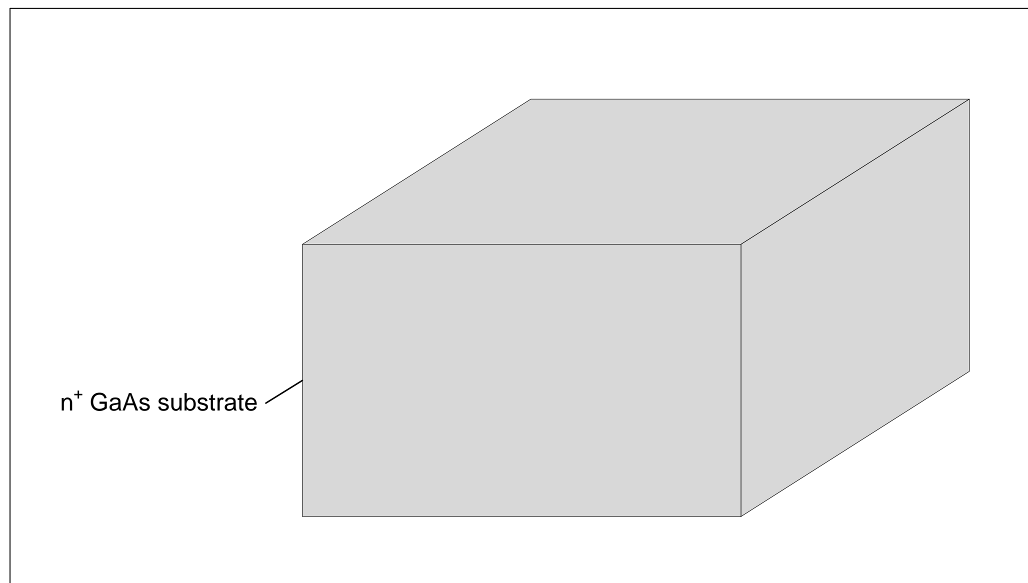



**Figure 13 GaAs wafer preparation to fabricate the semiconductor laser**

The epitaxial growth is designed to be a single quantum well hetero structure which has a p-i-n diode structure as shown in Figure 14. For this fabrication, InGaAs is positioned at the center as a quantum well. The epitaxial layers are deposited materials forming a single-crystal heterostructure with the same structural orientation as the substrate crystal structure. The typical thickness of each layer depends on how to confine the light. In this work, the epitaxy layers were grown by Metal Organic Chemical Vapor

Deposition (MOCVD). This technique is widely used in the growth of semiconductor epitaxial layers including III-V compounds on GaAs [19].

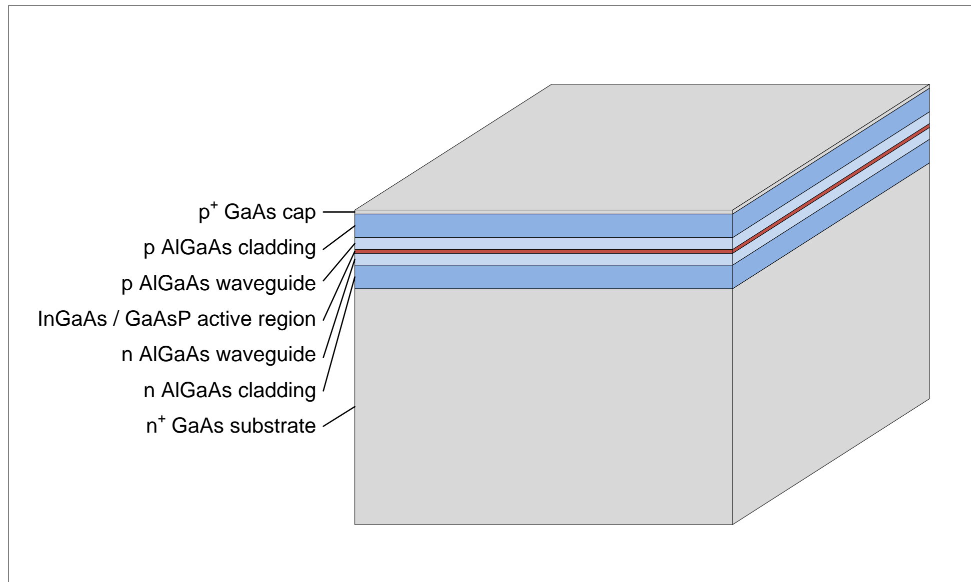



**Figure 14 Growth of epitaxial structure to create lasing by MOCVD**

### 2.1.2 Mesa Lithography

The mesa structure is needed to confine the mode in the lateral direction and help prevent excessive current spreading [20]. After growth of the epitaxial layers, a photolithography process is performed, which produces a pattern on the surface of the wafer using light-sensitive photoresist material and controlled exposure to light, as shown in Figure 15. Before spinning the photoresist, a bake and surface priming process are performed to prevent atmospheric moisture on the surface and to improve the adhesion of the photoresist.

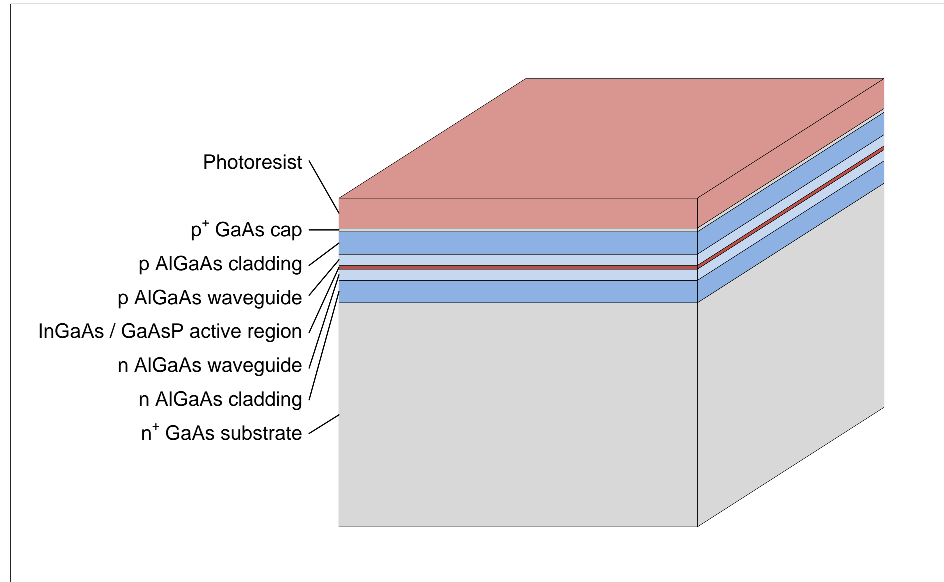



**Figure 15 Spin coating photoresist on the wafer**

After spin coating, a baking process called 'soft bake' is performed. This bake is to ensure that most of the solvent in the photoresist is driven off, to avoid contamination and sticking to the mask in an exposure process. It also improves resist adhesion to the substrate. The positive photoresist is softened by exposure to the UV light by an aligner and the exposed areas are subsequently removed in the development process. That means the pattern printed on the wafer surface has the same shape as the pattern on the mask. Figure 16 shows that the areas of the photoresist exposed to the UV light undergo a photochemical reaction and become soluble and soften in the developer.

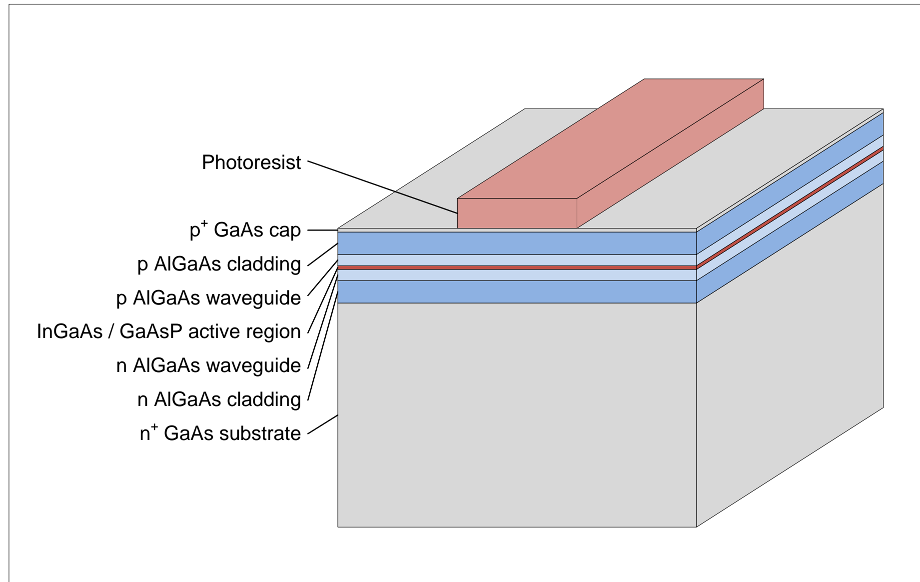



**Figure 16 Mesa patterning by photolithography process**

### 2.1.3 Mesa Etch

In order to make the mesa structure, the GaAs wafer needs to be etched. Etching is the process to remove the unnecessary part of material selectively. The basic purpose of etching is to reproduce the mask feature on the coated resist wafer. The area under the pattern on the wafer is not affected by the etchant, as photoresist protects it during the process. Hard baking of the photoresist before etching increases the thermal, chemical, and physical stability of the developed resist structures, further improving its performance during the etch [21][22]. Figure 17 and Figure 18 show schematic images of the mesa structure before and after removal of the photoresist of etching process. There are two methods of etching, wet etching and dry etching. Wet etching uses aqueous solutions to etch, whereas dry etching uses a gaseous plasma. The wet etching method is used in this fabrication because it can achieve a high etching rate with good selectivity at low cost efficiency (compared with dry etching). In developing an etching process, two

things must be considered: etch rate (how much material is removed per unit time) and etch selectivity (the ratio of the material etch rate to the mask etch rate). After etching, boiling acetone is used to remove the photoresist mash.

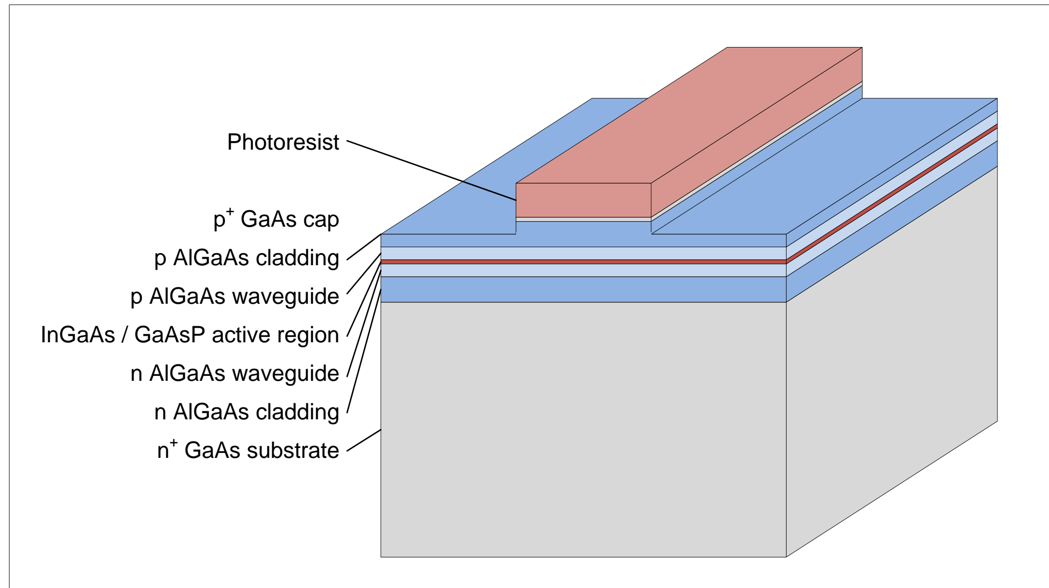



**Figure 17 Wet mesa etching of GaAs wafer**

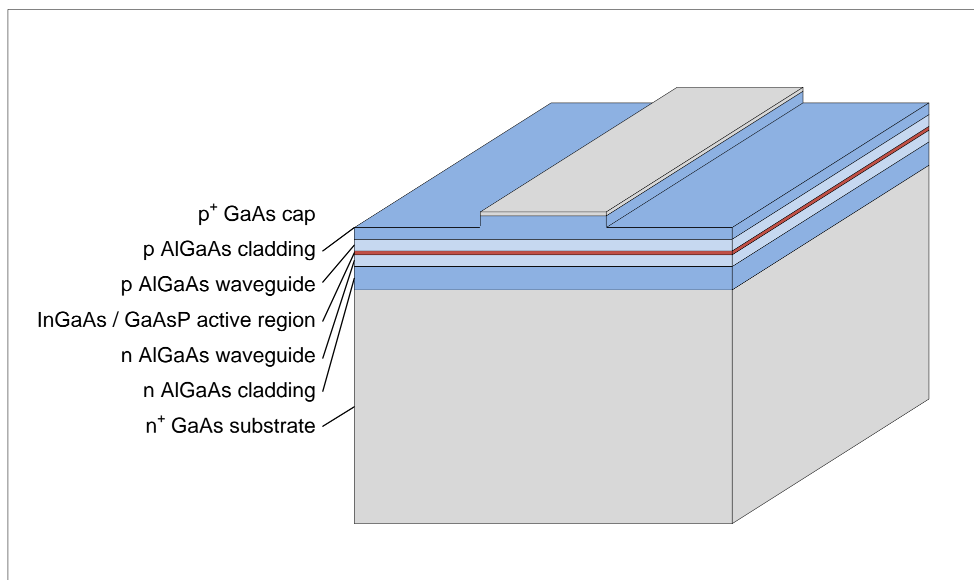



**Figure 18 Removing photoresist after etching process by boiling acetone**

### 2.1.4 Contact Window Definition

An oxide layer is used to insulate the metal from the p-side of the device in all area except where current is to be injected. The oxide layer is deposited by an E-beam evaporation after a cleaning process is performed. This is illustrated schematically in Figure 19. Deposition is a process that places the film layer on the wafer. There are two kinds of techniques of film deposition: chemical process and physical processes. Chemical process, for example, are chemical vapor deposition (CVD) and plating. Evaporation, physical vapor deposition and spin on methods are example of physical process. The electron beam evaporation, which is used in this step, fires a high energy beam from an electron gun to boil a small target of material in vacuum condition. The vapor from target is deposited on the wafer.

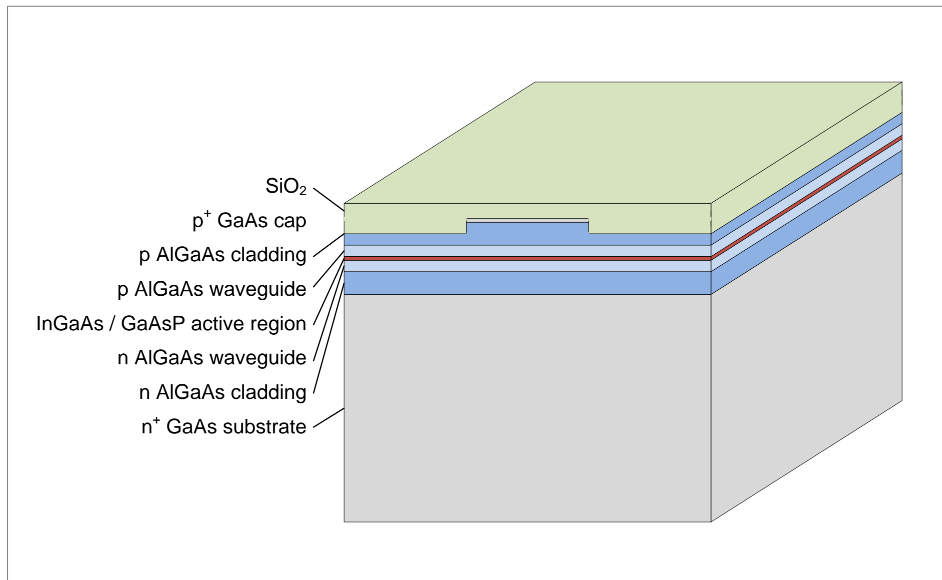



**Figure 19 Oxide level deposition by e-beam evaporator**

Figure 20 shows the process that is used to pattern the stripe contact window after oxide deposition. This oxide aperture layer is added to confine the applied current to the mesa center, to reduce leakage currents, and improve mode selection. In this step, alignment to

the previously processed layers is very important. To improve adhesion, hexamethyldisilazane treatment is performed on the oxide surface of the wafer.

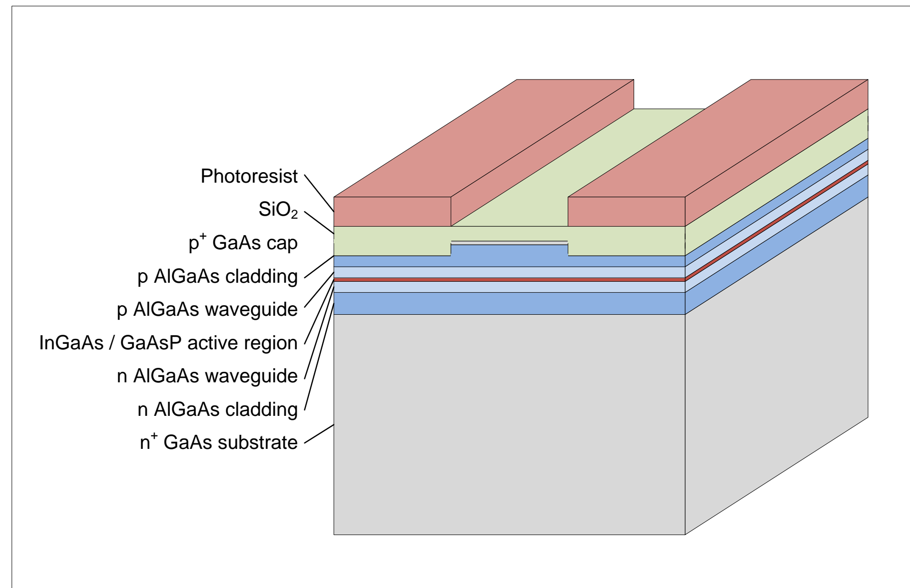



**Figure 20 Stripe patterning on the oxide by photolithography process**

After the photolithography, the SiO2 oxide layer is etched by Buffered Oxide Etch (BOE) to open the contact window to confine applied current as mentioned previously. It is illustrated in Figure 21. Dealing with BOE is dangerous work because BOE includes hydrogen fluoride (HF) even if it is diluted, etching should be performed carefully. A BOE can burn covering less than 2 percent of the human body can be fatal. HF should be handled in a laminar flow bench, using two pairs of nitrile gloves and eye protection. Any small spills should be wiped up immediately with wipes and rinsed [23].

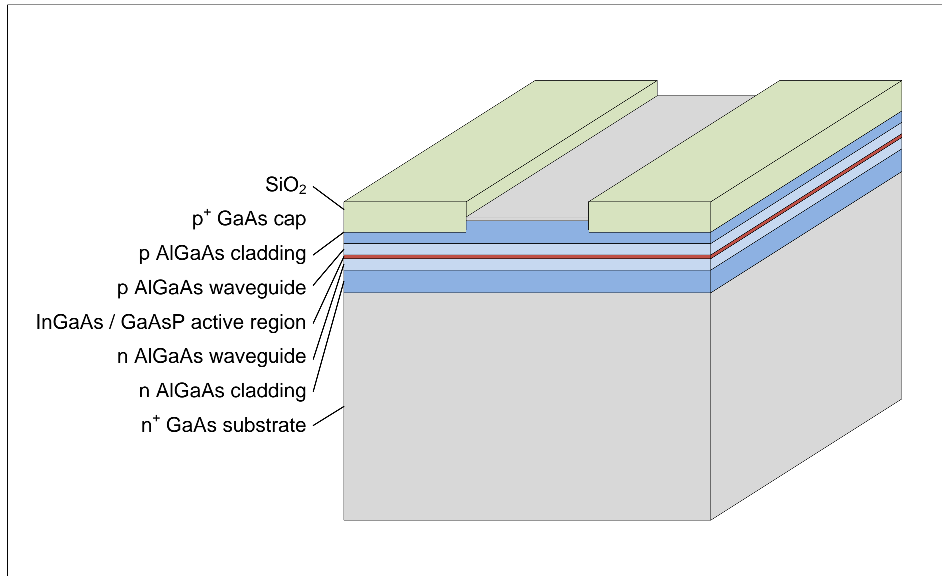



**Figure 21 Oxide wet etching of SiO2 to open the contact window**

### 2.1.5 Metallization

For P-side ohmic contact, Titanium (Ti), Platinum (Pt) and Gold (Au) are deposited by E-beam evaporator as shown in Figure 22. These metals are used because GaAs and Au contacts have different work function which makes Schottky contact or Ohmic contact. Ohmic contact is an electrical junction between metal and semiconductor material that has a linear current-voltage curve [24].

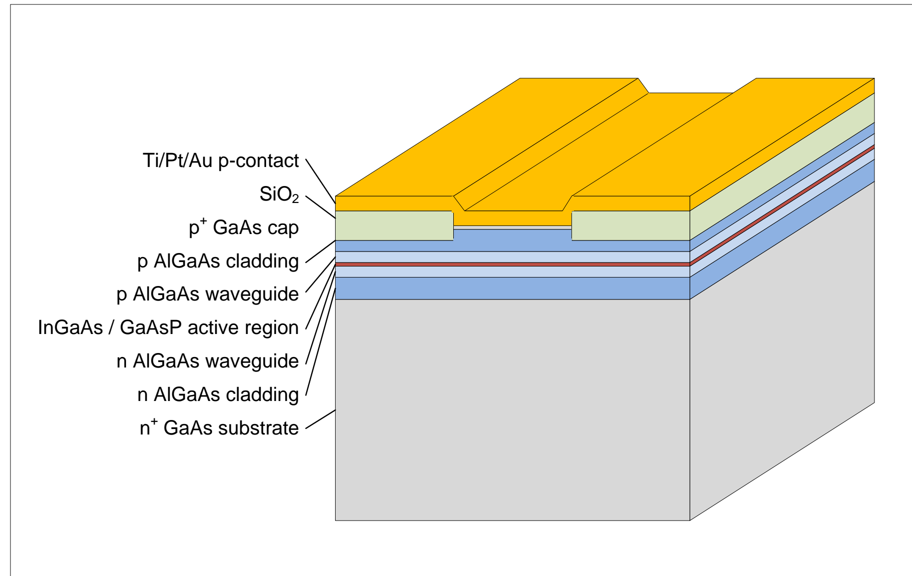



**Figure 22 Metal deposition on P-side (top side)**

The next step is polishing the bottom side of GaAs substrate for N-side contact and junction down bonding as shown in Figure 23. The thickness of the wafer can be controlled by polishing. In general, the target thickness is 200µm~500µm, as thinner wafers are typically easier to cleave and has exhibit reduced series resistance. The original wafer thickness is about a millimeter. This step was skipped in this work.

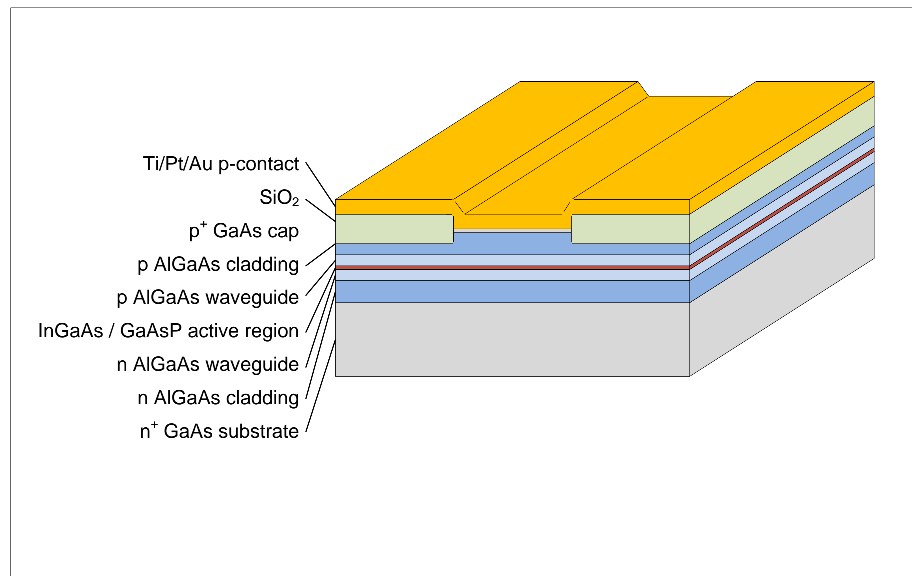



**Figure 23 Polishing the bottom side of GaAs wafer**

After the polishing step, N-side ohmic contacts are deposited with AuGe, Ni and Au on the backside, which is N-type GaAs substrate as shown in Figure 24. The electrical properties of alloyed AuGe offers relatively lower contact resistance to N-type GaAs.

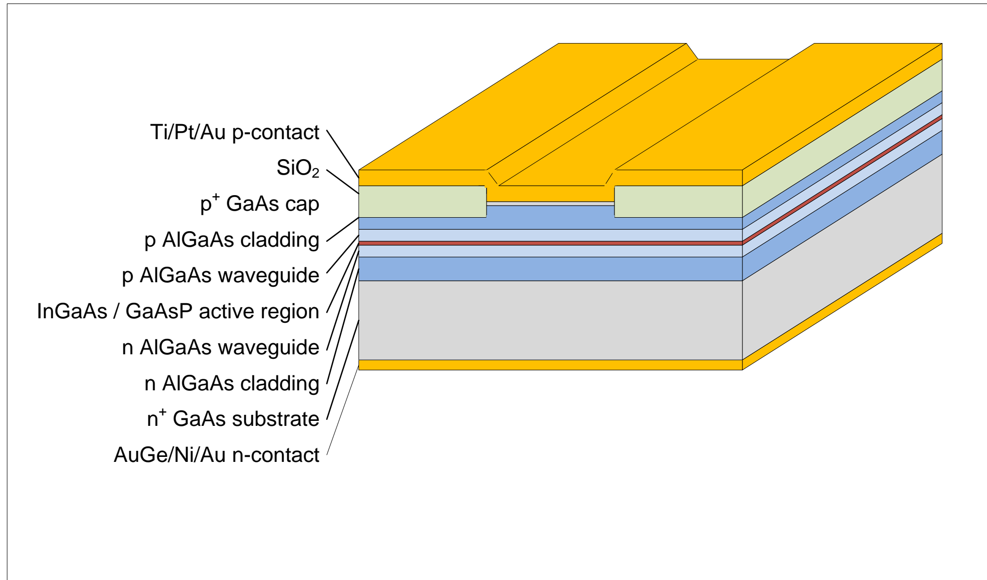



**Figure 24 Metal deposition on N-side (bottom side)**

### 2.1.6 Cleave, Coat and Bond

In this step, each laser is cleaved by hand. After that, the facets of lasers are coated with asymmetric reflectivities. This is called Partial-reflecting (PR) which the laser comes out; the other side is called High-reflecting (HR). The facet direction is considered a crystal orientation of the GaAs wafer to get perpendicular side as shown in Figure 25. In this work, the side facet coating is skipped, and the lasers are tested uncoated.

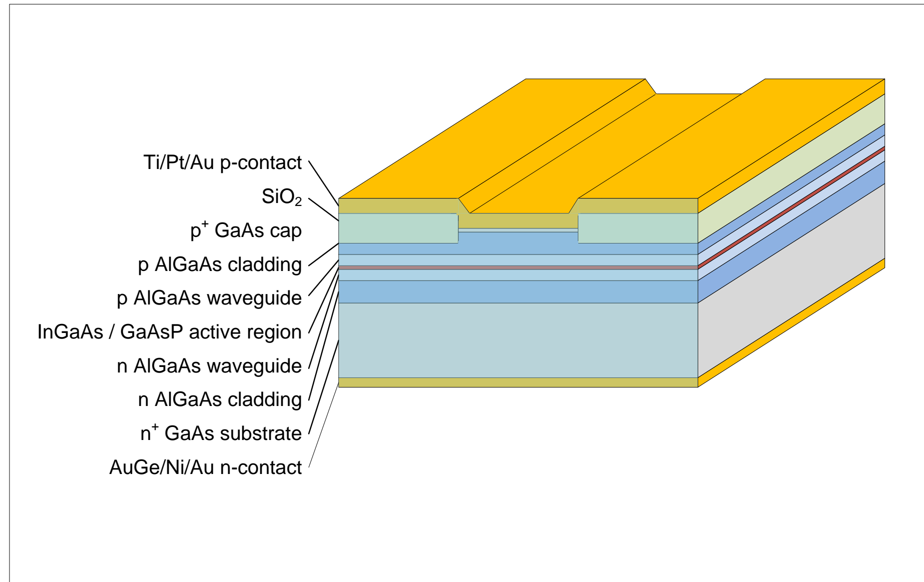



**Figure 25 Cleaving and coating on side to create a lasing process**

The last step is the bonding process between chip and heat-sink with indium solder, as illustrated in Figure 26. Indium solder is widely used to bond semiconductor lasers due to its simplicity and it can bond directly to copper. AuSn is another option for higher reliability, as it requires expansion to be matched heat sinks. C-mount heat-sink is used for bonding as shown in Figure 27. To wire bond, a manual wire bonder is used with 25µm diameter gold wire. The bond wire can be either Au or Al wire due to the fact that it bonds well to gold and copper. A standard wire diameter of 25µm diameter is common [25].

**Figure 26 Die attach and wire bonding on a heat-sink**

**Figure 27 A Schematic and picture of C-Mount heatsink**

## 2.2 Mask Design

This laser is designed with 3 different photolithography levels: mesa, oxide and an optional metal level. The layouts are created with CAD layout software called "L-Edit" by Tanner EDA. The screenshot was captured and is shown in Figure 28. This mask set was designed for 4 different mesa sizes – 4µm, 20µm, 100µm and 200µm in a 10mm by 10mm unit cell. A total of 29 unit cells fit on a 5″ x 5″ mash. Table 1 shows the specifications of mask design. The different sizes of mesas were selected in order to vary the output characteristic of lasers. It is designed to be easy to cleave by hand, by providing 2mm cleave streets between adjacent mesas. A layout of all three levels is shown in Figure 29.

**Table 1 Mask specifications**

| **Mask Specifications** | | | |
|---|---|---|---|
| **Material** | Chrome on Sodalime | **Format Type** | GDSII |
| **Size** | 5 by 5 inches | **Thickness of Mask** | 0.2286mm |
| **# of Unit Cell** | 29 cells | **Unitcell Size** | 10mm by 10 mm |
| **Mesa Sizes** : 4µm, 20µm, 100µm, 200µm | | | |

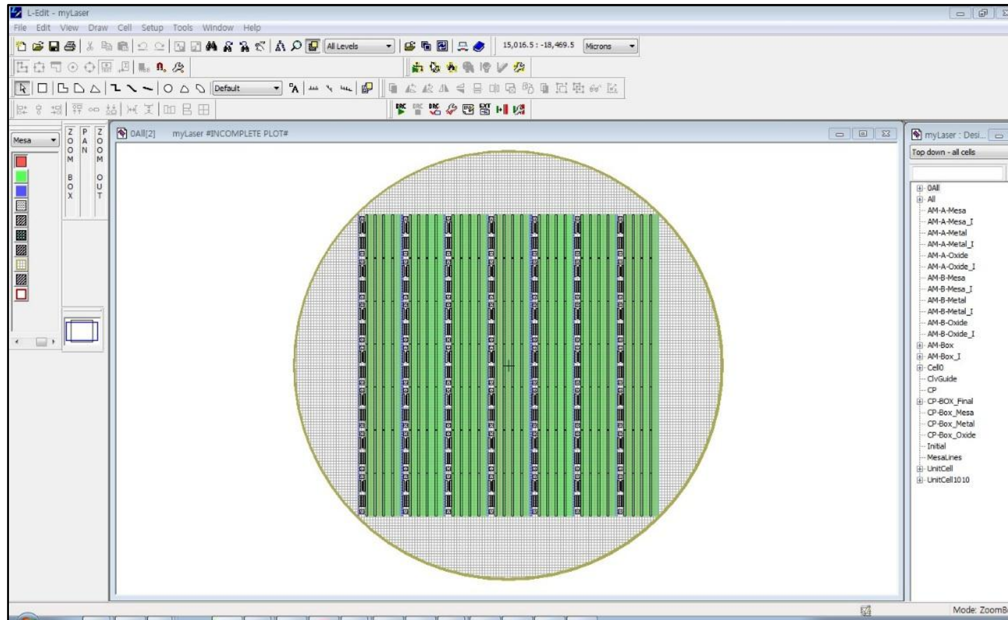



**Figure 28 Screen capture of the CAD layout software called “L-EDIT”**

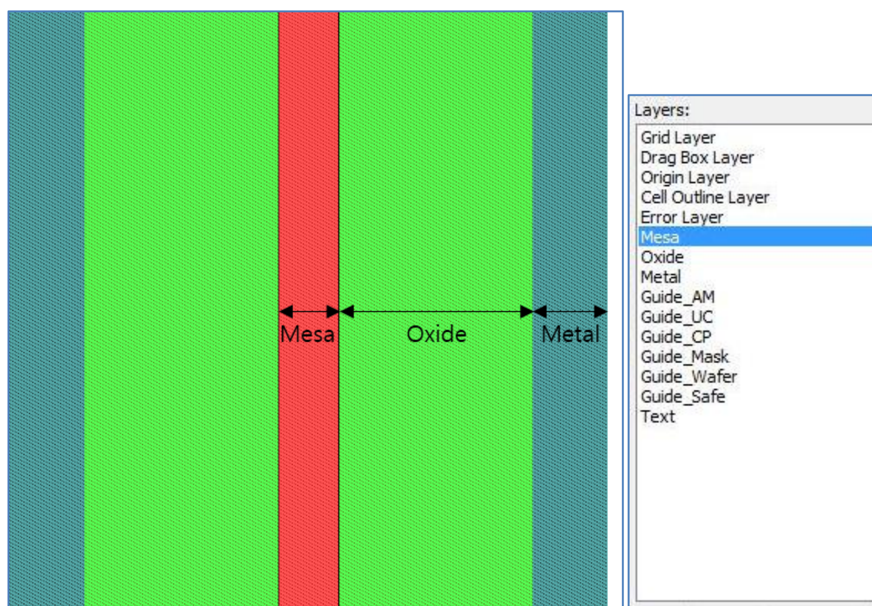



**Figure 29 Layer lists and layout of the three mask levels for one of mesas designed with L-Edit**

The mesa level of this mask determine the width of mesa to both control the injection current profile and confine the optical mode in the lateral direction. The oxide level is designed isolate the top contact further control the lateral injection current profile.

Alignment marks are designed for 3 levels and each pair can be matched to every other level in the photolithography process as shown in Figure 31. This is required to ensure that they will be visible with microscope and allow accurate alignment in photolithography process. These marks provides the most accurate alignment with 5 crosses and 4 pairs of meshed shape structures.

Figure 30 shows a pair of alignment mark set individually. The thickness of smallest feature is 2μm. Each pair of meshes are designed to be unmatched except just center peak to help to align vertically or horizontally. The order of alignment with an aligner is – first, match the biggest cross into the center. Second, figure out the alignment mark is angled or not with 4 sides small crosses. At last, fix the exact position using 4 meshes.

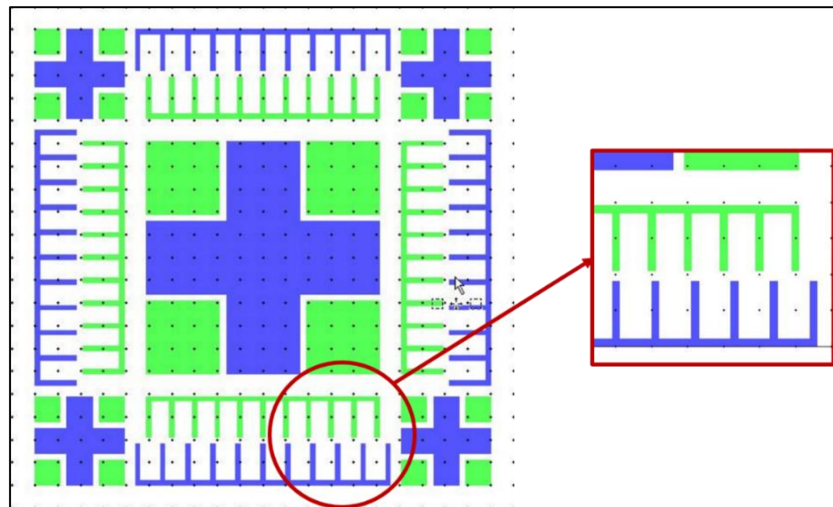


**Figure 30 Picture of magnified meshes of the alignment mark**

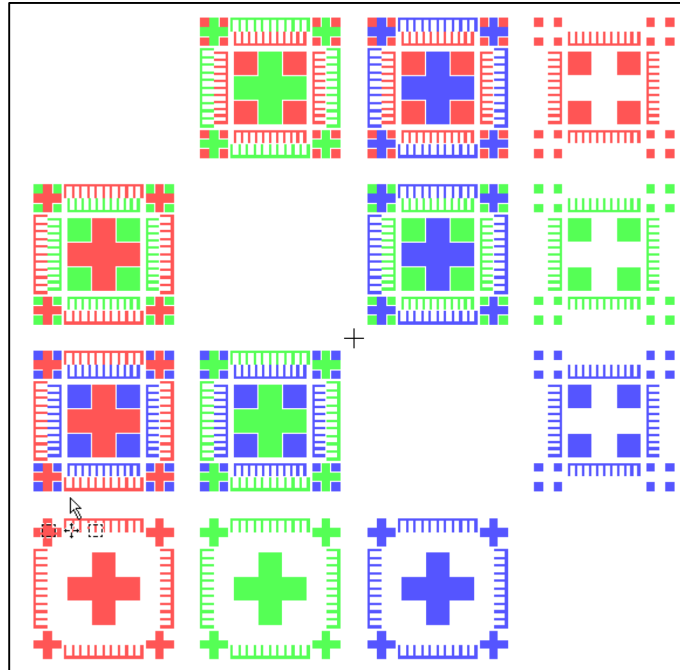


**Figure 31 Alignment marks layout for three mask levels**

Each mask is chrome patterned on 0.2286mm of a sodalime glass. There are usually two kinds of materials for photomask, one is the sodalime, and the other is quartz. The most different feature is thermal expansion and cost. In most cases, the sodalime glass is used due to the price being much cheaper than the quartz. And thermal expansion is not a big issue in this fabrication.

The photos of each masks are shown on Figure 32. The chrome is printed on the mask as shown in Figure 33. It is 20 times magnified. This mask is designed for using positive photoresist, Ultra-Violet light pass through the glass part and it is also blocked by opaque part. The photoresist that is exposed to light becomes soluble to the photoresist developer.

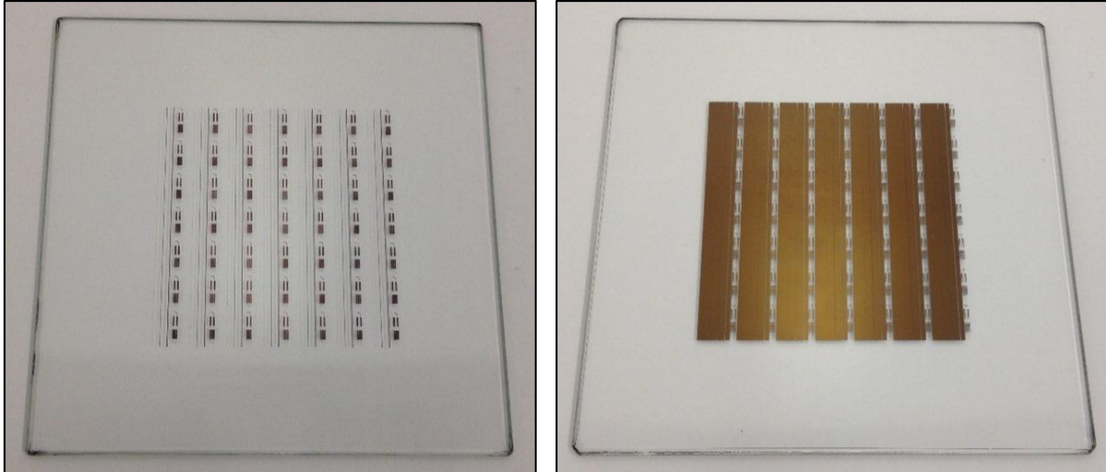


**Figure 32 Picture of photomasks for positive photoresist (left: mesa, right: oxide)**

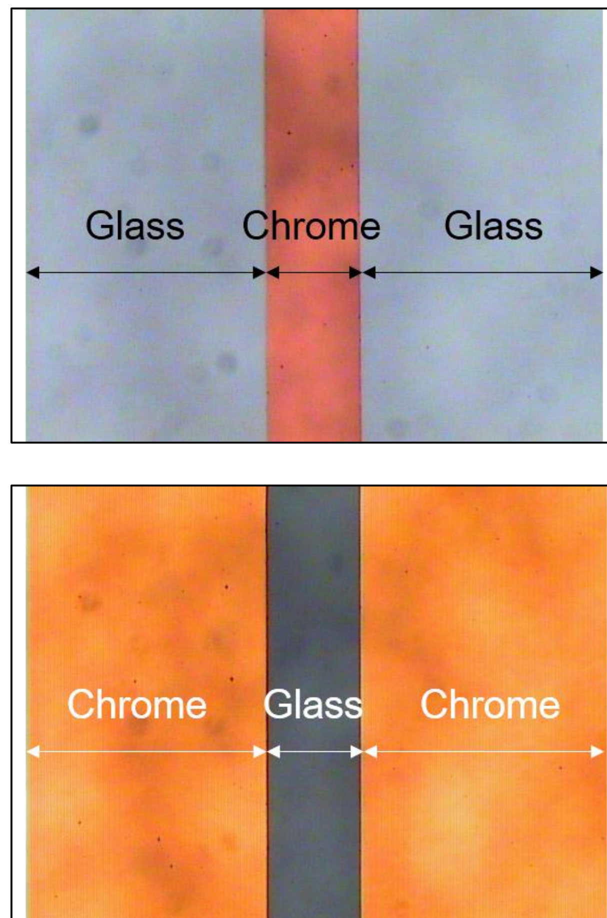



**Figure 33 Microscope picture of mesa and oxide of each actual mask (20x Mag.)**

Figure 34 and Figure 35 show a magnified alignment mark for each mask, but these look different. This problem occurs when the mask is manufactured at a mask fabrication company. The reason of the difference between the masks is the tolerance of glass and chrome thickness. Most of the 2um parts are visible in one direction of the mask but in the other direction, some seem to disappear.

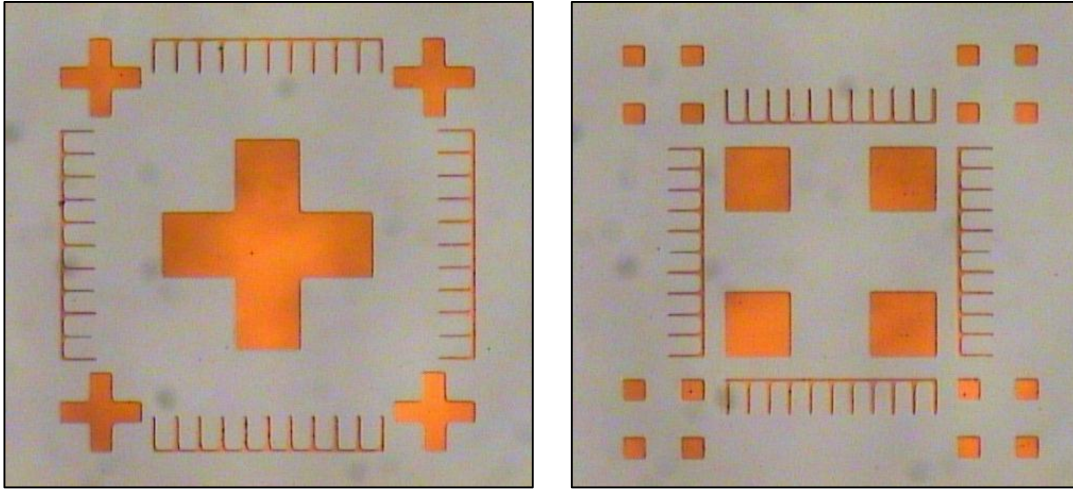


**Figure 34 Microscope pictures of the alignment mark of actual mask – Good (20x Mag.)**

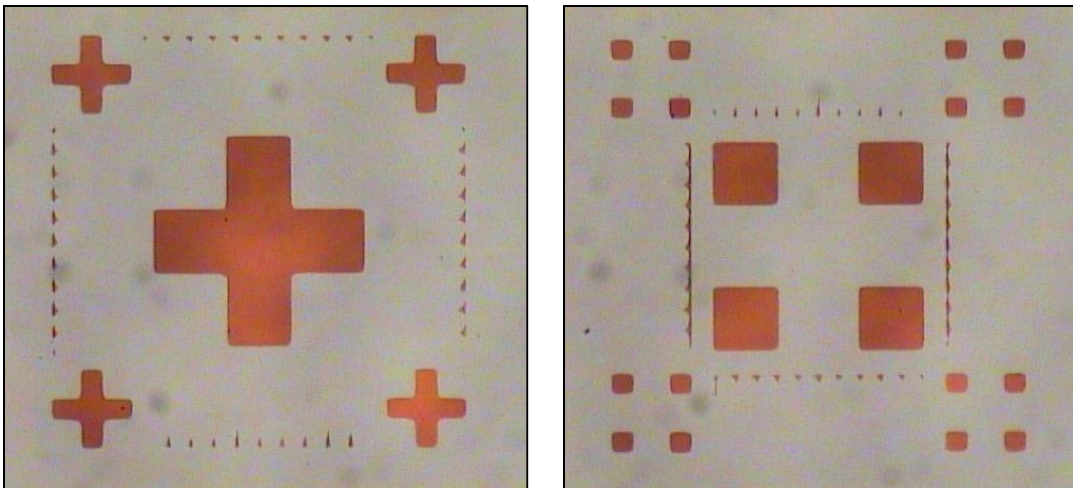


**Figure 35 Microscope pictures of the alignment mark of actual mask – Bad (20x Mag.)**

Figure 36 shows contact pad on the oxide mask [26]. It is designed for measuring a contact resistance of the wafer. Each square has a different distance and expected linear resistance profile. This work was skipped in this fabrication.

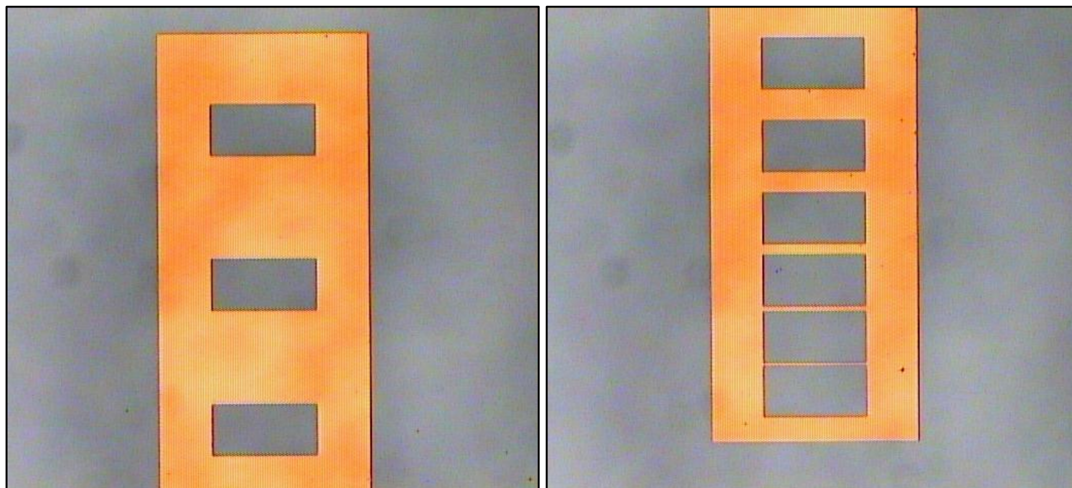
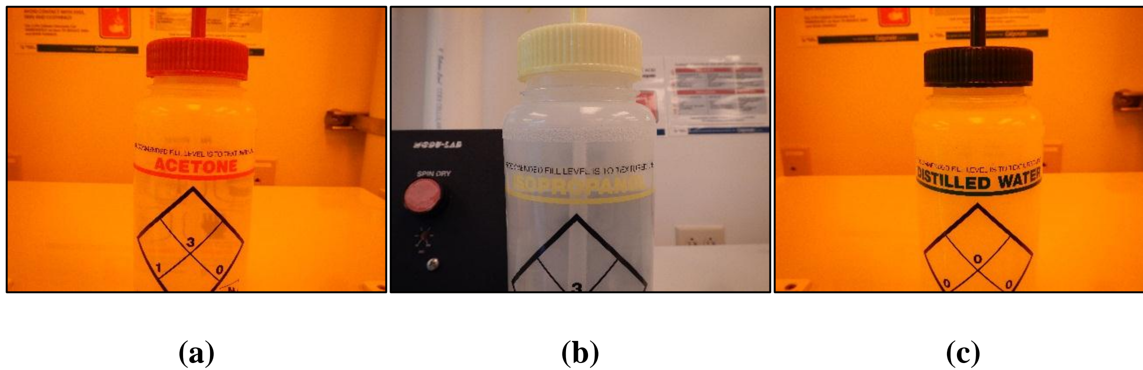


**Figure 36 Microscope pictures of contact pad of actual mask (20x Mag.)**

## 2.3 Photolithography Process Development

The photolithography process for this study begins with the cleaning of a piece of GaAs wafer by Acetone (a), Isopropyl (IPA) (b), DI (c), and IPA, respectively, as shown in Figure 37. Substrates contaminated with particle impurities can be prepared with this four-stage substrate cleaning to better resist wetting and adhesion. Acetone removes organic impurities on the wafer, and this contaminated acetone is rinsed by IPA, which unlike DI, is miscible with acetone. After the IPA is applied, DI is used to clean the IPA on the wafer. Lastly, the DI on the wafer is cleaned by IPA again.




**(a)** **(b)** **(c)**

**Figure 37 Pictures of bottles of acetone, isopropyl alcohol and DI water for cleaning process**

After cleaning, the piece of GaAs wafer is taped on the dummy wafer in preparation for the upcoming processes. Attention must be paid when putting a piece of tape at the edge of the wafer fragment because the yield of the outcome could be decreases if the edge of the piece of wafer is too covered by tape. See Figure 38. Also, if less tape than normal is used, the piece of wafer will be ejected during the spinning process that spreads photoresist. The taping position of piece of wafer is also crucial for reducing centrifugal force for the dummy wafer, and for spreading the photoresist uniformly so as to reduce an edge problem called ‘edge bead’ as shown in Figure 39. The

photoresist on the wafer flows very gradually to the edges and does not experience a force strong enough to be taken off the edges.

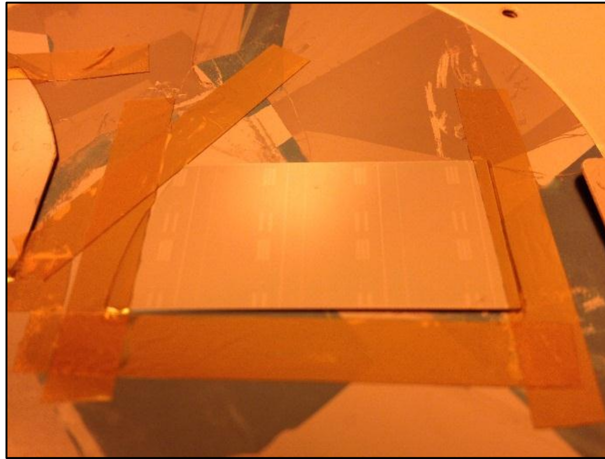


**Figure 38 Picture of taped sample on the dummy wafer**

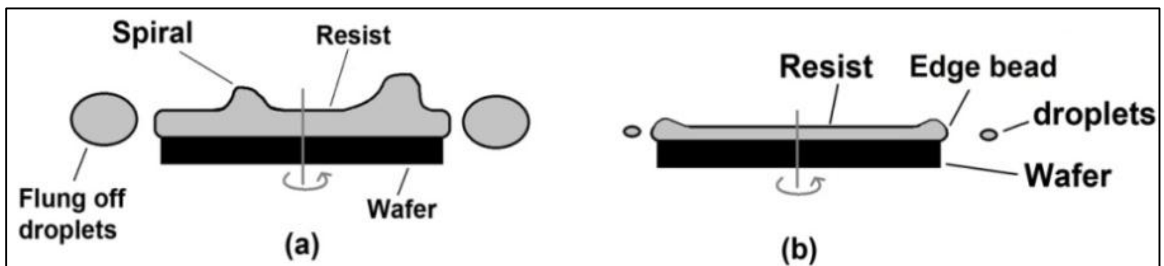



**Figure 39 The illustration of edge bead [27]**

Next, baking is needed to remove moisture from the wafer. Moisture on the wafer can affect the adhesion of the resist to the surface of the wafer. A hot plate is used for this step at 150°C for 20min as shown in Figure 40.

**Figure 40 An image of the hot plate utilized for baking processes**

After baking the wafer, the second phase is spinning the HMDS on the wafer for surface priming. Figure 41 shows bottles used for this photolithography work. HMDS treatment is a common method for Si wafers, not for GaAs wafers [28]. This pre-treatment may not be effective on GaAs on the surface of wafer. There is very little information available for GaAs, but a study suggests a pre-coat native oxide etch on GaAs to improve adhesion. In this experiment, the initial lithography consisted of the HMDS vapor prime at 4500 RPM for 20 seconds, at 110°C for 45seconds with a spin coater (BIDTEC SP100) as shown in Figure 42.

**Figure 41 Pictures of bottles of Photoresist (AZ5214-E IR) and HMDS**

Following another round of the photolithography process is the spinning of the photoresist on the wafer. Clariant AZ5214E Image Reversal photoresist is used. This is a special photoresist which can be used both in positive and negative tone. In this work, the photoresist is used as a positive photoresist. The photoresist is coated at 4500RPM for 30 seconds for 1.7µm as shown in Figure 43. According to the plot in Figure 44, photoresist thickness of 1.4µm is expected, but actual thickness is measured as 1.7µm by a film thickness measurement equipment system Figure 53. In order to achieve lower thickness variation, a longer spinning time is often used as shown in APPENDIX B. After spinning, soft bake is performed at 110°C for 45 seconds to remove the solvent in the photoresist.

**Figure 42 The picture of the spin coater(BIDTEC SP100) and vacuum chuck**

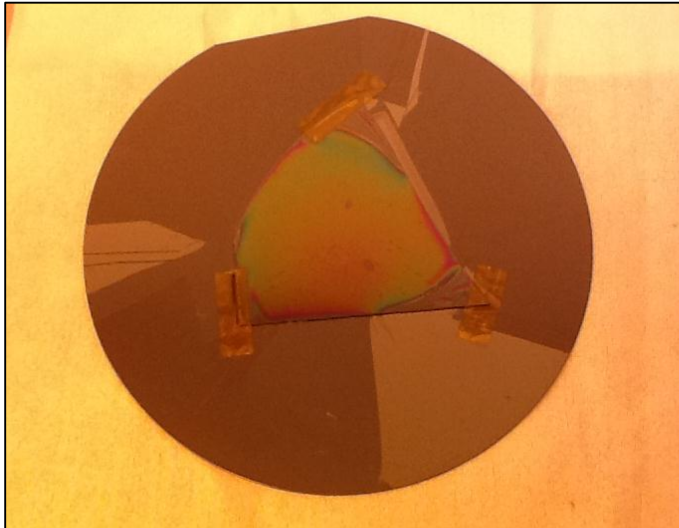


**Figure 43 The picture of after spinning of GaAs wafer piece taped with dummy wafer**

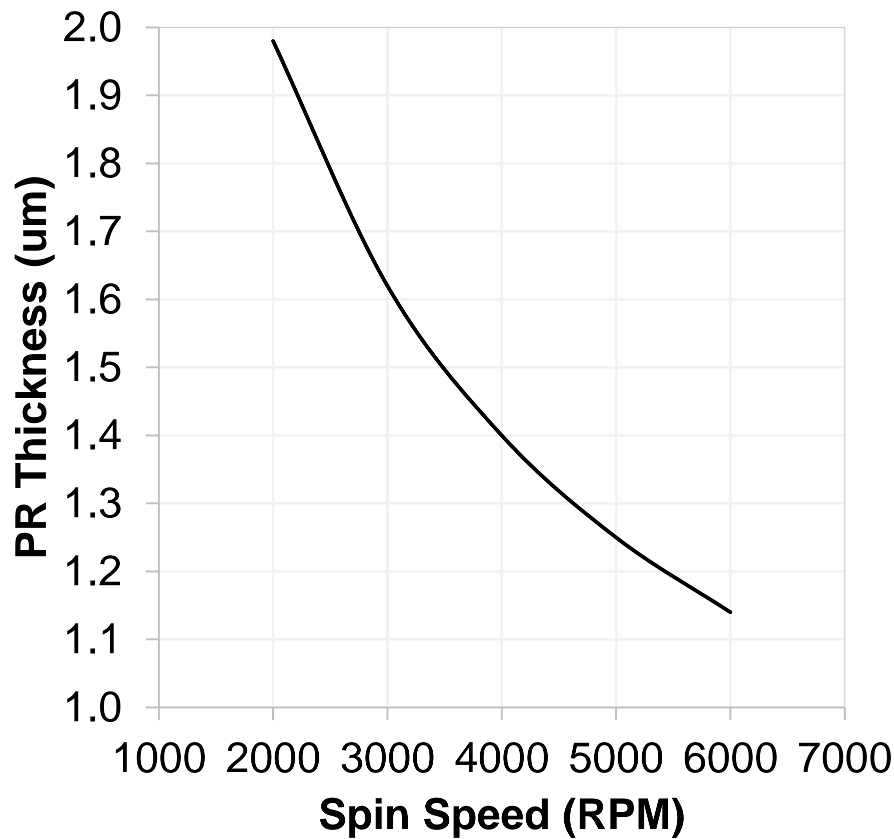



**Figure 44 The plot of spin speed vs. photoresist thick from the supplier datasheet**

When the soft bake is performed, the piece of wafer is detached from the dummy wafer for exposure. With the dummy wafer, the sample is too thick to put on the chuck under a photomask in the aligner. This work is performed carefully because the piece of GaAs wafer is fragile. Exposure depends on resist thickness and lamp intensity. This piece of wafer is covered in 1.7μm thick photoresist, and it is exposed to UV light at an intensity 13mW/cm$^2$, for 5 seconds at 365nm. This recommendation is from the datasheet of photoresist. The aligner, MJB4 (Suss MicroTec) manual aligner, is operated for exposure as shown in Figure 45. It is designed for 4 inch wafer samples.

**Figure 45 The pictures of the mask aligner MJB4 by SussMicrotec Co.**

In this fabrication, there are two photolithography processes, one for the mesa structure and one for oxide. For oxide photolithography, alignment with the mesa structure is a critical process. These two photomasks have an alignment array in each unit cell, which means alignment can occur by matching several alignment marks.

To develop the photoresist after the exposure step, a developer AZ351B is mixed with DI in a 1:3 ratio as shown in Figure 46. Figure 47 shows after development for the 2nd lithography for oxide etching. This process is monitored visually to observe when the photoresist is removed from the wafer. This method is optimized with the best timing which depends on sample’s condition when the development is sufficient. But in mass production, this is impossible because of yield and cost-efficiency. The process of development takes around 50 seconds. If there is a baking step before development, the photoresist on the wafer works as a negative photoresist.

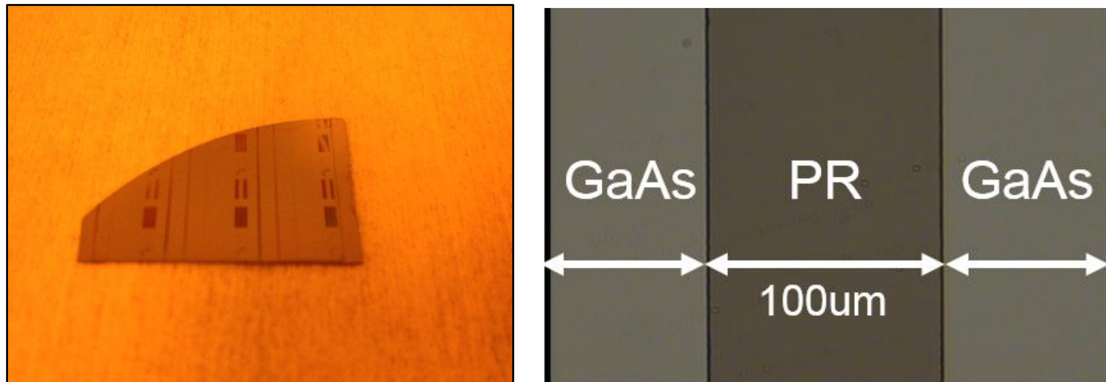



**Figure 46 Pictures of the sample and 100µm photoresist stripe after develop process – sample (left), 20x Mag. of microscope (right)**

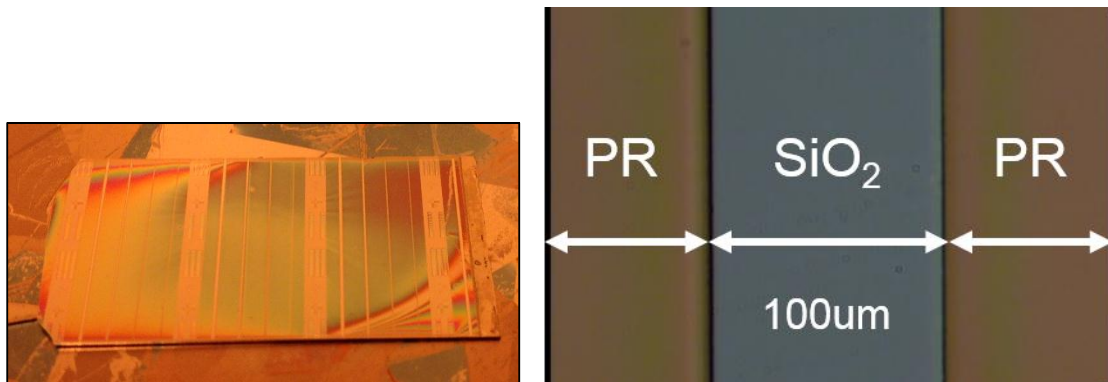



**Figure 47 Pictures of the sample and 100µm photoresist stripe after second photolithography process using oxide mask – sample(left), 20x Mag. of microscope(right)**

The final step of photolithography is a hard bake. The hard bake can be performed in order to increase the thermal, physical and chemical stability of the developed photoresist structures for subsequent processes, including chemical etching. It is baked at 110℃ for 60 seconds.

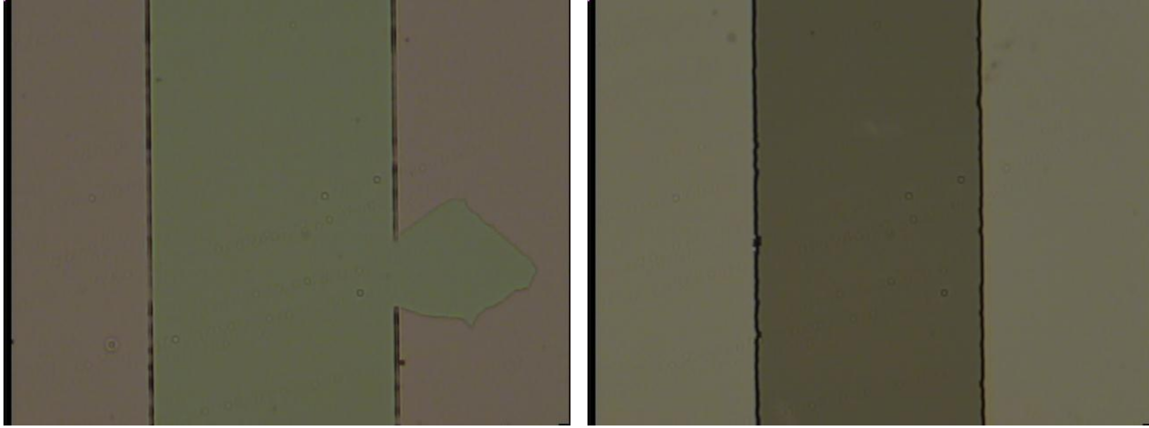


**Figure 48 Microscope pictures of (left) under exposure and (right) over exposure photoresist (after development, x20 mag)**

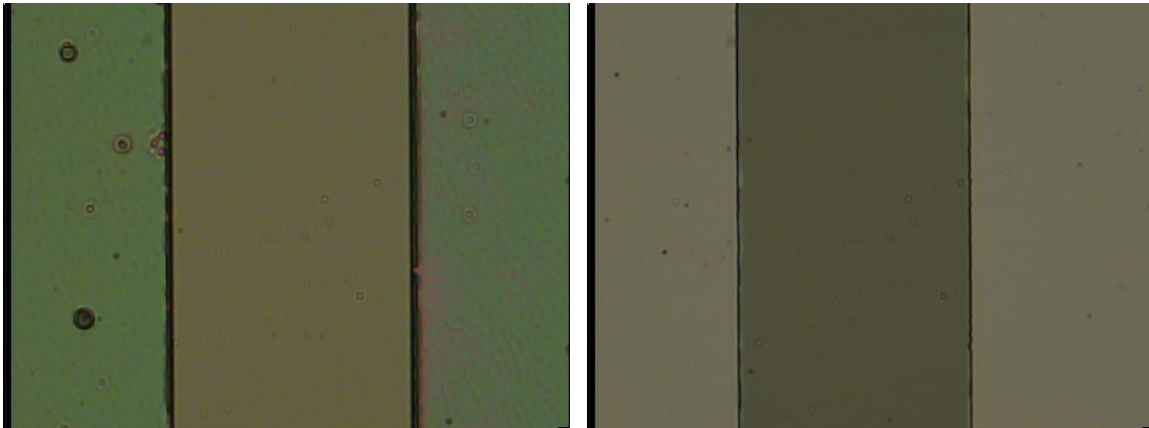


**Figure 49 Microscope pictures of (left) under development and (right) over development photoresist (x20 mag)**

## 2.4 Etch Process – Mesa & Oxide

### 2.4.1 Determine semiconductor and oxide etch rates

This laser fabrication process has two etching operations – one is GaAs etching and the other is $SiO_2$ etching. The determination of the etching rate of these two materials is critical to the development of the laser fabrication process. The system to assess etch rate is discussed further in this paper. Figure 50 depicts where etching process is performed.

**Figure 50 The picture of a wet bench where etching process is performed**

For etching GaAs wafers, several studies have researched the following options: $Br_2$:Methanol, H2O2:NH4OH:DI, H2SO4:H2O2:DI, H2SO4:H2O2:HCl, or HCl:DI [29]. The etchant, which is mixed from 1 $H_2SO_4$ : 8 $H_2O_2$ : 160 DI, is selected in this process for its ubiquity as well as the relative ease with which its etch rate can be manipulated through the volume of DI in the solution [30]. The expected etch rate is 43Å/sec [31].

Four GaAs samples are used to determine the etch rate by varying the etch duration. In

this case, etch times of 3min, 4min, 5min and 20min were used. After etching, the sample is cleaved and the cross-section is observed with a scanning electron microscope (Hitachi TM3000). An example image of one of the etched mesas is shown in Figure 51. This is a photo of a piece of cleaved semiconductor after etching. An etch selectivity is observed that is a measure of how effective the etch process is in removing the material to be etched. On the other hand unaffected other material remains in the wafer. The slope in Figure 51 shows an isotropic etch profile of etch rates from different materials with preferred crystallography direction. In this work, the isotropic etch profile does not affect the sample negatively.

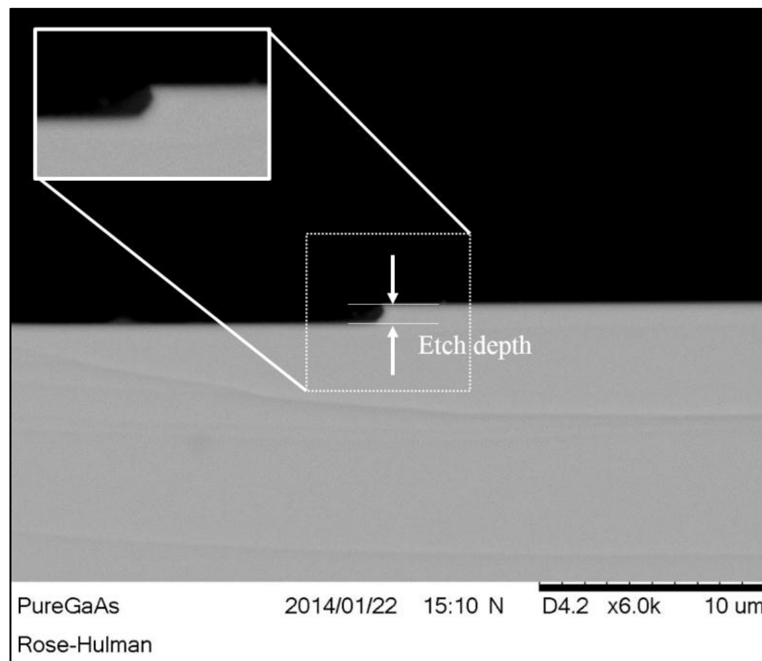



**Figure 51 Etched surface of GaAs wafer taken by a scanning electron microscope (6000x Mag.). This sample was etched to a depth 0.84µm.**

To calculate the etch rate, mesa heights are measured with 6000 times magnification SEM pictures. Both sides of all mesa structure on the surface of wafer (one

unit cell) are used to calculate the average height. This calculation is shown in Table 2.1. According to Figure 52, the average etch rate is determined 0.22μm/min (52.25Å /sec).

**Table 2 Calculate Etch Rate for GaAs wafer**

| | Sample 1 | Sample 2 | Sample 3 | Sample 4 |
|---|---|---|---|---|
| **Etching Time** | 3min | 4min | 5min | 20min |
| **Average Etched Time** | 0.65μm | 0.86μm | 1.12μm | 4.11μm |
| **Calculated Etch Rate** | 0.22μm/min | 0.21μm/min | 0.22μm/min | 0.21μm/min |

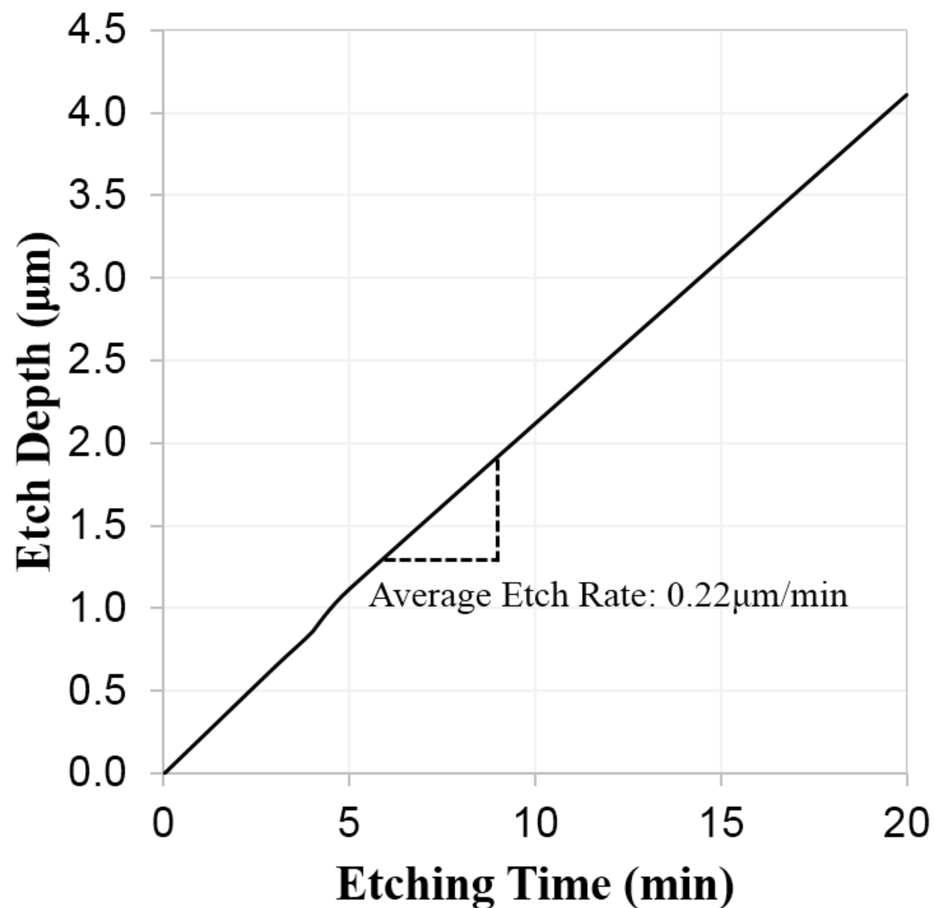



**Figure 52 Plot of Etch Rate for GaAs wafer**

The etch rate of $SiO_2$ is determined using a different process by etching with 1 Hydro Fluoride : 25 DI water [32]. Several silicon samples having around 3300Å $SiO_2$ surface film were etched for various times and the film thickness was measured using specific equipment (Filmetrics F40) shown as Figure 53. Table 3 shows the thickness of $SiO_2$ film at several etching times. This equipment measures the thickness of thin film by using spectral reflectance as shown in Figure 54 (It is used to reflect light off the film and then analyze the reflected light over a range of wavelengths). The etch rate was determined to be 13.18 Å /sec as shown in Figure 55.

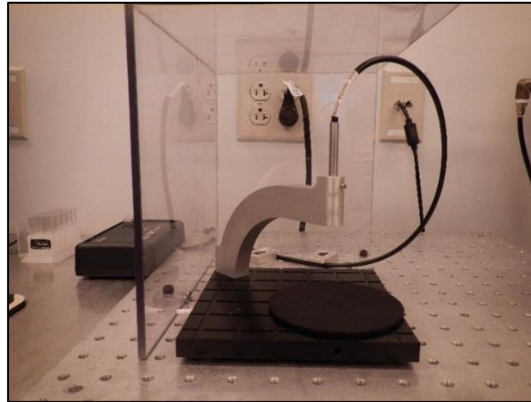


**Figure 53 The picture of film thickness measurement system (Filmetrics F40)**

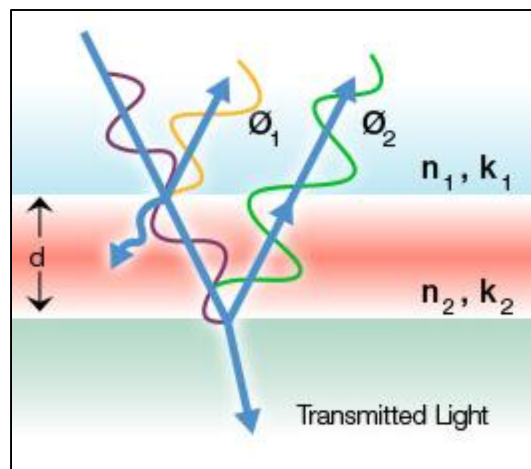



**Figure 54 A mechanism of measuring the thickness of thin film by Filmetrics F40**

**Table 3 Measured and Calculate Etch Rate for $SiO_2$ film**

| Time | 0sec | 30sec | 60sec | 90sec | 120sec | 150sec |
|---|---|---|---|---|---|---|
| SiO2 Film Thickness | 3313Å | 2910Å | 2430Å | 2108Å | 1779Å | 1288Å |
| | | | | | | Average Etch Rate: 13.18Å /sec |

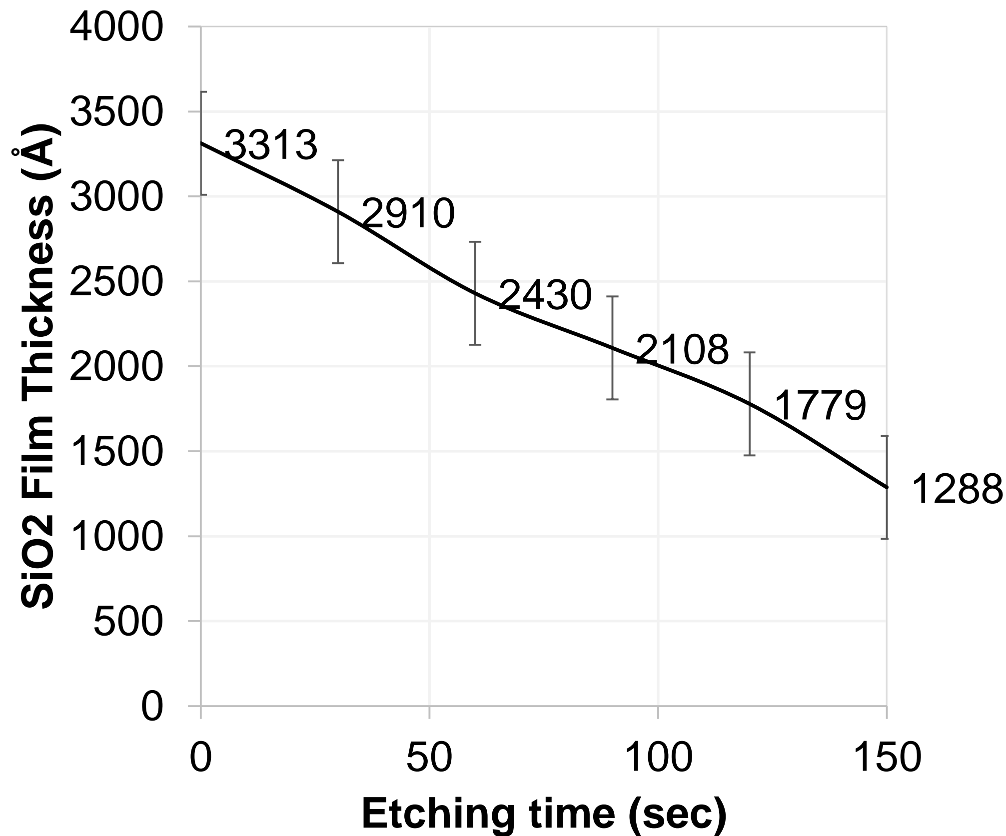



**Figure 55 Plot of Etch Rate for $SiO_2$ Film**

Figure 56 is the picture of wafer before and after etching with HF mixture. After oxide photolithography, the remaining PR on the wafer works as a barrier to protect SiO2 film, as represented by a microscope picture in Figure 57.

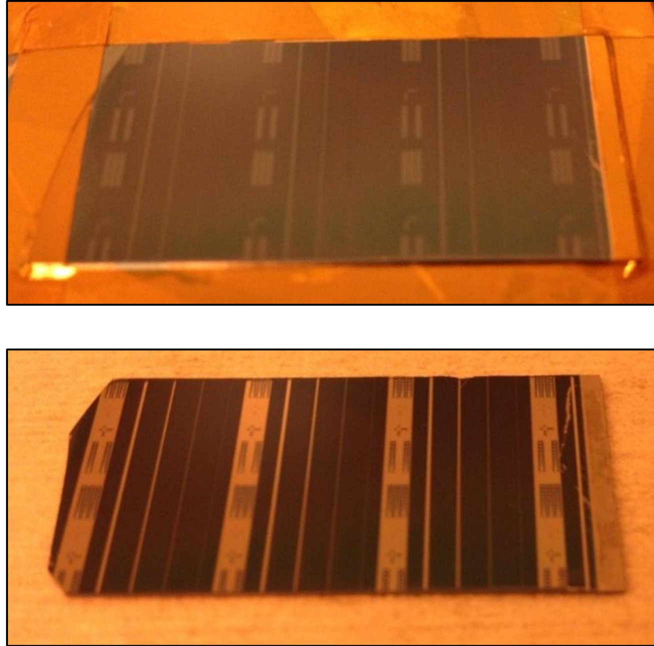


**Figure 56 Pictures of before(above) and after(below) $SiO_2$ etching**

**Figure 57 Microscope picture of 100µm width stripe window before(left) and after(right) $SiO_2$ etching (20x Mag.)**

2.5 <u>Metal Deposition Process</u>

In order to have electrical contacts on each side of the deuce, two deposition processes are needed. The contact metallization is important for minimizing contact resistance, and for maintaining better improved contact adhesion. Necessarily, this requires an ohmic contact, which is a non-rectifying junction. The ohmic contact is an

electrical junction between two conductors which has a linear current versus voltage curve. This allows charge to move easily both directions between two conductors, unlike a diode which allow charge to flow just one direction [33]. On the other hand, the current-voltage curve of the Schottky contact has diode characteristic as shown in Figure 58 [34]. Figure 59 depicts energy band diagram that demonstrates that the depletion region makes potential barrier for blocking moving electrons between both sides [35]. The titanium film (p-side) is used for adhesion like a glue layer between the $SiO_2$ insulating layers and the conduct layer. The platinum film is deposited as diffusion barrier for preventing interdiffusion between the titanium and gold layers.

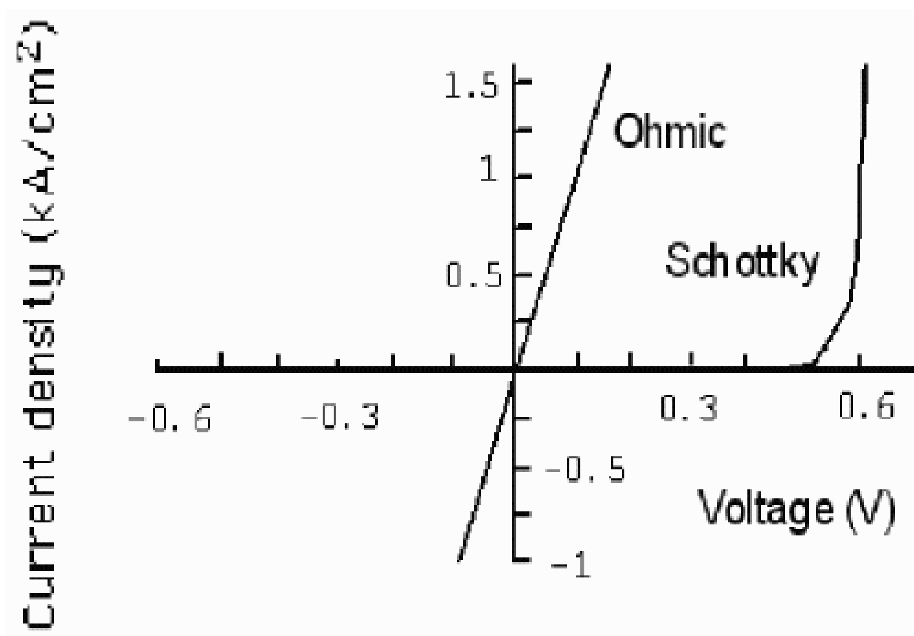



**Figure 58 Current-voltage characteristics of ohmic and Schottky barrier metal-semiconductor contacts to GaAs [33]**

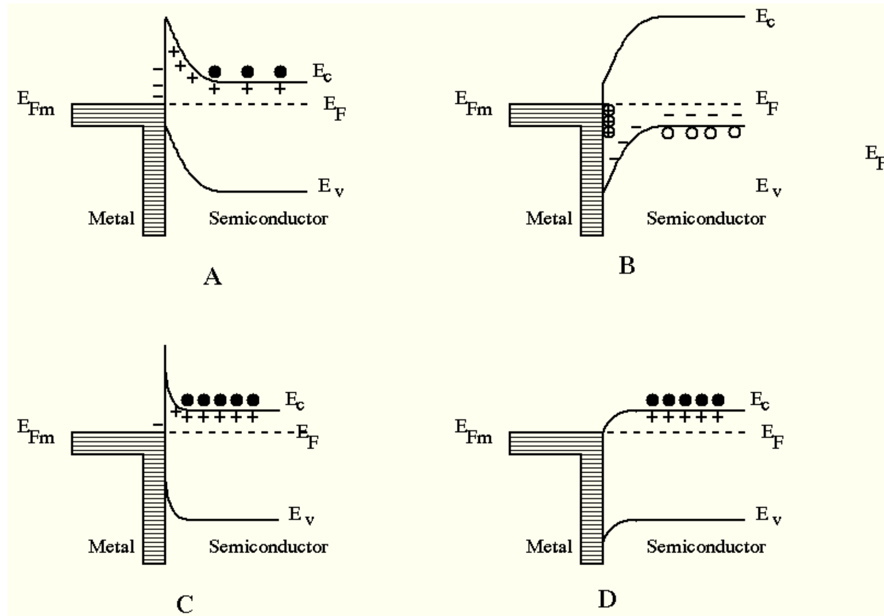



**Figure 59 Energy diagram of (A) Metal to n-type semicondutor Schottky diode (B) Metal to p-type semicondutor Schottky diode (C) Metal to n-type Schottky diode becoming ohmic due to tunneling (D) Metal to n-type ohmic contact**

In this work, Ti/Pt/Au is deposited on top of fabricated laser for the P-side contact. This metallization system has been widely used for semiconductor lasers [36][37]. Ti is used because it has proven effective in reducing surface contamination when incorporated in ohmic contacts on GaAs. Pt is deposited as a diffusion barrier and Au is deposited for a contact. The thickness of metallization is 150Å titanium, 1000Å platinum and 1500 Å gold. These thicknesses are not critical to the performance but the deposit order is crucial.

For the N-side contact, AuGe/Ni/Au is used as it has been shown to produce uniform ohmic electrical contacts to GaAs over a large resistivity ranges [38][39][40]. 400Å of AuGe, 200Å of Ni, and 1500Å of Au are deposited by E-beam evaporator under high vacuum. That is an electron beam evaporator which uses a high-energy beam from

an electron gun to boil a solid metal in a small pocket. Since the heating is not uniform, lower vapor pressure materials can be deposited. Ti and AuGe alloy are both used for adhesion between insulators and conductive metallic layers.

After the deposition process, annealing step is performed for metal contacts. Annealing consists of three steps: heating to critical temperature, maintaining a suitable temperature, and cooling [41]. Annealing heats the deposited metal and GaAs substrate to repair crystalline damage, and it reduces the internal stresses [42]. The anneal serves to create the alloy between Ti/GaAs and AuGe/GaAs which reduces contact resistance

## 2.6 Bonding Process

In this step, the fabricated laser is physically attached to the C-mount heat sink with Indium solder as shown in Figure 60. Indium solder is one of the most widely used solders in semiconductor laser die bonding [43]. The reliability and performance of the semiconductor laser are affected by the thermal properties of the laser construction. To melt the indium solder, a hot plate was set to 180℃ (melting point of Indium: 156℃).

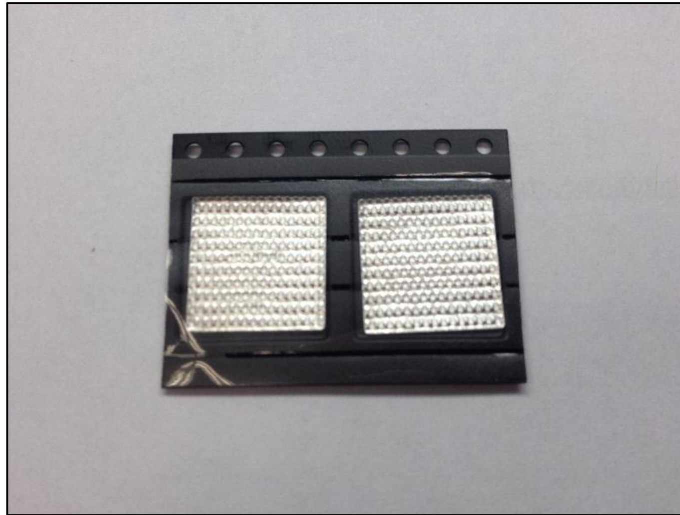


**Figure 60 Picture of two Indium solder preforms.**

After 5 minutes heating, the C-mount heat sink is put on the hot plate with guide as shown in Figure 61. The guide holds the C-mount heat sink in place during the die attach process. First, the indium solder is put on the top of the heat sink. After the indium has melted (~2 minutes), the solder is spread by a tweezer. Next, the heat sink is allowed to cool. After cooling, the indium is spread uniformly using sandpaper to better improve adhesion with the semiconductor laser. The semiconductor laser is put on top of the indium pad and the temperature is once again raised to 180°C to solder the chip to the heat sink. Ideally, a die bonder would be used for this process. However, due to we have not, this step had to be completed manually. It is a crude method in several ways –

amount of indium solder, uniformity of spread indium solder, proper bonding pressure and upright bonding position.

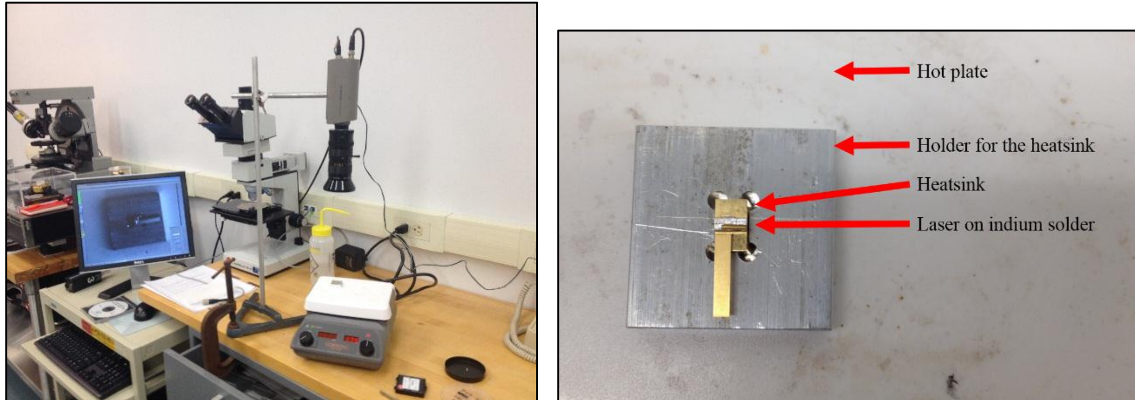



**Figure 61 The experiment setting for die bonding**

After the die bonding process, wire bonding is performed with K&S 4700 (Julicke & Soffa) dual manual wire bonder as shown in Figure 62. Six wires are bonded for one semiconductor laser, as the fusing current of 25μm diameter gold wire is 0.6A [44]. Figure 63 shows the result of the wire bonding process.

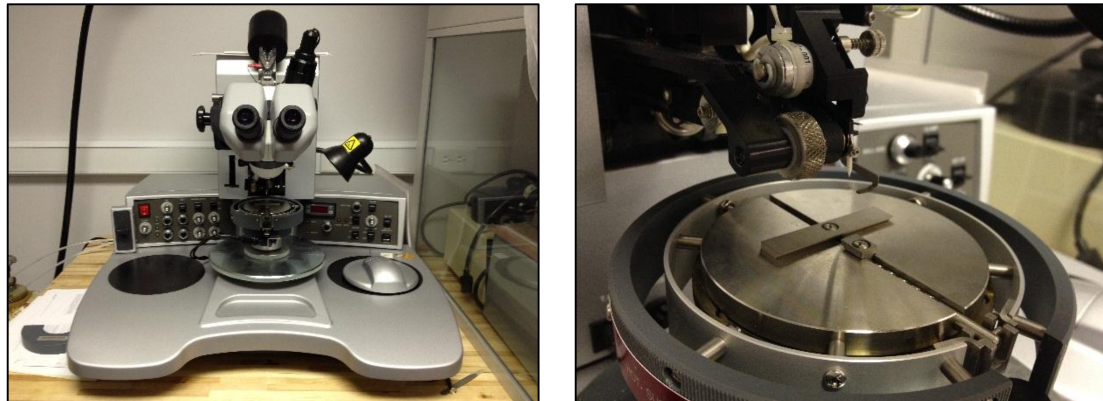


**Figure 62 The picture of wire bonder K&S 4700 by Kulicke & Soffa Co.**

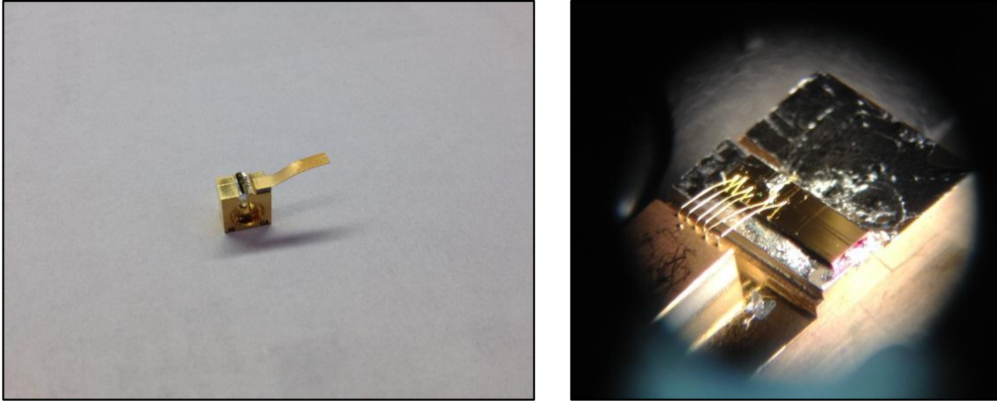
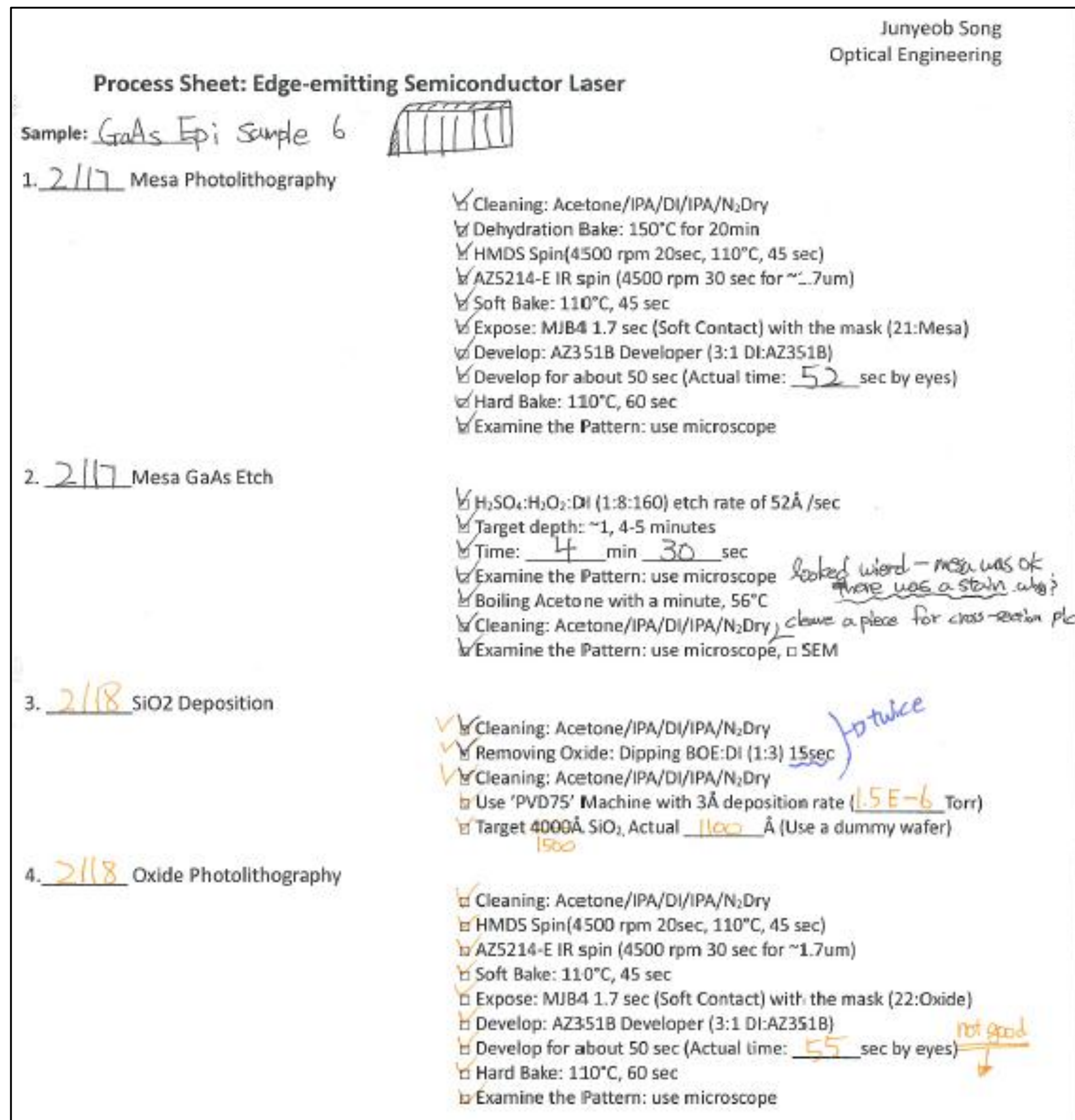


**Figure 63 The picture of bonded semiconductor laser on the heat sink**

## 2.7 Final Process

After die attachment & wire bonding, the fabrication process is complete, and the chip is ready for testing. The process traveler which summarizes the entire process is presented in Figure 64 and summarized in Table 4.



Junyeob Song
Optical Engineering

**Process Sheet: Edge-emitting Semiconductor Laser**

**Sample:** GaAs Epi Sample 6

1. 2/17 Mesa Photolithography

- ☑ Cleaning: Acetone/IPA/DI/IPA/$N_2$Dry
- ☑ Dehydration Bake: 150°C for 20min
- ☑ HMDS Spin(4500 rpm 20sec, 110°C, 45 sec)
- ☑ AZ5214-E IR spin (4500 rpm 30 sec for ~1.7um)
- ☑ Soft Bake: 110°C, 45 sec
- ☑ Expose: MJB4 1.7 sec (Soft Contact) with the mask (21:Mesa)
- ☑ Develop: AZ351B Developer (3:1 DI:AZ351B)
- ☑ Develop for about 50 sec (Actual time: 52 sec by eyes)
- ☑ Hard Bake: 110°C, 60 sec
- ☑ Examine the Pattern: use microscope

2. 2/17 Mesa GaAs Etch

- ☑ $H_2SO_4$:$H_2O_2$:DI (1:8:160) etch rate of 52Å /sec
- ☑ Target depth: ~1, 4-5 minutes
- ☑ Time: 4 min 30 sec
- ☑ Examine the Pattern: use microscope looked wierd – mesa was ok there was a stain why?
- ☑ Boiling Acetone with a minute, 56°C
- ☑ Cleaning: Acetone/IPA/DI/IPA/$N_2$Dry cleave a piece for cross-section
- ☑ Examine the Pattern: use microscope, ☐ SEM

3. 2/18 SiO2 Deposition

- ☑ Cleaning: Acetone/IPA/DI/IPA/$N_2$Dry
- ☑ Removing Oxide: Dipping BOE:DI (1:3) 15sec — twice
- ☑ Cleaning: Acetone/IPA/DI/IPA/$N_2$Dry
- ☑ Use 'PVD75' Machine with 3Å deposition rate (1.5 E−6 Torr)
- ☑ Target 4000Å $SiO_2$ Actual 1100 Å (Use a dummy wafer) 1500

4. 2/18 Oxide Photolithography

- ☑ Cleaning: Acetone/IPA/DI/IPA/$N_2$Dry
- ☑ HMDS Spin(4500 rpm 20sec, 110°C, 45 sec)
- ☑ AZ5214-E IR spin (4500 rpm 30 sec for ~1.7um)
- ☑ Soft Bake: 110°C, 45 sec
- ☑ Expose: MJB4 1.7 sec (Soft Contact) with the mask (22:Oxide)
- ☑ Develop: AZ351B Developer (3:1 DI:AZ351B)
- ☑ Develop for about 50 sec (Actual time: 55 sec by eyes) not good
- ☑ Hard Bake: 110°C, 60 sec
- ☑ Examine the Pattern: use microscope

6. _________P-Side Metal Deposition (UIUC)
   - □ Ti / Au: 1500Å / 1500Å
7. _________Lap & Polish
8. _________N-Side Meteal Deposition (UIUC)
   - □ AuGE / Ni / Au: 400Å / 200Å / 1500Å
9. _________Cleave
10. _________Die Attach
    - □ Cutting: Indium solder
    - □ Melting: Indium solder (180°C, 5min) on heat sink
    - □ Cooling
    - □ Spread Indium Solder Uniformly: using a sandpaper
    - □ Heating (180°C, 5min)
    - □ Putting the sample onto heat sink
    - □ Pressing the chip gently using a backside of tweezer
11. _________Wire Bond
    - □ Bonding: Au 25umΦ six wires

**Figure 64 Captured image of process sheet**

**Table 4 Summary of determined parameter for fabrication lasers**

| **Photolithography process** | |
|---|---|
| Spin coating | 4500RPM for 30 seconds for 1.7µm |
| Softbake | 110℃ for 45 seconds |
| Exposure | 13mW/cm$^2$, for 5 seconds at 365nm |
| Develop | AZ351B:DI (1:3) for 50 seconds |
| Hardbake | 110℃ for 60 seconds |
| **Etching for GaAs** | $H_2SO_4$ : $H_2O_2$ : DI(1:8:160)<br>Etch rate: 43Å/sec |
| **Etching for SiO2** | HF: DI(1:25)<br>Etch rate: 13.18 Å /sec |

# 3. LASER CHARACTERIZATION

After all processing is completed, the semiconductor laser is characterized in an optical laboratory. For this measurement, current is supplied by a LDX-36000 for a high power laser diode as shown in Figure 65, and the laser output is fed into a thermal power detector XLPF12-3S-H2-DO as shown in Figure 66. For spectral measurement, the laser out is coupled into a fiber through to AQ6370© optical spectrum analyzer made by Yokogawa. Parameters including voltage and power are measured with a digital multimeter. The optical beam is profiled in both the near-field and far-field.

For this characterization, two semiconductor laser chips are characterized. Table 5 shows the specifications. Device A is commercially bonded chip, Device B is bonded at Rose-Hulman institute of technology (RHIT), and Device C is fabricated and bonded at RHIT. Device A is coated 808nm laser with 100µm stripe and 1.5mm cavity length is bonded with a gold-tin (AuSn) solder on copper-tungsten (CuW) heatsink. This device was provided by nLight Corp (Vancouver, WA). Device B is 912nm wavelength laser but with uncoated, cleaved, and bonded manually. Device C is 885nm wavelength laser with 1.5mm cavity length, uncoated, cleaved, and bonded manually.

**Table 5 Specification of characterized devices[1]**

| | **Epi Growth** | **Wafer Fab.** | **Bond** | **Wave -length** | **Cavity Length** | **Emitter Length** | **Bond Orientation** | **Test Condition** |
|---|---|---|---|---|---|---|---|---|
| **Device A** | @nLight | @nLight | @nLight | 808nm | 1.5mm | 95µm | Junction down | CW, 25°C |
| **Device B** | @nLight | @nLight | @RHIT | 912nm | 3.5mm | 100um | Junction up | QCW*, 25°C |
| **Device C** | @nLight | @RHIT | @RHIT | 885nm | 1.5mm | 200um | Junction up | QCW*, 25°C |

* 500us of pulse duration, and 20% of duty cycle

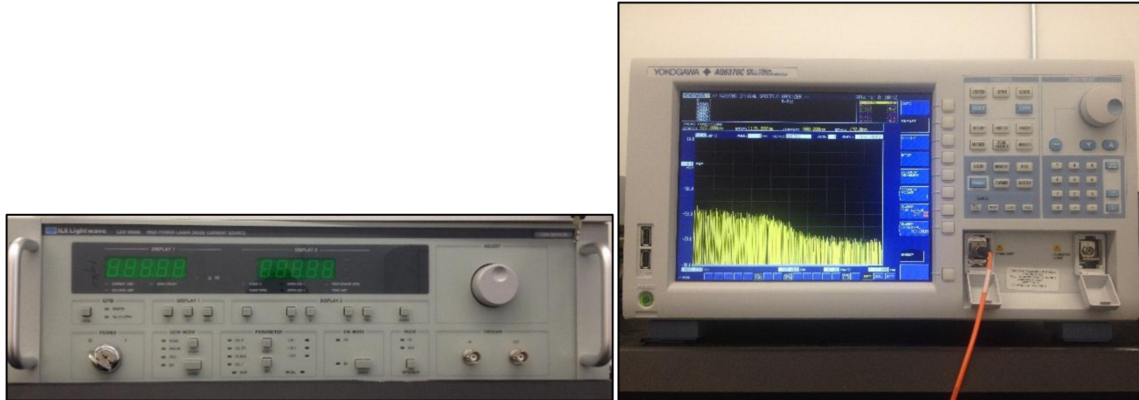



**Figure 65 The picture of a current source for semiconductor laser (LDX-36000) and optical spectrum analyzer (AQ6370© )**

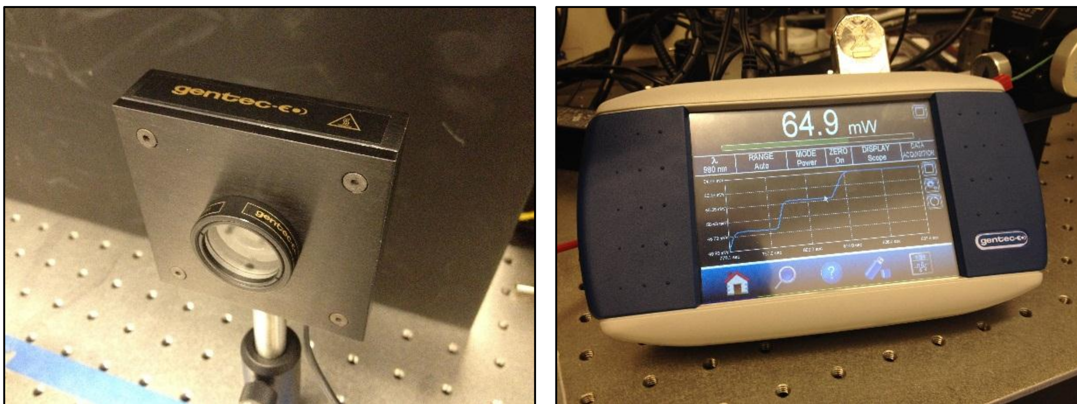


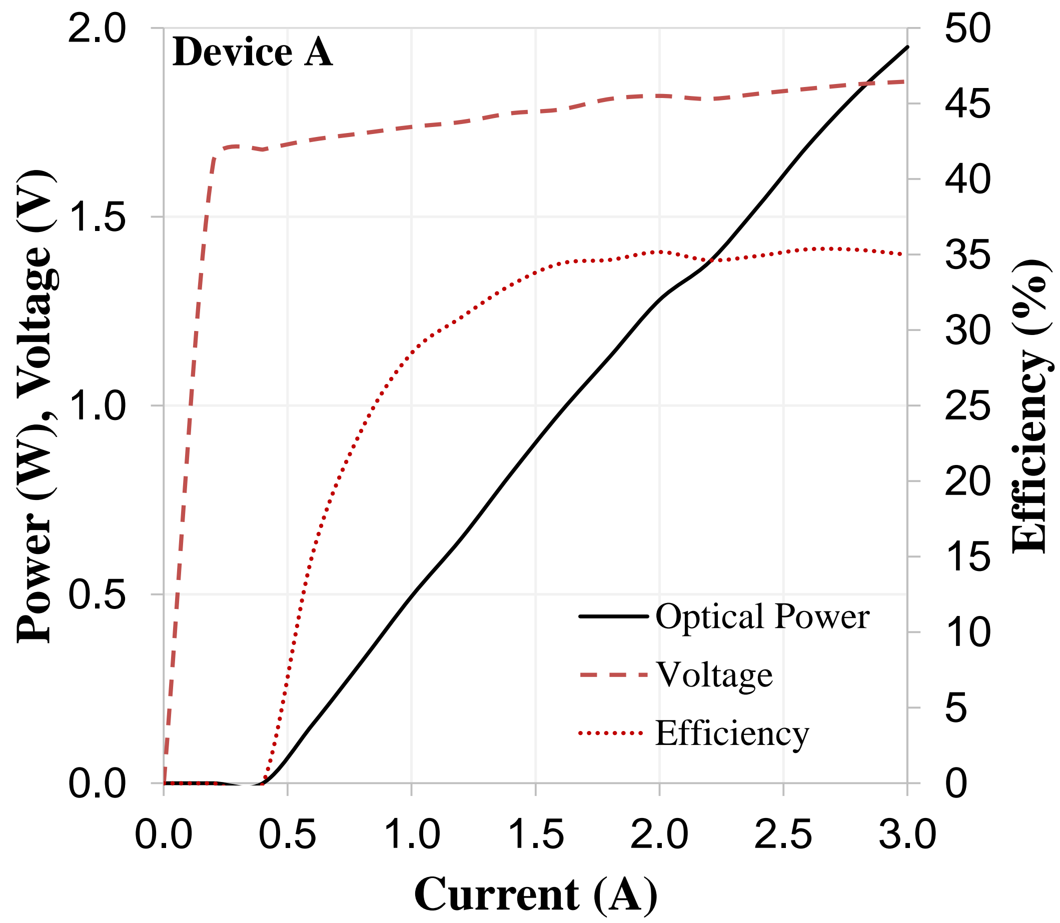

**Figure 66 The picture of equipment for measuring power of semiconductor laser**

### 3.1 Power, Voltage and Power conversion efficiency vs. Current

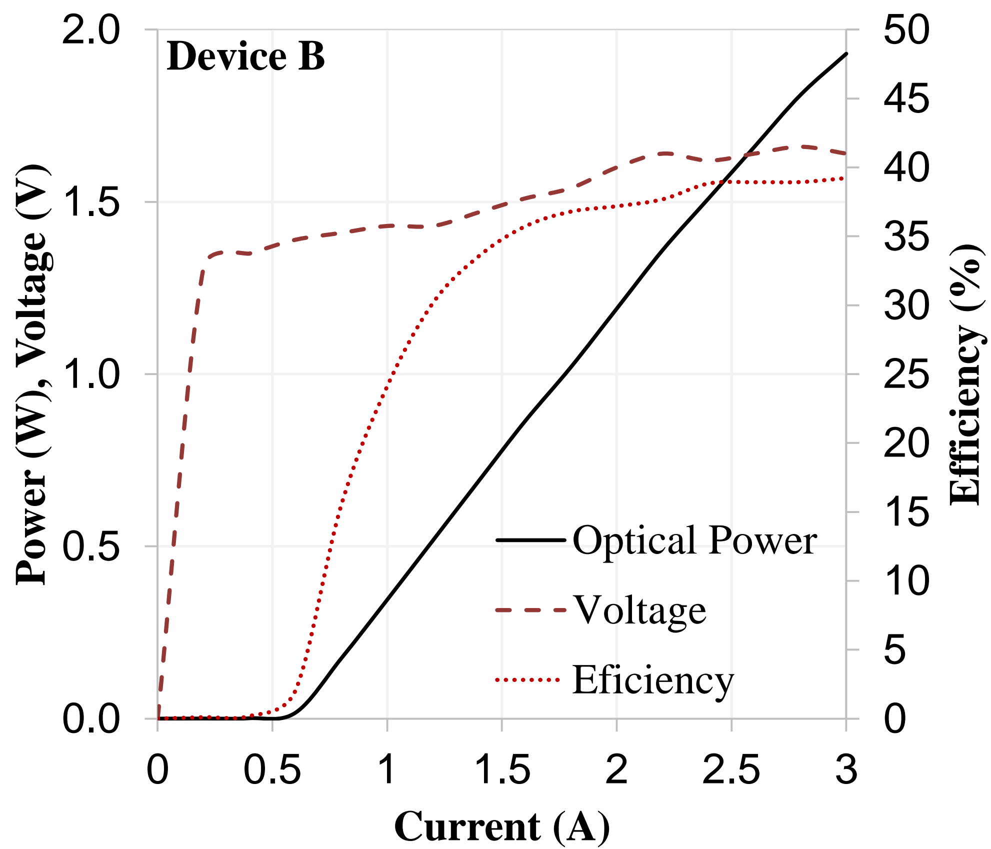
First of all, a basic test for the semiconductor laser is performed. This is called a light-current-voltage test, or L-I-V test. All semiconductor lasers have a light current characteristic, with a defined threshold current. The laser is connected to the current supply (LDX-36000), and the thermal power detector is set in front of the laser as shown in Figure 68.

Figure 67 shows optical power, voltage, and efficiency vs. current. For Device A (a), the laser threshold current is 0.4A, under the threshold where stimulated emission dominates and over the threshold where stimulated emission dominates, and quantum efficiency increase dramatically. A series resistance is calculated with slope of voltage plot in stimulated emission region. It is 63.6mΩ. It also presents that peak efficiency at 1.5A is 34% and maximum power is on the order 2A. This is measured until 3A until the efficiency slope is saturated. Device B (b) has 0.6A threshold current, 130mΩ series resistance, 39% peak efficiency at 2.4A. This difference in results shows that bond, and cleave quality affect the output parameters. Device C has 0.8A threshold current, and 11% peak efficiency at 2.4A.

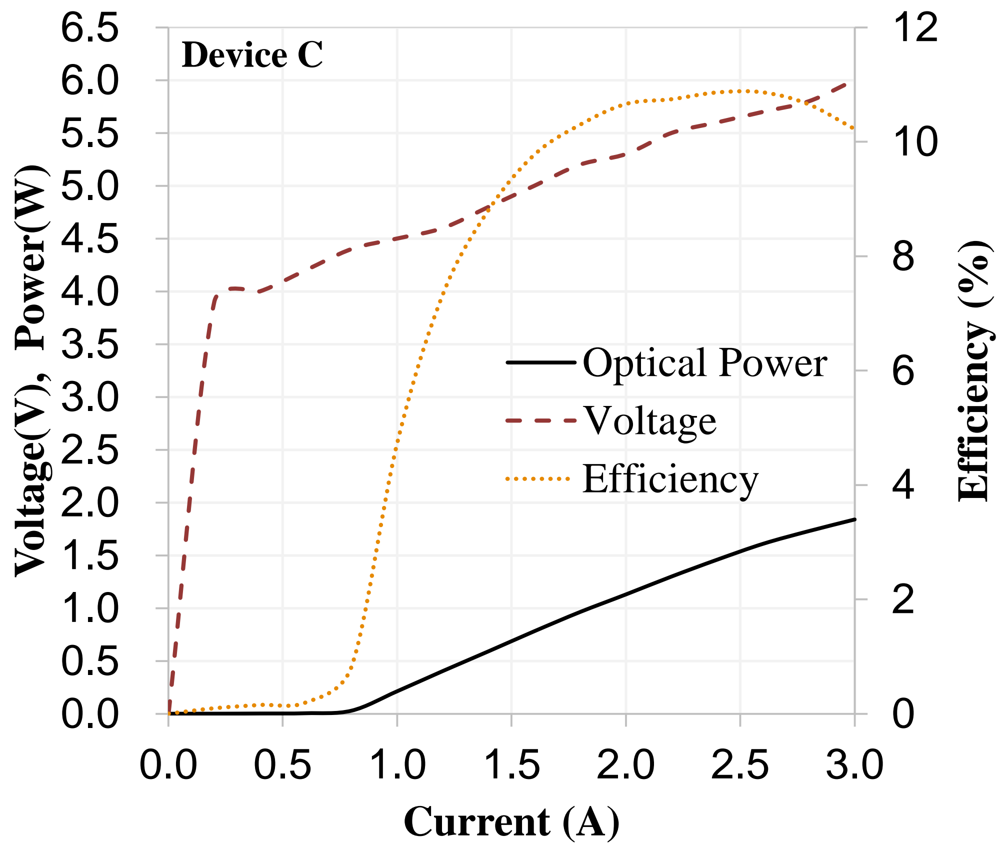
A continuous wave (CW) of injection current is used for Device A and a quasi-continuous wave is used for Device B and C, because of their difference of junction type. Device A is bonded junction down (the laser junction is close to the heat sink), it has less thermal resistance than device B and C bonded junction up [45].




**(a)**




**(b)**




**(c)**

**Figure 67 The plot of power, voltage and power conversion efficiency vs. injection currents for a high-power separately confined heterostructure quantum well semiconductor laser (a) Device A (b) Device B (c) Device C**

## 3.2 Spectrum at several current value

The spectra of Device A are measured by the spectrum analyzer (Yokogawa AQ6370© ) as shown in Figure 68. Figure 69 shows spectra at several injection current that plot presents the wavelength shifts by the injection current, because the spectrum depends on a temperature [46]. Increasing temperature makes spectral shift to the higher wavelength of the spectrum. The forward laser currents increases Joule heat and the laser chip temperature goes up as well.

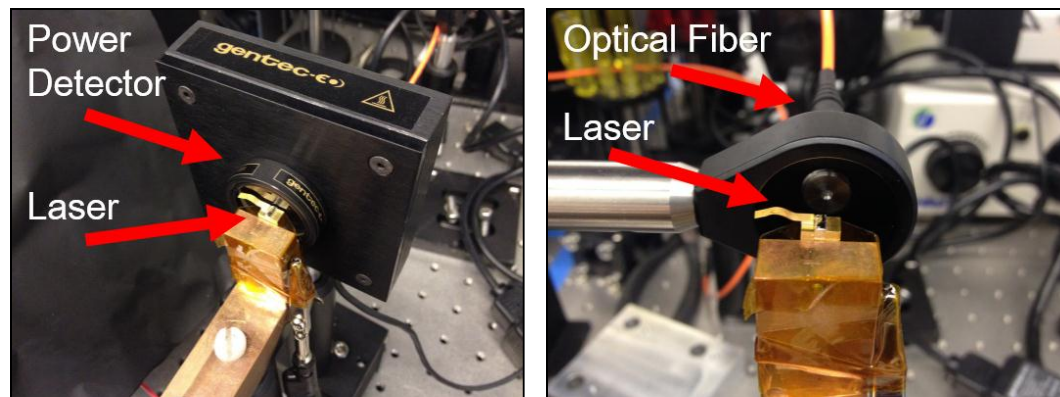



**Figure 68 The picture of the experiment set for measuring optical power and spectra**

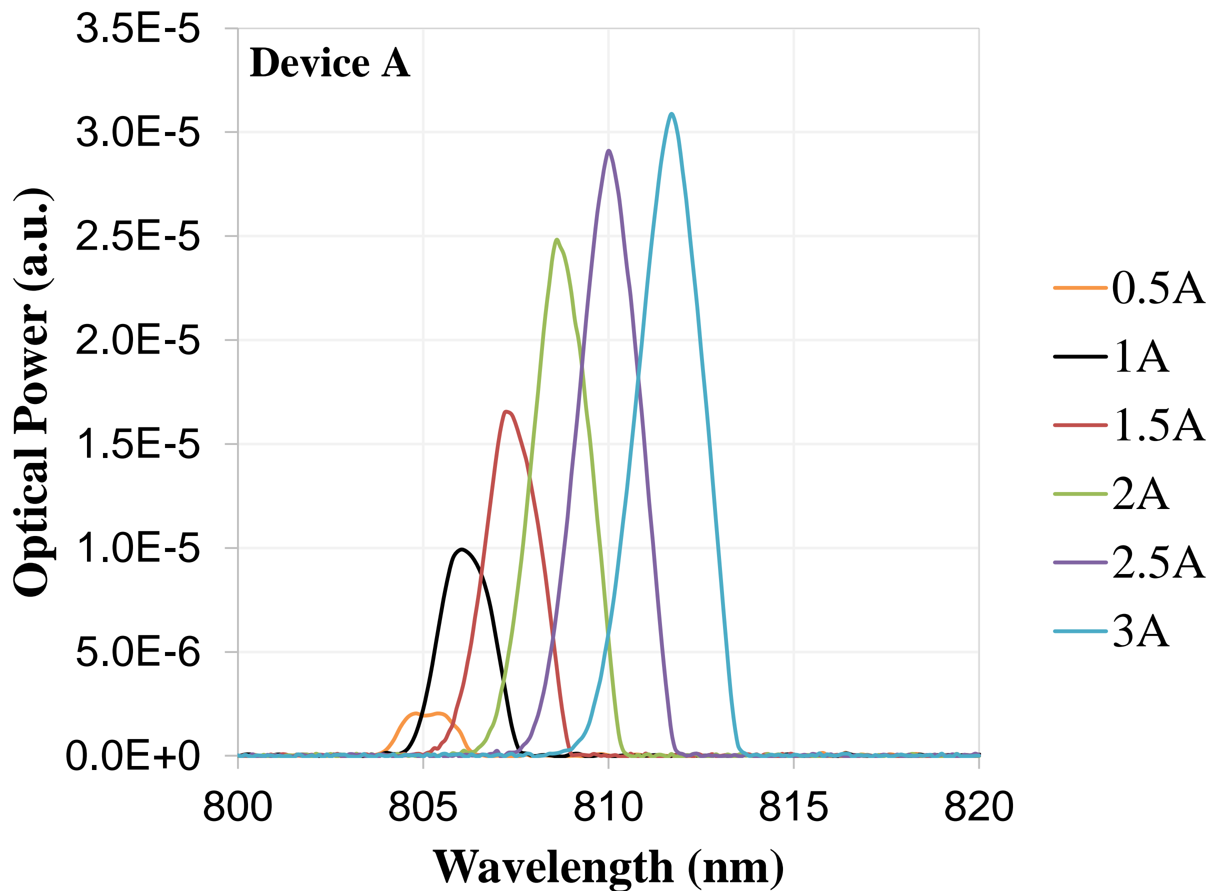



**Figure 69 Spectral characteristic at several injection currents**

The thermal resistance is calculated from Figure 70. This laser spectrum shifts 0.24nm per temperature, so the thermal resistance is 6.5℃ per Watt as shown in Equation 3.1.

$$812nm - 806nm = 6nm$$

$$\frac{6nm}{0.24nm/℃} = 25℃$$

$$\frac{25℃}{3.8W} = 6.5\,℃/W \tag{3.1}$$

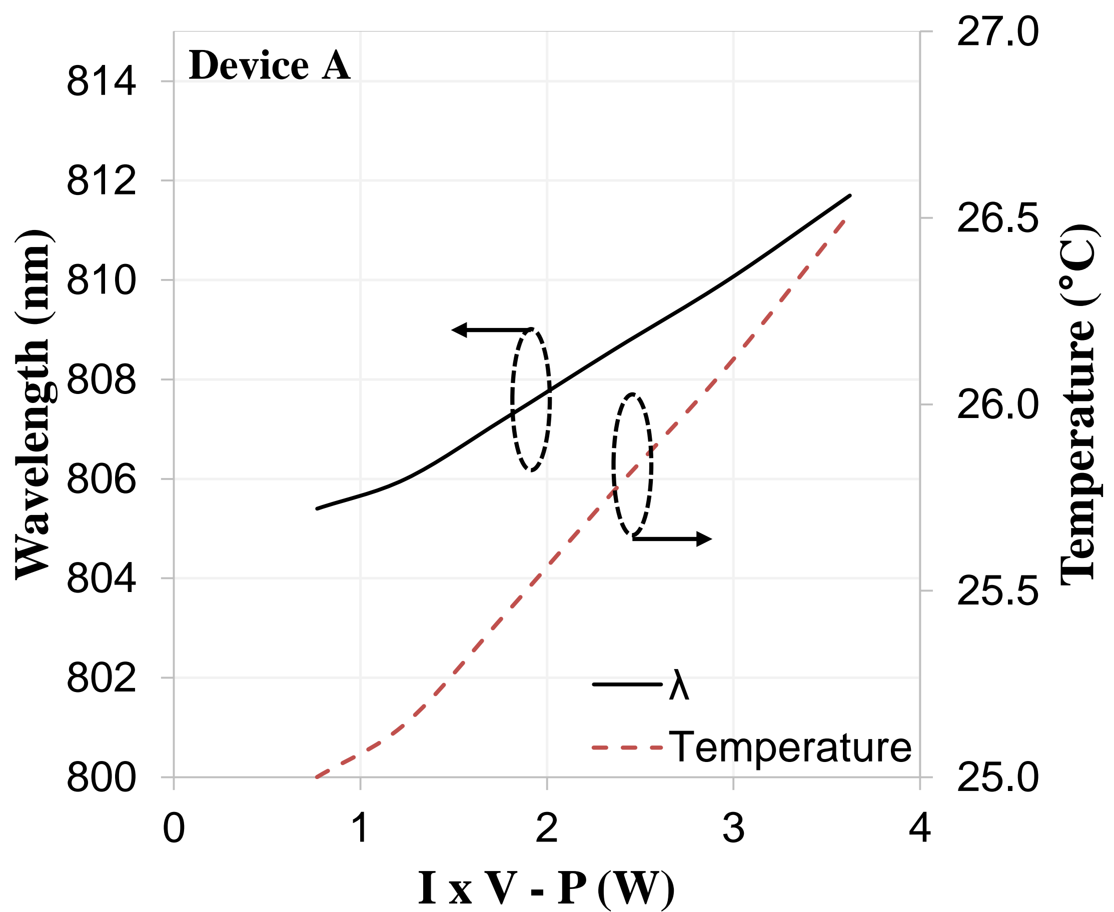



**Figure 70 The plot of spectrum wavelength and temperature vs. power differences**

FWHM of wavelength increases by injection current as shown in Figure 71. The FWHM is an expression of the extent of a function, given by the difference between the two extreme values of the independent variable at which the dependent variable is equal to half of its maximum value. The trend of values means gain spectrum is broader with injection current caused by the gain saturation, overheating of the active region.

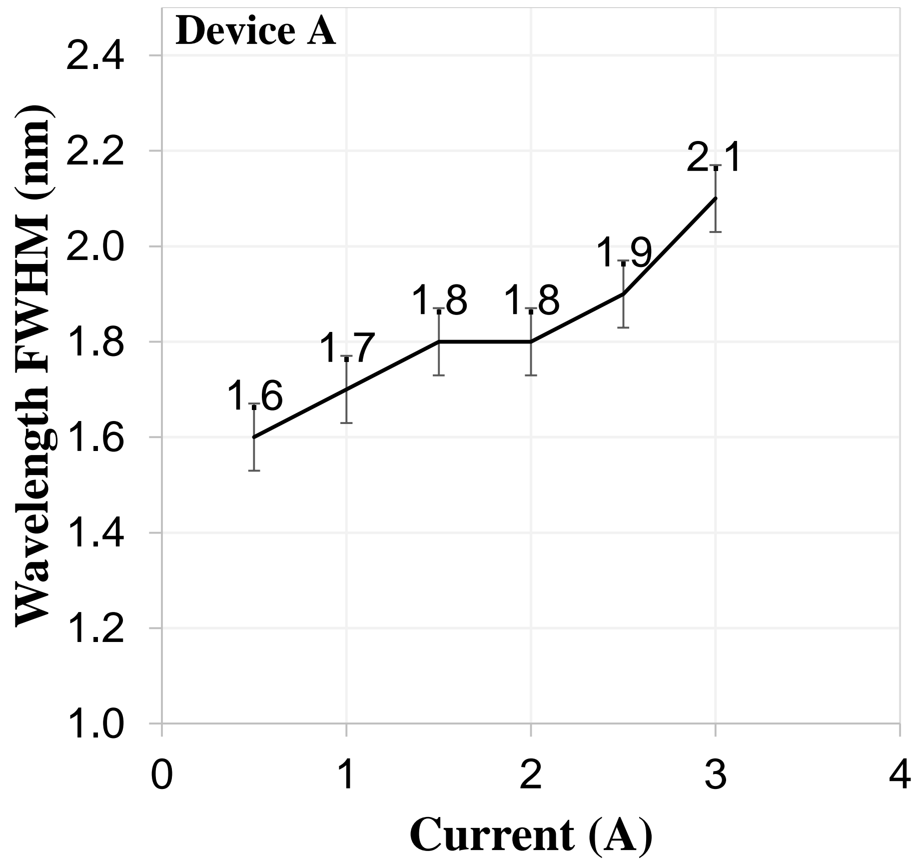



**Figure 71 The plot of wavelength FWHM vs. injection currents**

**Table 6 The calculated value of FWHM**

| I(A) | 0.5 | 1 | 1.5 | 2 | 2.5 | 3 |
|---|---|---|---|---|---|---|
| FWHM(nm) | 1.6 | 1.7 | 1.8 | 1.8 | 1.9 | 2.1 |

3.3 Near-field Measurement

Figure 72 shows a spatial emission profiles for diodes. Measuring these profiles are used for determine the shape of laser. The near-field measurement is one of the methods that figures out a beam profile. This profile shows a quality of laser beam. Figure 73 illustrates the experiment setup for near-field measurement. The CCD camera is on the translation stage for adjusting the focus of beam image. The wavefront in front of the facet of the laser through a microscope objective is captured by a CCD camera as shown in Figure 74.

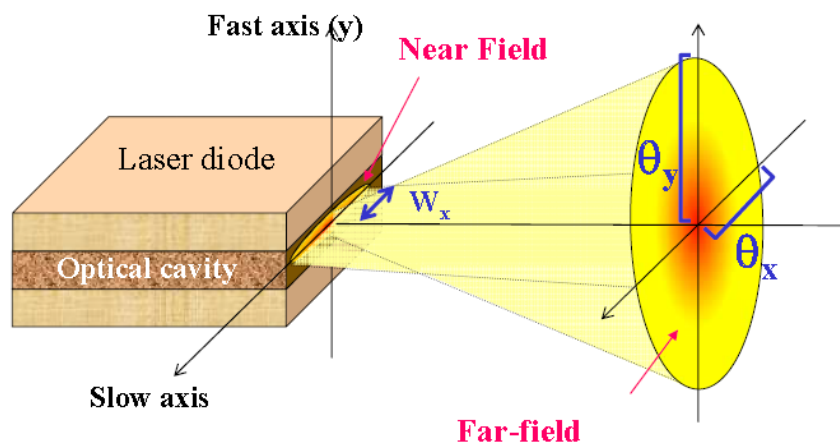



**Figure 72 The spatial emission for laser diodes**

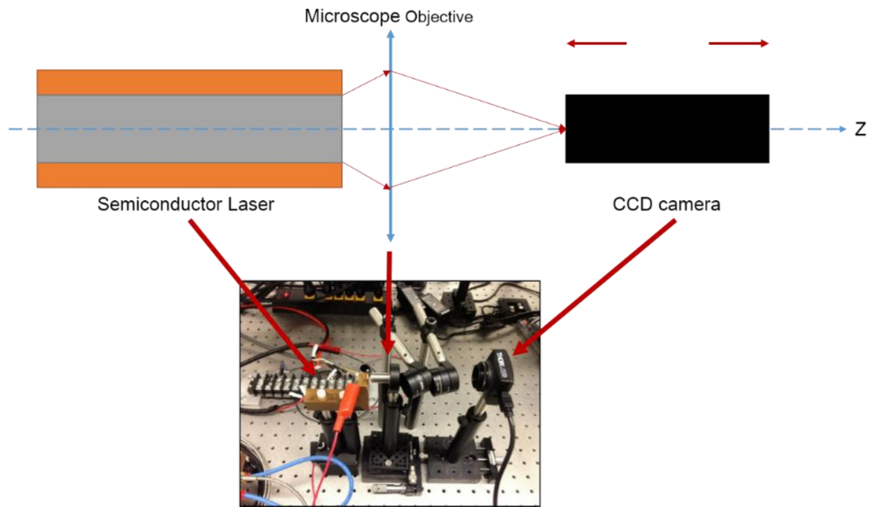
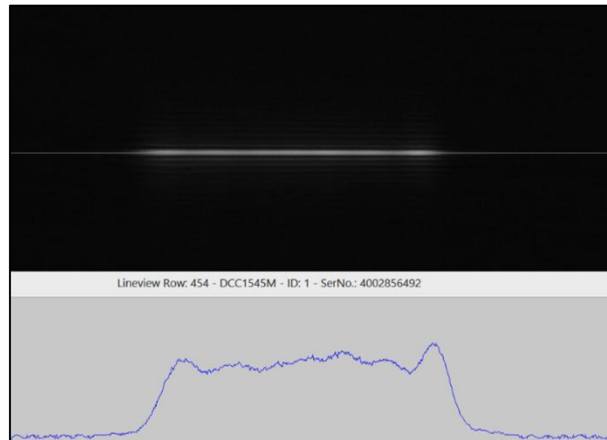
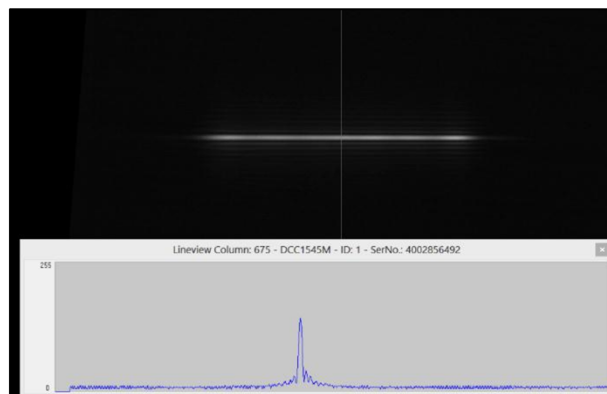



**Figure 73 The illustration of setup for near-field measurement**




**(a)**




**(b)**

**Figure 74 The profiles of near field measurement (a) at slow axis, (b) at fast axis**

3.4 Divergence (Far-field) Measurement

Lastly, the divergent beam from the laser is measured which has wide divergence because of a narrow emitter. Laser diode with an active layer emits coherent light with far-field angular divergence in the plane. The angular divergence determines the far-field radiation pattern. Because the active layer size is small, the laser diode is characterized by an angular divergence larger than that of other common lasers. The detector is set on the rotation stage by connecting with four long posts, 100μm slit is used in front of the detector as shown in Figure 75. Figure 76 shows a profile of device A. The injection current is 0.4A and calculated FWHM is 5.5.

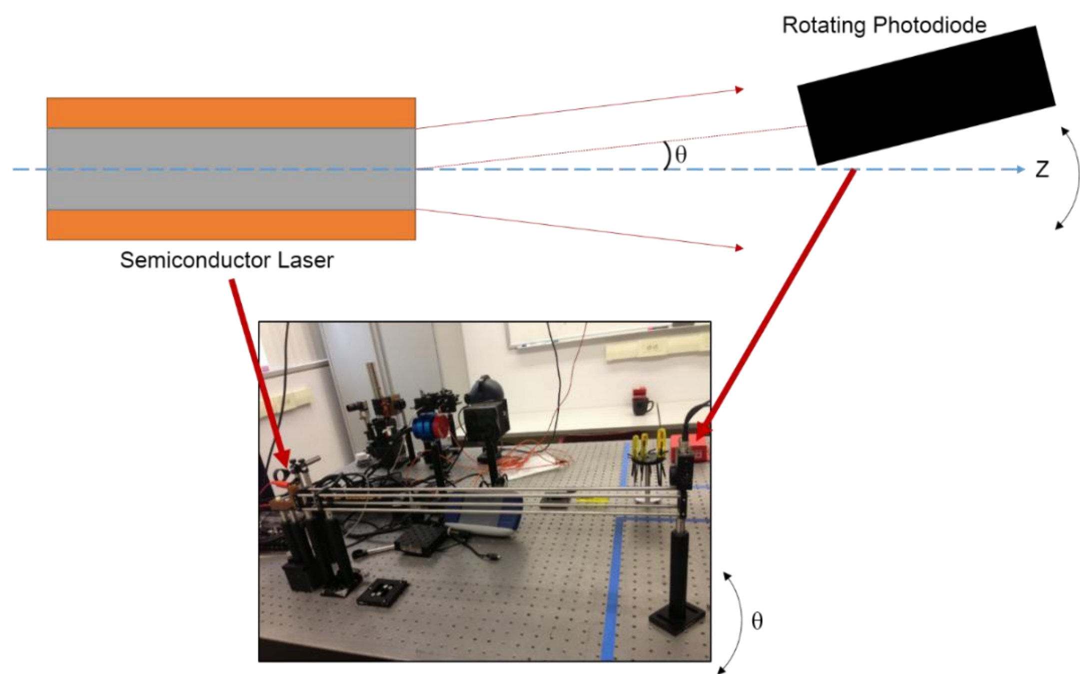



**Figure 75 The illustration of setup for far-field measurement**

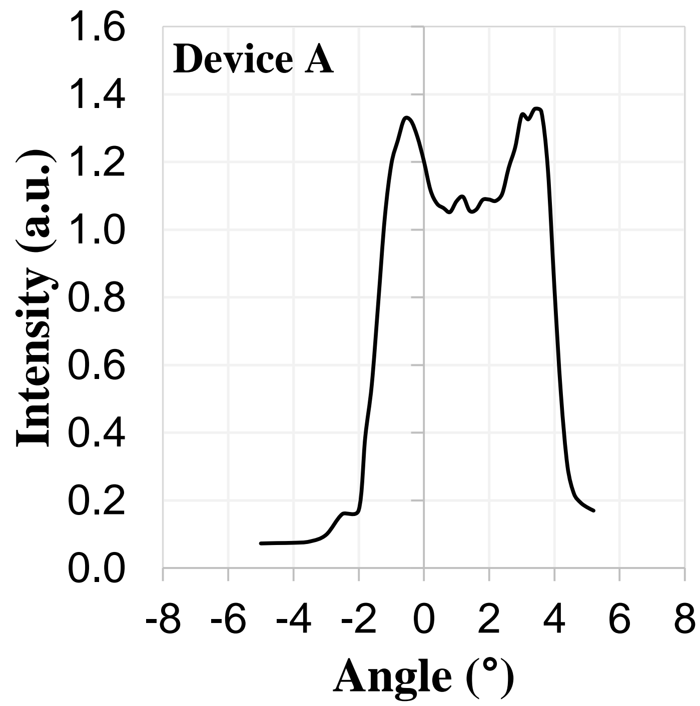



**Figure 76 The plot of far-field measurement**

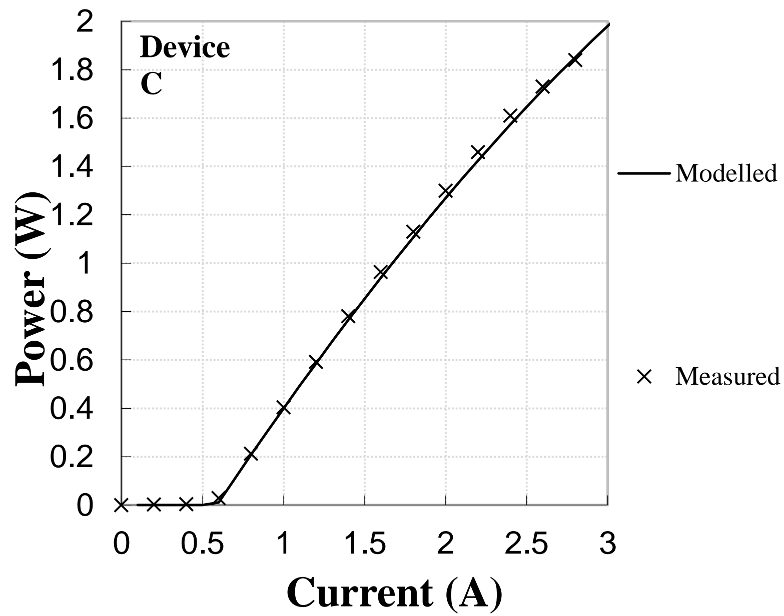
## 3.5 Analysis

In this section the characterization results of Device A, B, and C are discussed. According to Figure 67, LIV characteristics can be compared. Device A, and B showed similar curve trends that mean the die attach process and wire bonding process worked at RHIT were completed successfully. In spite of that Device A was fabricated in the company, even though the efficiency of Device B is better than Device A. On the other hand, the efficiency of Device C is lower than other devices – 11%. This is because the diode voltage was much higher as compared with others. Device C was made with the same die attach and wire bonding process but with a different metallization process. To step down the higher voltage, different metal layers should be used, or an annealing process should be carried out.

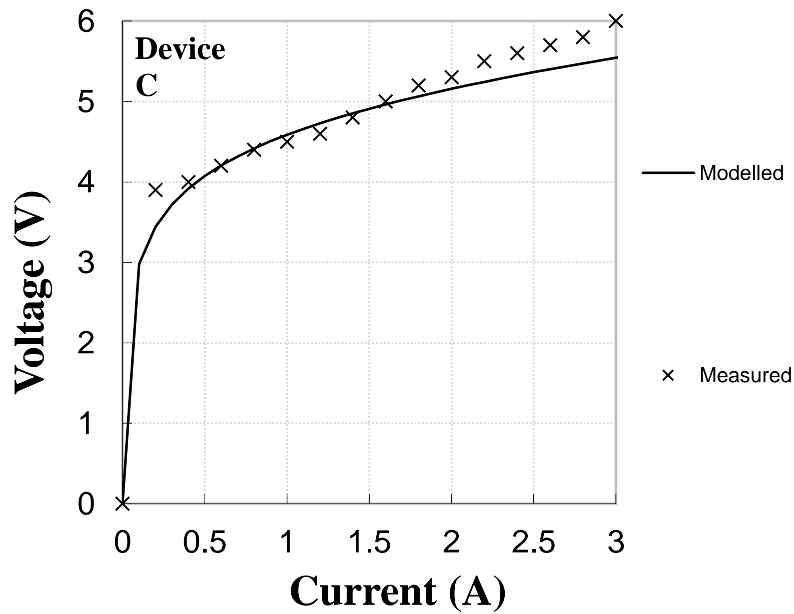
Table 7 shows the parameters for modelling the semiconductor laser which is Device C. This modelling is based on the rate equations. Figure 77 shows the measured and modelled results with Device C. This device is uncoated, the reflections of both sides (Rth. Rfront) are used 30%.

**Table 7 Materials and device parameters for modelling of Device C**

| | | | |
|---|---|---|---|
| Cavity Length (μm) | 1500 | A (SHR) | 1.00E-05 |
| Emitter Width (μm) | 200 | B (Spon) | 1.00E-09 |
| # Emitters per Bar | 1 | C (Auger) | 1.00E-30 |
| Rth | 4.2 | J<->n constant | 5.41976E-16 |
| Rfront (%) | 0.3 | Modal Gain (cm-1) | 15 |
| Rback (%) | 0.3 | ηi | 85% |
| $\Sigma_j V_j$ (meV) | 650 | Jo (A/cm$^2$) | 100 |
| $\Sigma_i \sigma_i$ (Ωcm$^2$) | 6.50E-05 | Wavelength (nm) | 885 |
| Jdiode (A/cm2) | 3.00E+00 | αi (cm-1) | 0.4 |
| Additional Rs (Ω) | 1.00E-01 | To (K) | 110 |
| Temperature (°C) | 25 | T1 (K) | 450 |




**(a)**




**(b)**

**Figure 77 Modelling results of Device C (a) Power, (b) Voltage**

# 4. CONCLUSION

In this work, GaAs edge-emitting semiconductor lasers were fabricated and characterized. This required development of a cleanroom fabrication process from scratch. All fabrication took place in the MiNDS(Micro and Nano Device and Systems) cleanroom. The characterization included power vs. current behavior, voltage vs. current behavior and efficiency vs. current behavior, spectral characteristics, and near-field and far-field analysis, and the modelling for the device which fabricated at RHIT was carried out.

Mask design chapter was showed that the material, thickness and the critical dimension, which is smallest feature size, are considered. Sodalime glass is much less expensive than quartz and it was enough to fabricate masks for this work.

Photolithography process was performed with AZ5214E-IR photoresist and AZ351B developer. This photoresist can be used as both positive and negative. 1.7µm thickness was okay for mesa etching and oxide etching. HMDS vapor priming was also applied, and it was successful.

The etch rates of GaAs layer and $SiO_2$ oxide on GaAs wafer were determined. The ratio that 1 $H_2SO_4$: 8 $H_2O_2$: 160 DI mixture was used for GaAs layer and its rate was 52Å /sec. The ratio that 1 HF: 25 DI rate was mixed for SiO2 oxide etching and its rate was 13Å /sec. The metallization process is performed with E-beam evaporator. For P-side, Ti / Au: (1500Å / 1500Å ) was deposited and for N-side, AuGe / Ni / Au: 400Å / 200Å / 1500Å was deposited.

Indium solder was used for die attachment between the c-mount heatsink and the fabricated laser. It was performed on the hot plate. The gold wire of 25μm diameter was also selected to wire bond, and 6 wires was bonded for this semiconductor laser.

The result showed that the fabricated semiconductor could potentially attain better performance. Future work will be centered around the goal of increasing output efficiency. One method could include using a tool designed for cleaving such as a wafer piler or dicing saw machine. This will provide better facet surface. Another method being considered is using a die bonder to reduce contact resistance, since the die bonder machine will yield better results than bonding by hand. For better efficiency, different metal layers will be used and an annealing process will be carried out for.

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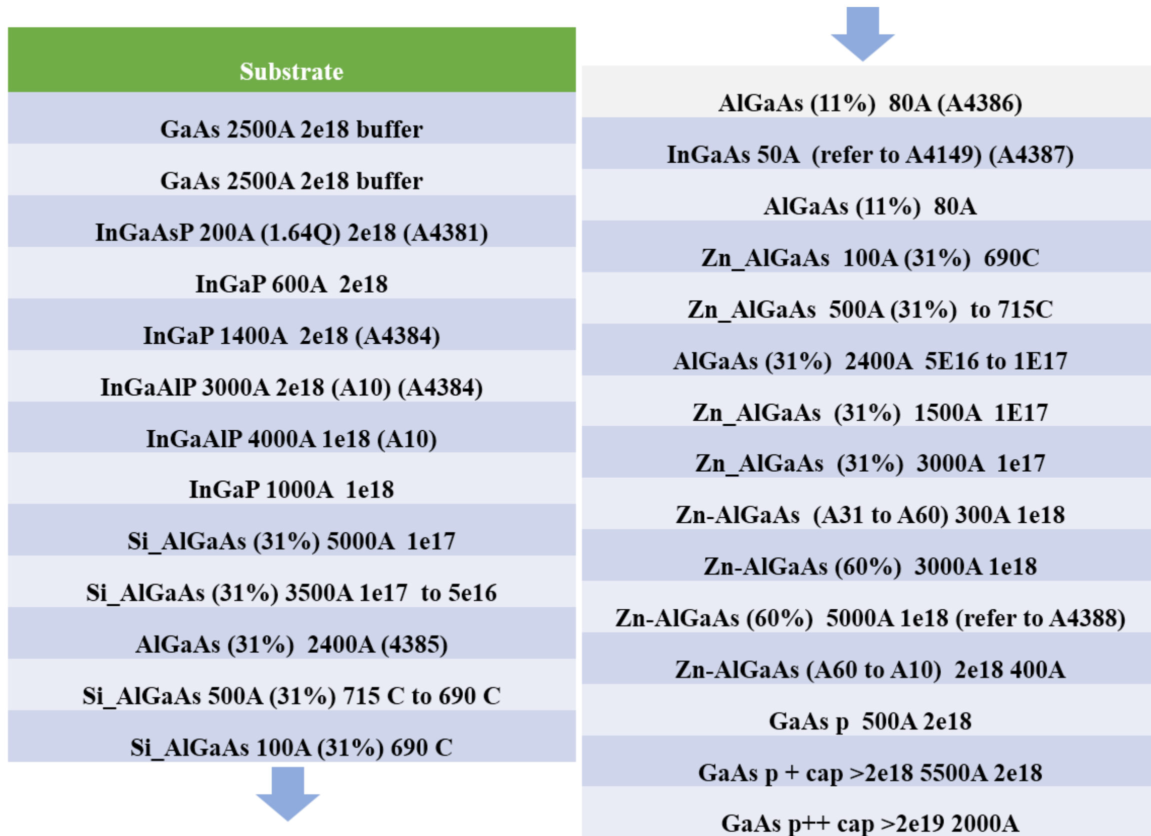
# APPENDIX A – Device C Epitaxial Structure design



# APPENDIX B – AZ5214E IR Data Sheet

Product Data Sheet

## AZ 5214 E

Image Reversal
Photoresist

## GENERAL INFORMATION

This special photoresist is intended for lift-off-techniques which call for a negative wall profile. Although they are positive photoresists (and may even be used in that way) comprised of a novolak resin and naphthoquinone diazide as photoactive compound (PAC) they are capable of image reversal (IR) resulting in a negative pattern of the mask. In fact AZ 5214E is almost exclusively used in the IR-mode.

The image reversal capability is obtained by a special crosslinking agent in the resist formulation which becomes active at temperatures above 110°C and - what is even more important - only in exposed areas of the resist. The crosslinking agent together with exposed PAC leads to an almost insoluble (in developer) and no longer light sensitive substance, while the unexposed areas still behave like a normal unexposed positive photoresist. After a flood exposure (no mask required) this areas are dissolved in standard developer for positive photoresist, the crosslinked areas remain. The overall result is a negative image of the mask pattern.

As everybody knows a positive photoresist profile has a positive slope of 75 - 85° depending on the process conditions and the performance of the exposure equipment (only submicron-resists get close to 90°). This is mainly due to the absorption of the PAC which attenuates the light when penetrating through the resist layer (so called bulk effect). The result is a higher dissolution rate at the top and a lower rate at the bottom of the resist. When AZ 5214E is processed in the IR-mode this is reversed as higher exposed areas will be crosslinked to a higher degree than those with lower dose, dissolution rates accordingly. The final result will be a negative wall profile ideally suited for lift-off.

The most critical parameter of the IR-process is reversal-bake temperature, once optimised it must be kept constant within ± 1°C to maintain a consistent process. This temperature also has to be optimised individually. In any case it will fall within the range from 115 to 125°C. If IR-temperature is chosen too high (>130°C) the resist will thermally crosslink also in the unexposed areas, giving no pattern. To find out the suitable temperature following procedure is suggested:

Coat and prebake a few substrates with resist. Without exposing them to UV-light subject them to different reversal-bake temperatures, i.e. 115°, 120°, 125° and 130°C. Now apply a flood exposure of > 200mJ/cm² and afterwards immerse them into a standard developer make up, i.e. AZ 351B, 1:4 diluted, or AZ 726 MIF for 1 minute. From a part of the substrates the resist will be removed, another part (those exposed to a too high temperature) will remain with the resist thermally crosslinked on it. Optimum RB-temperature now is 5° to 10°C below the temperature where crosslinking starts.

The flood exposure is absolutely uncritical as long as sufficient energy is applied to make the unexposed areas soluble. 200 mJ/cm² is a good choice, but 150 - 500 mJ/cm² will have no major influence on the performance.

Finally it should be noted that the imagewise exposure energy is lower than with normal positive processes, generally only half of that. So a good rule of thumb is: compared to a standard positive resist process, imagewise exposure dose should be half of that, flood exposure energy double of that for AZ 5214E IR-processing.

Once understanding and being familiar with this IR-procedure it is quite simple to set up a different process for lift-off. A T-shaped profile can be achieved by the following process sequence:

The prebaked AZ 5214E photoresist is flood exposed (no mask) with a small amount of UV energy, just to generate some exposed PAC at the surface. Now the reversal-bake is performed to partially crosslink this top areas. By this treatment a top layer with a lowered dissolution rate compared to the bulk material is generated. After this the resist is treated like a normal positive photoresist (imagewise exposure and development) to generate a positive image! Due to the lower dissolution rate in the top layer a T-shaped profile with overhanging lips will be the result.

## PHYSICAL and CHEMICAL PROPERTIES

| | | AZ 5214E | |
|---|---|---|---|
| Solids content [%] | | 28.3 | |
| Viscosity [cSt at 25°C] | | 24.0 | |
| Absorptivity [l/g*cm] at 377nm | | 0.76 | |
| Solvent | | methoxy-propyl acetate (PGMEA) | |
| Max. water content [%] | | 0.50 | |
| Spectral sensitivity | | 310 - 420 nm | |
| Coating characteristic | | striation free | |
| Filtration [µm absolute] | | 0.1 | |

## FILM THICKNESS [µm] as FUNCTION of SPIN SPEED (characteristically)

| spin speed [rpm] | 2000 | 3000 | 4000 | 5000 | 6000 |
|---|---|---|---|---|---|
| | | | | | |
| AZ 5214E | 1.98 | 1.62 | 1.40 | 1.25 | 1.14 |
| | | | | | |

## PROCESSING GUIDELINES

| Dilution and edge bead removal | AZ EBR Solvent |
|---|---|
| Prebake | 110°C, 50", hotplate |
| Exposure | broadband and monochromatic h- and i-line |
| Reversal bake | 120°C, 2 min., hotplate (most critical step) |
| Flood exposure | > 200 mJ/cm² (uncritical) |
| Development | AZ 351B, 1:4 (tank, spray) or AZ 726 (puddle) |
| Postbake | 120°C, 50s hotplate (optional) |
| Removal | AZ 100 Remover, conc. |

## HANDLING ADVISES

Consult the Material Safety Data Sheets provided by us or your local agent!
This AZ Photoresists are made up with our patented safer solvent PGMEA. They are flammable liquids and should be kept away from oxidants, sparks and open flames.
Protect from light and heat and store in sealed original containers between 0°C and 25°C, exceeding this range to -5°C or +30°C for 24 hours does not adversely affect the properties.
Shelf life is limited and depends on the resist series. The expiration date is printed on the label of every bottle below the batch number and coded as [year/month/day].
AZ Photoresists are compatible with most commercially available wafer processing equipment. Recommended materials include PTFE, stainless steel and high-density poly-ethylene and -propylene.