View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Scitech Research Journals

Boson Journal of Modern Physics (BJMP)
ISSN: 2454-8413

SCITECH RESEARCH ORGANISATION|
Volume 2, Issue 2
November 03, 2015|
Boson Journal of Modern Physics
www.scitecresearch.com

Design of QCA Full Adders without Wire Crossing

[*]Abbas Rezaei, [1]Abed Mostafaee, [2]Mohammad Mahdi Karkhanehchi , [3]Seyed Muhammad Jamshidi.

[*]Electrical Engineering Department, Kermanshah University of Technology, Kermanshah, Iran.
[1]Academic Center for Education, Culture and Research- Kermanshah, Iran.
[2]Academic Center for Education, Culture and Research- Kermanshah, Iran.
[3]Department of electronic Engineering, Kermanshah branch, Islamic Azad University, Kermanshah, Iran.

Abstract

In the scale of nanometer, Quantum-dot Cellular Automata (QCA) is a new technology, which utilizes the QCA cells in order to design and implement logical circuits. QCA makes it possible for us to design in Nano scale. Furthermore, in comparison to CMOS technology, it has highly low consumption power. Thus, in the future, QCA technology will be a powerful rival for VLSI. This paper presents two new and optimized QCA designs for Full adder. In comparison to the previous designs, all of the QCA Full adders presented in this paper are relatively optimized. In addition, they are implemented without any wire crossing. In order to test the proposed QCA Layouts and also display the results of the simulations, QCADesigner software is used.

Keywords: Quantum-dot Cellular Automata; QCA Cell; Full adder, Design.

1. Introduction

In the recent decades, high-voltage and high-consumption-power circuits, containing several dozen of transistors, were replaced by CMOS technology [1]. Based on the Moore's law the number of transistors on a chip would double every two years. Today`s CMOS technology encounters some problems such as physical limitations, high consumption power, limitations in decreasing channel length and decreasing the output resistance [2]. QCA is a new technology, which in comparison to CMOS technology, has a relative priority in the case of low consumption power, low area, high speed in data processing and transfer and also the ability for wires crossing on each other. A QCA cell is the basis element to design the QCA circuits, which is shown in Figure 1(a). Transferring data and also the QCA Gates implementation are based on the QCA cell. The cell is composed of four quantum dots ant two free electrons. According to the Coulomb Repulsion Law, the two free electrons move diagonally among the quantum points and present two stable states representing the logical 0 and 1 as shown in Figure 1(b) [3,4].

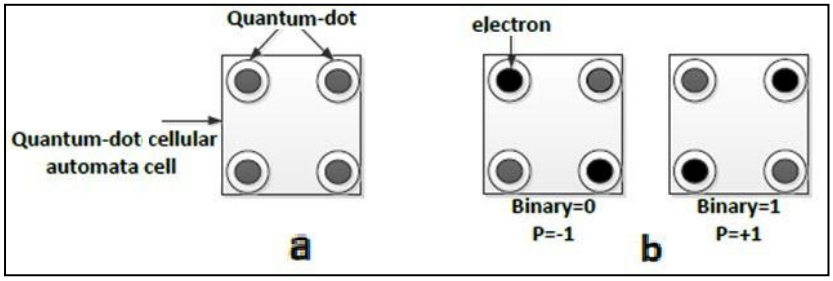

Figure 1. QCA.

A QCA wire is formed by joining a number of QCA cells by which a huge volume of data can be transferred at a high speed. There are two kinds of QCA wire. In the first one, the input cell polarization is duplicated over the adjacent cells. In the second one, the standard cells are placed in a diagonal orientation, which are geometrically similar to the 45°rotated cells in a horizontal orientation. Figures 2(a) and 2(b) shows these two QCA wires. Wires in QCA technology can cross each other without interference in two ways; coplanar crossing and multi-layer

crossing; which are shown in Figures 2(c) and 2(d), respectively. Majority gate is formed of 5 cells including 3 input cells, 1 output cell and 1 central cell. The output of majority Gate follows the central cell, and the central cell is a function of the input cells. The Figure 3(a) shows the Layout of a QCA majority Gate. The input and output wave forms of the majority Gate is shown in Figure 3(b). Moreover, the circuit diagram of the majority gate is shown in Figure 3(c).

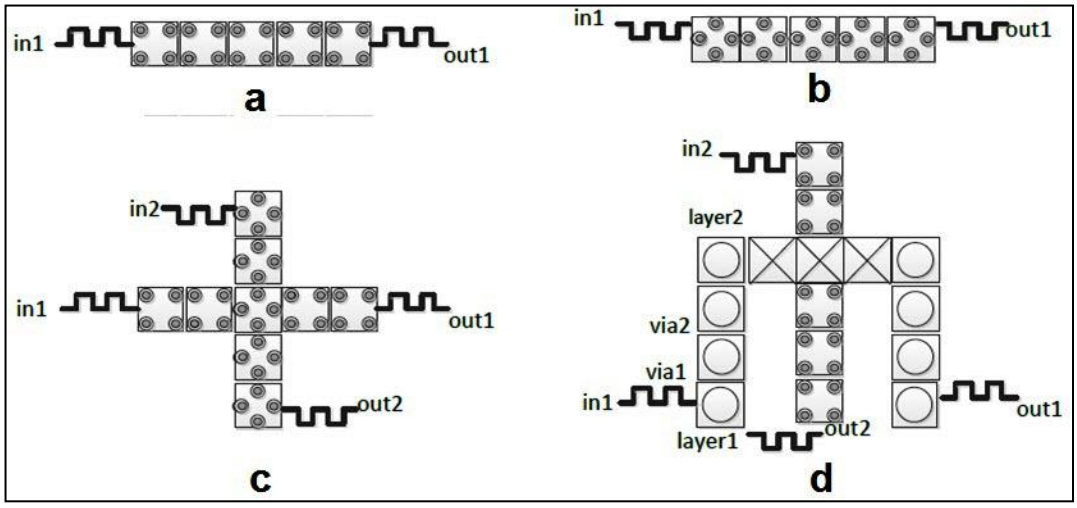

Figure 2. (a) QCA binary wire, (b) QCA inverter chain wire,(c) QCA coplanar crossing, (d) QCA multi-layer crossing.

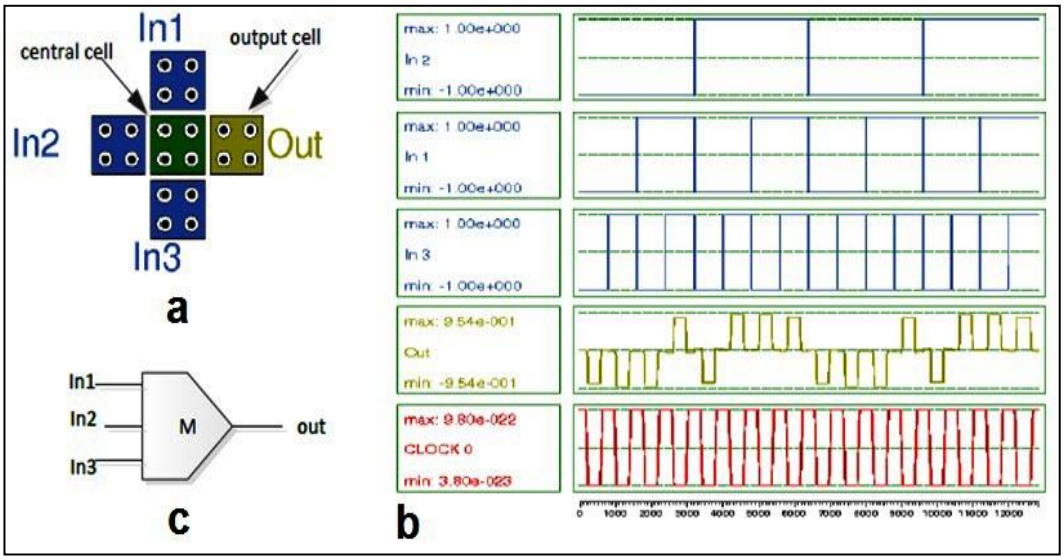

Figure 3. (a) The QCA layout of Majority Gate (b) The Input and Output wave forms of Majority Gate (c) The Circuit diagram of Majority Gate.

The equivalent output of the Majority Gate is given by the following equation:

$$F = M(A,B,C) = A.B + A.C + B.C \tag{1}$$

If we set one of the three inputs of the Majority Gate logical "0" or logical "1", the AND and OR Gates can be implemented in OCA. The QCA Layout of AND and OR Gates, and also their circuit diagram are shown in Figure 4.

AND Gate can be derived by the following equation:

$$F = M(A,B,0) = A.B + A.0 + B.0 = A.B \tag{2}$$

OR Gate can be derived by the following equation:

$$F = M(A,B,1) = A.B + A.1 + B.1 = A + B \tag{3}$$

According to the Coulomb Law, if two QCA cells are diagonally together, they can make an Invert Gate. QCA inverter Gate can be implemented in various schemes. Different types of QCA Invert Gates are shown in Figure 5.

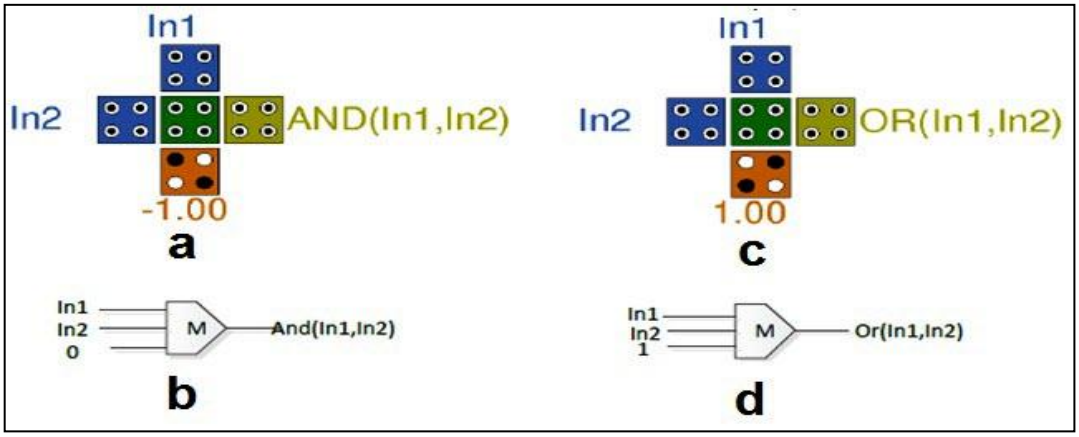

Figure 4. (a) The Layout Outward of AND Gate in QCA,(b) The Circuit Schematic of And Gate, (c) The Layout Outward of OR Gate in QCA,(d) The Circuit Schematic of OR Gate.

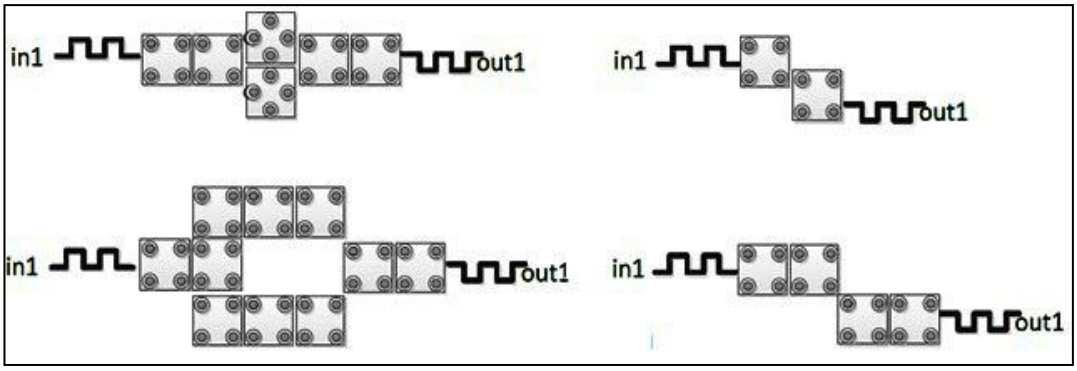

Figure 5. QCA inverter Gates.

In QCA, the clock signal is used to control and synchronize all sections of the circuit. In QCA, there are four clock signals: Clock0, Clock1, Clock2 and Clock3, which have the phase difference of 90 degrees [6,7]. Each clock signal in QCADesigner software represented in the different colors. Each clock signal is composed of four phases: Switch, Hold, Release, and Relaxed. Four clock signals are shown in Figure 6(a). A QCA wire with its output wave form in QCADesigner software, which is implemented using four clock signals, is shown in Figure 6.

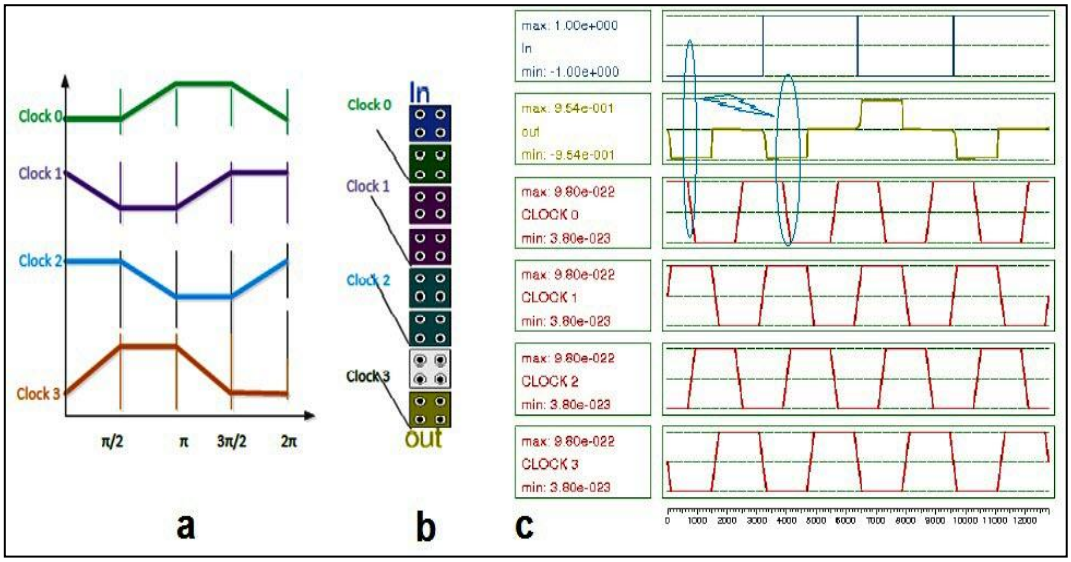

Figure 6. (a) An Outward of clock signal in QCA,(b) QCA wire in four clock,(c) An Outward of output and input waves forms in QCA wire.

2. Proposed QCA Full Adder Designs

Different designs of QCA Full adder have been presented in the last few years by the researchers. This article presents two novel QCA Full adder designs. The proposed QCA Full adder designs are implemented and simulated using QCADesigner.

2.1 The First Design

This Full adder is composed of five AND Gates, three OR Gates and three NOT gates with three inputs (a, b and c) and two outputs (Sum and Carry). We are used the following equations to implement the first QCA Full Adder design:

$$Sum = \bar{b}.(a+c).\overline{a.c} + b.\overline{(a+c)(\overline{a.c})} \tag{4}$$

$$Carry = a.c + b.(a+c)(\overline{a.c}) \tag{5}$$

The circuit diagram of the first Full adder and its QCA Layout are shown in Figure 7. This design are implemented with 292 cells. The input to output delay is 12 clock phases, and its approximate area is 0.416 μm^2.

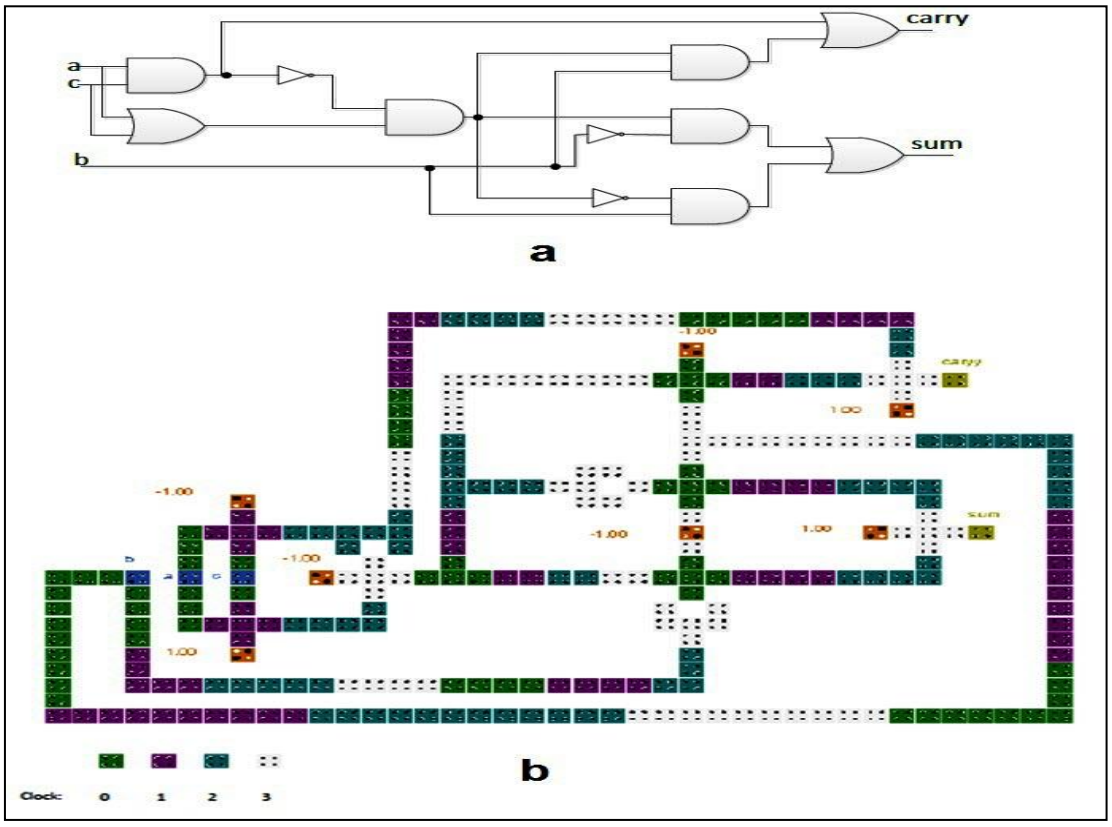

Figure 7. The first QCA Full Adder (a) circuit diagram (b) QCA Layout.

2.2. The Second Design

To design the second proposed QCA Full Adder, we are used the following equations, which realize a Full Adder with only the majority Gates, and inverters:

$$Sum = a.b.cin + a.\bar{b}.\overline{cin} + \bar{a}.b.\overline{cin} + \bar{a}.\bar{b}.cin = M(\overline{M}(a,b,cin), M(a,b,\overline{cin}), cin) \tag{6}$$

$$Carry = a.b + a.cin + b.cin = M(a,b,cin) \tag{7}$$

This Full adder is composed of three majority Gates, two inverter Gates with three inputs (a, b and c) and two outputs (Sum and Carry). The circuit diagram of the second proposed Full adder and its QCA Layout are shown in Figure 8. The main advantage of this design is the absence of any wire crossing in its QCA layout. This design is implemented with 45 cells. The input to output delay is 3 clock phases and its approximate area is 0.33 μm^2.

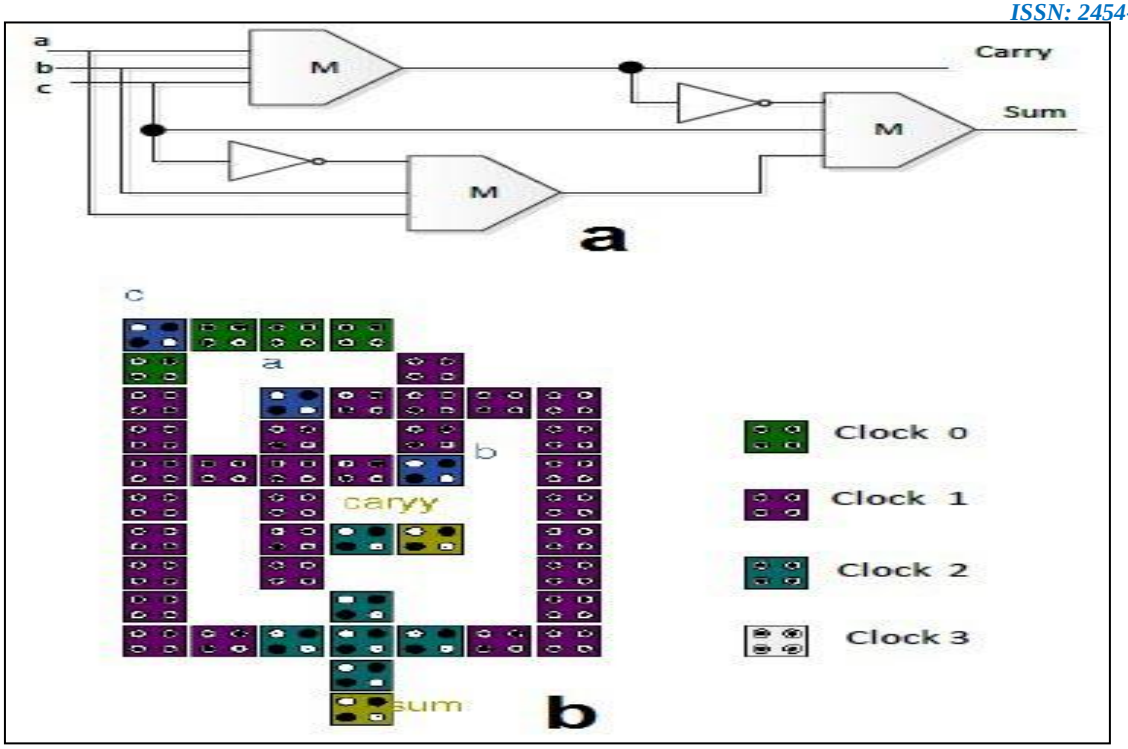

Figure 8. The second proposed QCA Full Adder(a) circuit diagram (b) QCA Layout.

3. Results and Discussion

The simulation results of the proposed Full adders are shown in Figure 9 and Figure 10. For this purpose, QCADesigner software is used. The following parameters are used in the Bitable approximation engine: Number of samples 20000, Convergence tolerance 0.001, Radius of effect 65nm, Relative permittivity 12.9, Clock high 9.8-22J, Clock low 3.8-23J, Clock amplitude factor 2, Layer separation 11.5nm, and Maximum iterations per sample 100. The comparison between the proposed QCA Full Adder designs and the previous works in terms of wire crossing types, cell numbers, areas and delay is shown in Table 1. Both suggested designs are implemented in QCA without any wire crossing, which is the main advantage of them.

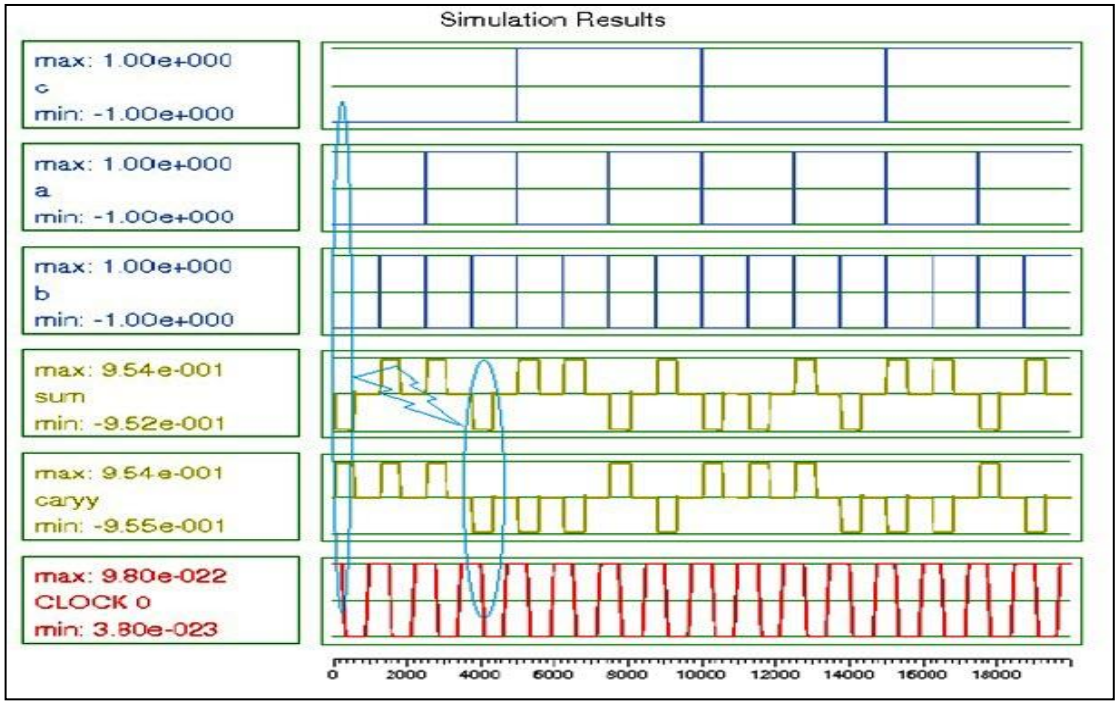

Figure 9. Simulation results of the first proposed QCA Full Adder.

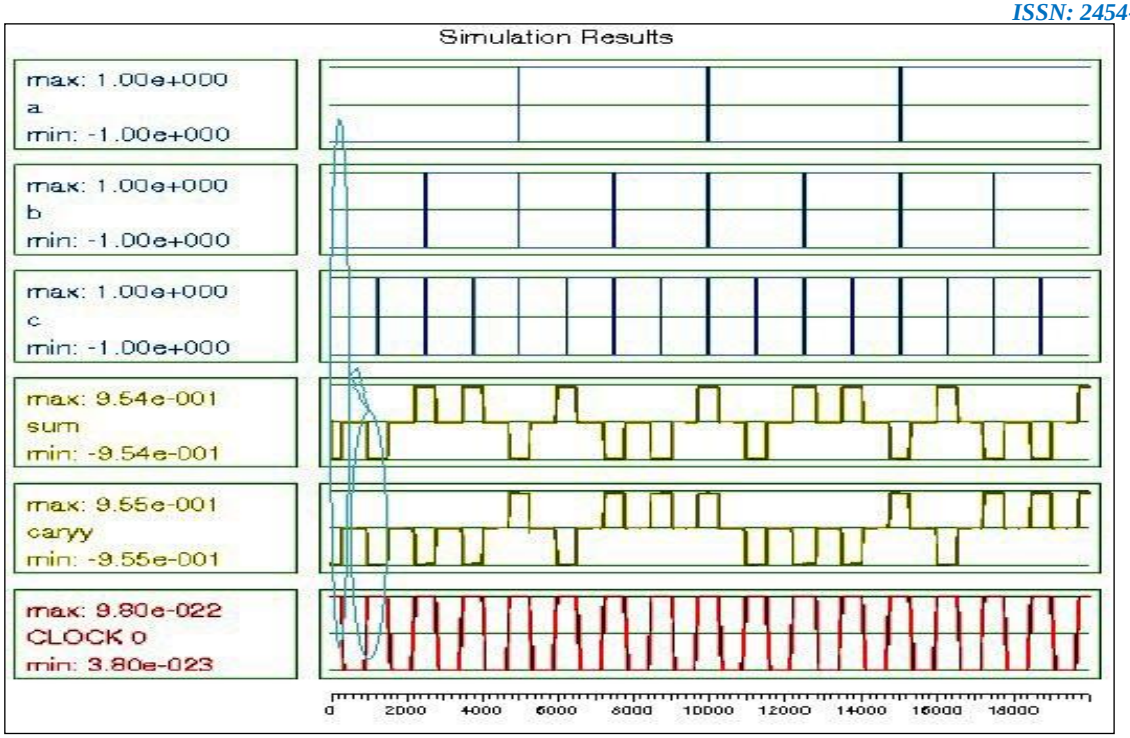

Figure 10. Simulation results of the second proposed QCA Full Adder.

Table 1. Comparison with the previous works.

Reference	Type of crossing	Cell count	Approximated area (μm^2)	Time delay (clock phase)
[8]	Multi-layer	23	0.01	3
[9]	Multi-layer	31	0.01	3
[10]	Multi-layer	31	0.02	3
[10]	Multi-layer	33	0.02	3
[11]	Multi-layer	52	0.04	3
[12]	Multi-layer	56	0.04	3
[13]	Multi-layer	73	0.04	3
[14]	Multi-layer	86	0.1	3
The first proposed design	Without wire crossing	292	0.416	12
The second proposed design	Without wire crossing	45	0.03	3

4. Conclusion

QCA is a new nanotechnology and in the near future the CMOS technology may be replaced with QCA. This paper proposed two designs to implement Full Adder in QCA. The proposed designs do not use any multi-layer crossing or coplanar crossing. The first design is implemented with 292 cell, 0.416 μm^2 area in 12 clock phases and second design is implemented with 45 cell, 0.03 μm^2 area in three clock phases delay. They have the simple structures and can be simply used in designing QCA circuits.

References

[1] Design of Analog CMOS Integrated Circuits, Behzad Razavi professor of Electrical Engineering University of California, Los Angeles, 2012.

[2] Compano R., Molenkamp L., and Paul D.J., Roadmap for Nanoelectronics, 2011.

[3] Sheikhfaal S., Angizi S., Sarmadi S., Moaiyeri M.H., Sayedsalehi S. Designing efficient QCA logical circuits with power dissipation analysis. Microelec. J. 2015; 46: 462-471.

[4] Teja V.C., Polisetti S. and Kasavajjala S. QCA based Multiplexing of 16 Arithmetic & Logical Subsystems-A paradigm for Nano Computing 2008. The 3rd IEEE Int. Conf. on Nano/Micro Engineered and Molecular Sys. 2008: 758-763.

[5] Amlani I., Orlov A.O., Toth G., Bernstein G.H., Lent C.S., Snider G.L. Digital logic gate using quantum-dot cellular automata, Science. 1999; 284: 289–291.

[6] Cho H. and Swartzlander E.E. Adder designs and analyses for quantum dot cellular automata. IEEE Trans. Nanotechnol. 2007; 6(3): 374–383.

[7] Hashemi S., Tehrani M., and Navi K. An efficient quantum-dot cellular automata full-adder. Scientific Research and Essays. 2012; 7: 177–189.

[8] Roohi A., Ronald F., Khoshavi N. Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder, Microelectronics J. 2015; 46(6): 531–542.

[9] Sen B., Rajoria A., Sikdar B.K. Design of Efficient full adder in quantum-dot cellular automata. The Scientific World Journal. 2013; 2013: 531–541.

[10] Sayedsalehi S., Moaiyeri M.H., Navi K. Novel efficient adder circuits for quantum-dot cellular automata. J. Comput. Theor. Nanosci 2011; 8 : 1769–1775.

[11] Roohi A., Khademolhosseini H., Sayedsalehi S., Navi K. A symmetric quantum-dot cellular automata design for 5-input majority gate, J. Comput. Electron. 2014; 13: 701–708.

[12] Navi K., Roohi A., Sayedsalehi S. Designing reconfigurable quantum-dot cellular automata logic circuits, J. Comput. Theor. Nanosci. 2013, 10: 1137–1146.

[13] Navi K., Farazkish R., Sayedsalehi S., Rahimi Azghadi M. A new quantum-dot cellular automata full-adder. Microelectron. J. 2010; 41(12): 820–826.

[14] Cho H., Swartzlander E. E. Adder and multiplier design in quantum dot cellular automata, IEEE Trans. Comput. 2009; 58: 721–727.