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Implementation of a Complete Gate for Quantum-Dot Cellular Automata

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Abstract

In the last few decades, scaling in feature size and increase in processing power have been achieved by conventional CMOS technology. Due to basic physical limitations, the conventional VLSI technology faces serious challenging problems in feature size reduction. Quantum dot cellular automata (QCA) has the potential to be one of the features promising nanotechnologies because of higher speed, smaller size and lower power consumption in comparison with transistor-based technology. In this paper, a complete Gate structure for implementation in QCA is presented. The inputs of the proposed structure are a, b and Cin (carry in) and the outputs are AND, OR, NAND, NOR, XOR, XNOR, NOT (Not a), Sum and Cout (carry out). The proposed layout is designed and simulated in the QCA Designer software. The results show that, our complete Gate structure is optimized in terms of cell count, area, and delay. Therefore, this structure can be used in designing of QCA based circuits.

Keywords: Quantum-Dot Cellular Automata; QCA Cell; QCA Designer; Complete Gate Structure.

1. Introduction

Quantum-dot Cellular Automata (QCA) [1, 2] relies on new physical phenomena, and innovative techniques that radically depart from a CMOS-based model. The fundamental unit of the QCA is the QCA cell, which created with four quantum dots and two electrons as shown in Figure 1(a) [3, 4]. Binary information is encoded in the two possible polarizations (P= +1 to represent logic ”1” and P=-1 to represent logic ”0”) [3, 4]. QCA devices can be constructed using different cell arrangements [1-6].

The two types of QCA wire (binary wire and inverter chain) are shown in Figure 1(b). Because of the electrostatic interactions between cells, the binary signal propagates from input to output in a QCA wire. The inverter gate is shown in Figure 1(c) which is usually formed by placing the cells with only their corners touching. The QCA majority gate is shown in Figure 1(d) which performs a function as:

$$f = M(a,b,c) = a.b + a.c + b.c \quad (1)$$

The schematics of the inverter and majority gate are shown in Figure 1 (e) and Figure 1(f) respectively.

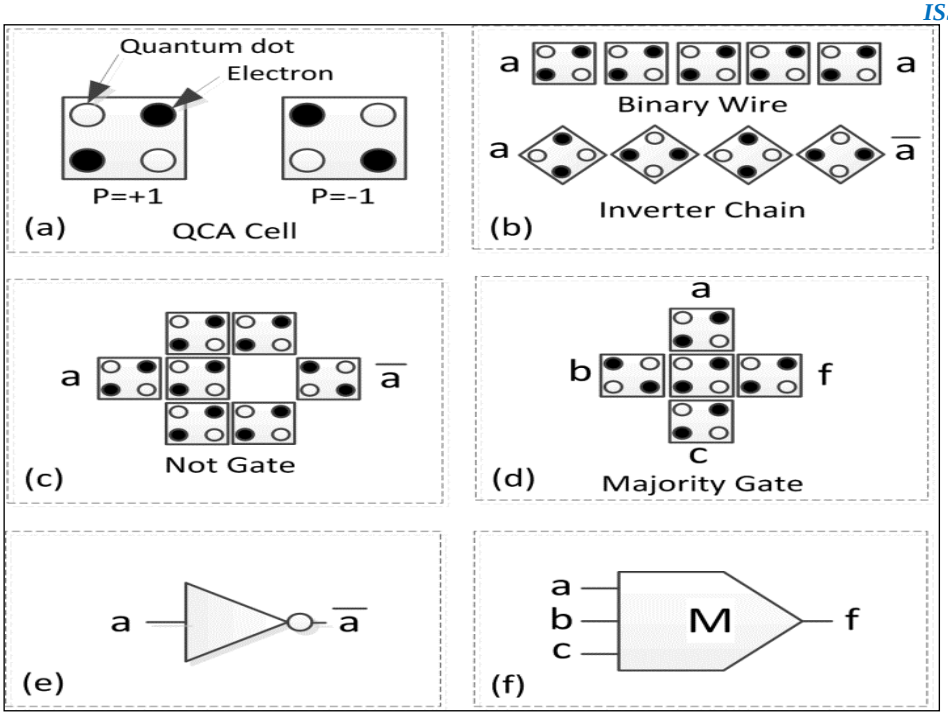

Figure 1: QCA basis components.

Using inverters and majority gates, any QCA circuit can be implemented. For example, the equations for a one-bit Full adder (FA) are given by [7-9]:

$$\begin{aligned} Sum &= a.b.Cin + a.\overline{b}.\overline{Cin} + \overline{a}.b.\overline{Cin} + \overline{a}.\overline{b}.Cin = M(\overline{M}(a,b,Cin), M(a,b,\overline{Cin}), Cin) \\ Cout &= a.b + a.Cin + b.Cin = M(a,b,Cin) \end{aligned} \quad (2)$$

Also, the equation for a XOR Gate is given by [10, 11]:

$$XOR = a.\overline{b} + \overline{a}.b. = M(M(\overline{a},b,-1), M(a,\overline{b},-1), 1) \quad (3)$$

The schematic diagram of the XOR Gate and one-bit FA are presented in Figure 2 (a) and Figure 2 (b) respectively. In this paper, we proposed optimized QCA complete Gate structure, which require minimum area and number of cells. In addition, it works with only six clock phases.

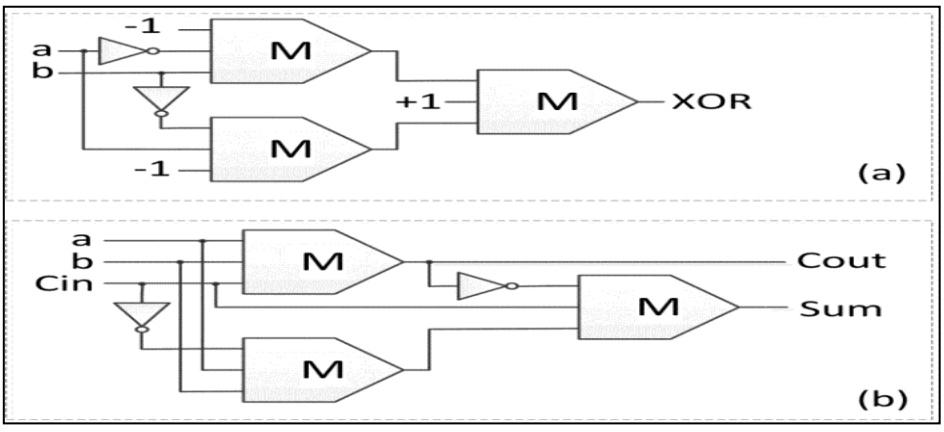

Figure 2: Schematics of (a) XOR Gate (b) one bit Full adder.

2. Complete Gate Structure Design

The layout of the proposed complete Gate structure is shown in Figure 3. The inputs of the proposed structure are a, b and Cin (carry in) and the outputs functions are AND (a,b), OR (a,b), NAND (a,b), NOR (a,b), XOR (a,b), XNOR (a,b), NOT (a), BUFFER(a) and one-bit Full adder (a+b+Cin). Figure 4 shows the implementation details of the proposed layout in QCA Designer software (http://www.mina.ubc.ca/qcadesigner). As shown in Figure 4, the proposed layout is designed in two layers. The input to output delay for all gates and functions is six clock phases.

The specifications of the proposed complete Gate structure are as follow: Number of QCA cells 234, Approximated Area 0.275 μm^2, Approximated wasted area in cells 438, Two-layer wire crossing, Number of wire crossing 4 and Delay (number of clock phases) 6.

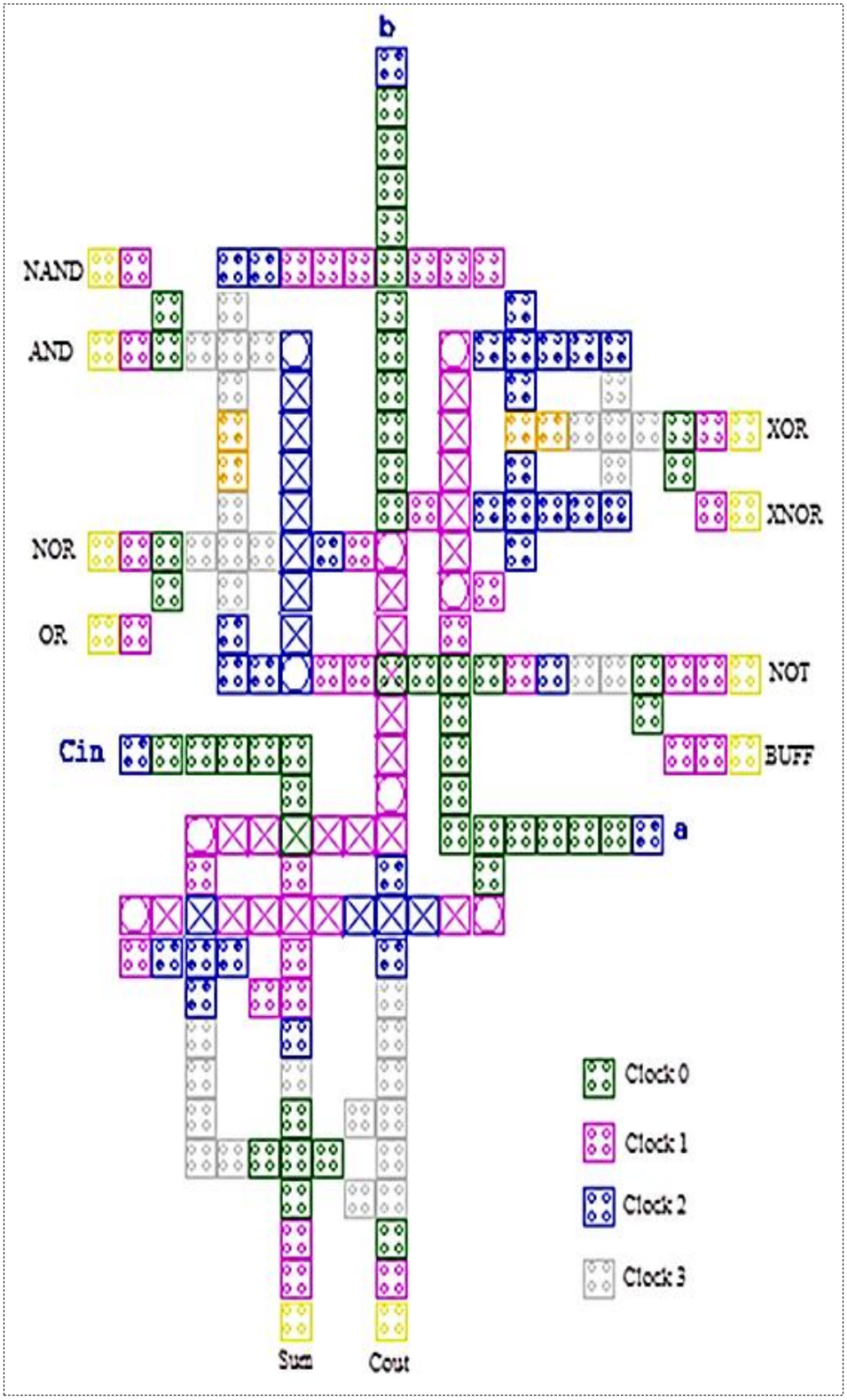

Figure 3: Layout of the proposed complete Gate implementation.

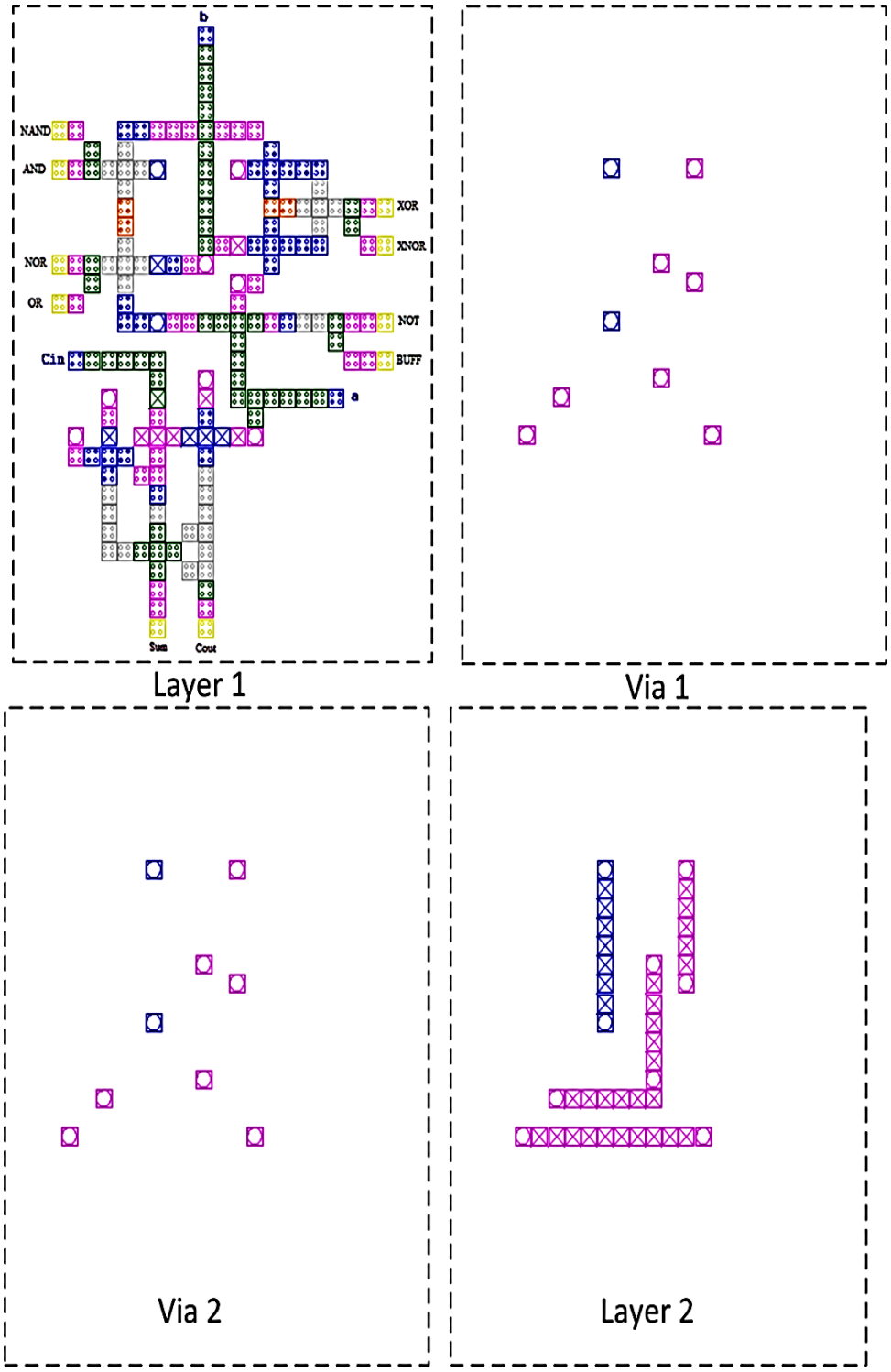

Figure 4: Implementation details of the proposed layout in QCA Designer.

3. Results and Discussion

QCA Designer software version 2.0.3 (http://www.mina.ubc.ca/qcadesigner) is used for simulation of the proposed design. The following parameters in bitable approximation are used: cell size 18nm×18nm, quantum dots diameter 5nm, number of samples 50000, convergence tolerance 0.0001, radius of effect 65nm, relative permittivity 12.9, clock high 9.8e-22J, clock low 3.8e-23J, clock amplitude factor 2, layer separation 11.5nm, maximum iterations per sample 1000 and randomize simulation order. The input and output waveforms for the proposed design is shown in

Figure 5. From Figure 5, it is clear that, our complete Gate structure is working properly and the delay between the inputs and the outputs is six clock phases. Therefore, we can use this structure for designing of QCA based circuits.

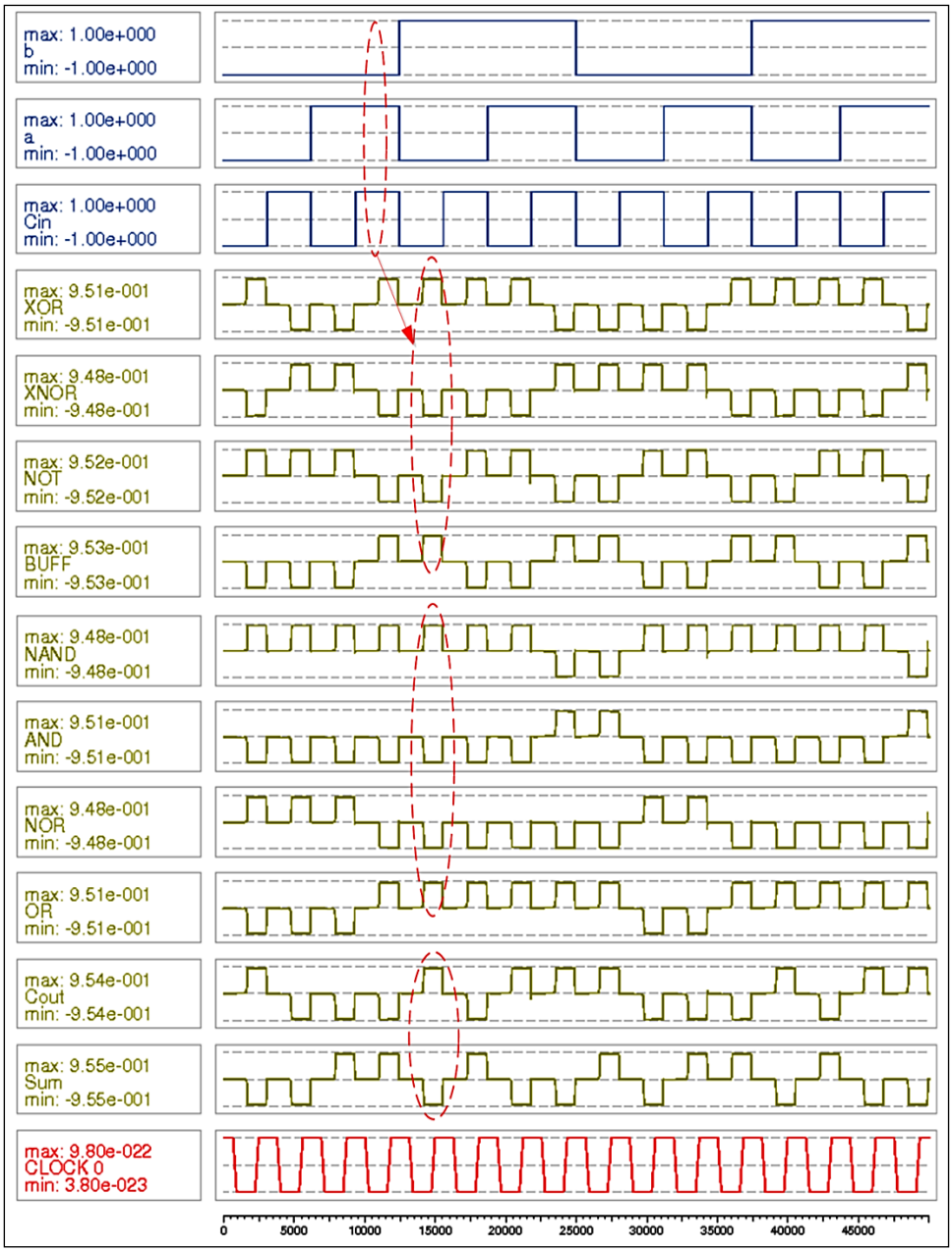

Figure 5: Simulation result.

4. Conclusion

In this paper, a complete Gate structure for implementation in QCA is presented. This structure implements AND, OR, NAND, NOR, XOR, XNOR, NOT and one-bit Full adder. QCA Designer software is used for simulation of the proposed layout. The results showed that, our complete Gate structure work satisfactory and it is optimized in terms of cell count, area, and delay.

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