


# Simple method for monitoring the switching activity in memristive cross-point arrays with line resistance effects

E. Miranda[a,*], A. Morell[b], J. Muñoz-Gorriz[a], J. Suñé[a]

[a] *Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Cerdanyola del Valles, Spain*

[b] *Departament de Telecomunicació i Enginyeria de Sistemas, Universitat Autònoma de Barcelona, 08193 Cerdanyola del Valles, Spain*

**Abstract**

A simple method for monitoring the switching activity (forming, set, reset events and stuck-at-0/1 faults) in memristive cross-point arrays with line resistance effects is proposed. The method consists in correlating incremental current changes in a four-terminal configuration with the location of the switching cell within the array. To this end the potential drop in the interconnection wires as well as the nonlinearity of the switching elements are considered. The problem is solved by iterating the Kirchhoff's current law for the coupled word and bit lines with appropriate boundary conditions. The main experimental advantage of the proposed method is that only four SMUs (source-measurement unit) are needed to identify the switching cell. In this way, our method could greatly contribute to foster the system-level reliability analysis of cross-point arrays since additional circuitry for the individual addressing of the switching device is not required.

## 1. Introduction

Memristive cross-point arrays (CPA) are nowadays intensively investigated by academia and industry because of their relevance in the fields of information storage and artificial intelligence [1]. CPAs are often associated with the matrix-vector multiplication operation which is a key operation in many computationally intensive algorithms [2,3]. In memory devices, the direct interconnection of devices (selectorless CPA) leads to the so-called sneak-path problem [4]. A CPA basically consists in the combination of two networks of vertical (N bit lines) and horizontal (M word lines) wires with a passive nonvolatile memory device or memristor at each intersection (see Fig. 1). Both for memory and neuromorphic applications, the conductance of each memristive device is set to a specific value representing a memory state or a synaptic weight, respectively. In addition, as the fabrication technology improves and the device dimensions shrink, the line resistance in CPAs is becoming a serious issue [5,6]. CPAs are not exempt from suffering faults related to the switching capability both associated with the fabrication process and with the lifetime of the devices [7-10]. This work explores the possibility of investigating reliability aspects of CPAs from a system-level approach. The idea is to rework the 2D current-ratio (CR) technique used to localize the occurrence of successive breakdown events in MOS transistors for the CPA case [11]. The method consists in biasing the structure appropriately and correlating incremental current changes in the terminals with the location of the switching event. This requires determining the voltage distribution at each node of the CPA considering the interconnection resistances. Recall that this voltage distribution modifies as the switching cells change their states. This is a complex nonlinear problem that is often solved using circuit simulators [12]. As the switching device, we will use in this work the memdiode (diode with memory) which allows to simulate a continuum of states by simply changing a parameter in the model [13].

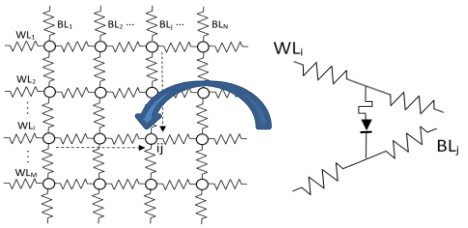


Figure 1. a) Typical MxN CPA with line resistance. b) Detail of the intersection between word and bit lines. The symbol corresponds to the memdiode.

* Corresponding author. enrique.miranda@uab.cat

## 2. Method description and equations

The method proposed to identify the locations ($1 \le i \le M, 1 \le j \le N$) of the switching cells is based on detecting current changes in a four-terminal configuration. The CPA is connected as depicted in Fig. 2a. $V_N$, $V_S$, $V_E$, $V_W$ and $I_N$, $I_S$, $I_E$, $I_W$ correspond to the North, South, East and West voltage and current terminals, respectively. The arrows indicate the positive convention for the currents. Figure 2b illustrates the connections at a particular intersection. Notice that the switching element between word and bit lines is represented by a memdiode.

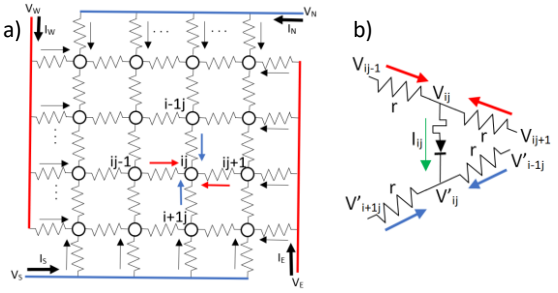


Figure 2. a) Four-terminal connection considered in this work and current convention. b) Detail of the intersection between the top and bottom wire networks.

It is easy to demonstrate that, according to Kirchhoff's current law, $V_{ij}$ and $V'_{ij}$, the voltages at the top and bottom networks, respectively, can be expressed as:

$$V_{ij} = \frac{1}{2}\left[V_{ij-1} + V_{ij+1} - rI_{ij}\right] \quad (1)$$

$$V'_{ij} = \frac{1}{2}\left[V'_{i-1j} + V'_{i+1j} + rI_{ij}\right] \quad (2)$$

where $I_{ij} = I\left(V_{ij} - V'_{ij}\right)$ is the current that flows through the memdiode $ij$ and $r$ he resistance of each section of the wire. Notice that (1) and (2) define a system of coupled nonlinear equations that can be solved by iteration.

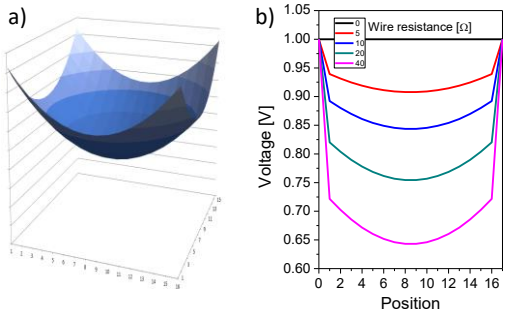


Figure 3. a) Voltage distribution at the CPA nodes ($V_W$=$V_E$=1V and $V_N$=$V_S$=0V). b) Voltage distribution as a function of the position along the 16x16 network and wire resistance $r$.

The boundary conditions at the four terminals in Fig. 2a will depend on the kind of test we want to carry out. We can leave the terminals opened or closed. For instance, in a constant voltage stress experiment, we bias the top and bottom wire networks with voltages $V_W$=$V_E$=1V and $V_N$=$V_S$=0V. Of course, these values will depend on the particular characteristics of the array but should be in a range compatible with the switching process of interest (forming, set, reset, stuck-at faults, etc.). Figure 3 shows the voltage distribution $V_{ij}$-$V'_{ij}$ in a 16x16 CPA when all the devices are in the high resistance state (HRS). Notice the surface curvature associated with the voltage drops caused by the wire resistances. It is clear that not all the devices *see* the same voltage drop. For example, this could strongly affect the set time of the devices which is expressed as [14]:

$$\tau_S = \tau_0 exp\left(-\frac{\left|V_{ij} - V'_{ij}\right|}{V_0}\right) \quad (3)$$

where $\tau_0$ and $V_0$ are constants. As observed in Fig. 3, the largest voltage drops occur at the corners of the array, and therefore those devices are expected to switch first. If we want to correct this nonuniform voltage distribution, resistance compensations at the terminal wires are an option [15]. Importantly, in what follows, the temporal aspect of the switchings is not considered. From here on the attention is exclusively focused on determining the position of the switching event within the array.

Similarly to the 2D CR method used to localize the failure sites in the gate oxide of a MOS transistor [11], we can locate the switching device using:

$$i = int\left(\frac{M\Delta I_E}{\Delta I_W + \Delta I_E}\right) + 1 \quad (4)$$

$$j = int\left(\frac{N\Delta I_S}{\Delta I_N + \Delta I_S}\right) + 1 \quad (5)$$

where $\Delta I_N$, $\Delta I_W$, $\Delta I_S$, and $\Delta I_E$ refer to the incremental current changes at the four terminals. *int* is the integer part of the number. The basic idea is that each switching event generates a perturbation in the CPA voltage/resistance distribution which is detected in the terminal currents. The magnitude of the current changes is related to the distance of the switching cell to each of the opposite terminals.

## 3. Memdiode model

In this work, the switching elements at the intersections of the lines are modelled as memdiodes.

A memdiode is a behavioral memory device represented by a diode with hysteretic properties [13,16]. For the sake of completeness, it is succinctly reviewed here. Physically, the memdiode expresses the presence of a potential barrier (Schottky, tunneling, quantum constriction, etc.) that controls the electron flow. This barrier remains stable (even if the power is turn off) until it is modified by a set or reset process. The memdiode model follows a typical memristive scheme, *i.e.* its conduction properties are described by two equations, one equation for the electron transport (*I-V*) and a second equation for the memory state of the device ($\lambda$-*V*) which changes according to the input signal. Since we will not deal here with hysteretic properties and switching transients, a discussion about the memory operator is irrelevant for the present analysis. The equation for the *I-V* characteristic of a memdiode is expressed as:

$$I(V) = sgn(V)\cdot\{(\alpha R)^{-1} W\{\alpha R I_0(\lambda) exp[\alpha(|V| + \\ +RI_0(\lambda))]\} - I_0(\lambda)\} \qquad (6)$$

where $I_0(\lambda) = I_{min}(1-\lambda) + I_{max}\lambda$ is the diode current amplitude, $\alpha$ a positive constant related to the particular features of the conduction mechanism, $R$ a series resistance, and $W$ the Lambert function. (1) is the solution of two antiparallel diodes with a single series resistance. The inverse currents of the diodes are neglected. $I_{min}$ and $I_{max}$ are the minimum and maximum values of the current amplitude, respectively. $|V|$ is the absolute value of the applied bias and *sgn* the sign function. As shown in Fig. 4, as $I_0$ increases in (6), the *I-V* curve changes its shape from linear-exponential to linear, as experimentally observed in many memristive devices. $\lambda$ is a control parameter that runs between 0 (HRS) and 1 (LRS). The model allows testing intermediate conduction states as well. Here, we will focus on the extreme situations $\lambda$=0 and $\lambda$=1. Notice that, in our approach, there is no need to consider separate expressions for the HRS and LRS *I-V* curves as in previous works [17,18]. Expression (6) is used in (1) and (2).

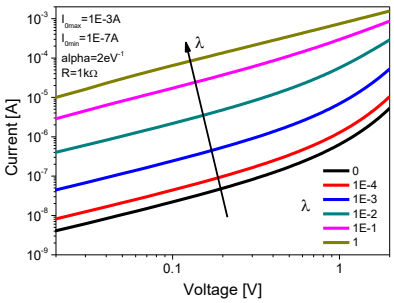


Figure 4. I-V curves for a memdiode. The parameter λ changes the current magnitude from HRS (λ=0) to LRS (λ=1) in a continuous way.

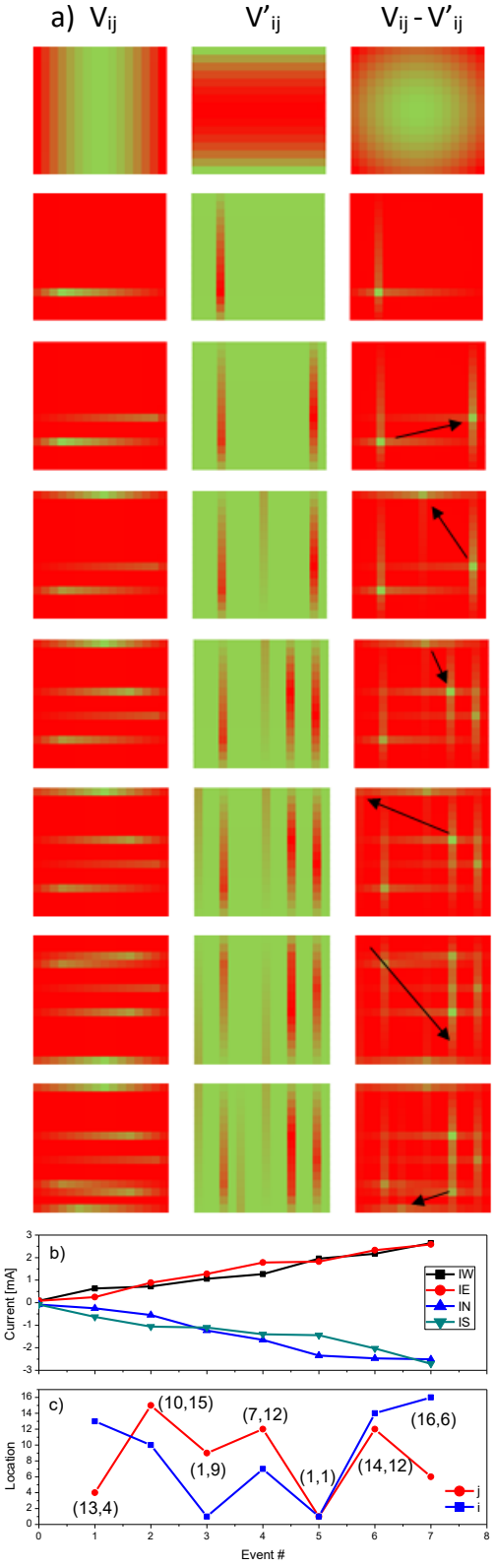


Figure 5. Switching events in a 16x16 CPA. a) Voltage distribution in the top/bottom layers and difference. b) Evolution of the terminal currents. c) Location of successive events. Follow the arrows in a). $r$=5Ω, $V_W$=$V_E$=1V and $V_N$=$V_S$=0V.

## 3. Results and discussion

Once the location procedure for the switching cell and the conduction model for the memristive structure are established, eqns. (1) and (2) can be solved numerically. Let's consider first a 16x16 CPA. Figure 5a shows the hypothetical evolution of the array caused by the application of constant voltages ($V_W$=$V_E$=1V and $V_N$=$V_S$=0V) to the terminals. The top row in Fig. 5a corresponds to all devices in HRS. The second row shows a first OFF/ON switching event. The intersection of the horizontal and vertical lines clearly points out the location of the switching cell. Figure 5b shows the evolution of the four terminal currents. The incremental data are used to compute the locations (see Fig. 5c) of the events *via* eqns. (4) and (5).

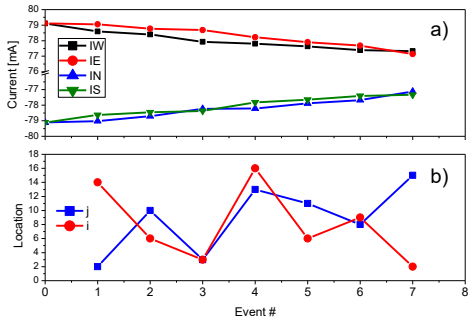


Figure 6. a) Evolution of the terminal currents. b) Location of consecutive switching events.

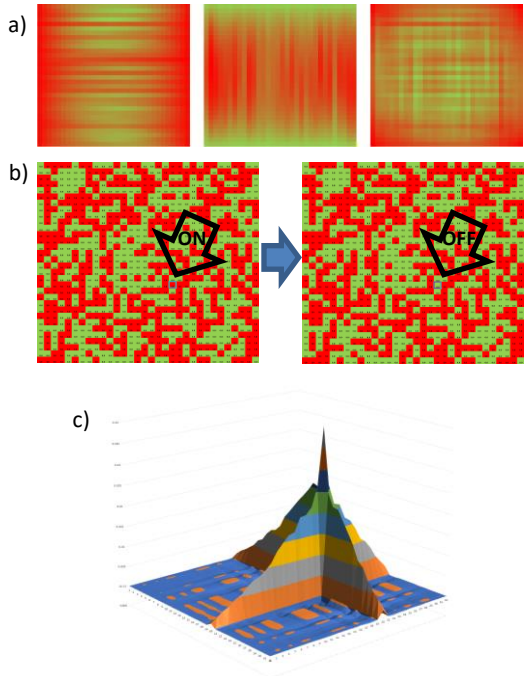


Figure 7. a) Top layer, bottom layer and voltage difference. b) Identification of the switching cell in a 32x32 CPA (i=20,j=20). c) Change in the voltage distribution (before and after) around the switching cell.

Figure 6 illustrates the case in which all memristors in the 16x16 CPA are initially in LRS. As the cells switch off (see Fig. 6a), the terminal currents decrease. Again, this information is used to detect the location of the successive switching events.

It is worth emphasizing that since the method is based on the incremental modification of the currents, the initial state configuration can be as complex as required. In this regard, Fig. 7 shows the case of a 32x32 CPA with a random distribution of LRS and HRS cells. The method is able to detect that the memdiode ($i$=20,$j$=20) switched off. For larger arrays the ability of the method to detect a switching event strongly depends on the current window (difference between LRS and HRS) and on the computation errors involved. Of course, in practice the method will be ultimately limited by the resolution of the experimental setup, the noise in the system, the variability of the switching process, etc. These issues require an in-depth analysis.

## 4. Conclusions

A simple method for determining the location of a switching cell within a cross-point array was presented. The method is based on monitoring the evolution of the currents in a four terminal configuration. The proposed approach is general in the sense that it does not make any specific reference to the physics of the conduction mechanism associated with the memristive device. Although a similar approach has been successfully applied to the case of failure events in MOS transistors, experimental validation in CPAs is still pending.

## References


[1] C. Sung, H. Hwang, I. Yoo, Perspective: A review on memristive hardware for neuromorphic computation. J. Appl. Phys. 124 (2018) 151903.

[2] P. Gu, B. Li, T. Tang, S. Yu, Y. Ca, Y. Wang, H. Yang, Technological exploration of RRAM crossbar array for matrix-vector multiplication. The 20th Asia and South Pacific Des. Aut. Conf. Japan, 2015.

[3] Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli, W. Wang, D. Ielmini. Solving matrix equations in one step with cross-point resistive arrays. PNAS 5 (2019) 4123.

[4] R. Naous, M. Zidan, A. Salem, K. Salama. Channel equalization techniques for non-volatile memristor memories. Conf. on Inf. Sc. and Syst., 2016.

[5] B. Liu, H. Chen, X. Li, T. Huang, Q. Wu, M. Barnell. Reduction and IR-drop compensations techniques for reliable neuromorphic computing systems. IEEE 2014.

[6] A. Chen. A comprehensive crossbar array model with solutions for line resistance and nonlinear device characteristics. IEEE Trans. Electron Dev. 60 (2013)

1318.
[7] M. Escudero-Lopez, F. Moll, A. Rubio, I. Vourkas. An on-line test strategy and analysis for a 1T1R crossbar memory. IEEE 23rd Int. Symp. On on-line testing and robust System Design, Greece, 2017.
[8] C. Dias, L. Guerra, J. Ventura, P. Aguiar. Memristor-based Willshaw network: Capacity and robustness to noise in the presence of defects. Appl. Phys. Lett. 106 (2015) 223505.
[9] C. Chen, H. Shih, C. Wu, C. Lin, P. Chiu, S. Sheu, F. Chen. RRAM defect modeling and failure analysis based on march test and a novel squeeze-search scheme. IEEE Trans. Comput. 64 (2015) 180.
[10] P. Pouyan, E. Amat, A. Rubio. Memristive crossbar memory lifetime evaluation and reconfiguration strategies. IEEE Trans. Emerg. Top. Comp. 6 (2018) 207.
[11] M. Alam, D. Varghese, B. Kaczer. Theory of breakdown position determination by voltage- and current-ratio methods. IEEE Trans. Elect. Dev. 55 (2008) 3150.
[12] S. Kim, H. Kim, S. Choi. Numerical study of read scheme in one-selector one-resistor crossbar array. Solid St. Electron. 114 (2015) 80.
[13] E. Miranda. Compact model for the major and minor hysteretic I-V loops in nonlinear memristive devices. IEEE Trans. Nanotech. 14 (2015) 787.
[14] A. Rodriguez-Fernandez, C. Cagli, J. Suñé, E. Miranda. Switching voltage and time statistics of filamentary conductive paths in $HfO_2$-based ReRAM devices. IEEE Electron Dev. Lett. 39 (2018) 656.
[15] S. Agarwal, R. Schiek, M. Marinella. Compensating for parasitic voltage drops in resistive memory arrays. IEEE Int. Memory Workshop, 2017.
[16] G. Patterson, J. Suñé, E. Miranda. Voltage-driven hysteresis model for resistive switching: SPICE modeling and circuit applications. IEEE Trans. Comp. Aided Des. Int. Circ. Sys. 36 (2017) 2044.
[17] W. Choi, K. Moon, M. Kwak, C. Sung, J. Lee, J. Song, J. Park, S. Chekol, H. Hwang. Hardware implementation of neural network using pre-programmed resistive device for pattern recognition. Solid St. Electron. 153 (2019) 79.
[18] R. Han, P. Huang, Y. Zhao, X. Cui, X. Liu, J. Kang. Efficient evaluation model including interconnect resistance effect for large scale RRAM crossbar array matrix computing. Sci. China Inf. Sci 62 (2019) 022401.