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Innovative Digital dc-dc Architectures for High-Frequency High-Efficiency Applications

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Summary

The new generation of automotive controllers requires a space-constrained and high-efficiency step-down architecture. Hence, recently a potential alternative for the conventional step-down topologies is highly demanded. The new architecture should meet the high power density, high efficiency, wide operating ranges, high EMI capabilities, and low-cost requirements. This thesis, developed at the University of Padova and sponsored by Infineon Technologies, aims at investigating potential candidate topologies for automotive step-down conversion capable of eliminating or offsetting some of the common shortcomings of conventional solutions currently in use.

Many research effort is paid for the soft switching quasi-resonant topologies in order to miniaturize the passive components through the switching frequency increase. However, the variable switching frequency, increased components count, and narrow operating ranges prevent the wide adoption of the quasi-resonant topologies in the target application. The first objective of this project is to investigate the quasi-resonant buck converter topology in order to stand on the limitations and operating conditions boundaries of such topology. The digital efficiency optimization technique, which is developed in this work, extends the operating ranges in addition to reduce operating frequency variations.

On the other hand, the multilevel hybrid topologies are potentially able to meet the aforementioned requirements. By multiplying ripple frequency and fractioning voltage across the switching node the multilevel topologies have the direct advantage of reduced passive components. Moreover, multilevel topologies have many other attractive features include reduced MOSFET voltage rating, fast transient response, a Buck-like wide range voltage conversion ratio, and improved efficiency. These features candidate the multilevel topologies, in particular, the three-level flying-capacitor converter, as an innovative alter-

native for the conventional topologies for the target application.

Accordingly, the three-level flying-capacitor converter (3LFC) is investigated as a second objective for this project. Flying-capacitor (FC) voltage balancing in such topology is quite challenging. The 3LFC under valley current mode control shows an interesting performance, where the FC voltage is self-balanced. In this work, the stability of the converter under valley and peak current mode control is studied and a simplified stability criterion is proposed. The proposed criterion address both current loop static stability and FC voltage stability. The valley current mode modulator results to be inherently stable as soon as the current static instability is compensated with an external ramp. On contrary, the FC voltage in peak current mode control (P-CMC) will never be balanced unless the converter operated with relatively high static peak-to-peak inductor current ripple. Since P-CMC has an inherent over-current protection feature, P-CMC based architectures are widely used in the industrial applications. However, in practice the peak current controlled three-level converter is inherently unstable. Consequently, the instability of the P-CMC 3LFC is addressed. A sensorless stabilizing approach, with two implementation methodologies, is developed in this work. The proposed technique eliminates the instability associated with the FC voltage runaway, in addition to FC voltage self-balancing. Moreover, the proposed methodology offers reduced size, less complexity, and input voltage independent operation. Besides, the proposed approach can be extended to system with a higher number of voltage levels with minimal hardware complexity.

The proposed techniques and methodologies in this work are validated using simulation models and experimentally. Finally, in the conclusions the results of the Ph.D. activity are summarized and recommendations for the further development are outlined.

Acknowledgments

"O mankind, indeed We have created you from male and female and made you peoples and tribes that you may know one another. Indeed, the most noble of you in the sight of Allah is the most righteous of you. Indeed, Allah is Knowing and Acquainted."

Holy Quran, Chapter(49), verse(13)

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Contents

Chapter 1

Introduction

1.1 Background and motivation

High power density, high efficiency, fast transient response, and less complexed control architecture are key features in the automotive application. Accordingly, many researchers aim to explore potential alternatives to the conventional step-down topologies [2–4]. Conventional converters have filter inductor 5-10 times larger than the active and control components [5]. Moreover, large inductor size leads to a slow transient response [6, 7]. Consequently, many researchers recently embrace the inductor size reduction as a key solution to develop a cost-effective and high-efficiency power supply on a chip (PSoC) and power supply in a package (PSiP) [8].

On one hand, increasing the switching frequency has the direct advantage of inductor size reduction and improved transient response [5, 9]. On the other hand, the operating frequency increase is coupled with a dramatic increase in the switching losses. That defect prevents using such solution with the conventional topologies. The proposed methods for load transient improvement and converter size reduction are divided into control-based and topology-based solutions [6].

The topology based solutions achieve the size reduction by achieving one or more features which are listed below:

1. increase the inductor current ripple frequency (switching node frequency),

2. decrease voltage swing across the switching node,

3. enable high frequency operation by decreasing the switching losses.

The soft-switching topologies like quasi-resonant converters topologies reduce the switching losses in order to enable the converter to operate at higher frequencies. Soft-switching topologies usually need extra passive elements to generate the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) [9]. On the other hand, the multilevel and hybrid topologies achieve significant reduction in the inductor size using additional active and capacitive passive components. In the multi-level topologies, the voltage swing across the switching node and the voltage stress across the devices are reduced by $(N-1)$, where N is the number of levels. The effective switching frequency is increased by $(N-1)$ across the switching node [10]. Recently, the 3-level flying capacitor (3L-FC) topology is proposed as a potential alternative for the conventional topologies for integrated solutions [5, 6, 10–14].

1.2 Objectives and Contribution

This PhD program aims at exploring potential alternatives to the conventional step-down topologies. The end goal is to identify conversion architectures which are able to overcome the challenges of high efficiency, space constraints, and fast transient response of the new generation of automotive controllers.

The Ph.D. program contribution proceeds along the following lines:

1. Development of the operating constraints of the quasi-resonant Buck converter by studying the converter steady-state behavior in case of using constant off-time variable frequency controller,

2. Development of a deadbeat digital online efficiency optimization technique which predicts the minimal switching voltage operating point in one switching cycle, in addition to input voltage range extension and compressed operating frequency variations capabilities,

3. In-depth investigation of the 3LFC Buck converter stability under valley and peak current mode control,

4. Development of a stability criterion for the peak/valley current mode controlled 3L-FC converter. The methodology which describes the static instability in the current loop due to the subharmonic oscillation, in addition to full description of the flying-capacitor voltage stability and balancing features,

5. Development of a sensor-less digital stabilizing approach for peak current programmed controlled 3LFC converter based on two different mixed signal architectures.

1.3 Thesis overview

1.3.1 Introduction

Reduced switching losses is the key feature in the soft-switching converters, which enables such topologies to work on higher operating frequencies. The high operating frequency improves the converter dynamics and reduces the converter size. However, the soft-switching topologies usually need extra passive elements to generate the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) states [9]. The quasi-resonant buck converter is investigated as an integrated solution in this thesis as will be shown in chapter 2.

Reduced voltage swing across the switching node and increased ripple frequency are the most attractive properties of the multilevel topologies. In the neutral point clamped topology these features are achieved by adding an additional active element. On the other hand, with additional hybrid compination of capacitive passive and active components in the multi-level converters the same features are adopted [15]. On one hand, in the multi-level topologies the voltage swing across the switching node and the voltage stress across the devices are reduced by $(N-1)$. On the other hand, the effective switching frequency is increased by $(N-1)$ across the switching node where N is the number of levels [10]. Recently, the three-level flying-capacitor topology is gained the researchers attention as a potential topology for the low-power low-voltage applications [5, 6, 10–14].

The work presented in this thesis investigates two high-frequency dc-dc step down topologies, *zero-voltage switching quasi-resonant Buck* and *three level flying capacitor Buck converters*, which are investigated in chapter 2 and chapter 3 respectively. An overview of the topologies under study and the related proposed control techniques is introduced in the next subsections.

1.3.2 Zero-voltage switching quasi-resonant Buck topology

A tank network is used in the quasi-resonant converter (QRC) in order to generate an oscillating voltage across the switching node. Hence, the upper MOSFET is turned on with zero-voltage switching (ZVS). Soft-switching mechanism theoretically eliminates the switching dynamics (zero dv/dt). Therefore, the switching losses at turn-on instant theoretically equals zero [2]. Moreover, the reverse recovery losses of the freewheeling diode is inherently eliminated with the asynchronous operation of the upper and lower switches.

However, in the conventionally controlled QRC one of the subintervals is imposed by the tank network resonance. Hence, using variable frequency control architecture is necessary [9]. An on-off control scheme with hysteretic override is proposed in [2] to present a constant operating frequency solution. However, that technique leads to a reduced dynamic response and higher output capacitance. Besides, the operation of the conventional QRC is load and circuit parameters dependent [9]. Consequently, the QRC has a drawback of narrow input voltage and load operating ranges. Accordingly, the converter efficiency optimization and extension of the operating ranges are interesting research points to be investigated. A deadbeat digital online efficiency optimization technique capable of extending the input voltage range and reducing the operating frequency variations is developed in this work [16]. The proposed controller is reported in chapter 2 with simulation and experimental assessment.

The main goal of the program targets a solution for an automotive application with a high degree of integration. Hence, the variable switching frequency, increased voltage stress on the upper switch, and increased magnetic elements are the vital drawbacks which motivated the author to investigate other alternatives.

1.3.3 Three-level flying-capacitor topology

The significant reduction in the output filter size and many other attractive features nominate the three-level flying-capacitor (3LFC) as a potential candidate for high-frequency high-efficiency integrated solutions.

Steady-state ideal operation in addition to the challenges faces the adoption of the 3LFC topology are discussed in chapter 3. Most of the attractive features of the 3LFC rely on that, FC voltage is balanced at $V_{fly} = \frac{V_g}{2}$. Two main challenges related to flying capacitor (FC) voltage are recognized in the literature, converter starting and FC voltage balancing.

FC has no charge at starting, hence the switches suffer from higher voltage stress during start-up. In [5] a start-up routine is proposed to charge the FC voltage at $\frac{V_g}{2}$ before starting the normal operation. However, in such solution the upper switch must block the full input voltage directly after power-up until the starting of charging circuitry. That problem is recently addressed in [17].

On the other hand, under the ideal conditions the FC voltage is self balanced during normal operation. However, in practice due to the circuit parasitics and asymmetrical delays, the FC voltage is unbalanced. Hence, using an active balancing methodology is essential. Otherwise, the topology loses most of its features [5, 7, 14, 18]. In the literature many FC voltage stabilizing techniques have been proposed. The techniques in [14] and [19] require FC voltage sensing in order to balance the corresponding voltage. An inherent self balancing feature associated with valley current mode control is proposed in [5] and [20]. The FC voltage balancing methodologies are reported in details in chapter 3.

1.3.4 Stability properties of the three-levels flying-capacitor Buck Converter Under valley or peak current-programmed-control

The CMC is attractive for dc-dc applications due to the fact that tightly controlled inductor current results in more robust and simpler wide-bandwidth control [21]. Moreover, the CMC naturally ensures system stability against input voltage variations, the performance which is highly required in the specifications of automotive applications. Theory of CMC for basic Buck, Boost and Buck-Boost converters is well covered by numerous papers and

textbooks, and many small-signal modeling techniques have been disclosed which rely on averaging techniques [22–25] as well as describing function methods [26]. On the other hand, the additional state variable due to the presence of the FC in the 3L-FC topology complicates the stability analysis of the topology under-study. Therefore, the stability properties of the 3LFC topology under valley and peak current mode control considering both current loop static stability and FC voltage stability is presented in chapter 4.

The current subharmonic oscillations boundaries are developed when the FC voltage is replaced with a constant voltage source. By considering a weak coupling between the FC voltage and inductor current, then the hypothesis of large FC has no effect on the validity of the proposed stability analysis. The aforementioned assumption is discussed in chapter 4. The minimal compensation ramp slope required to suppress the current static subharmonic oscillation is calculated. As for the FC voltage stability, the FC voltage in V-CMC converter is found inherently stable once the current static instability is compensated by a compensation ramp – a property which has been highlighted in the literature but never formally proven. On the other hand, P-CMC converter results to be inherently unstable, due to the FC voltage runaway phenomena, unless the converter is running with relatively large peak-to-peak current ripple. The minimal current ripple required in order to stabilize the P-CMC is calculated. The stability study, which is presented in chapter 4, is proposed in [27, 28].

1.3.5 Sensorless stabilizing approach of peak-current-programmed controlled three-levels flying-capacitor converter

The P-CMC is commonly used in dc-dc converters due to the inherent over current protection feature [29–34]. However, the P-CMC 3LFC is inherently unstable. Therefore, the author presents in chapter 5 two sensorless mixed-signal stabilizing architectures for P-CMC 3L-FC converter. The proposed approach measures the duty command difference $D_2 - D_1$ in order to detect the FC voltage unbalance. Accordingly, the proposed technique offers reduced size beside the input voltage independent operation.

Finally, chapter 6 draws the main conclusions summarizing the relevant results achieved

by the Ph.D. activity. Proposals for future works and subjects for further investigations are also outlined.

Chapter 2

Quasi-Resonant Buck Converter

2.1 Quasi-Resonant Buck Converter State of the Art

Generally, an inductor-capacitor based tank network is connected to modify a conventional topology to work in the quasi-resonant mode. Many configurations are addressed in the textbooks like in [22]. Quasi-resonant operation can bring a significant reduction in the switching losses with improved EMI capabilities [9, 22]. However, many challenges stand behind the wide adoption of the quasi resonant topologies especially in the automotive application. In particular the variable switching frequency operation and limiting the efficiency improvement to narrow input voltage and load operating ranges are more relevant to the target application. Here, one of the quasi-resonant zero-voltage-switching (ZVS) buck converter topology configurations, shown in Fig. 2-1(a), is investigated. The tank network consists of a resonant capacitor C_r, which is connected between the switching node and the ground, and a resonant inductor L_r which is connected between the switching node and the freewheeling diode (FWD) as shown in Fig. 2-1(a). Under the small ripple approximation, the output stage can be approximately replaced with a current source as shown in Fig. 2-1(b). In order to investigate the steady-state operation of the topology under study, ideal conditions are assumed which are listed below:

1. No MOSFET on resistance.

2. No diodes forward voltages.

3. Ideal inductances.

4. Ideal capacitances.

5. Small ripple approximation (SRA) on output inductor L_o.

In addition, some basic parameters related to the oscillating behavior of the tank network should be defined.

During the freewheeling period the tank network starts to oscillate with a natural angular frequency ω_r given by

$$\omega_r = \sqrt{\frac{1}{L_r C_r}}. \tag{2.1}$$

That oscillation may enable the power switch to be switched ON at zero voltage. The peak of the oscillating voltage is a function in the tank characteristic impedance Z_0, which is given by

$$Z_0 = \sqrt{\frac{L_r}{C_r}}, \tag{2.2}$$

and load current I_o. Operating the converter under the ZVS mechanism has an essential condition which is defined by

$$J \geq 1, \tag{2.3}$$

where J is the ratio between absolute resonant voltage peak and input voltage level which given by

$$J = \frac{I_o Z_0}{V_g}. \tag{2.4}$$

According to (2.3) and (2.4), one of the drawbacks of the topology under study is that the power switch must block a voltage V_{blk} during turn off given by

$$V_{blk} = V_g(1 + J), \tag{2.5}$$

which is at least twice the input voltage level V_g.

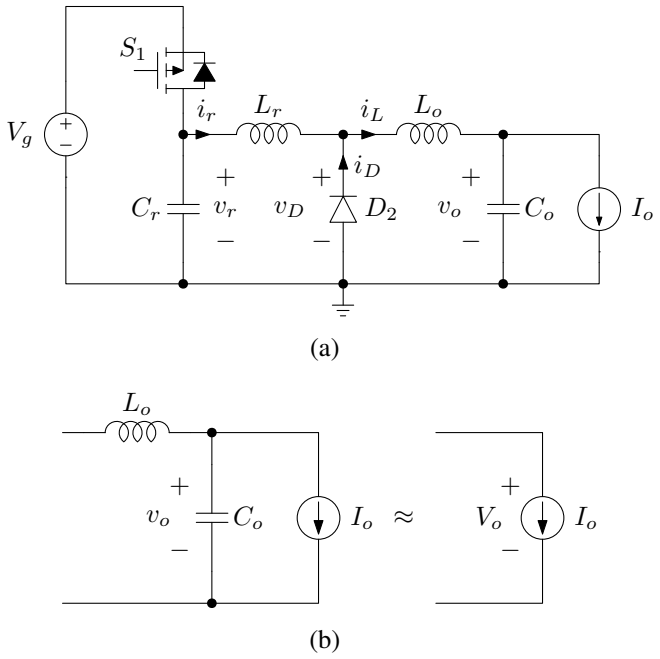


Figure 2-1: Quasi-resonant buck converter: (a) converter topology and (b) the output stage under small ripple approximation

2.1.1 Ideal Steady State Operation

The converter voltage conversion ratio μ is the ratio between the output voltage V_o and the input voltage V_s. The converter output voltage is always equal to the average of the voltage across the freewheeling diode $\langle v_D \rangle_{T_s}$. Therefore, deriving an expression for the voltage conversion ratio μ requires the freewheeling diode voltage to be averaged over one switching cycle.

A converter operated with ZVS has four topological states, as shown in the steady-state waveforms reported in Fig. 2-2, which are defined by four conduction angles α, β, γ, and δ. Each topological state is investigated to derive the conduction angles (α, β, γ, and δ) and freewheeling diode voltage expressions.

First topological state α

Here the power switch turn off instant is considered the beginning of the switching cycle. The converter enters the first topological state, defined by the sub-interval α and shown in Fig. 2-3(a), after the switch turns OFF. At turn off instant, the resonant capacitor C_r is

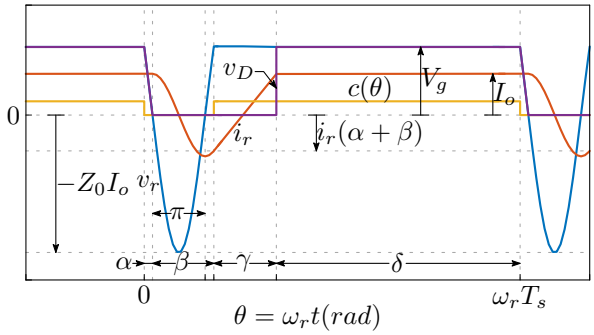
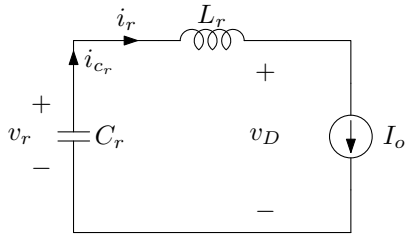
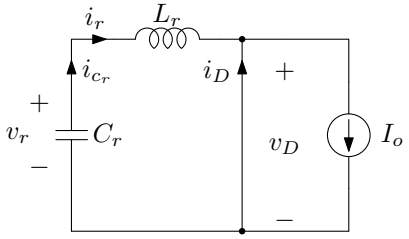


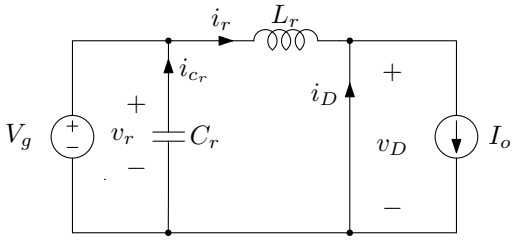
Figure 2-2: Quasi-resonant ZVS operated buck converter steady-state waveforms



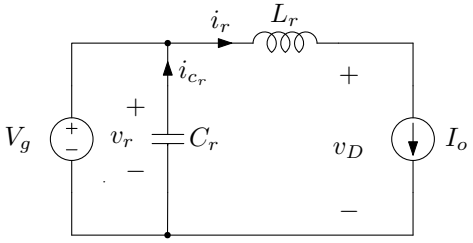
(a) First topological state α



(b) Second topological state β



(c) Third topological state γ



(d) Fourth topological state δ

Figure 2-3: ZVS operated QRC topological states under SRA assumption

initially charged with a voltage equal to V_g. Afterwards, the capacitor starts to discharge linearly. The subinterval α ends at the operating point where $V_r = 0$. Hence, the conduction angle α is given by

$$\alpha = \frac{V_g}{Z_0 I_o} = \frac{1}{J}. \tag{2.6}$$

FWD voltage (v_D) during conduction angle (α) is given by

$$v_{D_\alpha}(\theta) = V_g - I_o Z_0 \theta. \tag{2.7}$$

Second topological state β

At the beginning of the subinterval β the resonant tank starts to oscillate and the converter enters the second topological state shown in Fig. 2-3(b). By considering the ZVS operation, the subinterval β ends when the resonant voltage $v_r = V_s$. Then, the conduction angle β is given by

$$\beta = \pi + \arcsin\big(\frac{1}{J}\big). \tag{2.8}$$

The conduction angle β defined in (2.8) is valid under the condition of $J \geq 1$. The FWD voltage will given by

$$v_{D_\beta}(\theta) = 0, \tag{2.9}$$

during the conduction angle β.

Third topological state γ

The third topological state, shown in Fig. 2-3(c), starts by turning on the power switch. The resonant node will be connected to the input source voltage V_s and the resonant capacitor C_r acts as input filter. The resonant current i_r starts to increase linearly from an initial value $i_r(\alpha + \beta)$, which is given by

$$i_r(\alpha + \beta) = I_o \cos(\beta), \tag{2.10}$$

to the output current level I_o. At resonant current $i_r = I_o$ the subinterval γ, which is given by

$$\gamma = J\big(1 + \sqrt{1 - \frac{1}{J^2}}\big), \tag{2.11}$$

ends and the FWD is turned OFF. Consequently, the FWD voltage during sub-interval γ is given by

$$v_{D_\gamma}(\theta) = 0. \tag{2.12}$$

Fourth topological state δ

The fourth topological state, shown in Fig. 2-3(d), equals the switch ON time. Consequently, the conduction angle δ is simply expressed by

$$\delta = \frac{2\pi}{F} - \frac{1}{J} - \pi - \arcsin\left(\frac{1}{J}\right) - J\left(1 + \sqrt{1 - \frac{1}{J^2}}\right), \tag{2.13}$$

where the frequency ratio F is given by

$$F = \frac{f_s}{f_r}. \tag{2.14}$$

f_s and f_r are the switching and resonant frequencies respectively. The FWD is OFF during the sub-interval δ, accordingly, the FWD voltage (v_D) will be given by

$$v_{D_\delta}(\theta) = V_s. \tag{2.15}$$

Steady-state voltage conversion ratio μ

The average value of the output voltage can be deducted by calculating the average of the FWD voltage in one switching cycle [22]. Hence, the voltage transfer ratio of the ideal ZVS operated quasi-resonant buck converter μ is given by

$$\mu = 1 - \frac{F}{2\pi}\left[\frac{1}{2J} + \pi + \arcsin\left(\frac{1}{J}\right) + J\left(1 + \sqrt{1 - \frac{1}{J^2}}\right)\right]. \tag{2.16}$$

2.1.2 ZVS Mechanism and System Boundaries

As mentioned earlier the ZVS operation depends on the value of J. The converter resonant voltage v_r, resonant current i_r, and gate signal $c(\theta)$ steady-state waveforms are observed, at three different values of J ($J_1 > 1,\ J_2 = 1,\ and\ J_3 < 1$), in order to demonstrate the aforementioned dependency.

- $J = J_1 > 1$:

  Generally, the resonant voltage reaches the input voltage level when the conduction

angle $\theta = \alpha + \beta$, under the condition $J > 1$. As shown in Fig. 2-4(a), in such operating condition the switch is turned ON when the resonant current has a negative initial value defined in (2.10).

- $J = J_2 = 1$:

  However, as in the last case the voltage reaches the input voltage level at the same conduction angle, but the initial current at switch turning ON instant is zero. Hence, the converter with $J = 1$ is operated under zero-voltage and zero-current switching, as shown in Fig. 2-4(b). The operating point where $\beta = \frac{3\pi}{2}$.

- $J = J_3 < 1$:

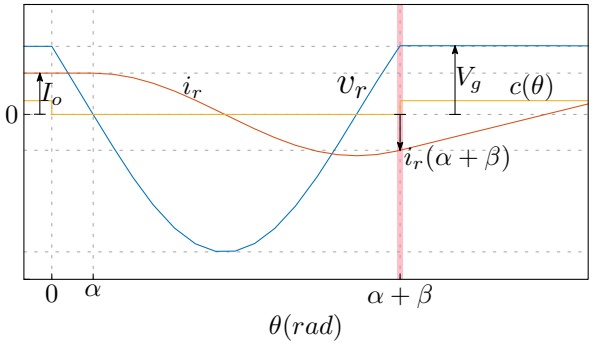
  The resonant voltage never reaches the input voltage level in the operating mode where $J < 1$, and the ZVS operation is not either granted. However, by switching the converter at the zero-current-switching (ZCS) operating point, where $\beta = \frac{3\pi}{2}$, the power switch is turned ON with the minimal voltage, as shown in Fig. 2-4(c). The aforementioned operating point is declared the partial hard-switching in this work.

So far the operation of the converter under study is investigated with ideal conditions and at the minimum switching voltage operating point. The operating point in which the voltage across the switch before turn on is zero if $j \geq 1$ and minimum value at $J < 1$. In the following section the converter operation is analyzed away from the minimum switching voltage operating point. The digression clarifies the system boundaries and system limitations.

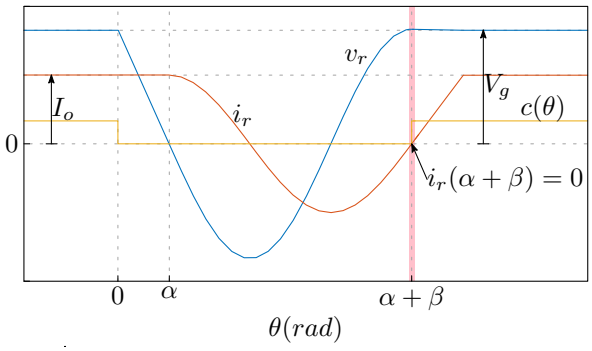
2.1.3 Operation away from the minimum switching voltage operating point

Delayed turn ON with $J > 1$

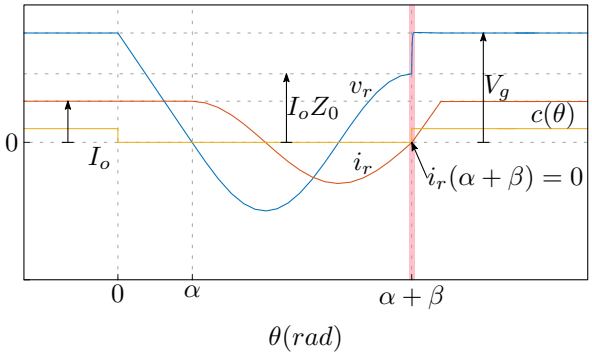
Delaying the switching on instant with an angle ζ after the ZVS point forces the switch's body diode to conduct. Accordingly, the resonant voltage will be clipped at $v_r = V_g$ as shown in Fig. 2-5(a). As shown there is no change in the converter topological states, in this case the converter has the same third topological state γ of the normal operation. The converter will not enter a different topological state until the delay angle ζ exceeds the



(a) Steady-state waveforms with $J > 1$



(b) Steady-state waveforms with $J = 1$



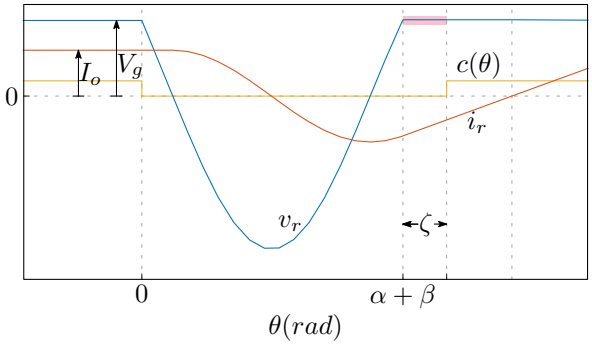
(c) Steady-state waveforms with $J < 1$

Figure 2-4: Resonant voltage v_r, resonant current i_r, and gate signal $c(\theta)$ steady-state waveforms in three different operating conditions: (a) $J > 1$, (b) $J = 1$, and (c) $J < 1$

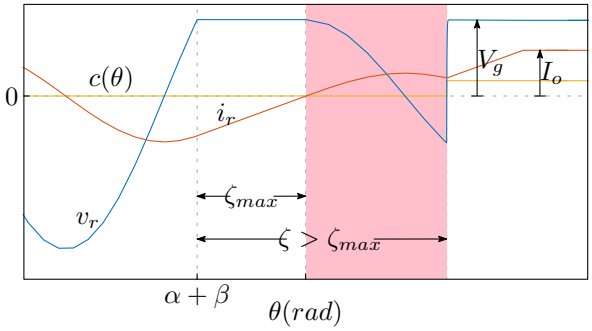
maximum value ζ_{max}, which is given by

$$\zeta_{max} = \sqrt{J^2 - 1}, \tag{2.17}$$

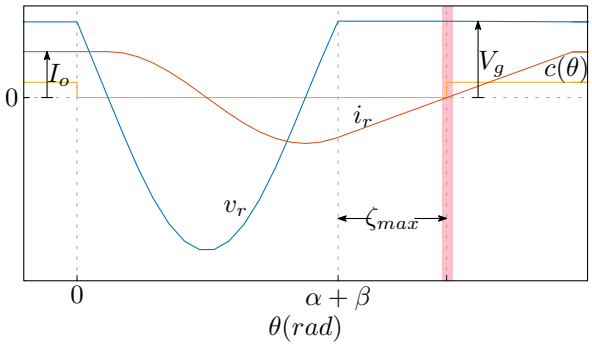
as shown in Fig. 2-5(b). At the maximum delay angle ζ_{max} the converter is operated under ZVS and ZCS as shown in Fig. 2-5(c). Hence, increasing the turn-off time has no effect on



(a) Steady-state waveforms $\zeta < \zeta_{max}$



(b) Steady-state waveforms $\zeta > \zeta_{max}$



(c) Steady-state waveforms $\zeta = \zeta_{max}$

Figure 2-5: Resonant voltage v_r, resonant current i_r, and gate signal $c(\theta)$ steady-state waveforms when the turn ON instant is delayed with angle ζ: (a) $\zeta < \zeta_{max}$, (b) $\zeta > \zeta_{max}$, and (c) $\zeta = \zeta_{max}$

the voltage conversion ratio unless the converter enters another oscillating period, which results in increasing the resonant inductor losses.

Effect of MOSFET body diode forward voltage drop

The reason why delaying the turn-on instant has no effect on the topological states is the hypothesis of ideal conditions. In practice, the power switch's body diode conducts during

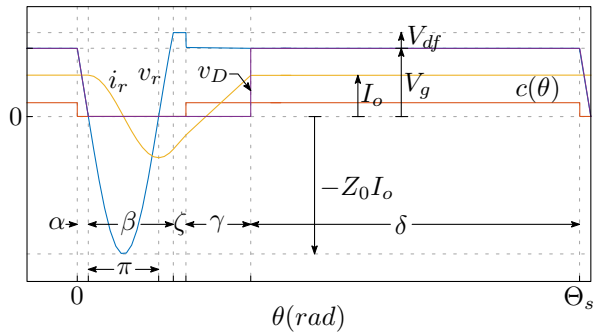


Figure 2-6: QRC waveforms by considering body-diode forward voltage V_{df} and turning ON delay ζ

the subinterval ζ. Then, considering a non-zero forward voltage V_{df} of the body diode, results in a change in the voltage conversion ratio, due to the change in the voltage across the FWD during the body diode conduction angle ζ, as shown in Fig. 2-6. The voltage conversion ratio under such condition is given by

$$\mu = 1 - \frac{F}{2\pi}\left[\frac{1}{2J} + \pi + \arcsin\left(\frac{V_g + V_{df}}{JV_g}\right) + J\left[1 + \sqrt{1 - \left(\frac{V_g + V_{df}}{JV_g}\right)^2}\right] - \frac{V_{df}}{V_g}\zeta\right]. \tag{2.18}$$

In order to quantify the effect of the body diode forward voltage, the variation in the voltage conversion ratio is calculated according to the variations in the conduction angle ζ at different values of the normalized forward voltage $\frac{V_{df}}{V_g}$, as shown in Fig. 2-7. The additional topological state, which is imposed due to the delayed turn-on and diode forward voltage, has a minor effect on the overall voltage conversion ratio μ.

Delayed turn ON with $J \leq 1$

When $J = 1$, the ZVS switching instant is also synchronized with the ZCS instant $i_r(\alpha + \beta) = 0$. The power MOSFET turn ON instant occurs when the resonant voltage reaches the maximum value V_g as shown in Fig. 2-4(b). Consequently, the body diode will never conduct and in this case the maximum delay angle $\zeta_{max} = 0$. Similarly, the same when $J < 1$ except that in the normal operation switching ON occurs at partial hard-switching as shown in Fig. 2-4(c). Partial hard-switching means when the switch is turned

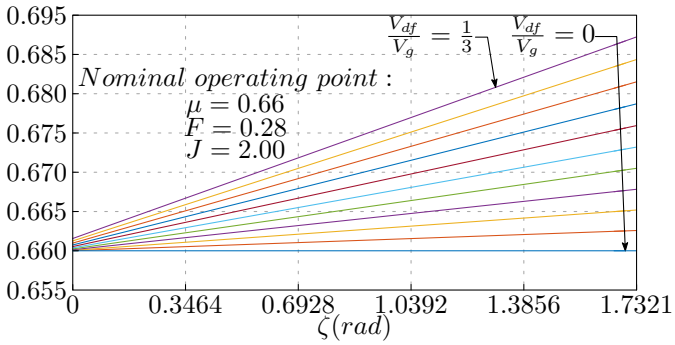


Figure 2-7: Variation in the voltage transfer ratio according to variations in the normalized body diode forward voltage ($\frac{V_{df}}{V_g}$) and turning ON delay angle ζ

ON with voltage difference less than input voltage level. Accordingly, in case of $J \leq 1$, turn on instant delay enables the switching node voltage to continue oscillating with the tank network natural frequency ω_r, where the MOSFET body diode is always reverse biased.

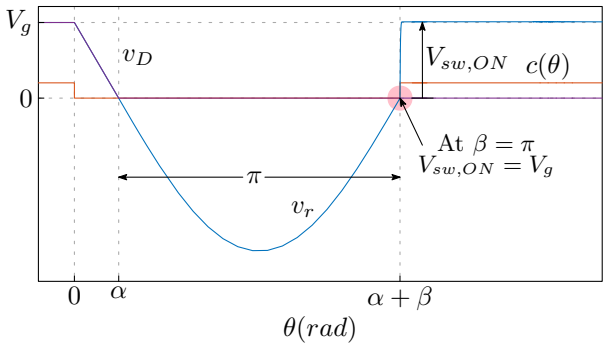
Early turning ON

Anticipating the turn-on instant before the ZVS point enables the converter to operate into two different operating regions according to value of the subinterval β and regardless of the tank voltage ratio J.

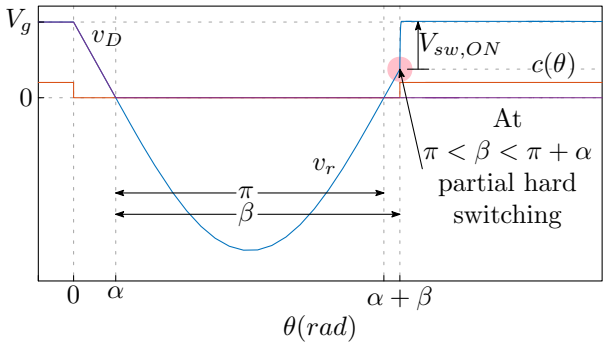
As shown earlier turning on the power switch at $\beta = \pi + \arcsin(\frac{1}{J})$ enables the converter to work with zero voltage across the switch during turn-on. Otherwise, anticipating turn-on at $\beta = \pi$ puts the power switch under voltage stress at turn-on equals V_g, as shown in Fig. 2-8(a). In the region between $\beta = \pi$ and $\beta = \pi + \arcsin(\frac{1}{J})$ the converter operates in what is called the partial hard-switching operating region, the case which is shown in Fig. 2-8(b). In that operating condition, the voltage stress across the switch at turn-on is $v_{sw}(\beta) < V_g$. At the boundary of the partial hard-switching operating region where $\beta = \pi$ the switching frequency is given by

$$f_{s,\beta=\pi} = \frac{\big(1 - D\big)\omega_r}{\pi + \dfrac{1}{J}}, \tag{2.19}$$

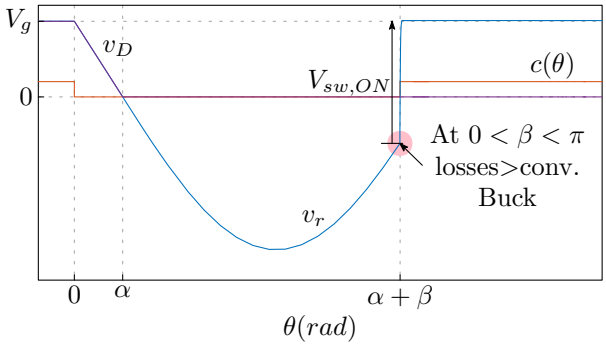
At that given frequency the capacitive switching losses are comparable with those of a



(a) QRC operated before ZVS with $\beta = \pi$, $V_{sw,ON} = J\cos(\beta) = V_g$



(b) QRC partial hard-switching operating region with $\pi < \beta < \pi + \arcsin(\frac{1}{J})$, $V_{sw,ON} = J\cos(\beta) < V_g$



(c) QRC high switching losses operating region with $0 < \beta < \pi$, $V_{sw,ON} = J\cos(\beta) > V_g$

Figure 2-8: Resonant voltage v_r, diode voltage v_D, and gate signal $c(\theta)$ steady-state waveforms when the turn ON instant is anticipated before the ZVS operating point: (a) $\beta = \pi$, (b) $\pi < \beta < \pi + \arcsin(\frac{1}{J})$, and (c) $0 < \beta < \pi$

hard-switched Buck converter. This operating point will be later considered as the worst case condition. The input voltage at such operating point is considered the maximum value beyond which advantages of the quasi resonant structure are lost. The MOSFET in the region $0 < \beta < \pi$ is exposed to a higher voltage stress than that in the conventional buck

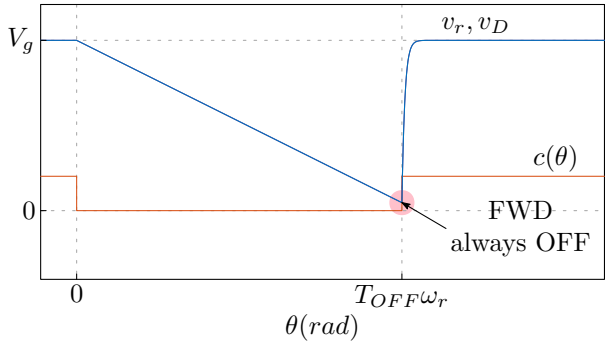


Figure 2-9: QRC operated before ZVS with $T_{OFF} < \frac{\alpha}{\omega_r}$

converter, as shown in Fig. 2-8(c), resulting on higher switching losses

As shown in Fig. 2-8 the converter switches between two topological states during the turn-off time T_{OFF}, when the FWD starts to conduct after the subinterval α. Hence, at the operating point when $T_{OFF} = \frac{\alpha}{\omega_r}$ the FWD has a zero conduction period $\beta = 0$, and the operating frequency at that particular operating point is given by

$$f_{s_{max},\beta=0} = J\big(1 - D\big)\omega_r. \tag{2.20}$$

Afterwards, the converter entirely loses the switching operation of the FWD with $T_{OFF} < \frac{\alpha}{\omega_r}$ and hence $v_D = v_r$ which leads to continuous voltage across the output filter stage, as shown in Fig. 2-9. That operating condition most likely happens at light loads when the resonant capacitor voltage is slowly discharging due to the low current in the output filter inductor which may leads to $T_{OFF} < \frac{\alpha}{\omega_r}$.

2.2 Voltage Mode Control

2.2.1 Constant OFF-Time Controller

As shown in (2.16) the output voltage depends on the switching frequency. Therefore, according to the analysis shown earlier in subsection 2.1.3, the constant OFF time variable frequency modulator is used conventionally for output voltage regulation loop in the QRC control, as shown in Fig. 2-10.

Observe that ZVS condition (2.3) is only satisfied over a certain range of input volt-

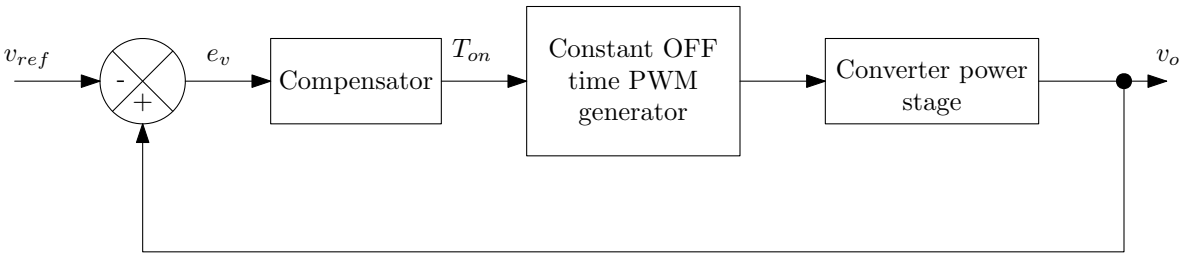


Figure 2-10: Conventional QRC output voltage regulation loop

ages and load currents, while it is violated under light load conditions and/or at high input voltages. The operating point where the voltage across the switch before turn-on becomes equal to V_g is the worst case condition and the input voltage at such operating point is considered as the maximum input voltage and given by

$$V_{g,wc} = Z_0 I_o(\omega_r T_{OFF} - \pi), \tag{2.21}$$

where at $V_g = V_{g,wc}$ the situation becomes comparable with that of a conventional synchronous Buck converter.

ON-time and operating frequency limitation

The ON time must be large enough to allow the freewheeling diode (FWD) to turn off, otherwise the converter will lose the conversion action. Hence, the minimum ON time $T_{ON_{min}}$ will be defined when the sub-interval $\delta = 0$ and given by

$$T_{ON_{min}} = \frac{\gamma}{\omega_r}. \tag{2.22}$$

Considering the constant OFF-time modulator then the maximum switching frequency will be given by

$$f_{s,max} = \frac{1}{T_{OFF} + \frac{\gamma}{\omega_r}}, \tag{2.23}$$

recalling the expressions of γ and J from (2.11) and (2.4) respectively, then the expression of maximum operating frequency in (2.23) will be given by

$$f_{s,max} = \frac{1}{T_{OFF} + \frac{\frac{I_o Z_0}{V_g}\left(1+\sqrt{1-\left(\frac{V_g}{I_o Z_0}\right)^2}\right)}{\omega_r}}. \tag{2.24}$$

Practically, with input voltage and/or load current variations the constant OFF-time controller responds by changing the modulating signal ON-time, and hence the operating frequency. For example, with a constant input voltage V_g the controller increases the operating frequency in order to compensate a load current reduction perturbation. At the load current level where the (2.22) is true, the converter operates with the maximum operating frequency. Afterwards, the converter will entirely loose the regulation action.

2.3 Proposed Digital Efficiency Optimization Technique

So far the converter analysis shows the strong dependency of the operation and boundary conditions on the circuit and operating parameters. Consequently, in this section the developed digital efficiency optimization technique is reported. The technique has the advantage of reducing the converter operation dependency on the circuit parameters, in addition to extending the converter operating range.

2.3.1 Introduction

Sensing the variation in the circuit parameters and operating condition, in order to improve the QRC operation, is quite challenging and increases the system complexity. In this work, a simplified mixed-signal architecture is proposed in order to improve the overall performance of the converter under study.

Variation in the converter input voltage and load current may be represented in a variation of J. The time from turn-off instant until the FWD turn-on instant, where the resonant

voltage cross zero value to negative, as shown in Fig. 2-11(a), is given by

$$t_\alpha = \frac{1}{J\omega_r}. \tag{2.25}$$

Accordingly, sensing the time t_α inherently gives a sense about the input voltage, load current, and tank network parameters variations. Moreover, the time between the positive-slope zero-crossing of the resonant voltage and the optimum turn-on instant t_λ is given by

$$t_\lambda = \frac{\arcsin(\omega_r t_\alpha)}{\omega_r}, \tag{2.26}$$

as long as the ZVS condition $J > 1$ is fulfilled, as shown in Fig. 2-11(a). Otherwise, the optimum turn-on instant, with minimal voltage across the switch before turn-on and ZCS, is $\frac{\pi}{2}$ away from the positive-slope zero-crossing of the resonant voltage. Hence, in a such condition the time t_λ is given by

$$t_{\lambda|J\leq 1} = \frac{\pi}{2\omega_r}, \tag{2.27}$$

regardless of the operating condition, as shown in Fig. 2-11(b). Therefore, the technique relies on, firstly, measuring the time between turn off instant and resonant voltage negative slope zero-crossing t_α. Subsequently, the ZVS turn on instant is simply generated t_α after the resonant voltage positive slope zero crossing in case of $t_\alpha < \frac{\pi}{2\omega_r}$. Otherwise, the optimum turn on instant is always after $\frac{\pi}{2\omega_r}$ from the v_r positive zero-crossing. Consequently, the core of the proposed technique relies on the approximation,

$$t_\lambda = \begin{cases} t_\alpha & \alpha < \frac{\pi}{2} \\ \frac{\pi}{2\omega_r} & \alpha \geq \frac{\pi}{2} \end{cases} \tag{2.28}$$

That approximation $t_\lambda \approx t_\alpha$ is only true around small values of the angle α mathematically, however, as will be shown later, such approximation has a minor effect on the converter performance and efficiency even for higher values of α. Consequently, by measuring t_α and replicating such interval after the positive-slope zero-crossing of resonant voltage for the generation of the switch turn-on, ZVS is automatically achieved. Moreover, the optimum turn-on instant is $\frac{\pi}{2\omega_r}$ after the second zero-crossing of resonant voltage for all values of

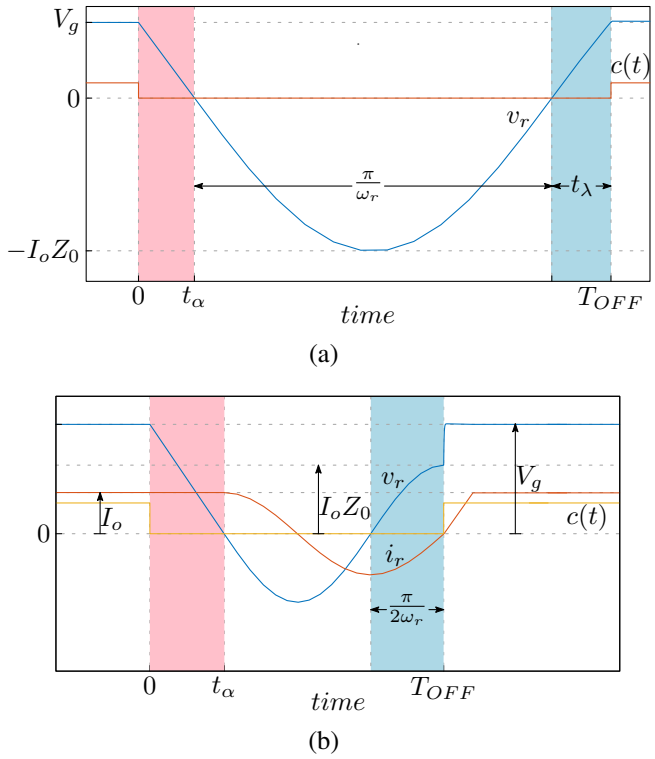


Figure 2-11: Proposed technique basic concept: (a) $J > 1$ and (b) $J \leq 1$

$t_\alpha \geq \frac{\pi}{2\omega_r}$.

As clarified above, and as it will be further validated in the simulation and experimental results, such control strategy provides a near-optimal determination of the turn-on instant: within the ZVS range $J \geq 1$, the switch is turned-on as soon as $v_r = V_g$, i.e. $V_{sw,on} = 0$; outside the ZVS range $J < 1$ the switch is turned on in close proximity of the peak of the resonant voltage v_r, therefore mitigating hardswitching losses. Observe that this has the beneficial side effect of minimizing freewheeling conduction losses of the switch body diode.

2.3.2 Digital implementation and limitations

According to the system block diagram shown in Fig. 2-12, the constant T_{OFF} modulator in the conventional system is replaced with programmable T_{OFF} modulator (P-T_{OFF} PWM). The operation of the proposed system is described with the following steps:

1. A delay-line or a counter starts after the power switch turn-off instant,

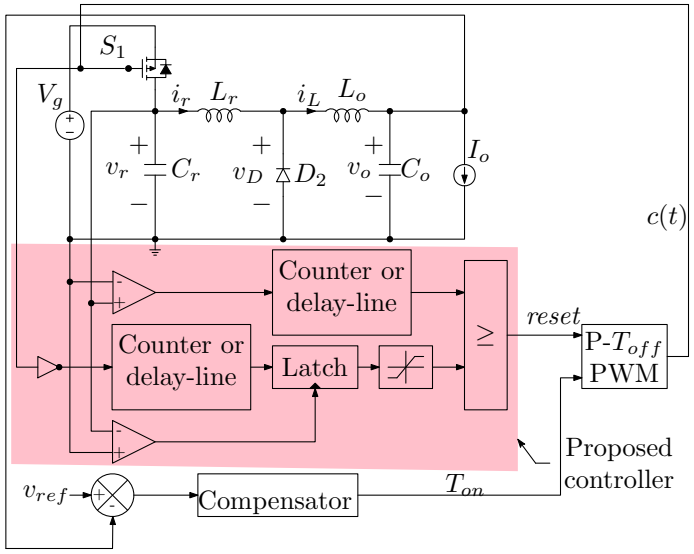


Figure 2-12: Proposed controller block diagram

2. An analogue comparator is used to generate a latch signal for the value which is generated by the delay-line/counter at the negative-slope zero-crossing of v_r,

3. The latched value is saturated at the $\frac{pi}{2}$ digital equivalent,

4. Another delay line/counter starts after v_r positive-slope zero-crossing,

5. A digital comparator is used to compare the value of the second delay-line/counter with the latched value to generate the optimum turn-on trigger signal.

Measurement of interval α is affected by errors and inaccuracies originating from:

- Zero-crossing propagation delay T_{ZC};
- Gate-drive circuitry propagation delay T_{GD};
- Switch turn-on and turn-off propagation delays T_{switch};
- Digital circuits (latches and comparators) propagation delays $T_{digital}$.

As long as such delays can be represented or approximated as a constant source of error T_{error}, their combined effect can be compensated in various ways, depending on the implementation technique.

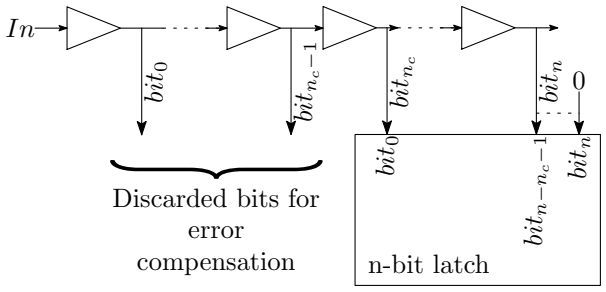


Figure 2-13: Error compensation in the measurement of α in the case of delay-line implementation.

If a delay-line is used to provide a thermometric coding of α, delay compensation can be simply achieved, as shown in Fig. 2-13, by discarding a certain number n_C of bits equivalent to T_{error}. In a counter-based implementation, on the other hand, one could simply subtract T_{error} from the measured time.

2.3.3 Input voltage range extension

With constant off-time modulation, the worst-case condition $V_{sw,on} = V_g$ – at which hard-switching losses are comparable with those of a hard-switched Buck converter – defines an upper value for V_g beyond which advantages of a quasi-resonant structure are lost. With the proposed controller, on the other hand, one *always* has $V_{sw,on} < V_g$. In other words, for a given maximum $V_{sw,on}$ decided at the design stage, the input voltage range of the QRBC is significantly extended when the proposed controller is used. Consider a $5\,\mathrm{V}$-to-$3.3\,\mathrm{V}$, $500\,\mathrm{mA}$ with $L_r = 1\,\mu\mathrm{H}$ and $C_r \approx 11\,\mathrm{nF}$ ($Z_0 \approx 9.5\,\Omega$) and assume a fixed off-time is designed to achieve $J = 1$ at nominal input voltage and maximum load current. At such operating point one has, in virtue of (2.25) and (2.26),

$$\omega_r T_{OFF} = \alpha + \beta = 1 + \frac{3}{2}\pi, \tag{2.29}$$

and the worst-case input voltage (2.21) with constant off-time modulation is $V_{g,wc} \approx 12\,\mathrm{V}$. Steady-state waveforms are reported in Fig. 2-14(a). By optimizing the off-time interval with the proposed controller, on the other hand, one achieves approximately the same $V_{sw,on} \approx 12\,\mathrm{V}$ at $V_g \approx 16.6\,\mathrm{V}$, as illustrated in Fig. 2-14(b). More generally, the relation-

ships between normalized $V_{sw,on}$ and V_g for a standard Buck converter, a constant off-time QRBC and a QRBC optimized with the proposed controller, are compared in Fig. 2-15 for the above-mentioned design example.

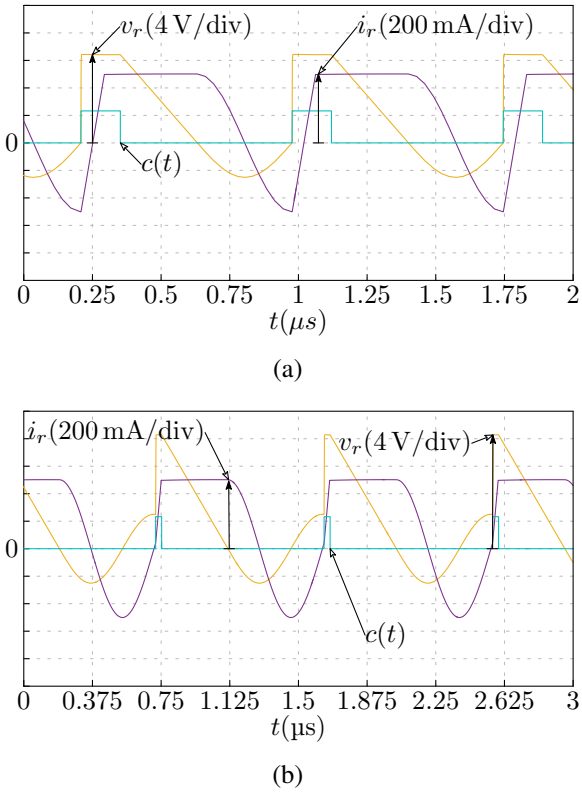


Figure 2-14: Simulated resonant voltage v_r, resonant current i_r and gating signal c of the QRBC operated under (a) constant off-time modulation and input voltage $V_g \approx 12\,\text{V}$, and (b) proposed optimized modulation and input voltage $V_g \approx 16.6\,\text{V}$. Switch turn-on voltage is $V_{sw,on} \approx 12\,\text{V}$ in both cases.

2.3.4 Compression of Switching Frequency Variation Range

As shown earlier, the freewheeling diode OFF-interval $T_{OFF,FWD}$ is

$$T_{OFF,FWD} = T_{OFF} - \frac{\alpha}{\omega_r} + \frac{\gamma}{\omega_r}. \tag{2.30}$$

Since α is proportional to V_g and inversely proportional to I_o, $T_{OFF,FWD}$ decreases for increasing input voltages and increases with increasing load current levels. Since the converter output voltage is equal to the average voltage V_D across the freewheeling diode, impact

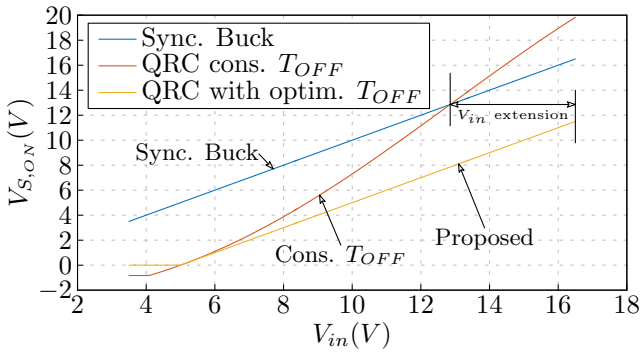


Figure 2-15: Turn-on switch voltage $V_{sw,on}$ versus converter input voltage V_g for a standard Buck converter, a constant off-time QRBC and the proposed optimized QRBC.

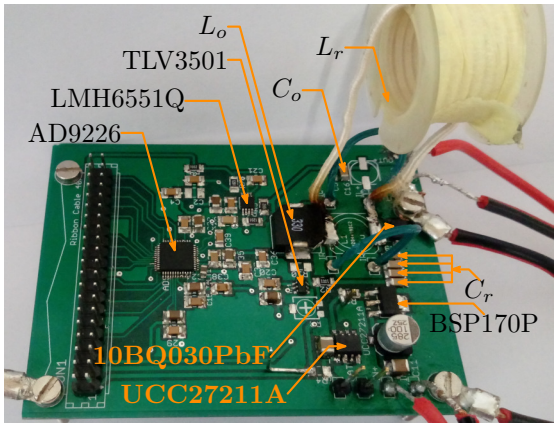


Figure 2-16: Experimental prototype.

of V_g and I_o on $T_{OFF,FWD}$ translates into wide switching rate variations required for output voltage regulation.

With the proposed optimization technique, on the other hand, the off-time is inherently increased with increasing input voltages and/or decreasing load currents, partially compensating the above effect. This leads to a much more compressed range of switching frequency variation, which is an interesting feature in a variable-switching rate controller. This advantage of the proposed approach is verified experimentally in subsection 2.3.5.

2.3.5 Experimental results

A 5 V-to-3.3 V, 500 mA QRBC converter is prototyped using discrete components, as shown in Fig. 2-16, with the parameters reported in Table 2.1. A commercial FPGA

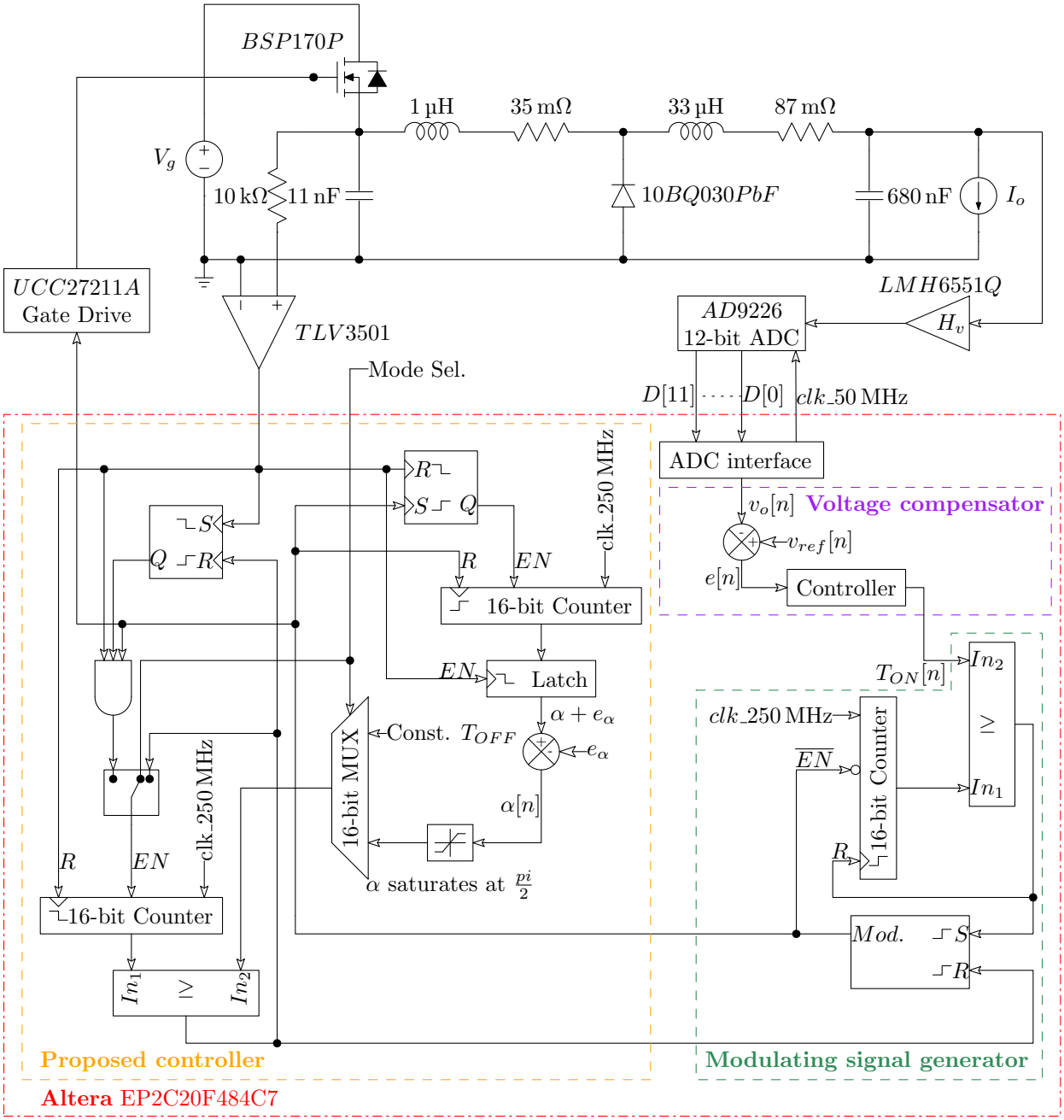


Figure 2-17: Practical implementation of the proposed technique.

development board is used to implement the digital voltage compensation loop and the proposed turn-on optimization loop as shown in Fig. 2-17. Voltage compensator is developed according to the quasi-resonant converter small signal model presented in [22,35–38]. Fig. 2-18(a) and Fig. 2-18(b) respectively report the steady-state waveforms at full load current and nominal input voltage $V_g = 5\,\mathrm{V}$ with a conventional constant off-time modulation

Table 2.1: Experimental prototype parameters

Input voltage V_g	$5\,\mathrm{V}$
Output voltage V_o	$3.3\,\mathrm{V}$
Output current I_o	$500\,\mathrm{mA}$
Nominal switching frequency f_s	$500\,\mathrm{kHz}$
Resonant capacitor C_r	$11\,\mathrm{nF}$
Resonant Inductor L_r	$1\,\mu\mathrm{H}$
Filter inductance L_o	$33\,\mu\mathrm{H}$
Filter capacitance C_o	$680\,\mathrm{nF}$
P-MOS	BSP170P
Free-wheeling diode	VS-10BQ030PbF
Gate-drive IC	UCC27211A
Zero-crossing detector	TLV3501
Feedback amplifier	LMH6551Q
ADC	AD9226
FPGA	EP2C20F484C7

and with the proposed technique. The worst-case input voltage for this converter, as defined in (2.21), is $V_g = 11.3\,\mathrm{V}$, which also corresponds to the switch voltage at turn-on. The small mismatch between the analytical worst-case voltage $\approx 12\,\mathrm{V}$ and the experimental measured value $11.3\,\mathrm{V}$ is due to the damping effect of circuit parasitics. Experimental steady-state waveforms at such operating point and with a conventional constant off-time modulation are shown in Fig. 2-18(c), matching the simulation results shown earlier in Fig. 2-14(a). Once the proposed controller is enabled, an approximately $4\,\mathrm{V}$ reduction in the switch voltage at turn-on is achieved, as shown in Fig. 2-18(d). Furthermore, the switch turn-on action is performed under zero-current-switching (ZCS). Consequently, a substantial efficiency improvement is expected outside the ZVS operating range as will be shown later in the efficiency measurements. With the proposed digital optimizer enabled, the input voltage can be further increased to $V_g = 16\,\mathrm{V}$, as shown in Fig. 2-18(e), confirming the extension of available input voltage range enabled by the technique. At $V_g = 16\,\mathrm{V}$ the switch voltage at turn-on is $V_{sw,on} \approx 12\,\mathrm{V}$.

Steady-state waveforms shown in Fig. 2-19(a) and Fig. 2-19(b) also illustrate that the proposed digital optimizer extends the operating range in terms of minimum load current.

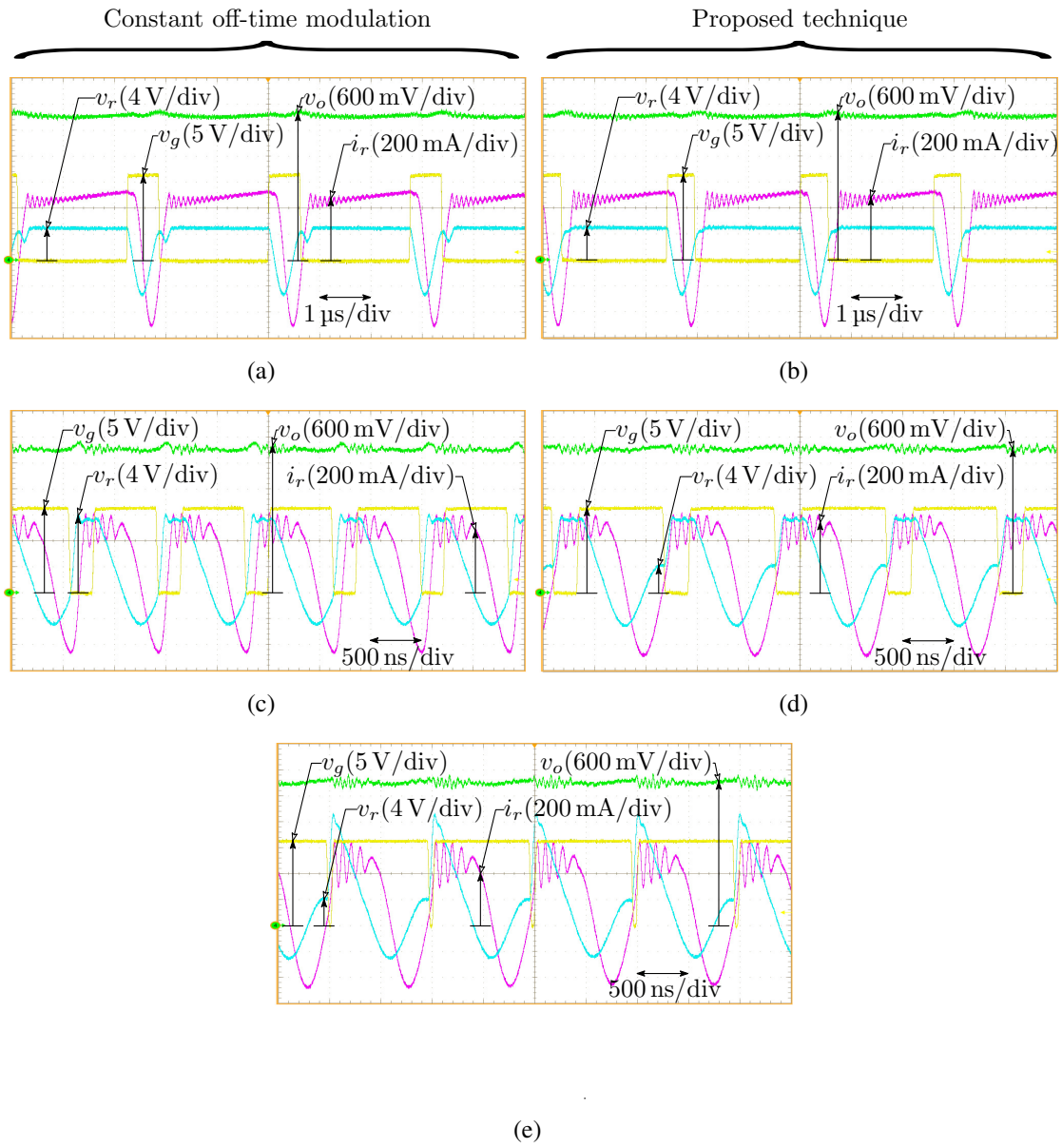


Figure 2-18: Experimental steady-state waveforms at full load current $I_o = 500\,\text{mA}$: (a) nominal operating point $V_g = 5\,\text{V}$ with constant off-time modulation, (b) nominal operating point $V_g = 5\,\text{V}$ with proposed optimization technique, (c) worst-case input voltage $V_{g,wc} = 11.3\,\text{V}$ with constant off-time modulation ($V_{sw,on} = 11.3\,\text{V}$), (d) $V_g = 11.3\,\text{V}$ with proposed optimization technique ($V_{sw,on} = 7\,\text{V}$), and (e) maximum input voltage $V_g = 16\,\text{V}$ with proposed optimization technique ($V_{sw,on} = 12\,\text{V}$).

Moreover, the proposed optimizer is introduced with the deadbeat operation feature, where the developed architecture is able to predict the optimum turn-on instant on cycle basis. Hence, as shown in Fig. 2-20 during a $50\,\%$-$100\,\%$ load step the developed controller is

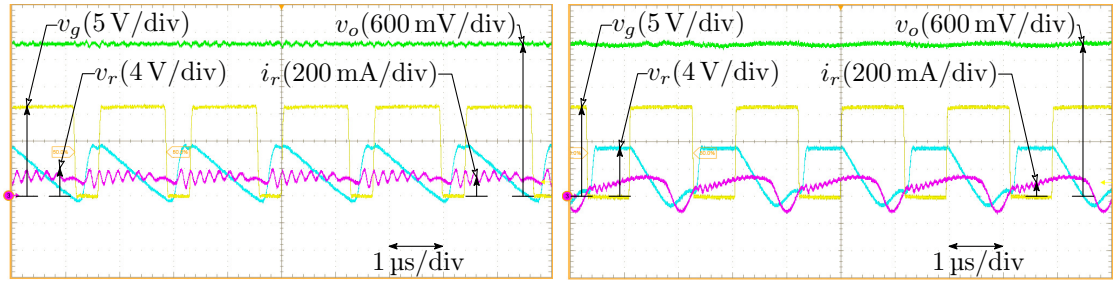


Figure 2-19: Experimental steady-state waveforms: (a) results at input voltage ($V_g = 7\,\mathrm{V}$) and load current ($I_o = 139\,\mathrm{mA}$) with constant off-time modulation and (b) results at input voltage ($V_g = 7\,\mathrm{V}$) and load current ($I_o = 100\,\mathrm{mA}$) with proposed controller.

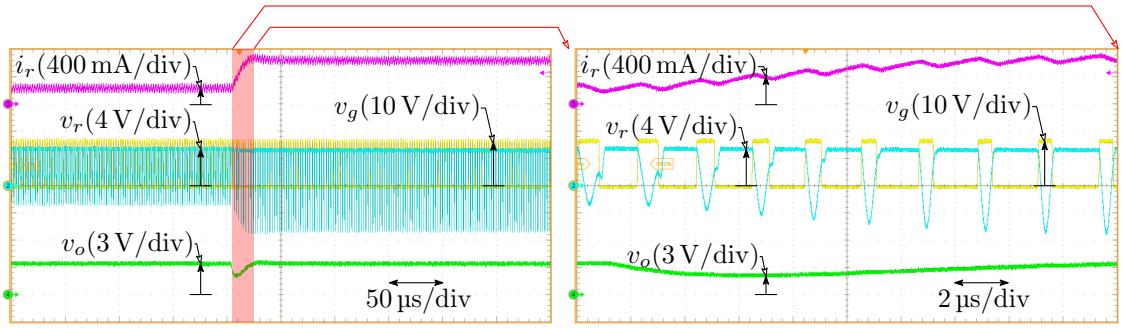


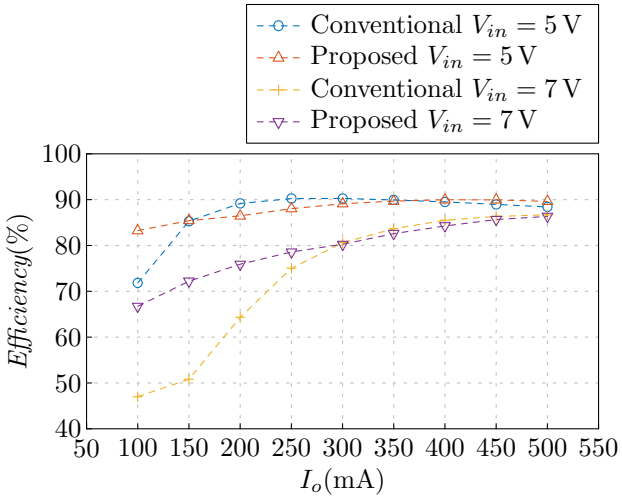
Figure 2-20: 50 %-100 % load step verifies the deadbeat operation of the converter.

cycle-by-cycle following the optimum turn-on point.

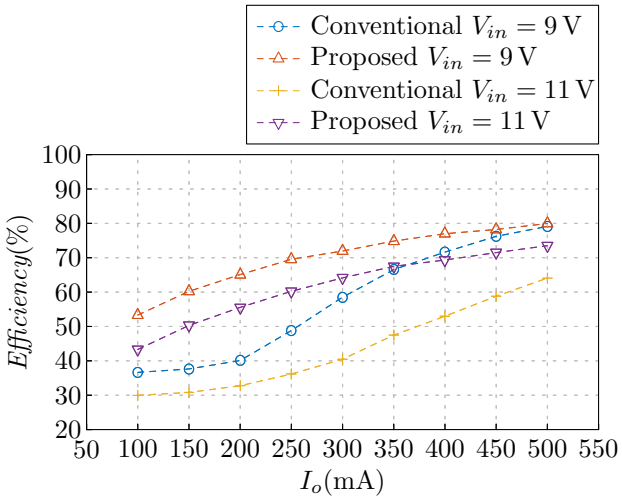
Experimental Efficiency Measurements

The prototype is tested with different input voltages and load currents. Corresponding efficiency plots are reported in Fig. 2-21(a) and Fig. 2-21(b).

As expected, the conventional and proposed technique exhibit comparable efficiency figures around the nominal operating point. On the other hand, significant improvement in the converter efficiency at light loads and away from the nominal input voltage can be observed by comparing the results shown in Fig. 2-21(a) and Fig. 2-21(b). As anticipated in subsection 2.3.4, proposed optimization technique compresses the switching frequency variation range, as shown in Fig. 2-22(a) and Fig. 2-22(b). Notice that the decreased switching frequency, in addition to decreased switch turn-on voltage $V_{sw,on}$, improve the converter



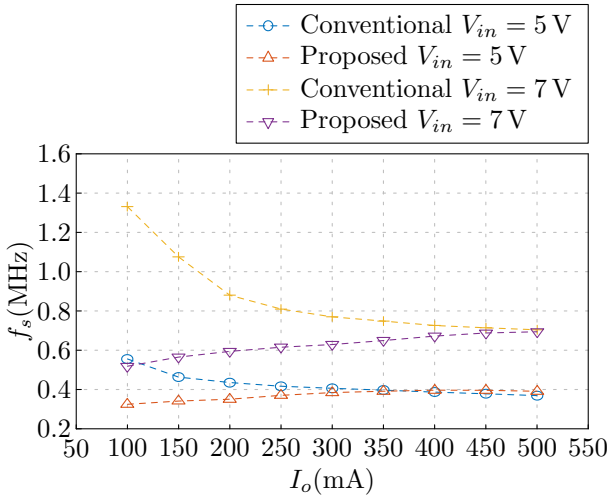
(a)



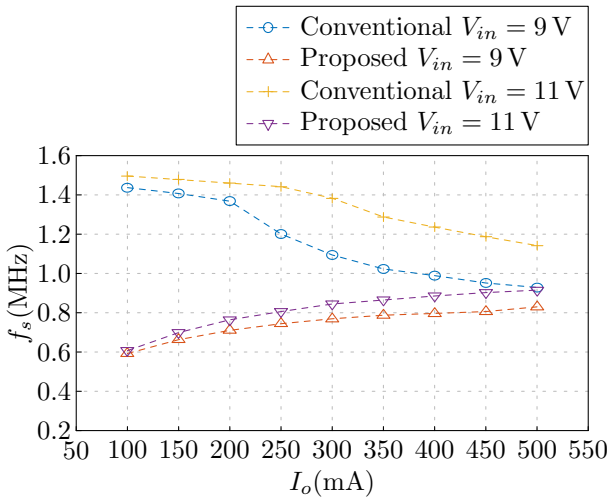
(b)

Figure 2-21: Converter efficiency at different input voltages and load levels: (a) converter efficiency at input voltage ($V_g = 5\,\mathrm{V}$ and $7\,\mathrm{V}$) and (b) converter efficiency at input voltage ($V_g = 9\,\mathrm{V}$ and $11\,\mathrm{V}$).

efficiency significantly outside the ZVS range. Fixed gate driving losses, not included in the above efficiency measurements, do not qualitatively change the impact of the proposed technique. In an integrated realization of the converter, where the gate driving circuit can be tailored to the integrated switch, such contribution can be significantly optimized.



(a)



(b)

Figure 2-22: Converter switching frequency variations at different input voltages and load levels: (a) switching frequency variations at input voltage ($V_g = 5\,\mathrm{V}$ and $7\,\mathrm{V}$) and (b) switching frequency variations at input voltage ($V_g = 9\,\mathrm{V}$ and $11\,\mathrm{V}$).

2.4 Summary and Contribution

In this chapter, the zero-voltage switched quasi-resonant buck converter is studied in detail. The converter investigation is extended to include the operation away from the minimum voltage across the switch operating point, where the conventional controller limitations and boundary conditions are reported. A low-complexity efficiency optimization technique for high-frequency quasi-resonant buck converters is developed. The technique minimizes the

voltage across the active switch at the device turn-on via a cycle-by-cycle digital correction of the turn-off interval, while simultaneously extending the input voltage range of the converter for a given maximum switch turn-on voltage. Furthermore, a beneficial side effect of the proposed approach is a compression of the switching frequency variation range over a conventional constant off-time modulation. The low-complexity of the proposed technique makes it suitable to be embedded into an integrated controller. The approach is discussed theoretically and with simulation examples, including provisions for compensating errors arising in the involved time measurements. The technique is then experimentally verified on a $5\,\mathrm{V}$-to-$3.3\,\mathrm{V}$, $500\,\mathrm{mA}$ discrete QRC prototype, confirming the aforementioned advantages. The analysis and results of the proposed digital efficiency optimization technique is published in [16].

Chapter 3

Three-level Flying-Capacitor dc-dc Buck Converter

3.1 Introduction

Multi-level flying-capacitor converters were originally introduced in [15] as versatile multi-level commutation cells in the context of high-voltage, high-power converter applications. Later on, such architecture became attractive as a compact solution for the dual $42/14V$ automotive system [18]. Even more recently, the three-level flying-capacitor (3LFC) topology shown in Fig. 3-1(a) has gained interest for space-constrained low-voltage, low-power conversion automotive applications [20, 39, 40]. By halving the voltage swing across the filter inductance with respect to the traditional Buck converter, the 3LFC has the immediate advantage of reducing the size of the magnetic element. Other attractive features of the topology include a reduced MOSFET voltage rating, fast transient response and a Buck-like, wide range voltage conversion ratio [1, 5–7, 10–12, 14, 19, 20].

One profound difference of the 3LFC converter with respect to traditional basic topologies is the presence of an additional state variable, i.e. the flying-capacitor (FC) voltage. The importance of the FC voltage dynamics and control is well recognized in the literature of both high-voltage multilevel converters [41–45] and low-power 3LFC [5, 7, 14]. As a matter of fact, most of the real advantages of the 3LFC topology directly descend from the FC voltage being stable and balanced, i.e. that its equilibrium point is stable and equal to

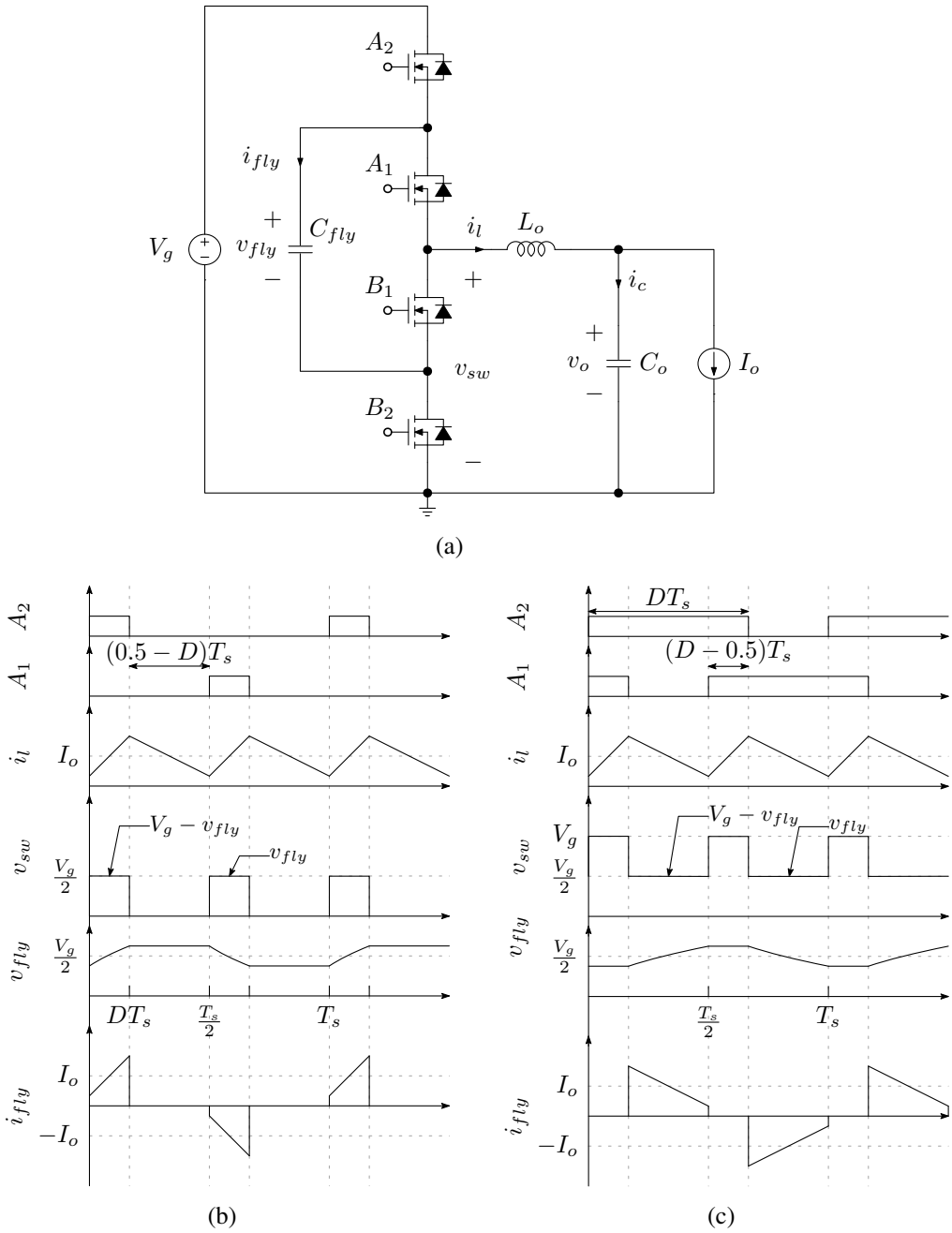


Figure 3-1: Three-level flying-capacitor converter: (a) 3L-FC converter topology, (b) steady-state waveforms in case of $M < 0.5$ and balanced FC-voltage, and (c) steady-state waveforms in case of $M > 0.5$ and balanced FC-voltage

$\frac{V_g}{2}$. For example, as long as the FC voltage is balanced, the switching node voltage swing equals $\frac{V_g}{2}$, with an effective switching frequency equal to twice of the switching rate $2f_s$, as shown in Fig. 3-1(b)-(c), resulting in reduced inductor size by four times [5]. Voltage stress

across the switches also critically depends on the value of the FC voltage. While the FC voltage is self balanced in ideal conditions, mismatches associated with circuit parasitics, power switches, and gate-drive circuits lead to FC voltage unbalance, offsetting many of the above-mentioned benefits [5, 10, 14].

Two main challenges prevent the wide adoption of the 3LFC topology, both are related to the FC-voltage. Firstly, at the startup the FC has zero voltage, hence the active switches suffer from higher voltage stress at startup. The problem is addressed in [5] by applying a startup routine which softly charges the FC until $V_{fly} = \frac{V_g}{2}$. However, still the upper switch must block the full input voltage at the power-up until starting the FC charging. The problem still presents an open research point in the topology under study, because using a higher voltage rating device for the upper switch affects the efficiency improvement achieved in the 3LFC. On the other hand, during the converter normal operation, ideally the FC voltage is self-balanced. However, circuit parasitics and system tolerances lead to FC-voltage unbalance. Consequently, the second challenge in the converter under study is about developing a reliable control architecture which grantee balanced FC voltage while the output voltage is kept well regulated. The issue which is addressed within this desertion.

3.2 Ideal Operating Modes

3.2.1 Introduction

In the 3LFC topology there are two groups of switches, i.e. (A_1, B_1) and (A_2, B_2). Switches belonging to the same group are driven in a complementary fashion, while the two switching groups are driven with an interleaving delay equal to $T_s/2$. The interleaved switching strategy splits the converter operation into two different operating modes according to voltage conversion ratio $(M < 0.5)$ and $(M > 0.5)$ as shown in Fig. 3-1(b)-(c) respectively. Ideally the converter voltage conversion ratio M is equal the duty cycle D like the conventional buck topology. Such modulating strategy enables the switching node voltage to swing with voltage difference always equal to $\frac{V_g}{2}$ with a frequency equal to twice of the switching rate. In the operating mode $M < 0.5$ the switching node voltage is modulated

between 0 and $\frac{V_g}{2}$, as shown in Fig. 3-1(b). On the other hand, the switching node voltage is DC shifted by $\frac{V_g}{2}$ enabling the voltage swinging between $\frac{V_g}{2}$ and V_g in the operating mode $M > 0.5$, as shown in Fig. 3-1(c). The reduced voltage variation across the switching node in addition to the increased inductor and output capacitor voltage ripples frequencies give the direct advantage of inductor size reduction and output capacitor size reduction by factors of 4 and 8 respectively compared to the conventional buck converter [46–48], as shown in Fig. 3-2. However, the converter has an additional passive element which is the flying-capacitor. A discussion regarding the passive elements design is shown later. It is important to recognize that, although the output filter stage ripple has a fundamental frequency $2f_s$, but the FC-voltage ripple and FC current has a base frequency of f_s.

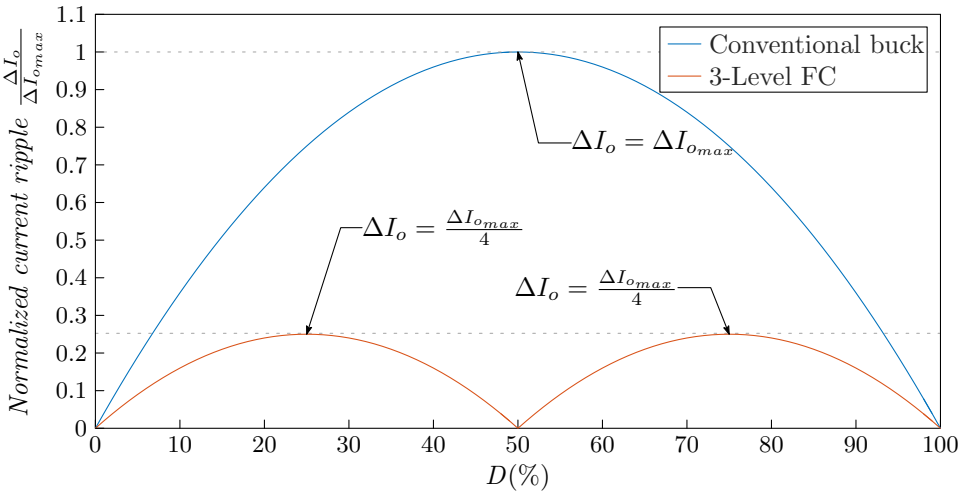
3.2.2 Operating mode with $M < 0.5$

With a voltage conversion ratio $M < 0.5$ the converter enters the first operating mode with three topological states shown in Fig. 3-3(a)-(c). Within a single switching cycle the converter switches between the first, second, and third topological states repeating the second topological state twice. Hence, the switching sequence becomes (topological state 1)→(topological state 2)→(topological state 3)→(topological state 2). Consequently, as the conventional buck converter, only two active switches are changing their states at the same time. Considering ideal conditions, then the topological states are investigated as follows.

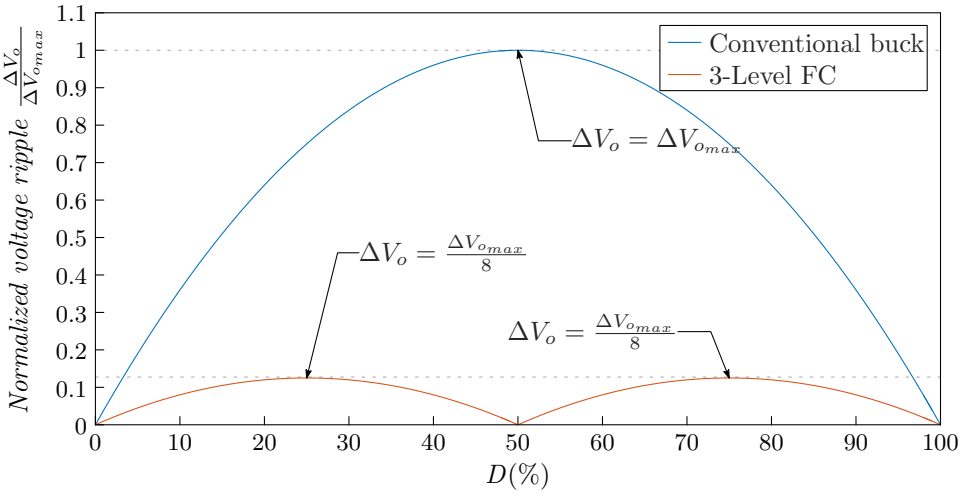
First topological state

The first topological state shown in Fig. 3-3(a) switches A_2 and B_1 are on. The output inductor current i_L ramps up charging the flying and output capacitor. Meanwhile, the switching node voltage v_{sw} is given by

$$v_{sw} = V_g - v_{fly}. \tag{3.1}$$



(a)

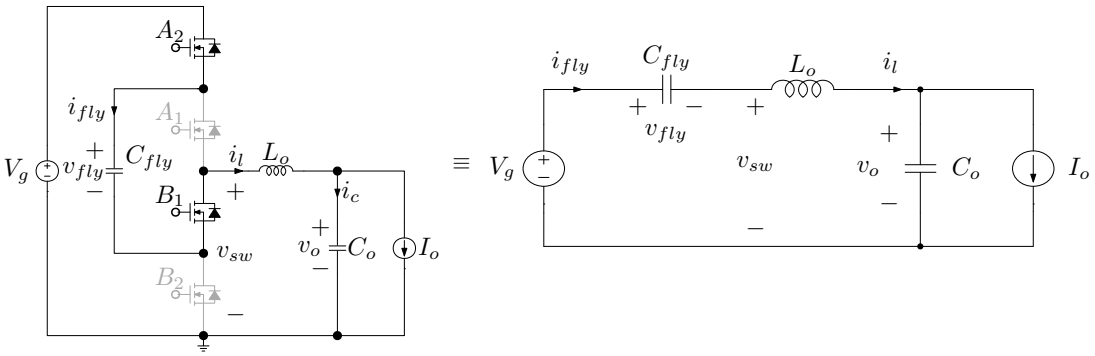


(b)

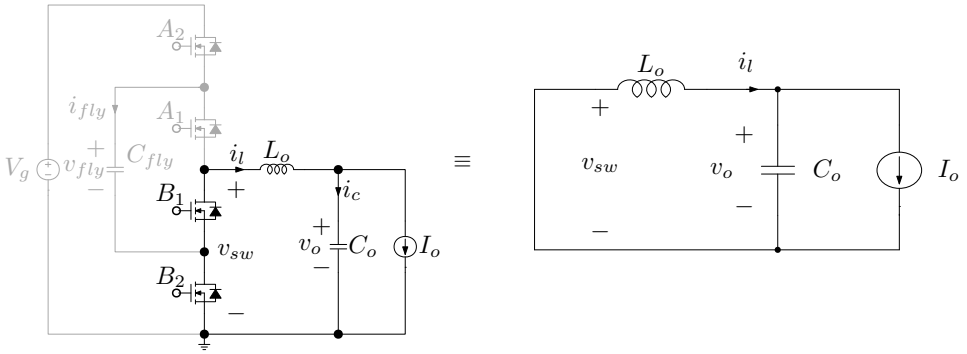
Figure 3-2: Output filter normalized ripples variation against duty cycle in conventional buck converter and 3LFC: (a) output inductor current normalized ripple and (b) output capacitor voltage normalized ripple

Second topological state

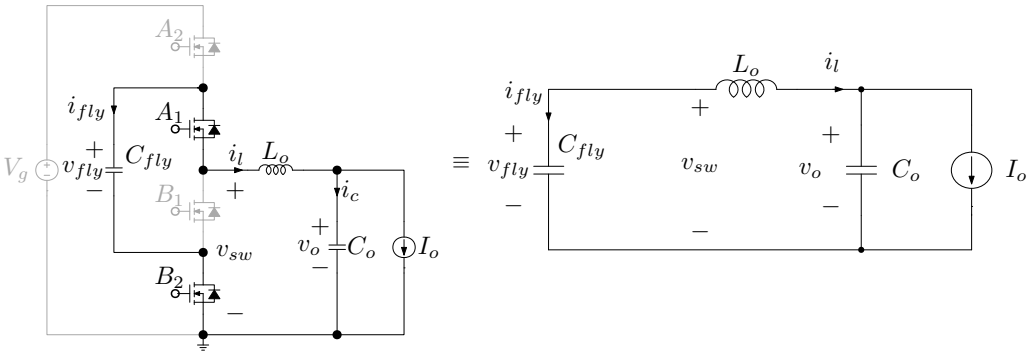
Here, the inductor current is discharging, where B_2 and A_2 are turned on and off respectively, as shown in Fig. 3-3(b). Accordingly, the FC is floating and switching node is grounded ($v_{sw} = 0$).



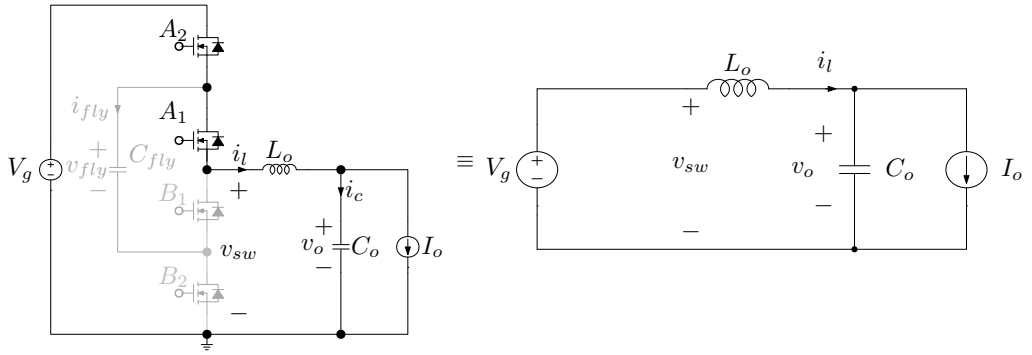
(a) First topological state A_2 and B_1 are ON



(b) Second topological state B_1 and B_2 are ON



(c) Third topological state A_1 and B_2 are ON



(d) Fourth topological state A_1 and A_2 are ON

Figure 3-3: Three-level flying-capacitor converter topological states

Third topological state

By turning off B_1 and turning on A_1 the converter switched to the third topological state shown in Fig. 3-3(c). Here, the FC is directly connected to the switching node and discharging into the output filter and load. Consequently, the switching node voltage is given by $v_{sw} = v_{fly}$.

Afterwards, the converter repeats the topological state 2 before starting a new switching cycle. Considering the ideal conditions hypothesis then the the switching node voltage swings between 0 and $\frac{V_g}{2}$ twice/switching-cycle, where the output inductor current ripple ΔI_L, output capacitor voltage ripple ΔV_o, and FC voltage ripple ΔV_{fly} are respectively given by

$$\Delta I_{L,M<0.5} = \frac{V_g D(0.5 - D)}{L_o f_s}, \tag{3.2}$$

$$\Delta V_{o,M<0.5} = \frac{V_g D(0.5 - D)}{16 L_o C_o {f_s}^2}, \tag{3.3}$$

$$\Delta V_{fly,M<0.5} = \frac{D I_o}{C_{fly} f_s}, \tag{3.4}$$

and represented in the steady-state waveforms shown in Fig. 3-1(b).

3.2.3 Operating mode with $M > 0.5$

Similarly, the converter switching between the first, third, and fourth topological states within a single switching cycle in the operating mode $M > 0.5$. The converter repeats the fourth topological state, shown in Fig. 3-3(d), twice in a single switching cycle. Hence, the converter switching sequence in such condition is (topological state 4)→(topological state 1)→(topological state 4)→(topological state 3), where only two active switches change states at the same time.

Fourth topological state

In this topological state both upper switches A_1 and A_2 are turned on, connecting the input source across the switching node ($v_{sw} = V_g$), as shown in Fig. 3-3(d). Meanwhile, the inductor current is charging until A_1 is turned off and B_1 is on.

Then the converter enters the first topological state, but in this operating mode the inductor current decreases where the output voltage $V_o > \frac{V_g}{2}$. Hence, during the topological state 1 the FC is charging where the FC current direction in the same direction of the inductor current, as shown in Fig. 3-1(c). Subsequent, the converter switches to the fourth topological state again after turning A_1 and B_1 on and off respectively. Finally, the converter switches to the third topological state when A_2 is turned off, where the FC is discharging with current $i_{fly} = -i_L$.

Although the switching node voltage swings with voltage difference $\frac{V_g}{2}$ like the first operating mode, in the operating mode $M > 0.5$ the switching node oscillates between V_g and $\frac{V_g}{2}$ twice/switching-cycle. Consequently, the inductor current ripple, output voltage ripple, and FC voltage ripple are respectively given by,

$$\Delta I_{o,M>0.5} = \frac{V_g(1-D)(D-0.5)}{L_o f_s}, \tag{3.5}$$

$$\Delta V_{o,M>0.5} = \frac{V_g(1-D)(D-0.5)}{16 L_o C_o {f_s}^2}, \tag{3.6}$$

$$\Delta V_{fly,M>0.5} = \frac{(1-D)I_o}{C_{fly} f_s}. \tag{3.7}$$

3.3 Passive elements design

(3.2), (3.3), (3.4), (3.5), (3.6), and (3.7) are the basic design equations to select the passive elements values.

3.3.1 Output filter size

For the output filter selection, like the conventional dc-dc converters, descending from the operating frequency, maximum allowable output voltage ripple $\Delta V_{o,max}$, devices ratings constraints, then the maximum allowable inductor current ripple $\Delta I_{L,max}$ is determined accordingly. Then from (3.2) and (3.5) the minimum inductor $L_{o,min}$ is given by

$$L_{o,min,M<0.5} = \frac{V_g M(0.5-M)}{\Delta I_{L,max} f_s}, \tag{3.8}$$

$$L_{o,min,M>0.5} = \frac{V_g(1-M)(M-0.5)}{\Delta I_{L,max} f_s}, \tag{3.9}$$

according to where the dc steady-state operating point is located, in the operating modes $M < 0.5$ or $M > 0.5$ respectively. Accordingly, the output capacitance values for the operating modes $M < 0.5$ and $M > 0.5$ are given respectively by,

$$C_{o,min,M<0.5} = \frac{V_g D(0.5-D)}{16 L_{o,min,M<0.5} \Delta V_{o,max} {f_s}^2}, \tag{3.10}$$

$$C_{o,min,M>0.5} = \frac{V_g(1-D)(D-0.5)}{16 L_{o,min,M>0.5} \Delta V_{o,max} {f_s}^2}. \tag{3.11}$$

3.3.2 Flying-capacitor value

The FC size has a direct impact on the switches voltage stress. Therefore, the maximum FC-voltage ripple $\Delta V_{fly,max}$ depends on the input voltage level and the maximum allowable voltage stress on the power switches $\Delta V_{switch,max}$, where,

$$\Delta V_{fly,max} = 2(\Delta V_{switch,max} - \frac{V_g}{2}). \tag{3.12}$$

Then the value of the minimum FC $C_{fly,min}$ is given by,

$$C_{fly,min,M<0.5} = \frac{M I_o}{\Delta V_{fly,max} f_s}, \tag{3.13}$$

$$C_{fly,min,M>0.5} = \frac{(1-M) I_o}{\Delta V_{fly,max} f_s}, \tag{3.14}$$

in the operating modes $M < 0.5$ and $M > 0.5$ respectively. For the purpose of size comparison between the 3LFC and the conventional buck converter, some researchers [11] put another constraint on the FC selection, i.e. the total capacitance $C_{fly} + C_o$ is not greater than the output capacitance of similar ripple buck converter operated with the same switching frequency. But, generally speaking the reduction in the magnetic element physical size is much larger than the FC size, so even with higher total capacitance the 3LFC topology still achieves a significant reduction in the overall converter size.

3.4 Converter start-up

The additional state variable in the 3LFC due to the presence of the FC leads to many challenges. Among these challenges, the unequally distributed voltage across the power switches at converter start-up is one of the main issues may affect the efficiency improvement which could be achieved by the 3LFC topology adoption.

The starting problem may be divided into two main challenges. The first is starting the converter normal modulation with uncharged FC. Then, the FC-voltage starts to buildup, where the power switches suffers from voltage stresses greater than the nominal value $\frac{V_g}{2}$. The time when the switches exposed to higher stresses depends on FC size, load current, output filter size, and switching frequency. Such problem prevents using lower voltage devices, which in turn affects the efficiency improvement expected to be achieved by using 3LFC. In order to overcome this challenge a start-up circuitry with a start-up routine are proposed to softly charge the FC until $V_{fly} = \frac{V_g}{2}$ before starting the converter modulation in [5]. However, another starting issue associated with converter power-up is recognized. Whereas, the upper MOSFET must be capable of blocking the converter full voltage directly after power-up until starting the start-up routine. While the FC is charging, the upper MOSFET blocked voltage decreases as the FC-voltage increases.

In order to show this property, a SIMetrix circuit level simulation is built based on $IRLML2502$ commercial HEXFET® power MOSFET, with $V_g = 16\,\mathrm{V}$, $I_o = 500\,\mathrm{mA}$, $f_{sw} = 500\,\mathrm{kHz}$, and FC charging current $I_{ch} = 500\,\mathrm{mA}$. An ideal current source is used to charge the FC to the nominal balanced voltage $\frac{V_g}{2}$. Starting the ideal current source is delayed with $2\,\mu\mathrm{s}$ from starting simulation to emulate a power-up delay. As shown in Fig. 3-4 the upper switch is blocking voltage $V_{A_2,\,blk} = V_g$ during the time between power-up and starting FC charging. Afterwards, the voltage across A_2 starts to decrease linearly with the same slope of the FC-voltage charging.

Accordingly, the higher voltage stress mitigation by anticipating the FC charging with respect to converter modulation starting is not enough to totally overcome the starting problem in the 3LFC topology. But, very recently in mid of 2018 two sets of method are proposed in [17] to overcome this challenge. These methods split the input voltage across

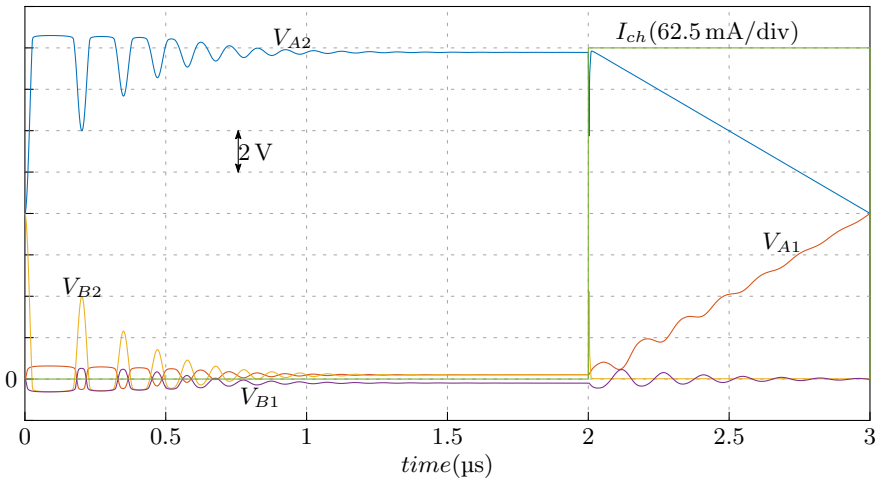


Figure 3-4: The starting problem associated with the time between power-up and end of FC charging

multiple capacitors and consequently across multiple switches in order to grantee voltage stress across the converter active elements lower than the nominal value.

3.5 Flying Capacitor Voltage Balancing

As a matter of fact, most of the real advantages of the 3LFC topology rely on that the FC voltage being stable and balanced, i.e. that its equilibrium operating point is stable and equal to $\frac{V_g}{2}$. The FC voltage is slef balanced at equilibrium point $V_{fly} = \frac{V_g}{2}$ in ideal conditions, but mismatches associated with circuit parasitics, power switches, and gate-drive circuits lead to FC voltage unbalance, offsetting many of the multi-level advantages [5, 10, 14]. Generally speaking, the circuit imperfection, asymmetrically affect the FC charging and discharging, is leading to FC voltage unbalance. Some of these mismatches affect the impedance seen by the capacitor during charging and/or discharging phases, like the MOSFET turn-on resistance $R_{ds,ON}$ mismatch. On the other hand, mismatches in charging and/or discharging periods are imposed due to asymmetrical delays, like gate drive and MOSFET turn-on and turn-off delays.

In order to quantify the effect of circuit parasitics on the FC voltage mismatch, a voltage mode controlled 3LFC simulation model, with the parameter shown in Table 3.1, is built. Using 20-step Monte Carlo SIMetrix based simulation, the variation in the FC voltage

Table 3.1: Simulation model parameters to investigate the effect of $R_{ds,ON}$ and gate derive delay on the FC voltage mismatch

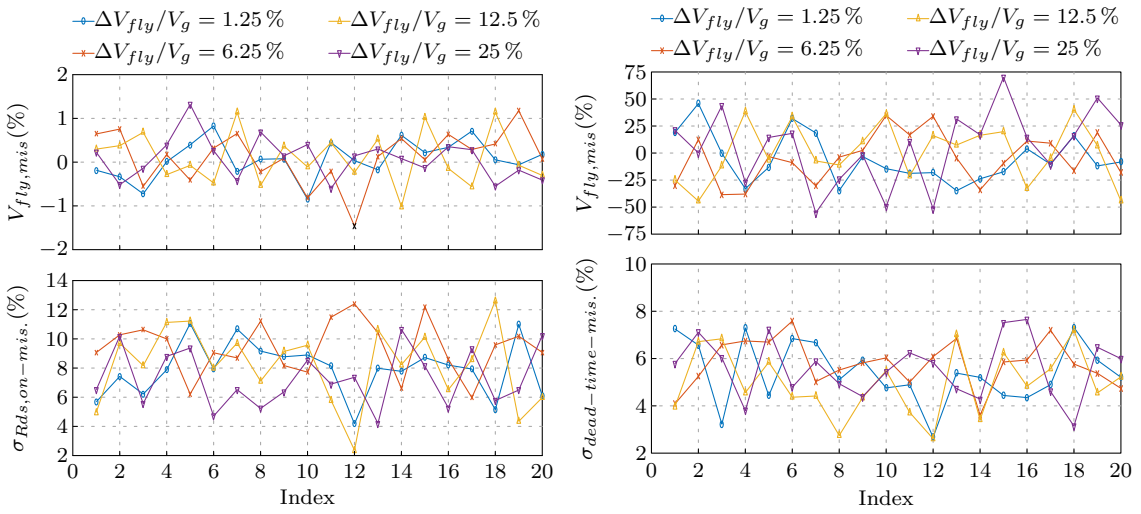
Input voltage V_g	$16\,\mathrm{V}$
Output voltage V_o	$5\,\mathrm{V}$
Load current I_o	$500\,\mathrm{mA}$
Switching frequency f_s	$500\,\mathrm{kHz}$
Inductor current normalized ripple $\frac{\Delta i_L}{I_o}$	$14\,\%$
Output voltage normalized ripple $\frac{\Delta v_o}{V_o}$	$0.1\,\%$
FC voltage normalized ripple $\frac{\Delta V_{fly}}{V_g}$	$[0.625\,\%, 3.125\,\%, 6.25\,\%, 12.5\,\%]$
Output inductance L_o	$27\,\mu\mathrm{H}$
Output capacitor C_o	$1.75\,\mu\mathrm{F}$
Flying capacitor C_{fly}	$[3125\,\mathrm{nF}, 625\,\mathrm{nF}, 313\,\mathrm{nF}, 156\,\mathrm{nF}]$

mismatch is investigated according to the variations in the MOSFET $R_{ds,ON}$ and gate drive delay uncertainties. The system is simulated with four different values of the FC $(3125\,\mathrm{nF}$, $625\,\mathrm{nF}$, $313\,\mathrm{nF}$, and $156\,\mathrm{nF})$, these values give normalized FC voltage ripples $\frac{\Delta V_{fly}}{V_g}$ of $0.625\,\%$, $3.125\,\%$, $6.25\,\%$, and $12.5\,\%$ respectively.

3.5.1 Effect of MOSFET $R_{ds,ON}$

In the first set of simulations, a $15\,\%$ mismatch in the MOSFETs $R_{ds,ON}$ is uniformly distributed around the nominal value of $39\,\mathrm{m\Omega}$. The values of the on resistances mismatches are randomly selected for each switch at every simulation step of the Monte Carlo simulation. The standard deviation of the on resistances mismatches $\sigma_{Rds,on\text{-}mis.}$ of the four MOSFETs at each simulation step is calculated in order to study the FC voltage mismatch variations with respect to the $R_{ds,ON}$ mismatch. The FC voltage normalized mismatch around the nominal value $\frac{V_g}{2}$ is calculated at each simulation step.

As can be easily observed from Fig. 3-5(a), the FC voltage mismatch is weakly depend on the MOSFET $R_{ds,ON}$ tolerances, where a FC voltage mismatch less than $2\,\%$ is observed with respect to $R_{ds,ON}$ mismatch in range of $14\,\%$.



(a) variation of the FC voltage mismatch against the variation of the standard deviation of the MOSFET $R_{ds,ON}$ mismatches at four different values of the FC

(b) variation of the FC voltage mismatch against the variation of the standard deviation of the dead-time delay mismatches at four different values of the FC

Figure 3-5: Effect of MOSFET on resistance mismatch and dead-time mismatch on the FC voltage balancing: (a) on resistance and (b) dead-time

3.5.2 Effect of gate drive uncertainty

A $10\,\%$ mismatch in the dead-time around a nominal value $t_{dd} = 20\,\mathrm{ns}$ is selected to represent the gate drive uncertainty. Similar to the first set of the simulation, at each simulation step the FC voltage mismatch is calculated. Afterwards, the normalized FC voltage mismatch is plotted against the standard deviation of the dead-time mismatch, as shown in Fig. 3-5(b). The results obtained here is remarkably different from the aforementioned case, where the FC voltage mismatch shows a strong dependency on the time delay mismatch with value could reach to $75\,\%$. To that end, using a FC voltage active balancing technique in the 3LFC topology is essential, where with time delay mismatch in range of $0.1\,\%$ of the basic switching cycle ($T_s = 2\,\mu\mathrm{s}$), the FC could lose balancing by $75\,\%$. Moreover, even with higher FC value a significant mismatch is imposed due to the time delay imperfection.

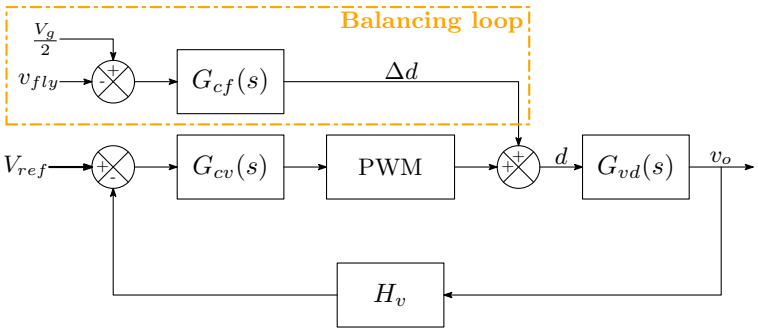


Figure 3-6: Block diagram for the 3LFC voltage control loop with a FC voltage balancing loop employed

3.6 Voltage Mode Control

By adopting the conventional textbook averaging approaches [22, 49], the 3LFC model can be developed under the condition of balanced and constant FC voltage. In the literature, an exact Buck-like dynamics model was developed for the 3LFC under the assumptions of balanced FC voltage and small ripple approximation (SRA) [10, 11]. Accordingly, converter dynamics are independent of the FC under the hypothesis of balanced FC voltage. However, the previous discussions regarding the effects of mismatches point to the need to actively balance the FC voltage [10, 48, 50, 51].

3.6.1 Flying capacitor voltage balancing methodologies under voltage mode control

Originally, the FC voltage was balanced in [1] by employing an extra feedback loop in order to control the FC voltage, as shown in Fig. 3-6. Afterwards, many researchers adopted the same methodology to balance the FC voltage like the work proposed in [10, 50].

Flying capacitor voltage sensing based methodology

The 3LFC has two switching groups as mentioned earlier, hence there are two duty commands D_1 and D_2 associated to the switches A_1 and A_2. The steady state balanced operating point is given at $D_1 = D_2 = M$, where M is the converter voltage conversion ratio. In order to balance the FC voltage in [1], a digital slow integrator based controller is

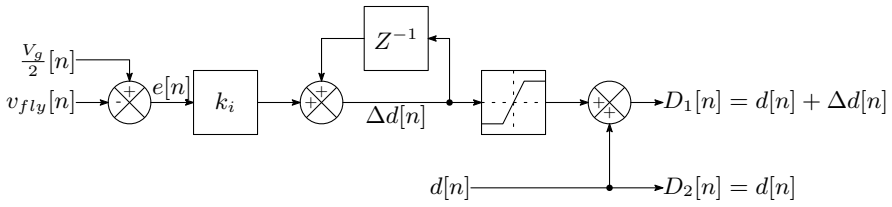


Figure 3-7: The block diagram of the FC voltage sensing based balancing methodology proposed in [1]

implemented as shown in Fig. 3-7. The FC voltage is measured and compared to $\frac{V_g}{2}$, then the error is integrated, and finally the control command is fed forward as a duty correction $\Delta d[n]$ to be added to the gating signal applied to switch A_1. In [10] the authors claim that this balancing technique has a potential instability problem associated with the large inductor current ripple or light load condition. More recently in [50] the author claimed that this instability is PWM carrier dependent. The system with trailing edge carrier modulator is unstable. On contrary, the system operating with dual edge modulator is inherently stable.

The instability problem comes from the fact that there is an inherent feedback action on the FC voltage, imposed by the inductor current dynamics . At certain boundary conditions, defined in [50], and given by

$$I_{crit} = \begin{cases} \frac{V_g}{2L_o f_s}\left(D^2 - \frac{\Delta d}{4}\right) & \text{operating mode } M < 0.5 \\ \frac{V_g}{2L_o f_s}\left[(1-D)^2 - \frac{\Delta d}{4}\right] & \text{operating mode } M > 0.5 \end{cases} \tag{3.15}$$

the FC voltage inherent feedback reverses its sign and generates a positive feedback. However, the 3LFC small-signal model considering the inherent feedback action is still an open research point.

The work presented in [50] shows that, the FC voltage instability is not only due to the inductor current but also relies on the type of the PWM modulator. Since, the instability boundary shown in (3.15) is developed for a system operated with single edge PWM

modulator, then the FC average current under a nonzero duty correction Δd is given by

$$I_{fly} = \begin{cases} I_o - \frac{V_g}{2L_o f_s}\left(D^2 - \frac{\Delta d}{4}\right) & \text{operating mode } M < 0.5 \\ I_o - \frac{V_g}{2L_o f_s}\left[(1-D)^2 - \frac{\Delta d}{4}\right] & \text{operating mode } M > 0.5 \end{cases} \tag{3.16}$$

Otherwise, when a dual edge modulator is used the FC average current is given by,

$$I_{fly} = I_o \Delta d, \tag{3.17}$$

which leads to a unified feedback sign and an inherently stable system. Moreover, the authors in [50], for a digitally controlled converter, proposed an additional digital circuitry with a single edge modulator to partially emulate the operation of the dual edge modulator to achieve the inherent stability and maintain the digital PWM resolution.

Valley current point balancing based methodology

For voltage mode controlled multi-level converter, a technique is proposed in [52] to balance the FC voltage through balancing the inductor current valley points. However, later on, it is claimed in [48, 51] that the valley current point balancing has a stability problem at light load condition. But, the authors in [48, 51] presented a stabilizing technique based on controlling the phase shift between the modulating signals, while the duty commands correction is used to balance the FCs voltages based on the valley current points balancing.

From the author point of view here, using current measurement in a voltage mode controlled system may have no additional advantages except that in a system with higher number of levels, only one parameter should be measured in order to balance the all flying capacitors voltages.

Since the motivation behind this work was developing a space constrained step-down architecture for the automotive application, where the fast transient response and the converter reliability are key features, then a more attention is paid to current programmed controllers. In 2009 valley current mode control is proposed in [5] as an alternative control architecture for the 3LFC with an inherent FC voltage balancing feature. On one hand, the

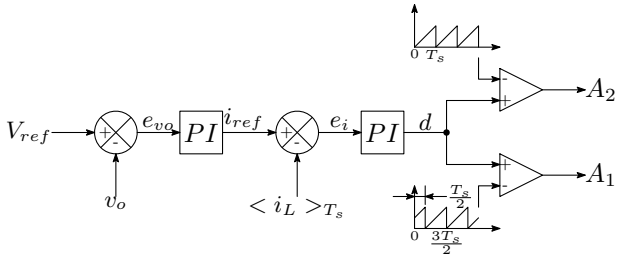
V-CMC introduces an innovative solution combines between fast transient response and the reduced complexity due to inherent balancing. On the other hand, the system lacks the over current protection, the feature which requires an additional hardware complexity to be added to the V-CMC. On contrary, the peak current mode controller has an inherent over-current protection, that is why the P-CMC is preferred in the dc-dc architectures [21], but the P-CMC results to be inherently unstable due to the FC voltage runaway [53].

3.6.2 Flying capacitor voltage balancing methodologies under current mode control

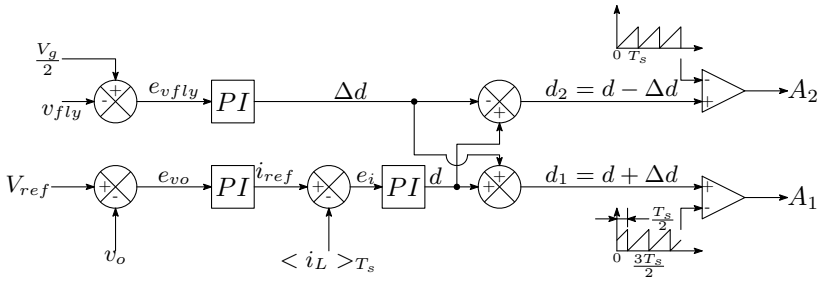
The current mode control of the 3LFC started to be deeply investigated very recently in [27, 28, 53, 54].

Average current mode control

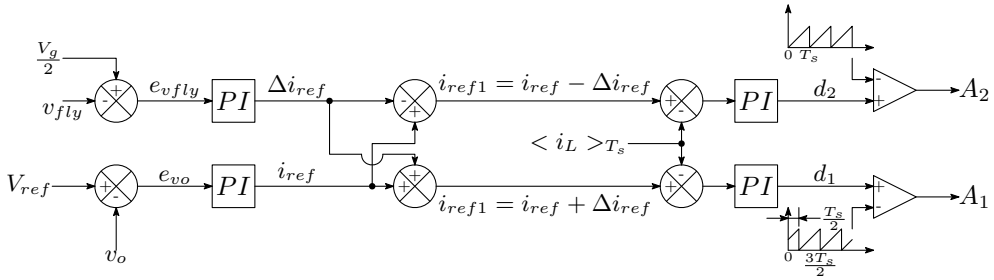
The conventional average current mode controller (A-CMC) for the 3LFC is shown in Fig. 3-8(a). The average current mode control for the 3LFC is firstly proposed in [54]. Two methodologies are investigated in [54] for the sole role of FC voltage balancing under the A-CMC. In the first method, the duty offsetting technique, which was firstly proposed for the voltage mode controlled system, is here adopted to balance the FC voltage in the average current programmed system, as shown in Fig. 3-8(b). On the other hand, in the second technique an asymmetrical offset is imposed on the current reference provided by the outer voltage regulation loop, as shown in Fig. 3-8(c), in order to balance the FC voltage. The asymmetrical corrections within a single switching cycle are equally in the magnitude and opposite in the sign. Since the CMC is used the direct advantage of faster transient response is gained. However, the A-CMC operating with a single edge modulator has the same instability problem associated with the light load condition as the voltage mode controlled converter. The authors in [54] suggested a mode selector monitors the load current to change the feedback sign in order to eliminate the instability problem at the light load conditions. Moreover, as in the voltage controlled system, additional hardware circuitries and control complexity are required to balance the FC voltage in average current controlled



(a) Conventional average current mode controller for the 3LFC without FC voltage balancing



(b) Average current mode controller for the 3LFC with duty offsetting based FC voltage balancing



(c) Average current mode controller for the 3LFC with reference offsetting based FC voltage balancing

Figure 3-8: Average current mode controller of the 3LFC: (a) without balancing, (b) balancing with duty offsetting, and (c) balancing with reference offsetting

architecture. Consequently, the increased complexity and lack of some basic features like over current protection, the average current mode controller architecture contradicts with the target application and basic motivations of this project.

Valley current mode control (V-CMC)

In this type of control the output voltage regulation loop provides the inductor current valley point reference is the valley current mode control (V-CMC) architecture. In the constant frequency V-CMC 3LFC the current reference is fed to be compared with the

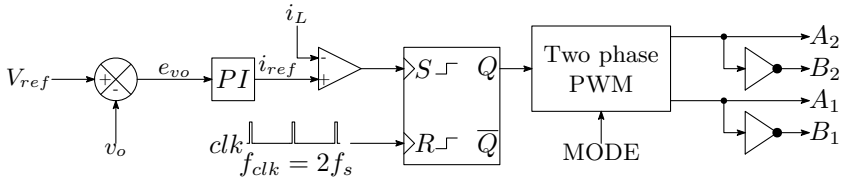


Figure 3-9: Valley current mode controller for 3LFC topology

measured inductor current in order to initiate the inductor current charging phase. On the other hand, the discharging phase is synchronized with a clock has a fixed frequency $f_{clk} = 2f_s$. The control architecture which is proposed in [5] and shown in Fig. 3-9 has a self balanced FC voltage feature. However, the the inherent FC voltage balancing feature of the V-CMC architecture is formally proven in [27,28]. Detailed study of the system stability under V-CMC is reported in the next chapter. The V-CMC converter has many attractive features, like fast transient response and FC voltage self balancing without any additional components, but the system still lacks the increased reliability of the peak current mode controlled system due to the over-current protection feature. The over-current protection can be added to valley current mode control but with additional complexity.

Peak current mode control (P-CMC)

Similarly, the peak current mode control (P-CMC) is implemented like V-CMC system, but with synchronous clock attached to the flip-flop reset input and comparator output connected to set terminal. Hence, in P-CMC inductor discharging phase is triggered by the clock, where the comparator output initiates the charging phase, as shown in Fig. 3-10. The peak-CMC has the advantage of fast transient response and the attractive feature of inherent over current protection, which increases the system reliability. Unfortunately, the P-CMC is inherently unstable if employed in the 3LFC, the property which is recognized in [5,53], and very recently addressed in [53]. In chapter 4 a stability criterion is proposed for the three levels flying capacitor converter under valley and peak current mode control, with a detailed study of the FC voltage runaway phenomenon [27,28]. Moreover, the instability associated with the FC voltage runaway is here addressed with a sensorless stabilizing and balancing technique which is introduced in chapter 5.

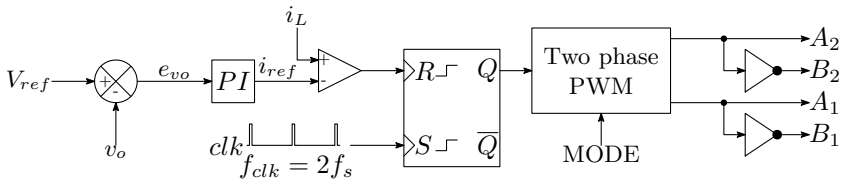


Figure 3-10: Peak current mode controller for 3LFC topology

3.7 Summary

In this chapter, the state-of-the-art of the three-levels flying-capacitor converter is introduced, covering the basic operation and steady-state DC analysis of the converter. In addition to, the literature review of the basic FC voltage balancing methodologies under voltage mode control and current mode control.

Voltage mode controlled systems running with triangular carrier based modulator and employing a FC voltage balancing loop results to be inherently stable. On contrary, using single edge modulators leads to potential instability problems at light loads [50]. Similar instability behavior in average current mode control is recognized in [54] associated with light load conditions. The conclusions in [54] is provided for a system with trailing edge modulator. Otherwise, stability in case of using different carrier type must be separately investigated. So far, the V-CMC is the only control strategy which results to be inherently stable and has an inherent FC voltage balancing feature [5]. For the P-CMC modulator, the system suffers from instability associated with the FC voltage runaway [53].

Chapter 4

Stability Properties of Three-Level Flying-Capacitor Converter Under Valley/Peak-Current-Programmed-Control

4.1 Introduction

One first objective of this chapter is to clarify the basic static stability properties of peak current-mode-control (P-CMC) and valley current-mode-control (V-CMC) when applied to the 3LFC converter, including the formulation of basic criteria for selecting the slope of the compensating ramp [27, 28]. As mentioned earlier, one profound difference of the 3LFC converter with respect to traditional basic topologies is the presence of an additional state variable, i.e. the flying-capacitor (FC) voltage. A second objective of this work is therefore to address the stability properties of the FC voltage of the 3LFC converter when the latter is operated under peak or valley current-mode control [27, 28].

For the purpose of studying the inductor static stability properties and FC voltage stability independently, it will be assumed that the FC voltage dynamics is only weakly coupled with the inductor current control loop. Such hypothesis formally amounts to replace the

FC with a constant voltage source. Consequently, the inductor current waveshape remains triangular. The validity of that basic hypothesis is discussed in the next section.

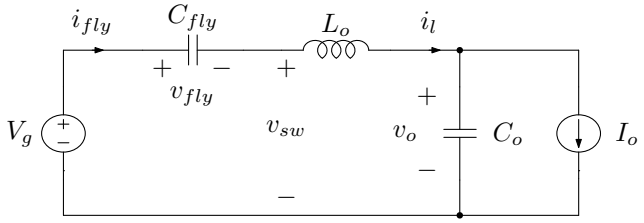
4.2 Discussion on the basic assumption for FC voltage stability analysis

The inductor current time domain exact expressions are developed for the sole role of deriving the sufficient constraint which grantees the validity of the basic assumption. On one hand, the inductor current i_L is independent of the FC during the discharging phase in the operating mode $M < 0.5$. On the other hand, during the charging phase in the operating mode $M > 0.5$, the inductor current is FC independent. Generally, the topological states where the FC affect the inductor current waveform are topological state 1 and 3, which are respectively shown in Fig. 4-1(a) and Fig. 4-1(b). At steady-state balanced condition the inductor current in both topological states is exactly given by

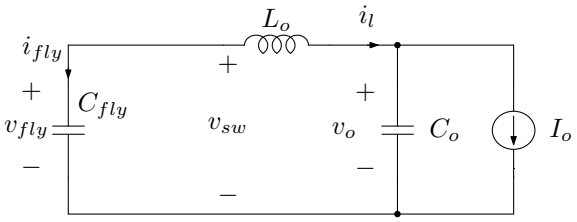
$$i_L(t) = \begin{cases} I_{valley}\cos(\omega_{rfly}t) + \frac{2V_g(0.5-M)+\Delta V_{fly}}{2L_o\omega_{rfly}}\sin(\omega_{rfly}t) & \text{operating mode } M < 0.5 \\ I_{peak}\cos(\omega_{rfly}t) - \frac{2V_g(M-0.5)-\Delta V_{fly}}{2L_o\omega_{rfly}}\sin(\omega_{rfly}t) & \text{operating mode } M > 0.5 \end{cases} \tag{4.1}$$

where I_{valley} and I_{peak} are the inductor current at the valley and peak points respectively, ΔV_{fly} is the peak-to-peak flying capacitor voltage ripple, and ω_{rfly} is the angular resonant frequency of the output inductor and flying capacitor tank network,

$$\omega_{rfly} = \frac{1}{\sqrt{L_o C_{fly}}}. \tag{4.2}$$



(a) Topological state 1



(b) Topological state 3

Figure 4-1: The topological state where the FC affect the inductor current waveforms

Since the converter is operating off-resonant mode, then to a second-order approximation, the above current expression becomes

$$i_L(t) = \begin{cases} I_{valley} + \frac{V_g(0.5-M)}{L_o}t + \underbrace{\frac{\Delta V_{fly}}{2L_o}t - I_{valley}\frac{\omega_{rfly}^2}{2}t^2}_{C_{fly}\text{-dependent terms}} & \text{operating mode } M < 0.5 \\ I_{peak} - \frac{V_g(M-0.5)}{L_o}t + \underbrace{\frac{\Delta V_{fly}}{2L_o}t - I_{peak}\frac{\omega_{rfly}^2}{2}t^2}_{C_{fly}\text{-dependent terms}} & \text{operating mode } M > 0.5 \end{cases} \tag{4.3}$$

The FC can be certainly replaced with a constant source without affecting the analysis, which will be shown later, as long as the C_{fly}-dependent contribution remains negligible with respect to the first-order variation of the current,

$$\left|\frac{\Delta V_{fly}}{2L_o}t - I_{valley}\frac{\omega_{rfly}^2}{2}t^2\right|_{t=DT_s} \ll \frac{V_g(0.5-M)}{L_o}DT_s, \tag{4.4}$$

$$\left|\frac{\Delta V_{fly}}{2L_o}t - I_{peak}\frac{\omega_{rfly}^2}{2}t^2\right|_{t=(1-D)T_s} \ll \frac{V_g(0.5-M)}{L_o}DT_s, \tag{4.5}$$

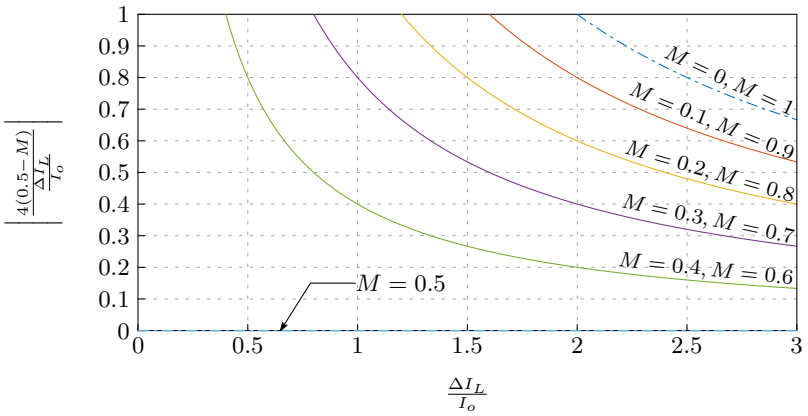


Figure 4-2: Limit expressed by (4.6) (right hand side) versus the normalized inductor peak-to-peak current ripple $\frac{\Delta I_L}{I_o}$ and for various voltage conversion ratios M.

in cases of $M < 0.5$ and $M > 0.5$ respectively. (4.4) and (4.5) both lead to the same constraint which grantees the applicability of the decoupling assumption and given by,

$$\frac{\Delta V_{fly}}{V_g} \ll \left| \frac{4(0.5 - M)}{\frac{\Delta I_L}{I_o}} \right|. \tag{4.6}$$

The inequality (4.6) shows that the normalized flying capacitor voltage ripple $\frac{\Delta V_{fly}}{V_g}$ should be much smaller than the boundary given by the right hand side and graphically represented in Fig. 4-2 to precisely apply the stability criteria proposed in this chapter.

4.3 Static stability

Since the converter has two modes of operation and two modulation schemes are addressed in this stability analysis, then firstly the operating mode $M < 0.5$ is investigated for both valley and peak modulation. Subsequently, the both modulation strategies will be studied in case of operating mode $M > 0.5$.

The subharmonic oscillations boundaries in conventional CMC buck converter are usually derived by studying the effect of a perturbation on the inductor current ($\Delta i_{k+1} = K\Delta i_k$). Stability region is defined as the region where $|K| < 1$, which means that the effect of the perturbation vanishes over time. The same methodology is here adopted for the 3LFC topology under the hypothesis that the FC voltage is balanced, as mentioned earlier.

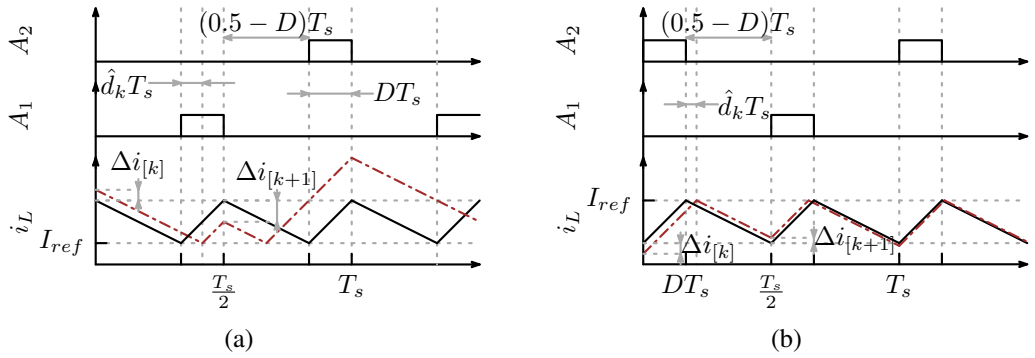


Figure 4-3: Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC in case of $M < 0.5$.

4.3.1 Static stability without slope compensation

Operating mode $M < 0.5$

In V-CMC, the inductor current discharging phase is initiated by a clock with a fixed period equal to $T_s/2$, while the charging phase is determined by the inductor current intersecting the current loop setpoint I_{ref}. On the other hand, for P-CMC, inductor current charging is initiated by a clock with a fixed period equal to $T_s/2$, while the discharging phase is determined by the P-CMC comparator. Steady-state and perturbed current waveforms for the two types of CMC modulation are shown in Fig. 4-3. The inductor current charging and discharging absolute slopes are given by m_{ON} and m_{OFF} respectively,

$$m_{ON,M<0.5} = \frac{(0.5-M)V_g}{L_o}, \tag{4.7}$$

$$m_{OFF,M<0.5} = \frac{MV_g}{L_o}, \tag{4.8}$$

where M is the voltage conversion ratio. Since the FC voltage is assumed balanced and constant, the absolute slopes of the inductor current stay unchanged under current perturbation condition. Hence, the current perturbation at the beginning of the $(k+1)$-th switching cycle is given as a function of the current perturbation at the previous switching cycle k by,

$$\Delta i_{[k+1]}|_{V\text{-}CMC,M<0.5} = -\frac{m_{ON}}{m_{OFF}}\Delta i_{[k]}, \tag{4.9}$$

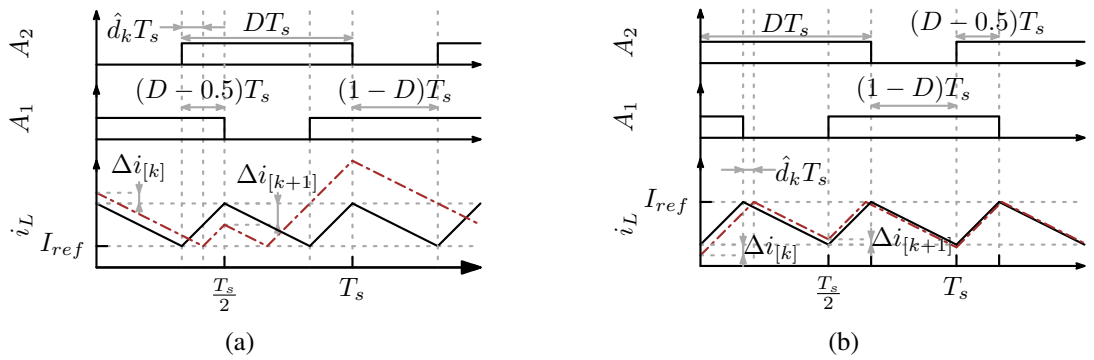


Figure 4-4: Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC in case of $M > 0.5$.

$$\Delta i_{[k+1]}\big|_{\text{P-CMC},M\,<\,0.5} = -\frac{m_{OFF}}{m_{ON}}\Delta i_{[k]}. \tag{4.10}$$

From (4.9) and (4.10), the stability conditions of V-CMC and P-CMC are respectively given by

$$\frac{0.5-M}{M} < 1, \tag{4.11}$$

$$\frac{M}{0.5-M} < 1, \tag{4.12}$$

From (4.11), the V-CMC converter has a static stable region given by

$$0.25 < M < 0.5. \tag{4.13}$$

On the other hand, from (4.12), the region

$$0 < M < 0.25, \tag{4.14}$$

is the static stability region for P-CMC converter.

Operating mode $M > 0.5$

In order to extend the analysis for the whole operating range, the steady state and perturbed waveforms, shown in Fig. 4-4, for the system operating with $M > 0.5$ are considered. The absolute slopes m_{ON} and m_{OFF} in that operating mode are given by

$$m_{ON,M>0.5} = \frac{(1-M)V_g}{L_o}, \tag{4.15}$$

$$m_{OFF,M>0.5} = \frac{(M-0.5)V_g}{L_o}, \tag{4.16}$$

resulting in the static stability conditions of V-CMC and P-CMC converter which are given by

$$\frac{1-M}{M-0.5} < 1 \Leftrightarrow M > \frac{3}{4} \qquad \text{(V-CMC)}, \tag{4.17}$$

$$\frac{M-0.5}{1-M} < 1 \Leftrightarrow M < \frac{3}{4} \qquad \text{(P-CMC)}, \tag{4.18}$$

respectively.

4.3.2 Use of an external ramp

An external ramp can be used to extend the CMC 3LFC converter static stability to the entire operating range $(0 < M < 1)$.

Operating mode $M < 0.5$

For the operating mode $M < 0.5$, the current reference is modified by adding a compensation ramp with an absolute slope S_e as shown in Fig. 4-5. Accordingly, the reference current i_{ref} is given by

$$i_{ref}(t) = \begin{cases} I_{ref} + S_e t & \text{V-CMC} \\ I_{ref} - S_e t & \text{P-CMC} \end{cases} : \text{where } 0 < t < \frac{T_S}{2} \tag{4.19}$$

Subsequently, the quantities I_1, I_2, I_3, and I_4 are respectively given by

$$I_1 = \begin{cases} I_{ref} + S_e(0.5-D)T_s - S_e\hat{d}_{[k]}T_s & \text{V-CMC} \\ I_{ref} - S_eDT_s + S_e\hat{d}_{[k]}T_s & \text{P-CMC} \end{cases} \tag{4.20}$$

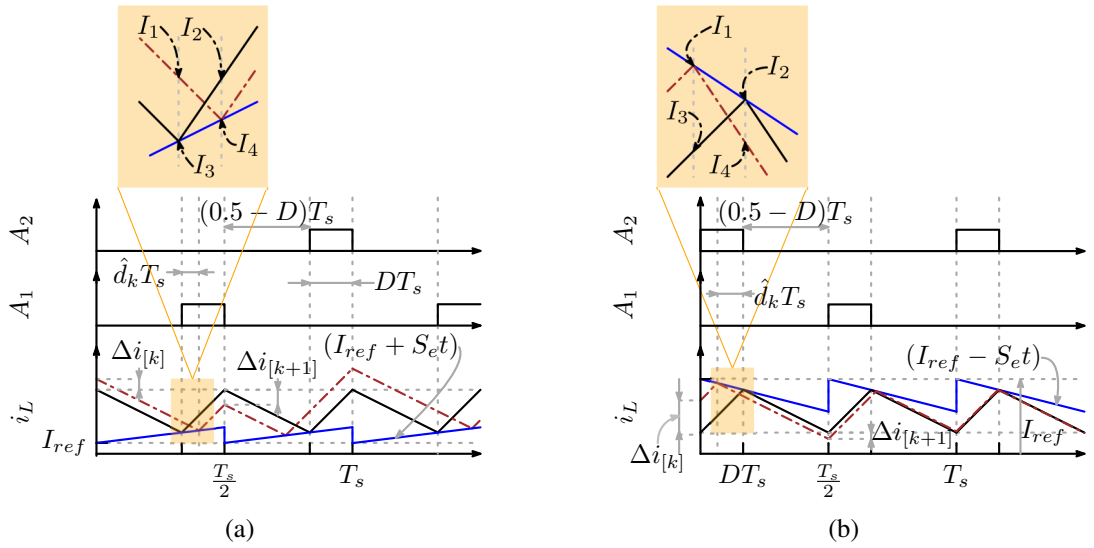


Figure 4-5: Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC including compensation ramp, for $M < 0.5$.

$$I_2 = \begin{cases} I_{ref} + S_e(0.5-D)T_s & \text{V-CMC} \\ I_{ref} - S_e DT_s & \text{P-CMC} \end{cases} \tag{4.21}$$

$$I_3 = \begin{cases} I_{ref} + S_e(0.5-D)T_s + \frac{V_o}{L_o}\hat{d}_{[k]}T_s & \text{V-CMC} \\ I_{ref} - S_e DT_s - \frac{0.5V_g - V_o}{L_o}\hat{d}_{[k]}T_s & \text{P-CMC} \end{cases} \tag{4.22}$$

$$I_4 = \begin{cases} I_{ref} + S_e(0.5-D)T_s + \left(\frac{0.5V_g - V_o}{L_o} - S_e\right)\hat{d}_{[k]}T_s & \text{V-CMC} \\ I_{ref} - S_e DT_s + \left(S_e - \frac{V_o}{L_o}\right)\hat{d}_{[k]}T_s & \text{P-CMC} \end{cases} \tag{4.23}$$

For both modulation strategies the current perturbation in the switching cycle k is given by

$$\Delta i_{[k]}|_{M<0.5} = I_1 - I_3. \tag{4.24}$$

By substituting from (4.20) and (4.22), then the current perturbation $\Delta i_{[k]}$ is given by

$$\Delta i_{[k]}|_{M<0.5} = \begin{cases} -\left(\frac{V_o}{L_o} + S_e\right)\hat{d}_{[k]}T_S & \text{V-CMC} \\ \left(S_e + \frac{0.5V_g - V_o}{L_o}\right)\hat{d}_{[k]}T_S & \text{P-CMC} \end{cases} \tag{4.25}$$

Since the current perturbation in the next cycle $k+1$ is given by

$$\Delta i_{[k+1]}\big|_{M\,<\,0.5} = I_4 - I_2, \tag{4.26}$$

then the current perturbation propagates according to

$$\Delta i_{[k+1]}\big|_{M\,<\,0.5} = \begin{cases} -\frac{0.5-M-\frac{S_eL_o}{V_g}}{M+\frac{S_eL_o}{V_g}}\Delta i_{[k]} & \text{V-CMC} \\ -\frac{M-\frac{S_eL_o}{V_g}}{0.5-M+\frac{S_eL_o}{V_g}}\Delta i_{[k]} & \text{P-CMC} \end{cases} \tag{4.27}$$

From (4.27) the minimal value of compensation ramp slope which satisfies

$$\left|\frac{0.5-M-\frac{S_eL_o}{V_g}}{M+\frac{S_eL_o}{V_g}}\right| < 1, \tag{4.28}$$

and

$$\left|\frac{M-\frac{S_eL_o}{V_g}}{0.5-M+\frac{S_eL_o}{V_g}}\right| < 1, \tag{4.29}$$

for all values of M in the range $0 < M < 0.5$ is given by

$$S_e\big|_{M<0.5} = \frac{V_g}{4L_o}. \tag{4.30}$$

Similarly, the current perturbation propagation equation in the operating mode $M > 0.5$ is derived, considering the waveforms shown in Fig. 4-6, and given by

$$\Delta i_{[k+1]}\big|_{M\,>\,0.5} = \begin{cases} -\frac{1-M-\frac{S_eL_o}{V_g}}{M-0.5+\frac{S_eL_o}{V_g}}\Delta i_{[k]} & \text{V-CMC} \\ -\frac{M-0.5-\frac{S_eL_o}{V_g}}{1-M+\frac{S_eL_o}{V_g}}\Delta i_{[k]} & \text{P-CMC} \end{cases} \tag{4.31}$$

Hence, in presence of the compensation ramp the static stability conditions are given by

$$\left|\frac{1-M-\frac{S_eL_o}{V_g}}{M-0.5+\frac{S_eL_o}{V_g}}\right| < 1 \qquad \text{(V-CMC)} \tag{4.32}$$

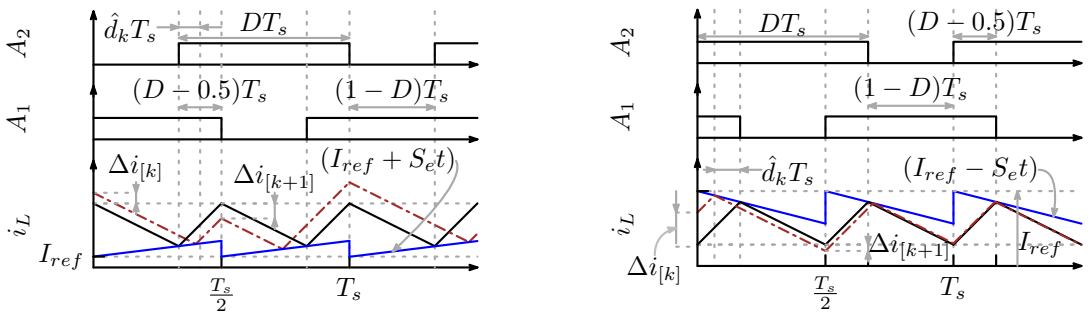


Figure 4-6: Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC including compensation ramp, for $M > 0.5$.

$$\left| \frac{M - 0.5 - \frac{S_e L_o}{V_g}}{1 - M + \frac{S_e L_o}{V_g}} \right| < 1 \qquad \text{(P-CMC)}, \tag{4.33}$$

for V-CMC and P-CMC converters respectively. The minimum value of the compensating ramp which stabilizes the inductor current over the entire operating range $0.5 < M < 1$ is

$$S_e|_{M>0.5} = \frac{V_g}{4L_o} \tag{4.34}$$

for both V-CMC and P-CMC. This is the same result obtained for the $0 < M < 0.5$ case.

4.4 Flying capacitor voltage balancing

Under the basic assumption of the large FC, discussed in section 4.2, the static stability of the current loop is investigated with a constant balanced FC-voltage in the last section. By considering a perturbation $\hat{V}_f$ imposed on the balanced FC voltage $\frac{V_g}{2}$, the FC voltage stability is studied in this section. Firstly, the analysis is proposed for the operating mode $M < 0.5$, afterwards the discussion is extended to the other operating mode with $M > 0.5$.

4.4.1 FC voltage balancing for $M < 0.5$ operating mode

With the FC voltage perturbation the steady-state waveforms of the converter under V-CMC and P-CMC in a such condition are reported in Fig. 4-7. With FC voltage mismatch,

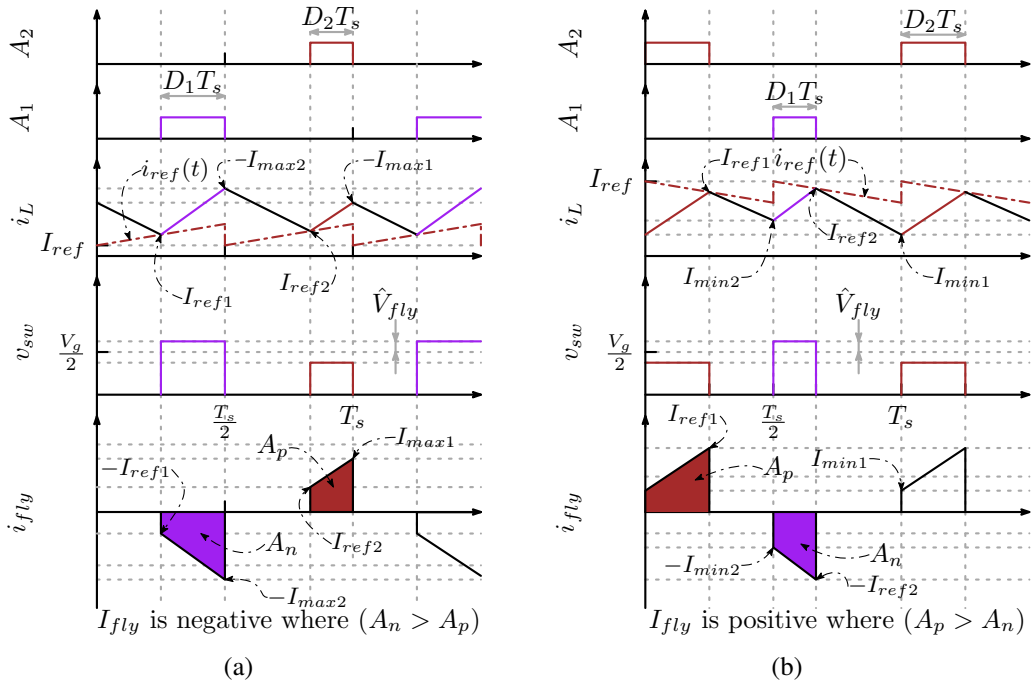


Figure 4-7: Steady-state waveforms of (a) V-CMC and (b) P-CMC including a compensation ramp and considering a small positive perturbation $\hat{V}_f$ in the FC voltage (case $M < 0.5$).

current-programmed control induces two different duty ratios, D_1 and D_2, for the switching groups, which are given by

$$D_1|_{\text{V-CMC, } M<0.5} = M\frac{0.25 - M - \frac{\hat{V}_f}{2V_g} - \frac{S_eL_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 - \frac{S_eL_o}{V_g}}, \tag{4.35}$$

$$D_2|_{\text{V-CMC, } M<0.5} = M\frac{0.25 - M + \frac{\hat{V}_f}{2V_g} - \frac{S_eL_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 - \frac{S_eL_o}{V_g}}, \tag{4.36}$$

$$D_1|_{\text{P-CMC, } M<0.5} = M\frac{0.25 - M - \frac{\hat{V}_f}{2V_g} + \frac{S_eL_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 + \frac{S_eL_o}{V_g}}, \tag{4.37}$$

$$D_2|_{\text{P-CMC, } M<0.5} = M\frac{0.25 - M + \frac{\hat{V}_f}{2V_g} + \frac{S_eL_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 + \frac{S_eL_o}{V_g}}, \tag{4.38}$$

For the purpose of keeping a homogeneous flow of the proposed analysis and not to confuse the reader, a trace for the derivation of the above expressions and the following equations

is provided in Appendix A.

The stability of the FC voltage is here assessed from the sign of the average flying capacitor current I_{fly}: if I_{fly} and $\hat{V}_f$ have the same sign, the FC voltage will further deviate from $V_g/2$, leading to instability. If I_{fly} and $\hat{V}_f$ have opposite sign, the initial unbalance will be compensated and the FC voltage will reach stability at $V_g/2$. The average values of flying capacitor current are given by

$$I_{fly} = \frac{1}{T_s}(A_p - A_n), \tag{4.39}$$

where A_p and A_n are the positive and negative areas under the curve of the flying capacitor current, as shown in Fig. 4-7(a)-(b). Substituting A_p and A_n in (4.39) gives the exact expression of average flying capacitor current (see Appendix A),

$$I_{fly}|_{\text{V-CMC, } M\,<\,0.5} = (D_2 - D_1)\Big[I_{ref} + \frac{MV_g}{4L_o f_s} + \frac{S_e}{2f_s}[1 - (D_1 + D_2)]\Big], \tag{4.40}$$

$$I_{fly}|_{\text{P-CMC, } M\,<\,0.5} = (D_2 - D_1)\Big[I_{ref} - \frac{MV_g}{4L_o f_s} - \frac{S_e(D_1 + D_2)}{2f_s}\Big]. \tag{4.41}$$

For $M < 0.5$ and as long as $\hat{V}_f \ll V_g$, by substituting the values of D_1 and D_2 from (4.35) and (4.36) into (4.40) and from (4.37) and (4.38) into (4.41) expressions of I_{fly} can be approximated as

$$I_{fly}|_{\text{V-CMC},M\,<\,0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}}\left[I_{ref} + \frac{MV_g}{4L_o f_s} + \frac{(0.5 - M)S_e}{f_s}\right], \tag{4.42}$$

$$I_{fly}|_{\text{P-CMC},M\,<\,0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}}\left[I_{ref} - \frac{MV_g}{4L_o f_s} - \frac{MS_e}{f_s}\right]. \tag{4.43}$$

Selecting the compensation ramp slope to be $S_e \geq \frac{V_g}{4L_o}$ makes the sign of the flying capacitor average current dependent on I_{ref}. A more insightful expression is obtained by writing the above results in terms of the load current I_o and the inductor current static ripple ΔI_L

(see Appendix A),

$$I_{fly}|_{\text{V-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}}\left[I_o + \frac{\Delta I_L M}{2(0.5-M)}\right], \tag{4.44}$$

$$I_{fly}|_{\text{P-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}}\left[I_o - \frac{\Delta I_L M}{2(0.5-M)}\right]. \tag{4.45}$$

In the case of V-CMC (4.44), selecting the compensation ramp slope to be $S_e \geq \frac{V_g}{4L_o}$ forces the FC average current to have an opposite sign of the FC voltage perturbation. As a consequence, *V-CMC inherently stabilizes the FC voltage once the subharmonic current oscillation is suppressed*. On the other hand, for P-CMC (4.45), even if $S_e > \frac{V_g}{4L_o}$ the sign of the FC-average-current depends on the inductor current static ripple ΔI_L, which results in an additional condition required to stabilize P-CMC. From (4.45) the FC voltage balancing condition for P-CMC becomes

$$\frac{\Delta I_L}{I_o} > \frac{2(0.5-M)}{M}, \tag{4.46}$$

for the operating mode $M < 0.5$. This result is remarkably different from what obtained for the V-CMC: *in P-CMC the FC voltage is stable only if the relative peak-to-peak inductor current ripple is sufficiently large. The static stability compensation obtained with a compensation ramp does not allow to also stabilize the FC voltage dynamics.*

4.4.2 FC voltage balancing for $M > 0.5$ operating mode

By considering the waveforms shown in Fig. 4-8, and following the same steps shown in the previous section, then the FC voltage stability in the operating mode $M > 0.5$ can be easily investigated.

As mentioned in the previous section valley and peak modulation strategies are inducing different duty commands in presence of a voltage mismatch ($\hat{V}_{fly}$) in the flying capacitor

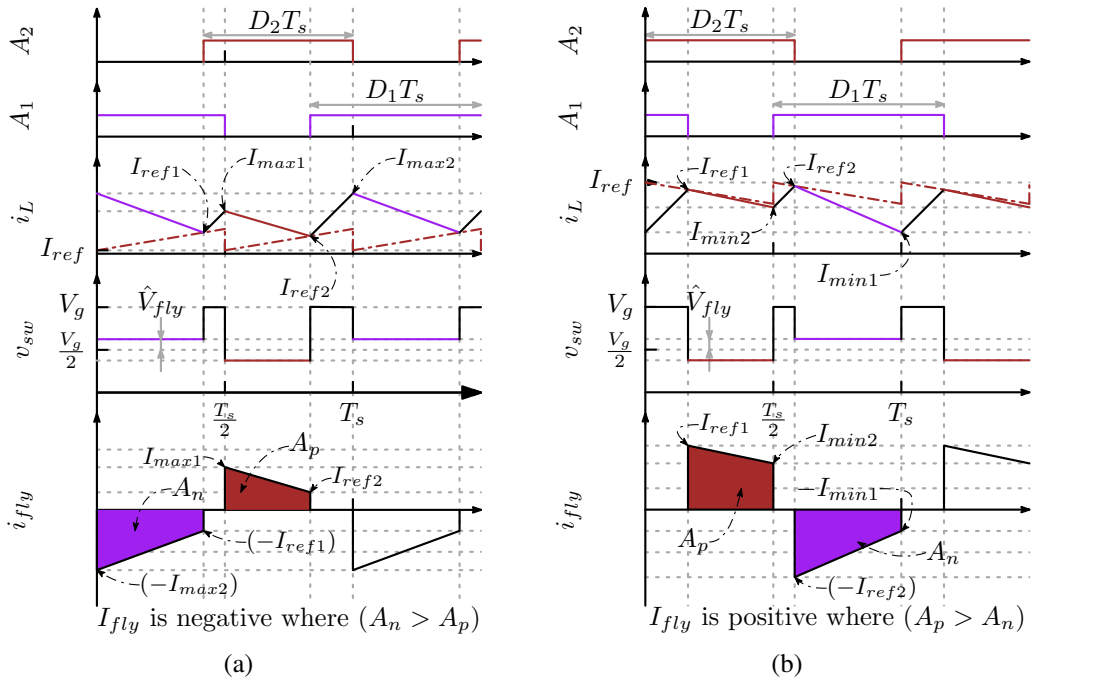


Figure 4-8: Steady-state waveforms of (a) V-CMC and (b) P-CMC including a compensation ramp and considering a small positive perturbation $\hat{V}_f$ in the FC voltage (case $M > 0.5$).

voltage. The different duty commands in this operating mode are given by,

$$D_1|_{\text{V-CMC},M>0.5} = \frac{M\left(0.75 - M - \frac{S_e L_o}{V_g}\right) - \frac{\hat{V}_f}{V_g}\left[0.5(1-M) - \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}, \tag{4.47}$$

$$D_2|_{\text{V-CMC},M>0.5} = \frac{M\left(0.75 - M - \frac{S_e L_o}{V_g}\right) + \frac{\hat{V}_f}{V_g}\left[0.5(1-M) + \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}, \tag{4.48}$$

$$D_1|_{\text{P-CMC},M>0.5} = \frac{M\left(0.75 - M + \frac{S_e L_o}{V_g}\right) - \frac{\hat{V}_f}{V_g}\left[0.5(1-M) - \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}, \tag{4.49}$$

$$D_2|_{\text{P-CMC},M>0.5} = \frac{M\left(0.75 - M + \frac{S_e L_o}{V_g}\right) + \frac{\hat{V}_f}{V_g}\left[0.5(1-M) + \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}, \tag{4.50}$$

resulting in the approximated average flying capacitor currents given by (see Appendix A)

$$I_{fly}|_{\text{V-CMC, } M>0.5} \approx \frac{(1-M)\frac{\hat{V}_{fly}}{V_g}}{0.75 - M - \frac{S_e L_o}{V_g}}\Big[I_o + \frac{(1-M)\Delta I_L}{2(M-0.5)}\Big], \tag{4.51}$$

$$I_{fly}|_{\text{P-CMC, } M>0.5} \approx \frac{(1-M)\frac{\hat{V}_{fly}}{V_g}}{0.75 - M + \frac{S_e L_o}{V_g}}\Big[I_o - \frac{(1-M)\Delta I_L}{2(M-0.5)}\Big]. \tag{4.52}$$

According to (4.52) an additional condition should be fulfilled to stabilize the FC voltage in P-CMC converter,

$$\frac{\Delta I_L}{I_o} > \frac{2(M-0.5)}{1-M}. \tag{4.53}$$

Qualitatively speaking, the situation for $M > 0.5$ does not show major differences with respect to the $M < 0.5$ case. In particular, V-CMC can be fully stabilized with an appropriate choice of the compensation ramp slope. On the other hand, stability of P-CMC is only achieved when the inductor peak-to-peak current ripple is sufficiently large, and the sole static stability compensation obtained with a compensation ramp does not allow to also stabilize the FC voltage dynamics.

4.5 Stability criterion summary

From (4.11), (4.17) and from (4.12) and (4.18), inductor current static stability regions of V-CMC and P-CMC when no compensating ramp is employed are, respectively,

$$(0.25 < M < 0.5) \vee (0.75 < M < 1) \qquad \text{(V-CMC)} \tag{4.54}$$

$$(0 < M < 0.25) \vee (0.5 < M < 0.75) \qquad \text{(P-CMC)} \tag{4.55}$$

From (4.28), (4.29), (4.32), and (4.33) the variation of the minimal value of the normalized compensation ramp slope $S_{nrm,min} = \frac{S_{e,min}}{\frac{V_g}{L_o}}$ required to suppress the current subharmonic oscillations as a function of M is shown in Fig. 4-9. According to the curve shown in Fig. 4-9 the minimal slope required to suppress the current subharmonic oscillations is

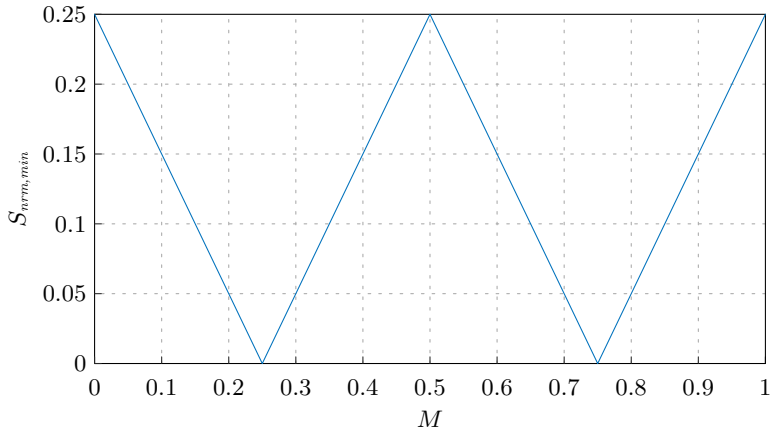


Figure 4-9: Minimal normalized external ramp slope variations with respect to voltage conversion ratio variations for V-CMC and P-CMC

$$S_e|_{minimal} = \frac{V_g}{4L_o}, \tag{4.56}$$

regardless of the operating mode and controller type. The inherent stability of the V-CMC strategy is formally proven by verifying that the current subharmonic oscillation elimination is the sufficient condition which achieves flying capacitor charge balance, assessed from the sign of the approximated average flying capacitor current shown in (4.42), and (4.51). On the other hand, the FC voltage in P-CMC converter will never be balanced unless the converter is operated with relatively high static peak-to-peak inductor current ripple in addition to using a compensation ramp. Hence, the additional condition required to stabilize the P-CMC converter is given by

$$\frac{\Delta I_L}{I_o} > r(M), \tag{4.57}$$

where $r(M)$ is given by

$$r(M) = \begin{cases} \frac{2(0.5-M)}{M} & \text{operating mode } M < 0.5 \\ \frac{2(M-0.5)}{1-M} & \text{operating mode } M > 0.5 \end{cases} \tag{4.58}$$

and defines the minimal current ripple required to stabilize the P-CMC. Fig. 4-10 shows the variation in $r(M)$ with respect to the voltage conversion ratio. Finally, the proposed

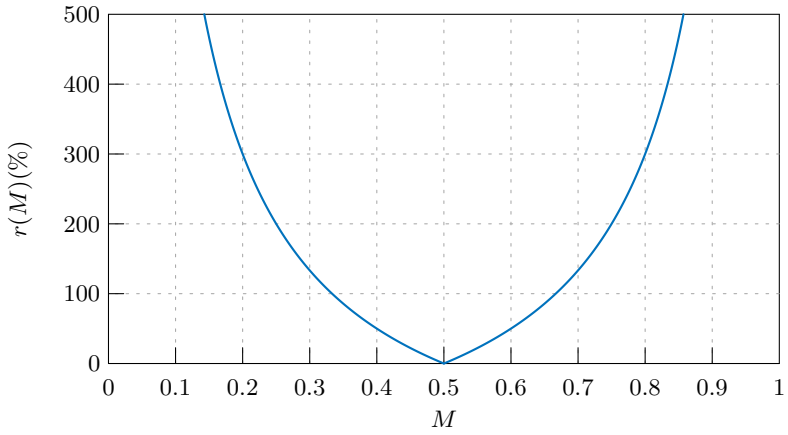


Figure 4-10: Minimum value of the normalized current ripple which achieves FC voltage balancing in P-CMC converter, versus the voltage conversion ratio M.

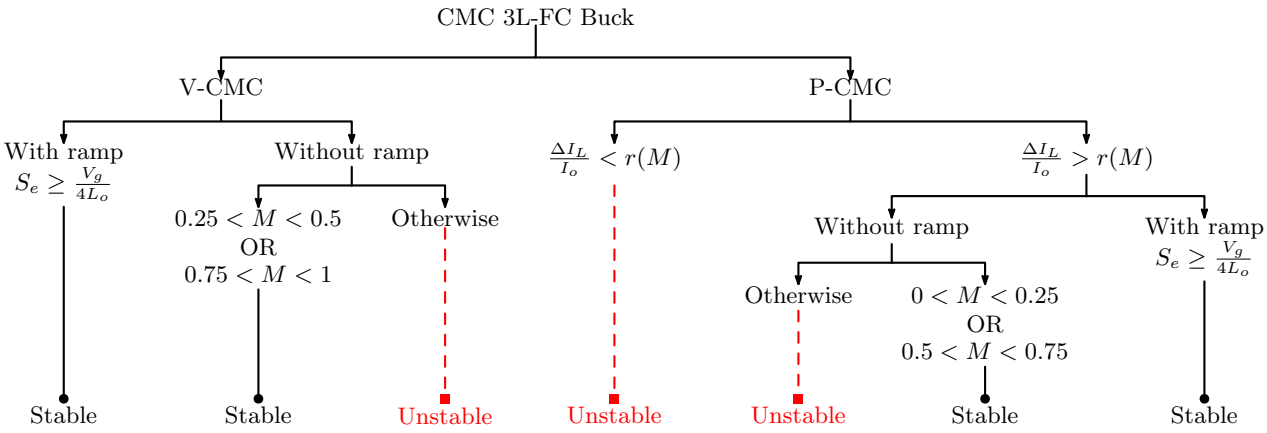


Figure 4-11: Summary of the stability properties of current-mode-controlled three-level flying-capacitor Buck converter.

stability study is summarized graphically in Fig. 4-11.

4.5.1 P-CMC with quasi-square-wave (QSW) operation

By selecting the inductor current static ripple higher than 200% puts the converter in the so called quasi square wave (QSW) operation. The value of the ripple is selected so that the time interval with negative inductor current is long enough to turn-on the upper switches with zero-voltage switching (ZVS). Such operation improves the converter overall efficiency [20]. Excessive increase in the inductor current ripple, however, makes the operation inefficient where the conduction losses become more relevant.

Table 4.1: Simulation and Experimental Setup Parameters

Parameter	Value	Unit
Output voltage (V_o)	3.3	V
Load current (I_o)	500	mA
Operating frequency (f_s)	500	kHz
Flying capacitor (C_{fly})	400	nF
Output inductance test case 1 (L_{o_l})	6.5	µH
Output inductance test case 2 (L_{o_s})	300	nH
Output capacitance (C_o)	10	µF

Based on (4.58) the minimal ripple $r(M)$ required for converter stabilization corresponds to the $0.25 \leq M \leq 0.75$ range is less than the QSW operation boundary $(r(M) < 200\,\%)$. Consequently, whenever the converter voltage conversion ratio lies between 0.25 and 0.75, there is the possibility to design the topology for operation in QSW mode under peak current-mode control. This would retain the basic advantage of P-CMC of inherent over-current protection and would guarantee FC-voltage stability and good efficiency without additional control complexity.

4.6 Simulation Results

A Matlab/Simulink® model is built to verify the proposed analysis according to the parameters shown in Tab. 4.1. Simulations are conducted with the desired peak or valley current-mode controller, and with the voltage loop compensated by a PI controller. Simulation is performed in two steps: first, the converter is simulated with a constant voltage source in place of the flying capacitor. The flying source has voltage $V_{fly} = \frac{V_g}{2}$ to verify the static stability regions of the converter under study. Next the model is simulated using a flying-capacitor to verify the derived FC voltage balancing constraints. Two inductors L_{o_l} and L_{o_s} are considered to simulate two different test cases, which are listed in Tab. 4.1 as test case 1 (low ripple case) and test case 2 (high ripple case) respectively.

Converter under the V-CMC strategy with $M = 0.2$ has static instability according to (4.54), which is verified in Fig. 4-12(a), where the static instability appears in the non-periodic inductor current waveform. On the contrary, P-CMC converter with the same

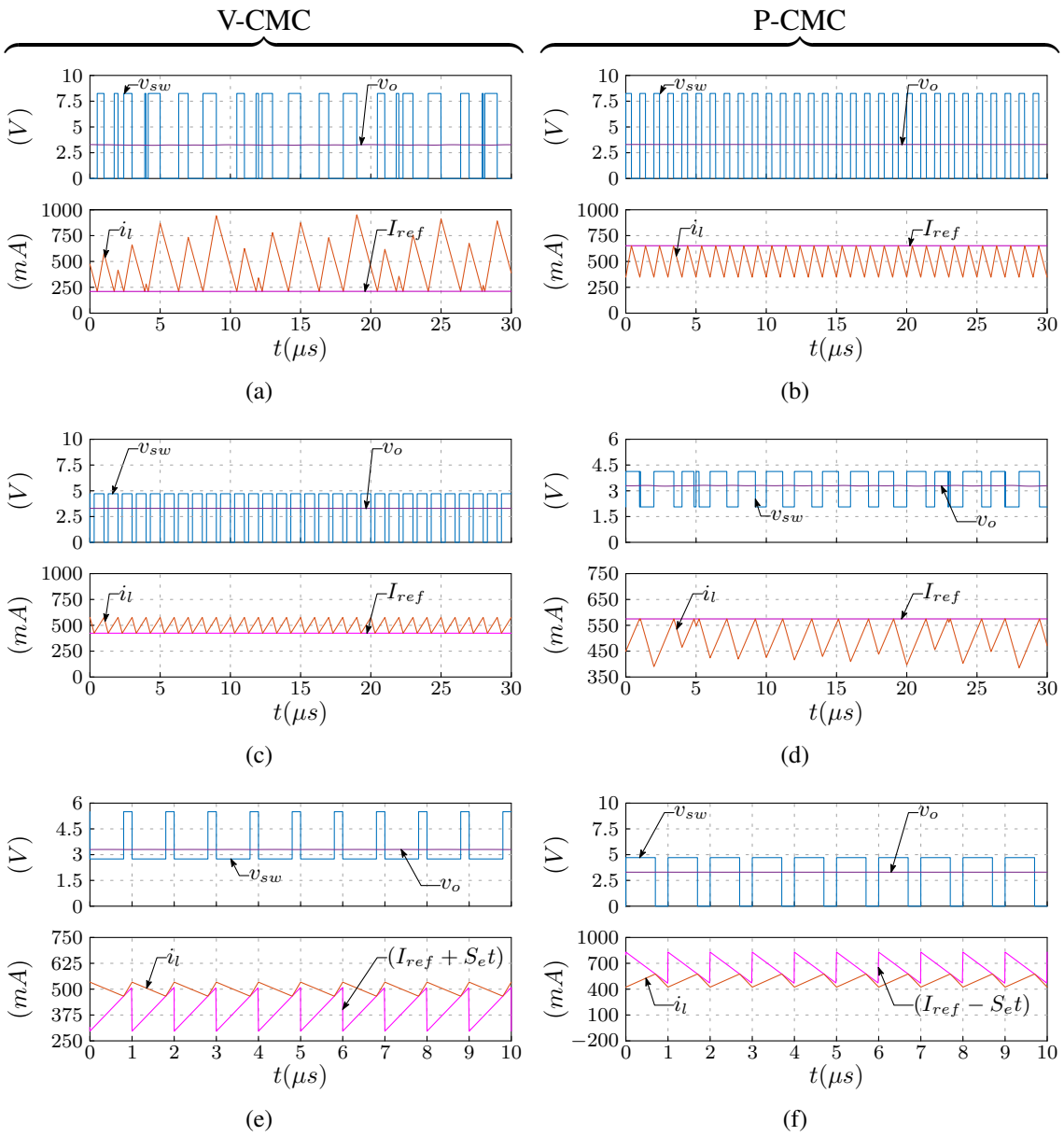


Figure 4-12: Simulation results with a voltage source replacing the flying capacitor: (a) $M = 0.2$ with V-CMC, (b) $M = 0.2$ with P-CMC, (c) $M = 0.35$ with V-CMC, (d) $M = 0.8$ with P-CMC, (e) $M = 0.6$ with V-CMC using ramp compensation ($S_e = 211.54\,\mathrm{mA}/\mu\mathrm{s}$), and (f) $M = 0.35$ with P-CMC using ramp compensation ($S_e = 362.64\,\mathrm{mA}/\mu\mathrm{s}$).

voltage conversion ratio $M = 0.2$ is statically stable as shown in Fig. 4-12(b). On contrary, the periodic current waveforms shown in Fig. 4-12(c) is due to that, the V-CMC without slope compensation is statically stable in the region $0.25 < M = 0.35 < 0.5$ according to (4.54). Moreover, according to (4.55) the uncompensated P-CMC system in the range

$0.75 < M < 1$ is statically unstable, as shown in Fig. 4-12(d).

According to (4.30), in order to suppress the subharmonic oscillation for the case $L_o = 6.5\,\mu\mathrm{H}$ and with $M = 0.6, V_g = 5.5\,\mathrm{V}$ under V-CMC, a compensating ramp slope equal to $211.54\,\mathrm{mA}/\mu\mathrm{s}$ is required. Similarly, with the same inductance but for P-CMC with $M = 0.35, V_g \approx 9.4\,\mathrm{V}$, the compensating ramp slope is $362.64\,\mathrm{mA}/\mu\mathrm{s}$. The proposed equation of the minimal compensation ramp slope (4.30) is verified as shown in the stable periodic inductor current waveforms illustrated in Fig. 4-12(e) and Fig. 4-12(f).

For the following set of the simulation results the flying-source is replaced with a flying-capacitor $C_{fly} = 400\,\mathrm{nF}$ to verify the FC voltage balancing constraints in the converter under study. The system is simulated starting from an initial FC voltage $V_{fly,initial} = (0.5V_g + 0.1)\mathrm{V}$. As proved in the proposed stability study, V-CMC is inherently stable once the current subharmonic oscillations are suppressed, which is verified in Fig. 4-13(a), where the FC voltage is balanced for a ramp compensated converter which has voltage conversion ratio $M = 0.2$. On the other hand, in the case of a converter with the same voltage conversion ratio under P-CMC, which is statically stable, the FC voltage diverges, as shown in Fig. 4-13(b). The output filter inductance $L_o = 6.5\,\mu\mathrm{H}$ in this case (test case 1) gives current ripple factor $\frac{\Delta I_L}{I_o} \approx 0.61$, which leads to unstable operation due to FC voltage runaway phenomenon, which was analytically proven in (4.45) and (4.52). On the other hand, using a relatively small inductance $L_o = 300\,\mathrm{nH}$ gives a high ripple factor $\frac{\Delta I_L}{I_o} \approx 1.32$ (test case 2), resulting in a stable P-CMC converter as shown in Fig. 4-13(c), where the FC voltage is balanced.

4.7 Experimental Results

A $3.3\,\mathrm{V}$, $500\,\mathrm{mA}$, $500\,\mathrm{kHz}$ prototype is built with the parameters shown in Table 4.1. As shown in the simplified block diagram of Fig. 4-14, a mixed-signal solution is implemented in the proof-of-concept prototype for the sole purpose of providing enough flexibility to validate the modulation strategies and operating modes of the converter under study. The output voltage controller is digitally implemented on an FPGA. The digitally generated current reference and compensation ramp are fed to a DAC to generate the current set

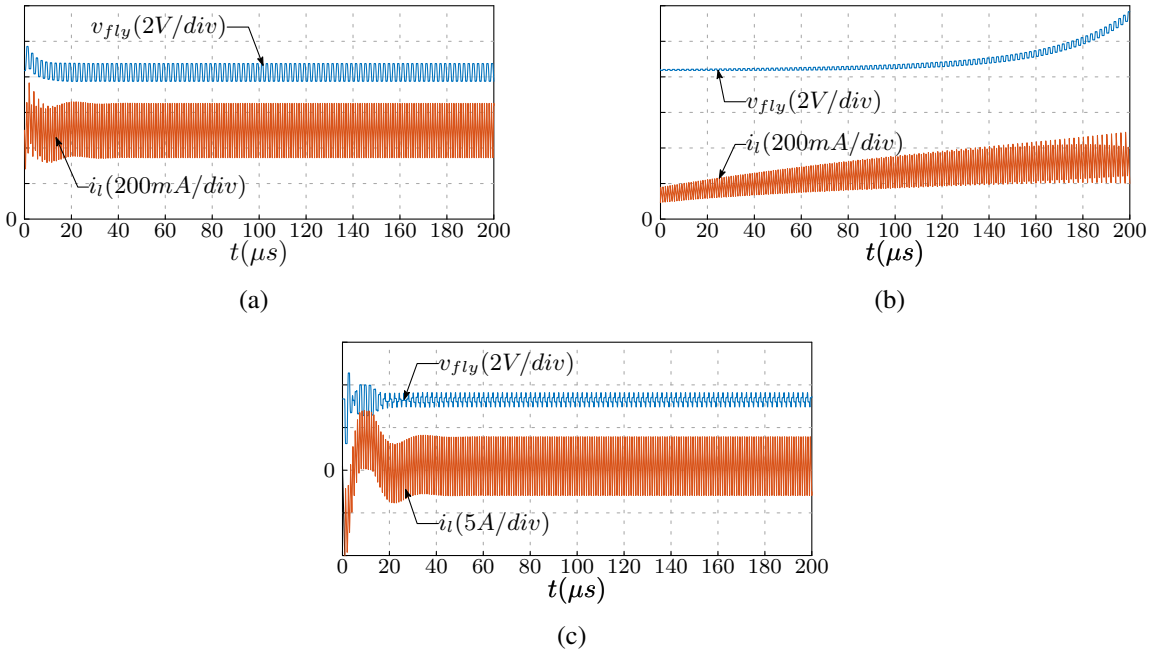


Figure 4-13: Simulation results for a converter operating with a flying capacitor $C_{fly} = 400\,\text{nF}$ and $M = 0.2$: (a) V-CMC, (b) P-CMC with $L_o = 6.5\,\mu\text{H}$, which gives $\frac{\Delta I_L}{I_o} \approx 0.61$ (test case 1), and (c) P-CMC with $L_o = 300\,\text{nH}$, which gives $\frac{\Delta I_L}{I_o} \approx 1.32$ (test case 2).

point which applied to analog comparators. Then, the inductor current intersection trigger signals generated by the analog comparators are fed back to the FPGA. Meanwhile, the trigger signals and internally generated synchronization clock signals in the FPGA are used to generate the interleaving modulating signals.

Two physical inductors L_{o_l} and L_{o_s}, as shown in the experimental prototype photo in Fig. 4-15, with a manual selector are mounted on the PCB to emulate two different test cases, which are listed in Tab. 4.1 as test case 1 (low ripple case) and test case 2 (high ripple case) respectively.

The discrete prototype loop exhibits propagation delays in the order of tens of nanoseconds and associated with power switches turn-on and turn-off times, gate drive IC propagation, digital isolator delay, and analog comparator delay. Hence, the turn-off instant of the switches in case of P-CMC and turn-on instant in case of V-CMC are delayed with respect to the intersection instant between the current reference and inductor current. Such delays, which can be optimized in an integrated solution, by no means prevent a compre-

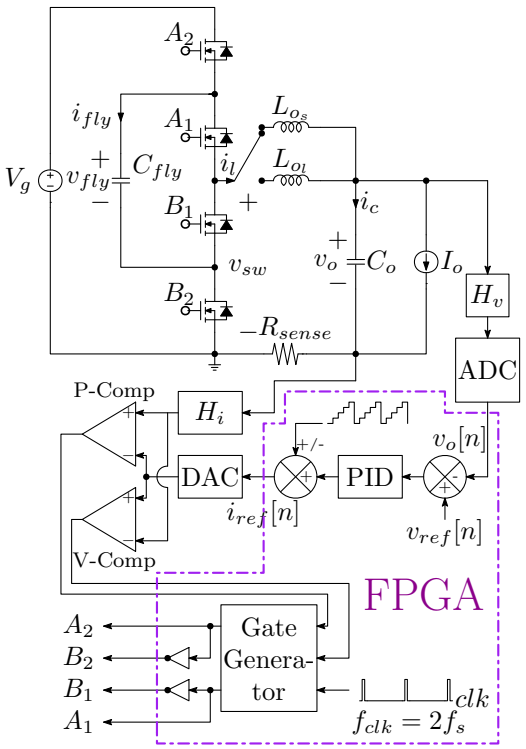


Figure 4-14: Block diagram of the experimental setup.

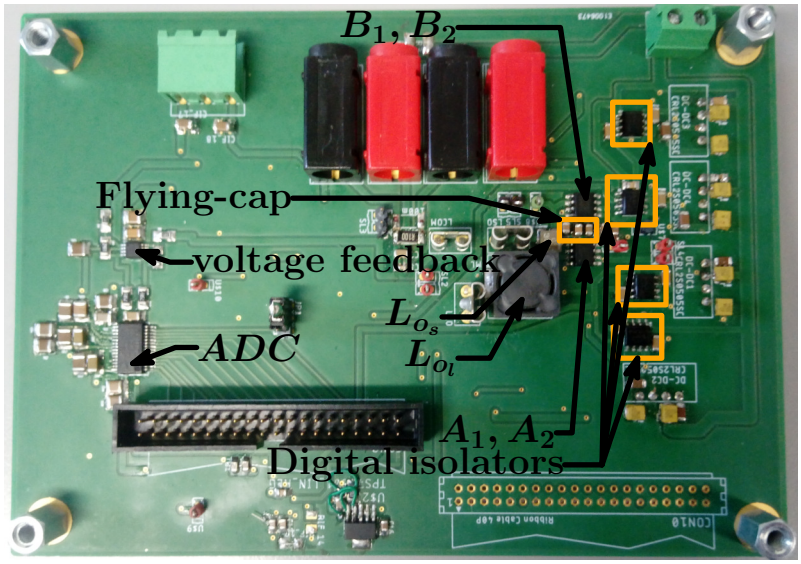


Figure 4-15: Experimental prototype photo.

hensive validation of the main results disclosed in the previous sections. To this end, six test scenarios have been processed in order to experimentally verify the the proposed analysis.

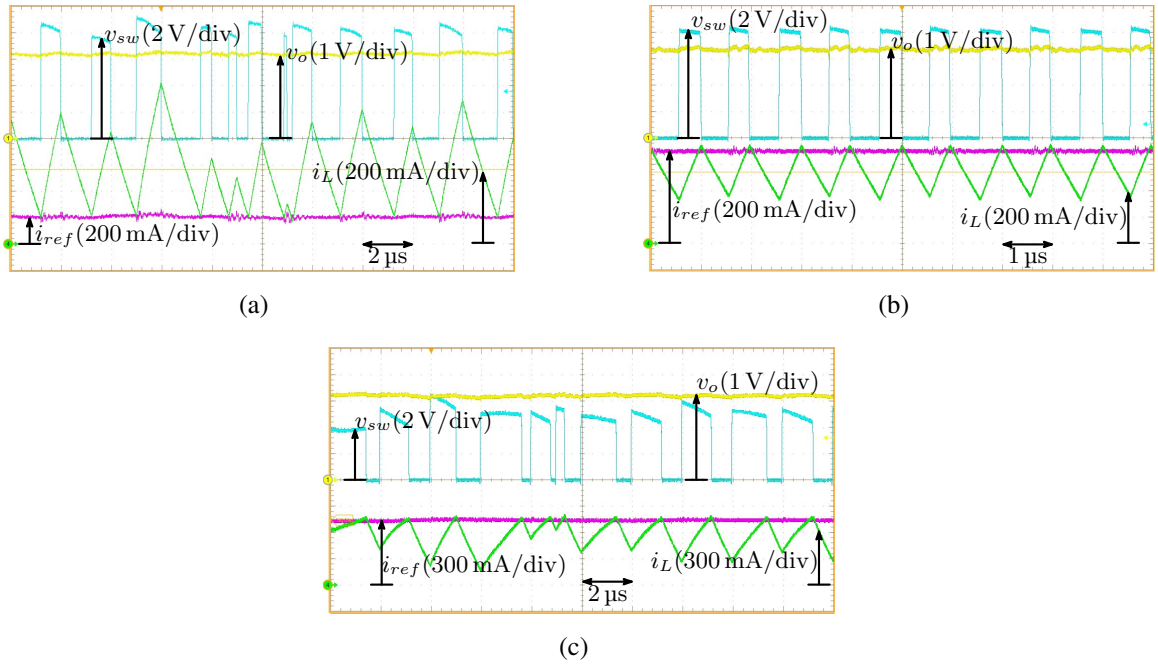


Figure 4-16: Experimental steady-state operation with a constant voltage source replacing the FC: (a) V-CMC and $M = 0.2$, (b) P-CMC and $M = 0.2$, and (c) P-CMC and $M = 0.35$.

4.7.1 Test scenario 1

In this test case the FC is replaced with a constant DC-source imposing a voltage equal to $\frac{V_g}{2}$ in order to verify the developed static stability regions of the converter under study. No compensation ramp is employed in this test case. As shown in Fig. 4-16(a), a converter with $M = 0.2$ under V-CMC has subharmonic oscillation in the output inductor current. On the other hand, control the converter with P-CMC strategy at the same voltage conversion ratio $M = 0.2$ gives stable operation as shown in Fig. 4-16(b). With P-CMC the current becomes statically unstable when $M > 0.25$, as shown in Fig. 4-16(c), where the P-CMC converter is operated at $M = 0.35$.

4.7.2 Test scenario 2

As in the test scenario 1 the FC is still replaced with a constant voltage source. In this case, however, the current loop is compensated using an external ramp superimposed to the current reference. Hence, in this test case the minimal compensation ramp slope required

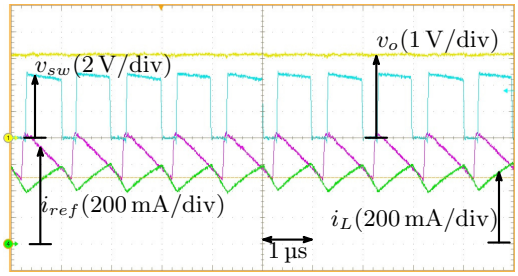


Figure 4-17: Experimental steady-state operation for P-CMC and $M = 0.35$ with a constant voltage source replacing the FC and using a compensating ramp which has slope $S_e = \frac{V_g}{4L_o} \approx 363\,\text{mA}\,\mu\text{s}^{-1}$.

to suppress the current static instability, derived in (4.56), is verified. As shown in Fig. 4-17, the compensated P-CMC converter having $M = 0.35$ is statically stable, where the inductor current is periodic and has ripple frequency $f_{ripple} = 1\,\text{MHz}$, equal to twice the switching rate. The results shown in Fig. 4-17 confirm the validity of (4.56), where the external compensation ramp slope is $S_e = \frac{V_g}{4L_o} \approx 363\,\text{mA}\,\mu\text{s}^{-1}$.

4.7.3 Test scenario 3

In order to verify the FC-voltage stability, the converter is next tested using a flying capacitor $C_{fly} = 400\,\text{nF}$. As proved analytically in the previous sections, the FC-voltage is inherently stable and self balanced in V-CMC converter once the the subharmonic oscillations are suppressed, which is experimentally verified for both operating modes $M < 0.5$ and $M > 0.5$ in Fig. 4-18(a)-4-18(b) respectively.

In order to verify the inherent instability of the FC voltage under P-CMC when the inductor ripple is small, the converter with $M = 0.2$ and $L_o = 6.5\,\mu\text{H}$ is first put in steady-state using a plain voltage-mode controller. Afterwards, the P-CMC controller is enabled and the FC voltage monitored. As soon as the P-CMC controller is enabled, the FC voltage starts to drift away from the steady state value set by the voltage mode control, as shown in Fig. 4-19(a). The phenomenon is highlighted in [53] as FC voltage runaway. Moreover, as shown in Fig. 4-19(b), using a compensation ramp slows down the voltage drifting, but does not eliminate such inherent instability.

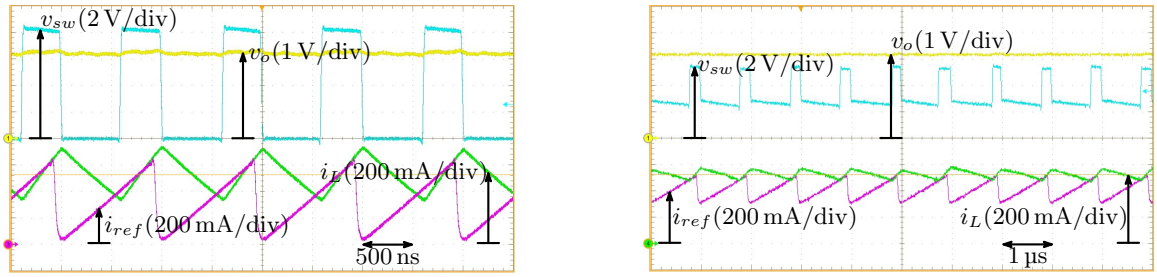


Figure 4-18: Experimental steady-state operation for V-CMC using a compensating ramp and a flying capacitor $C_{fly} = 400\,\text{nF}$: (a) $M = 0.2$ and $S_e = 635\,\text{mA}\,\mu\text{s}^{-1}$ and (b) $M = 0.6$ and $S_e = 215\,\text{mA}\,\mu\text{s}^{-1}$

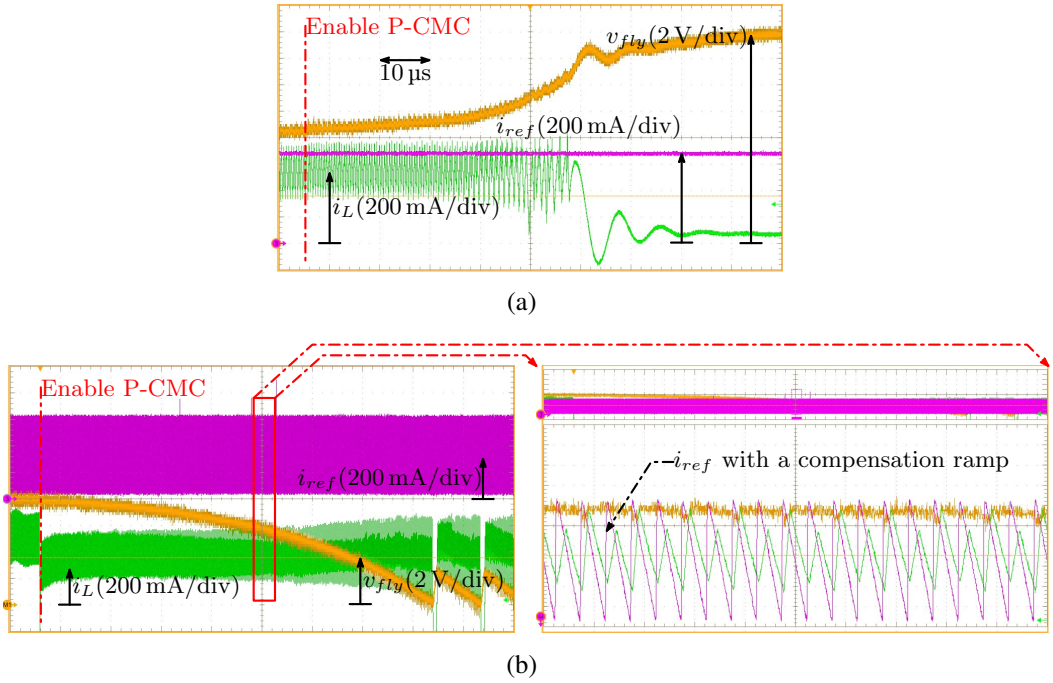


Figure 4-19: Experimental investigation of the inherent instability of P-CMC with small inductor current ripple. $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, output inductance $L_o = 6.5\,\mu\text{H}$, which gives $\frac{\Delta I_L}{I_o} \approx 0.61$ (test case 1). (a) Transition from voltage-mode control to P-CMC with no compensation ramp and (b) transition from voltage-mode control to P-CMC with compensation ramp having slope $S_e = 635\,\text{mA}\,\mu\text{s}^{-1}$.

4.7.4 Test scenario 4

In this test the output inductance is changed to a relatively small value $L_o = 300\,\text{nH}$ in order to verify the FC voltage stability constraint of the converter under P-CMC. Consequently, as

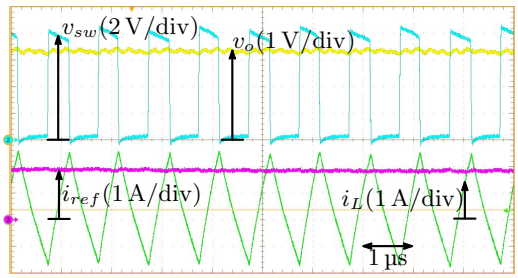


Figure 4-20: Experimental steady-state operation for P-CMC with $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 300\,\text{nH}$, which gives $\frac{\Delta I_L}{I_o} \approx 13.2$ (test case 2).

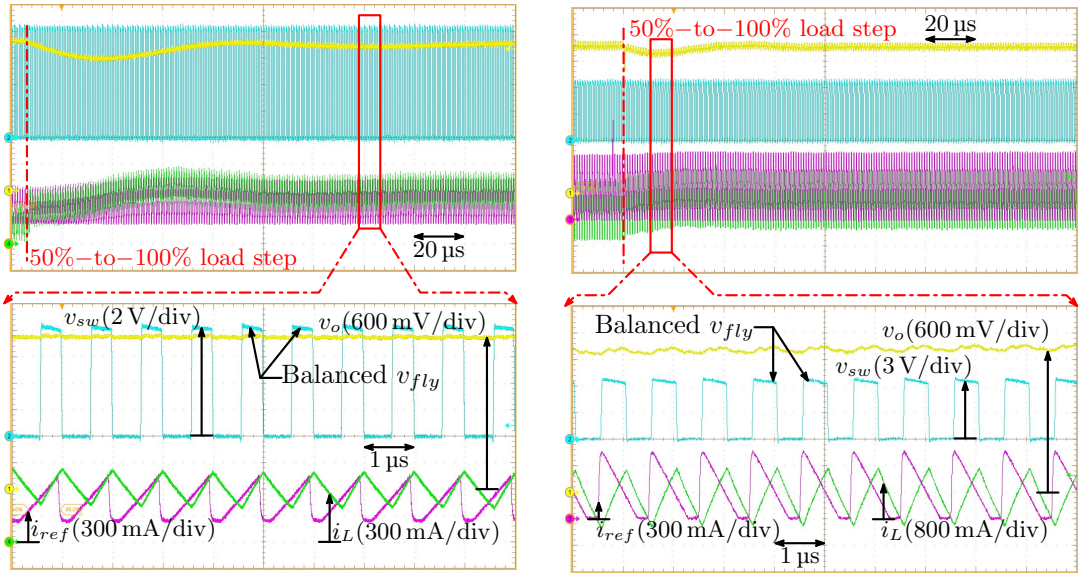
shown in Fig. 4-20, the FC-voltage is stable and self balanced by following the current peak reference in the converter running with large static peak-to-peak ripple factor $\frac{\Delta I_L}{I_o} \approx 13.2$.

4.7.5 Test scenario 5

To further investigate the inherent stability of the V-CMC under load changes, a $50\,\%-\text{to}-100\,\%$ step change in the load current with $L_o = 6.5\,\mu\text{H}$ is considered. The inherent stability of V-CMC under load transient is proven in Fig. 4-21(a), where after a $50\,\%-\text{to}-100\,\%$ load step the FC-voltage is stable and balanced at $\frac{V_g}{2} = 8.25\,\text{V}$ by following the current valley reference.

4.7.6 Test scenario 6

In this final test, the output inductance is changed to $L_o = 1\,\mu\text{H}$ to show the validity of using P-CMC with quasi-square-wave operation. A P-CMC converter is tested under a $50\,\%-\text{to}-100\,\%$ step change in the load current. The converter which has voltage conversion ratio $M = 0.25$ and controlled with P-CMC strategy is stabilized by enabling the converter to work in the QSW operating region as shown in Fig. 4-21(b), where the output inductance $L_o = 1\,\mu\text{H}$ gives current ripple factor $\frac{\Delta I_L}{I_o} = 3$. The stable operation and balanced FC-voltage appears in the periodic inductor current waveform and in the equal peaks of the switching node voltage v_{sw} at $\frac{V_g}{2} = 6.6\,\text{V}$ respectively, after a $50\,\%$-to-$100\,\%$ load transient.



(a) Experimental tests on V-CMC including closed-loop voltage regulation. $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$. Load step change from $I_o = 250\,\text{mA}$ to $I_o = 500\,\text{mA}$

(b) Experimental tests on P-CMC including closed-loop voltage regulation. $M = 0.25$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 1\,\mu\text{H}$. Load step change from $I_o = 250\,\text{mA}$ to $I_o = 500\,\text{mA}$

Figure 4-21: Detrimental tests for test scenarios 5 and 6.

4.8 Summary and Contribution

In this chapter, the stability properties of 3LFC buck converter under valley or peak current-mode control are investigated. The static-stability regions of P-CMC and V-CMC are derived first, and the minimal compensation ramp slope required to statically stabilize the inductor current is calculated. Next, stability of the FC voltage is investigated. For V-CMC, the FC voltage is automatically stabilized once the current subharmonic oscillations are suppressed, a property never formally proven in previous literature. On the other hand, the P-CMC converter suffers from inherent FC voltage instability unless the converter operates with a relatively large inductor current ripple. The proposed stability analysis is verified both via computer simulations and experimentally on a $3.3\,\text{V}$, $500\,\text{mA}$, $500\,\text{kHz}$ prototype.

The proposed stability criterion is developed under a basic assumption that the inductor current stability analysis can be carried out by assuming a *constant* FC voltage, amounts to

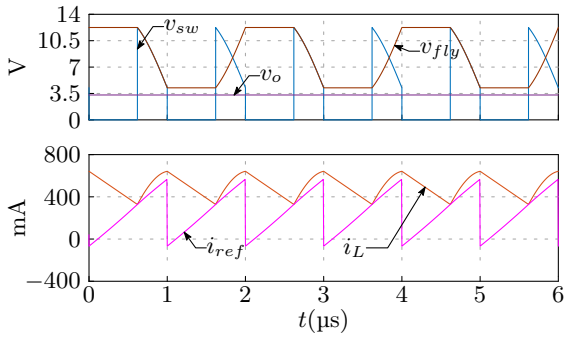


Figure 4-22: Simulation results for V-CMC with $M = 0.2$, $V_g = 16.5\,\mathrm{V}$, $I_o = 500\,\mathrm{mA}$, $\frac{\Delta V_{fly}}{V_g} = 48.5\,\%$, and $\frac{4(0.5-M)}{\frac{\Delta I_L}{I_o}} = 2$. The parameters violate the decoupling condition (4.6).

the requirement that the inductor current waveshape remains triangular. In section 4.2 that basic assumption is discussed in details, and it is concluded that as long as the inequality (4.6) is preserved, the stability criteria proposed in this context can be precisely applied. It is important to recognize, however, that violation of (4.6) does *not* always imply that the basic conclusions of the stability analysis are incorrect. As exemplified in Fig. 4-22, instability in a V-CMC converter with $M = 0.2$ and $\frac{\Delta V_{fly}}{V_g} \approx 48.5\,\%$ is correctly compensated by an external ramp with the minimal slope derived from the proposed analysis. Even though the inductor current is slightly non-triangular, the conclusions of the proposed analysis are still applicable. Overall, it can be argued that (4.6) represents a sufficient, but not always necessary condition for the applicability of the disclosed criterion. More precise considerations, however, would require a quantitative analysis of the system stability in presence of a non-triangular inductor current, a subject outside the scope of the present work.

The proposed stability criterion is firstly proposed in a conference paper [27] with experimental assessment. Afterwards, the experimental verification is extended with additional results for the system with both outer voltage and inner current loops closed under load transient and published in a journal paper [28].

Chapter 5

Sensorless Stabilizing Technique for the Peak-Current-Programmed Control of the 3LFC Topology

5.1 Introduction

Development of a stable peak current programmed control architecture for the 3LFC is necessary for the adoption of that topology in the automotive industry. The stability analysis reported in chapter 4 shows that, the peak current mode control strategy induces different duty cycle commands D_1 and D_2 under FC voltage unbalance condition. The FC-voltage runaway instability behavior is originated from the inherent positive feedback action imposed by the duty cycle imbalance, as analytically proved in chapter 4 [28]. In this chapter, a sensorless stabilizing approach for P-CMC 3LFC converter is proposed. The FC-voltage imbalance is here observed by measuring the duty cycle commands mismatch $D_2 - D_1$. The proposed technique not only eliminates the instability associated with the FC-voltage but offers a self balancing feature.

Two mixed-signal implementation architectures are used to develop the proposed approach. In the first architecture, the sensorless peak offsetting modulation (PO-MOD), the duty cycle commands information available within the digital controller is used to detect

the FC-voltage mismatch. The measured duty cycle error $D_2 - D_1$ is compensated through a digital PI compensator. The PI regulator provides a peak current reference correction δI_{ref}. Afterwards, the original current reference I_{ref}, which is provided by the output voltage regulator, is asymmetrically corrected with δI_{ref} within a signle switching cycle, to provide the current set point $i_{ref,cor}$, as follows,

$$i_{ref,cor}(t)\big|_{M\,<\,0.5} = \begin{cases} I_{ref} - S_e t - \delta I_{ref} & 0 < t < \frac{T_s}{2} \\ I_{ref} - S_e t + \delta I_{ref} & \frac{T_s}{2} < t < T_s \end{cases} \tag{5.1}$$

in the operating mode $M < 0.5$. On the other hand, the current reference in the operating mode $M > 0.5$ is given by

$$i_{ref,cor}(t)\big|_{M\,>\,0.5} = \begin{cases} I_{ref} - S_e t + \delta I_{ref} & 0 < t < \frac{T_s}{2} \\ I_{ref} - S_e t - \delta I_{ref} & \frac{T_s}{2} < t < T_s \end{cases} \tag{5.2}$$

A quite similar architecture is recently proposed in [53]. However, the developed architecture in this dissertation has no additional measurement devices and offers an input voltage independent operation. In addition, the detailed analytical verification of PO-MOD architecture in this context is reported in section 5.3.

Similarly, the sensorless interleaving angle modulation (IA-MOD) architecture adopts the proposed duty cycle difference sensing based approach to eliminate the FC-voltage instability. The IA-MOD architecture utilizes the phase shift between the modulating signals ϕ in order to eliminate the FC voltage instability. Here, the two modulating signals are initially interleaved with $\frac{T_s}{2}$. Then, a correction $-dT_s$ is added to the initial interleaving time, based on the duty cycle error regulation. The methodology provides a stabilization and balancing technique for the FC-voltage. An analytical verification of the developed architecture is reported in section 5.4.

5.2 Proposed Control Approach

As reported in chapter 4, the uncompensated duty cycle commands are different and given by

$$D_1 = \begin{cases} M\dfrac{0.25-M-\frac{\hat{V}_f}{2V_g}+\frac{S_eL_o}{V_g}}{0.25-M-\left(\frac{\hat{V}_{fly}}{V_g}\right)^2+\frac{S_eL_o}{V_g}}, & M<0.5 \\ \dfrac{M\left(0.75-M+\frac{S_eL_o}{V_g}\right)-\frac{\hat{V}_f}{V_g}\left[0.5(1-M)-\frac{\hat{V}_f}{V_g}\right]}{0.75-M+\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}, & M>0.5 \end{cases} \tag{5.3}$$

$$D_2 = \begin{cases} M\dfrac{0.25-M+\frac{\hat{V}_f}{2V_g}+\frac{S_eL_o}{V_g}}{0.25-M-\left(\frac{\hat{V}_{fly}}{V_g}\right)^2+\frac{S_eL_o}{V_g}}, & M<0.5 \\ \dfrac{M\left(0.75-M+\frac{S_eL_o}{V_g}\right)+\frac{\hat{V}_f}{V_g}\left[0.5(1-M)+\frac{\hat{V}_f}{V_g}\right]}{0.75-M+\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}, & M>0.5 \end{cases} \tag{5.4}$$

when the FC-voltage is not balanced at $\frac{V_g}{2}$ in the conventional P-CMC converter. In such condition and under the large FC assumption discussed in Appendix A, the FC average current I_{fly} is given by

$$I_{fly} = \begin{cases} (D_2-D_1)\left[I_o-\frac{MV_g(D_1+D_2)}{4L_of_s}-\left(\frac{S_2}{2f_s}-\frac{MV_g}{2L_of_s}\right)(D_2-D_1)^2\right], & M<0.5 \\ (D_2-D_1)\left[I_o-\dfrac{V_g(1-M)}{2L_of_s}+\dfrac{V_g(1-M)(D_1+D_2)}{4L_of_s}+\right. & \\ \qquad\left.\left(\dfrac{S_e}{2f_s}+\dfrac{V_g(1-M)}{2L_of_s}\right)(D_2-D_1)^2\right]. & M>0.5 \end{cases} \tag{5.5}$$

The FC average current shown above leads to an inherent feedback action which has a sign depends on the inductor current ripple factor $\frac{\Delta I_L}{I_o}$, as shown in (4.45) and (4.52).

The duty cycle commands error $D_{error} = D_2 - D_1$ depends on the FC voltage mismatch. As soon as the FC-voltage mismatch is compensated, the duty cycle commands equalize.

In fact

$$D_{error} = \begin{cases} \dfrac{M\frac{\hat{V}_f}{V_g}}{0.25-M-\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_e L_o}{V_g}} & M < 0.5 \\ \\ \dfrac{(1-M)\frac{\hat{V}_f}{V_g}}{0.75-M+\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_e L_o}{V_g}} & M > 0.5 \end{cases}, \tag{5.6}$$

Therefore, the duty cycle error D_{error} is here calculated in order to observe the FC-voltage mismatch $\hat{V}_f$. Consequently, the proposed sensorless stabilizing and balancing approach relies on employing an extra control loop to regulate the duty cycle commands error. As consequence of duty error regulation the inherent negative feedback action is compensated. Moreover, as a consequence of forcing the duty cycle commands error to zero the FC voltage imbalance is compensated and FC voltage is balanced at $\frac{V_g}{2}$. Finally, according to (5.6) the converter steady state operating point is $D_1 = D_2 = M$, $v_f = \frac{V_g}{2}$, $I_{fly} = 0$, and stabilizing controller output is zero.

Two different implementation methodologies are proposed in order to integrate the proposed control approach within the conventional P-CMC loop. The sensorless peak offsetting modulation (PO-MOD) architecture which utilizes a current reference correction, is the first implementation. On the other hand, the second implementation, sensorless interleaving angle modulation (IA-MOD), controls the the interleaving angle between the two modulation signals. The two proposed methodologies PO-MOD and IA-MOD block diagrams are respectively shown in Fig. 5-1 and Fig. 5-2.

5.3 Sensorless peak offsetting modulation

According to the block diagram of the PO-MOD architecture shown in Fig. 5-1, the duty cycle values of the modulating signals A_1 and A_2 are monitored and the duty cycle error is calculated. The measured error is fed to a PI-compensator which provides the current reference correction δI_{ref}. The current reference correction is imposed according to the active switches states, as shown in (5.1) and (5.2). By adopting the same methodology in [28], considering the converter waveforms shown in Fig. 5-3 the current reference correction in

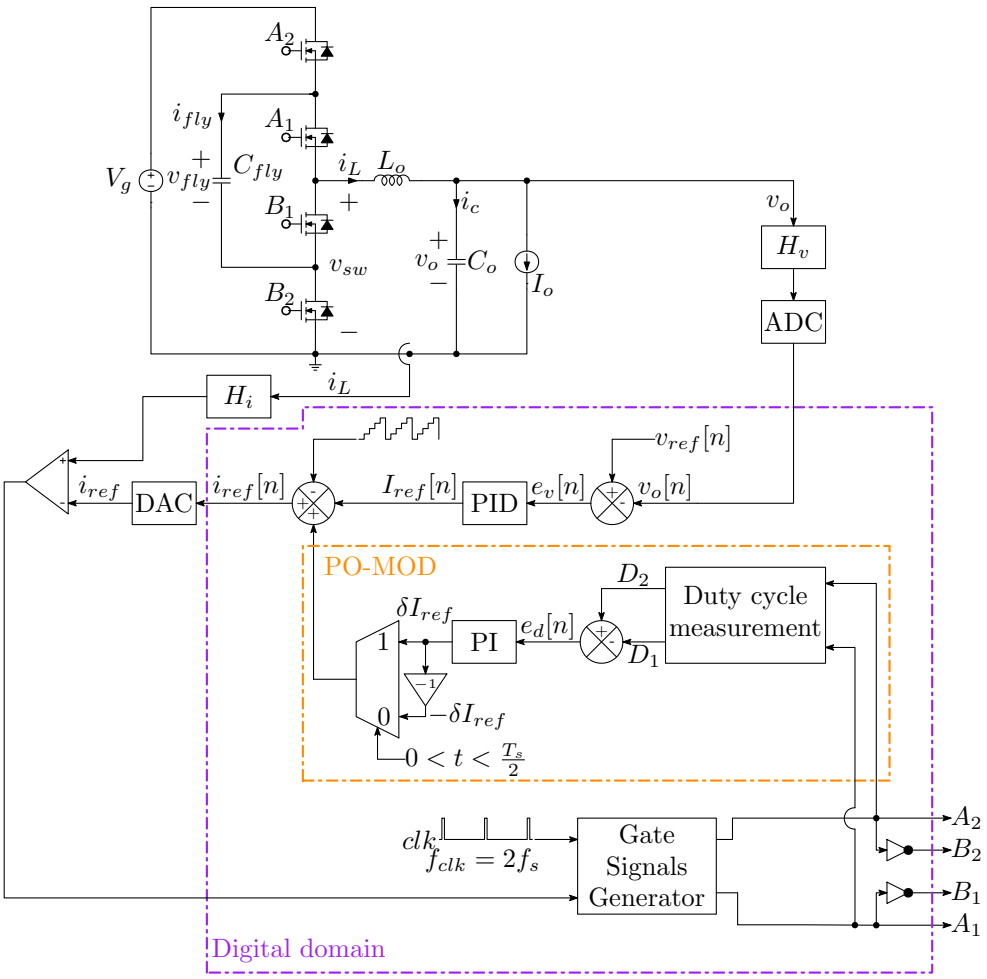


Figure 5-1: Sensorless peak offsetting (PO-MOD) based implementation

the PO-MOD architecture has an impact on the duty cycle commands given by

$$D_1 = \begin{cases} D_{1,\,\text{uncompensated}} + \underbrace{\dfrac{\frac{2\delta I_{ref} L_o f_s}{V_g}(0.5 - \frac{\hat{V}_f}{V_g})}{0.25 - M - \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}}_{\text{peak offsetting modulation effect}} & M < 0.5 \\ D_{1,\,\text{uncompensated}} + \underbrace{\dfrac{\frac{2\delta I_{ref} L_o f_s}{V_g}\left(0.5 - \frac{\hat{V}_f}{V_g}\right)}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}}_{\text{peak offsetting modulation effect}} & M > 0.5 \end{cases}, \tag{5.7}$$

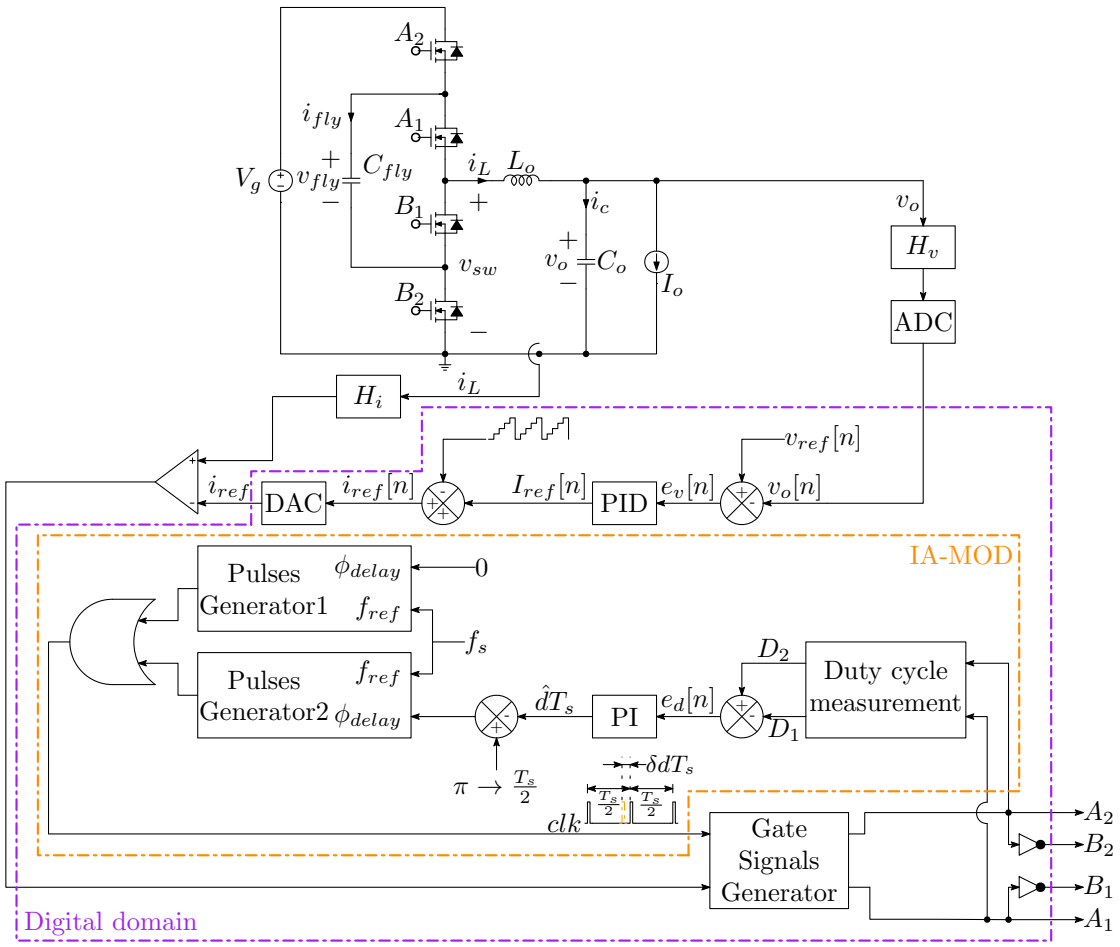


Figure 5-2: Sensorless interleaving angle modulation (IA-MOD) based implementation

$$D_2 = \begin{cases} D_{2,\,uncompensated} + \underbrace{\dfrac{-\frac{2\delta I_{ref} L_o f_s}{V_g}\left(0.5+\frac{\hat{V}_f}{V_g}\right)}{0.25 - M - \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}}_{\text{peak offsetting modulation effect}} & M < 0.5 \\ D_{2,\,uncompensated} + \underbrace{\dfrac{-\frac{2\delta I_{ref} L_o f_s}{V_g}\left(0.5+\frac{\hat{V}_f}{V_g}\right)}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}}_{\text{peak offsetting modulation effect}} & M > 0.5 \end{cases}, \tag{5.8}$$

where $D_{1,\,uncompensated}$ and $D_{2,\,uncompensated}$ are the expressions of the uncompensated duty cycle commands in (5.3) and (5.4). For the FC average current, the peak offsetting modulation

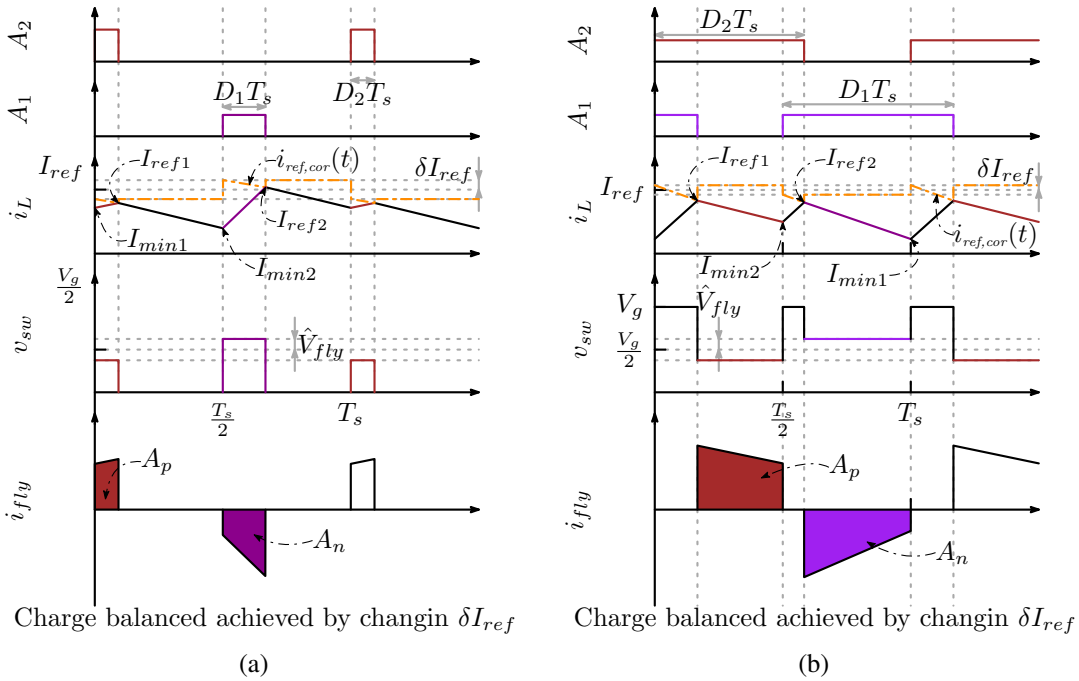


Figure 5-3: Steady-state waveforms of P-CMC including a compensation ramp and considering a small positive perturbation $\hat{V}_f$ in the FC voltage using peak offsetting modulation (PO-MOD) method: (a) $M < 0.5$, (b) $M > 0.5$.

results in a FC average current equals to

$$I_{fly} = \begin{cases} (D_2 - D_1)\Big[I_o - \dfrac{V_o(D_1+D_2)}{4L_of_s} - \dfrac{S_eL_o - MV_g}{2L_of_s}(D_2 - D_1)^2 \\ \qquad\qquad -\delta I_{ref}(D_2 - D_1)\Big], & M < 0.5 \\ (D_2 - D_1)\Big[I_o - \dfrac{V_g(1-M)}{2L_of_s} + \dfrac{V_g(1-M)(D_1+D_2)}{4L_of_s} + \\ \quad \left(\dfrac{S_e}{2f_s} + \dfrac{V_g(1-M)}{2L_of_s}\right)(D_2 - D_1)^2 + \delta I_{ref}(D_2 - D_1)\Big], & M > 0.5 \end{cases} \tag{5.9}$$

In order to obtain a clear conclusion about the effect of the peak offsetting on the the FC voltage stability, the values of D_{1f} and D_{2f} in (5.9) are replaced with the values shown in (5.7) and (5.8). The expression of I_{fly} is then linearized under the assumption of small signal variations $\hat{V}_f \ll \frac{V_g}{2}$ and $\delta I_{ref} \ll I_{ref}$. Then, the FC average current is approximately

given by

$$I_{fly} \approx \begin{cases} \underbrace{\dfrac{M\frac{\hat{V}_f}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}}\left[I_o - \dfrac{\Delta I_L M}{2(0.5-M)}\right]}_{\text{uncompensated current}} + \\ \underbrace{\dfrac{-2\delta I_{ref} L_o f_s}{V_g\left(0.25 - M + \frac{S_e L_o}{V_g}\right)}\left[I_o - \dfrac{\Delta I_L M}{2(0.5-M)}\right]}_{\text{PO-MOD correction}} & M < 0.5 \\ \\ \underbrace{\dfrac{(1-M)\frac{\hat{V}_{fly}}{V_g}}{0.75 - M + \frac{S_e L_o}{V_g}}\left[I_o - \dfrac{(1-M)\Delta I_L}{2(M-0.5)}\right]}_{\text{uncompensated current}} + \\ \underbrace{\dfrac{-2\delta I_{ref} L_o f_s}{V_g\left(0.75 - M + \frac{S_e L_o}{V_g}\right)}\left[I_o - \dfrac{(1-M)\Delta I_L}{2(M-0.5)}\right]}_{\text{PO-MOD correction}} & M > 0.5 \end{cases} \tag{5.10}$$

As shown in (5.10), the FC average current is partially equal to the value which is imposed by the conventional P-CMC and reported in (4.45) and (4.52). In addition to the contribution of the employed stabilizing controller. The same stability criterion in chapter 4 is here adopted to study the FC voltage stability under PO-MOD. The system with PO-MOD is stable if and only if the PO-MOD is capable of producing a FC average current with an opposite sign with respect to the initial FC voltage perturbation in all operating conditions. As shown in (5.10), the sign of the FC average current is imposed by a term which has sign depends on controller output δI_{ref} and the inductor current ripple. Accordingly, the behavior of the employed stabilizing controller must be studied under the conditions

$$\frac{\Delta I_L}{I_o} < r(M), \tag{5.11}$$

and

$$\frac{\Delta I_L}{I_o} > r(M), \tag{5.12}$$

where $r(M)$ is the same function defined in (4.58) and given by

$$r(M) = \begin{cases} \dfrac{2(0.5-M)}{M} & \text{operating mode } M < 0.5 \\ \\ \dfrac{2(M-0.5)}{1-M} & \text{operating mode } M > 0.5 \end{cases} . \tag{5.13}$$

In practice inequality (5.11) represents a heavy load conditions, where the light load and no load conditions are represented by (5.12). In order to study stability in all operating condition, firstly the FC average current expression is represented as a function of the stabilizing loop error D_{error} as

$$I_{fly} \approx \begin{cases} D_{error}\left[I_o - \dfrac{\Delta I_L M}{2(0.5-M)}\right] & M < 0.5 \\ \\ D_{error}\left[I_o - \dfrac{(1-M)\Delta I_L}{2(M-0.5)}\right] & M > 0.5 \end{cases} , \tag{5.14}$$

where D_{error} is the value of $D_2 - D_1$ which is given by

$$D_{error} = \begin{cases} \dfrac{M\frac{\hat{V}_f}{V_g} - 2\delta I_{ref} L_o f_s}{V_g\left(0.25 - M + \frac{S_e L_o}{V_g}\right)} & M < 0.5 \\ \\ \dfrac{(1-M)\hat{V}_f - 2\delta I_{ref} L_o f_s}{V_g\left(0.75 - M + \frac{S_e L_o}{V_g}\right)} & M > 0.5 \end{cases} , \tag{5.15}$$

under the small signal assumption.

Now hypothetical conditions are considered for the sole purpose of studying the system stability in all operating conditions. Firstly, a condition is assumed where a converter initially has a positive FC voltage perturbation, small inductor current ripple which means the inequality (5.11) is true, and a positive FC average current. Accordingly, the duty cycle error D_{error} is certainly positive. Subsequently, the PO-MOD controller shown in Fig. 5-1 acts by increasing δI_{ref} in order to compensate the positive error in the duty cycle

command. The reduction in the duty cycle error D_{error} according to control action results in I_{fly} reduction. Under such condition the controller keeps increasing δI_{ref} until the duty cycle difference D_{error} reverses sign. As a consequence of D_{error} sign reversal, the FC average current reverses sign and $\hat{V}_f$ starts decreasing. Afterwards, with a negative D_{error} the PO-MOD controller starts to decrease δI_{ref} in order to compensate the negative error. The action which decreases I_{fly} respectively. The aforementioned behavior is repeated until steady state condition $D_{error} = 0$, $I_{fly} = 0$, and $\hat{V}_f = 0$. Such control action is an inherent negative feedback on the FC voltage.

In the second case, the same hypothetical condition shown above is considered but with large inductor current ripple, which means the inequality (5.12) is true. Here, the ΔI_L dependent term is always negative. Accordingly, in case the converter has positive I_{fly} the duty cycle error D_{error} is certainly negative according to (5.14). The controller responds in such condition by reducing the control command δI_{ref} until the duty cycle error reverses sign according to (5.15). Since the duty cycle error sign is reversed the FC average current is negative and FC voltage perturbation decreases.

To that end, and according to (5.14) and (5.12) the proposed PO-MOD eliminates the instability associated with FC voltage runaway by imposing an inherent negative feedback action on the FC voltage in all operating conditions.

5.4 Interleaving angle modulation

In this technique the interleaving angle between the the modulating signals rising edges is controlled, as shown in Fig. 5-2, in order to stabilize the system. A correction $-dT_s$ is imposed on the nominal interleaving value $\frac{T_s}{2}$, as shown in the waveforms in Fig. 5-4. Under the FC voltage mismatch condition and using the interleaving angle modulation, the duty cycle commands are given by

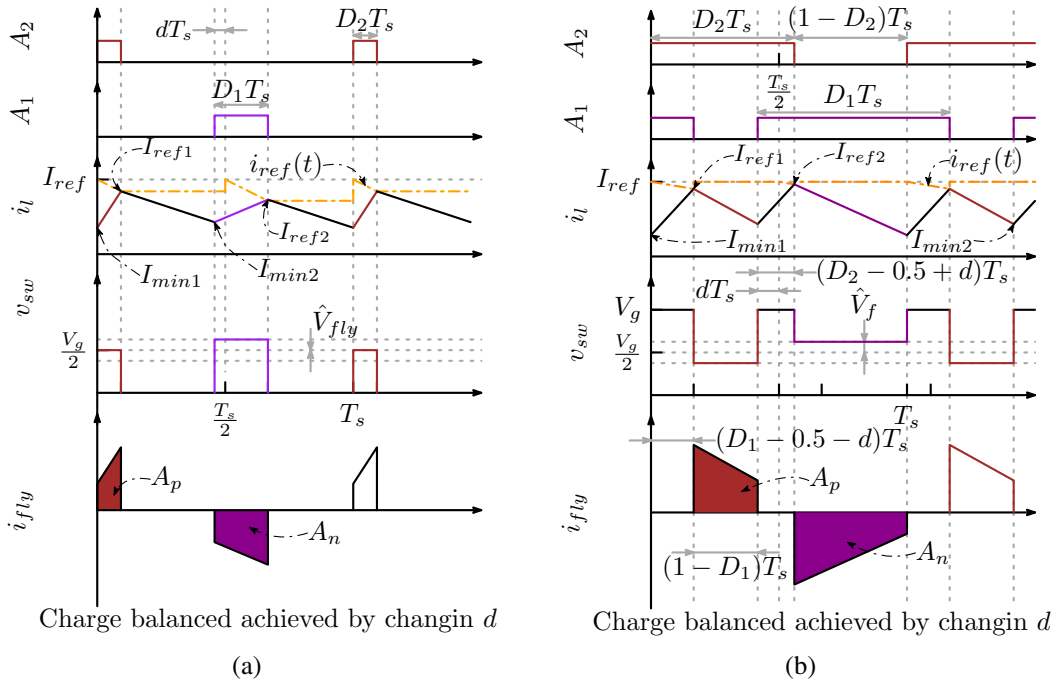


Figure 5-4: Steady-state waveforms of P-CMC including a compensation ramp and considering a small positive perturbation $\hat{V}_f$ in the FC voltage using interleaving angle modulation (IA-MOD) method: (a) $M < 0.5$, (b) $M > 0.5$.

$$D_1 = \begin{cases} D_{1,\,\text{uncompensated}} + \underbrace{\dfrac{d\left(0.5-\frac{\hat{V}_f}{V_g}\right)\left(\frac{S_eL_o}{V_g}-M\right)}{0.25-M-\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}}_{\text{angle modulation effect}} & M<0.5 \\ D_{1,\,\text{uncompensated}} + \underbrace{\dfrac{d\left(0.5-\frac{\hat{V}_f}{V_g}\right)\left(1-M+\frac{S_eL_o}{V_g}\right)}{0.75-M+\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}}_{\text{angle modulation effect}} & M>0.5 \end{cases}, \tag{5.16}$$

$$D_2 = \begin{cases} D_{2,\ uncompensated} + \underbrace{\dfrac{-d\left(0.5+\frac{\hat{V}_f}{V_g}\right)\left(\frac{S_eL_o}{V_g}-M\right)}{0.25-M-\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}}_{\text{angle modulation effect}} & M<0.5 \\ D_{2,\ uncompensated} + \underbrace{\dfrac{-d\left(0.5+\frac{\hat{V}_f}{V_g}\right)\left(1-M+\frac{S_eL_o}{V_g}\right)}{0.75-M+\left(\frac{\hat{V}_f}{V_g}\right)^2+\frac{S_eL_o}{V_g}}}_{\text{angle modulation effect}} & M>0.5 \end{cases}, \tag{5.17}$$

leading to the FC average current which is given by

$$I_{fly} = \begin{cases} (D_2-D_1)\Big[I_o - \dfrac{MV_g(D_{1f}+D_{2f})}{4L_of_s} - \dfrac{(S_eL_o-MV_g)(D_2-D_1)^2}{2L_of_s} \\ \quad -\dfrac{3d\,(S_eL_o-MV_g)}{2L_of_s}\left(D_2-D_1+\dfrac{2d}{3}\right)\Big] - d\dfrac{MV_g(D_1+D_2)}{2Lf_s} & M<0.5 \\ (D_2-D_1)\Big[I_o - \dfrac{V_g(1-M)}{2L_of_s} + \dfrac{V_g(1-M)(D_1+D_2)}{4L_of_s} + \\ \quad \left(\dfrac{S_e}{2f_s}+\dfrac{V_g(1-M)}{2L_of_s}\right)(D_2-D_1)^2 + \\ \quad \dfrac{3dV_g\left(1-M+\frac{S_eL_o}{V_g}\right)}{2L_of_s}\left(D_2-D_1+\dfrac{2d}{3}\right)\Big] - \\ \quad \dfrac{d(1-M)V_g(2-D_1-D_2)}{2L_of_s} & M>0.5 \end{cases}, \tag{5.18}$$

Similarly, the values of the duty cycle commands D_{1f} and D_{2f} are replaced and the equation is linearized to obtain the approximated FC average current which is given by

Table 5.1: Simulation and Experimental Setup Parameters

Parameter	Value	Unit
Input voltage V_g	16.5	V
Output voltage (V_o)	3.3	V
Conversion ratio (M)	20	%
Load current (I_o)	500	mA
Operating frequency (f_s)	500	kHz
Flying capacitor (C_{fly})	400	nF
Output inductance (L_o)	6.5	µH
Output capacitance (C_o)	10	µF

$$I_{fly} = \begin{cases} \underbrace{\frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}}\left[I_o - \frac{\Delta I_L M}{2(0.5-M)}\right]}_{\text{uncompensated current}} + \\ \underbrace{-d\left[\frac{M^2 V_g\left(0.5 - M + \frac{S_e L_o}{V_g}\right)}{2L_o f_s\left(0.25 - M + \frac{S_e L_o}{V_g}\right)} + \frac{I_o\left(\frac{S_e L_o}{V_g} - M\right)}{0.25 - M + \frac{S_e L_o}{V_g}}\right]}_{\text{IA-MOD correction}} & M < 0.5 \\ \underbrace{\frac{(1-M)\frac{\hat{V}_{fly}}{V_g}}{0.75 - M + \frac{S_e L_o}{V_g}}\left[I_o - \frac{(1-M)\Delta I_L}{2(M-0.5)}\right]}_{\text{uncompensated current}} + \\ \underbrace{-d\left[\frac{V_g(1-M)^2\left(0.5 - M + \frac{S_e L_o}{V_g}\right)}{2L_o f_s\left(0.75 - M + \frac{S_e L_o}{V_g}\right)} + \frac{I_o\left(1 - M + \frac{S_e L_o}{V_g}\right)}{0.75 - M + \frac{S_e L_o}{V_g}}\right]}_{\text{IA-MOD correction}} & M > 0.5 \end{cases} \tag{5.19}$$

The term represents the IA-MOD effect is always negative as long as

$$S_e \geq \frac{V_g}{2L_o}. \tag{5.20}$$

Then, by adopting the same FC voltage stability analysis methodology shown earlier, in the IA-MOD technique the inherent negative feedback on the FC voltage is easily concluded from (5.19). Hence, the AI-MOD architecture is inherently stable in all operating modes and conditions by proper selection of the compensation ramp slope (5.20).

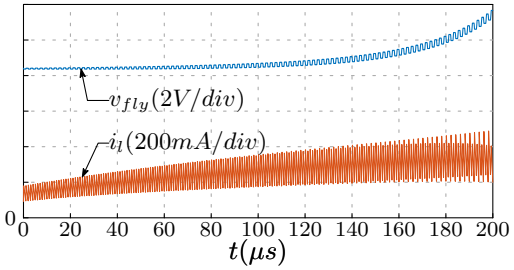


Figure 5-5: Simulation results for a 3LFC running with the conventional P-CMC without stabilizing technique when $\frac{\Delta I_L}{Io} = 61\,\%$.

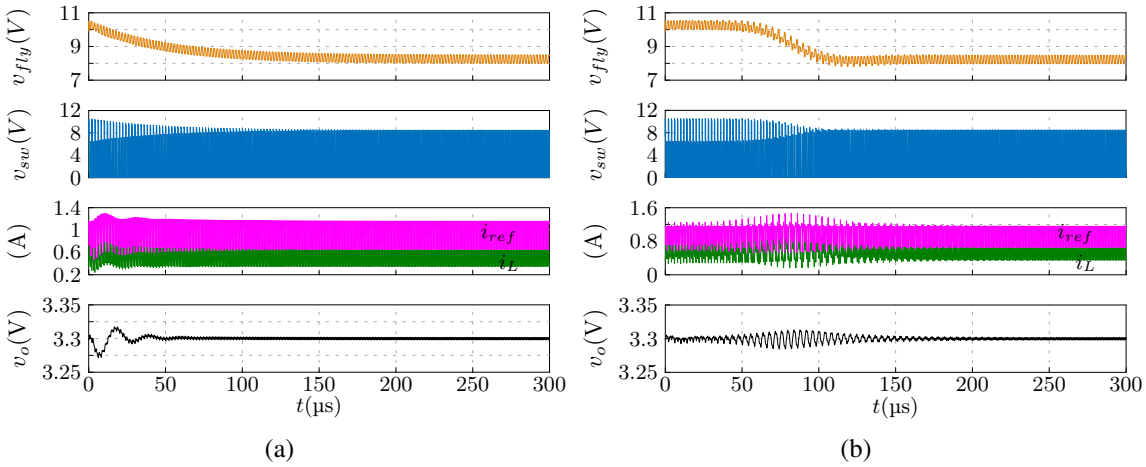
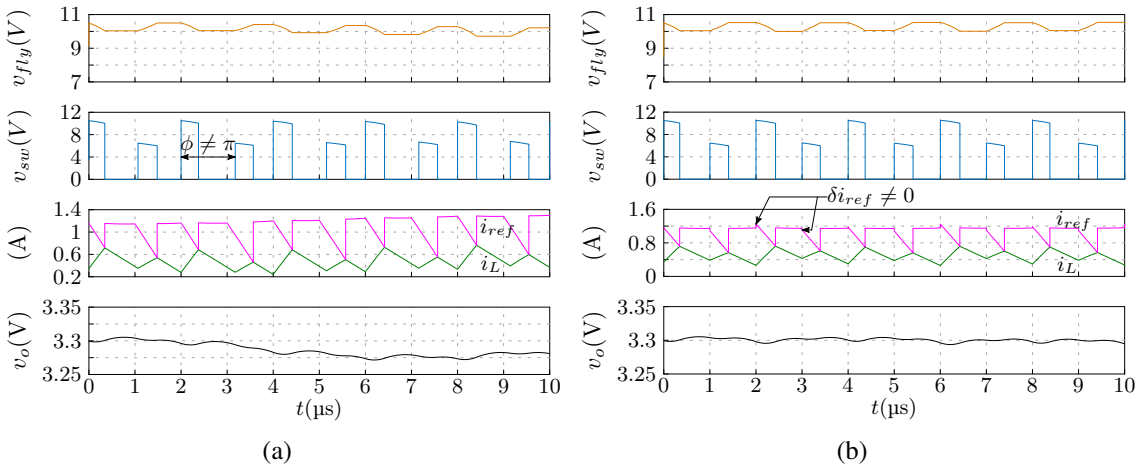


Figure 5-6: Simulation results for a 3LFC controlled with P-CMC and has a voltage conversion ratio $M = 0.2$, output voltage $v_o = 3.3\,\mathrm{V}$, load current $I_o = 500\,\mathrm{mA}$: (a) IA-MOD and (b) PO-MOD after 2 V perturbation in the FC-voltage

5.5 Simulation Results

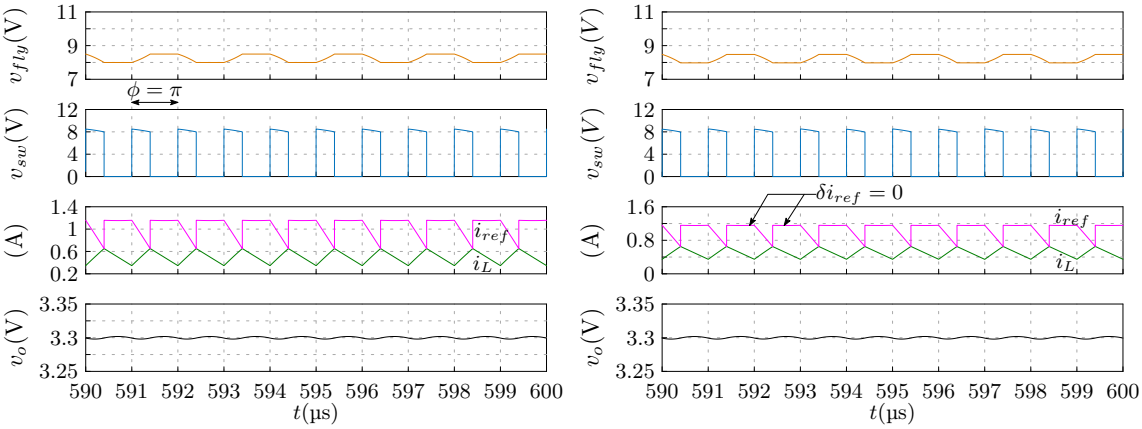
A Matlab® simulink based model is built to verify the proposed approach with the parameters shown in Table 5.1. The nominal FC average voltage of the converter which has $M = 0.2$ and output voltage $v_o = 3.3\,\mathrm{V}$ is $V_{fly} = 8.25\,\mathrm{V}$. The FC-voltage under conventional P-CMC control is unstable due to the FC-voltage runaway, as shown in Fig. 5-5.

In order to verify the proposed stabilizing architectures, the simulation is started with an initial perturbation $\hat{V}_{fly} = 2\,\mathrm{V}$ which is imposed on the FC voltage. By employing the proposed sensorless approach, the two developed architectures IA-MOD and PO-MOD, are able to eliminate the FC voltage instability, as shown in Fig. 5-6(a) and Fig. 5-6(b) respectively.



(a) (b)

Figure 5-7: Simulation results for a 3LFC controlled with P-CMC and has a voltage conversion ratio $M = 0.2$, output voltage $v_o = 3.3\,\mathrm{V}$, load current $I_o = 500\,\mathrm{mA}$ during the first five switching cycle after the FC voltage perturbation: (a) IA-MOD and (b) PO-MOD



(a) (b)

Figure 5-8: Simulation results for a 3LFC controlled with P-CMC and has a voltage conversion ratio $M = 0.2$, output voltage $v_o = 3.3\,\mathrm{V}$, load current $I_o = 500\,\mathrm{mA}$ during the last five switching cycle after the FC voltage perturbation: (a) IA-MOD and (b) PO-MOD

The waveforms shown in Fig. 5-7(a), verify that the IA-MOD architecture modulates the phase shift between the modulating signals in order to eliminate the instability, where the angle between the modulating signal rising edges $\phi \neq \pi$. On the other hand, in PO-MOD architecture the instability is eliminated by reference offsetting, as shown in the asymmetrical current reference in Fig. 5-7(b). Moreover, the proposed approach offers FC voltage balancing feature as shown in the periodic waveforms in Fig. 5-8(a) and Fig. 5-8(b).

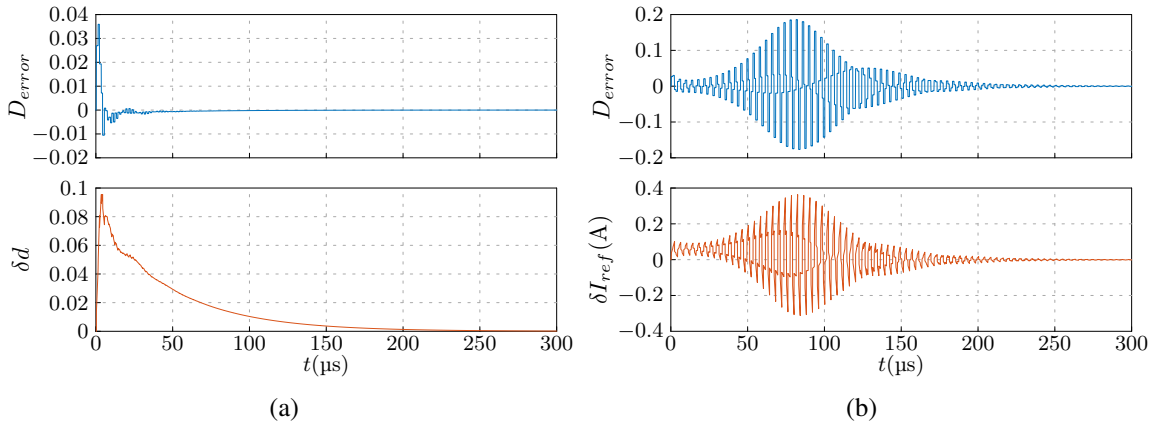


Figure 5-9: Stabilizing techniques loop control commands; duty cycle error D_{error}, interleaving modulation value d, and peak reference modulation value δI_{ref}: (a) for interleaving angle modulation technique and (b) for peak offsetting modulation technique

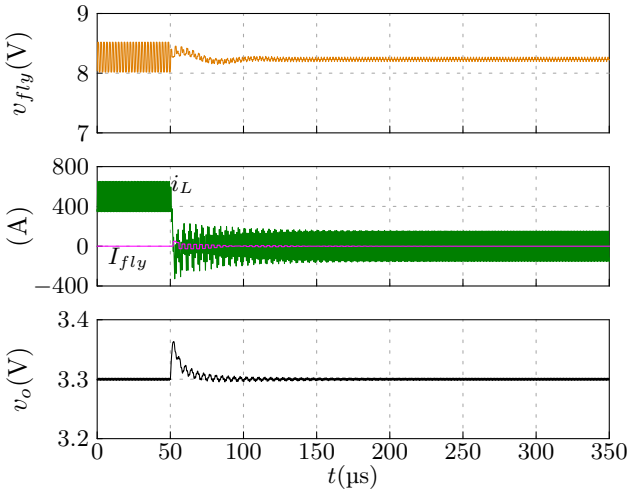


Figure 5-10: Simulation results for a 3LFC controlled with P-CMC and has a voltage conversion ratio $M = 0.2$, output voltage $v_o = 3.3\,\mathrm{V}$, load current $I_o = 500\,\mathrm{mA}$, and $L_o = 6.5\,\mu\mathrm{H}$ with load step change from full-load to no load to simulate the violation of the condition (5.11)

As claimed earlier the steady-state balanced operating point of the converter, where the interleaving angle modulation technique is employed, is at $D_1 = D_2$ and interleaving angle correction $d = 0$, which is verified in the results shown in Fig. 5-9(a). Similarly, the reference current offset δI_{ref} is zero at the steady-state balanced operating point as shown in Fig. 5-9(b).

For the sole purpose of testing system stability when the condition shown in (5.11)

is violated, a converter with PO-MOD employed is tested under a load step change from $500\,\mathrm{mA}$ to no load. As shown in Fig. 5-10, the system is stable with zero FC average current $I_{fly} = 0$ and balanced FC voltage at no load condition.

5.6 Experimental Results

Experimental setup is built with the parameters shown in Table 5.1 in order to experimentally verify the proposed approach. The both developed architectures are digitally implemented on a commercial FPGA board. The current reference is generated in the digital domain, then a DAC is used to generate the current reference to the analog comparator. Two test scenarios are developed in order to validate the proposed techniques.

5.6.1 Test scenario 1

Here, the converter is firstly put in the steady-state condition with a plain voltage-mode controller. Afterwards, the peak current-mode controller is enabled. As shown in Fig. 5-11, enable the conventional P-CMC leads to instability due to FC-voltage runaway. Otherwise, as shown in Fig. 5-12(a), when the sensorless interleaving angle modulation technique is enabled, after $1.5\,\mathrm{ms}$ from enabling the P-CMC, that leads to FC-voltage balancing and system stability. Moreover, from the zoom-in waveforms, shown below the original results, before achieving the FC-voltage balancing the interleaving angle between the two modulating signal is $\phi \neq \pi$. On the other hand, after steady-state the correction value provided by the stabilizing loop $d = 0$ as shown in the zoom-in version shown on top of the original results, and hence $\phi = \pi$.

Similarly, the sensorless peak offsetting modulation technique is validated in Fig. 5-12(b), where after enabling the PO-MOD technique the FC-voltage is balanced at $\frac{V_g}{2}$ and the system is stabilized. With a FC-voltage imbalance the current reference is modulated, as shown in the asymmetrical current reference within a single switching cycle in the zoom-in results on the bottom of the original results. On the other hand, at steady state the current reference is fixed and the current correction $\delta I_{ref} = 0$.

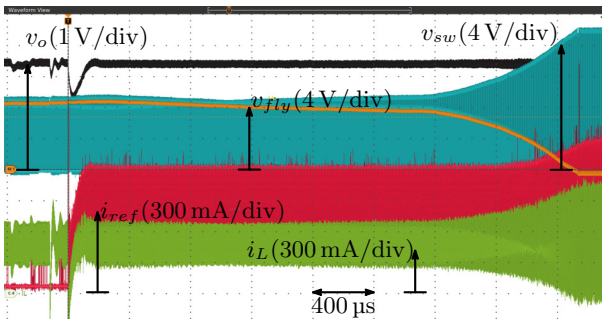


Figure 5-11: Experimental results of P-CMC converter has a voltage conversion ratio $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$ without stabilizing technique

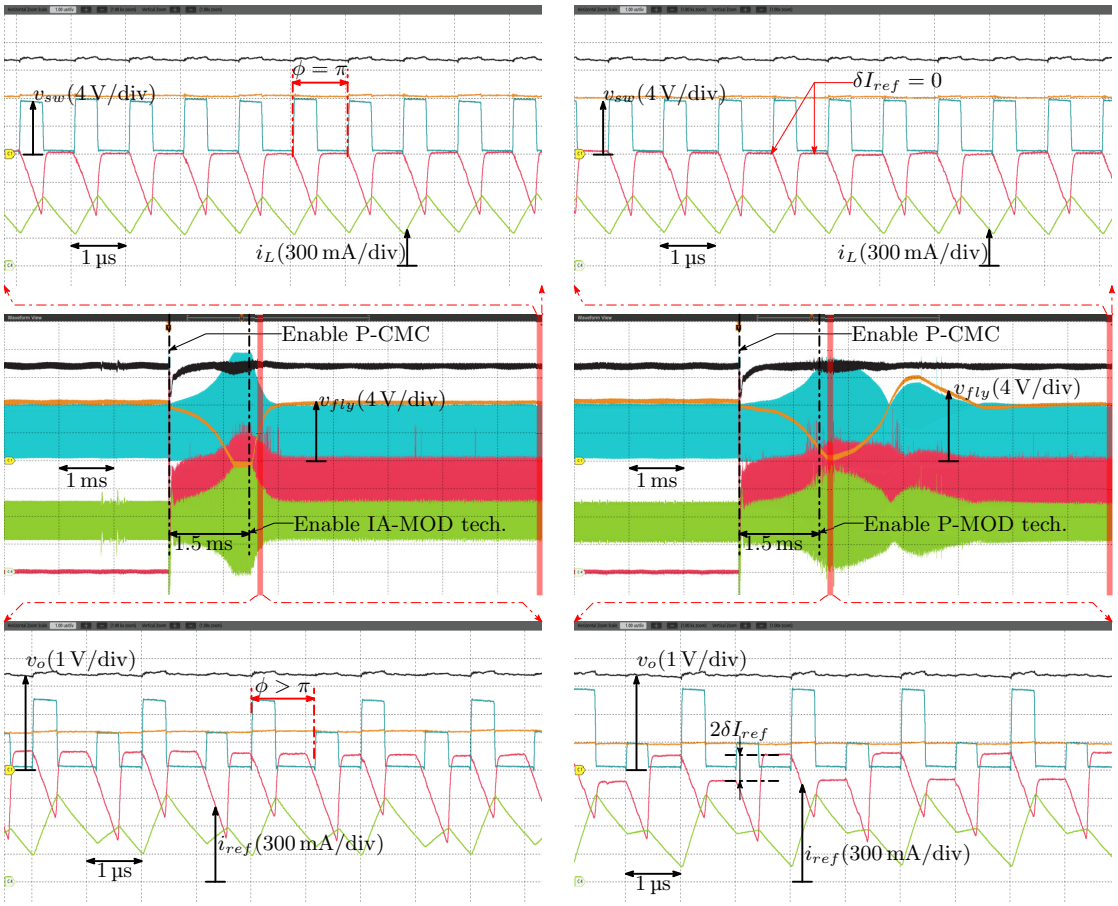


Figure 5-12: Experimental results of P-CMC converter has a voltage conversion ratio $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$ started with voltage mode control, afterwards the P-CMC is enabled without balancing technique, and finally the stabilizing technique is enabled after $1.5\,\text{ms}$ of enabling P-CMC: (a) IA-MOD and (b) PO-MOD

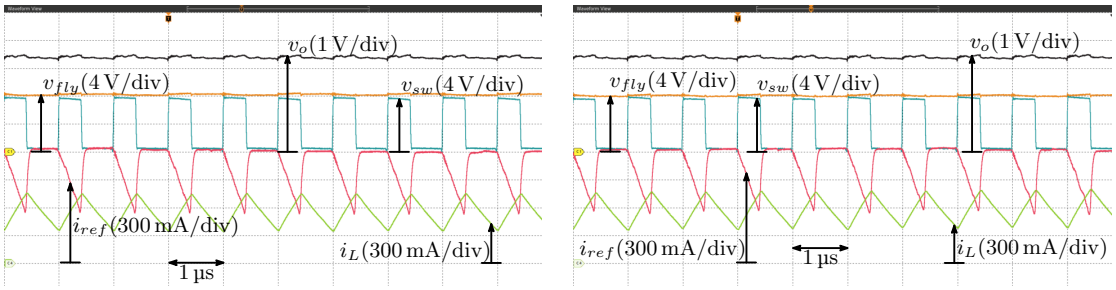


Figure 5-13: Experimental results of P-CMC converter has a voltage conversion ratio $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$: (a) P-CMC with IA-MOD technique steady-state and (b) P-CMC with PO-MOD technique steady-state waveforms

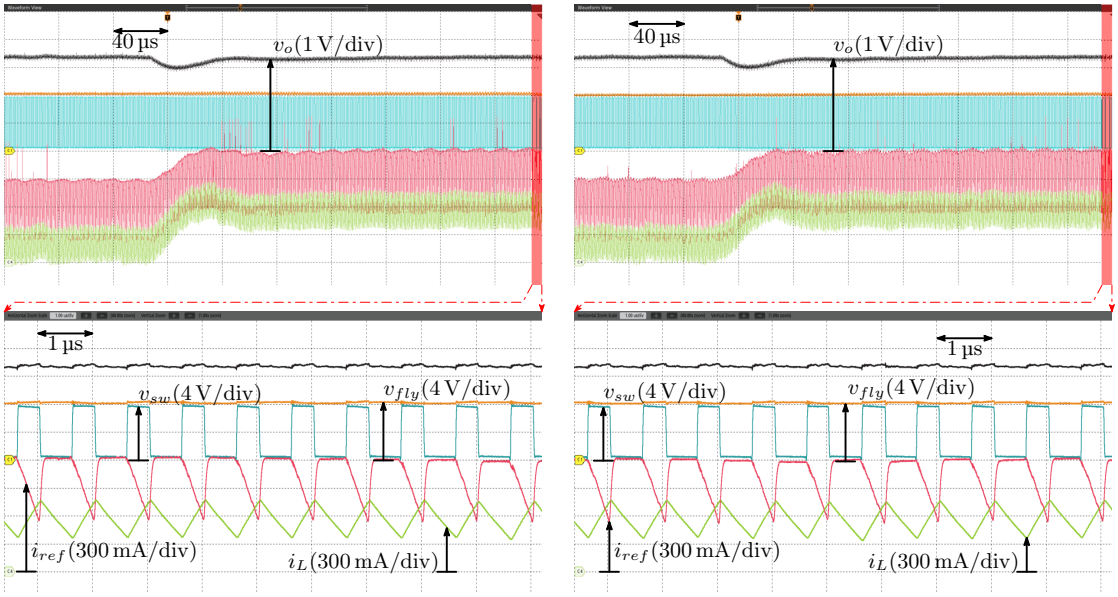


Figure 5-14: Experimental results of P-CMC converter has a voltage conversion ratio $M = 0.2$, flying capacitor $C_{fly} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$: (a) P-CMC with IA-MOD technique with 50 % to 100 % load step and (b) P-CMC with PO-MOD technique with 50 % to 100 % load step

5.6.2 Test scenario 2

Here, the system is running with the P-CMC and the stabilizing technique is employed. As shown in the steady-state condition both IA-MOD and PO-MOD architectures stabilize the system and balance the FC-voltage as shown in Fig. 5-13(a) and Fig. 5-13(b) respectively.

Afterwards, the validity of the developed architectures are verified under a load transient condition. As shown respectively in Fig. 5-14(a) and Fig. 5-14(b) after a $50\,\%$-to-$100\,\%$ load step both interleaving angle modulation and peak offsetting modulation are able to stabilize and balance the FC-voltage.

5.7 Summary and Contribution

In this chapter, a sensorless approach is proposed to stabilize the peak current-mode controller for the three-level flying-capacitor converter. The proposed technique is able to detect the FC-voltage imbalance by measuring the error between the duty cycle commands. Two implementation architectures are developed based on the proposed approach, the sensorless peak offsetting modulation (PO-MOD), and sensorless interleaving angle modulation (IA-MOD). The both architectures are able to eliminate the instability associated with the FC-voltage runaway in the conventional P-CMC 3LFC. The sensorless operation of the proposed architectures offers a reduced size, reliable, and cost effective mixed-signal solution for 3LFC controller. Moreover, using the P-CMC guarantees an inherent overcurrent protection which enables the adoption of the 3LFC in the automotive application. In addition to, the proposed approach can be extended to a larger number of voltage levels. An analytical justification of the developed approach using the two proposed methodologies is introduced, and the implementation architectures are validated in simulation and experimentally.

Chapter 6

Conclusions

6.1 Conclusions

In this work two converter topologies are investigated. The first is the ZVS quasi-resonant buck converter topology. On one hand, some merits are gained by adopting the quasi-resonant topology like improved EMI capabilities and increased operating frequency. On the other hand, in such topology many limitations are recognized associated with the converter operating ranges and strong dependency on the component tolerances. The digital efficiency optimization technique in chapter 2 is proposed in order to improve the converter performance. The proposed technique offers extended operating range, reduced dependency on the component tolerances, and compressed operating frequency range. In addition to more flat efficiency variation with load changes. The developed technique analysis and results are proposed in a conference paper [16]. Even with the improved performance by the proposed optimization technique, the converter features are inconsistent with the target application and company needs.

Subsequently, the three-level flying-capacitor converter (3LFC) is investigated. The topology offers high power density and improved transient response due to the increased effective ripple frequency. The 3LFC adoption faces many challenges like converter starting, FC voltage balancing, and the operation around the zero-ripple operating point ($M = 0.5$). Employing FC stabilizing control creates many instability problems. Voltage mode controlled converter with an additional FC voltage balancing loop is inherently stable if and

only if a dual edge modulator is used. Otherwise, when the system is implemented with trailing edge modulator a potential instability recognized associated with light load conditions [50]. The same instability concern is recognized in the average current mode controlled converter with trailing edge modulator. The valley current mode control (V-CMC) is presented as a control solution for the 3LFC with an inherent FC voltage balancing feature in [5], but the peak current mode control (P-CMC) is unstable [53]. In this work a stability criterion of the 3LFC under valley and peak current mode control is proposed.The inherent stability and FC voltage balancing in V-CMC is formally proven. The instability of P-CMC associated with the FC voltage runaway, which is recognized in [5, 53], is studied in details. The P-CMC results to be inherently unstable unless the system run with relatively high peak-to-peak inductor current ripple, the feature which firstly presented in this work. The proposed stability criterion with simulation and experimental assessment is presented in a conference paper [27] and extended in a journal version [28].

The interesting features of the P-CMC motivate the development of a the sensorless stabilizing approach for P-CMC architecture reported in chapter 5. The proposed approach detecting the FC voltage imbalance by measuring the duty commands difference. Two implementation methodologies are developed, interleaving angle modulation (IA-MOD) and peak offsetting modulation (PO-MOD). The implementation methodologies are analytically studied and verified with simulation models and experimentally. The proposed stabilizing approach offers a system with some interesting features like

1. sensorless operation,
2. FC voltage self-balancing,
3. input voltage independent operation,
4. reduced size,
5. availability of extension to higher number of levels with the minimal hardware complexity.

Appendices

Appendix A

Derivation of expressions D_1, D_2, and I_{fly} in chapter 4

Considering the steady state waveforms in Fig. A-1, a derivation of the expressions of the different duty commands, D_1 and D_2, and flying capacitor average current I_{fly} are developed. Under the flying capacitor voltage mismatch the switching node voltage v_{sw} has asymmetrical levels. The switching node average voltage V_{sw} is given by

$$V_{sw} = \frac{D_1 + D_2}{2} V_g + \hat{V}_f (D_1 - D_2), \tag{A.1}$$

when output voltage $V_o = V_{sw}$ then the voltage conversion ratio is given by

$$M = \frac{D_1 + D_2}{2} + \frac{\hat{V}_f}{V_g} (D_1 - D_2), \tag{A.2}$$

regardless of the modulation scheme and operating mode. Accordingly, from (A.2) D_2 is given by

$$D_2 = \frac{M - (0.5 + \frac{\hat{V}_f}{V_g}) D_1}{0.5 - \frac{\hat{V}_f}{V_g}}. \tag{A.3}$$

The presented equations will be divided into two main sections. On one hand, the first section reports the trace for the equations in case of using the V-CMC modulation scheme

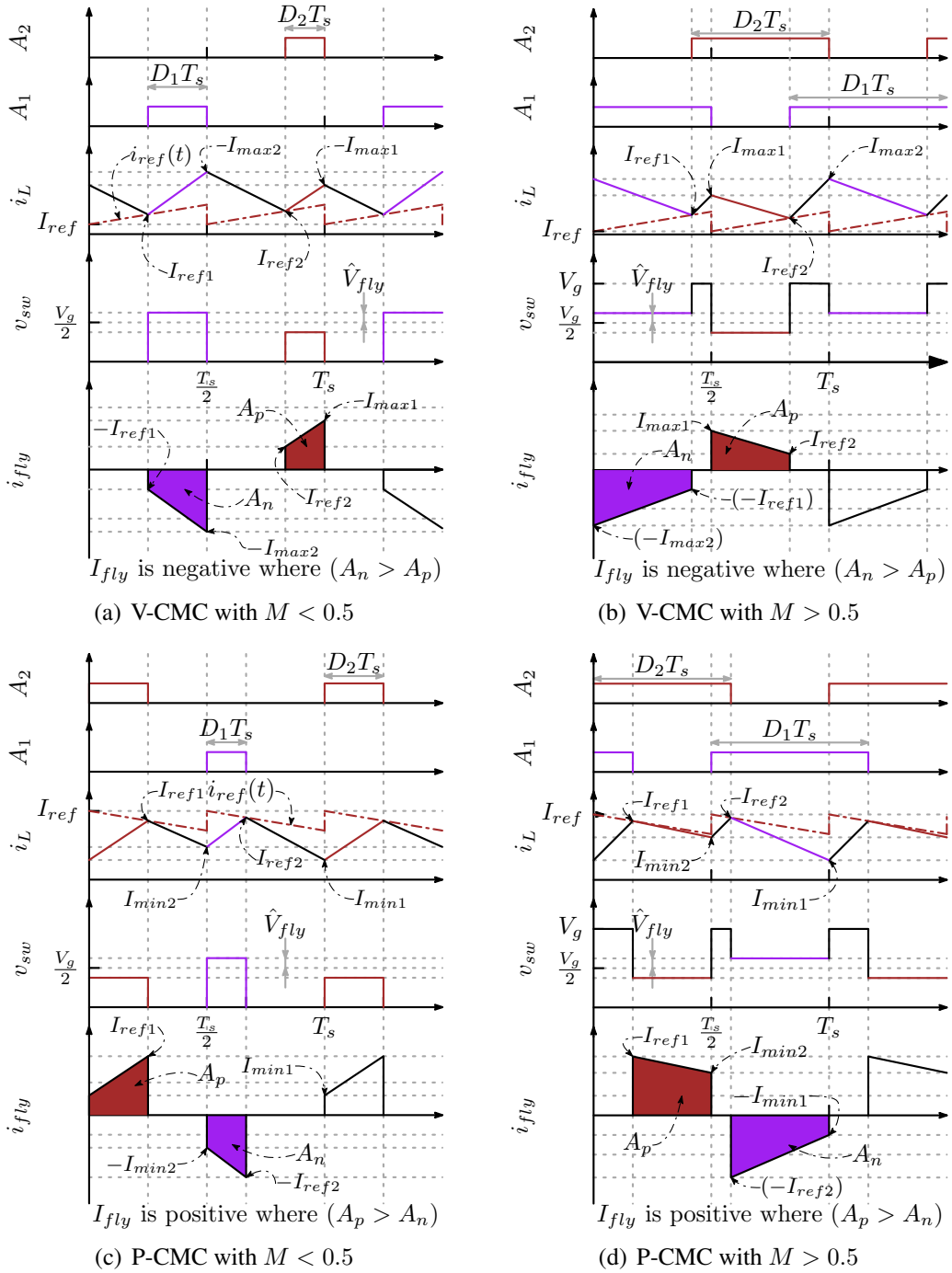


Figure A-1: Steady-state waveforms including a compensation ramp and considering a small positive perturbation $\hat{V}_f$ in the FC voltage.

considering the two operating modes $M < 0.5$ and $M > 0.5$. On the other hand, in the second section the P-CMC modulation scheme equations are listed.

A.1 Equations for V-CMC

A.1.1 Operating mode $M < 0.5$

The inductor current intersects the valley reference waveform i_{ref} at two different thresholds I_{ref1} and I_{ref2} during a single switching cycle, as shown in Fig. A-1(a). The values of the inductor current valley points are given by

$$I_{ref1} = I_{ref} + S_e(0.5 - D_1)T_s, \tag{A.4}$$

$$I_{ref2} = I_{ref} + S_e(0.5 - D_2)T_s. \tag{A.5}$$

From the definition of the inductor current slope during the subinterval D_1T_s,

$$\frac{I_{max2} - I_{ref1}}{D_1T_s} = \frac{0.5 - M + \frac{\hat{V}_f}{V_g}}{\frac{L_o}{V_g}}. \tag{A.6}$$

By substitution from (A.4) into (A.6), then,

$$I_{max2} = I_{ref} + \frac{0.5 - M + \frac{\hat{V}_f}{V_g}}{\frac{L_o f_s}{V_g}} D_1 + \frac{S_e(0.5 - D_1)}{f_s}, \tag{A.7}$$

Similarly, by calculating the inductor current slope during the subinterval $(0.5 - D_2)T_s$, then,

$$I_{max2} = I_{ref} + \frac{M(0.5 - D_2)}{\frac{L_o f_s}{V_g}} + \frac{S_e(0.5 - D_2)}{f_s}. \tag{A.8}$$

From (A.7) an (A.8),

$$D_1 = \frac{0.5M - (M + \frac{S_e L_o}{V_g})D_2}{0.5 - M + \frac{\hat{V}_f}{V_g} - \frac{S_e L_o}{V_g}} \tag{A.9}$$

By substituting (A.3) into (A.9) the expressions of duty commands D_1 and D_2, shown in (4.35) and (4.36), are derived,

$$D_1|_{\text{V-CMC, } M<0.5} = M\frac{0.25 - M - \frac{\hat{V}_f}{2V_g} - \frac{S_e L_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}, \tag{A.10}$$

$$D_2|_{\text{V-CMC, } M<0.5} = M\frac{0.25 - M + \frac{\hat{V}_f}{2V_g} - \frac{S_e L_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}. \tag{A.11}$$

For the purpose of calculating the flying capacitor average current, firstly the values of the asymmetrical inductor current peaks I_{max1} and I_{max2} are determined. The absolute slope of the inductor current discharging phase m_{OFF} is output voltage dependent and independent of FC-voltage perturbation $\hat{V}_f$. The expressions for I_{max1} and I_{max2} are derived from the expressions of m_{OFF} in the subintervals $0 \rightarrow (0.5 - D_1)T_s$ and $\frac{T_s}{2} \rightarrow (1 - D_2)T_s$ respectively,

$$I_{max_1} = I_{ref} + \left(\frac{S_e L_o + MV_g}{L_o f_s}\right)(0.5 - D_1) \tag{A.12}$$

$$I_{max_2} = I_{ref} + \left(\frac{S_e L_o + MV_g}{L_o f_s}\right)(0.5 - D_2) \tag{A.13}$$

From (A.4), (A.5), (A.12), and (A.13) the expression of the flying capacitor average current, shown in (4.40), is derived

$$I_{fly}|_{\text{V-CMC, } M<0.5} = (D_2 - D_1)\Big[I_{ref} + \frac{MV_g}{4L_o f_s} + \frac{S_e}{2f_s}[1 - (D_1 + D_2)]\Big], \tag{A.14}$$

Similarly, the inductor average current is calculated and an expression for the fixed current reference I_{ref} is developed,

$$I_{ref} = I_o - \frac{2S_e L_o + MV_g}{4L_o f_s} + \frac{S_e(D_1 + D_2)}{2f_s} + \frac{MV_g(D_1 + D_2)}{4L_o f_s} - \frac{S_e L_o + MV_g}{2L_o f_s}(D_2 - D_1)^2 \tag{A.15}$$

By replacing I_{ref}, D_1, and D_2 into (A.14) and linearize under the assumption of small perturbation, then the flying capacitor average current expression is approximated as,

$$I_{fly} \approx \frac{M\frac{\hat{V}_f}{{V_g}^2}}{0.25 - M - \frac{S_e L_o}{V_g}}\left[I_o + \frac{MV_o}{2L_o f_s}\right]. \tag{A.16}$$

By substituting from (3.2) into (A.16) the expression of the flying capacitor average current shown in (4.44) is derived,

$$I_{fly}|_{\text{V-CMC},M\,<\,0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}} \times \left[I_o + \frac{\Delta I_L M}{2(0.5 - M)}\right]. \tag{A.17}$$

A.1.2 Operating mode $M > 0.5$

Similarly, as shown in Fig. A-1(b), the asymmetrical reference currents I_{ref1} and I_{ref2} are given by

$$I_{ref1} = I_{ref} + S_e(1 - D_2)T_s, \tag{A.18}$$

$$I_{ref2} = I_{ref} + S_e(1 - D_1)T_s, \tag{A.19}$$

in the operating mode where $M > 0.5$. From the definition of the inductor current slope during the subinterval $(1 - D_2)T_s \rightarrow 0.5T_s$,

$$I_{max1} = I_{ref} + \frac{S_e}{f_s} - \frac{V_g - V_o}{2L_o f_s} + \left(\frac{V_g - V_o}{L_o f_s} - \frac{S_e}{f_s}\right) D_2. \tag{A.20}$$

Similarly, considering the current slope in the subinterval $0.5T_s \rightarrow (1.5 - D_1)T_s$ then,

$$I_{max1} = I_{ref} + \frac{S_e}{f_s} + \frac{V_o - \frac{V_g}{2} + \hat{V}_f}{L_o f_s} - \left(\frac{V_o - \frac{V_g}{2} + \hat{V}_f}{L_o f_s} + \frac{S_e}{f_s}\right) D_1. \tag{A.21}$$

From (A.20) and (A.21),

$$D_2 = \frac{0.5M + \frac{\hat{V}_f}{V_g}}{1 - M - \frac{S_e L_o}{V_g}} - \frac{M - 0.5 + \frac{\hat{V}_f}{V_g} + \frac{S_e L_o}{V_g}}{1 - M - \frac{S_e L_o}{V_g}} D_1. \tag{A.22}$$

By substituting (A.3) into (A.22) the expressions of duty commands D_1 and D_2, shown in (4.47) and (4.48), are derived,

$$D_1|_{\text{V-CMC},M\,>\,0.5} = \frac{M\left(0.75 - M - \frac{S_e L_o}{V_g}\right) - \frac{\hat{V}_f}{V_g}\left[0.5(1-M) - \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}, \tag{A.23}$$

$$D_2|_{\text{V-CMC},M\,>\,0.5} = \frac{M\left(0.75 - M - \frac{S_e L_o}{V_g}\right) + \frac{\hat{V}_f}{V_g}\left[0.5(1-M) + \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}, \tag{A.24}$$

Similar to the case of $M < 0.5$, the values of the asymmetrical inductor current peaks I_{max1} and I_{max2} are calculated by considering the value of m_{OFF} during the subintervals, $(1-D_2)T_s \rightarrow 0.5T_s$ and $(1.5-D_1)T_s \rightarrow T_s$ respectively,

$$I_{max1} = I_{ref} + \frac{S_e(1-D_2)}{f_s} + \frac{V_g(1-M)(D_2-0.5)}{L_o f_s}, \tag{A.25}$$

$$I_{max2} = I_{ref} + \frac{S_e(1-D_1)}{f_s} + \frac{V_g(1-M)(D_1-0.5)}{L_o f_s}. \tag{A.26}$$

From (A.18), (A.19), (A.25), and (A.25), the FC average current in case of $M > 0.5$ is given by

$$I_{fly}|_{\text{V-CMC, }M\,>\,0.5} = (D_2 - D_1)\Big[I_{ref} + \frac{(1-M)V_g}{4L_o f_s} + \frac{S_e}{f_s} - \frac{S_e(D_1+D_2)}{2f_s}\Big]. \tag{A.27}$$

Following the same steps for calculating FC average current the output inductor average current I_o can be calculated and hence the reference current I_{ref} is given by

$$\begin{aligned} I_{ref} = I_o - \frac{S_e}{fs} + \frac{S_e(D_1+D_2)}{2f_s} + \frac{V_g(1-M)}{4L_o f_s} - \\ \frac{V_g(1-M)(D_1+d_2)}{4L_o f_s} + \frac{S_e L_o - V_g(1-M)}{2L_o f_s}\left(D_2 - D_1\right)^2. \end{aligned} \tag{A.28}$$

Substitute from (A.28) into (A.27) and apply a first order approximation as shown in the previous case, then the FC average current expression shown in (4.51) is derived,

$$I_{fly}|_{\text{V-CMC, } M>0.5} \approx \frac{(1-M)\frac{\hat{V}_{fly}}{V_g}}{0.75-M-\frac{S_e L_o}{V_g}}\Big[I_o+\frac{(1-M)\Delta I_L}{2(M-0.5)}\Big], \tag{A.29}$$

A.2 Equations for P-CMC

The same methodology shown above is here adopted in order to explain how the expressions of the duty commands and FC average current are developed in case of using the P-CMC modulating scheme. In P-CMC under the FC mismatch condition the inductor current hits the reference set point at two different thresholds I_{ref1} and I_{ref2} as shown in Fig. A-1(c) and Fig. A-1(d). In addition to, that inductor current has asymmetrical valley points I_{min1} and I_{min2}.

A.2.1 Operating mode $M < 0.5$

In this operating mode I_{ref1} and I_{ref2} , shown in Fig. A-1(c), are given by

$$I_{ref1} = I_{ref} - S_e D_2 T_s, \tag{A.30}$$

$$I_{ref2} = I_{ref} - S_e D_1 T_s, \tag{A.31}$$

where the current valley values I_{min1} and I_{min2} are given by

$$I_{min1} = I_{ref} - S_e D_1 T_s - \frac{V_o(0.5-D_1)}{L_o f_s}, \tag{A.32}$$

$$I_{min2} = I_{ref} - S_e D_2 T_s - \frac{V_o(0.5-D_2)}{L_o f_s}, \tag{A.33}$$

Two expressions of I_{min2} are derived by considering the current slopes during the subintervals $D_2T_s \rightarrow 0.5T_s$ and $0.5T_s \rightarrow (0.5+D_1)T_s$, in order to express the first duty command

D_1 in terms of M and D_2 as

$$D_1 = \frac{0.5M}{0.5 - M + \frac{\hat{V}_f}{V_g} + \frac{S_e L_o}{V_g}} + \frac{\frac{S_e L_o}{V_g} - M}{0.5 - M + \frac{\hat{V}_f}{V_g} + \frac{S_e L_o}{V_g}} D_2. \tag{A.34}$$

From (A.3) and (A.34) the duty commands expressions shown in (4.37) and (4.38) are driven,

$$D_1|_{\text{P-CMC, } M < 0.5} = M \frac{0.25 - M - \frac{\hat{V}_f}{2V_g} + \frac{S_e L_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}, \tag{A.35}$$

$$D_2|_{\text{P-CMC, } M < 0.5} = M \frac{0.25 - M + \frac{\hat{V}_f}{2V_g} + \frac{S_e L_o}{Vg}}{0.25 - M - \left(\frac{\hat{V}_{fly}}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}. \tag{A.36}$$

The expression of the FC average current shown in (4.41),

$$I_{fly}|_{\text{P-CMC, } M < 0.5} = (D_2 - D_1)\Big[I_{ref} - \frac{MV_g}{4L_o f_s} - \frac{S_e(D_1 + D_2)}{2f_s}\Big], \tag{A.37}$$

is driven by averaging the FC current over one switching cycle and substitute from (A.30), (A.31), (A.32), and (A.33). The expression of I_{ref} is derived by calculating the inductor current average current,

$$I_{ref} = I_o + \frac{S_e(D_2 + D_1)}{2f_s} + \frac{V_o\left[1 - (D_1 + D_2)\right]}{4L_o f_s} - \left(\frac{S_e}{2f_s} - \frac{V_o}{2L_o f_s}\right)(D_2 - D_1)^2. \tag{A.38}$$

By substitute I_{ref}, D_1, and D_2 in (A.37) and then linearize, that is how the approximated FC average current shown in (4.45) is driven,

$$I_{fly}|_{\text{P-CMC}, M < 0.5} \approx \frac{M\frac{\hat{V}_f}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}}\left[I_o - \frac{\Delta I_L M}{2(0.5 - M)}\right]. \tag{A.39}$$

A.2.2 Operating mode $M > 0.5$

Similarly, as shown in Fig. A-1(d), the values I_{ref1}, I_{ref2}, I_{min1}, and I_{min2} for the P-CMC and in the operating mode $M > 0.5$ are respectively given by

$$I_{ref1} = I_{ref} - S_e(D_1 - 0.5)T_s, \tag{A.40}$$

$$I_{ref2} = I_{ref} - S_e(D_2 - 0.5)T_s, \tag{A.41}$$

$$I_{min1} = I_{ref} - S_e(D_1 - 0.5)T_s - \frac{(V_g - V_o)(D_1 - 0.5)}{L_o f_s}, \tag{A.42}$$

$$I_{min2} = I_{ref} - S_e(D_2 - 0.5)T_s - \frac{(V_g - V_o)(D_2 - 0.5)}{L_o f_s}. \tag{A.43}$$

In the case of $M < 0.5$ an additional relation between D_1 and D_2 is derived by calculating the value of I_{min2} in the subintervals $D_2T_s \rightarrow 0.5T_s$ and $0.5T_s \rightarrow (0.5 + D_1)T_s$. Similarly, in case of $M > 0.5$, the value of D_1 is given as a function of M and D_2 by

$$D_1 = \frac{-0.5M - \frac{\hat{V}_f}{V_g}}{0.5 - M - \frac{\hat{V}_f}{V_g} + \frac{S_e L_o}{V_g}} + \frac{1 - M + \frac{S_e L_o}{V_g}}{0.5 - M - \frac{\hat{V}_f}{V_g} + \frac{S_e L_o}{V_g}} D_2, \tag{A.44}$$

by calculating I_{min2} from the inductor current slope during the subintervals $(D_1 - 0.5)T_s \rightarrow 0.5T_s$ and $0.5T_s \rightarrow D_2T_s$. From (A.3) and (A.44) the expressions of D_1 and D_2 shown in (4.49) and (4.50) are driven,

$$D_1|_{\text{P-CMC}, M\,>\,0.5} = \frac{M\left(0.75 - M + \frac{S_e L_o}{V_g}\right) - \frac{\hat{V}_f}{V_g}\left[0.5(1 - M) - \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}, \tag{A.45}$$

$$D_2|_{\text{P-CMC}, M\,>\,0.5} = \frac{M\left(0.75 - M + \frac{S_e L_o}{V_g}\right) + \frac{\hat{V}_f}{V_g}\left[0.5(1 - M) + \frac{\hat{V}_f}{V_g}\right]}{0.75 - M + \left(\frac{\hat{V}_f}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}, \tag{A.46}$$

Then the approximated FC average current in (4.52),

$$I_{fly}|_{\text{P-CMC}, M\,>\,0.5} \approx \frac{(1 - M)\frac{\hat{V}_{fly}}{V_g}}{0.75 - M + \frac{S_e L_o}{V_g}}\left[I_o - \frac{(1 - M)\Delta I_L}{2(M - 0.5)}\right]. \tag{A.47}$$

is given by deriving the FC average current and then substituting the value of D_1, D_2, I_{min1}, and I_{min2} from (A.45), (A.46), (A.42), and (A.43) respectively, subsequently, applying a first order approximation.

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