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HIGH EFFICIENCY ALN/GAN HEMTS FOR Q-BAND APPLICATIONS WITH AN IMPROVED THERMAL DISSIPATION*

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In this paper, we demonstrate Q-band power performance of carbon doped AlN/GaN high electron mobility transistors (HEMTs) using a deep sub-micrometer gate length (120 nm). With a maximum drain current density I_D of 1.5 A/mm associated to a high electron confinement and an extrinsic transconductance g_m of 500 mS/mm, this structure shows excellent electrical characteristics. A maximum oscillation frequency f_{max} of 242 GHz has been observed. As a result, a state-of-the-art combination at 40 GHz of output power density ($P_{OUT} = 7$ W/mm) and power added efficiency (PAE) of 52% up to $V_{DS} = 25$ V has been obtained. The achievement of such outstanding performance is attributed to the reduced thermal resistance (R_{TH}) as compared to the commonly used double heterostructure by means of Raman thermography.

Keywords: High electron mobility transistors (HEMTs), Double heterostructure field effect transistor (DHFET), GaN, Raman thermography, output power density (P_{OUT}), power added efficiency (PAE).

1. Introduction

The requirements for the emerging wireless communication systems such as 5G significantly increases the need for compact solid-state high power amplification based on gallium nitride (GaN) material. Achieving both high power-added-efficiency (PAE) and output-power-density (P_{OUT}) in the millimeter-wave range represents currently one of the key goals for the GaN technology. Indeed, higher PAE not only saves electrical power usage but also can reduce the size and cost of high power amplifiers (HPAs), due to the lower amount of heat dissipated. For instance, in space applications, the traveling wave tube amplifiers (TWTA) are still commonly used, because of the high PAE while

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delivering high P_{OUT} . Despite excellent PAE demonstrated so far with GaN devices up to Ka band [1]-[5], a limited set of data in the Q band (40 GHz) and above are available. As shown by HRL laboratory [6],[7] the double heterostructure field effect transistor (DHFET) using an AlGaN back barrier allowed combining a high electron confinement with high frequency performance together with low trapping effects [8]-[14]. However, AlGaN alloys have the drawback to provide much lower thermal conductivity than the binaries GaN or AlN [15], which in turn causes an increase in the peak channel temperature during operation [16]. Compared to Fe doped GaN buffers, carbon-doped HEMT structures show lower memory effects [17], lower risk of diffusion and the elimination of contamination risks when used in Si CMOS-based foundries. That is why, this structure is widely used for high voltage power applications. In this work, a carbon-doped HEMT structure [19], using a 0.12 μm gate technology has been evaluated and compared to a DHFET [20] with the aim of pushing the bias operation in the millimeter-wave range while maintaining a reduced junction temperature.

2. Device Fabrication

The AlN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on 4 in. SiC substrates. The HEMT structure consists of a transition layer to GaN, a 1 μm -thick carbon-doped GaN buffer layer followed by a 150 nm thick un-doped GaN channel, a 4 nm ultrathin AlN barrier layer and a 10-nm-thick in situ Si_3N_4 cap layer (Fig. 1). The in-situ SiN layer is used both as early passivation as well as to prevent strain relaxation [21]-[23]. The channel thickness has been chosen with respect to the trade-off between the electron confinement and the trapping effects. In the second structure called DHFET, the GaN buffer layer is replaced by a 1 μm -thick $\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}$ layer as shown in Figure 1. Room temperature Hall measurements showed high electron sheet concentrations of 1.8×10^{13} and $1.6 \times 10^{13} \text{ cm}^{-2}$ with an electron mobility of about $1100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ in the HEMT and DHFET heterostructures, respectively. The device fabrication details can be found in [20]. Ohmic contact resistance (R_c) extracted from linear transmission line method (TLM) was as low as $0.3 \Omega.\text{mm}$ for both heterostructures. A 0.12 μm Ni/Au T-gate length was defined by e-beam lithography (see Fig. 1). The gate-source and gate drain spacing were 0.3 and 2 μm , respectively, and the unit device width was 50 μm .

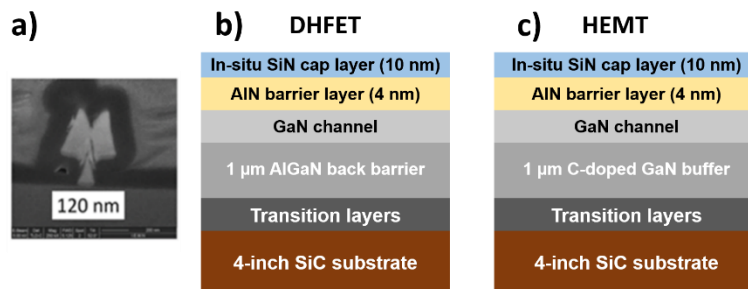


Fig. 1. a) FIB view of the 0.12 μm T-gate and schematic cross section of b) DHFET and c) C-doped HEMT.

3. DC AND SMALL SIGNAL CHARACTERIZATIONS

DC characterizations have been performed with a Keysight A2902A parameter analyzer. Fig. 2 shows some typical I_D - V_{DS} characteristics for both structures. The gate source voltage was swept from -6V to +2V with a step of 0.5 V. For the DHFET, a maximum drain current density (I_{Dmax}) of 1.3 A/mm is observed. The devices based on the HEMT structure deliver a higher I_{Dmax} of 1.5 A/mm under the same conditions reflecting the higher carrier concentration.

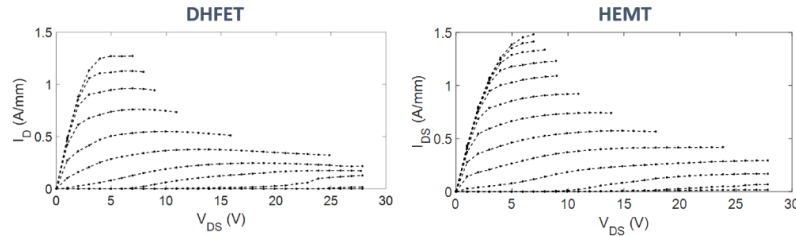


Fig. 2. Output characteristics of a $2 \times 50 \mu\text{m}$ AlN/GaN DHFET and HEMT.

The transfer characteristics of both structures at $V_{DS} = 6, 8$ and 10 V appear in Fig. 3. Excellent device pinch-off behavior was obtained, which is illustrated by the low off-state leakage current below $10 \mu\text{A}/\text{mm}$ and the high breakdown voltages of 80V and 110V for the HEMT and DHFET structures, respectively. A low threshold voltage shift as a function of V_{DS} is also observed in both cases. This confirms that a good electron confinement can be also obtained without the insertion of an AlGaN back barrier, despite the use of short gate lengths (< 150 nm). In addition, a slightly higher extrinsic transconductance is observed for the HEMT structure with a g_m around 500 mS/mm at $V_{DS}=10\text{V}$ against 470 mS/mm at $V_{DS}=10\text{V}$ for the DHFET. The current-gain and power-gain cut-off frequencies are extracted from the scattering (S) parameters using Rhode and Schwarz ZVA67GHz network analyzer at $V_{DS} = 20\text{V}$. The quiescent current bias point has been varied around the peak transconductance so that the maximum frequency performances are extracted. The DHFET yields a $f_T = 45$ GHz and $f_{max} = 235$ GHz, while slightly better RF performances are achieved for the HEMT with $f_T = 60$ GHz and $f_{max} = 242$ GHz (see Fig. 4). This indicates that we may benefit from a shorter effective gate length with the HEMT structure at such high bias. Fig. 5 show the pulsed I-V characteristics performed with a quiescent drain voltage ($V_{Q,DS}$) up to 25V at $V_{GS} = +1\text{V}$ (all pulse conditions are described on Fig. 5). For both structures, a low gate-lag and a rather similar drain-lag of about 20% are observed.

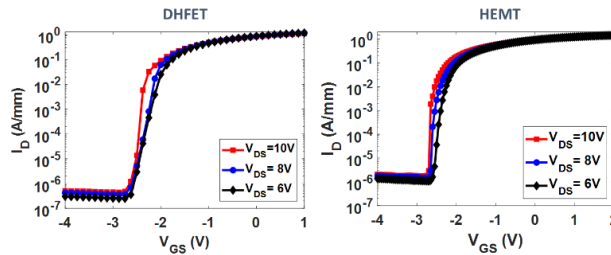
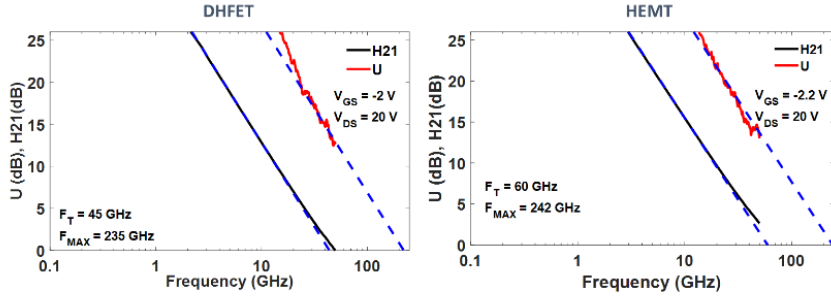
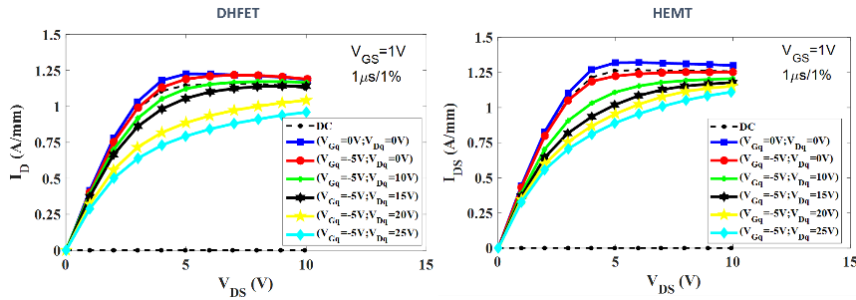


Fig. 3. Transfer characteristics at $V_{DS} = 6, 8, 10$ V of a $2 \times 50 \mu\text{m}$ AlN/GaN DHFET and HEMT.

Fig. 4. RF performance of a $2 \times 50 \mu\text{m}$ AlN/GaN DHFET and HEMT.Fig. 5. Pulsed I-V characteristics of a $2 \times 50 \mu\text{m}$ AlN/GaN DHFET and HEMT.

4. LARGE SIGNAL CHARACTERIZATION AT 40 GHZ

Large signal characterizations have been realized on a nonlinear vector network analyzer system (Keysight Network Analyser PNA-X, N5245A-NVNA) capable of on-wafer large signal device characterization up to the Q-band in continuous and pulsed mode. Further details can be found in [24]. On both structures, load-pull measurements have been carried out in pulsed mode ($1 \mu\text{s}$ width and 1% duty cycle). It can be stressed that the same measurement conditions with a drain current density of 100 mA/mm has been used for the HEMTs and DHFETs. Fig. 6 shows the pulsed power performance of a $2 \times 25 \mu\text{m}$ AlN/GaN HEMT at 40 GHz with $V_{DS} = 15\text{V}$, 20V , and 25V . The rather low gain is due to the biasing conditions in deep class AB. A high saturated P_{OUT} of 7 W/mm was achieved with a peak PAE of 52% (corresponding to a drain efficiency of 74%) associated to a linear power gain above 8 dB. Furthermore, at $V_{DS} = 10\text{V}$ a PAE as high as 56% (corresponding to a drain efficiency of 75%) combined with an output power density of 1.6 W/mm have been reached. Similarly, the pulsed power performance of a $2 \times 25 \mu\text{m}$ DHFET structure at 40 GHz is shown in Fig. 7. The output power density evolves linearly as a function of the drain bias (see Figure 8) up to $V_{DS} = 25\text{V}$ for both structures reflecting the high material quality and associated processing. It is worth noting that the HEMT structure shows the ability to deliver a PAE above 50% up to $V_{DS} = 25\text{V}$.

For the DHFET, an increasing evolution of the PAE up to $V_{DS} = 20\text{V}$ is observed, reaching more than 45% associated to an output power density of 5.1 W/mm at $V_{DS} = 20\text{V}$.

Nevertheless, at $V_{DS} = 25V$ a strong degradation is observed with a PAE decreasing to 35%. It can be noticed that no device degradation (Fig. 9) is observed in both cases (such as an eventual gate leakage current increase) subsequent to the number of pulsed power sweeps. Thus, the significant drop of the PAE at $V_{DS} = 25V$ is attributed to the self-heating, despite the pulsed mode. In turn, the $1\mu s$ pulse width is large enough to allow the increase of the junction temperature at such a high voltage within the DHFET structure. As can be seen from the benchmark in Fig. 10, the achieved PAE / P_{OUT} combination at 40 GHz compares favorably to the state-of-the-art, especially for power densities above 5 W/mm.

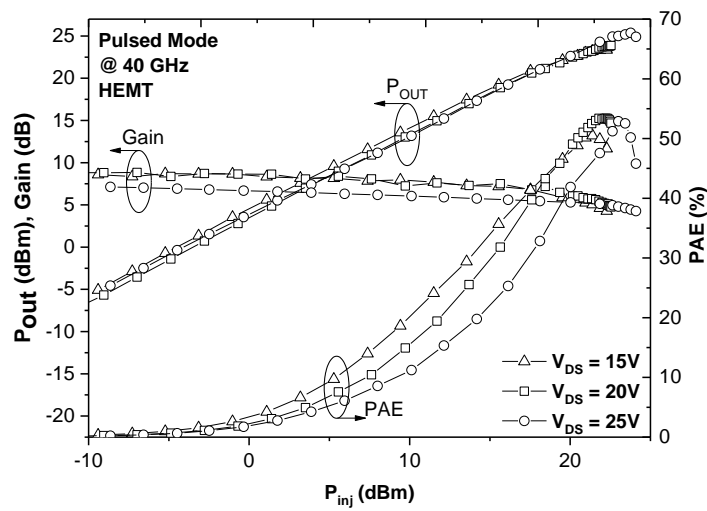


Fig. 6. Pulsed power performance of a $2 \times 25 \mu\text{m}$ AlN/GaN HEMT at 40 GHz with $V_{DS} = 15, 20, 25V$.

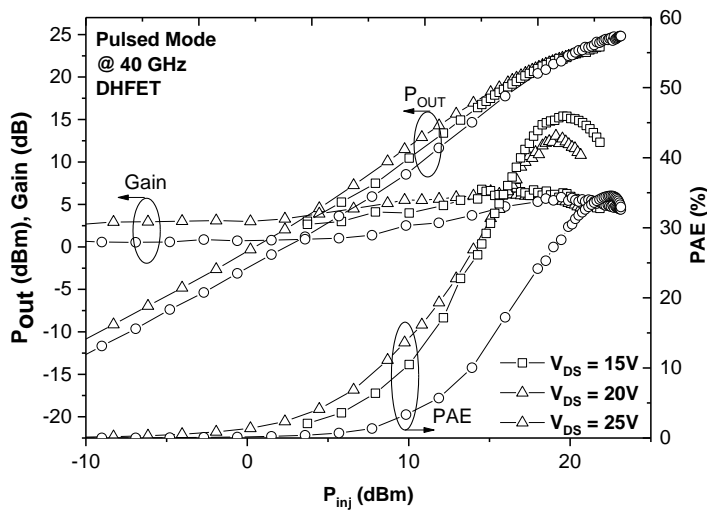


Fig. 7. Pulsed power performance of a $2 \times 25 \mu\text{m}$ AlN/GaN DHFET at 40 GHz with $V_{DS} = 15, 20, 25V$.

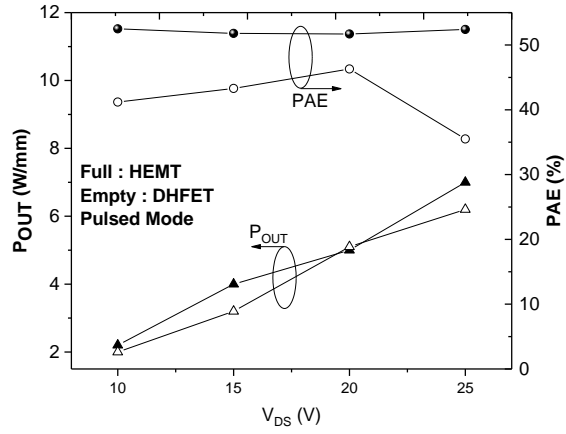


Fig. 8. Pulsed output power density (triangle) and PAE (circle) of both structures versus V_{DS} at 40 GHz.

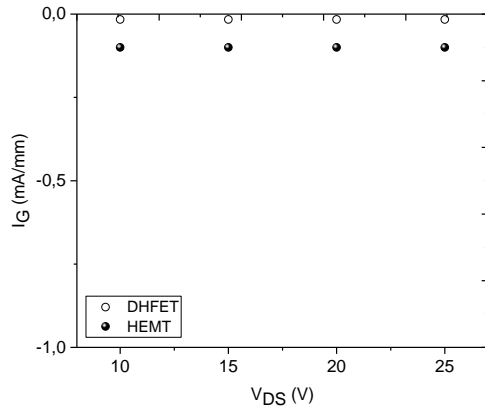


Fig. 9 Evolution of the gate leakage for the HEMTs (filled) and DHFETs (empty) at 40 GHz.

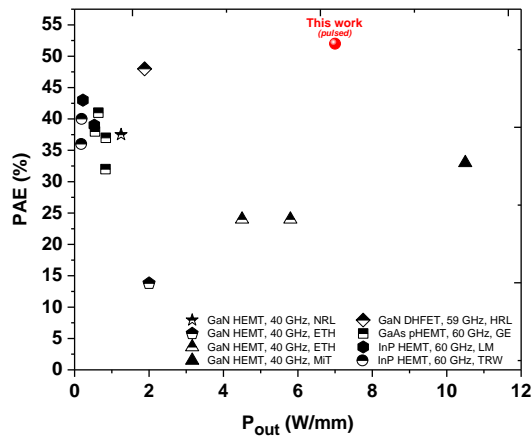


Fig. 10. Benchmark of peak PAE vs output RF power density for Q and V band [12], [15], [25]-[30].

5. RAMAN THERMOGRAPHY MEASUREMENT

The performance enhancement observed on the carbon-doped GaN HEMTs was attributed to a better thermal dissipation. To verify this statement, we assessed the channel temperature of these devices using Raman thermography [31]-[35]. These measurements were carried out on same dimensions $2 \times 50 \mu\text{m}$ DHFET and HEMT GaN/SiC devices. Thermal shift of E_g Raman peak of TiO_2 nanoparticles (NP) [36] deposited on the device surface, with respect to a reference value at the device pinch-off, was used to determine device surface temperature. This was measured by confocal Renishaw InVia Raman microscope in backscattering configuration under 488 nm laser excitation. A schematic representation of Raman TiO_2 NP temperature measurement location, on top of the passivation at the drain edge of the gate is displayed in Fig. 11. A finite elements steady-state thermal model (Fig. 12) was subsequently calibrated with the measured surface temperature data and used for the junction temperature (T_J) extraction.

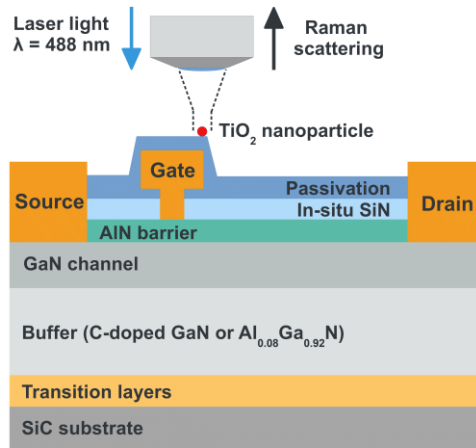


Fig. 11. Schematic representation of Raman TiO_2 NP temperature measurement.

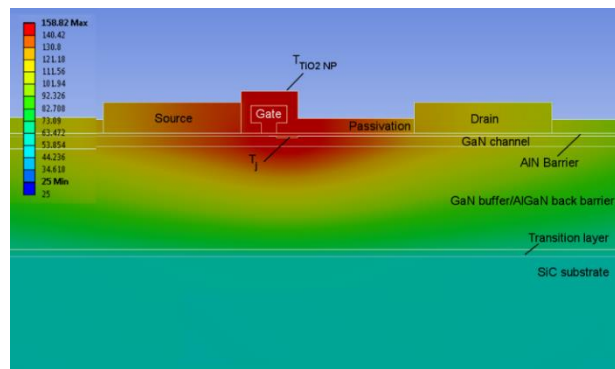
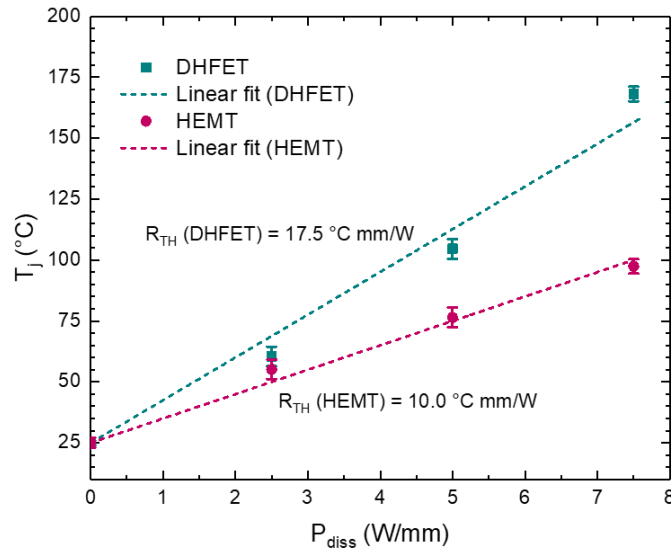


Fig. 12. Device thermal modeling fitted to the experimental data.

The determined peak junction temperatures are shown in Fig. 13. We note that the temperature rise difference between $T_{\text{TiO}_2 \text{ NP}}$ and T_J was $\sim 3.5\%$ and $\sim 5.5\%$ for the DHFET

and the HEMT, respectively as the device surface is close to the highest temperature location in the device. As expected, the DHFET reached much higher T_J (approaching ~60%) than the HEMT for $P_{\text{diss}} > 5$ W/mm. The thermal resistance $R_{\text{TH}} = \Delta T/P_{\text{diss}}$ was extracted from the slope of fitted trend lines of T_J vs P_{diss} . Overall, the results showed that R_{TH} of the HEMT (10°C mm/W) was ~43% lower as compared to the DHFET (17.5°C mm/W) and comparable to reported values of GaN on SiC devices of similar dimensions [37], confirming the results we obtained from the electrical measurements.



	DHFET				HEMT			
	I_D (mA) @ $V_{DS} = 10V$	0	25	50	75	0	25	50
T_J (°C)	25	69.6	114.2	158.8	25	49.9	74.9	99.8

Fig. 13. Peak channel temperature of the HEMTs and DHFETs as a function of the dissipated power density.

The table specifies the current used for each extracted junction temperature.

6. Conclusion

This work shows that a careful architecture of buffer layers should be employed in order to perform high performance millimeter-wave GaN devices. The use of higher bias operation ($V_{DS} \geq 20$ V) is possible when using deep sub-micrometer gate lengths only if the thermal resistance induced by the buffer layers is reduced. In particular, it is shown that a thick AlGaN back barrier (DHFET structure) with 8% Al into the buffer results in a significant drop of the PAE at $V_{DS} > 20V$ even in pulsed mode. This is illustrated by a much higher thermal resistance (obtained by Raman Thermography measurements) as compared to the HEMT structure. The optimized AlN/GaN HEMT structure enabled to deliver a state-of-the-art combination of PAE (> 50%) and an output power density of 7 W/mm at 40 GHz and $V_{DS} = 25V$.

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