Advances in Radio Science (2003) 1: 219–221

Advances in Radio Science

Organic Field-Effect-Transistors with Pentacene for radio-controlled-price-tag applications

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Abstract. This letter presents organic thin-film-transistors (OTFT) using the small organic molecule Pentacene targeting applications like radio controlled identification tags. Simple OTFTs as well as inverter circuits based on a p-conducting silicon wafer substrate are presented. Comparing PECVD oxide and LTO as dielectric, only LTO deposited layers provide sufficient electrical stability. PECVD oxides show defects called "pin-holes", leading to short circuiting through the gate dielectrics. OTFTs of L=1 μm/W=1000 μm were prepared providing I_{ds} = 61 μA at $-40\,V_{ds}$ and $-40\,V_{gs}$, a subthreshold slope of 10.3 V/dec and an on-off-ratio of 10^2. The inverter circuits using insulated gate contacts switch from V_A=-10 V to V_A=-3 V output voltage when the input voltage is varied from V_E=0 V to V_E=-8 V at a supplied voltage of V_B=-10 V.

1 Introduction

Low cost and mass production ability are two of the main advantages of organic semiconducting materials, represented by the small molecule Pentacene (see Fig. 1), in electronic devices like the organic thin film transistor (OTFT). Technological applications like smart cards for health service or credit cards, single use flexible RF identification tags for baggage control at airports are predicted to be realised by "all-organic-electronic" in the near future. The performance of OTFTs made of p-conducting Pentacene has been improved significantly in the last years achieving now up to 2.2 cm^2/Vs charge carrier mobility (Gundlach et al., 1999), transistor switching rates in the upper kHz region (Klauk et al., 1999a; Klauk et al, 1999b) and on/off ratios up to 8 orders of magnitude (Brown et al., 1995; Wu et al., 1997).

This letter presents a simple type of gate-addressable OTFT (see Fig. 2a), based on silicon wafer substrates using well established UV contact photolithography for defining the structures in the photoresist whereas lift-off and wet-chemical-etching were applied to form the contacts. The gate length was varied between 1–10 μm for single transistors. Additionally, inverter structures are presented, using a layout with respect to a self-blocking transistor behaviour.

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2 Preparation

Starting with 100 mm p-type silicon wafers, a 300 nm thick silicon-oxide layer was grown thermally to insulate the gate-contacts from the conducting wafer material. On this field oxide, the gate contacts were formed by sputtering of 100 nm Ti in high vacuum and wet-chemical etching with a UV-photolithography patterned photo-resist as the mask layer. The gate-oxide was deposited by plasma enhanced chemical vapour deposition (PECVD) or low temperature oxide (LTO) at 410°C up to a thickness of 150 nm for sufficient electrical insulation but high field effect quality. The contact holes through the gate-oxide to the gate-metal where defined by contact lithography and transferred into the oxide by wet etching in a buffered HF solution, followed by resist stripping in an O_2-plasma and standard cleaning as similarly applied after each lithographical step. A last UV-contact-photolithography step was applied to form the metal-wires.

Previously published results predicted optimal adhesion and electrical parameters for a laminated system of a Ni adhesion promotion layer below the Au conducting layer (Pannemann et al., 2003). Both were deposited by DC sputtering with Ar and structured by lift-off technique with acetone in ultrasonic agitation. Using the lift-off technique, SEM investigations revealed sharp contact edges providing a smooth surface for good electrical connection to the Pentacene. All test devices were coated with Pentacene used as received from the supplier (Aldrich). Thermal evaporation in high vacuum ambient at 6×10^{-7} mbar on the preheated substrate (60°C) ensured a high quality of the Pentacene film. The deposition rate was adjusted to 0.1 nm/sec, and the total Pentacene layer thickness varied between 40–80 nm within

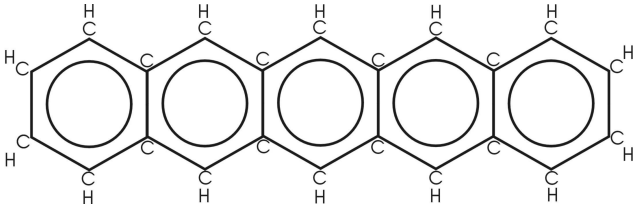

Fig. 1. Schematic structure of the p-conducting organic semiconductor Pentacene.

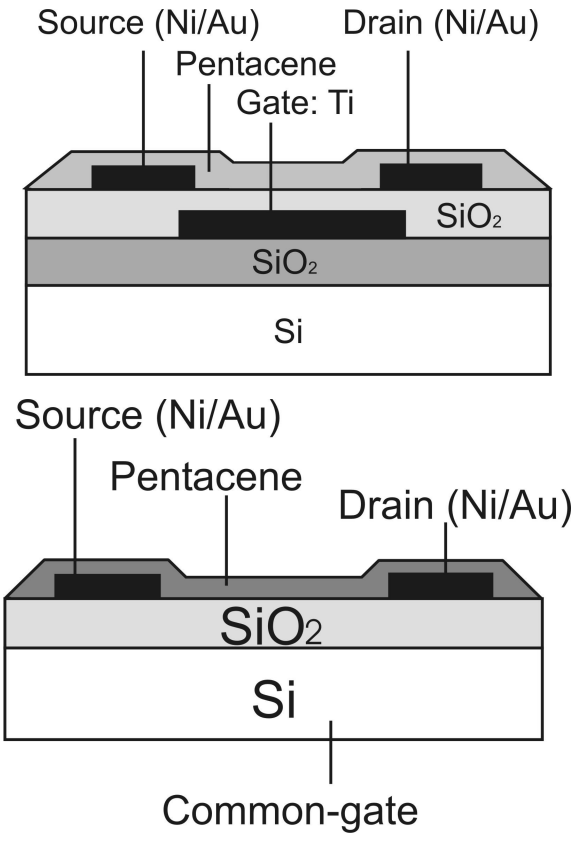

Fig. 2. (a) Insulated gate OTFT on 100 mm silicon wafer substrate, using a PECVD oxide or LTO gate-dielectric of 150 nm thickness. **(b)** OTFT using the p-type silicon substrate as common gate, used for single transistor experiments only.

one series of preparation. Finally, the electrical characterisation of the inverter circuits was carried out using a HP 4156A Semiconductor parameter analyser while the sample was kept in a shielded metal box.

A second slightly different type of sample layout was used to understand the influence of preparation parameters and to prove the simple transistor functions (see Fig. 2b). In this case the silicon substrate was addressed as a common gate of all transistors on the wafer measuring the single test OTFTs. The preparation differed only in skipping the preparation step of the addressable gate-contact. As only one transistor at the time was measured, there was no disturbing interaction of neighbouring transistors.

3 Experimental

First experiments were carried out on single testing structures as described last in the preparation process. On-currents up to 61 μA at $-40\,V_{gs}$ and $-40\,V_{ds}$ were measured for an OTFT of 1 μm gate length and 1000 μm gate width (see Fig. 3a). The subthreshold slope was 10.3 V/dec (see Fig. 3b) and the on-off-ratio limits in the range of 10^2 referred to an undefined off-state leakage current through the gate-dielectrics. Varying the gate area, a charge carrier mobility of 0.1 cm^2/Vs was achieved for a transistor of L=10 μm/W=10 μm. In different preparation cycles, positive as well as negative values of threshold voltages near 0 V were detected. The measurements revealed that enhancement mode transistor operation seems to coincide with high Pentacene film quality. Atomic force microscopy inspections of the organic film surface confirmed grains with diameters up to 250 nm for films of Pentacene corresponding to OTFTs providing good electrical properties (see Fig. 4).

Preparing the OTFTs for inverter circuits, PECVD and LTO insulating layers were compared. As the previously structured Ti-gate should not be affected by the formation of the insulating oxide layer, these low temperature deposition processes are recommended. OTFTs proceeded with PECVD insulating layers show a high leakage current through the gate oxide, attributed to "pin-holes" generating a short circuit between the gate- and the drain/source-contacts. The origin of these defects was determined in structural damage of the formation within the growing process of the oxide. LTO insulating layers provide high structural and electrical quality, resulting in a low leakage current combined with an optimized deposition temperature. Figure 5 shows the characteristic of an inverter with LTO insulating layer and L=20 μm/W=127 μm for the load-OTFT and L=10 μm/W=100 μm for the driver-OTFT. At a supply voltage of V_B=-10 V, the inverter's output voltage switches from V_A=-10 V to V_A=-3 V when the input voltage is varied from V_E=0 V to V_E=-8 V. With some resuming improvements, ring-oscillators can be realised, and future experiments will focus on measuring the switching frequency e.g..

4 Conclusion

This letter presents Pentacene OTFTs providing I_{ds} = 61 μA at $-40\,V_{ds}$ and $-40\,V_{gs}$, a subthreshold slope of 10.3 V/dec and an on-off-ratio of up to 10^2. Positive as well as negative threshold voltages were measured, depending of the Pentacene film quality. The grain size in our Pentacene crystals was determined to a diameter of 250 nm resulting in a charge carrier mobility of up to 0.1 cm^2/Vs. OTFTs with a PECVD insulating oxide layer showed high leakage currents attributed to "pin-hole" defects in the formation of the oxide layer. High quality LTO deposited films with low leakage current were used to prepare inverter circuits, switching at a supply voltage of V_B=-10 V from V_A=-10 V to V_A=-3 V in output voltage varying the input voltage between V_E=0 V

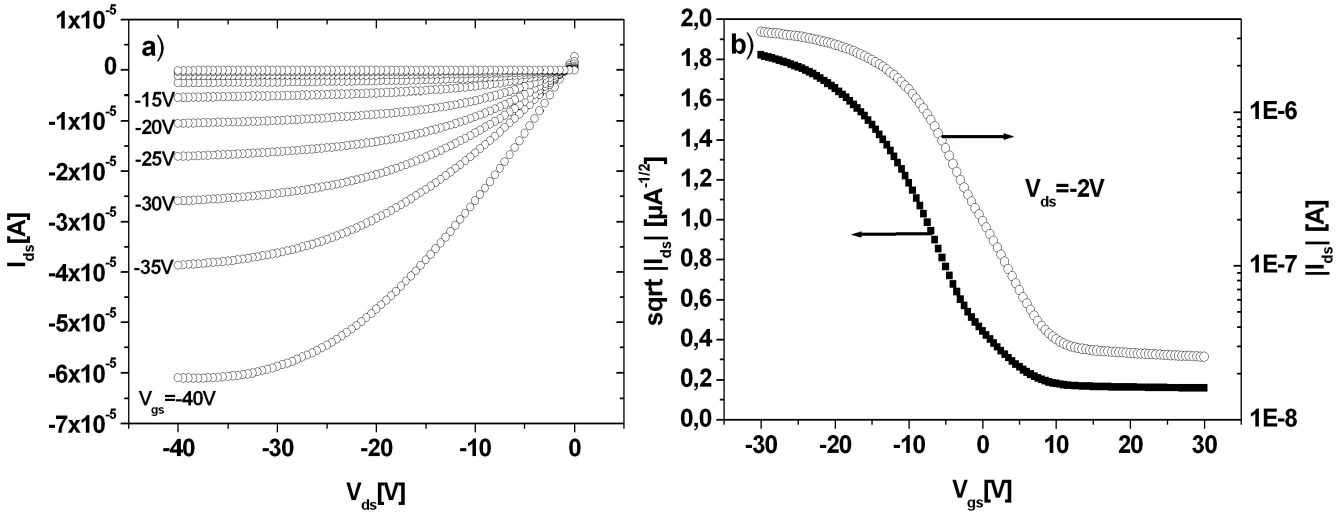

Fig. 3. **(a)** V_{ds}- I_{ds} characteristics, and **(b)** V_{gs}-sqrt (I_{ds}) / V_{gs}-I_{ds} characteristics of a 58 nm Pentacene OTFT (L=1 μm/W=1000 μm) providing Ni-Au-contacts, prepared at 6×10^{-7} mbar on a 60°C substrate.

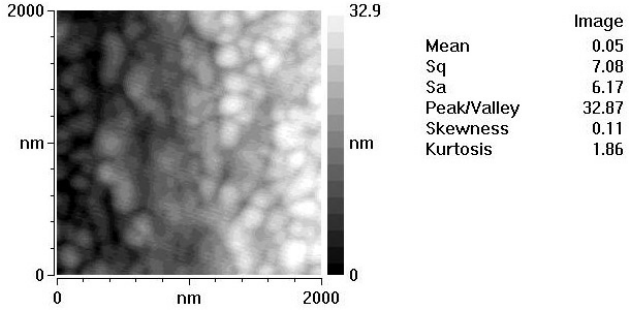

Fig. 4. Atomic force microscopy (non contact mode): Surface of a layer of 80 nm Pentacene, thermally evaporated on SiO_2 showing grain sizes about 250 nm.

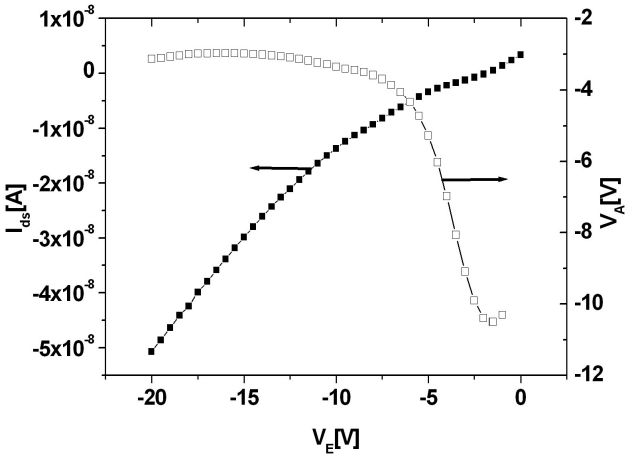

Fig. 5. V_E–I_{ds} / V_E–V_A characteristics of a 60 nm Pentacene inverter circuit (load OTFT: L=20 μm/W=127 μm, drive OTFT: L=10 μm/W=100 μm) providing Ni-Au-contacts, prepared at 5.7×10^{-7} mbar on a 60°C substrate.

and V_E=−8 V. With this, future experiments will focus on building ring-oscillators facing the target of realising radio-controlled-identification-tags.

Acknowledgements. The authors acknowledge W. Büttner, M. Dierkes, H. Funke, R. Otterbach and the staff of the University of Paderborn around H. S. Kitzerow. Financial support was supplied by German DFG (Hi551/7-1).

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