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Simulation and Optimisation of SiGe MOSFETs

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纪念我敬爱的父亲，
并献给我的母亲和妻子。

In the loving memory of my father

Quan Yin Zhao

To my mother **Gui Zhi Wang** *and my wife* **Li Cui**

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ABSTRACT

This research project is concerned with the development of methodology for simulating advanced SiGe MOSFETs using commercial simulators, the calibration of simulators against higher level Monte Carlo simulation results and real device measurements, and the application of simulation tools in the design of next generation p-channel devices.

The methodology for the modelling and simulation of SiGe MOSFET devices is outlined. There are many simulation approaches widely used to simulate SiGe devices, such as Monte Carlo, hydrodynamic, energy transport, and drift diffusion. Different numerical techniques including finite difference, finite box and finite element methods, may be used in the simulators.

The $Si_{0.8}Ge_{0.2}$ p-MOSFETs fabricated especially for high-field transport studies and the $Si_{0.64}Ge_{0.36}$ p-channel MOSFETs fabricated at Warwick and Southampton Universities with a CMOS compatible process in varying gate lengths were calibrated and investigated. Enhanced low field mobility in SiGe layers compared to Si control devices was observed. The results indicated that the potential of velocity overshoot effects for SiGe p-MOSFETs was considerably higher than Si counterparts, promising higher performance in the former at equal gate lengths at ultra-small devices.

The effects of punchthrough stopper, undoped buffers and delta doping for SiGe p-MOSFETs were analysed systematically. It was found that the threshold voltage roll off might be reduced considerably by using an appropriate punchthrough stopper. In order to adjust the threshold voltage for digital CMOS applications, p-type delta doping was required for n^+-polysilicon gate p-MOSFET. The use of delta doping made the threshold voltage roll off a more serious issue, therefore delta doping should be used with caution.

The two-dimensional process simulator TSUPREM-4 and the two-dimensional device simulator MEDICI were employed to optimise and design Si/SiGe hybrid CMOS. The output of TSUPREM-4 was transferred automatically to the MEDICI device

simulator. This made the simulation results more realistic. For devices at small gate length, lightly doped drain (LDD) structures were required. They would decrease the lateral subdiffusion and allow threshold voltage roll off to be minimised. These structures, however, would generally reduce drain current due to an increase in the series resistance of the drain region. Further consideration must be made of these trade-offs.

Comparison between drift diffusion and hydrodynamic simulation results for SiGe p-MOSFETs were presented for the first time, with transport parameters extracted from our in-house full-band hole Monte Carlo transport simulator. It was shown that while drift diffusion and hydrodynamic simulations provided a reasonable estimation of the *I-V* characteristics for Si devices, the same could not be said for aggressively scaled SiGe devices. The resulting high fields at the source end of the devices meant that non-equilibrium transport effects were significant. Therefore for holes, models based on an isotropic carrier temperature were no longer appropriate, as it was shown by analysing the tensor components of the carrier temperature obtained from Monte Carlo simulation.

Two-dimensional drift diffusion and Monte Carlo simulations of well-tempered Si p-MOSFETs with gate lengths of 25 and 50 nm were performed. By comparing Monte Carlo simulations with carefully calibrated drift diffusion results, it was found that non-equilibrium transport was important for understanding the high current device characteristics in sub 0.1 μm p-MOSFETs. The well-tempered devices showed better characteristics than the conventional SiGe devices. Both threshold voltage roll off and the subthreshold slope were acceptable although the effective channel length of this device was reduced from 50 nm to 25 nm. In order to adjust the threshold voltage for the digital CMOS applications, p-type delta doping was used for 50 nm well-tempered SiGe p-MOSFETs. As the delta doping made the threshold voltage roll off too serious, it was not suitable for 25 nm well-tempered SiGe p-MOSFETs.

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CHAPTER 1

Introduction

1.1 Silicon-Germanium

Since the 1970's, silicon integrated circuits have penetrated into almost everything with electrical components. The reason that silicon has over 95% of the microelectronics market is that Si devices have the combination of a cheap semiconductor and an excellent oxide-SiO_2. The properties of the Si/SiO_2 material system make it ideally suited for digital applications with a very high level of complexity. However, a variety of fast-growing markets, especially in the areas of high-frequency analogue applications, appear to be outside the scope covered by the electronic and optoelectronic properties of Si.

Although properly designed III-V heterostructures can excel in almost every category of electronic and optoelectronic properties, they lack an insulator with high quality and versatility required for VLSI technology. In this respect, the Si/SiGe heterosystem is a much better suited alternative, which has the advantages of both Si and III-V devices. Si/SiGe strained layers can be utilised as conduction channels in otherwise traditional MOSFETs, resulting in so-called hetero-MOSFETs. Referring to the experiences gained with III-V MODFETs, the advantages a hetero-MOSFET can offer are obvious: at room temperature the carrier mobility can be increased by a factor of two to three by employing the band offset at the Si/SiGe heterojunction to spatially separate the mobile carriers from the ionised dopants on the one side, and from the interface with the SiO_2 insulator on the other side. This will provide the hetero-MOSFET with higher operating frequencies without sacrificing its intrinsic VLSI ability. In addition, a Si/SiGe MOSFET has the properties of low noise and high linearity. As a newer semiconductor device, SiGe one is expected to play a more important role in microelectronic field.

1.2 The Role of Device Modelling

A semiconductor device is characterised by a set of physical parameters, e.g., mobility, lifetime, as well as technological parameters like geometry, impurity profile, and so on. The aim of device modelling is to provide deep insight, to forecast the future, to design the next generation devices and to optimise existing ones.

Device modelling begins with well characterised process models, which translate specific process conditions into resulting device structures and properties. These structures then translate directly into device parameter inputs to physical device models which can simulate the field and current distributions in the device and determine the terminal characteristics. Finally the terminal characteristics can be interpreted into CAD level models which are used in circuit simulators to design and predict the performance of the finished analogue or digital modules.

It is very important today to get things "right first time" particularly in the semiconductor field. A single mistake in the design of a circuit mask set, or the incorrect specification of an epitaxial growth sequence can cost a lot of money in process and engineering, with many months delay. In the development phase of a process, each run is very expensive and each change to a process may involve a new mask design, procurement of fresh material and, in extreme cases, investment in expensive a new processing equipment. Getting the design wrong in manufacture and having to develop processes by multiple runs, adds up to high costs and unacceptable delay. Device modelling offers the opportunity to reduce process iterations, understand what the critical design areas are and reduce development times and costs.

Device modelling is extremely important for SiGe devices. This is because not only there are more parameters to be optimised for SiGe devices than Si devices, but also there is less experimental data for SiGe since it is a new material. Monte Carlo simulations can be used to provide many transport parameters, e. g., mobility, relaxation time, carrier drift velocity and carrier energy. Monte Carlo simulations can also be used to analyse the strain and non-equilibrium effects in SiGe devices. Drift diffusion simulations

may be helpful in investigating the scaling potential of Si/SiGe devices in the MOSFET context.

In short, device modelling is playing an ever increasing important role in semiconductor industry, which is developing next generation devices and understanding how complex devices work.

1.3 About This Project

This PhD program is linked to the EPSRC project "SiGe for MOS Technologies" involving the Universities of Glasgow, Loughborough, Newcastle, Southampton, Warwick and Imperial College. The principal objective of the initiative is to evaluate the performance enhancements accessible through incorporation of epitaxial SiGe into MOSFET devices, thereby delivering simple demonstrator CMOS circuits with significantly superior performance to that in conventional silicon. The Device Modelling Group of the University of Glasgow plays a pivotal role in the program, impinging on all activities, providing critical inputs and steering the device development. The work of the group comprises investigation, development and application of both SiGe n-MOSFET and p-MOSFET devices.

The aim of this project is to develop the methodology of simulation for advanced SiGe p-channel MOSFETs using commercial simulators, to calibrate the simulators against higher level Monte Carlo simulation results and real device measurements, and to use the simulation tools in the design of next generation p-channel devices.

The main objectives in the calibration of the simulation tools include: Parameter extraction; calibration of the MEDICI hydrodynamic simulations of short p-channel SiGe MOSFETs against the results of Monte Carlo (MC) simulation; calibration of the MEDICI drift diffusion simulations against both hydrodynamic MEDICI simulations and MC simulations; calibration of the drift diffusion MEDICI simulations against relatively long channel SiGe MOSFETs at the earlier stage of the program; at a later stage of the

program calibration of MEDICI against short p-channel SiGe MOSFETs fabricated and characterised by the partner groups.

In the context of device design the project is focused on the following objectives: Optimisation of the spacer between the channel and the gate oxide in order to avoid or delay the appearance of the parallel conducting channel adjacent to the SiO_2 interface; effective threshold voltage control using a delta doped layer introduced in the epitaxial growth; design of a punchthrough stopper to avoid the drain induced barrier lowering (DIBL) effect; optimisation of the buffer between the punchthrough stopper and the channel.

1.4 Thesis Outline

In Chapter 2, basic SiGe properties and SiGe device architectures are introduced. The state of the art for p-channel SiGe MOSFET is reviewed.

In Chapter 3, the methodology for SiGe device simulations is presented. The complete hierarchy of approaches that can be applied to device simulation is also assessed, including quantum approaches, Boltzmann transport equation, Monte Carlo approaches, hydrodynamic and energy transport approaches, drift diffusion approaches and compact approaches. The numerical techniques are also described. Finally the commercial simulator-MEDICI is introduced.

In Chapter 4, numerical simulations of $Si_{0.8}Ge_{0.2}$ p-MOSFETs with thick gate oxide and $Si_{0.64}Ge_{0.36}$ p-channel MOSFETs with thin gate oxide are carried out. The range of a traditional drift diffusion simulator is extended by a careful calibration of mobility parameters with respect to measured output characteristics at high longitudinal fields. The accuracy of the calibration scheme is verified against Monte Carlo calibrated hydrodynamic and energy transport models. Additionally, the influence of different cap thickness is investigated using a calibrated drift diffusion model. In the course of the

calibration, the important information about the low and high electric field transport properties within the strained SiGe layers is also obtained.

In Chapter 5, SiGe p-MOSFETs have been designed and optimised, using drift diffusion simulations. Firstly, the vertical layer structure design of SiGe p-MOSFETs is presented, including the choice of gate material, the silicon cap and oxide thickness sensitivity, and the SiGe profile in the channel. Secondly, several important parameters in two dimensional device design of SiGe p-MOSFETs are analysed. Finally, the delta doped SiGe p-MOSFETs are investigated.

In Chapter 6, the two-dimensional process simulator TSUPREM-4 and the two-dimensional device simulator MEDICI are employed to optimise and design Si/SiGe CMOS. The necessary process parameters provided by the partners at Southampton and Warwick Universities are outlined. The output of TSUPREM-4 is transferred automatically to the MEDICI device simulator. This makes the simulation results more realistic.

In Chapter 7, drift diffusion and hydrodynamic simulations for Si and SiGe p-MOSFETs over a variety of channel lengths from 0.5 to 0.1 μm are developed. Monte Carlo model is used to establish confidence limits for the drift diffusion and hydrodynamic models. In addition, the 'well tempered' Si and SiGe p-MOSFETs at gate lengths of 25 and 50 nm are investigated, using calibrated drift diffusion and two dimensional Monte Carlo simulations. The hole non-equilibrium transport effects in Si devices are also studied.

In Chapter 8, the major contributions of this PhD program are summarised. Then further work is suggested.

CHAPTER 2

SiGe for CMOS Applications

2.1 Birth of SiGe Devices

Silicon is unrivalled as a semiconductor material, having dominated the microelectronics market [1, 2]. The dynamic random access memory chip (DRAM) typifies the current state of silicon microelectronics. The 512 Mbit DRAMs are now commercially available using 0.18 μm technology with each chip containing more than 10^8 components. Circuits down to 0.1 μm feature sizes required for Gbit circuitry have been demonstrated [3, 4]. Transistors with switching speeds of 13 ps have also been realised, as has the fabrication of high performance ICs on silicon-on-insulator (SOI) substrates. The combination of field effect transistors (FET) and bipolar device on a single chip (BiCMOS) is now an established technology [5-7].

The most important reason for the unsurpassed success of Si devices lies in the combination of an easily available semiconductor and an excellent oxide-SiO_2 that serves as an insulator and a protecting passivation layer. The combination of Si/SiO_2 technology is the basis for the Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) that can be integrated monolithically in enormous quantities. The chemical and mechanical properties of SiO_2 are as essential as the low density of charged states in the oxide and at the Si interface in very large scale integration technology. These combined properties are the key to the fabrication of several million transistors with identical electrical behaviour on a single chip.

Although a variety of alternative semiconductors are more suitable and useful than Si used in some fields (e.g., optical communication), and several III-V compound semiconductor heterostructures devices (such as the high electron mobility transistor) are

now available commercially, these devices completely lack a native oxide or other insulator with the quality and versatility required for a VLSI technology. The problems associated even with a moderate level of integration density are a fundamental drawback of III-V compound heterotructures devices, which restricts the market volume that can be addressed by these materials. Hence, one is facing the question is it possible to combine the advantages of the Si/SiO_2 system with its VLSI capability, with the III-V heterostructure where has versatile possibilities for band structure engineering. As a step in this direction, the growth of III-V heterostructures on Si substrates has been proposed and pursued for quite some time [8]. However, despite the successful demonstration of light emitting diodes [9] and FETs fabricated this way, the substantial lattice mismatch and anti-phase boundary in the III-V heterostructure make this a troublesome combination of materials in terms of epitaxial growth and long-term stability of the devices [10].

In the seventies, a new SiGe heterostructure technology emerged. It was much better suited for Si integration heterosystem, and can be considered as a kind of "natural" choice: the two group-IV elements Si and Ge crystallise in the same diamond lattice, and form random $Si_{1-x}Ge_x$ alloys of arbitrary composition. By means of these alloys the band structure can be tuned within the relatively wide margins given by the two elemental semiconductors. In addition, the structural and chemical properties of the two are very similar, which eases epitaxial growth and the application of standard Si technologies, but they still differ enough to allow selective structuring procedures. The obvious advantages of a Si-based all-group-IV heterosystem were recognised at an early stage of heterostructure research, with the first report on an Si/SiGe superlattice appearing back in 1975 [11].

The progress in material growth and basic understanding of the band alignment initially lagged behind similar investigations made in the much more popular, lattice-matched GaAs/AlGaAs heterosystem. There were some problems, such as the lattice mismatch between Si and Ge, the strong segregation of most dopants, and also the growth techniques, e.g. molecular beam epitaxy (MBE), were still in their infancy. However, over the years, most of the growth and doping problems have been solved, and our understanding of the strain effects induced by the lattice mismatch has reached a state that

allows their exploitation as a further parameter in the field of man-engineered band structures.

At present, the Si/SiGe/Si sandwich structure is probably the most promising system found to date for Si compatible heterojunction bipolar transistor (HBT) [12] and one of the major reasons for the intense world-wide interest in SiGe, with demonstrated cut-off frequencies and maximum oscillation frequencies well beyond 100 GHz [13-15]. This is roughly a factor of two improvements as compared to the best existing Si bipolar junction transistors. Far more important is the fact that the Si/SiGe HBTs boost Si-based technologies into an area that has so far been exclusively dominated by III-V devices. Much research has been done on SiGe HBTs in the last years [16-19]. As the most advanced devices in the Si/SiGe heterosystem, HBT products have already been announced, or are expected to be available commercially in the very near future [20]. In addition, a variety of other potential applications are pursued by the ever-increasing number of research groups working in the field of Si-based heterostructures. As an example, optoelectronic functions including infrared detectors [21], waveguides and even light emitting diodes [22], are being investigated actively.

There is another important research area in the studies of SiGe MOSFETs. Since the aforementioned Si-MOSFET is the most widespread of all electronic devices, a successful introduction of the Si/SiGe heterostructure into this mainstream area is expected to have an enormous impact. A proper understanding of the reason behind this impact comes from the importance of the silicon complementary metal-oxide-semiconductor (CMOS) architecture, which is considered to be the primary building block in digital integrated circuits. This is attributed to its low power consumption and mature technology. However, there are some challenges in further scaling of CMOS technology into the nanometer (sub-100 nm) regime in the light of fundamental physical effects and practical considerations, such as lithography, power supply and threshold voltage, short-channel effect, gate oxide, high field effects, dopant number fluctuations and interconnect delays [23]. Furthermore, the hole mobility in Si MOS structures is two to three times lower than the electron mobility. To minimise asymmetric operation in CMOS applications, Si p-MOSFETs are designed with wider gates, thus affecting packing density and device speed. In order to solve these problems, new materials and

device structures have been proposed [23], including silicon-on-insulator (SOI), double-gate MOSFETs and SiGe MOSFETs.

Complementary SiGe MOSFETs can enhance the performance limit of conventional CMOS [24-27]. Due to barrier-confined carrier transport in quantum wells with higher mobility, higher channel velocity and higher carrier concentrations in the channel, one can expect higher transconductances, higher speed, lower gate delay, lower noise and low power consumption [28, 29]. Because of the enhanced hole mobility of SiGe p-MOSFETs, equally sized p- and n-MOSFETs can be designed with higher packing density.

2.2 Basic Properties of Si/SiGe Hetrosystem

Some of the fundamental material properties which influence silicon device operation are the semiconductor band-gap, the effective mass of the carriers, the scattering processes and the electron-hole recombination processes. If some of the Si atoms are replaced with Ge atoms to form layered structures of differing compositions, these fundamental properties can be altered dramatically. Si and Ge are completely miscible over the whole compositional range, giving rise to alloys with a diamond crystal structure. The lattice constants of Si and Ge differ by 4.17%, with Si having the smaller lattice spacing.

The different lattice constant between relaxed SiGe alloy and Si is shown in figure 2.1 (a). When SiGe is deposited on a silicon substrate, the mismatch can be accommodated in two ways: by the formation of dislocations at the interface (figure 2.1 (b)), in which case the alloy is relaxed a short distance from the interface; or by pseudomorphic growth, whereby the alloy is constrained to have the same lattice constant as the substrate in the plane perpendicular to the growth direction (figure 2.1 (c)), and is under biaxial compressive strain perpendicular to the growth direction.

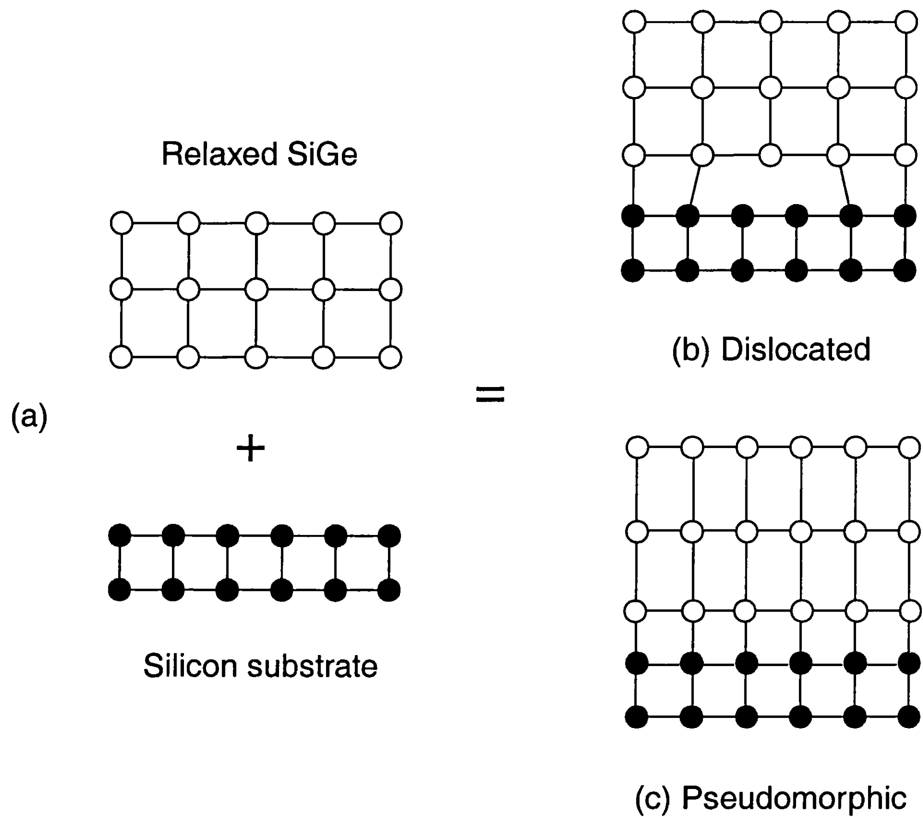


Figure 2.1 A two dimensional representation of pseudomorphic growth. (a) Relaxed SiGe (empty circles) has a larger lattice constant than silicon (filled circles); (b) dislocations at the interface; (c) pseudomorphic growth.

Similarly, when silicon is grown on a SiGe substrate (figure 2.2 (a)), the mismatch can also be accommodated in one of two ways: by the formation of dislocations at the interface (figure 2.2 (b)); or by pseudomorphic growth, whereby the silicon is constrained to have the same lattice constant as the substrate in the plane perpendicular to the growth direction (figure 2.2 (c)), and is under biaxial tensile strain perpendicular to the growth direction.

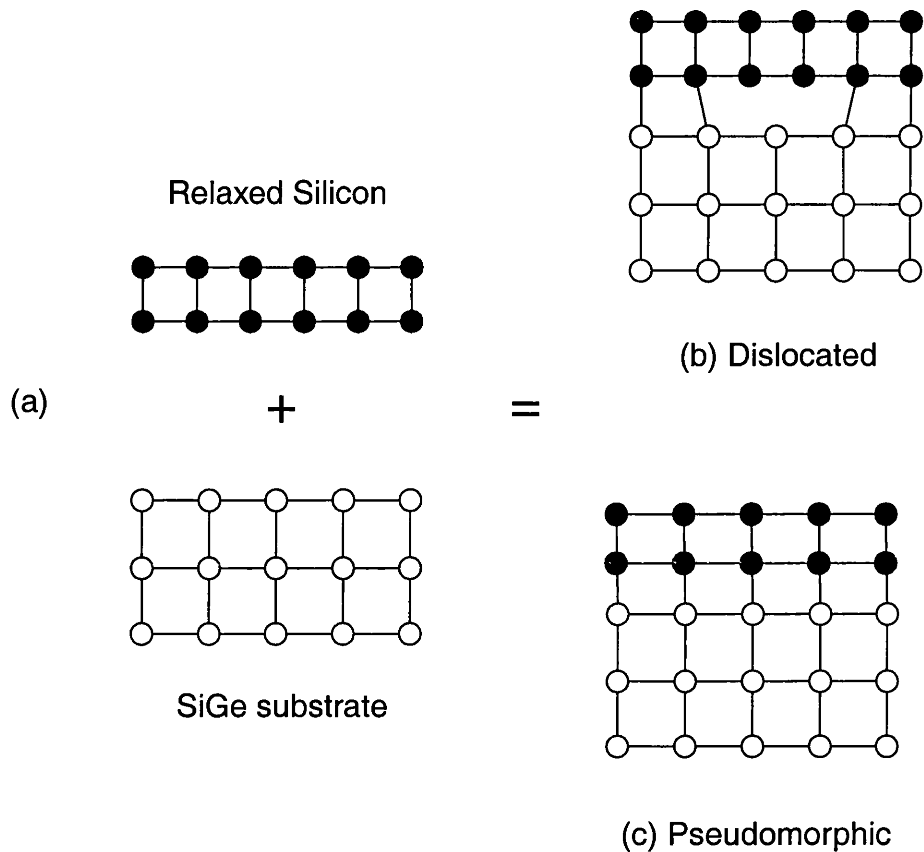


Figure 2.2 A two dimensional representation of pseudomorphic growth. (a) Relaxed SiGe (empty circles) has a larger lattice constant than silicon (filled circles); (b) dislocations at the interface; (c) pseudomorphic growth.

Interface dislocations are highly undesirable in a device because they act as recombination and scattering centres, which degrade carrier mobility and device performance. In contrast, pseudomorphic layers contain few extended crystallographic defects. In addition, the presence of strain has a number of implications for devices. It modifies the alloy bandstructure, affecting the band gap and the electron and hole transport properties.

Carrier mobility improvements using a strained layer come mainly from two sources: a reduction of the in-plane carrier effective mass, and a reduction of inter-valley

scattering. The biaxial compressive strain in SiGe layer perpendicular to the growth direction splits the light and heavy hole bands, with the heavy hole band lying lowest in hole energy, as shown in figure 2.3 (b). This leads to a reduction in the hole effective mass. The strain modified band structure also has other advantages. Firstly, the reduced mass means that the carrier acceleration in the electric field is increased. Secondly, intrasubband scattering is reduced because of the reduction in the density of states. Thirdly, intersubband scattering is suppressed by virtue of the band splitting. With the application of tensile strain, the degeneracy between light and heavy hole bands in Si is lifted too, as shown in figure 2.3 (c). A reduction of the in-plane carrier effective mass and a reduction of inter-valley scattering lead to hole mobility improvement.

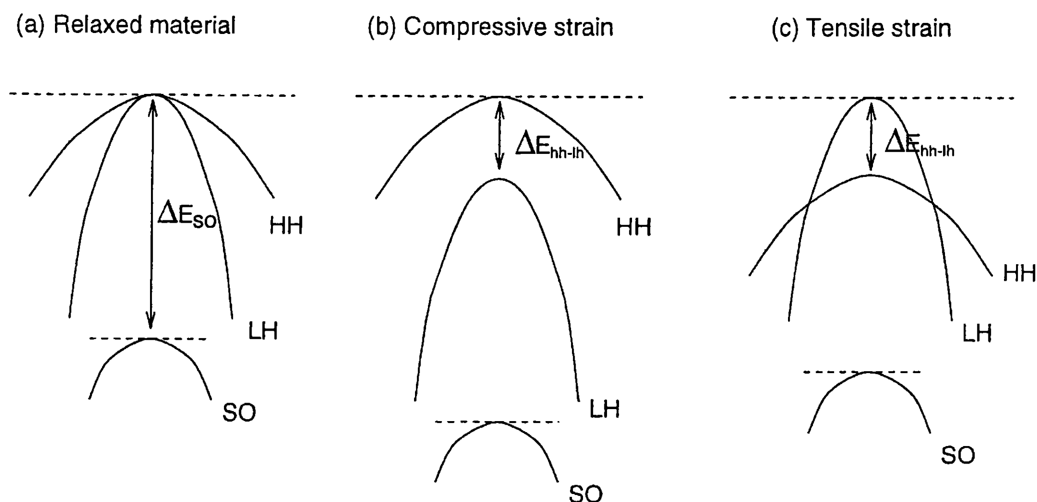


Figure 2.3 The effects on the valence band when the layer subjected to: (a) no strain; (b) compressive strain; and (c) tensile strain.

Changes similar to these happening in the valence band also take place in the conduction band. Once again band-edge degeneracy is broken and effective masses are altered. SiGe remains Si-like in its conduction band features up to 85% Ge, which covers more or less the entire range of practical applications. However, changes in strained Si on SiGe are in opposite directions, due to the opposite sign of strain. Biaxial in-plane tension in Si splits the six-fold degeneracy of the conduction band, as shown in figure 2.4. Two valleys are lowered in energy, and four are raised. This results in reducing the conductivity effective mass and suppressing inter-valley scattering.

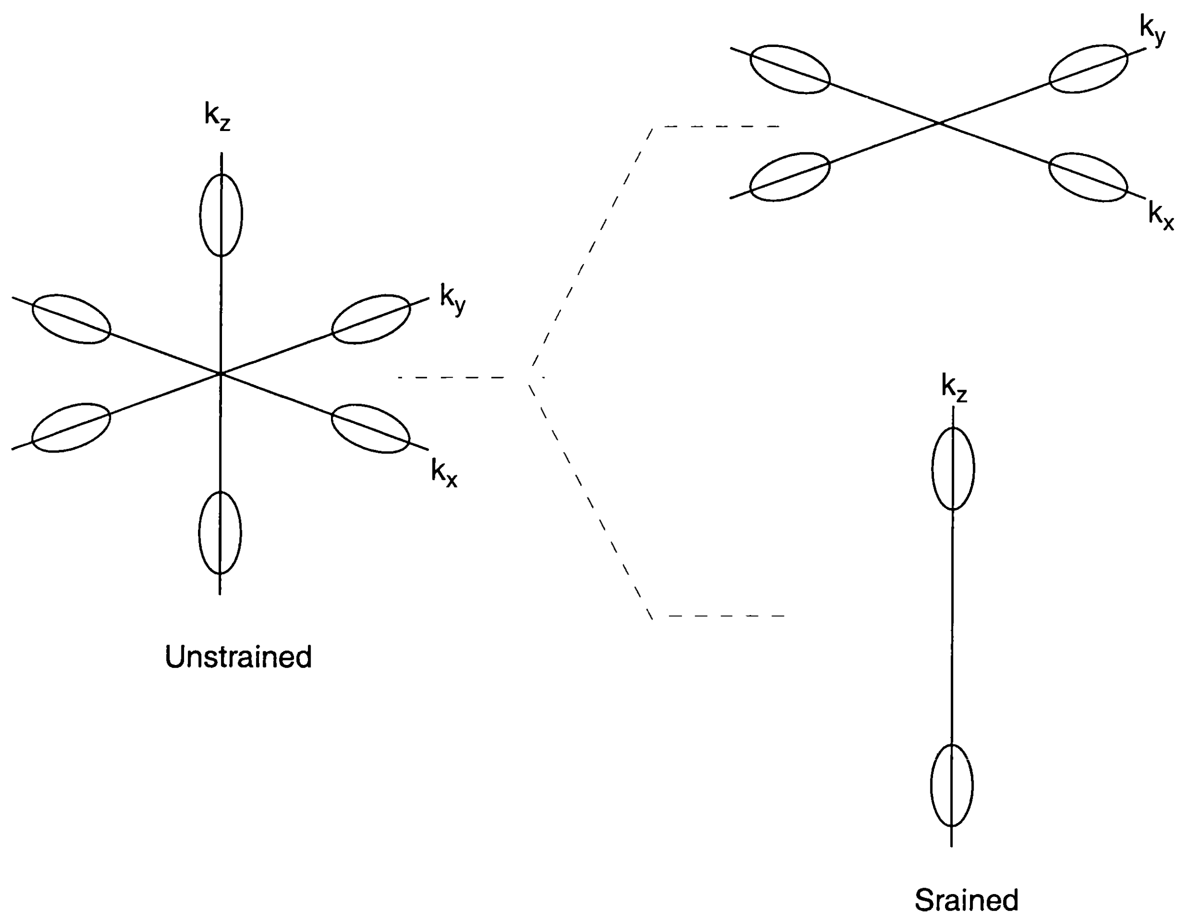


Figure 2.4 Schematic diagram illustrating the energy shift of the six-fold degenerate conduction band in strained silicon on relaxed SiGe.

2.3 SiGe Devices Architectures

The use of SiGe heterostructures has two major categories [30, 31]. In the first case a Si/SiGe/Si sandwich is grown on a silicon substrate to form a "fully coherent" structure in which all layers have the same in-plane lattice spacing as the substrate on which they are grown and in which the SiGe alloy is under biaxial compressive strain perpendicular to the growth direction. Figure 2.5 shows the band offset for a strained SiGe film grown on silicon. This is known as type I band alignment where most of the band offset occurs in the valence band while the band offset in the conduction band is very small. This type of structure is favourable for hole confinement and has been exploited in several novel heterostructure devices, such as buried channel p-MOSFETs,

p-channel modulation-doped field effect transistors (p-MODFETs) and heterojuction bipolar transistors (HBTs).

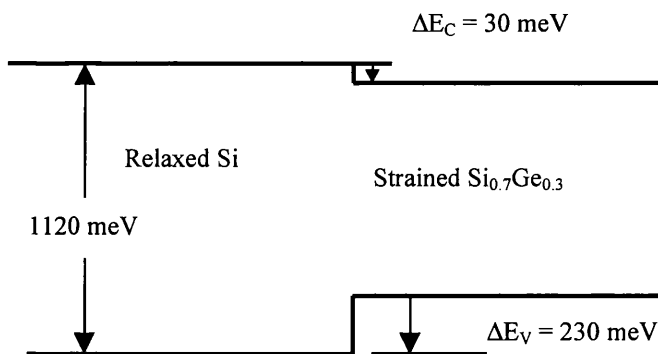


Figure 2.5 Illustration of the band offset between strained $Si_{0.7}Ge_{0.3}$ and relaxed Si.

In the second category a relaxed SiGe buffer layer is grown on a silicon (and sometimes a germanium) wafer to form a "virtual substrate" having a different lattice constant from the wafer. Tensile strained Si layers are then deposited onto this buffer layer. Figure 2.6 shows the band offset for a strained-Si epilayer grown on relaxed SiGe. In this case, a type II band offset occurs and the structure has several advantages over the more common type I band alignment, as a larger band offset is obtained in both the conduction and valence bands, relative to the relaxed SiGe layer. This allows both electron and hole confinements in the strained-Si layer, making it useful for both n- and p-type devices for strained-Si/SiGe-based CMOS technology.

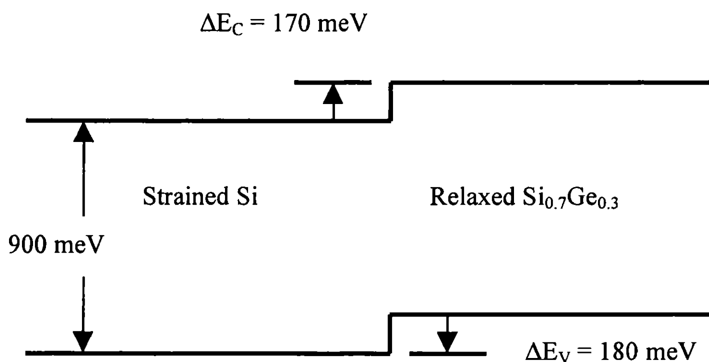


Figure 2.6 Illustration of the band offset between strained Si and relaxed $Si_{0.7}Ge_{0.3}$.

For strained Si on SiGe, the sixfold degeneracy of the conduction band ellipsoids is lifted and twofold and fourfold degenerate ellipsoids are left. The conduction band minimum is located in the doubly degenerate band, the small transverse mass of which leads to a smaller electron effective mass for conduction in the plane of the strained Si layer. The mobility in this plane is enhanced. One benefit of strained Si p-MOS or n-MOS over SiGe p-MOS, is that conduction does not occur in an alloy layer and hence, alloy scattering is eliminated. However, strained Si is more difficult to grow than strained SiGe, since bulk SiGe substrate is currently not available and the growth of relaxed SiGe without forming a large concentration of dislocation is generally a demanding task [32].

2.3.1 Strained Si p-MOSFET

p-MOSFETs can be realised either in pseudomorphic SiGe (type I) or strained Si on virtual substrates (type II). Nayak *et al* [33] have studied low-field hole mobility of strained Si layers on (100) $Si_{1-x}Ge_x$ substrates. It was shown that strain induced change in the valence-band structure results in dramatic improvement in hole mobility. For $x = 0.1$ and 0.2, mobility enhancement factors of 2.4 and 6, respectively, were found. They [34] also presented the operation and fabrication of a new strained-Si p-MOSFET. The hole confinement at the type-II band structure has been demonstrated for the first time by *C-V* and device transconductance measurements. The channel mobility of this device at high vertical field was found to be 40% and 200% higher at 300 K and 77 K, respectively, than that of a similarly processed bulk Si p-MOS.

The strain dependence of the hole mobility in surface-channel p-MOSFETs employing pseudomorphic, strained-Si layers was reported by Rim *et al* [35] for the first time. The measured hole mobility increases roughly linearly with strain, in agreement with published calculations.

A simulation study of a short-channel strained Si p-MOSFET was presented by Armstrong and Maiti [36]. An analytical model for hole mobility enhancement in strained silicon has been used in a two-dimensional device simulator to evaluate the strain dependence of the drain current and transconductance. Simulation results have been verified with experimental device results. The leverage of the strained-Si channel p-

MOSFET over conventional Si p-MOSFETs was shown both at low temperature and room temperature. Optimal confinement of holes within the strained silicon occurs for a graded $Si_{0.7}Ge_{0.3}$ buffer cap thickness of 40 nm. This layer structure gave rise to an enhancement in transconductance of up to 60%.

The hole mobility of p-type strained Si-MOSFETs fabricated on SiGe substrate was investigated theoretically and compared with the mobility of conventional Si p-MOSFETs [37]. Two-dimensional quantisation of the holes was taken into account in terms of a self-consistent six-band $\boldsymbol{k} \bullet \boldsymbol{p}$ model for the strained band structure. For a Ge concentration of 30% in the substrate, a mobility enhancement of a factor of 2.3 compared to the unstrained p-type device has been predicted.

2.3.2 Strained Si n-MOSFET

Strained Si is primarily useful to achieve high electron mobility in n-channel devices. Ismail *et al* [38] reported the growth of n-type modulation-doped Si/SiGe with the doped SiGe supply layer underneath the strained Si channel. A peak room temperature mobility of 2200 cm^2/Vs was measured at a sheet density of 2.5×10^{12} cm^{-2}.

The fabrication and analysis of SiGe based n-channel heterojunction MOSFETs has been reported [39]. Devices having channel lengths between 150 nm and 10 μm have shown good transistor behaviour. An extrinsic transconductance of 220 S/m has been measured, which is a very high reported for an HMOSFET. Another important result obtained in this study is that the use of a high thermal budget during processing did not have a catastrophic effect on the strained Si.

Enhanced performance has been demonstrated in n-MOSFETs with the channel regions formed by pseudomorphic growth of strained Si on relaxed $Si_{1-x}Ge_x$ substrate [40, 41]. Standard MOS fabrication techniques were utilised [42], including thermal oxidation of the strained Si. Strained-Si channel devices showed dramatic low field mobility enhancements both at low temperature [43] and room temperature [44, 45], when compared to conventional Si devices. Yeoh *et al* [46] have used electrochemical anodic oxidation to form gate oxides on strained n-channel Si/SiGe quantum wells. Comparison

of measured and calculated electron sheet densities in the quantum well indicated that the oxide growth did not cause degradation of the Si/SiGe material.

A two-dimensional model of a strained $Si/Si_{1-x}Ge_x$ transistor with delta doped layers was developed in [47]. A semi-classical drift diffusion model was used to study the effects of different conduction-band offsets and variation of distance between the Si channel and an n-type delta doped layer as well as the thickness of this delta doped layer at room temperature. It was found that a large conduction-band offset, or a large Ge concentration, confines electrons more strongly to the Si channel. It was also found that the smaller the distance between the Si channel and the delta doped layer and the thinner the delta doped layer, the larger the number of electrons in the Si channel. Ip and Brews [48] performed a design trade-off study for n-channel delta doped Si/SiGe heterojunction MOSFETs numerical simulation and analysis.

Simulations of n-type SiGe MOSFETs were performed to improve their vertical and lateral design [49]. Position and intensity of the doping was changed at the front side, backside and even inside the 2DEG (Two Dimensional Electron Gas) Si-channel. Sheet carrier concentrations were investigated. A novel structure with a p-type cap is proposed that reduces the threshold in a MOS gated HFET. The effect of the space between doping and 2 DEG was also studied.

Roldan *et al* [50] have studied the performance of superficial strained $Si/Si_{1-x}Ge_x$ channel MOSFETs. They developed a two-dimensional drift diffusion simulator including inversion layer quantization and low field mobility curves obtained by means of a Monte Carlo simulator. They have successfully reproduced experimental results. The dependence of the performance enhancement obtained in these devices on the germanium mole fraction, the drain-source and gate-source voltages were described in depth. They have also investigated electron density and mobility for buried strained-Si/SiGe MOSFETs at different temperature, using Monte Carlo simulations [51].

Rashed *et al* [52] have investigated electron transport in strained-silicon n-MOSFETs using a single particle Monte Carlo simulation tool consistent with the 2D nature of the electron gas. A Monte Carlo simulation has been devised and used to model

steady state and transient electron transport in SiGe n-MODFETs in [53]. The simulated device geometries and doping were matched to the nominal parameters described for the experimental structures as closely as possible, and the predicted *I-V* and transfer characteristics for the intrinsic devices showed fair agreement with the available experimental data.

2.3.3 Other SiGe devices

Recent studies [54-57] on the incorporation of a small amount of Carbon atoms in the Si/SiGe material system to develop new types of buffer layers with reduced misfit dislocations may be useful for fabrication of reliable and thinner virtual substrates (VS). Reduction of growth time for VS can push the cost down too.

Pure Ge-channel modulation-doped field-effect transistors with extremely high transconductance were reported in [58]. Cyca *et al* [59] have fabricated and characterised heterostructure Si/Ge/Si p-metal-oxide-semiconductor field effect transistors with 1-nm-thick pure Ge channels grown pseudomorphically on Si substrates. Since Ge has the smallest hole effective mass of all semiconductors, these devices are important to explore upper limits for hole mobility in MOSFETs.

Choi *et al* [60] introduced a new NMOS electrostatic discharge (ESD) protection transistor which contains a burried SiGe narrow-bandgap layer between the source and the drain region. Said *et al* [61] carried out a detailed analysis of the Si/SiGe heterostructure thin-film solar cell, both on the level of simulation and technical feasibility. Tashiro *et al* [62] have developed a P-I-N SiGe/Si superlattice photodetector with a planar structure for Si-based opto-electronic integrated circuits. Lee *et al* [63] have determined the spectral response and impact ionization coefficient ratio of $Si_{1-x}Ge_x$. Amour and Sturm [64] have showed that a two-carrier electronic device simulator can be used to understand the temperature dependence of photo-luminescence and electro-luminescence in $Si_{1-x}Ge_x$ heterostructures.

The use of polycrystalline SiGe as the gate material for deep submicron CMOS has also been investigated [65]. Houtsma *et al* [66] showed that boron-doped poly-SiGe is a very interesting gate material due to a low stress-induced leakage current and better gate oxide quality.

2.4 SiGe p-MOSFET

Since SiGe p-MOSFETs are the focus of the simulation studies in this thesis, special emphasis will be placed here. The type I band alignment is favourable for hole confinement and has been used for p-MOSFETs, in which the valence band offset ΔE_V between Si and SiGe varies nearly linearly with the Ge concentration. The conduction band offset ΔE_C, in contrast, is so small that it can be negligible at room temperature. The hole mobility in the strained SiGe layer is enhanced by a reduction in the effective hole mass in the longitudinal direction [67]. In addition, the strain induces the separation of the heavy and light hole bands [68, 69] which results in the reduction of inter-band scattering. Both of these effects lead to an increase in the hole mobility. An increase in the percentage of germanium incorporated the SiGe layer results in a further reduction of the hole effective mass [70].

A typical buried SiGe p-channel MOSFET is showed in figure 2.7. The energy band profile of a buried SiGe channel enhancement-mode p-MOSFET is shown in figure 2.8.

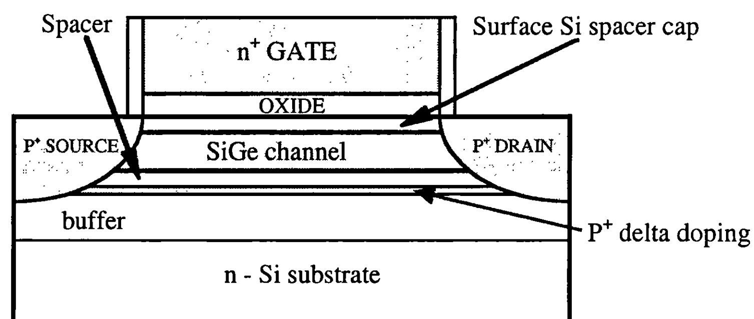


Figure 2.7 Schematic diagram of a typical buried SiGe p-channel MOSFET.

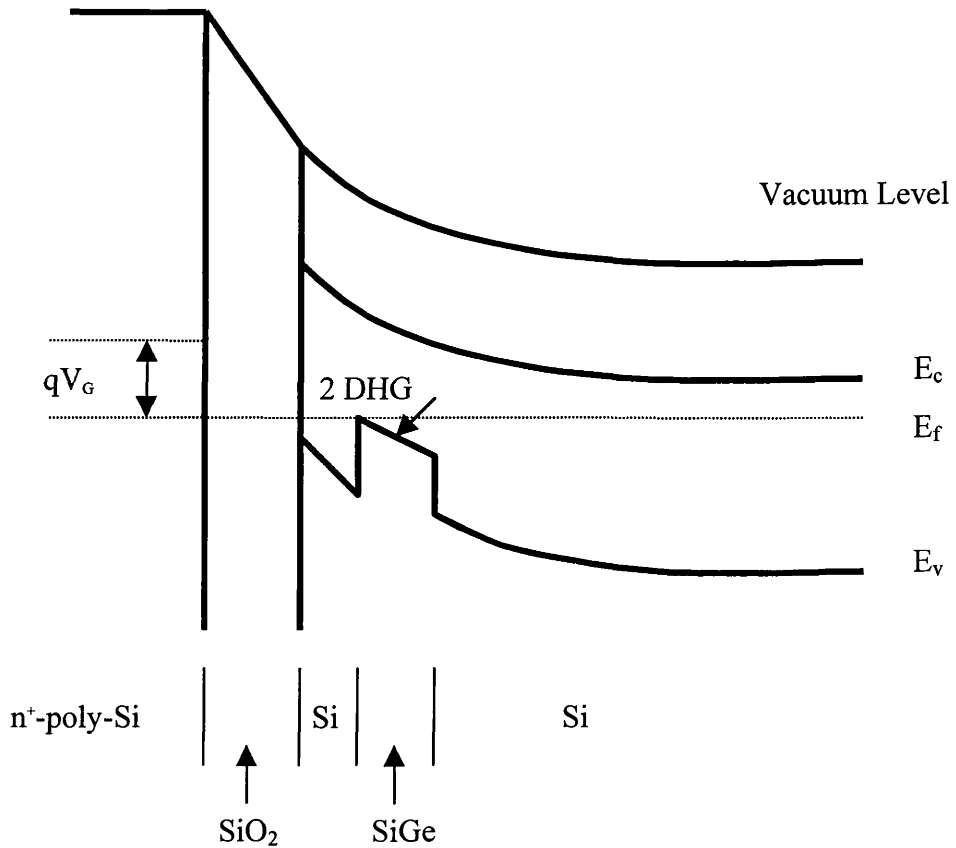


Figure 2.8 Energy band profile of a buried SiGe channel enhancement mode p-MOSFET. 2 DHG denotes two dimensional hole gas.

Incorporation of a buried SiGe layer into a p-MOS structure could lead to improvements in speed and higher packing densities in CMOS circuitry. This strategy would take advantage not only of the band structure of the strained SiGe alloy but also of possibly lower scattering by roughness or charge at the Si/SiGe interface as compared to the Si/SiO_2 interface [1]. It also circumvents the problems associated with the thermal oxidation of SiGe films by utilising the Si cap to form the gate dielectric. Since germanium oxides are not very stable, the thermal oxidation of SiGe results in a pile-up of Ge at the dielectric/SiGe interface with a concurrent increase in the interface state density [71]. The use of a Si cap allows thermal oxidation for the formation of a SiO_2 gate dielectric and greatly reduces interface state density. It might also be possible to reduce the mobility degradation, which is caused by scattering from the gate/SiO_2 interface roughness in the case of very thin oxides, which are prerequisite for short-channel

applications. Another virtue of the SiGe p-MOS structure is that the buried channel would be expected to reduce hot carrier degradation of the oxide. In addition, the increased probability of impact ionisation in the drain region, because of the lower band-gap in the alloy, might provide an energy dissipation mechanism, which would reduce the hot-carrier population [1].

The critical design parameters for SiGe p-MOSFET are the type of gate material, the thickness of Si cap and buffer, the concentration of the buffer and the delta doping, and the Ge mole fraction in the SiGe channel, as well as other parameters of a MOSFET such as oxide thickness and doping extension.

Two major problems have been encountered in trying to realise such a SiGe heterostructure technology that may be integrated in a CMOS production line [72]. The first is that to integrate strained layers into a CMOS line, the structures should be as closely compatible with conventional processing as possible unless the performance gain is so large that increased production costs can be justified. The second problem is that the valence band discontinuity of SiGe to Si is small, especially at low Ge content. With the content being kept low to allow the SiGe layer to be below the critical thickness, parallel conduction can occur in the transistors producing a 2D hole gas at the Si/SiO_2 interface. This parallel conduction significantly reduces the performance of such devices, which are designed to be controlled only by the two dimensional hole gas at the Si/SiGe interface.

2.4.1 Fabrication issues

Work on SiGe p-MOSFET devices has been steadily advancing for several years. The first reported SiGe FET grown on a Si substrate was a p-channel SiGe MODFET with a $TiSi_2$ Schottky-barrier gate contact [73]. Work on practical SiGe p-MOS devices is still in its infancy but shows considerable promise. The highest published low-field mobilities in such a device were around 500 cm^2/Vs at 300 K [74]. Although this is a noteworthy improvement, further progress is still required for a performance as good as a n-MOSFET.

To investigate the theoretical prediction of increased high-field drift velocity, p-channel Quantum Well (QW) MOSFETs were fabricated with $Si/Si_{1-x}Ge_x/Si$ quantum well heterostructures grown by molecular beam epitaxy with varying Ge mole fractions [75]. The fabrication sequence maintained a low thermal budget to prevent strain relaxation in the SiGe layer and involved a mixed optical/electron beam lithography scheme to define junction-isolated transistors with a minimum drawn gate lengths of 200 nm. The measured saturated transconductance of the p-QWMOSFETs were 20-50% higher than that of a reference Si p-MOSFET under equivalent biasing conditions.

$Si_{0.2}Ge_{0.8}$ quantum well p-MOSFETs with 5 nm gate oxides, 2.5 nm cap layer and an optional boron doped delta layer fabricated in a stand 0.6 μm CMOS process have also been demonstrated [76]. The maximum low field hole mobility was increased by 70% from 67 cm^2/Vs for a reference silicon transistor to 115 cm^2/Vs at 300 K, and by 100% from 110 cm^2/Vs to 220 cm^2/Vs at 98 K. In the high electric field region the drain current in the saturation region was improved by 20% for the same threshold voltage.

Maikap *et al* [77] have presented the results of the studies on the improved electrical properties of ultra-thin oxide films grown on strained $Si/Si_{1-x}Ge_x/Si$ at a low temperature using NO- and O_2- plasma. The NO- grown oxides showed excellent electrical properties. The improvement was attributed to enhanced nitrogen incorporation at the $Si-SiO_2$ interface.

Sidek *et al* [78] succeeded in integrating SiGe p-MOSFETs into a CMOS process leading to a considerable hole mobility improvement of up to 70%. Three different undoped layers were grown successively by MBE, including a 20 nm buffer layer, a 15 nm SiGe layer and a 15 nm cap layer. The Ge concentration of the SiGe layer was either uniform 20% or linearly graded 0-40% from the substrate to the surface. Anodic oxide and LTO were used as dielectrics. The annealing was performed at relatively modest temperatures, leading to one of the first practical demonstration of viable SiGe p-MOSFET in CMOS architecture.

Yeo *et al* [79] have demonstrated the ultra-short channel length (50 nm) SiGe channel heterostructure MOSFET reported to date. The device has a novel structure that

employs an undoped ultra-thin-body on a SOI substrate to suppress the short-channel effects. The thin body was fabricated by lateral SPE which also provides a convenient way to produces the SiGe/Si heterostructure. A 70% enhancement in the drive current is observed due to the introduction of $Si_{0.7}Ge_{0.3}$ in the channel.

2.4.2 Analytical models and theoretical studies

The holes have to be confined in the SiGe channel in order to reduce the parallel conduction. Carrier confinement has been one of the most important areas of simulation studies for SiGe p-MOSFET. Pawlowicz *et al* [80] indicated that a narrow triangular Ge composition profile can provide excellent subsurface hole confinement, using simultaneous Schrodinger-Poisson solutions verified by analysis of MOS capacitor *C-V* curves. Kovacic *et al* [81] discussed the factors affecting the hole population in the channel and the transconductance characteristics in the p-channel Si/SiGe MOSFET. Niu *et al* [82, 83] provided an analytical model of hole confinement gate voltage range, which was derived for SiGe p-channel MOSFET and verified by SEDAN-3 simulation. They also set up an analytical model of threshold voltage and inversion charge for the graded SiGe-channel p-MOSFET [84]. Additionally they analysed the effect of substrate bias in bulk and SOI SiGe p-MOSFETs [85].

The hole mobility is another important parameter for SiGe p-MOSFETs. It has been studied by many researchers. Manku and Nathan [86] have investigated the influence of the gate voltage and the Si-cap thickness on the effective mobility of SiGe p-MOSFETs, by solving the one-dimensional Poisson's equation. Kearney and Horrell [87], Tezuka *et al* [88] and Lander *et al* [89] have analysed the low temperature mobility of holes in the SiGe quantum wells theoretically and experimentally.

Sadek *et al* [90] presented a new analytical model used to calculate the charge carrier concentration and threshold voltage for p-type Si/SiGe FETs. Good agreement between the results calculated by this model and numerical simulations on one hand, and experimental results on the other hand has been found. Iniewski *et al* [91] also presented an analytical model for the threshold voltages in a Si/SiGe/Si MOS structure. This model

offered very good accuracy as compared to the results of one- and two-dimensional numerical simulations. It was shown that short-channel effects lower the threshold voltage of the SiGe channel and increase the threshold voltage for parasitic conduction in the Si cap layer. The holes in the SiGe channel, which increase as the channel length decreases, result in the increase of the threshold voltage in the Si cap layer. The model can serve as a useful tool for p-channel Si/SiGe/Si MOSFET design. Voinigescu *et al* [92] demonstrated that the experimental high frequency and low frequency *C-V* characteristics of Si/SiGe heterostructure MOS capacitors can provide accurate material-, process-, and device-related information such as the valence band offset, Si cap layer thickness, substrate doping and MOSFET threshold voltage.

Collaert and Meyer [93] derived an analytical model to investigate the influence of the Ge-concentration on the leakage current and subthreshold slope of vertical heterojunction MOSFETs. This model showed a good agreement with 2D simulation results. They [94] also presented an analytical model to analysis the short-channel threshold voltage of a novel vertical heterojunction p-MOSFET.

The Si/$Si_{1-x}Ge_x$ retrograded double quantum well p-type MOSFETs have been investigated recently. Chretien *et al* [95] developed an analytical model for the determination of the threshold voltages and an estimate of the hole densities in each conducting QW-channel including the silicon surface channel. Yousif *et al* [96] analysed the designs of different Si/$Si_{1-x}Ge_x$ retrograded double quantum well p-type MOSFETs, both on bulk silicon and on SOI substrates. The threshold voltage in different channels and the confined hole density profile at different gate potentials were investigated, using analytical and numerical approaches. Yousif *et al* [97] also analysed the short-channel effects in the devices. The validity of the model was confirmed by comparison with available experimental and numerical results where good agreement has been observed.

All these analytical models are useful as design tools in device optimisation. However, they can not be easily used for an arbitrary SiGe p-MOSFET. This is because each analytical model is derived for a special design. Also generally the size of SiGe devices are 0.25 μm or below, which require realistic two-dimensional models to consider

short channel effects. Thus, analytical models are most useful for one-dimensional design issues, such as threshold voltage adjustment.

2.4.3 The experimental work

Numerous workers have now fabricated devices displaying substantially enhanced hole mobilities compared with silicon controls. Measurements of mobility as a function of carrier sheet density indicate that interface charge and interface roughness scattering are important. These experiments also suggest that appropriate growth procedures could be developed which might minimise these scatting processes, giving devices still higher performance [98, 99].

Jiang and Elliman [100] have demonstrated that their SiGe transistors exhibited improved performance: the channel hole mobility and linear transconductance were up to 18% higher for surface channel SiGe transistors, and up to 12% higher for buried channel SiGe p-MOSFETs, than for equivalent Si control devices on the same chips.

Bouillon *et al* [101] presented a high performance 0.18 μm p-MOS technology based on the use of lowly doped SiGe channel. A 16% increase in the mobility and a 40% gain in the saturation current, due to the SiGe channel itself have been demonstrated and confirmed by Monte Carlo simulations. Carns *et al* [102] have found an increasing apparent hole mobility with increasing Ge content over a wide doping range, by analysing their experimental data.

Wu and Chang [103] reported experimental realisation of a inverted boron delta modulation-doped Si/SiGe heterostructure field effect transistors. The device linearity was enhanced as a result of reduction in parallel conduction at high forward gate bias and the better carrier confinement at the channel/spacer heterointerface. Based on these improved characteristics, the delta modulation-doped Si/SiGe heterostructure has a great feasibility for high performance and large input single circuit applications.

Mathew *et al* [104, 105] presented the dc, ac and low-frequency noise characteristics of SiGe channel p-FETs on silicon-on-sapphire (SOS). The SiGe p-FETs showed higher mobility, transconductance and cut-off frequency compared with the Si control devices.

2.4.4 The simulation work

Simulations are widely used in analysing, designing and optimising SiGe devices because they are faster and lower in costs than experiments. The three standard simulation approaches, including drift diffusion, hydrodynamic and Monte Carlo models, are widely applied to SiGe device simulation.

A. Drift Diffusion (DD) simulation

Niu *et al* [106] simulated the Ge implanted SiGe p-channel MOSFET. Persun *et al* [107, 108] investigated the design of Si and SiGe p-channel SOI MOSFET. Voinigescu *et al* [109] used DD simulations to establish the impact of design parameters on the subthreshold characteristics, hot carrier injection and high frequency performance of Si/SiGe FETs. Clifton *et al* [110] explored the design parameter space for pseudomorphic SiGe p-channel MOSFETs using the two dimensional numerical device simulator ATLAS II/BLAZE. Cho *et al* [111] investigated the effect of substrate engineering for delta doped SiGe p-MOSFET using a 3D device simulator DAVINCI.

A planar design was proposed for high mobility SiGe heterojunction CMOS technology [112]. Device and circuit simulations showed the performance leverage of this technology over bulk Si CMOS for L_{eff} = 0.2 μm. The simulations also address the general issue of the importance of mobility in submicron device performance, showing how the benefits of increased mobility persist at L_{eff} = 0.2 μm despite the onset of velocity saturation.

Shi *et al* [113] simulated the deep submicron (0.35 μm) strained $Si_{1-x}Ge_x$ buried channel p-MOSFETs with a Ge concentration up to 50%, using the MEDICI device simulator. The simulation results showed that the maximum drain current increase monotonically with the Ge mole fraction. The drive current enhancement is more than 300% for $Si_{0.5}Ge_{0.5}$ over Si. Subthreshold characteristics were analysed for different Ge mole fractions in their study. The effects of Si cap layer thickness and $Si_{1-x}Ge_x$ channel thickness on drive current and gate voltage operating window were analysed. The simulation results showed that the drive current is the highest when the $Si_{1-x}Ge_x$ layer thickness is between 100 and 300 Å. However, the $Si_{1-x}Ge_x$ layer thickness can be as low as 50 Å with less than a 10% penalty in the drive current, for structures with a 50 Å Si cap layer.

All simulations used in the above works employ drift diffusion, although most of them were calibrated by higher level models (such as: hydrodynamic or Monte Carlo models) or experimental data.

B. Hydrodynamic (HD) simulation

O'Neill *et al* [114, 115] compared conventional MOSFETs with SiGe heterojunction MOSFETs suitable for CMOS technology having channel lengths between 0.5 μm and 0.1 μm. They have investigated the high frequency performance of submicron Si/SiGe CMOS, using a hydrodynamic simulator, demonstrated an enhancement in f_T around 50% for n-channel devices and was more than doubled for p-channel devices.

Sadek *et al* [116] proposed a design for a Si/SiGe CMOS, which is planar and avoids inversion of the parasitic surface channel within the designed operating voltage range. The simulation results demonstrate the feasibility and advantages of heterojunction CMOS architecture.

Ieong and Tang [117] studied the influence of different hydrodynamic models on the prediction of submicron device characteristics using the general hydrodynamic

equation solver. They analysed the simulation results of various structures of SOI-MOSFETs and SiGe-HBTs.

C. Monte Carlo (MC) simulation

Hinckley and Singh [118] investigated the physics of hole transport in pseudomorphic $Si_{1-x}Ge_x$/Si (001) by Monte Carlo simulation. A regular, monotonic increase in hole mobility and effective temperature was found with increasing Ge alloy content from 0 to 40% Ge. The hole transport properties in $Si_{0.6}Ge_{0.4}$/Si (001) were found to be closely similar to the hole transport properties in bulk Ge. The increase in hole mobility was due to two strain related effects: (1) lifting of the zone-centre heave-hole and light-hole degeneracy; and (2) a reduction in the density of states, or equivalently, the effective mass of the carriers.

Dollfus *et al* [119] reported a Monte Carlo analysis of SiGe p-MOSFET and compared this with conventionally designed Si p-MOSFETs. They showed that in SiGe p-MOSFET, the effective channel mobility was increase by a factor of 2.6 with 60% of this improvement due to the confinement of holes in a potential well. The device performances I_{Dsat}, g_m and f_T were improved by at least 55% only due to the strain-induced lowering of the hole effective mass in SiGe.

Briggs *et al* [120] have calculated hole mobility in relaxed and strained undoped SiGe layers with Monte Carlo simulation. They [121] have also calculated low-field hole mobilities for relaxed and strained heavily doped SiGe alloy layers with Ge contents varying from 0 to 50%. Liou *et al* [122] have developed a SiGe Monte Carlo simulation with a full band Monte Carlo model. Hole drift velocity and impact ionisation coefficients at high fields were calculated. Bufler *et al* [123] presented Monte Carlo results for the velocity-field characteristics of holes in: (1) unstrained Si; (2) strained Si; and (3) strained SiGe using a full band model. They [124] also analysed hole transport at 300 K in (001)-strained $Si_{1-x}Ge_x$ alloy grown on unstrained $Si_{1-y}Ge_y$ using Monte Carlo simulation. Monte Carlo simulations have been carried out by Crow and Abram [125] to investigate

factors, which influence hole transport at 300 K for moderate electric fields (10^4-10^6 V/m) within compressively strained $Si_{1-x}Ge_x$ quantum wells deposited on Si.

Martin *et al* [126] presented a comparative Monte Carlo study dealing with the influence of the Ge profile on current-mode operation noise of n-Si/p-SiGe heterojunctions. Uniform profiles with different Ge contents as well as graded profiles of Ge in the p region are considered. It was shown that a Ge box profile produced larger enhancement in electron current density than in graded profiles. The triangular Ge profile produced the best noise characteristics of the devices studied throughout the considered frequency range.

Yeom *et al* [127] have calculated energy relaxation in the valence band using Monte Carlo simulations with a $\boldsymbol{k} \bullet \boldsymbol{p}$ band structure. The relaxation times for Si are about 10^{-13} s while those for Ge are an order of magnitude higher. To study the effect of biaxial strain produced through epitaxy on energy relaxation the results for $Si_{0.8}Ge_{0.2}$ on a{100} silicon substrate were also presented.

2.5 Summary

The basic properties of Si/SiGe heterosystem and SiGe device architectures have been introduced. The state of the art for p-channel SiGe MOSFET has also been reviewed. Work on practical SiGe p-MOS devices is still in its infancy but shows considerable promise. The highest published low-field mobilities in such a device were around 500 cm^2/Vs at 300 K. Incorporation of a SiGe p-MOSFET into CMOS could lead to improvements in speed and higher packing densities in CMOS circuitry. In the next chapter, the methodology for SiGe device simulation will be presented.

CHAPTER 3

Methodology for SiGe Device Simulations

Device modelling is playing an ever increasing important role in semiconductor industry. However, simulation software as it is purchased from the vendors can not answer and solve all the questions. The truth is that it is necessary to know and do much more in order to use the simulation software correctly and gain benefit from it.

Apart from knowing how to run the simulators, it is necessary to understand in depth the physics and operation of the device, the physical models embedded within the simulators, the validity and limitations of the models and the numerical techniques. Enough knowledge to deal with the first two questions, can be obtained by reading the manual of the simulators and semiconductor physics books. The detail on the others will be introduced below.

It is unlikely for a commercial simulator with default parameters to achieve a good agreement with the experiments without calibration. This is because the commercial simulators use phenomenological parameters, and there is usually more than one model for each parameter to choose from, even for silicon as a material in the simulators. The parameters for advanced materials (such as SiGe) are either not reliable or not available. Therefore, the need for calibration is now widely recognised both by the vendor of the simulation software and large manufactures. This part of work will be introduced in Chapter 4.

3.1 The Physical Models Embedded in the Simulators

A schematic diagram of the complete hierarchy of approaches that may be applied to device simulation is shown in figure 3.1 [128].

At the top of the hierarchy are the techniques based on a quantum description of transport. These techniques are still far from maturity and a subject of continuing research. Compact methods at the bottom of figure 3.1, are based on analytical solutions of the semiconductor equations. Such solutions require approximations of the carrier transport model and device geometry, in order to arrive at explicit solutions for the terminal device properties. Therefore, they can not be easily used for an arbitrary MOSFET because each analytical model is derived for a specific device. Analytical models are also widely used in device optimisation [80-97]. The quantum and compact approaches are introduced here for completeness, but are not discussed in detail.

Accurate analyses of an arbitrary semiconductor device are usually based on a mathematical model that consists of a system of partial differential equations. The equations that form the model are commonly called the basic semiconductor equations, which consist of:

- Poisson's equation:

$$\nabla \bullet (\varepsilon \nabla \psi) = -\rho \qquad (3.1)$$

where ε is the permitivity, ψ is the electrostatic potential, and ρ is the space charge density.

- Current continuity equations:

$$\nabla \bullet \vec{J}_n - q\frac{\partial n}{\partial t} = qR \qquad (3.2)$$

$$\nabla \bullet \vec{J}_p + q\frac{\partial p}{\partial t} = -qR \qquad (3.3)$$

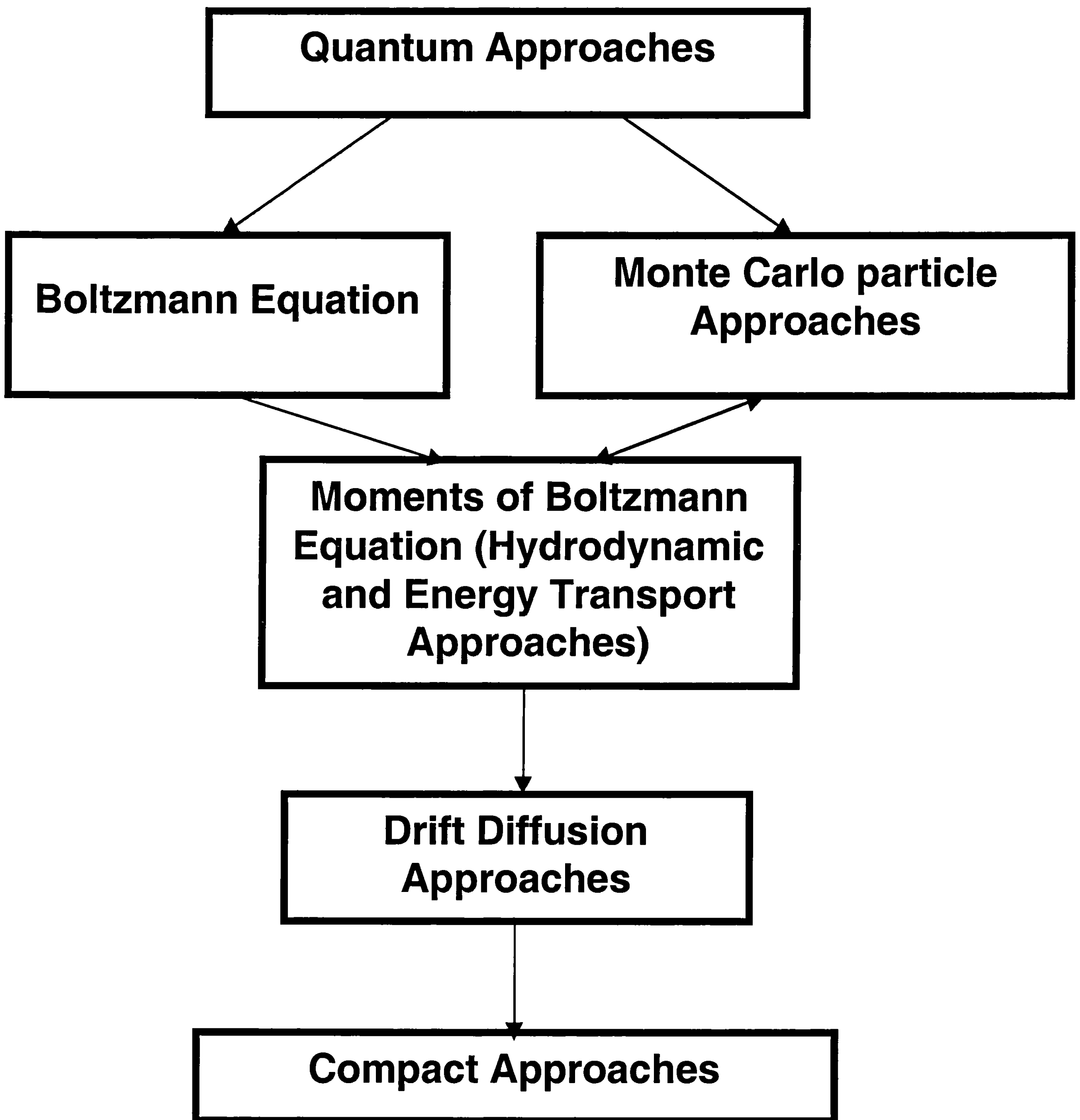


Figure 3.1 Hierarchy of semiconductor simulation models. The arrows indicate the direction of flow of information.

where $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities respectively, n and p are the electron and hole carrier concentrations respectively, and R is the net recombination rate.

- Carrier transport equations:

$$\vec{J}_n = -qn\vec{v}_n \quad (3.4)$$

$$\vec{J}_p = qn\vec{v}_p \quad (3.5)$$

where $\vec{v}_n$ and $\vec{v}_p$ are the average electron and hole velocities respectively.

The next problem is to find expressions, which relate the average carrier velocities to the electric field and to the carrier concentration. In order to obtain information about the carrier velocity it is necessary to describe the carrier concentration by means of a distribution function f in the seven dimensional phase space which consist of the spatial coordinates $\vec{r}=(x, y, z)^T$, the momentum coordinates $\vec{K}=(k_x, k_y, k_z)^T$, and time t. Subject to the following assumptions, the semi-classical Boltzmann transport equation can be used to describe the carrier transport [129].

- The scattering probability is independent of external forces.
- The duration of a collision is much shorter than the average time of motion of a particle; collisions are instantaneous.
- Carrier-carrier interaction is negligible.
- External forces are almost constant over a length comparable to the physical dimensions of the wave packet describing the motion of a carrier.
- The band theory and the effective mass theorem apply to the semiconductor under consideration.

The Boltzmann transport equation has the form:

$$\frac{\partial f}{\partial t} + \vec{v} \bullet \nabla_r f + \frac{e\vec{F}}{h} \bullet \nabla_k f = (\frac{\partial f}{\partial t})_c \quad (3.6)$$

$$(\frac{\partial f}{\partial t})_c = \sum_{\vec{K}',\lambda}[S_\lambda(\vec{K}',\vec{K})f(\vec{r},\vec{K}',t)[1-f(\vec{r},\vec{K},t)]-[S_\lambda(\vec{K},\vec{K}')f(\vec{r},\vec{K},t)[1-f(\vec{r},\vec{K}',t)] \quad (3.7)$$

where λ denotes scattering mechanisms, $\vec{F}$ is the electric field, $(\frac{\partial f}{\partial t})_c$ is the variation of distribution function due to scattering, $S(\vec{K},\vec{K}')$ is the transition probability between momentum states $\vec{K}$ and $\vec{K}'$, and $[1-f(\vec{K}',t)]$ is the probability of non-occupation for a momentum state.

3.1.1 Boltzmann transport equation

It is very difficult to solve the Boltzmann equation directly because the distribution function is a function of a seven-dimensional space (position, momentum and time), and the equation to be solved is a rather complicated integro-differential equation. Even in the approximation of parabolic bands, direct solution of the equation is very difficult for a realistic device structure. Since the distribution function is defined on the complete phase space, a multidimensional solution involves an enormous level of complexity.

The solution of the Boltzmann transport equation has been attempted in many other ways, due to the fact that an approach by direct discretization is very challenging. These methods include deterministic particle methods, Chamber's path integrals, scattering matrix approach, cellular automata and evolutionary algorithms [130-137].

3.1.2 Monte Carlo simulation

For nearly three decades, practical solution of the Boltzmann equation for semiconductor transport has been accomplished by means of particle Monte Carlo methods [138]. The term "Monte Carlo method" is usually applied to a variety of stochastic techniques, which use random number generation. In the case of particle transport, the Monte Carlo method is used to statistically solve the Boltzmann equation, without making assumptions about the distribution function. Self-consistent device applications require the simulation of an ensemble of particles, chosen to be a sufficiently representative sample of the carrier population within the device, and the solution of the

Poisson equation at frequent time intervals to update the forces acting on the particles. The Monte Carlo approach is equivalent to the Boltzmann equation in the limit of infinite sampling. However, because Monte Carlo simulations are able to resolve physical fluctuations, in many respects the approach can go beyond the limits of validity of the Boltzmann equation when it is properly implemented, at least in its ensemble self-consistent form.

Over the last decade, Monte Carlo device simulation including the complete band structure has become practical. In this approach, the band structure data is made available to the simulation through large tables for energy, velocity and density of states [139, 140]. The Monte Carlo method is often used to calibrate [141], validate and evaluate [142, 143] in the development of simpler models such as, the moment based drift diffusion (DD) [141] and hydrodynamic (HD) [144, 145] transport models. The Monte Carlo technique remains one of the most powerful and versatile approaches for studying carrier transport, for example, hot carrier effects in the short channel MOSFETs [146-148].

The main drawbacks of the Monte Carlo method are the large computational resources required and the statistical noise that arises from the fact that only a limited sample of real particles (typically 10 000 to 50 000) is simulated.

For SiGe devices, Monte Carlo is playing an even more important role because SiGe technology is not as mature as that of silicon. There is a dearth of available experimental data for SiGe. However, Monte Carlo simulations can provide low and high field transport parameters, such as mobility, relaxation time, and carrier drift velocity [120, 125]. In addition, Monte Carlo simulations can also be used to analyse the strain effects in Si/SiGe devices. On the other hand, the experimental mobility data has significant errors and /or is affected by uncertainties concerning the method used to extract the data from measurements [149]. Moreover, published data often refers only to Hall mobility, whereas the quantity of interest is the drift mobilities [40].

In this project, Monte Carlo simulations have been used to obtain parameters for hydrodynamic and drift diffusion simulations. Monte Carlo simulations are also used to calibrate these two models, and to analyse and design SiGe p-MOSFETs.

3.1.3 Moments of the Boltzmann equation

This level in the simulation hierarchy does not resolve the distribution function in detail, rather the transport model is based on moments obtained by integrating the Boltzmann equation after multiplication by suitable variables. The various transport variables are represented through average densities that are obtained as moments of the distribution function. For example, the electron density n, the average velocity v and the energy density E are given by the following expressions:

$$n = \int f(r,k,t)d^3k \tag{3.8}$$

$$nv = \int v(k)f(r,k,t)d^3k \tag{3.9}$$

$$E = \frac{m^*}{2}\int v^2(k)f(r,k,t)d^3k \tag{3.10}$$

There are a wide variety of approaches that originate from the moments of the Boltzmann equation, and which differentiate themselves mainly in the approximations or simplifications made to obtain practical implementations [150-152]. Two of them have more relevance today, and best exemplify the capabilities of the moments method. In the first approach (hydrodynamic model) the moments are initially performed and then average relaxation times for the momentum and energy continuity equations are introduced [151, 153]. In the second approach (energy transport model) the collision term in the Boltzmann equation is first formulated in terms of a microscopic relaxation time for the distribution function and then the moments are based on this approximated equation [152, 154].

A. Hydrodynamic simulations

Hydrodynamic transport equations which express the conservation of particles, momentum and energy may be obtained from the moments of the Boltzmann equation 3.6, then:

$$\frac{\partial n}{\partial t} + \nabla \bullet (\vec{v}n) = (\frac{\partial n}{\partial t})_{coll} \tag{3.11}$$

$$\frac{\partial \vec{P}}{\partial t} + \nabla(\vec{v} \bullet \vec{P}) = -qn\vec{F} - \nabla(nk_B\vec{T}) + (\frac{\partial \vec{P}}{\partial t})_{coll} \tag{3.12}$$

$$\frac{\partial E}{\partial t} + \nabla \bullet (\vec{v}E) = -qn\vec{v} \bullet \vec{F} - \nabla \bullet (nkB\vec{T}v) - \nabla \bullet \vec{Q} + (\frac{\partial E}{\partial t})_{coll} \tag{3.13}$$

where $\vec{v}$ is the average velocity, $\vec{P}$ is the momentum density, $\vec{T}$ is the carrier temperature tensor, $\vec{E}$ is the kinetic energy density, $\vec{F}$ is the electric field, and $\vec{Q}$ is the heat flow vector. No assumption has been made about the nature of the collision terms in the above equations. Equation 3.11 is the carrier continuity equation, equation 3.12 is the momentum balance equation and equation 3.13 is the energy balance equation.

Since the hydrodynamic equations are a truncated series of moments, a fourth equation that defines $\vec{Q}$ is necessary for closure. Heat conduction has been traditionally assumed to obey the classical Franz-Wiedemann law:

$$\vec{Q} = -\kappa \nabla \vec{T} \tag{3.14}$$

where κ is the heat conductivity of the electron gas.

However, it has been recognised in recent times [128] that this approach is not correct for semiconductor devices, particularly in respect of junctions, where models, implementing equation 3.14 predict unphysically large velocity overshoot. The problem of closing the hydrodynamical set of equations remains controversial and has yet to be resolved in a fully satisfactory way for modern semiconductor device simulations.

Assuming that all effects caused by degeneracy can be neglected, the scattering terms may be approximated to be represented by ensemble relaxation times, then:

$$(\frac{\partial \vec{P}}{\partial t})_{coll} = -\frac{\vec{P}}{\tau_M} \tag{3.15}$$

$$(\frac{\partial E}{\partial t})_{coll} = -\frac{E - E_0}{\tau_E} \tag{3.16}$$

where τ_M and τ_E represent the momentum and energy relaxation time respectively. These may be obtained from Monte Carlo simulations.

B. Energy transport simulations

In this approach a microscopic relaxation time τ for the distribution function is assumed in the Boltzmann equation by decomposing f into its even and odd parts, f_0 and f_1. Using the microscopic relaxation time approximation $(\partial f_1/\partial t)_{\text{coll}} = -f_1/\tau$, the odd part of the steady-state Boltzmann equation becomes:

$$f_1 = \frac{q\tau F}{\hbar}\nabla_k f_0 - \tau v \nabla_r f_0 \tag{3.17}$$

The zeroth- and second-order moments of the Boltzmann equation give the carrier continuity and energy balance equations:

$$\nabla \bullet \vec{J} = q \bullet R \tag{3.18}$$

$$\nabla \bullet \vec{S} = \vec{F} \bullet \vec{J} - n\left(\left.\frac{\partial E}{\partial t}\right|_{coll}\right) \tag{3.19}$$

where the current $\vec{J}$ and the energy flow $\vec{S}$ are defined by $\vec{J} = -qn\vec{v} = -q\int d^3k\vec{v}f$ and $\vec{S} = n\langle E\vec{v}\rangle = \int d^3kE\vec{v}f$ respectively. R stands for the carrier net generation-recombination rate.

Substitution of equation 3.17 into the expressions for $\vec{J}$ and $\vec{S}$ yields:

$$\vec{J} = -q\int d^3k\vec{v}f_1 = q(n\mu\vec{F} + \mu\nabla(un) + nu\frac{\partial\mu(u)}{\partial u}\nabla u) \tag{3.20}$$

$$\vec{S} = \int d^3kE\vec{v}f_1 = -\frac{5}{2}u(\frac{\vec{J}}{q} + \mu n \nabla u) \tag{3.21}$$

where u represents the thermal voltage kT/q. The necessary transport parameters, mobility μ and microscopic relaxation time τ, can be determined from bulk Monte Carlo simulations. It is important to notice that the Franz-Wiedemann law for heat flow is not invoked in this approach. Thus, an energy transport method is usually considered to be more accurate than a hydrodynamic approach.

Hydrodynamic and energy transport models occupy the middle ground between Monte Carlo and drift diffusion simulations. They are useful approaches, not only because they can be used to analyse non-equilibrium carrier dynamics, but also because they are simpler to implement than Monte Carlo. However, hydrodynamic models assume the carrier temperature to be a scalar. This neglects the anisotropic nature of the bandstructure, which may become important in small devices.

In this project, hydrodynamic and energy transport simulations are used to analyse the non-equilibrium carrier dynamic of SiGe p-MOSFETs. Hydrodynamic simulations are also used to calibrate drift diffusion model, and to design SiGe p-MOSFETs. Practical device simulations are described in details in the Chapters 4 and 7.

3.1.4 Drift-Diffusion method

Drift diffusion methods represent an approximation of the lowest-order transport system obtainable from the Boltzmann transport equation. The following assumptions are necessary to get the current relations in the sums of a drift and a diffusion.

- All scattering processes have been assumed to be elastic.
- The spatial variations of the collision time and the band structure are neglected.
- Effects of degeneracy have been neglected in the approximation for the scattering integral.

- The spatial variation of the external forces is neglected which implies a slowly varying electric field vector.
- The influence of the Lorentz force is ignored by assuming zero magnetic induction.
- The time and spatial variation of carrier temperature is neglected and, furthermore, lattice and carrier temperature are assumed to be equal.
- Parabolic energy bands are assumed which is an additional reason why degenerate semiconductor materials can not be treated properly.
- The zero order term of the series expansions of $\vec{J}_n$ and $\vec{J}_p$ into powers of the collision time only has been taken into account.
- The semiconductor has been assumed to be infinitely large.

Thus the transport equations are obtained:

$$\vec{J}n = q\mu_n n\vec{F}_n + qD_n\vec{\nabla}n \tag{3.22}$$

$$\vec{J}p = q\mu_p p\vec{F}_p - qD_p\vec{\nabla}p \tag{3.23}$$

where μ_n and μ_p are the electron and hole mobilities respectively, D_n and D_p are the electron and hole diffusion coefficient respectively.

The validity of the drift diffusion equations is empirically extended by introducing field dependent mobility μ and diffusion coefficient D, usually extracted from bulk material measurements. The simple derivation of approximations above used to describe the DD model should give a feeling of the limitation of drift diffusion approach. It should be kept in mind that even with the introduction of field-dependent quantities, velocity overshoot is not included in the drift diffusion approximations. Although drift diffusion models can not be used to analyse non-equilibrium carrier dynamics, they have been widely used in device design and modelling due to the speed of associated commercial simulators and academic work.

In this project, the drift diffusion simulator is the workhorse. The drift diffusion model has been used to design and optimise the Si/SiGe MOSFETs in chapters 4, 5, 6 and 7.

3.2 The Numerical Techniques

It is impossible for the basic semiconductor equations to be solved explicitly in general. Therefore, the solution must be calculated by means of numerical techniques. Any numerical approach for the solution of such a system consists essentially of three tasks. Firstly, the solution domain, which represents the geometry of the simulated device, has to be divided into a finite number of subdomains, in which the solution can be approximated easily with a desired accuracy. Secondly, the differential equations have to be approximated in each of the subdomains by algebraic equations which involve only values of the continuous dependent variables at discrete points in the domain and knowledge of the structure of the chosen functions which approximate the dependent variables within each of the subdomains. In that way one obtains a fairly large system of, in general nonlinear, algebraic equations with unknowns comprised of approximations of the continuous dependent variables at discrete points. Finally, the solution of this system is the final task to be carried out. Good numerical techniques can make simulations more accurate, stable and economic.

3.2.1 Discretisation method

The discretisation of the semiconductor equations can be done by using finite difference, finite box or finite element methods [129].

In the classical method of finite difference the domain, in which a solution of a differential equation is sought, is partitioned into subregions by a mesh which is a set of meshlines parallel to the coordinate axes. This task is most easily accomplished for a rectangular domain because the boundaries of the domain are also straight lines parallel to the coordinate axes and they therefore coincide with mesh lines.

The "finite box method" is just a more general finite difference method. In the classical finite difference approach for the solution of partial differential equations the meshlines introduced to partition the simulation domain start out at the boundary of the

domain and are continued throughout the domain up to the opposite side of the boundary. A rapidly varying behaviour of the solution of the basic semiconductor equations is, in the case of many devices, confined to small regions of the simulation domain. This can result in an enormous number of superfluous points located in regions where the solution exhibits a smooth, slowly varying behaviour, thus, wasting computer storage and time. Adler [155] has introduced the method of terminating meshlines in the finite difference approach to avoid this problem. Adler restricted himself to allow terminating lines only in one coordinate direction. This approach has been further generalised by Franz *et al* [156] to the concept of finite boxes.

The finite element method is a relatively new method. The term "finite element" was introduced by Clough [157] in 1960 in view of the direct analogy to engineering. Since then the finite element method has developed enormously and it can be seen as a general discretisation procedure of continuum problems posed by mathematically defined statements. Compared to the finite difference method, the finite element method is not only more suitable for arbitrary device geometry but also easier to choose or add the mesh. It also converges easily. Its drawback is that the discretisation is more complicated and it needs more computer resources.

3.2.2 The solution of systems of non-linear algebraic equations

After a fairly large system of general non-linear algebraic equations are obtained, they have to be solved. This can be done using "coupled" and "decoupled approaches".

In general, a decoupled approach is preferred at low bias because of its faster convergence and low cost per iteration. At medium and high bias the coupled approach becomes more convenient, since the convergence rate of decoupled approach becomes worse as the coupling between equations becomes stronger at higher bias. However, since decoupled approach has a fast initial error reduction, it is often convenient to couple the two procedures, using coupled approach after several decoupled iterations. It is very important for the coupled iteration to start as close as possible to the true solution.

The approaches of solving linear algebraic equations can be divided into two methods in mathematics: direct methods, such as LU decomposition; and iterative methods, such as SOR (Successive Over-Relaxation) method, CG (Conjugate Gradient) method and ADI (Alternating Direction Implicit) method [129].

3.3 The Commercial Simulator-"MEDICI"

There are many 2-D device simulators are available, such as CADDET, MINIMOS, GEMINI, FIELDAY, ATLAS and MEDICI. Several 3-D device simulators are also available, including DAVINCI, THUNDER and H-FIELDS-3D.

MEDICI, a commercial software package available from Avant!, is a powerful device simulation program that can be used to simulate the behaviour of a wide variety of semiconductor devices. It can solve the system of semiconductor equations in a one or two dimensional solution domain. The program may be used to predict electrical characteristics for arbitrary bias conditions.

MEDICI solves Poisson's equation, both the electron and hole current continuity equations and carrier transport equations in DD, HD and ET approximations to analyse devices such as diodes and bipolar transistors, as well as effects in which the current flow involves both carriers, such as CMOS latch-up. MEDICI can also analyse devices in which current flow is dominated by one type of carriers, such as MOSFETs, JFETs, and MESFETs. In addition, MEDICI can be used to study devices under transient operating conditions.

The finite box method is used in MEDICI for discretisation of the current continuity equations. It is very similar to the finite element in terms of triangulation. MEDICI supports four types of basic boundary conditions: Ohmic contacts, Schottky contacts, Contacts to Insulators and Neumann boundaries.

MEDICI uses a non-uniform triangular simulation grid (as shown in figure 3.2) and can model arbitrary device geometry with both planar and non-planar surface topographies. The simulation grid can also be refined automatically during the solution process. Additional nodes and elements can be added where a user specified quantity, such as potential or impurity concentration, varies by more than a specified tolerance over existing mesh elements. This flexibility makes modelling of complicated devices and structures possible. Electrodes can be placed anywhere in the device structure. Impurity distributions can be created by combining MEDICI's analytic functions with input from Avant!'s process modelling programs, Avant! SUPREM-3 and TSUPREM-4, and input from text files containing the impurity distributions.

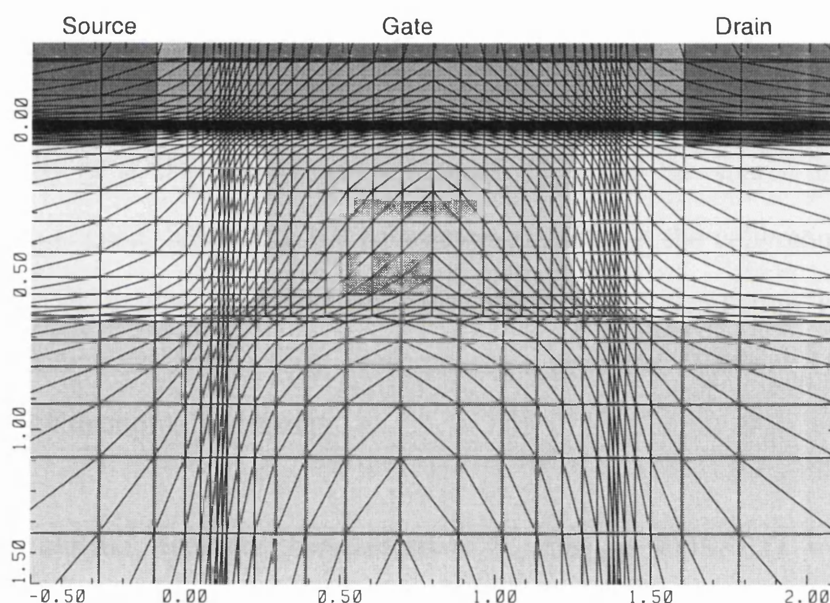


Figure 3.2 Schematic diagram of a SiGe p-MOSFET grid, with 1.5 μm channel length, used in MEDICI simulator in section 4.3. The lateral mesh lines are very dense near the interface and around the SiGe quantum well. The units of the axes are in microns.

MEDICI uses a number of physical models for accurate simulations, including models for recombination, photo-generation, impact ionisation, band gap narrowing, band to band tunnelling, mobility, and lifetime.

MEDICI is used in this project to analyse and optimise the SiGe MOSFET. Further information about MEDICI can be found in reference [158].

CHAPTER 4

Calibration

One of the objectives of this project is the calibration of MEDICI for SiGe materials and devices. The calibration is extremely important in order to build the necessary confidence in the results of numerical simulations and affects both the device design and the forecasts for the future potential of the technology. For calibration, it is necessary to acquire enough information about the devices by measuring the effective channel mobility (μ_{eff}), the effective channel length (L_{eff}) and the source-drain resistance ($R_{SD} = R_S + R_D$). Then these extracted parameters are used in the calibration process. In this work, the calibration is carried out by comparing the simulation results to the experimental data from devices with layer structure grown at Warwick University and fabricated at Southampton University.

In this chapter, numerical simulations of $Si_{0.8}Ge_{0.2}$ p-MOSFETs with thick gate oxide are carried out. These devices were fabricated especially for high field transport studies. The standard drift diffusion simulators may be extended into non-equilibrium transport region by the careful calibration of mobility parameters with respect to measured output characteristics at high longitudinal fields. The accuracy of the calibration scheme is verified against Monte Carlo calibrated hydrodynamic and energy transport models. Additionally, $Si_{0.64}Ge_{0.36}$ p-channel MOSFETs with thin gate oxide, which were fabricated with a CMOS compatible process in varying gate lengths and two different cap thickness are investigated using a calibrated drift diffusion model. In the course of calibration, important information about the low and high electric field transports properties within the strained SiGe layers are also obtained.

4.1. Parameter Extraction

In order to extract the parameters of the threshold voltage V_{TH}, the source-drain resistance R_{SD} and the effective mobility μ_{eff}, drain current (I_D) versus gate voltage (V_G) curves measured at different drain-source voltage (V_{DS}) for different channel lengths (L) have been used. The analysis is based on the procedure described by Laux [159] and Schroder [160], which was originally developed for Si-MOSFETs.

A linear extrapolation method is used to obtain V_{TH} from the I_D-V_G characteristics measured in the linear region (V_{DS} = -0.01 V, drain voltage is negative because p-MOSFETs are investigated.). It is essential to set V_{DS} very low such that gradual channel approximation can be used for the following analysis. Typically V_{DS} is several tens of mV. The curve of I_D versus V_{GS} is extrapolated to $I_D = 0$ from the vicinity (± 3 points) of V_{GS} value where the transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}}$ reaches a maximum, the threshold voltage is determined from where the slope cuts the gate voltage axis.

In order to extract the source-drain resistance R_{SD}, the R_{tot} versus L_{opt} (L_{opt} is defined as the optical microscopy gate length) curves for different values of $V_{GS} - V_{TH}$ have been plotted, where

$$\begin{aligned} R_{tot} &= \left.\frac{V_{DS}}{I_D}\right|_{(V_{GS}=\text{constant})} \\ &= R_{SD} + \rho_{ch}(L_{opt} - \Delta L) \end{aligned} \tag{4.1}$$

Here ΔL denotes the shortening of the gate from L_{opt} as a result of lateral diffusion of source and drain, and ρ_{ch} represents the channel resistivity. Ideally, all curves should intersect at a common point (R_{SD}, ΔL), provided that $|V_{GS}-V_{TH}| > 1$ (This is necessary to ensure (4.1) is valid [159]), and R_{SD} is independent of V_{GS}. Then both R_{SD} and ΔL can be obtained.

In order to extract the effective mobility μ_{eff}, the drain conductance $g_D \approx \frac{I_D}{V_{DS}}$ is calculated as a function of V_{GS} in the linear region ($V_{DS} = -0.01$ V, drain voltage is negative because p-MOSFETs are investigated). The effective mobility can then be calculated from the following equation [160].

$$\mu_{eff} = \frac{g_D L_{eff}}{W C_{ox}(V_{GS} - V_{TH})(1 - g_D R_{SD})} \tag{4.2}$$

Note that this equation is very sensitive to the value of C_{ox}, which is itself a function of gate voltage in weak inversion or accumulation. Although the equation has a singular point at $V_{GS} = V_{TH}$, in practice this is not observed. There are two main reasons for this: first, the experimental data for V_{GS} is not continual so that it is highly unlikely for measurement to be taken at exactly $V_{GS} = V_{TH}$. Second, however, generally g_D is a function of V_{GS} and for low V_{GS} (around –0.5V), g_D is also very small so that it tends to have a stabilising effect on equation 4.2. This is demonstrated in figure 4.8 where the maximum μ_{eff} is not observed at $V_{GS} = V_{TH}$. For higher (more negative) V_{GS} (around –2.5 V) g_D is much larger so that there is a pronounced maximum of equation 4.2. This is demonstrated in figure 4.9 where the maximum μ_{eff} is observed at $V_{GS} = V_{TH}$. It also possible to correct for effective channel width $W' = W_{eff}$ and effective gate voltage $V'_{GS} = V_{GSeff} = V_{GS} - I_D R_{SD}$, but normally their effect is negligible in wide devices biased at small V_{DS}.

4.2 Modelling Methodology

The device simulations are performed using MEDICI device simulator employing drift diffusion (DD), hydrodynamic (HD) and energy transport (ET) models [158]. To properly model the strained SiGe alloy, various material parameters have to be introduced

to replace the default Si values. The band gap of the strain $Si_{1-x}Ge_x$ (x denotes Ge mole fraction in the SiGe alloy) was calculated using an experimental fit [161] to low temperature data subsequently modified to consider temperature dependence. The band gap value is given by [162]:

$$E_g(T) = E_g(0) - \frac{4.74 \times 10^{-4} T^2}{T + 636 - 400x} \tag{4.3}$$

where

$$E_g(0) \approx 1.17 - 0.9x + 0.4x^2 \tag{4.4}$$

The valance band offset with respect to Si is linearly dependent on x with the following relation [163]:

$$\Delta E_v = 0.84x \tag{4.5}$$

The dielectric constant of the alloy is obtained by Clausius-Mossotti interpolation scheme [164], which can be expressed as:

$$\frac{\varepsilon_{Si_{1-x}Ge_x} - 1}{\varepsilon_{Si_{1-x}Ge_x} + 2} = (1-x)\frac{\varepsilon_{Si} - 1}{\varepsilon_{Si} + 2} + x\frac{\varepsilon_{Ge} - 1}{\varepsilon_{Ge} + 2} \tag{4.6}$$

DD model is used in the simulations to employ vertical and longitudinal-field dependent mobility models. The mobility along the channel is not constant and varies with parallel and perpendicular components of the local electric field, $F_{||}$ and $F_{\perp}$, according to the following relations:

$$\mu_{p\perp} = \frac{\mu_{po}}{\sqrt{1 + \frac{F_{\perp}}{F_c}}} \tag{4.7}$$

and

$$\mu_p = \frac{\mu_{p\perp}}{\left[1+\left(\frac{\mu_{p\perp}F_{\|}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \quad (4.8)$$

respectively. Equation 4.7 is the perpendicular electric field mobility model, which is suitable for low longitudinal fields. μ_{po} is the low-field mobility, and F_c, the critical field, is to model the mobility degradation due to vertical electric field and may be set by the gate voltage dependency of the channel conductivity. Equation 4.8 is Caughey-Thomas expression, which account for effects due to high field in the direction of current flow. v_{sat} can be associated with saturation velocity, while β is a fitting parameter in order to adjust the abruptness of velocity-field curve.

By a physics based calibration of the mobility parameters with respect to measured current-voltage characteristics, including an accurate description of 2D geometry with the aid of process simulator TSUPREM-4 and measured doping profiles, a reliable set of mobility parameters (μ_{po}, F_c, β and v_{sat}) can be deduced. The calibration started by varying the values of μ_{po} and F_c, until a close agreement was obtained between the simulated and measured transfer characteristics of devices at low (-10 mV) drain bias. The use of device measurements in conjection with drift diffusion simulator at low drain bias ensures physical correctness since transport takes place under quasi-equilibrium conditions. It then proceeded by tuning longitudinal field dependency of mobility for the entire bias range of V_{GS} and V_{DS}. Adjustment of β and v_{sat} at this step allows the drift diffusion approach to be extended to mimic the non-equilibrium transport condition. The procedure was repeated for all device lengths and also for Si (control) samples. It was essential, however, that the low field mobility parameters of equation 4.7 in all devices were kept the same as those obtained from the long channel limit. Thus, any difference between the parameters of equation 4.8 in each device was attributed to its response to the applied longitudinal fields, identifying the influence of non-equilibrium transport processes. By fixing the low field mobility parameters, the values of the junction depth

and ΔL can also be refined by carefully considering the influence of 2D effects such as punch-through in shorter devices.

HD [165-172] and ET [173-176] models based on the first three moments of Boltzmann transport equation were used to take into account high field non-equilibrium transport and non-local effects. To include a physically correct description of relaxation processes for holes in the HD/ET simulations, the relaxation times extracted from a bulk full band Monte Carlo (MC) simulations have been used.

4.3 $Si_{0.8}Ge_{0.2}$ p-MOSFETs with Thick Gate Oxide

The devices initially used to calibrate MEDICI and also to study high field transport in strained SiGe layers have been grown by a VG Semicon V90S solid source MBE system on lowly doped (2-10 Ω-cm) n-type Si (001) substrates. The growth was initiated with a 300 nm Si buffer layer to ensure the interface quality. The Ge content was 20% in nominally undoped strained $Si_{1-x}Ge_x$ channels, which have a thickness of 20 nm. This value provided a good compromise between lower hole effective mass, and mobility degrading mechanisms such as alloy scattering and interface roughening found in high-Ge content channels [74]. The thickness of Si cap layer was 7 nm and sufficient to ensure that the channel mobility was not affected by rough Si/SiO_2 interface. The transistor structure, as shown in figure 4.1, was designed specifically for high field measurements with a relatively thick gate oxide t_{ox} = 190 nm, and with drawn gate lengths (L_{opt}) of 29, 8.5, 4.7 and 1.5 μm, which were available in the partner groups. The gate width was 100 μm for all devices considered here. The gate oxidation was performed in two steps: (i) a plasma anodic oxide grown below 300 °C [74], followed by (ii) a low-pressure CVD oxide deposited at 400 °C. Source and drain contacts are defined by a single BF_2 implant at 20 kV, and then activated with an annealing step at 750 °C for 30 minutes. The thermal budget during fabrication was kept at a minimum to avoid relaxation. Si control samples

with an identical structure, except thinner oxides (100 nm) were also fabricated. All the measurements were carried out at room temperature using a HP4145 parameter analyser.

A crucial feature of $Si_{0.8}Ge_{0.2}$ p-MOSFETs was that relatively thick gate oxide allows high gate and drain biases to be applied without damaging the oxide or causing junction breakdown. This approach for studying high-field transport properties in a device configuration has been used before and also improves the inherent uniformity of the longitudinal field along the channel [177].

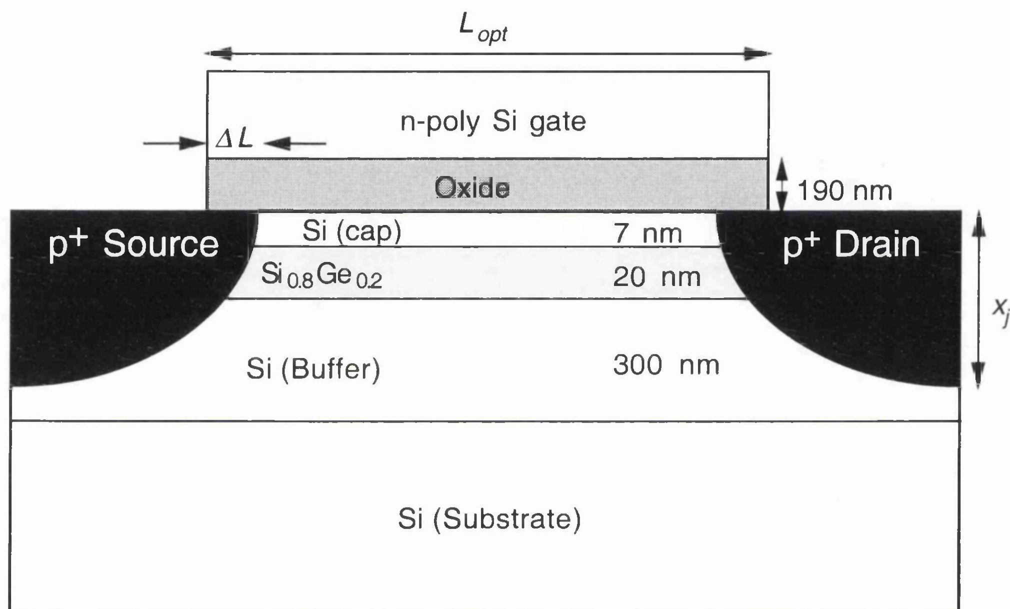


Figure 4.1 Schematic cross section of a $Si_{0.8}Ge_{0.2}$ p-MOSFETs with thick gate oxide.

In the results below, measurements were performed at V_{DS} = -0.01 V unless otherwise specified in this section. The details of the physical structure of the device, as reported by Warwick University, are given in table 4.1.

Transistor	L_{opt}(μm)				W(μm)	t_{ox}(nm)	C_{ox}(nF/cm^2)
Si	1.5	4.4	8.3	28.7	100	100	34.5
SiGe	1.5	4.7	8.5	29	100	190	18.2

Table 4.1 Device parameters used in the calculations.

	Si p-MOSFET				SiGe p-MOSFET			
L_{opt} (μm)	1.5	4.4	8.3	28.7	1.5	4.7	8.5	29
V_{TH}(V)	-0.21	-0.53	-0.54	-0.41	-2.62	-2.39	-2.26	-2.5

Table 4.2 Threshold voltage of Si and SiGe p-MOSFETs.

The threshold voltages of the devices are given in table 4.2 for both Si and SiGe devices of varying gate length. In figure 4.2 the R_{tot} versus L_{opt} curves are plotted for the Si control at different values of $V_{GS}-V_{TH}$. In order to make it clearer, the expanded region of figure 4.2 is shown in figure 4.3. All curves intersect at a common point, yielding R_{SD} = 140 Ω and ΔL = 0.49 μm. The lines for different values of $V_{GS}-V_{TH}$, are easily seen from the second fit in figure 4.4, where $-\Delta L \times \rho_{ch}$ + R_{SD} is plotted against ρ_{ch}. This is an indication that Si channel devices are well behaved and the extracted parameters are reasonable. In figures 4.5 and 4.6 the results of the same analysis for SiGe device are plotted, showing that the total resistance plots do not have a common intersect. However, it is justifiable to neglect those points (shown in figure 4.7) corresponding to low gate voltages as they throw into question the validity of the analysis (i.e. equation 4.1). It is also plausible that the R_{SD} of these devices exhibits dependence on the gate voltage. It turns out that the choice for the number of points to be included in the analysis is crucial for obtaining reasonable results. A linear fit to the last six points in the curves shown in figure 4.7 (The V_{GS} at the remaining points are not large enough to be considered.) result in R_{SD} = 128 Ω and ΔL = 0.18 μm. Even though these values were used later for extracting the effective mobility, it can be argued that a range of values for R_{SD} and ΔL are possible.

Substituting the parameters listed in table 4.1 and the extracted values for R_{SD}, μ_{eff} is calculated as a function of V_{GS}. Figure 4.8 shows μ_{eff} as a function of the gate voltage V_G for Si channel samples, while the corresponding curves for the SiGe devices are plotted in figure 4.9 for different channel length. Ignoring the points around the threshold voltages, it

is clear that the SiGe devices have significantly (about three times) higher mobility than their Si counterparts.

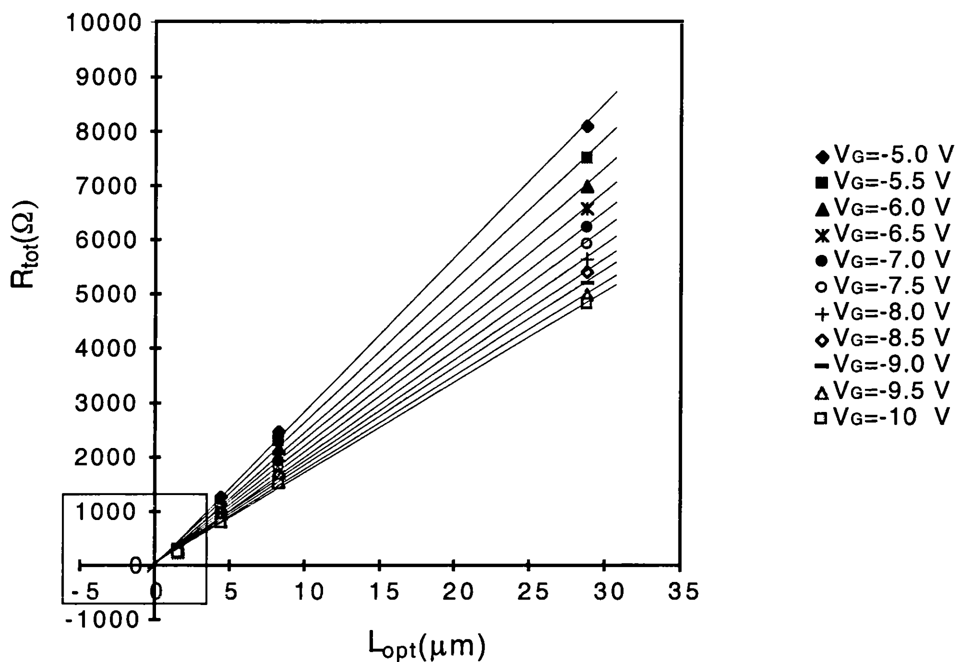


Figure 4.2 Total resistance versus channel length for Si p-MOSFET, V_{DS} = -0.01 V.

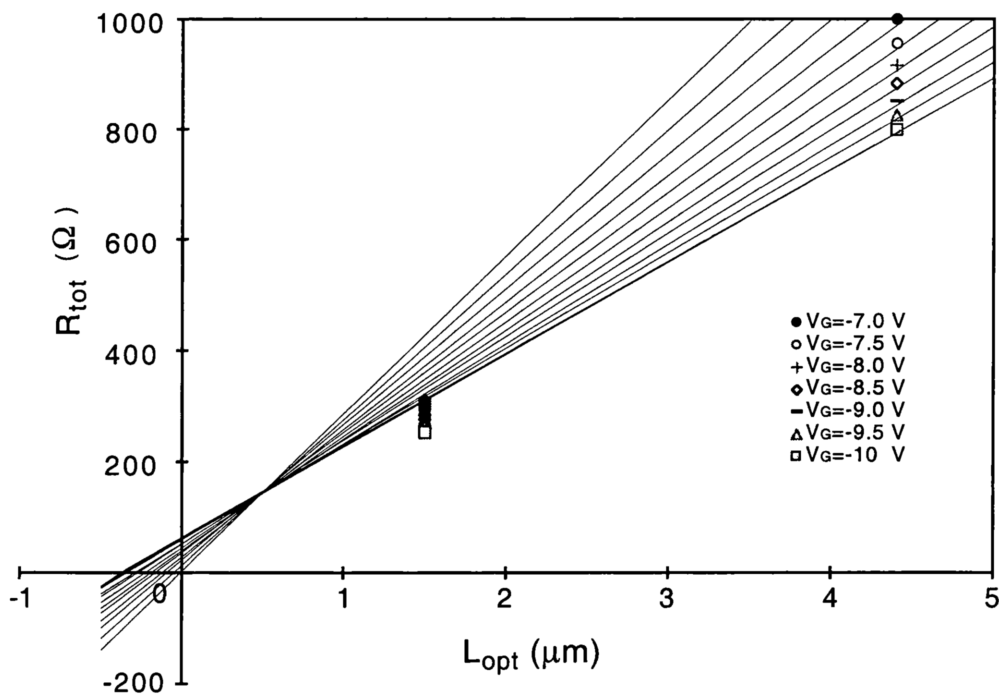


Figure 4.3 The expanded region of figure 4.2.

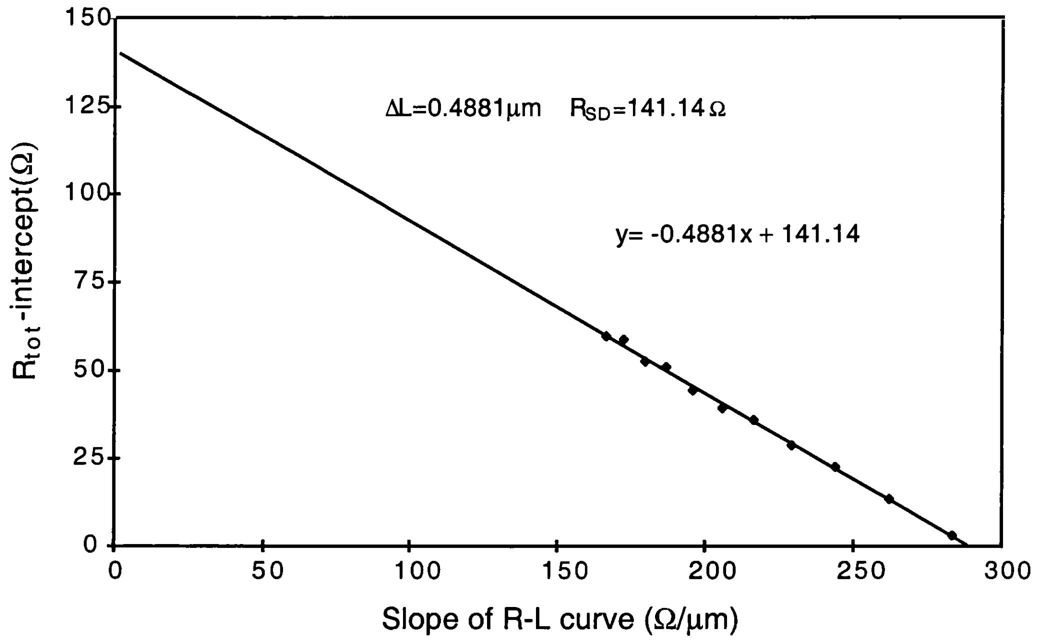


Figure 4.4 The intercept of total resistance versus the slope of total resistance-channel length curves for Si p-MOSFET, V_{DS} = -0.01 V.

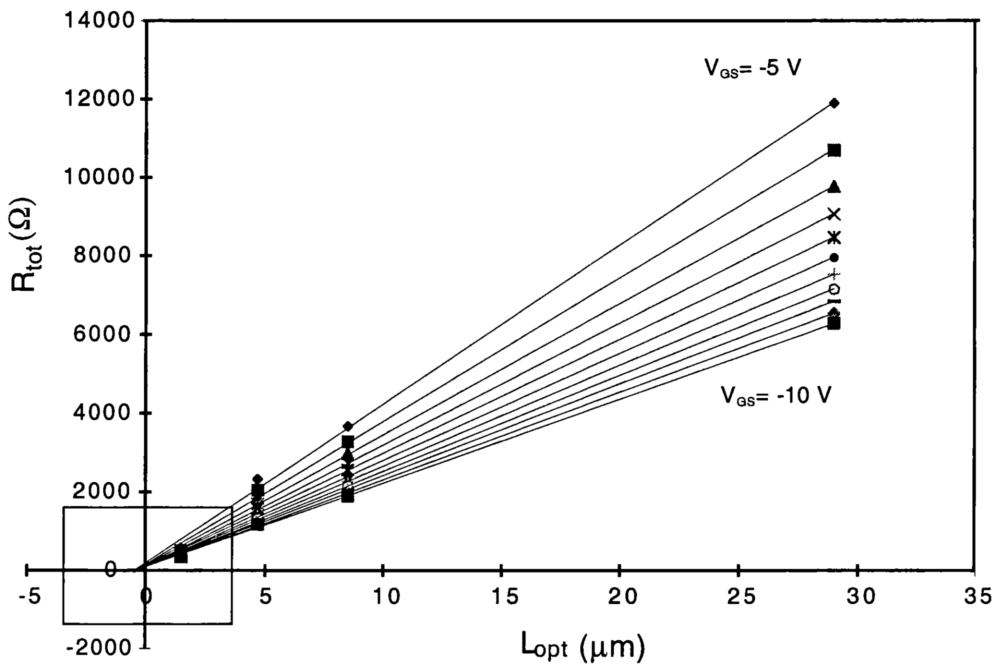


Figure 4.5 Total resistance versus channel length for SiGe p-MOSFET, V_{DS} = -0.01 V.

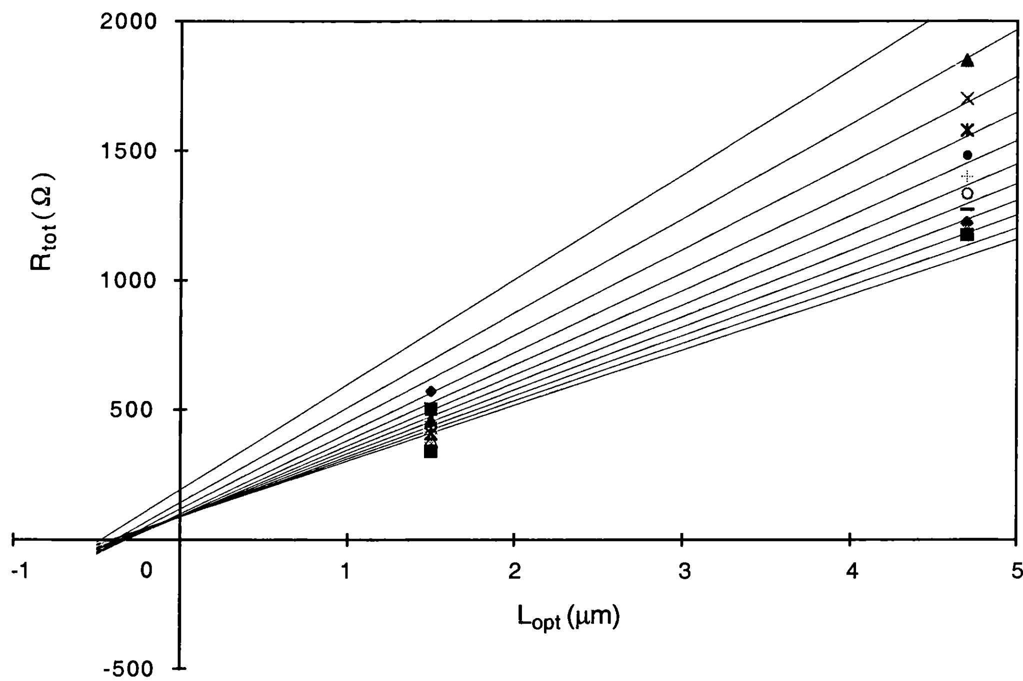


Figure 4.6 The expanded region of figure 4.5.

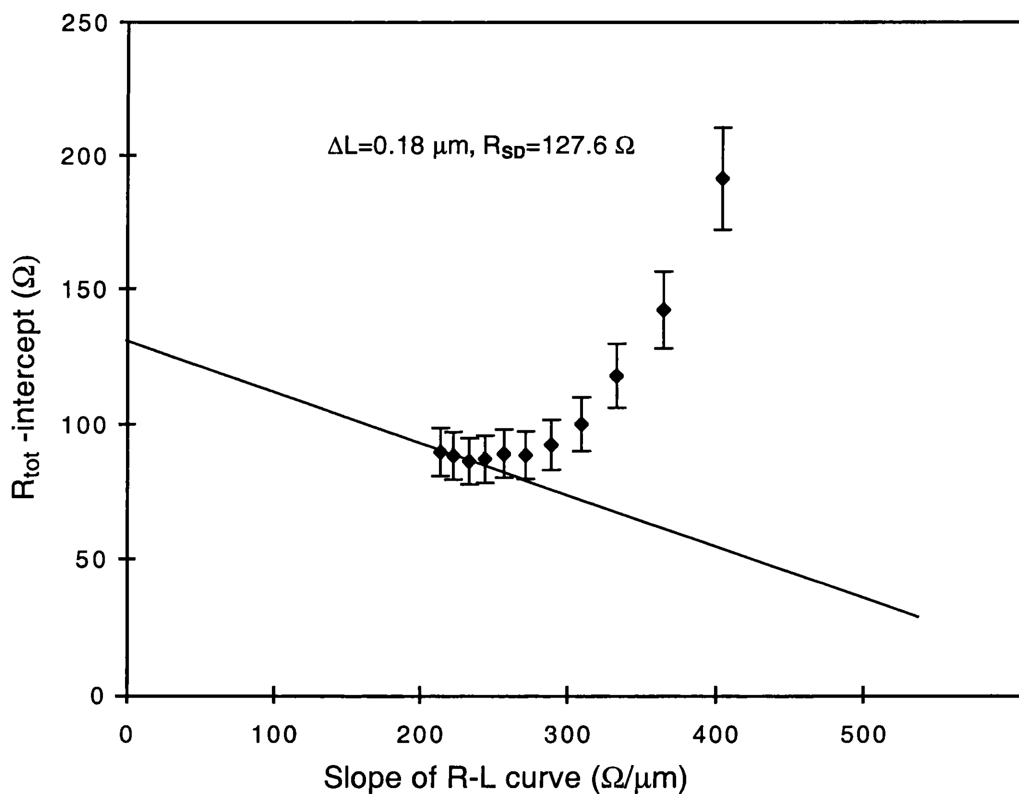


Figure 4.7 The intercept of total resistance versus the slope of total resistance-channel length curves for SiGe p-MOSFET, V_{DS} = -0.01 V.

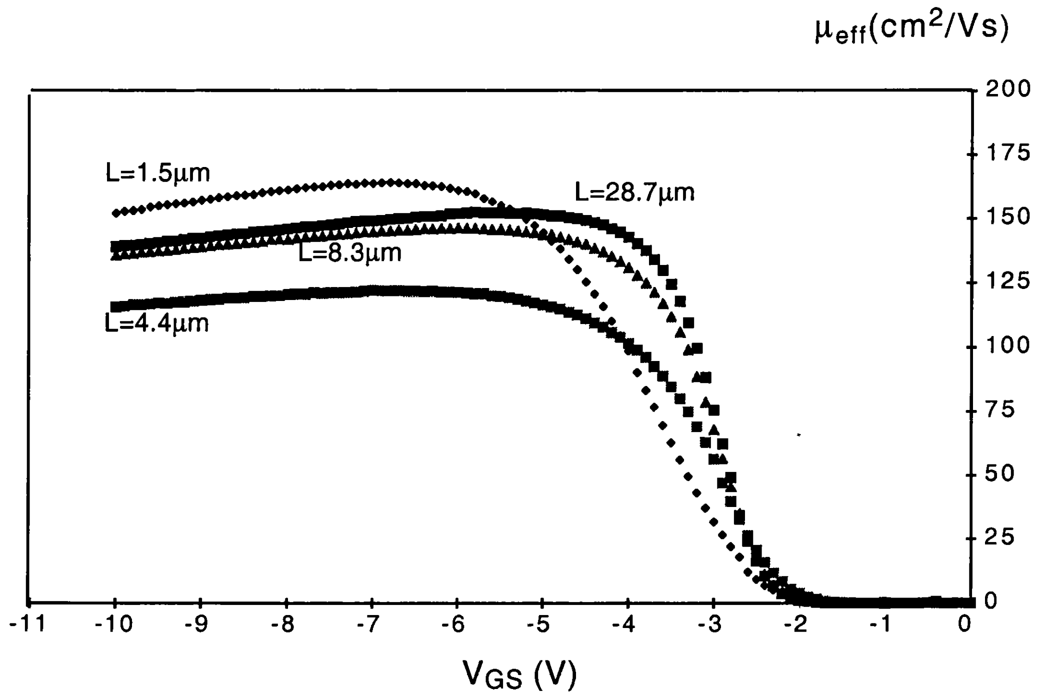


Figure 4.8 Effective mobility of the channel versus gate voltage for Si p-MOSFETs.

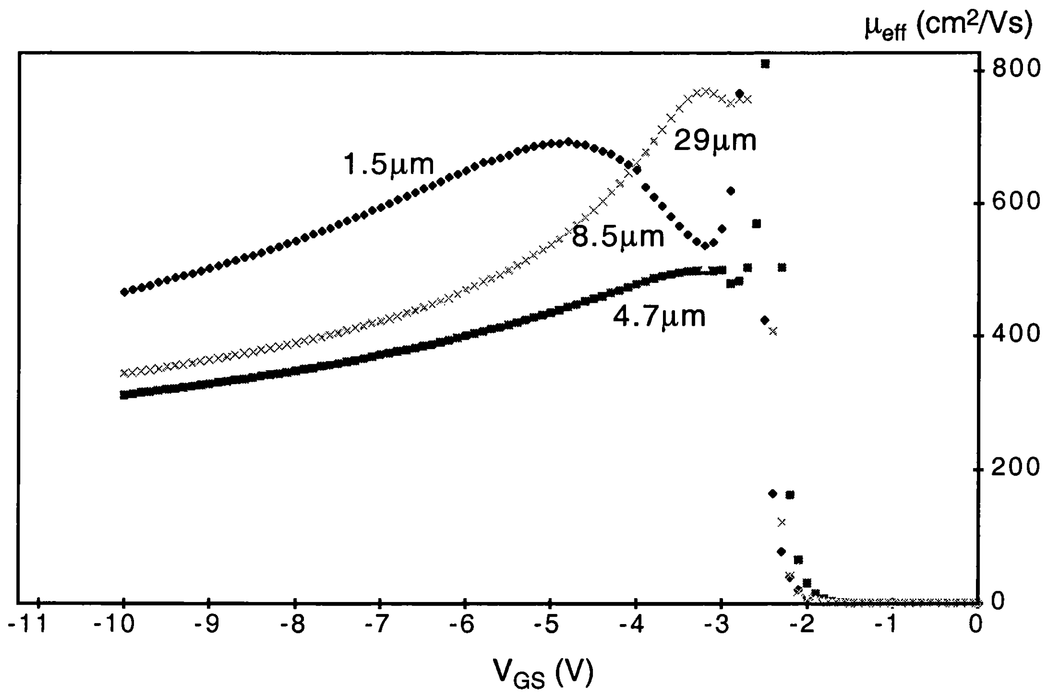


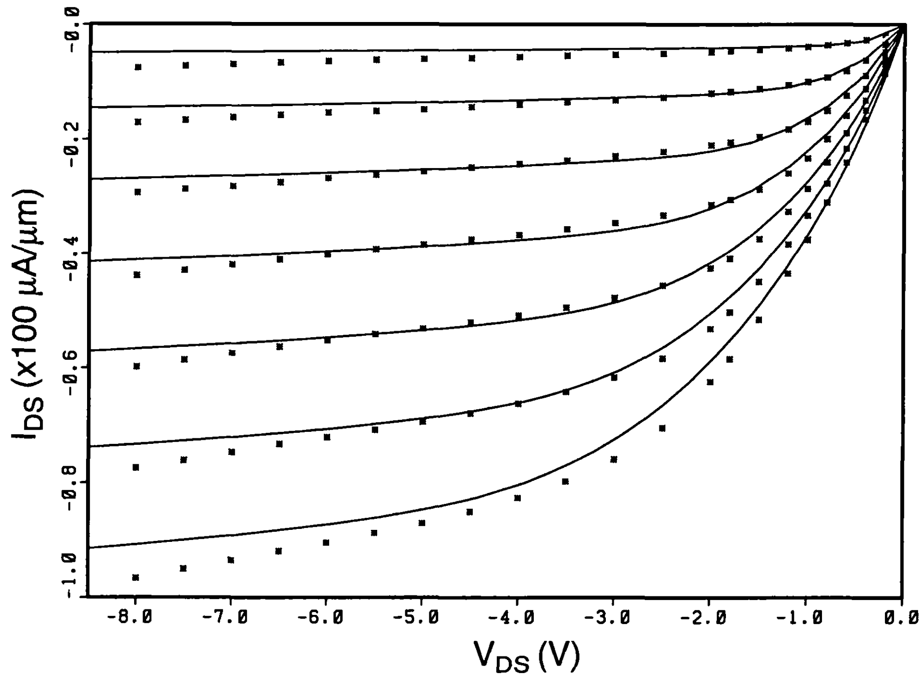
Figure 4.9 Effective mobility of the channel versus gate voltage for SiGe p-MOSFETs.

A total series source/drain resistance in strained-channel and bulk-Si p-MOSFETs of 128 Ω and 140 Ω, were extracted respectively. The corresponding sideways-diffusion length between source and drain is 0.09 (0.24) μm for SiGe (Si) devices. The peak of the extracted effective low-field hole mobility in the 8.5 μm device is about 550 (140) cm^2/Vs (see figures 4.7 and 4.8). These values served as an estimate in the calibration process.

Following the calibration procedure outlined in Section 4.2, a remarkably good agreement between simulated and measured current-voltage characteristics was achieved, as shown in figure 4.10 (a) and (b) for $Si_{0.8}Ge_{0.2}$ p-MOSFETs with drawn gate lengths of 1.5 μm and 8.5 μm, respectively. The agreement is especially good in the linear region of operation, which reflects the reliable values of the low-field mobility (μ_{po} and F_c) parameters obtained from the calibration with respect to low drain voltage measurement. Similar results were obtained also for the Si (control) samples. The overall accuracy in describing the short channel effects in the 1.5 μm device is limited by the uncertainties in x_j and ΔL.

The implications of using the DD simulation approach in the calibration procedure for longitudinal hole transport in strained $Si_{0.8}Ge_{0.2}$ and Si channels are presented in figure 4.11 for different gate lengths. This plot is constructed using those mobility parameters which give the best agreement between the measured and simulated device characteristics in each dimension. Naturally, these results are dependent upon the value chosen for R_{SD}. However, R_{SD} is important only when the channel length is short and the drain voltage is high. Therefore, devices with channel lengths of 4.7 and 8.5 μm will not be affected. It has been found that the v_{sat} and β values in $Si_{0.8}Ge_{0.2}$ p-MOSFETs are sensitive to gate length (i.e. effective field in the channel), in clear contrast with the Si control devices. It must be note that the velocity-field characteristics depicted in figure 4.11 does not truly reflect the equilibrium case in the bulk, but rather shows an average velocity of holes in the channel required to match the measured output current. This is best reflected in v_{sat}, which increases from its low value of 5.5×10^6 cm/s in long channel device to 9×10^6 cm/s in 1.5 μm device. The sharp increase in this parameter is indicative of the non-equilibrium transport determining the actual velocity of holes in the channel.

(a)



(b)

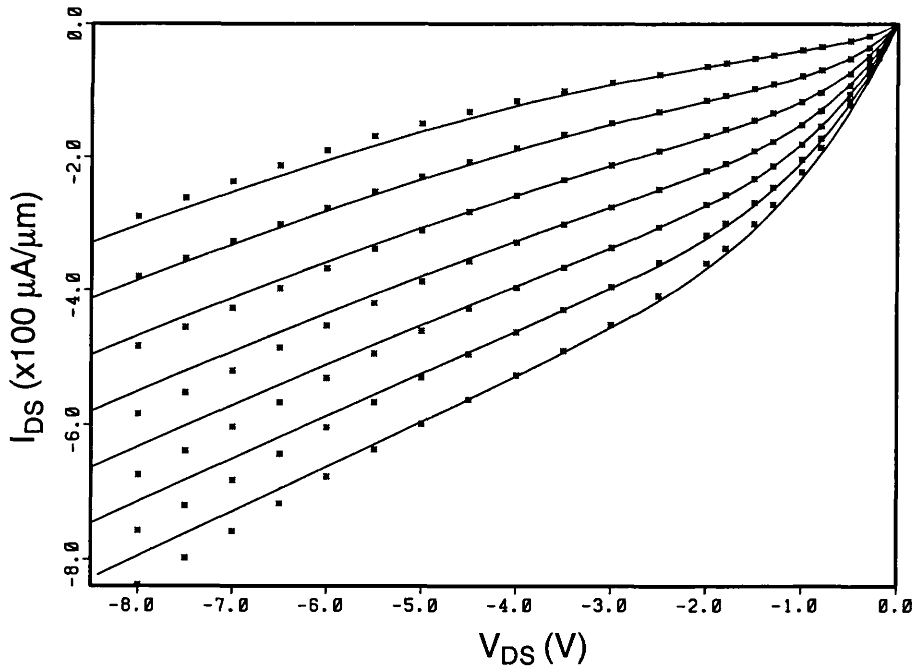


Figure 4.10 Comparison between the simulated (—) and measured (*) output characteristics of strained $Si_{0.8}Ge_{0.2}$ p-MOSFETs with channel length of: (a) 8.5 μm; and (b) 1.5 μm.

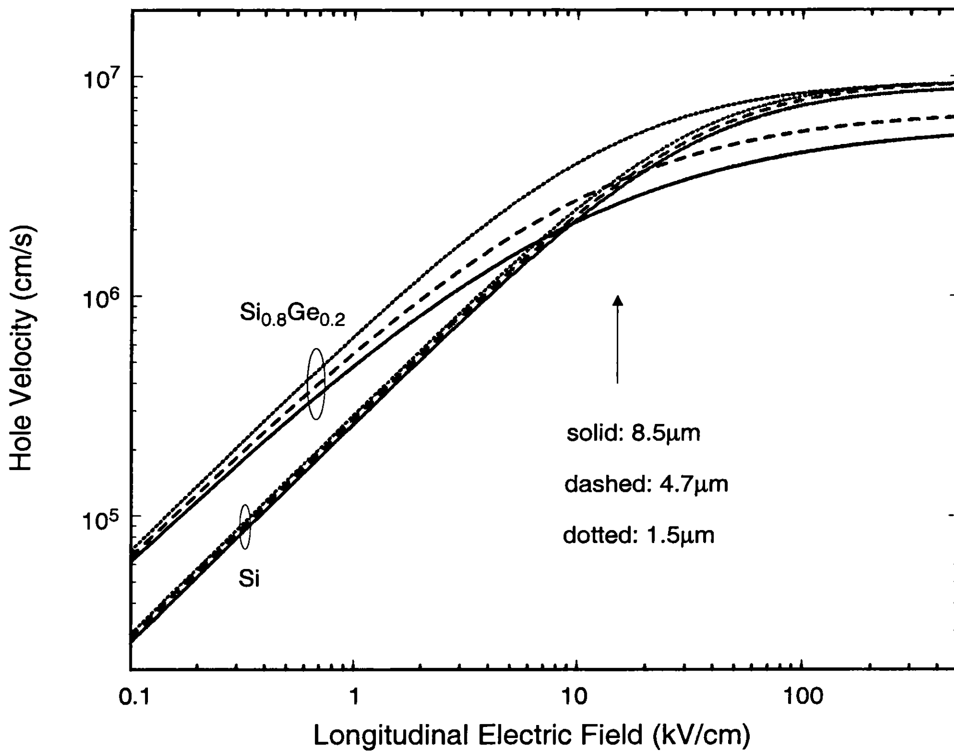


Figure 4.11 Velocity-longitudinal field characteristics of holes in $Si_{0.8}Ge_{0.2}$ and Si p-MOSFETs for different channel length of 8.5 μm, 4.7 μm, and 1.5 μm respectively.

The observation of increased non-equilibrium channel velocity in the shorter devices can be confirmed by the use of HD/ET simulations [178-180], which take into account the non-equilibrium carrier transport along the channel, and by other methods [181-185]. As a worst case scenario, the 1.5 μm device at the highest drain/gate bias condition of V_{DS} = -8 V and V_{GS} = -9 V was investigated. As shown in figure 4.12, the output current calculated from ET and HD models agrees with the measured values, as well as with the calibrated DD simulations. Similarly, figure 4.13 shows a comparison of the hole velocity along the $Si_{0.8}Ge_{0.2}$ channel 1 nm away from the interface, obtained from different models at the same bias conditions. A clear agreement between the velocity profiles from all three methods is obtained in large section of the channel except near the drain, where HD overestimates the velocity overshoot. This is a known artefact of the HD model, when the moment equations are closed using the classical Franz-Wiedemann

law, and does not necessarily reflect the true extent of overshoot [128]. The agreement between the simulated velocities in DD and ET models is especially good, confirming the success of the calibration procedure. The very high value of channel velocity in the 1.5 μm device is an indication of non-equilibrium transport and velocity overshoot. However, if the DD simulation is performed using v_{sat} and β values obtained from the long-channel device, poor agreement is found, as shown also in figures 4.12 and 4.13. In this case, the simulations significantly underestimate the measured current, which comes from the very low value of the equilibrium channel velocity. It is evident that the calibration procedure for mobility parameters successfully restores the actual velocity profile in the channel.

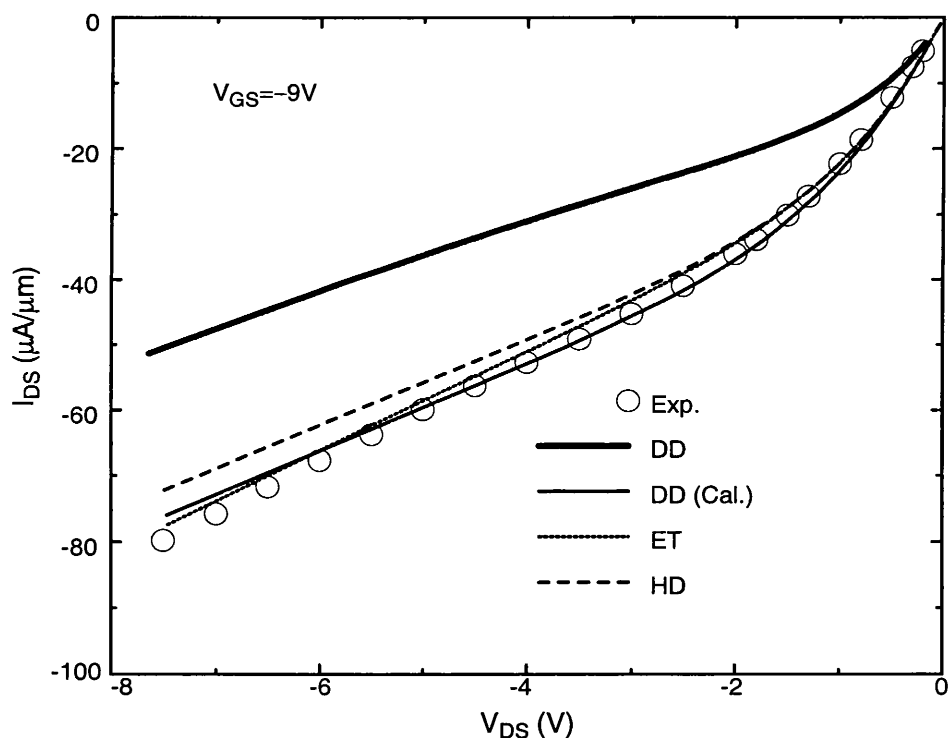


Figure 4.12 Output current versus drain voltage according to calibrated DD, HD, ET and uncalibrated DD (DD analysis is repeated using the mobility parameters obtained from a long channel device of 8.5 μm.)

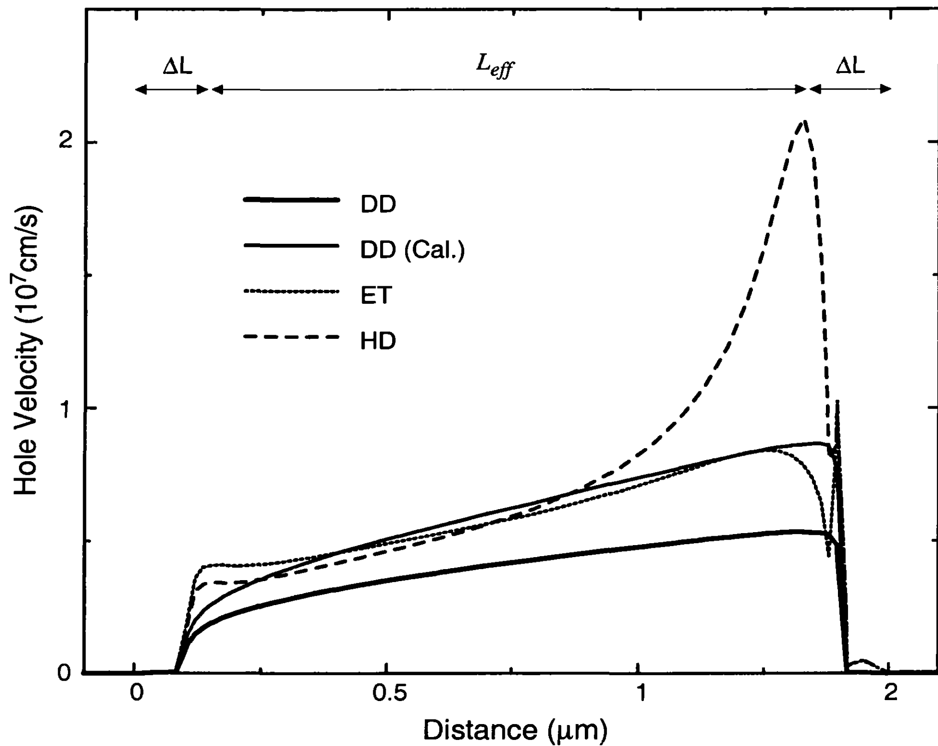


Figure 4.13 Hole velocity profiles according to calibrated DD, HD, ET and uncalibrated DD (DD analysis is repeated using the mobility parameters obtained from a channel device of 8.5 μm.).

The gate length dependency of saturation velocity of electrons and holes in MOSFETs in which spatial overshoot effects are present has been reported before [186]. A simulation study of the same phenomenon in strained Si is given by Roldan *et al* [187, 188]. This is due to the fact that the energy relaxation times of carriers change with the applied field. Since electric field profile and its peak value are different in each device for a given V_{DS}, non-equilibrium conditions in which velocity overshoot takes place are also modified. Accordingly, the DD simulations assume a higher average channel velocity as the gate length is reduced in order to account for those sections of the channel in which the hole drift velocity exceeds the saturation value. It is thus possible for simplified DD models, once calibrated, to "mimic" the non-equilibrium transport without recourse to more complicated models, making them still available as speedy alternatives in ultra-small

device simulations. However, it must be pointed out that the success of the analysis is sensitive to the level of accuracy in source/drain resistance, x_j and L. Biesemans *et al* [189] indicated that the errors in the double regression method proposed by Laux [159] and Schroder [160] may become significant depending on the range of L_{eff} studied. Because of rather large value of L_{eff} in the work, such uncertainties will be negligible and the following calibration procedure should not be impacted significantly. However, due care must be exercised to obtain accurate values for these parameters when extending the above analysis into smaller dimensions.

In figure 4.14 the longitudinal electric field and hole temperatures obtained from HD and ET simulations of 1.5 μm device are plotted. The very high hole temperature at the drain end of the channel indicates the extent of non-equilibrium conditions, which must be considered in the devices. Still more important to consider is the longitudinal field profile in the channel; holes face a high electric field of approximately 15 kV/cm as they enter the channel. Such high longitudinal fields near the source-end are a result of a very thick gate oxide in the devices intended for high-field measurements, which allows the application of high drain biases without pinch-off. 15 kV/cm is high enough to change the injection condition at the source due to the higher average velocity of holes as indicated by the sharp peak in the velocity-field characteristics of figure 4.14. It is essentially this injection condition which determines the actual current in the channel, not the velocity overshoot at the drain end [190, 191]. This point is best illustrated by the fact that the output current obtained from all models agree closely, even though HD model estimates a significantly larger overshoot compared to ET or calibrated DD model. Moreover, the vertical component of electric field further contributes to the increased hole velocity at the source by virtue of highly anisotropic valance band in the strained material coupling different directions of transport strongly. The lack of similar characteristics in the Si control devices is indicative of the higher potential of strained SiGe material for the overshoot effects, which can be beneficial for deep submicron devices.

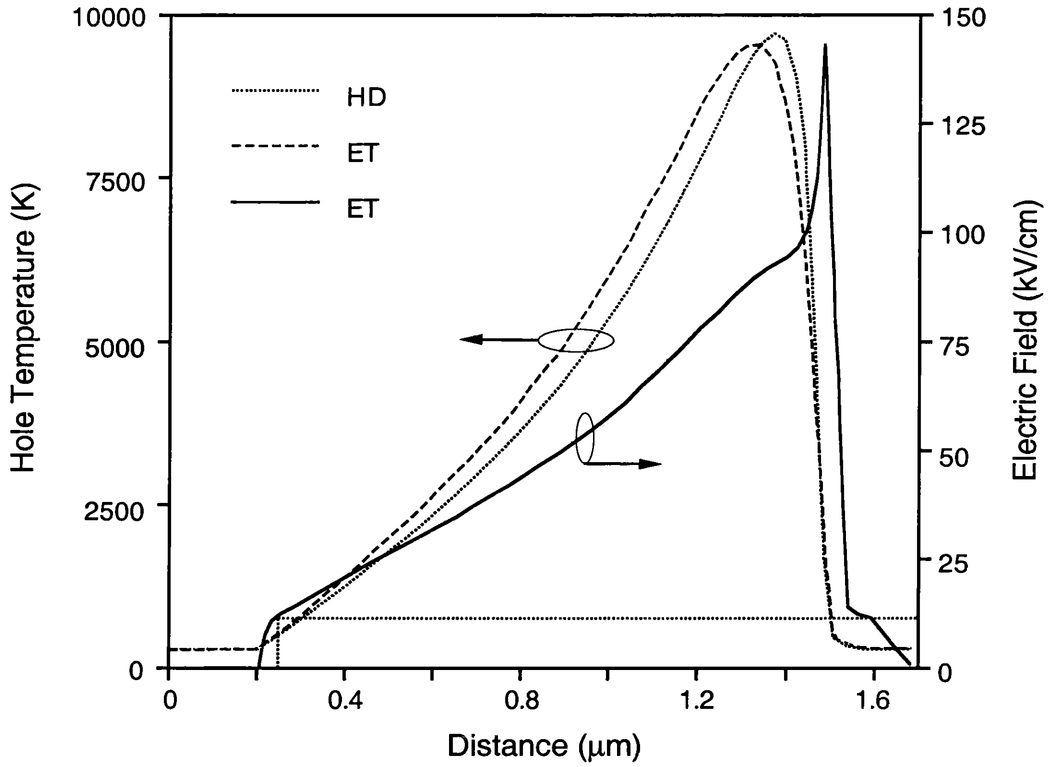


Figure 4.14 Hole temperature and longitudinal electric field along the channel.

High field hole transport characteristics in bulk $Si_{1-x}Ge_x$ alloys have been also experimentally studied by Liou *et al* [122]. They have shown that with increasing Ge content up to $x = 0.3$, the hole drift velocity in $Si_{1-x}Ge_x$ decreases at 300 K. They attributed this reduction of hole drift velocity to alloy scattering. Taking the long channel limit of v_{sat} given in figure 4.11 as a true saturation drift velocity for holes in the devices, this value appears to be smaller in strained $Si_{0.8}Ge_{0.2}$ than that in Si. This result is in agreement with that of Bufler *et al* [123], but contrasts with the results obtained by Hinckley and Singh [118]. If the drift velocity is eventually limited by optical phonon emission as in the bulk, then v_{sat} can be approximated as

$$v_{sat} = \sqrt{\frac{2E_{OPT}}{m^*}} \tag{4.9}$$

where E_{OPT} is optical phonon energy and m^* is the effective mass of the carriers [192]. The lower value of v_{sat} in $Si_{0.8}Ge_{0.2}$ of ~ 0.45×10^7cm/s as opposed to 10^7cm/s in Si may then be attributed to the lower optical phonon energy of 40 MeV ($Si_{0.8}Ge_{0.2}$) as compared to 63 MeV (Si). Obviously, equation 4.9 is very simplistic and does not take the changes in phonon dispersion itself into account in the alloy material, nor does it consider the impact of strain in the optical phonon scattering. However, the bulk Monte Carlo simulations for $x = 0.2$ also show that the saturation velocity is lower in strained SiGe, in agreement with the analysis above.

4.4 $Si_{0.64}Ge_{0.36}$ p-MOSFETs with Thin Gate Oxide and Short Channel

After the fabrication of the first batch of devices from the SiGe consortium, it was desirable to repeat the calibration process in respect of devices with different germanium concentration in the channel, shorter channel length and a properly scaled gate oxide. It was also possible to draw further conclusions regarding the non-equilibrium transport effects in these devices. A schematic of the structure of devices under consideration is shown in figure 4.15, where the main changes are in Ge concentration and oxide thickness.

Active layers were grown by MBE on a n^+ doped (2×10^{17}cm^{-3}) Si substrate to reduce short channel effects. The reason is that a heavily doped substrate decreases the probability of drain to source field penetration. The SiGe strained channel was isolated from the substrate with a 100 nm undoped Si buffer layer. The channel doping was background limited (~5×10^{15} cm^{-3}) to maximise the mobility. Two different Si cap thickness of 2 nm (wafer 1) and 8 nm (wafer 2) have been considered in the calibration process. The devices with drawn gate lengths (L_{opt}) of 3, 1.8, 1.3 and 0.5 μm for wafer 1, and 3.0, 2.0, 1.0 and 0.5 μm for wafer 2 were fabricated using standard CMOS processes flow. Using a process simulator (TSUPREM-4 [193]), the final doping profile in these

devices has been modelled, resulting in a junction depth (x_j) of 0.3 μm. The gate width was 40 μm and gate oxide thickness was 10 nm for all devices. As before total thermal budget was kept to a minimum (800 °C) to avoid degradation of the strained channel.

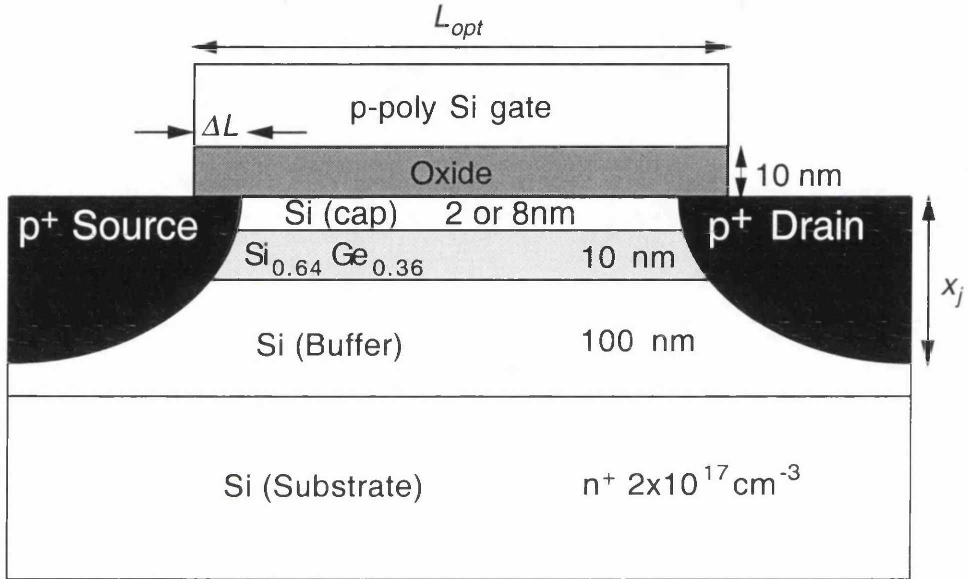


Figure 4.15 Simulated $Si_{0.64}Ge_{0.36}$ p-MOSFETs structure with thin gate oxide.

The DD simulations were calibrated with respect to measured device characteristics, and the calibrated DD simulations were then used to analyse the operation of the devices in order to deduce information about the transport in the SiGe channel. The calibration procedure started again by obtaining reliable estimates for the source R_S and drain resistances R_D, the sideways-diffusion length (ΔL), as well as the low field hole mobility μ_{PO} and threshold voltage V_{TH}, using the method described in Section 4.1. The analysis yielded values of 90 Ω for the series source and drain resistance and values of 0.08 μm and 0.12 μm for ΔL in wafer 1 and wafer 2 respectively. Once again, vertical and

longitudinal mobilites with the dependence on electric field described by equations 4.7 and 4.8 have been considered. Taking extracted parameters as initial values, the parameters of μ_{PO}, F_C, R_S and R_D were determined by adjusting them to obtain the best fit to experimental $I_D \sim V_{GS}$ data at a low drain bias (-50 mV) for each channel length. These parameters were then kept constant, while v_{sat} and β were tuned, to obtain the closest agreement with the measured I_D-V_D characteristics for different gate voltages. Further details of the calibration procedure are given in Section 4.2.

At the end of calibration, any increase in v_{sat} with reduction of gate length may be attributed to the effects of non-equilibrium carrier transport. In order to confirm the presence of such effect, finally, ET simulations were employed, which properly consider non-equilibrium transport. The relaxation times required for the ET model have been obtained from the full band Monte Carlo (FBMC) bulk simulator [194].

By employing the calibration procedure described in Section 4.2, very good agreement between the measured and simulated characteristics for both wafers have been obtained, as can be seen in figures 4.16 to 18. The two most important figures of merit (μ_{PO} and v_{sat}) for different channel lengths, are given in table 4.3, for both wafers. The first (second) parameter in each table cell refers to the SiGe (Si) layer. Note that the low field mobility parameters in table 4.3 are consistent for each wafer. The $Si_{0.64}Ge_{0.36}$ channel exhibits a ~70% improvement in wafer 1, whereas wafer 2 sports an impressive 230% increase in mobility. The lower mobility in wafer 1 is speculated to be due to the influence of Si/SiO_2 interface on the scattering in the SiGe channel, enhanced as a result of the very thin Si cap layer (2 nm) [195].

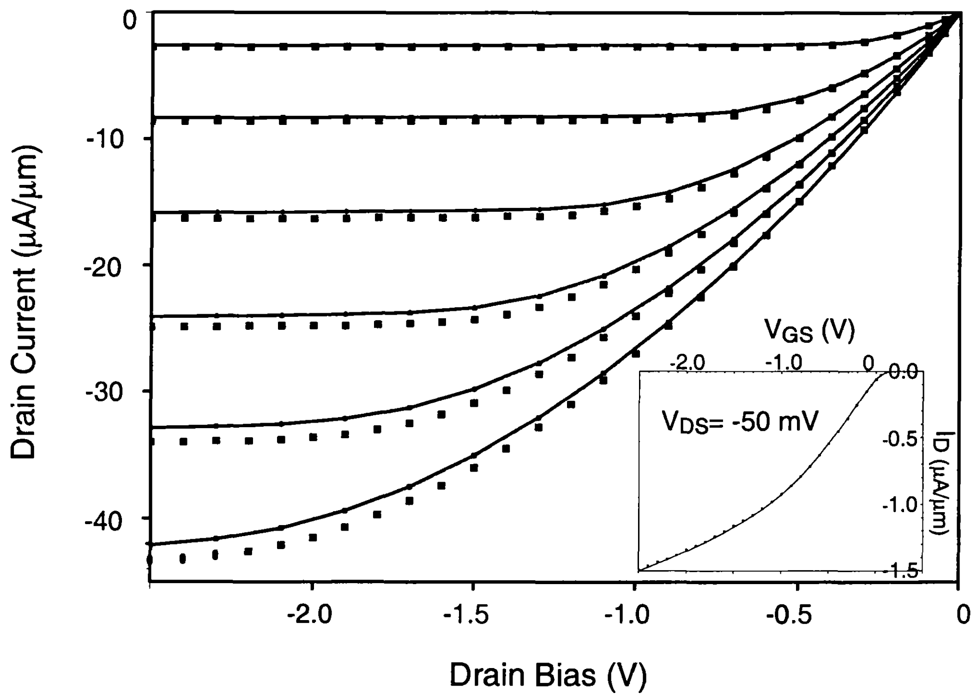


Figure 4.16 Comparison of the drain current versus drain voltage between measured (•) and simulated (—) data for wafer 2, L_{opt}=3 μm. The inserted picture shows the relationship between drain current and gate voltage.

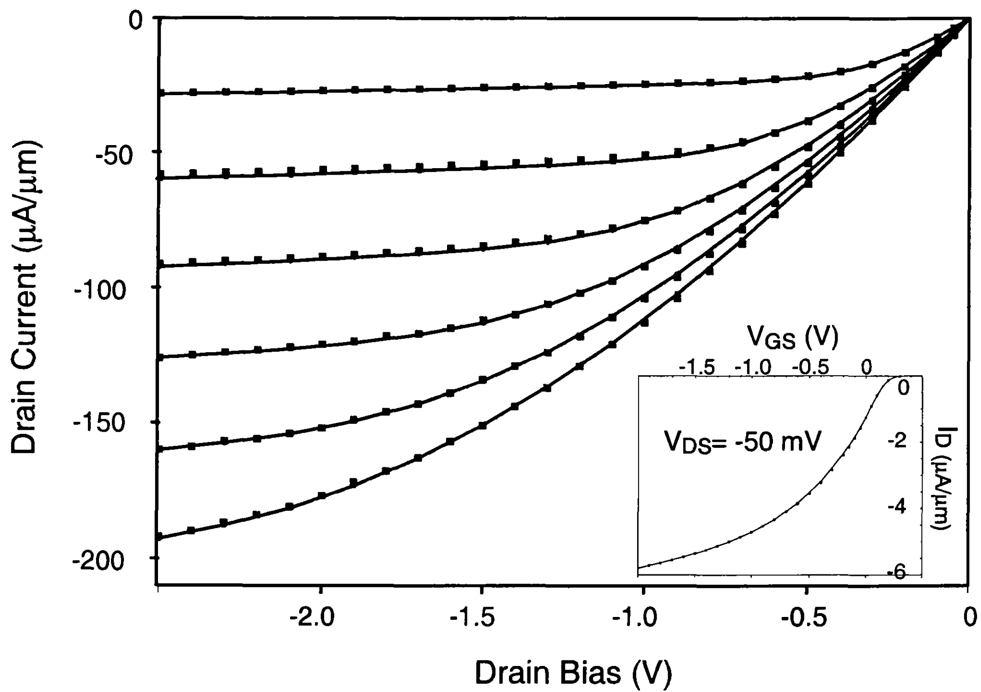


Figure 4.17 Comparison of the drain current versus drain voltage between measured (•) and simulated (—) data for wafer 2, L_{opt} = 0.5 μm. The inserted picture shows the relationship between drain current and gate voltage.

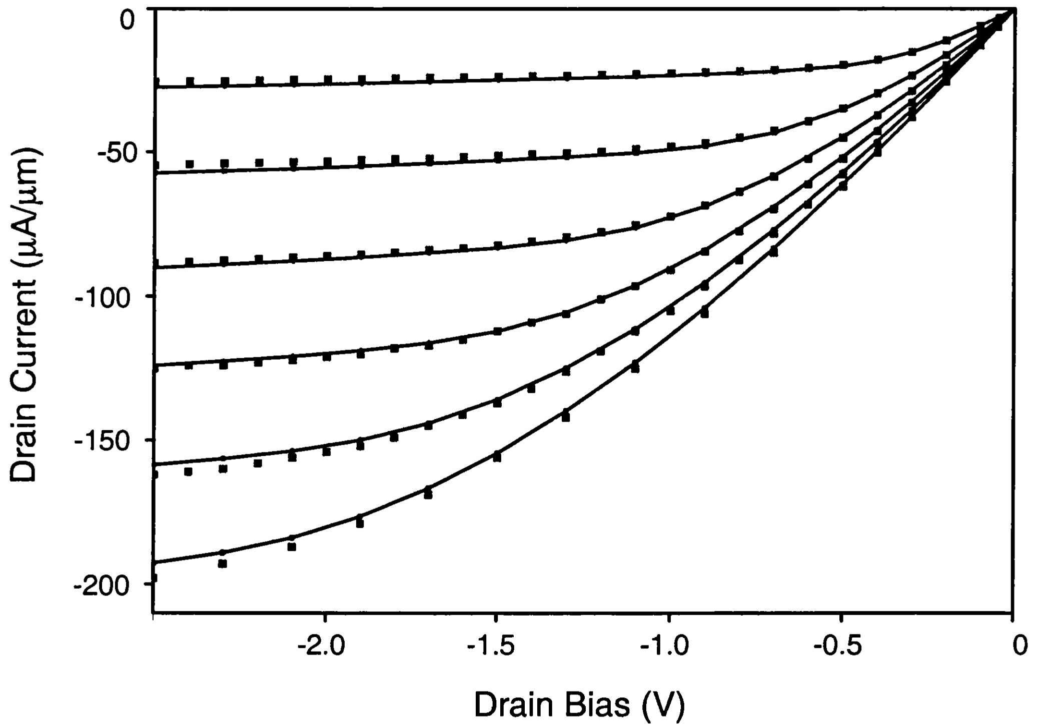


Figure 4.18 Comparison of the drain current versus drain voltage between measured (•) and simulated (—) data for wafer 1, $L_{opt} = 0.5$ μm

Wafer	$L(\mu m)$	$\mu(cm^2/Vs)$	$v_{sat}(10^7 cm/s)$
1	3.0	340/200	0.35/1
1	1.3	340/200	0.45/1
1	0.5	340/200	0.50/1
2	3.0	550/240	0.60/1
2	1.0	550/240	0.65/1
2	0.5	550/240	0.70/1

Table 4.3 Calibration parameters obtained. Two different Si cap thickness of 2 nm for wafer 1 and 8 nm for wafer 2 have been considered in the calibration process.

The implications of the calibration procedure are summarised in figure 4.19, where the longitudinal field versus hole velocity curves corresponding to values given in table 4.3 for both wafers were plotted. It is evident from the calibration procedure that the average

hole velocity in the channel increases as L_{opt} is scaled down to an effective channel length of 0.38 μm. It must be noted that, strictly within the calibration context, v_{sat} is different from the bulk saturation velocity and gives an indication of average carrier velocity in the channel. It is believed that non-equilibrium transport conditions in short channel devices (where the longitudinal electric field rapidly increases) are responsible for the increase in v_{sat}, required by the calibration process for good agreement with experiment. It has been found that velocity overshoot is expected to be more significant in SiGe p-MOSFETs than in Si devices, due to a larger relaxation time in the former as compared to the latter [194]. Hence, even though v_{sat} in strained SiGe is lower than bulk Si, non-equilibrium transport occurs in the former earlier.

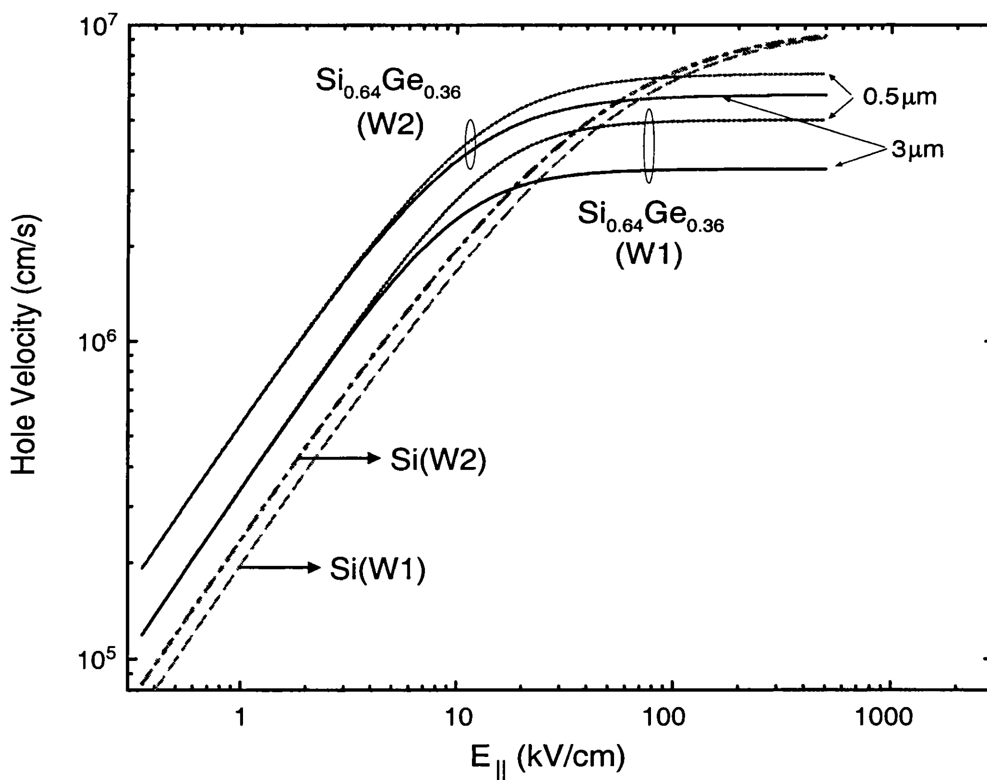


Figure 4.19 Velocity-field characteristics obtained from the calibration procedure.

At this point, it is useful to independently demonstrate the presence of non-equilibrium conditions in the devices. The ET model of MEDICI is used again to this end,

taking the energy relaxation times generated by the FBMC module. As shown in figure 4.20, for the shortest channel length the ET simulations agree with the experimental data and calibrated DD model. If, however, the DD simulation of the same device with v_{sat} obtained from the calibration of the long (3 μm) channel device has been repeated, the current is underestimated (figure 4.20). This confirms the accuracy of the calibration procedure and attest to the presence of non-equilibrium transport in the shortest device. Additional insight can be gained from the inset in figure 4.20, where the hole velocity profiles along the SiGe channel obtained from different models have been plotted. Firstly, ET velocity curves reach velocities above the saturation limit in the bulk [123] confirming the presence of non-equilibrium transport. Secondly, the DD velocities obtained using long channel (L_{opt} = 3 μm) calibration parameters in the short channel (L_{opt} = 0.5 μm) limit fails to reproduce the ET curve, in marked contrast with the calibrated DD simulations.

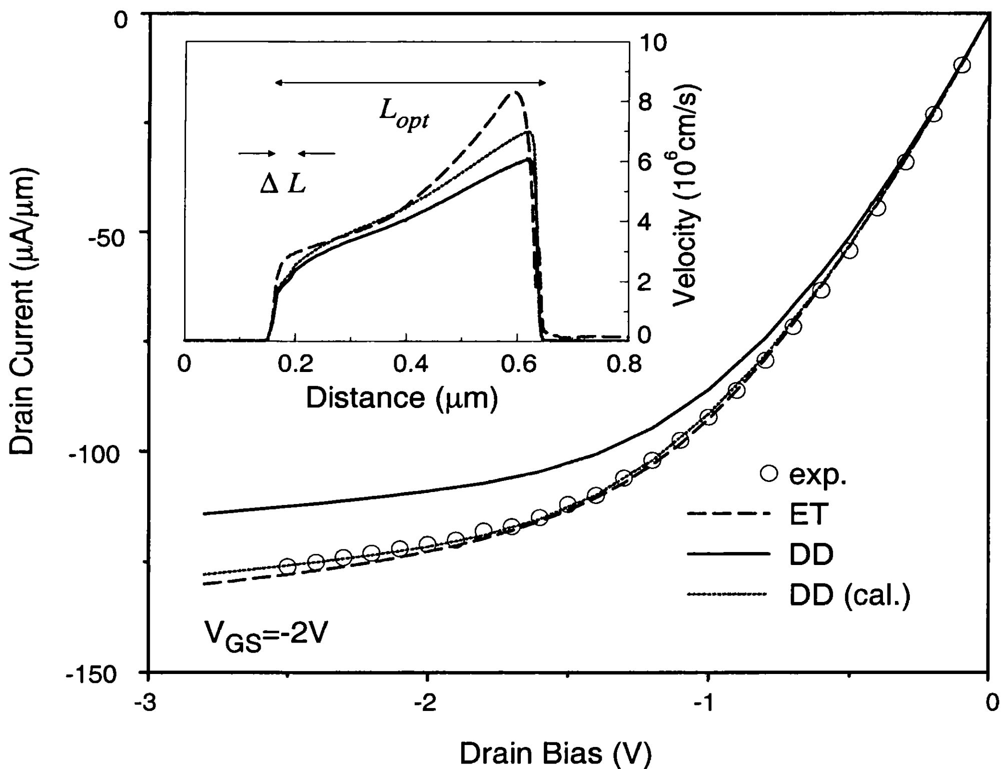


Figure 4.20 Comparison of DD and ET transport models in 0.5 μm p-MOSFETs. (wafer 2) V_{DS} = -2.5 V in the inset.

Finally, the thickness of Si cap has an important influence on the performance of SiGe p-MOSFETs is indicated. Although the devices with a thin Si cap have a lower mobility as discussed earlier, the drain currents in figures 4.17 and 4.18 are almost equal at V_{GS} = -3 V and V_{DS} = -2.5 V can be observed, for a channel length of 0.5 μm. This seemingly contradictory situation can be clarified, considering the Si cap mobility for both wafers in table 4.3 together with the parallel conduction observed in the thicker cap layers [71]. For a thick cap with a higher Si mobility, SiGe p-MOSFETs have significant parallel conduction with a populated 2DHG at the Si/SiO_2 interface. Consequently, the parallel conduction significantly reduces the drain current, along with the performance of these devices

4. 5 Summary

The $Si_{0.8}Ge_{0.2}$ p-MOSFETs fabricated especially for high-field transport studies and the $Si_{0.64}Ge_{0.36}$ p-channel MOSFETs fabricated with a CMOS compatible process in varying gate lengths and two different cap thickness have been calibrated and investigated. Enhanced low field mobility in SiGe layers compared to Si control devices has been observed. The use of a traditional drift diffusion simulator has been extended by a careful calibration of mobility parameters with respect to measured output characteristics. It has been found that the saturation velocity becomes strongly field dependent, and increases as the channel length is reduced. The accuracy of the calibration scheme has been verified against Monte Carlo calibrated hydrodynamic and energy transport models, confirming the presence of velocity overshoot and non-equilibrium transport processes along the channel. The increase in saturation velocity appears to be necessary for an appropriate calibration of hole velocity at the source end, which is subject to high fields in present devices. The results have indicated that the potential of SiGe pMOSFET's for velocity overshoot effects is considerably higher than Si counterparts, promising higher performance in the former at equal gate lengths at ultra-small devices.

The influence of the thickness of the Si cap layer in SiGe p-MOSFET architecture has also been examined. It has been found that the parallel conduction occurs more easily in a thick Si cap layer than in a thin Si cap layer, limiting the performance of Si/SiGe p-MOSFETs.

CHAPTER 5

Simulations Based SiGe p-MOSFETs Design

With the scaling of the devices to deep submicron dimensions, device modelling becomes essential in device design process. As devices are made ever smaller, many issues which have not been important in the past become significant. Among them are the drain induced barrier lowering, hot electron effects, non-equilibrium transport, etc. The physics of these phenomena can not be included in simple analytical deliberations and numerical simulation becomes mandatory.

The advantages of SiGe p-MOSFETs over conventional Si devices have been discussed in Section 2.1. However, problems have been encountered in realising the buried channel SiGe p-MOSFET, such as the confinement of holes in the SiGe channel. In addition, buried channel MOSFET design is more susceptible to short channel effects [196-200]. The short channel effects which are one of the fundamental electrical limitations for Si-VLSI [201-203], have been investigated widely in the past [204-210]. However, very little has been done to study these effects in short channel Si/SiGe devices [97]. In reference [91] short channel effects in single channel Si/SiGe devices were analytically discussed, and in reference [96, 97] a similar study using numerical simulations has been done for double quantum well p-MOSFETs.

In this chapter two generations of SiGe p-MOSFETs are designed and optimised using drift diffusion simulations. This is done in a hierarchical manner. First, the vertical layer structure design of SiGe p-MOSFETs is carried out, including the choice of gate material, the silicon cap and oxide thickness sensitivity and the SiGe profile in the channel. Second, some important parameters of the two dimensional device design of SiGe p-MOSFETs are analysed. Finally, the use of delta doping in designing SiGe p-MOSFETs are investigated.

5.1 Vertical Layer Structure Design

In order to maximise the device transconductance, the density of high mobility holes confined in the SiGe channel needs to be maximised while minimising the density of low mobility holes which flow at the Si/SiO_2 interface (silicon cap). The critical SiGe p-MOSFET design parameters, which affect the results, are the choice of gate material, the silicon-cap thickness, the gate-oxide thickness, and the SiGe profile within the channel (see figure 2.7). Unless otherwise specified in this section, the gate oxide is 10 nm thick and the doping of the n-type silicon substrate is 10^{16} cm^{-3}.

5.1.1 Choice of gate material

The type of gate material used in the SiGe p-MOSFET strongly affects the threshold voltage and the hole confinement in the SiGe channel. MEDICI simulation results plotted in figure 5.1 show the hole densities in the SiGe channel and in the parasitic Si channel at the Si/SiO_2 interface as a function of gate voltage for both a n^+- and a p^+- polysilicon gate SiGe p-MOSFET. The vertical channel profile of the SiGe devices consists of a 6 nm Si cap layer and a 10 nm wide $Si_{0.82}Ge_{0.18}$ channel. A uniform n-type doping of 10^{15} cm^{-3} is assumed throughout the Si and SiGe channels.

Both SiGe MOSFETs exhibit a similar behaviour: the SiGe channel turns on before the parasitic Si cap layer. The saturation of the SiGe channel hole density can be explained as follow: once a large number of holes appear in the silicon cap layer, their charge screens the gate potential and few holes are added to the SiGe channel with increasing gate voltage, limiting the maximum concentration of high mobility holes. A key figure of merit is the **Cross-Over-Voltage** which is the gate voltage at which the charge concentration in the SiGe channel and Si cap are equal. The p^+- and n^+- polysilicon gate SiGe p-MOSFETs show identical hole confinement, but the different workfunction of the gates results in a horizontal shift almost equal to the silicon bandgap.

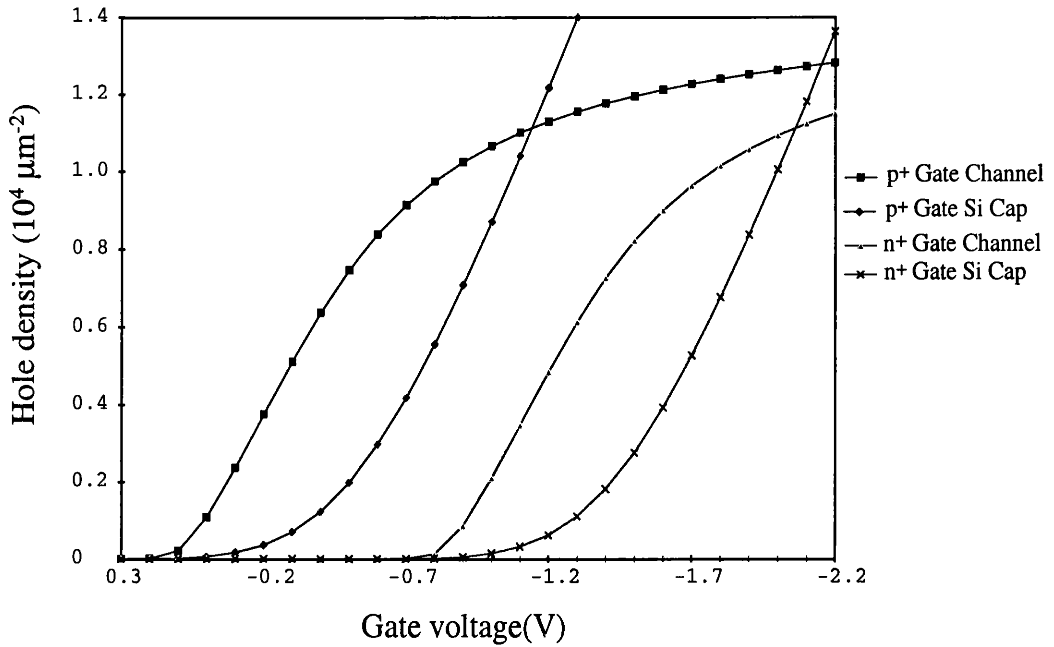


Figure 5.1 Hole density of the Si-cap and SiGe-channel versus gate voltage for p^+- and n^+-gate SiGe p-MOSFETs without threshold voltage adjustment.

As the threshold voltages given in figure 5.1 are not acceptable values for digital CMOS applications, n-type or p-type dopants are required to adjust V_{TH}. When the channel doping profile is adjusted such that both the p^+- and n^+- gate p-MOSFET have identical threshold voltage of -0.4 V, the hole density as plotted in figure 5.2 is obtained. The hole confinement in the SiGe channel for the n^+- gate design is significantly better than for the p^+- gate design. In the p^+- gate p-MOSFET, conduction in the Si-cap layer at the SiO_2/Si interface appears shortly after threshold and the cross-over voltage is as low as -0.7 V. For the n^+- gate design, the cross-over voltage exceeds -2.2 V. Furthermore, for the n^+- gate design, the additional holes supplied by the p-type dopants significantly increases the maximum number of holes within the SiGe channel. So for identical Si-cap and SiGe channels, the n^+ polysilicon gate SiGe p-MOSFET can be designed for operation at higher power supply voltages than the p^+ polysilicon gate SiGe p-MOSFET.

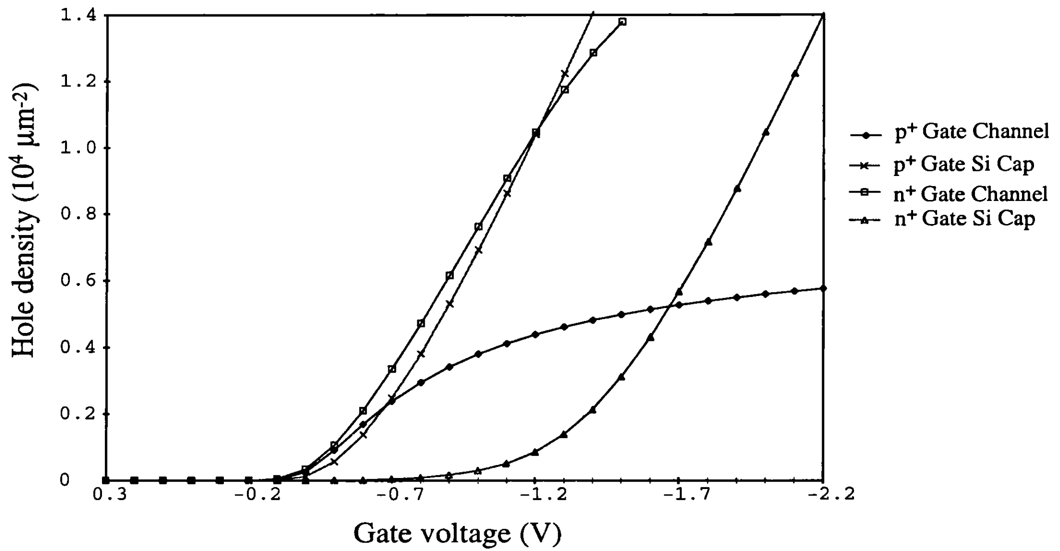


Figure 5.2 Hole density of the Si-cap and SiGe-channel versus gate voltage for p^+- and n^+-gate SiGe p-MOSFETs with a -0.4 V threshold voltage. For p^+-gate design, a uniform n-type doping profile of 2×10^{17} cm^{-3} over 50 nm is used. For the n^+-gate design, a uniform p-type doping profile of 1.5×10^{17} cm^{-3} over 50 nm is used.

5.1.2 Silicon cap and oxide thickness sensitivity

To maximise the gate-to-channel capacitance and hence increase the SiGe MOSFET transconductance, it is important to minimise both the thickness of the silicon cap and that of the gate oxide. MEDICI simulations indicate that decreasing the Si-cap thickness increases the cross-over voltage. In contrast reducing the gate oxide thickness has the opposite effect, decreasing the cross-over voltage. This is illustrated in figure 5.3 where the ratio of holes present in the Si-cap layer over those confined in the SiGe channel is plotted as a function of Si-cap thickness for both the n^+- and p^+- gate designs and for two different gate oxide thickness. The integrated dopant dose is adjusted such that for both designs and for a 10 nm gate oxide, a 6 nm Si-cap and a 10 nm $Si_{0.82}Ge_{0.18}$ channel, a device threshold voltage of -0.4 V is obtained. For the n^+- gate p-MOSFET, most holes remain confined to the SiGe channel for Si caps as thick as 8 nm. For p^+- gate

with a 5 nm gate oxide, the cap thickness must be on the order of 2 nm or less to confine the holes in the SiGe channel for gate voltages up to -1.5 V.

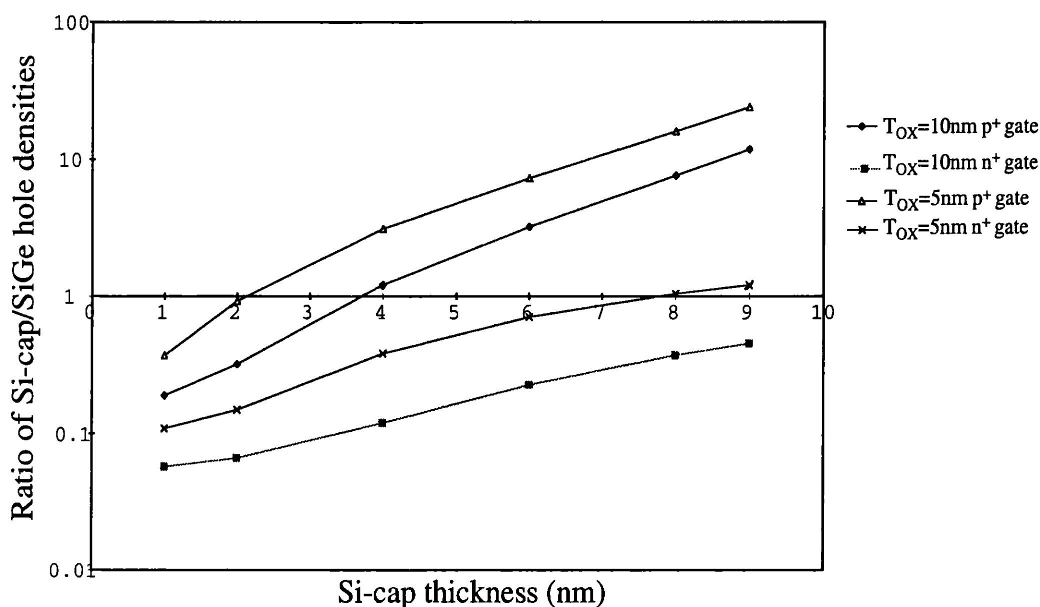


Figure 5.3 Ratio of hole concentration flowing in the Si-cap and the SiGe channel versus varying Si-cap thickness (V_{GS} = -1.5 V).

For Si-cap thicknesses below 2 nm, the p^+-gate design becomes an attractive alternative to the n^+-gate SiGe p-MOSFET. However, several trade-offs affect SiGe MOSFETs with narrow cap thickness. For example, because the current flows less than 2 nm away from the gate oxide, interface scattering may easily degrade the hole mobility; but with a thin Si-cap, the holes within the SiGe channel flow closer to the gate and the channel-to-gate capacitance increases. So the Si-cap thickness needed to optimise the transconductance is determined by a mobility/capacitance trade-off.

5.1.3 SiGe profile in the channel

Hole confinement in the SiGe channel is largely dependent on the Ge profile of the SiGe channel. To maximise the hole concentration in the SiGe channel and to insure adequate confinement at high gate voltages, a large valence band discontinuity at the uppermost Si/SiGe heterointerface is required. A high Ge concentration is required to

achieve this. The cross-over voltage versus the Ge concentration in the channel is plotted in figure 5.4. The cross-over voltage is linearly proportional to the percentage concentration of Ge. However, pseudomorphic epitaxial SiGe film is highly strained and must remain stable throughout device fabrication, placing a limitation on the SiGe thickness. As the Ge concentration increases, the maximum of SiGe layer thickness decreases, resulting in another trade-off problem.

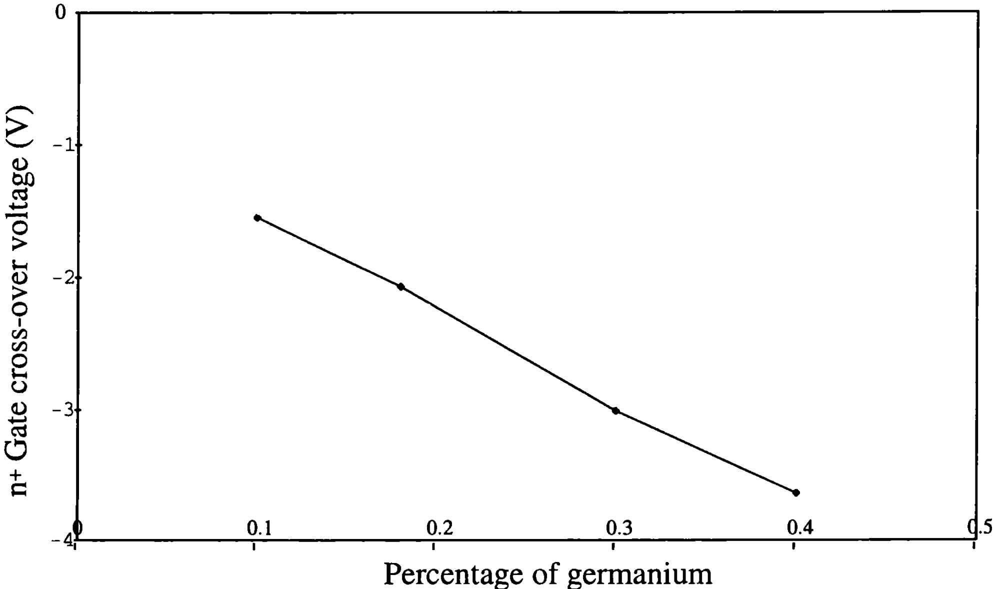


Figure 5.4 n^+-Gate cross-over voltage versus percentage of germanium in the SiGe channel for a constant Ge profile. No threshold voltage adjustment was used in these devices.

5.2 Two Dimensional Device Design

Two-dimensional MEDICI simulations were carried out to optimise 0.5 μm and 0.1 μm SiGe p-channel MOSFETs. The efforts have concentrated on optimum threshold voltage control, reducing the two-dimensional effects (threshold voltage roll off), and improving the subthreshold slope.

In the process of design three major components of SiGe p-MOSFETs were investigated.

(a) effect of the punchthrough buffer concentration;

(b) effect of the buffer thickness in the case of undoped buffers;

(c) the effect of delta doping for threshold voltage control.

All of which are indicated in figure 5.5.

Generally the definition of threshold voltage is not agreed upon. Throughout this work the same practical definition has been utilised. The V_{TH} is defined as:

$$V_{TH} = V_{GS} \text{ for which } I_{DS}=I_{TH}=(\frac{Weff}{Leff})\times 10^{-7} \text{ A}$$

where W_{eff} is the effective channel width, and L_{eff} is the effective channel length (both in microns).

In a similar approach, the drain induced two-dimensional effects are monitored by the V_{TH} *roll off*. This parameter is based on simulation of V_{TH} at two drain biases and defined as:

$$V_{TH} \textit{ roll off} = V_{TH} \text{ (at } V_{DS}= -0.01 \text{ V)} - V_{TH} \text{ (at } V_{DS} = -2 \text{ V)}$$

The subthreshold slope, S, is defined as:

$$S=V_2 \text{ (at } V_{DS} = -2 \text{ V)} - V_1 \text{ (at } V_{DS} = -2 \text{ V)}$$

where $V_2=V_{GS2}$ for which $I_{DS}=I_2=(\frac{Weff}{Leff})\times 10^{-8}$A and $V_1=V_{GS1}$ for which $I_{DS}=I_1=(\frac{Weff}{Leff})\times 10^{-7}$A.

Usually S ranges should be from 80 mV to 120 mV and V_{TH} *roll off* $\leq$ 200 mV. Parameters S and V_{TH} *roll off* are very important in a proper analysis of short channel effects in MOSFETs. Since they can be determined only by two dimensional simulations and require several points for a proper determination DD simulations are really the only viable option in such a design process.

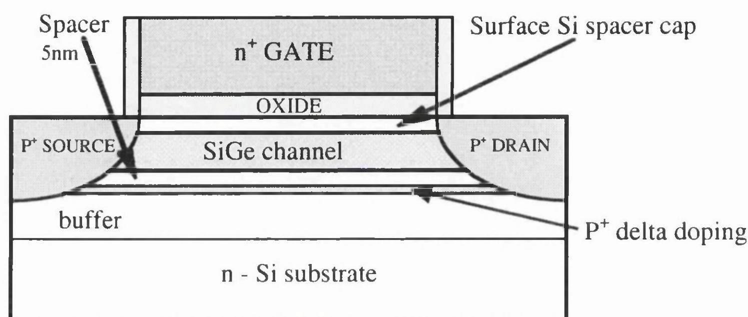


Figure 5.5 SiGe channel p-MOSFET structure.

5.2.1. MOSFETs with channel length 0.5 μm

Although current industry standards are around 0.15 μm devices [4], larger structures still have their "rich" applications, such as micropower circuits. In addition, many first experimental demonstration of SiGe MOSFET is based on devices of similar gate length. It is also useful to probe the advantages of SiGe p-MOSFETs as a function of gate length. The p-MOSFET structure similar to the one shown in figure 5.5 is designed in this phase of the work. A n^+ polysilicon gate is chosen because it has higher cross-over-voltage than p^+ polysilicon gate. A surface silicon spacer cap (t_{CAP} = 1 nm) is used to prevent the interface scattering from the gate oxide. The thickness of SiGe channel is 10 nm with 18% Ge mole fraction. P^+ delta doping is used to adjust the threshold voltage of the device. Silicon spacer (t_{spa} = 5 nm, unless otherwise specified in this section) is employed to separate the channel and the delta doping. The top three layers are assumed to be lightly doped (10^{15} cm^{-3}) in order to maximise the mobility in the region where a significant portion of the current flows. In order to reduce two-dimensional effects a heavily doped buffer ($\geq 5\times10^{16}$ cm^{-3}) is used. The thickness of the buffer is 200 nm, unless

otherwise specified in this section. A substrate doping concentration of 10^{15} cm^{-3} is used. An oxide thickness of 10 nm is assumed for the 0.5 μm device.

A. The effect of the punchthrough buffer concentration

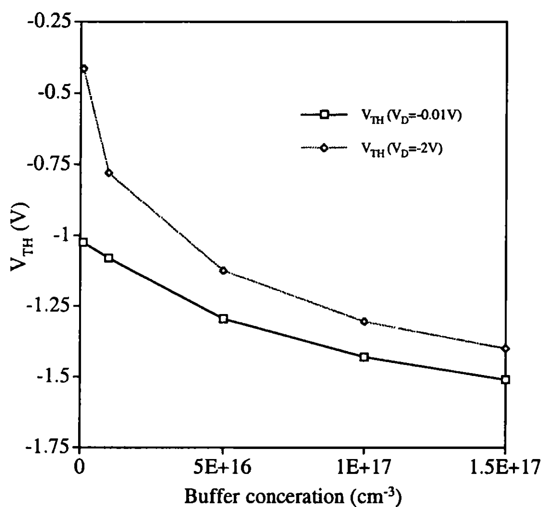


Figure 5.6 Threshold voltage versus buffer concentration. No delta doping is used.

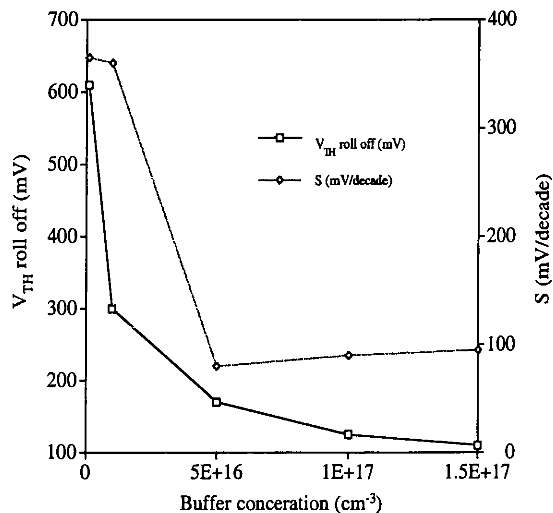


Figure 5.7 Threshold voltage roll off and subthreshold slope versus buffer concentration. No delta doping is used.

The buffer can be used as the punchthrough stopper to prevent two-dimensional effects if it is doped properly. The reason is that the punchthrough stopper decreases the probability of drain to source field penetration [201-204]. Figures 5.6 to 5.9 illustrate the dependence of threshold voltage, sub-threshold slope and threshold voltage roll off on the punchthrough buffer concentration N_{PT}. V_{TH} decreases (becomes more negative) as the buffer concentration increases. Hence, a high delta doping is needed when the punchthrough buffer is heavily doped in order to keep V_{TH} under control. In the case of the n^+-polysilicon gate when $N_{PT} < 5\times10^{16}$ cm^{-3}, both V_{TH} *roll off* and S are unsatisfactory because of pronounced two-dimensional effects. After $N_{PT} \geq 5\times10^{16}$ cm^{-3}, V_{TH} *roll off* and S become acceptable for a delta doping concentration of 0 or 1.5×10^{12} cm^{-2}. As V_{TH} *roll off* (1.5×10^{12})>V_{TH} *roll off* (0), delta doping makes threshold voltage roll off more

pronounced. Therefore, the delta doping concentration used in practical devices should be limited to avoid strong two-dimensional effects.

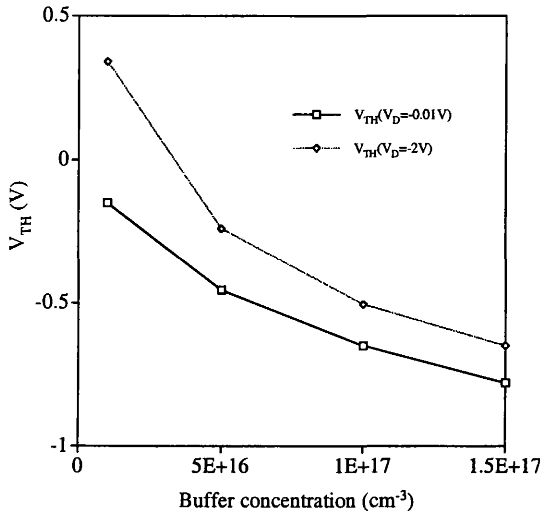


Figure 5.8 Threshold voltage versus buffer concentration. Delta doping is 1.5×10^{12} cm^{-2}.

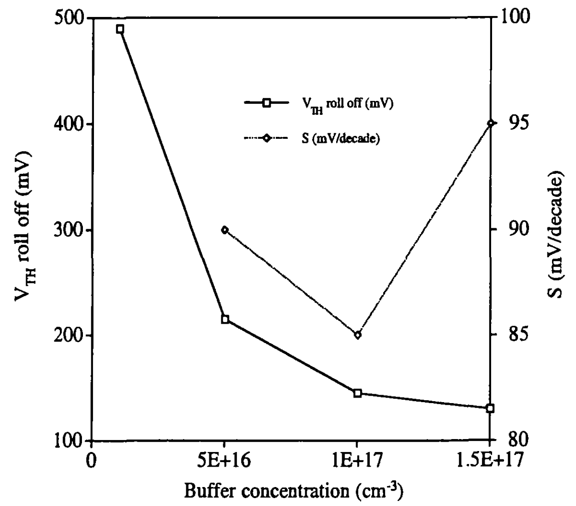


Figure 5.9 Threshold voltage roll off and subthreshold slope versus buffer concentration. Delta doping is 1.5×10^{12} cm^{-2}.

B. The effect of the undoped buffer thickness

It was decided that in the first batch the buffer grown between the Si-substrate and the channel would be undoped and the suppression of the short channel effects would be achieved by using substrates with high doping concentration. Figures 5.10 and 5.11 illustrate the dependence of threshold voltage, sub-threshold slope and threshold roll off on the buffer thickness t_{Buf}. The threshold voltage increases as the buffer thickness increases. At the same time, the V_{TH} *roll off* increases. It is important to note that S decreases initially when $t_{Buf} < 10$ nm and then increases when $t_{Buf} > 10$ nm. This means that the threshold voltage roll off begins to effect the device at the point when $t_{Buf} = 10$ nm, although its value remains relatively small, running from 139 mV to 155 mV.

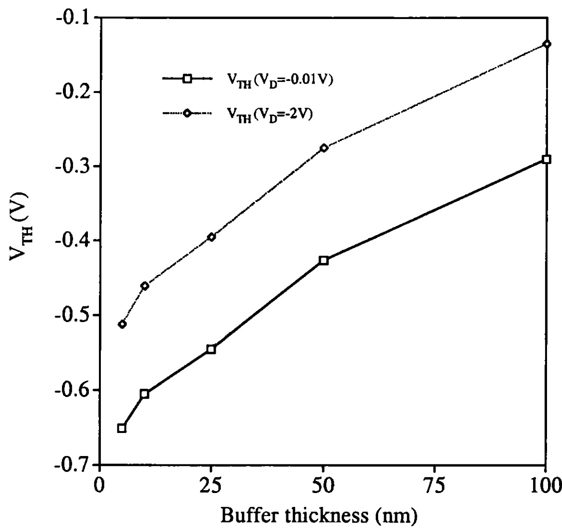


Figure 5.10 Threshold voltage versus undoped buffer thickness. The delta doping is 1.5×10^{12} cm^{-2}, the substrate concentration is 10^{17} cm^{-3}.

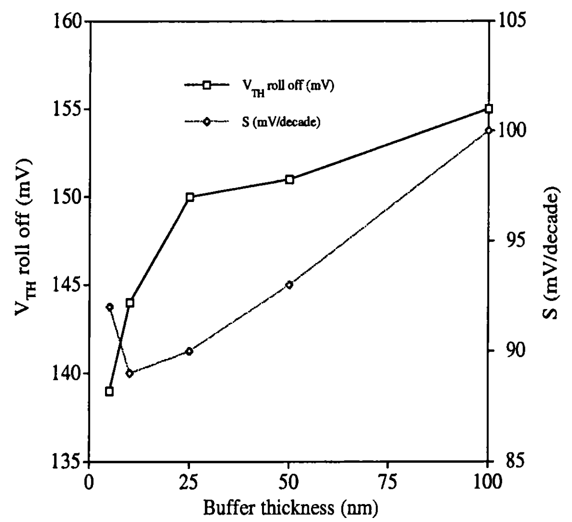


Figure 5.11 Threshold voltage roll off and subthreshold slope versus undoped buffer thickness. The delta doping is 1.5×10^{12}cm^{-2}, the substrate concentration is 10^{17} cm^{-3}.

C. The effect of delta doping for threshold voltage control

Although the delta doped layer is separated from the channel by a spacer layer, it still controls a fraction of holes from the channel, causing a shift in the threshold voltage. Thus, the n^{+}-polysilicon gate structures with n doped buffer underneath the channel may require a larger delta doping for threshold voltage control. Figures 5.12 and 5.13 illustrate the dependence of threshold voltage, sub-threshold slope and threshold voltage roll off on the delta doping concentration. The threshold voltage increases by approximately 0.05 V if the delta doping concentration is increased by 10^{11} cm^{-2}. Both S (from 83 mV to 95 mV) and V_{TH} *roll off* (from 115 mV to 150 mV) change with delta doping dose variation (from 0 to 2×10^{12} cm^{-2}). The delta doping however, should be kept as low as possible to avoid parallel conductance in the delta layer.

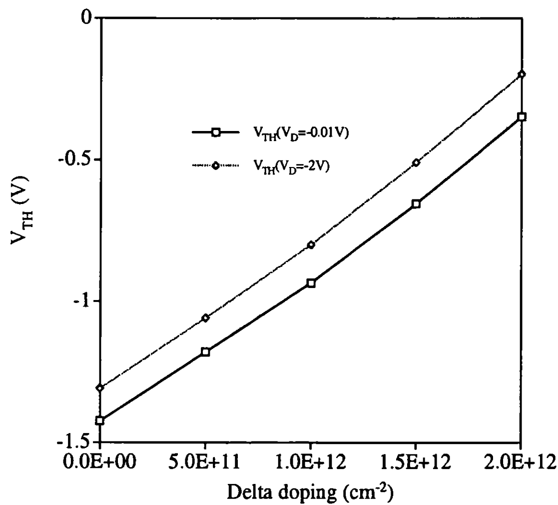


Figure 5.12 Threshold voltage versus delta doping. Buffer concentration is 10^{17} cm^{-3}.

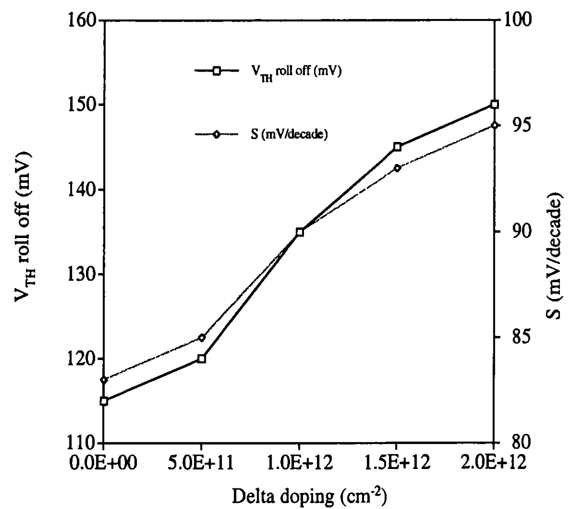


Figure 5.13 Threshold voltage roll off and subthreshold slope versus delta doping. Buffer concentration is 10^{17} cm^{-3}.

5.2.2. MOSFETs with channel length 0.1 μm

As the channel length of the device is scaled to 0.1 μm, its oxide thickness has to be reduced correspondingly. An oxide thickness of 3 nm is assumed for the 0.1 μm device. A n^+ polysilicon gate is chosen because it has higher cross-over-voltage than p^+ polysilicon gate. A surface silicon spacer cap (t_{CAP} = 1 nm) is used to prevent the interface scattering from the gate oxide. The thickness of SiGe channel is 10 nm with a 18% Ge mole fraction. A p^+ delta doping is used to adjust the threshold voltage of the device. A silicon spacer (t_{spa} = 5 nm, unless otherwise specified in this section) is employed to separate the channel and the delta doping. The top three layers are assumed to be lightly doped (10^{15} cm^{-3}) in order to maximise the mobility in the region where a significant portion of the current flows. In order to reduce two dimensional effects a heavily doped buffer is used. The thickness of the punchthrough buffer is 200 nm, unless otherwise specified in this section. A substrate doping concentration of 10^{15} cm^{-3} is used.

A. The effect of the punchthrough buffer concentration

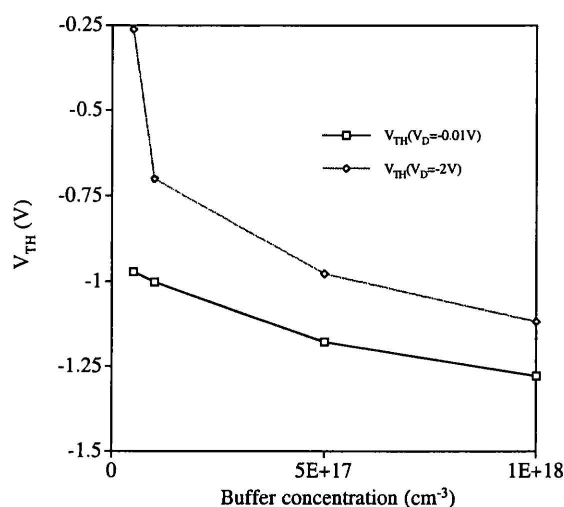


Figure 5.14 Threshold voltage versus buffer concentration. No delta doping is used.

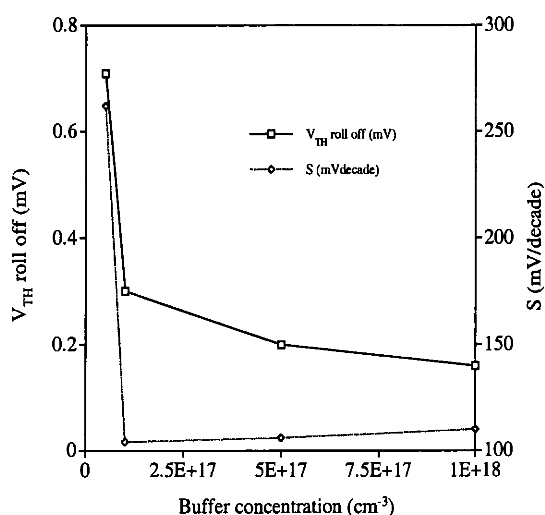


Figure 5.15 Threshold voltage roll off and subthreshold slope versus buffer concentration. No delta doping is used.

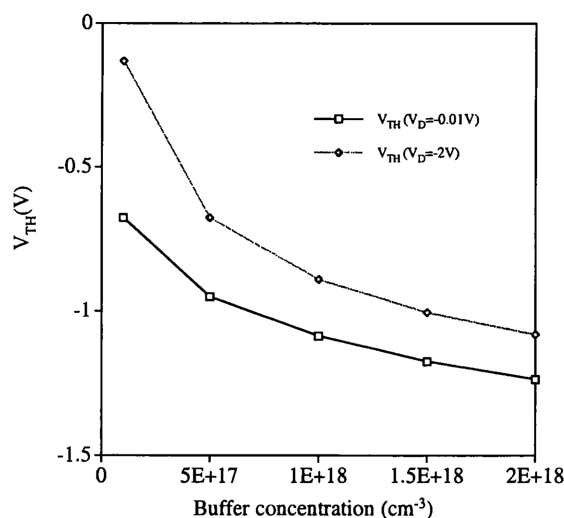


Figure 5.16 Threshold voltage versus buffer concentration. Delta doping is 1.5×10^{12} cm^{-2}.

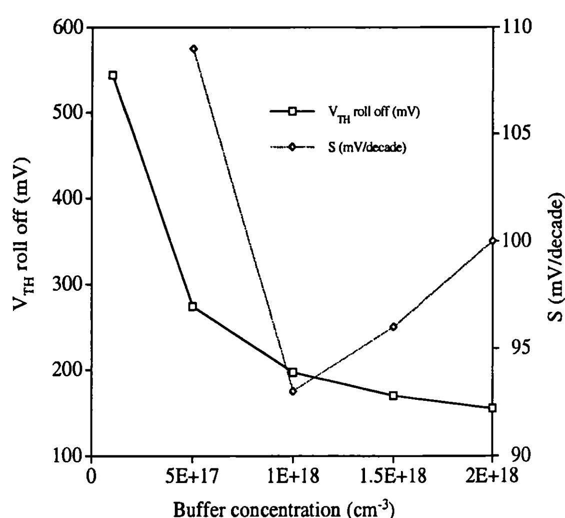


Figure 5.17 Threshold voltage roll off and subthreshold slope versus buffer concentration. Delta doping is 1.5×10^{12} cm^{-2}.

Figures 5.14 to 5.17 illustrate the dependence of threshold voltage, sub-threshold slope and threshold voltage roll off on the punchthrough buffer concentration N_{PT}. The V_{TH} *roll off* is too high for $N_{PT} \leq 5\times10^{17}$ cm^{-3}, however for $N_{PT} \geq 5\times10^{16}$ cm^{-3}, the V_{TH} *roll*

off and S become acceptable for a 0.5 μm device. The threshold voltage roll off is more serious if delta doping is used. Therefore a heavily doped punchthrough buffer should be used for 0.1 μm devices. The reason for this is the larger probability of drain to source field penetration for 0.1 μm devices than 0.5 μm devices.

B. The effect of the undoped buffer thickness

Figures 5.18 and 5.19 illustrate the dependence of threshold voltage, sub-threshold slope and V_{TH} *roll off* on the buffer thickness t_{Buf}. It can be seen that V_{TH} *roll off* and S are not acceptable after $t_{Buf} \geq 25$ nm. Even if $t_{Buf} = 10$ nm, the V_{TH} *roll off* = 222 mV. Because the buffer layer is undoped, an increase in its thickness amounts to decrease in the integral charges underneath the channel, resulting in worse two-dimensional effects in MOSFETs. Thus a rather thin buffer must be used for short channel p-MOSFETs.

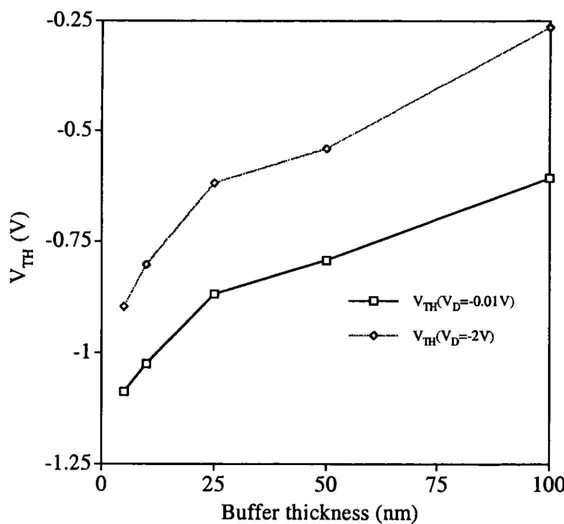


Figure 5.18 Threshold voltage versus undoped buffer thickness. The delta doping is 1.5×10^{12} cm^{-2}, the substrate concentration is 10^{18} cm^{-3}.

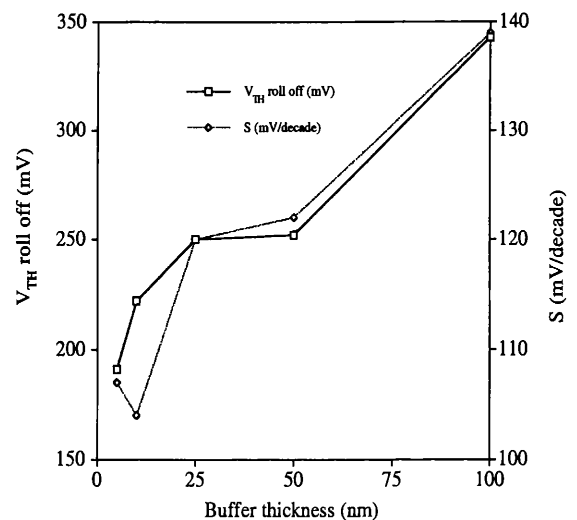


Figure 5.19 Threshold voltage roll off and subthreshold slope versus undoped buffer thickness. The delta doping is 1.5×10^{12} cm^{-2}, the substrate concentration is 10^{18} cm^{-3}.

C. The effect of delta doping for threshold voltage control

Figures 5.20 and 5.21 illustrate the dependence of threshold voltage, sub-threshold slope and threshold voltage roll off on the delta doping concentration. The threshold voltage increases by approximately 0.013 V if the delta doping concentration increase 10^{11} cm^{-2}. Both S (from 83 mV to 104 mV) and V_{TH} *roll off* (from 171 mV to 220 mV) change with the delta doping concentration variation (from 0 to 2×10^{12} cm^{-2}). It is clear that the optimum threshold voltage control and the suppression of short channel effects in 0.1 μm p-channel SiGe devices, requires further careful consideration.

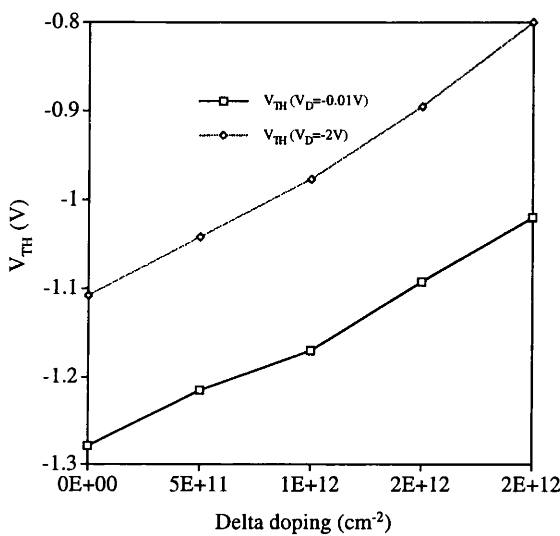


Figure 5.20 Threshold voltage versus delta doping. Buffer concentration 10^{18} cm^{-3}.

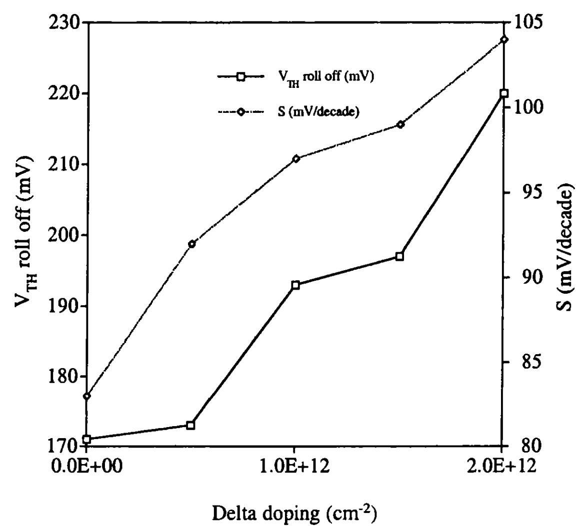


Figure 5.21 Threshold voltage roll off and subthreshold slope versus delta doping. Buffer concentration 10^{18} cm^{-3}.

5.3 Investigation of Delta Doped SiGe p-MOSFETs

Following the discussions between the partner groups on the design of SiGe p-channel MOSFETs, devices utilising a delta doped supply layer with varying channel lengths down to 0.1 μm were considered. A set of initial simulations were performed using

MEDICI to determine the threshold voltage, subthreshold slope and threshold voltage roll off (*V_{TH} roll off*) in such devices.

The basic device structure (as shown in figure 5.5) consists of a heavily doped n-type substrate, varying from $N = 5\times10^{17}$ cm^{-3} to $N = 5\times10^{18}$ cm^{-3} as required for adjusting threshold voltage. The parasitic charge at the substrate/buffer interface is of approximately 2×10^{11} cm^{-2}. The buffer is considered to be undoped with delta doping layer placed half way into the buffer layer. The SiGe channel/quantum well is 6 nm wide, with a Ge mole fraction of 50%, and is nominally undoped. This vertical structure is then capped with a 4 nm Si cap layer. The oxide below the n$^+$-poly gate is either 4 nm or 6 nm depending on the simulations performed.

5.3.1 The variation of the effective channel length

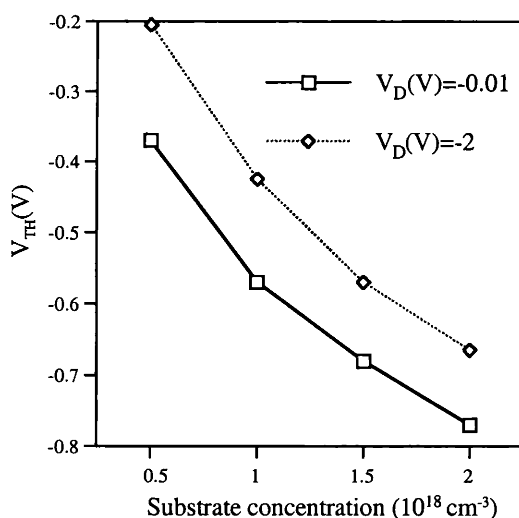


Figure 5.22 Threshold voltage versus substrate concentration.

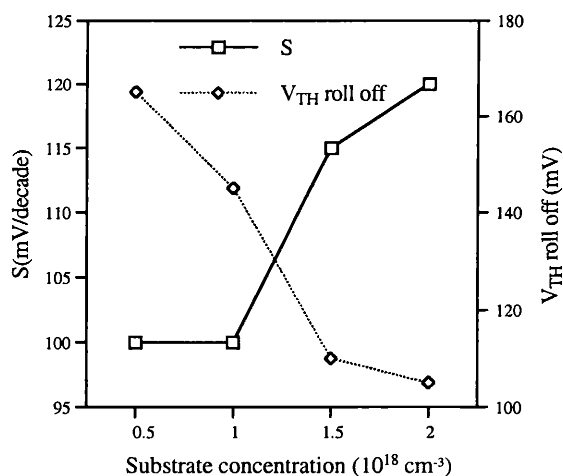


Figure 5.23 Subthreshold slope and threshold voltage roll off versus substrate concentration.

In these simulations a delta doped layer of 3×10^{12} cm^{-2} has been used, with an oxide thickness of 6 nm, and a junction depth of 0.1 μm. These values were chosen to agree with practical fabrication limitations in the SiGe project consortium. The substrate concentration has been varied to obtain a threshold voltage of around -0.5 V with

satisfactory subthreshold slope and threshold voltage roll off for a channel length of 0.5 μm, shown in figures 5.22 and 5.23, respectively. It is found that a substrate concentration of around 10^{18} cm^{-3} is required. This concentration was used to investigate the threshold voltage, subthreshold slope and threshold voltage roll off, variation as a function gate length down to an effective gate length of 0.1 μm, shown in figures 5.24 and 5.25, respectively. It is straightforward to conclude from these results that the basic design has an optimum above 0.2 μm but shows unacceptable short channel effects below 0.15 μm. Consequently, the effects of varying the delta doping concentration and oxide thickness in very short channel devices have been investigated. These simulations are described in further detail below.

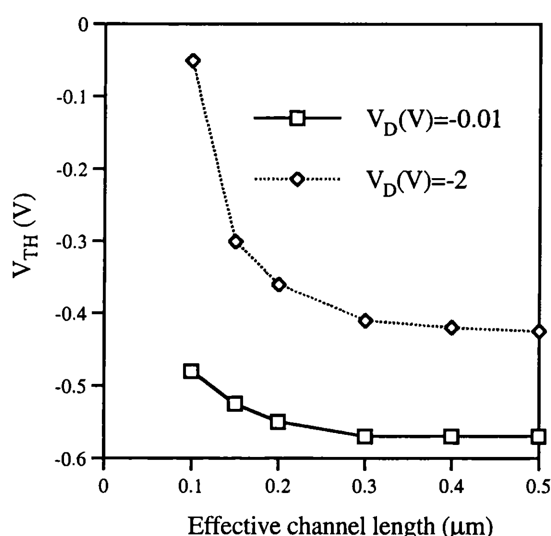


Figure 5.24 Threshold voltage versus effective channel length.

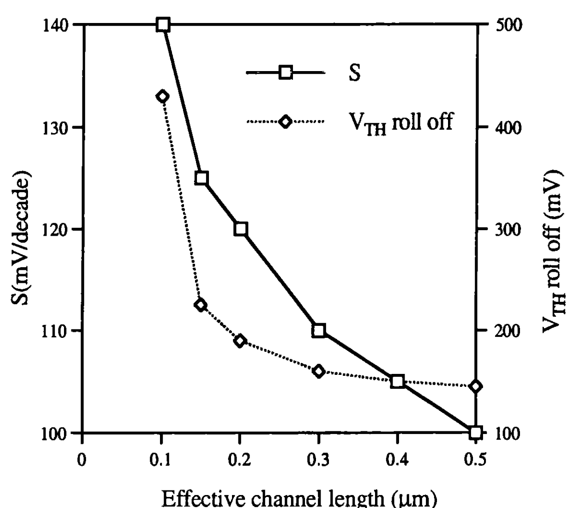


Figure 5.25 Subthreshold slope and threshold voltage roll off versus substrate concentration.

5.3.2 The effects of the thickness of the gate oxide

The thickness of the gate oxide has a strong influence on device operation. To improve the scaling of the channel length it has been reduced from 6 nm to 4 nm, while the other parameters are left unchanged. The devices characteristics as a function of gate length (from 0.5 μm to 0.1 μm) have been re-investigated. Figures 5.26 and 5.27, show

the threshold voltage, subthreshold slope and threshold voltage roll off respectively. It can be observed that the subthreshold slope and threshold voltage roll off for 0.15 μm channel length are improved. However, for a 0.1 μm device, the device characteristics are still unsatisfactory, therefore in order to reduce the observed short channel effects the dependence on the substrate concentration have also been re-investigated. The results from which are discussed and presented below.

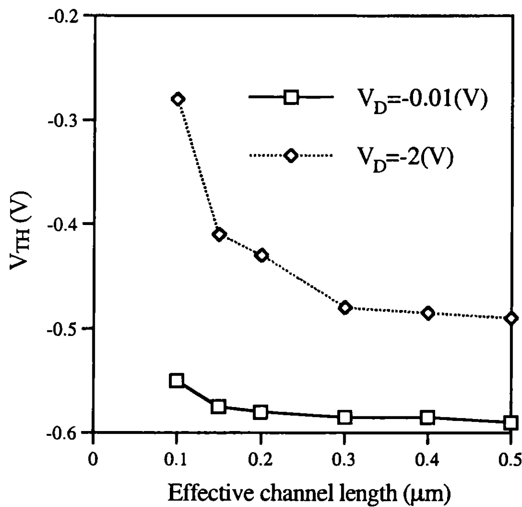


Figure 5.26 Threshold voltage versus effective channel length (T_{OX} = 4 nm).

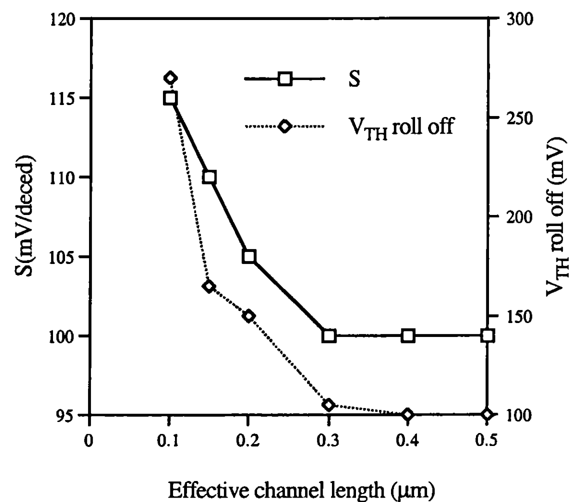


Figure 5.27 Subthreshold slope and threshold voltage roll off versus effect channel length (T_{OX} = 4 nm).

5.3.3 The effects of the substrate concentration and the delta doping

Simulations have been performed for a 0.1 μm p-MOSFET structure, with a delta doping of 3×10^{12} cm^{-2} and oxide thickness of 4 nm as before. Results for the threshold voltage, subthreshold slope and threshold voltage roll off versus substrate concentration are presented in figures 5.28 and 5.29 respectively, with substrate concentrations ranging from 10^{18} to 5×10^{18} cm^{-3}. Although increasing the substrate concentration has the desired affect of reducing the threshold voltage roll off, it is clear that the threshold voltage roll off criterion of approximately < 200 mV can not be achieved for a 0.1 μm device, even with a substrate concentration of 5×10^{18} cm^{-3}. The effects of reducing the delta doping have been investigated further in an attempt to improve short channel performance.

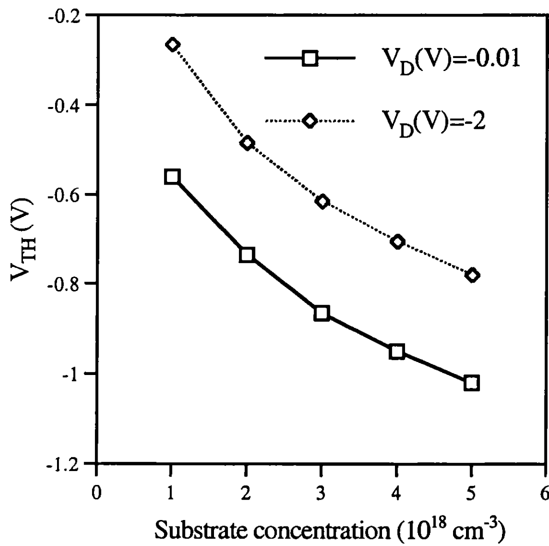


Figure 5.28 Threshold voltage versus substrate concentration.

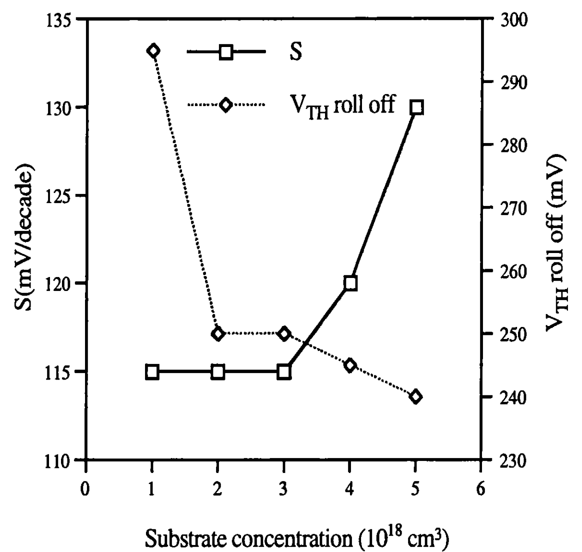


Figure 5.29 Subthreshold slope and threshold voltage roll off versus substrate concentration.

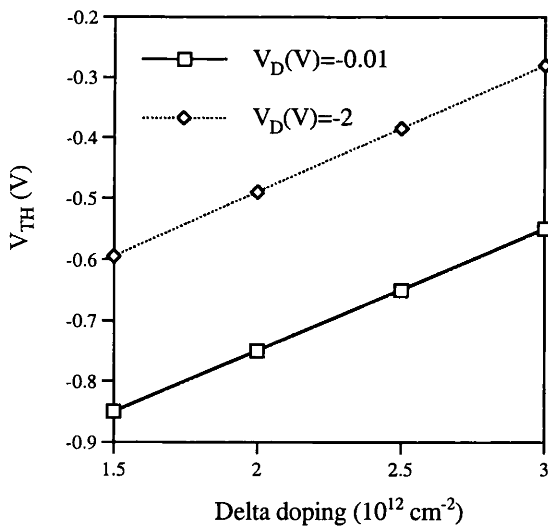


Figure 5.30 Threshold voltage versus delta doping ($N = 10^{18}$ cm^{-3}).

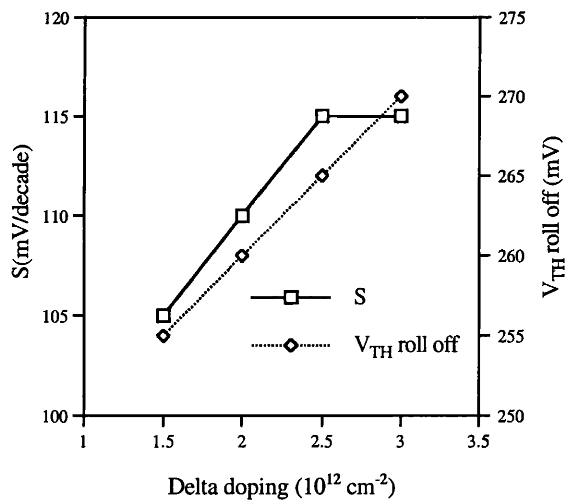


Figure 5.31 Subthreshold slope and threshold voltage roll off versus delta doping ($N = 10^{18}$ cm^{-3}).

Figures 5.30 and 5.31 show the threshold voltage, the subthreshold slope and threshold voltage roll off for 0.1 μm device with a substrate concentration of 10^{18} cm^{-3}.

For this substrate concentration the threshold voltage roll off is clearly unsatisfactory. No matter what the delta doping level is, in figures 5.32 and 5.33 the same results are presented as in figures 5.30 and 5.31, but this time with a substrate concentration of 4×10^{18} cm^{-3}. For a substrate concentration of 4×10^{18} cm^{-3}, both subthreshold slope and threshold voltage roll off are still unsatisfactory, although they became a little better. So this means that it is not possible to get satisfactory improvement of the short channel effects for 0.1 μm device, by increasing the substrate concentration or decreasing the delta doping if the oxide thickness is kept at 4 nm.

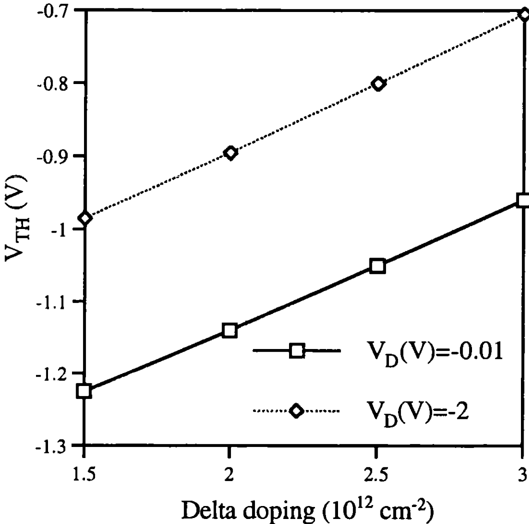


Figure 5.32 Threshold voltage versus delta doping ($N = 4\times10^{18}$ cm^{-3}).

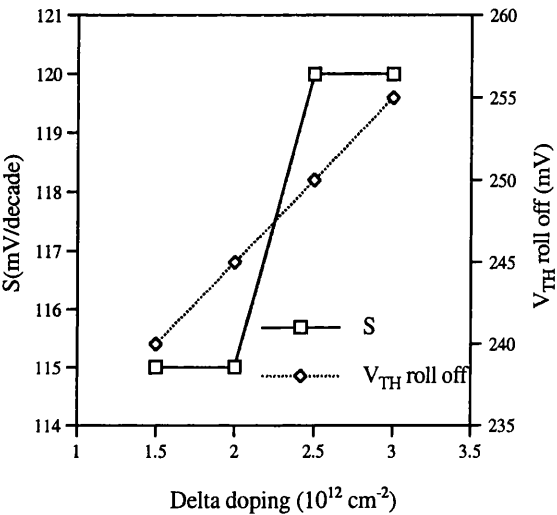


Figure 5.33 Subthreshold slope and threshold voltage roll off versus delta doping ($N = 4\times10^{18}$ cm^{-3}).

5.4 Summary

The main points arising from the results of the simulations presented above, for 0.5 μm and 0.1 μm Si/SiGe p-channel MOSFETs, are summarised below:

- The threshold voltage roll off can be avoided using a punchthrough buffer, such as in the simulations. When a delta doping of 1.5×10^{12} cm^{-2} is used in order to adjust the threshold voltage to around -0.5 V, the buffer concentration should be 10^{17} cm^{-3} for a 0.5 μm device with a n^{+}-type polysilicon gate.

- The maximum thickness of the undoped buffer depends on the channel length. For channel length of 0.5 μm the maximum affordable thickness of the undoped buffer is 100 nm. For a 0.1 μm MOSFET the buffer thickness has to be reduced to 10 nm.

- In order to adjust the threshold voltage for the digital CMOS applications, p-type delta doping is required for n^{+}-polysilicon gate p-MOSFET. As the delta doping makes the threshold voltage roll off more serious, the delta doping dose used in these devices should be reduced as little as possible. The use of p^{+}-polysilicon gate however, may shift the threshold voltage too much or even result in open channel transistors in the case of undoped buffer structures.

An extensive study of the delta doped SiGe p-channel MOSFET proposed for CMOS applications have been presented above, the main points are as follows.

- It is easy to obtain a threshold voltage of around -0.5 V, with a satisfactory subthreshold slope and threshold voltage roll off for a channel length of ≥ 0.2 μm, by adjusting the substrate concentration and the delta doping.

- The thickness of the gate oxide has a strong influence on the control of short channel effects. The smaller the thickness of the gate oxide, the better the properties of the subthreshold slope and threshold voltage roll off.

- It would be difficult to scale the SiGe p-channel devices with delta doping layers below 0.2 μm, and to retain an acceptable threshold voltage, based on the growth facilities available in the consortium.

CHAPTER

6

Processing and Device Simulations Based Optimisation of CMOS Design

Silicon integrated circuit technology has evolved to fabricate more than 10^8 components on a single chip. Trial-and-error methodology to optimise such a complex process is no longer desirable because of the enormous cost and turn around time. From this point of view, computer simulation is a cost effective alternative, not only supplying a right answer for increasingly tight processing windows, but also serving as a tool to develop future technologies [211-213]. Coupling with a device analysis program, a process simulator is a powerful design tool because the process sensitivity to device parameters can be easily extracted by simple changes made to processing conditions in computer inputs.

Interest in process simulation started much later compared with device simulation. In the 60's and 70's, most process modelling had been done by analytical methods. As the process became sophisticated and the devices were scaled down, the secondary effects such as the doping dependence of diffusivity, oxidation enhanced diffusion, severely affected the accuracy of the simple analytical models. SUPREM (Stanford University PRocess Engineering Models) was introduced in 1977 and was the first program capable of simulating most IC fabrication steps. After that, the enhanced versions SUPREM II and III were available in 1978 and 1983 respectively. All of them were 1-D numerical process simulators.

As the device shrinks further, the 2-D effects are increasingly important in the process modelling. Lee from Stanford University developed 2-D process simulator, BIRD, which employed Green's function to solve the diffusion equation. The Green's function approach requires constant diffusivity and is only valid in the low concentration case. To overcome this limitation, Chin and Kump also from Stanford University

developed a numerical 2-D process simulator, SUPRA using the Green's function method for low impurity concentration as in BIRD and finite difference method for high impurity concentration.

TSUPREM-4 [193] is a computer program for simulating the processing steps used in the manufacture of silicon integrated circuits and discrete devices. TSUPREM-4 simulates the incorporation and redistribution of impurities in a two-dimensional device cross section perpendicular to the surface of the silicon wafer. The output information provided by the program includes:

- Boundaries of the various layers of materials in the structure;
- Distribution of impurities within each layer;
- Stresses produced by oxidation, thermal cycling, or film deposition.

The breed of Si/SiGe CMOS optimised in this work is shown in figure 6.1. This particular structure is also known as hybrid SiGe CMOS since it comprises surface channel n-MOSFETs and only p-channel devices utilise strained quantum well as transport channels. Integrating SiGe within Si results in high speed and packing density for CMOS circuits. However, it also leads to some unclear parameters of processing simulations because SiGe is a new alloy for semiconductor industry. Therefore processing simulation only can be used to guide device simulation and optimisation.

In this chapter, the two-dimensional process simulator TSUPREM-4 and the two-dimensional device simulator MEDICI are used to optimise and design Si/SiGe CMOS. The necessary process parameters are provided by the partners at Southampton and Warwick Universities. The output of TSUPREM-4 is transferred automatically to the MEDICI device simulator. This makes the simulation results more realistic.

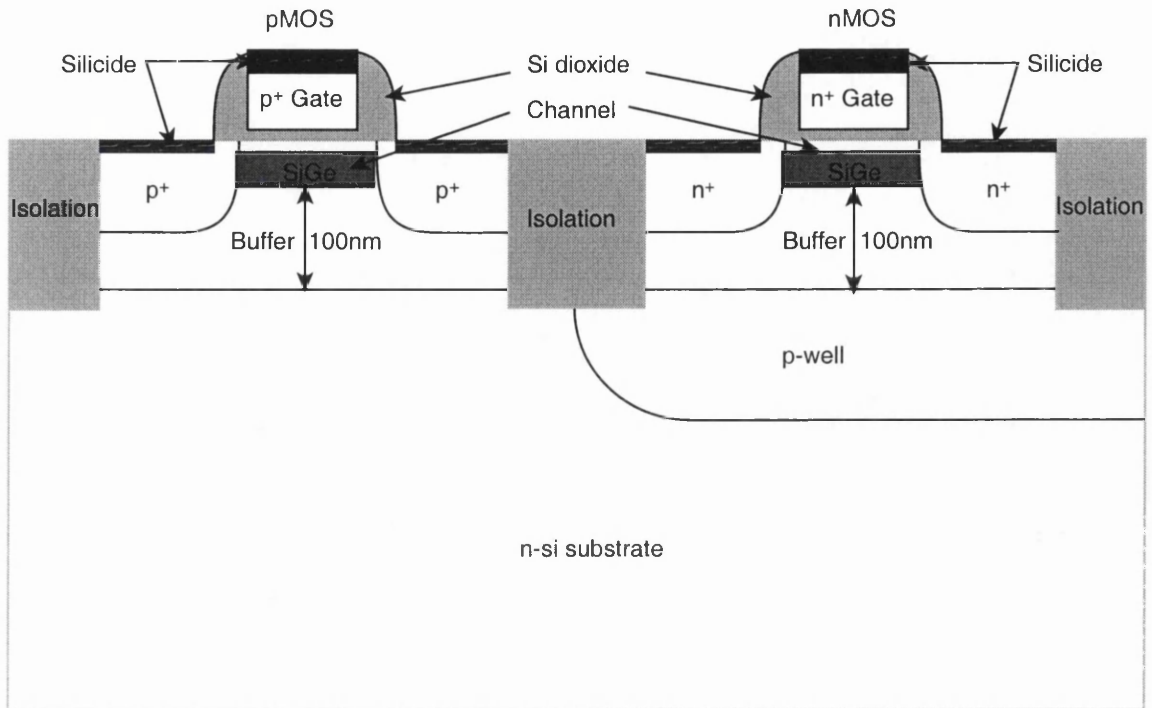


Figure 6.1 Si/SiGe CMOS structure.

6.1 Simulation Based Optimisation of SiGe p-Channel MOSFET Design

Simulations were performed on a series of 0.5 μm gate length SiGe p-channel MOSFETs with the device structure shown in figure 6.1. Within the process requirements set by the partners in Southampton, device threshold voltage should be optimised to –0.5 V while avoiding, if possible, short channel effects. The minimum gate length possible for realistic devices employing these process parameters was also investigated.

The devices consisted of a lightly doped (10^{15} cm^{-3}) n-type substrate with implanted n-well. This was formed through dual implants of phosphorus at energies of 160 kV, 70 kV and doses of 10^{13}, 4×10^{12} cm^{-2} respectively. A 100 nm buffer was then epitaxially grown – the doping density in this buffer is the critical control variable which

allows us to vary the device threshold voltage, V_{TH}. A further 15 nm of nominally undoped SiGe channel and Si surface spacer followed before a 6 nm gate oxide (grown by dry thermal oxidation at 800 °C) and p^+-polysilicon gate. Source and drain implants of BF_2 were made at an energy of 35 kV and dose of 5×10^{15} cm^{-2}. This produced a modelled junction depth of approximately 210 nm and a source-drain subdiffusion of approximately 105±5 nm (dependant on the precise doping of the buffer).

Simulations were carried out using the two-dimensional process simulator TSUPREM-4 and the two-dimensional device simulator MEDICI. The processing parameters provided by the partners at Southampton and Warwick universities were used, and the latest implant damage enhanced diffusion models were included. The output of TSUPREM-4 was transported automatically to the MEDICI device simulator. Buffer doping was varied between 2.5×10^{17} cm^{-3} and 10^{18} cm^{-3} and device threshold voltage obtained. The subthreshold voltage slope, S was also calculated. For proper device operation a slope of around 80~120 mV/decade for drain voltages of both V_D = -0.01 V and V_D = -2 V is considered necessary. Threshold voltage roll off, V_{TH} *roll off* of no greater than 200 mV is also considered appropriate. The definition introduced in chapter 5 is used.

6.1.1 Optimisation of 0.5 μm devices

Figures 6.2 and 6.3 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off on the buffer concentration. When the gate length is 0.5 μm, it is obvious that the buffer concentration should be 7.5×10^{17} cm^{-3}, which promises a device threshold voltage of around -0.5 V. In addition, both the subthreshold slope and threshold voltage roll off are acceptable.

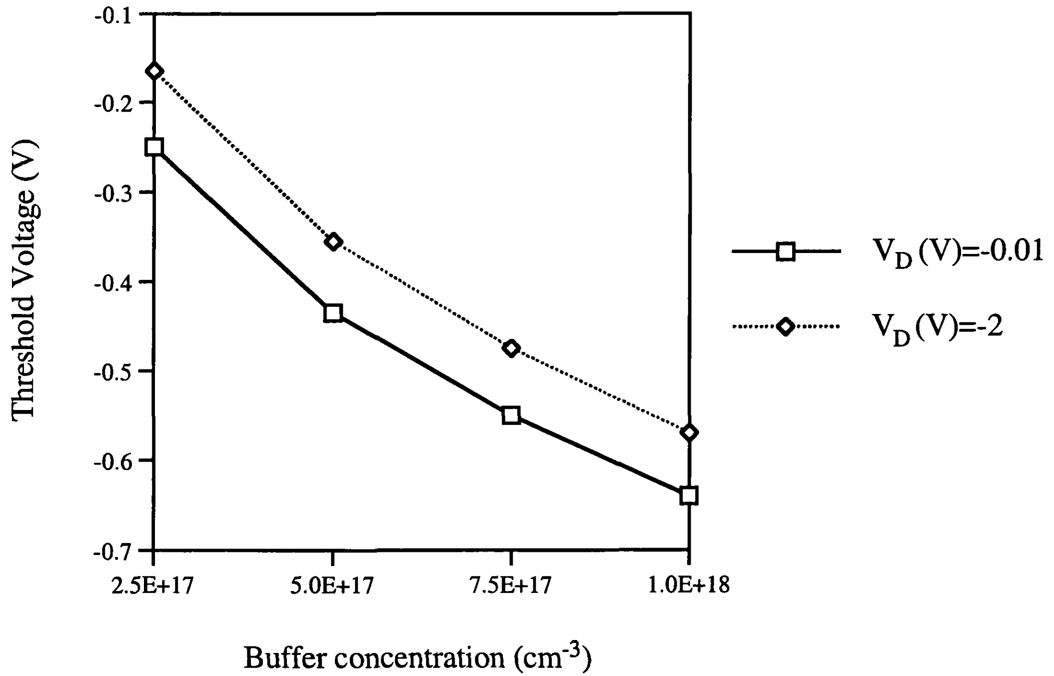


Figure 6.2 Threshold voltage versus buffer concentration.

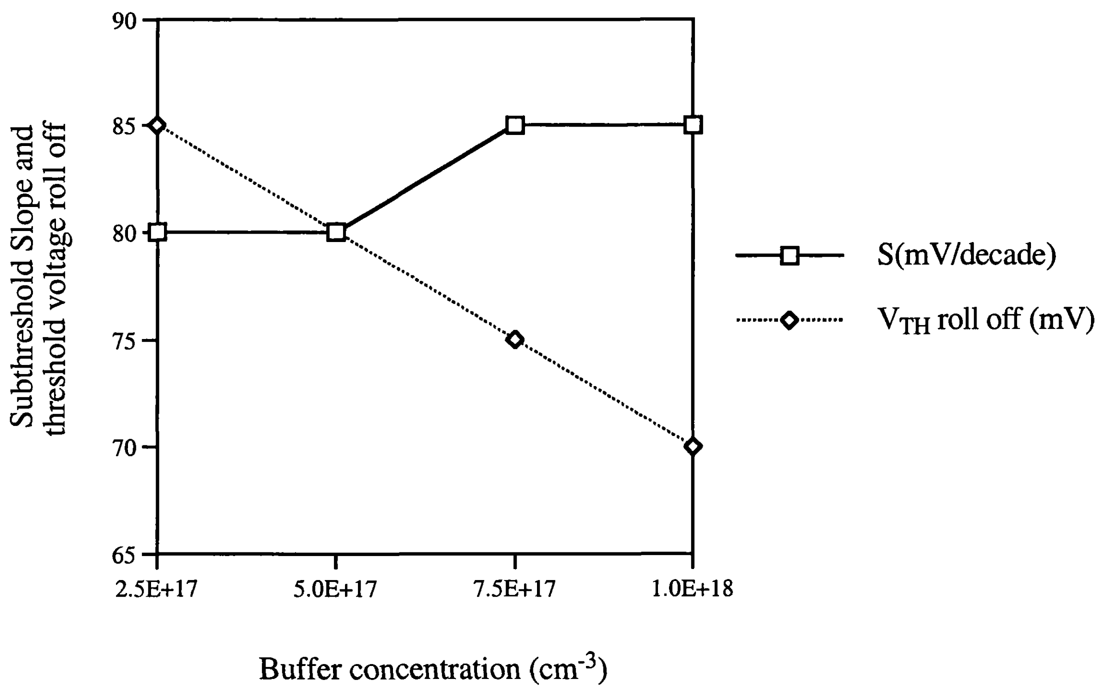


Figure 6.3 Threshold voltage roll off and subthreshold slope versus buffer concentration.

6.1.2 Optimisation of reduced gate length devices

Figures 6.4 to 6.7 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off as a function of gate length for buffer concentrations of 7.5×10^{17} cm^{-3} and 2×10^{18} cm^{-3}.

Two-dimensional short channel effects increase as the device gate length decreases, with a characteristic "knee" in the graphs showing the gate length at which control of two-dimensional effects is lost. For a buffer concentration of 7.5×10^{17} cm^{-3} this occurs at a gate length of 0.35 μm. A buffer concentration of 2×10^{18} cm^{-3} allows a gate length of 0.3 μm to be achieved. However, buffer concentrations greater than 7.5×10^{17} cm^{-3} also produce a threshold voltage shift further from the optimal -0.5 V. The magnitude of V_{TH} for an 0.3 μm device with buffer concentration 2×10^{18} cm^{-3} is between -0.8 V and -1.0 V which is too high for CMOS applications. Although p-type delta doping below the channel can be used to tune the threshold voltage, delta doping will increase the short channel effects (see Section 5.2.1.A). The solution is a trade-off, and if the gate length decreases further, even this method would fail.

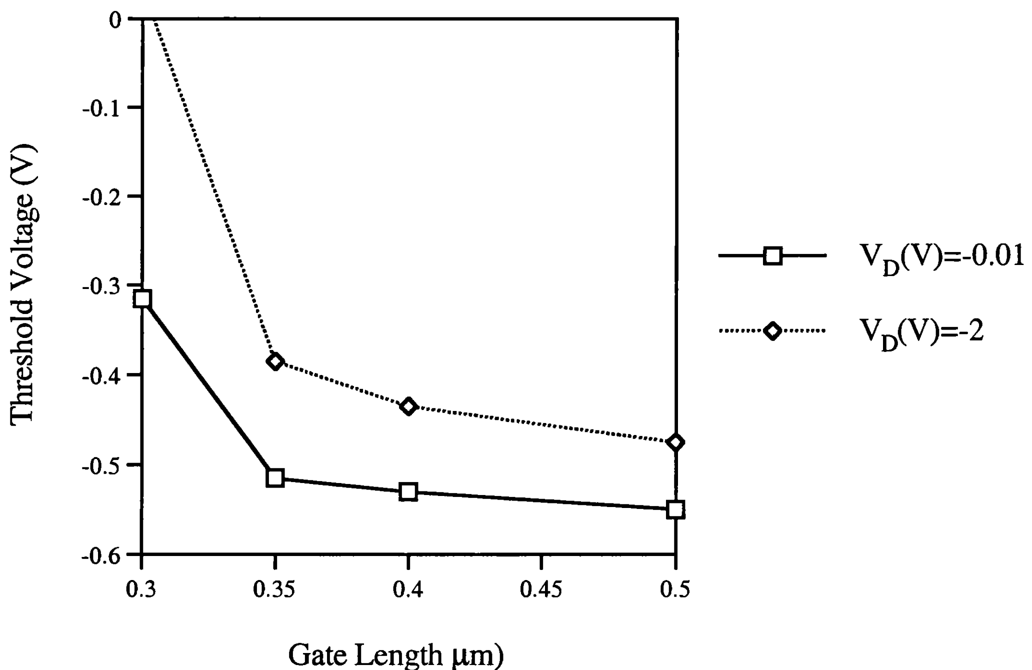


Figure 6.4 Threshold voltage versus gate length. Buffer concentration is 7.5×10^{17} cm^{-3}.

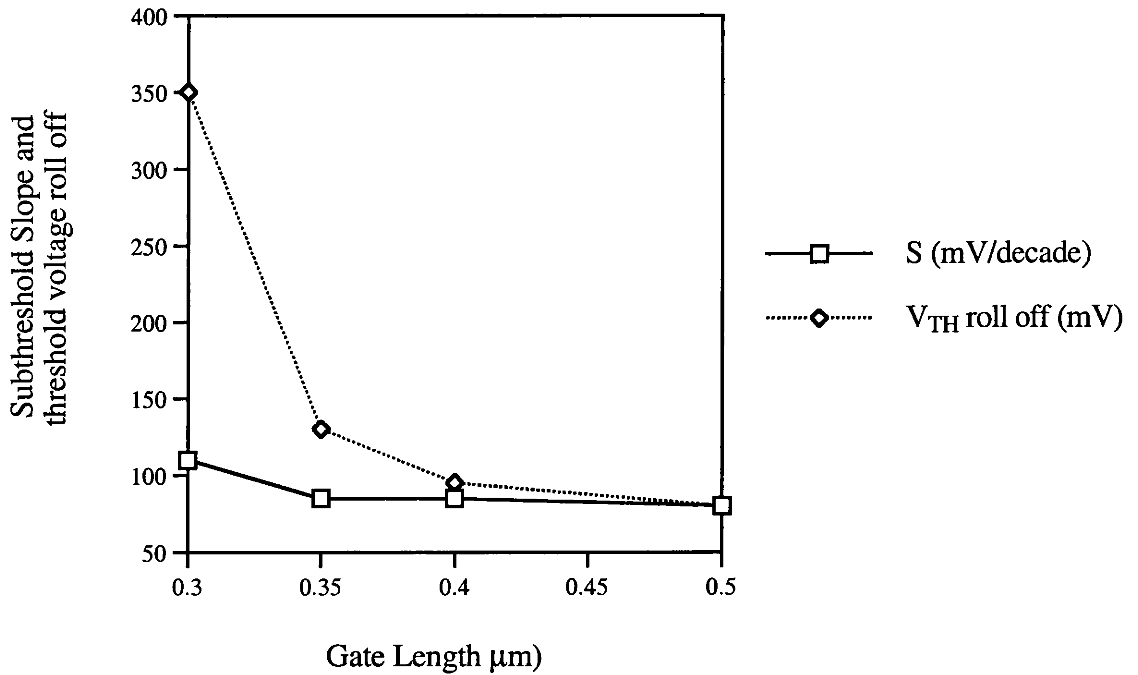


Figure 6.5 Threshold voltage roll off and subthreshold slope versus gate length. Buffer concentration is 7.5×10^{17} cm^{-3}.

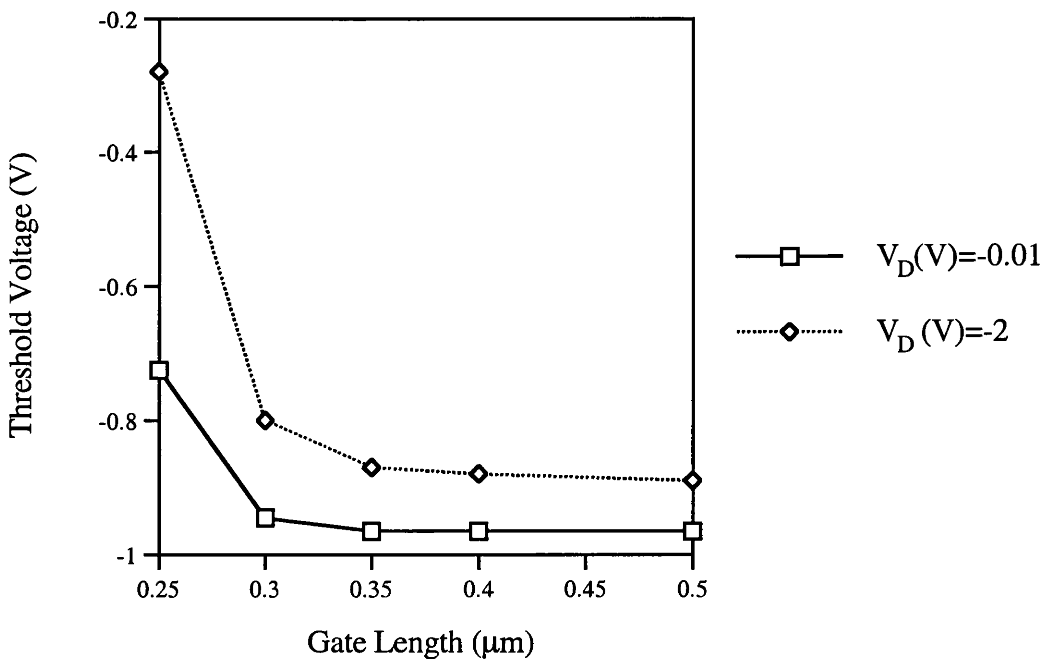


Figure 6.6 Threshold voltage versus gate length. Buffer concentration is 2×10^{18} cm^{-3}.

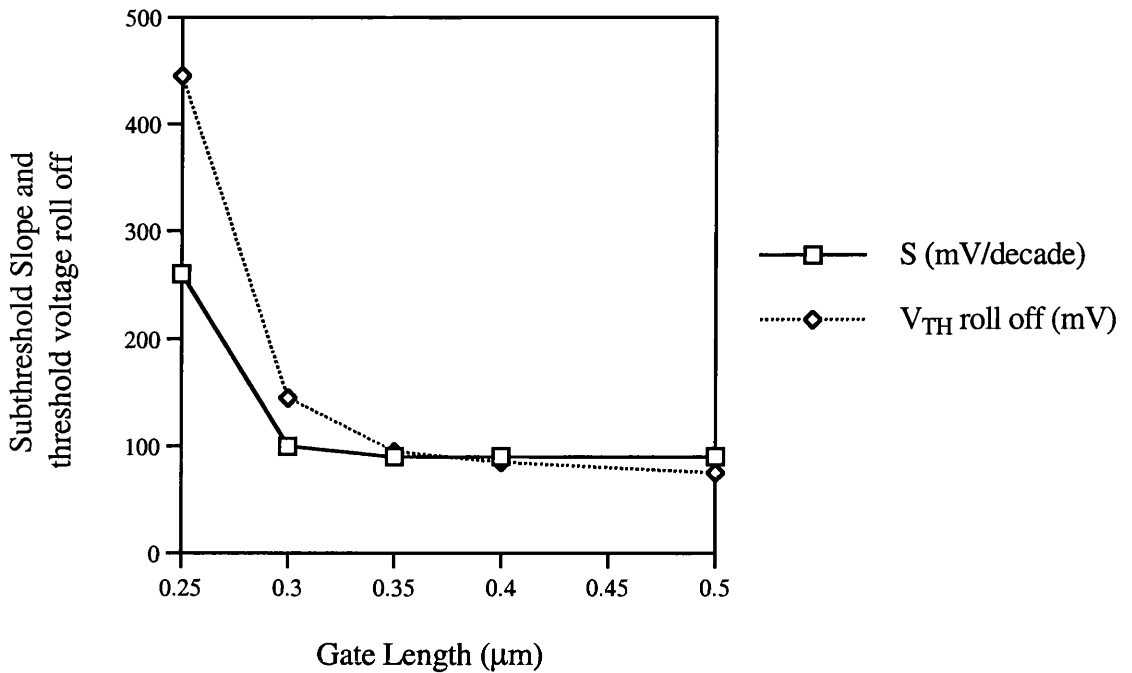


Figure 6.7 Threshold voltage roll off and subthreshold slope versus gate length. Buffer concentration is 2×10^{18} cm^{-3}.

To satisfy the requirement of threshold voltage at -0.5 V, it is necessary to use a buffer concentration of 7.5×10^{17} cm^{-3}, with the smallest gate length possible being 0.35 μm to avoid short channel effects.

6.2 Simulation Based Optimisation of n-Channel MOSFET Design

Simulations were performed on a series of 0.5 μm gate length n-channel MOSFETs to be fabricated as part of a Si/SiGe CMOS process. The device structure is shown in figure 6.1. The devices should have V_{TH} = 0.5 V while avoiding short channel effects within the constraints set by the layer structure (required for correct SiGe p-channel device operation) and processing limitations. The minimum practical gate length of realistic devices under these process limitations have also been investigated.

The devices consisted of a lightly doped (10^{15} cm^{-3}) n-type substrate with implanted p-well. This was formed through dual implants of boron at energies of 60 keV, 25 keV and doses of 10^{13}, 5×10^{12} cm^{-2} respectively. A 100 nm n-type buffer was then epitaxially grown. The doping density of this buffer was 7.5×10^{17} cm^{-3}, and was a requirement for correct p-channel device threshold voltage and to suppress the short channel effects. For the n-channel device a boron implant counter doping step was needed. Energy and dose of this implant will affect device threshold voltage, although ideally a low energy implant should also be employed for detailed threshold voltage control. Note that implant energies at Southampton university were limited to > 25 keV.

A further 15 nm of nominally undoped SiGe channel and Si surface spacer followed before a 6 nm gate oxide and n^+-polysilicon gate. Source and drain implants of arsenic were carried out at an energy of 50 keV and dose of 5×10^{15} cm^{-2}. These gave a modelled junction depth of approximately 160 nm and a source-drain sideways diffusion of approximately 80 nm.

Simulations were carried out using TSUPREM-4 and MEDICI. The latest implant damage enhanced diffusion models were included. Initial simulations showed a minimum boron implant of 25 keV was appropriate for counterdoping of the 100 nm n-type buffer, but its projected range overshoots the n-channel region. A 25 keV implant alone will give imprecise threshold control, and should be augmented by a low energy implant to set dopant concentrations at the surface.

In the absence of an available low energy implant, crude threshold voltage control was attempted. The implant energy was fixed at 25 keV and the dose varied between 1.0×10^{13} cm^{-2} and 1.6×10^{13} cm^{-2}, and then device threshold voltage calculated. The profiles of boron, phosphorus and the net doping were plotted. The subthreshold voltage slope S, was also computed to monitor short channel effects. For proper device operation a slope of between 80 to 120 mV/decade for drain voltages of both V_D = 0.01 V and V_D=2 V is required. Threshold voltage roll off, V_{TH} *roll off* of no greater than 200 mV is also considered appropriate. The definition introduced in Section 5.1 is used.

6.2.1 Optimisation of boron implant

Figures 6.8-6.10 illustrate the profiles of boron, phosphorus and the net-doping respectively. The zero of the graph represents the interface of the substrate and 100 nm buffer. The boron concentration does compensate the phosphorus dose within the 100 nm buffer and forms a punchthrough stopper below it. It does not compensate for phosphorus which has diffused from the buffer towards the SiO_2 interface; the device remains n-type there.

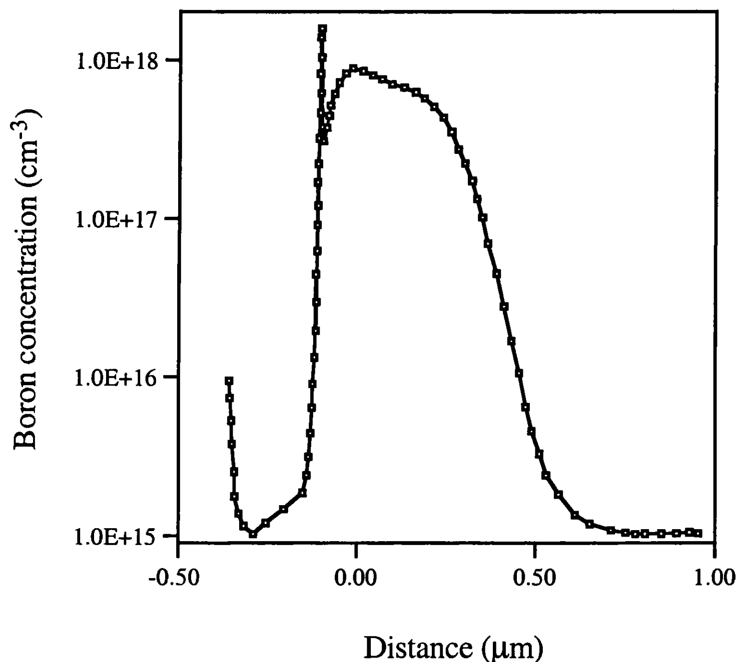


Figure 6.8 The profile of boron in the n-channel MOSFET. The zero of the graph represents the interface of the substrate and the buffer.

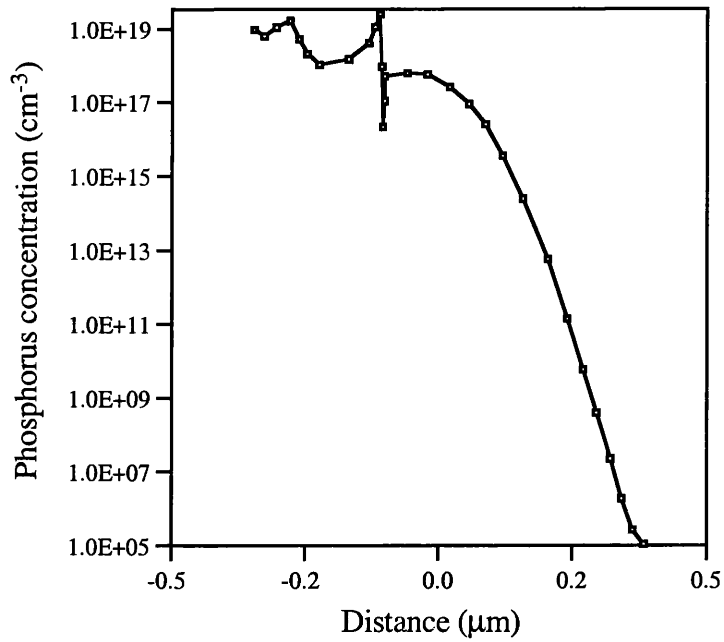


Figure 6.9 The profile of phosphorus in the n-channel MOSFET. The zero of the graph represents the interface of the substrate and the buffer.

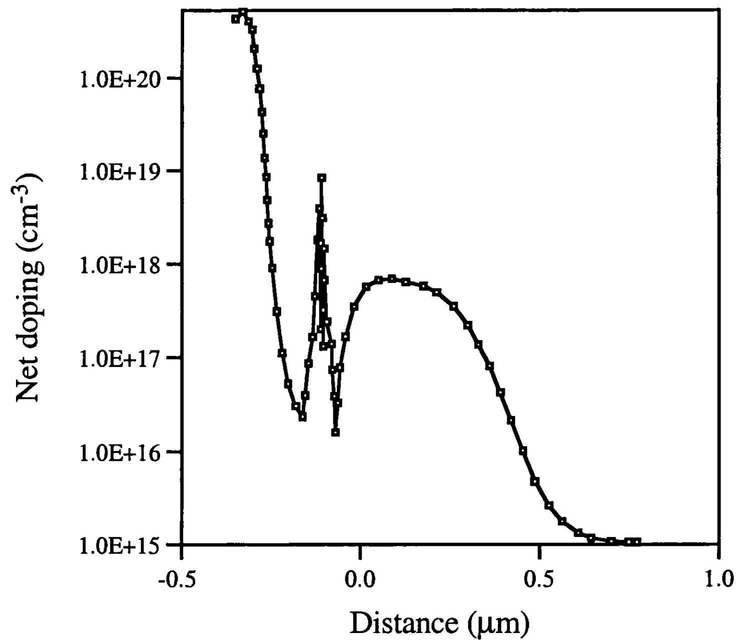


Figure 6.10 The profile of the net doping in the n-channel MOSFET. The zero of the graph represents the interface of the substrate and the buffer.

6.2.2 Optimisation of 0.5 μm devices

Figures 6.11 and 6.12 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off on the boron implant dose. When the gate length is 0.5 μm, a boron implant dose of 1.2×10^{13} cm^{-2} gives a device threshold voltage of around 0.5 V. In addition, both the subthreshold slope and threshold voltage roll off are acceptable.

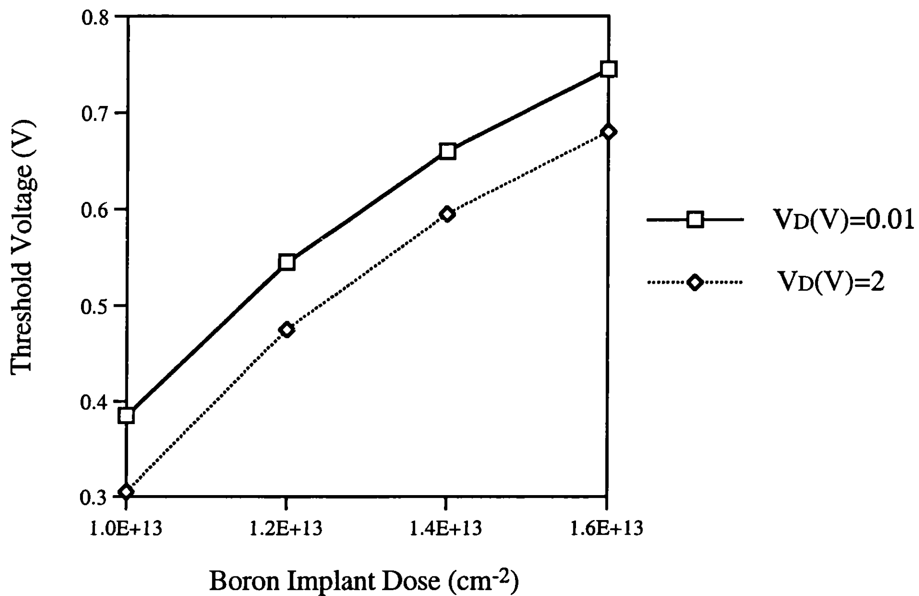


Figure 6.11 Threshold voltage versus boron implant dose.

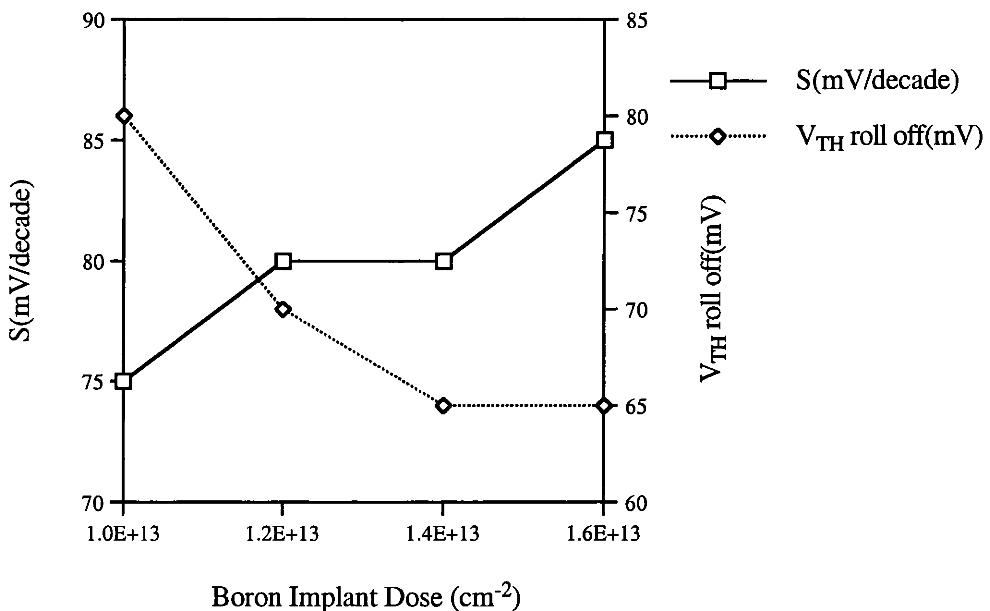


Figure 6.12 Threshold voltage roll off and subthreshold slope versus boron implant dose.

6.2.3 Optimisation of reduced gate length devices

Figures 6.13 and 6.14 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off as a function of gate length for boron implant dose of 1.2×10^{13} cm^{-2}.

Two-dimensional short channel effects increase as the device gate length decreases, with a characteristic "knee" in the graphs showing the gate length at which control of two-dimensional effects is lost. For a boron implant dose of 1.2×10^{13} cm^{-2} this occurs at a gate length of 0.3 μm. To satisfy the requirement of threshold voltage at 0.5 V and no punchthrough effects, it has been found that it is necessary to use a boron implant dose of 1.2×10^{13} cm^{-2}, with the smallest gate length possible being 0.3 μm to avoid short channel effects. For devices below 0.3 μm gate length, LDD structures will in all probability be required [214, 215]. They will decrease the sideways diffusion and allow threshold voltage roll off to be minimised [216, 217]. LDD structures may also increase the hot carrier resistance of the MOSFET [218-222]. These structures, however, will generally reduce drain current due to an increase in the series resistance of the drain region [223-225]. Further work must be considered on these trade-offs.

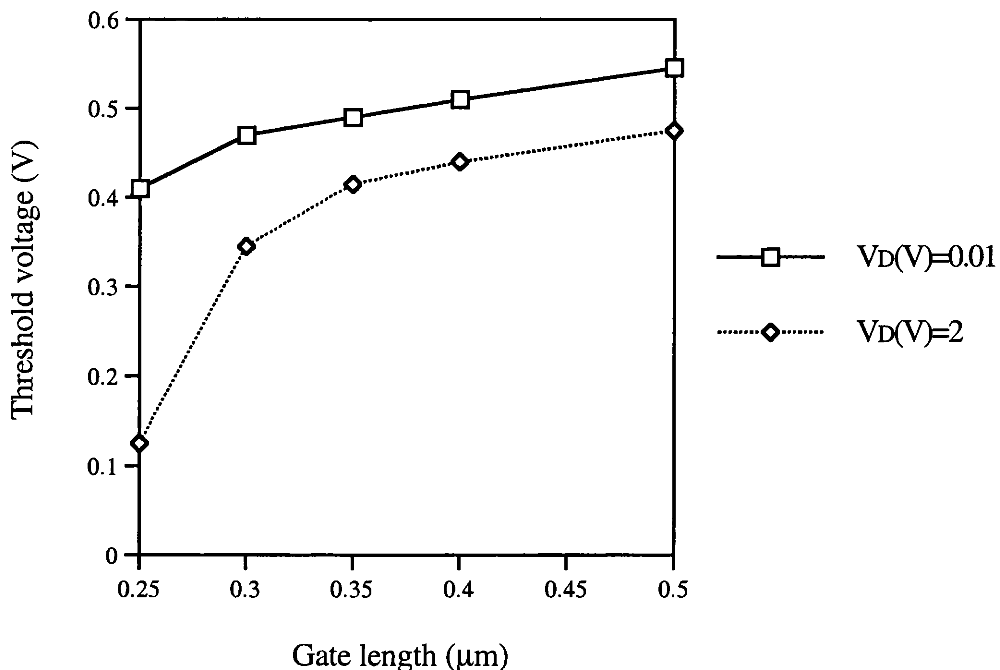


Figure 6.13 Threshold voltage versus gate length.

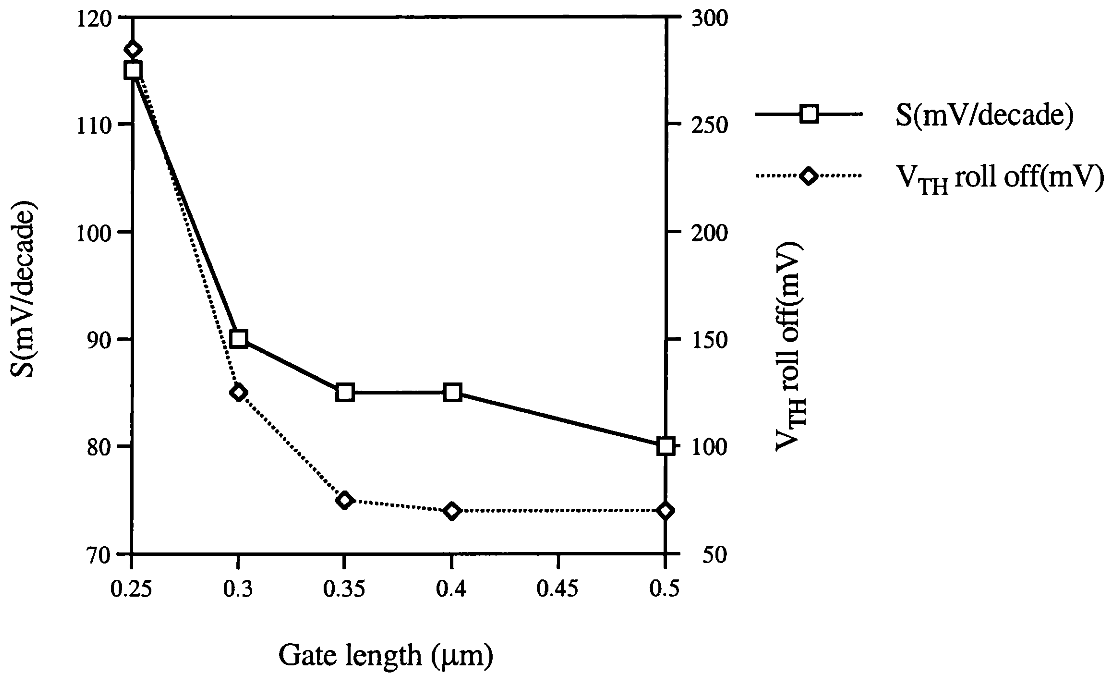


Figure 6.14 Threshold voltage roll off and subthreshold slope versus gate length.

6.3 Summary

From the simulations of hybrid Si/SiGe CMOS above, the main points regarding the optimisation are as follows:

- A doped buffer can be used to adjust threshold voltage and to prevent short channel effects. The suggestion is that a buffer concentration of 7.5×10^{17} cm^{-3} will satisfy the threshold voltage requirement of -0.5 V, for a gate length range of 0.35 μm to 0.5 μm.

- A buffer concentration of 2×10^{18} cm^{-3} can be chosen for a 0.3 μm gate length device if p-type delta doping below the channel is used to tune the threshold voltage from −0.9 V to −0.5 V. However, delta doping will increase the short channel effects. The solution is a trade-off, and if the gate length decreases further, even this method will fail.

- For devices at or below 0.3 μm gate length, LDD structures may be required. They will decrease the lateral sideways diffusion and allow threshold voltage roll off to be minimised. These structures, however, will generally reduce drain current due to an increase in the series resistance of the drain region. Further consideration must be made of these trade-offs.

- One boron implant can be used to adjust threshold voltage and to prevent short channel effects for Si/SiGe n-MOSFET. The suggestion is that a boron implant with energy of 25 keV and dose of 1.2×10^{13} cm^{-2}, will satisfy the threshold voltage requirement of 0.5 V, for a gate length range of 0.3 μm to 0.5 μm.

- However, this method only allows crude V_{TH} control, and for more reproducible results, a separate 25 keV buffer counter doping and lower energy V_{TH} control doping should be employed.

CHAPTER 7

Scaling Potential of Si and SiGe p-MOSFETs

For more than 30 years, MOS device technologies have been improving at a dramatic rate [6]. A large part of the success of the MOSFET is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The ability to improve performance consistently while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. However, serious design and technology problems posed by continuously shrinking MOSFETs have been recognised. Short channel effects and hot carrier effects are among a long list, all of which can degrade device performance. New device structures, such as lightly doped drain (LDD) and super-halo doping profiles are needed to reduce these effects. Moreover, when devices are scaled to submicron dimensions, even the commonplace design tools comprising drift diffusion transport models assuming a carrier temperature equal to the lattice temperature becomes questionable.

In this chapter, drift diffusion and hydrodynamic simulations for Si and SiGe p-MOSFETs over a variety of channel lengths from 0.5 to 0.1 μm are presented. A Monte Carlo model has been used to establish confidence limits for the drift diffusion and hydrodynamic models. In addition, the well-tempered Si p-MOSFETs at gate lengths of 25 and 50 nm are investigated, using calibrated drift diffusion and two dimensional Monte Carlo simulations. Hole non-equilibrium transport effects in Si devices are also studied. Finally well-tempered SiGe p-MOSFETs are studied and compared against their Si counterparts.

7.1. Description of Models

7.1.1 Monte Carlo method

The Monte Carlo method is attractive for modelling carrier transport in semiconductors as it allows for the exact bandstructure of the material and the scattering rates to be implemented in a self-consistent framework. However, it has the disadvantage that it requires substantial computational resources making it often impractical for device design, where it is necessary to perform many different simulations within a short period of time. One of the main applications for Monte Carlo simulation within device simulation is to calibrate and provide confidence in the drift diffusion and hydrodynamic simulators. Therefore the Monte Carlo simulator used during the course of deep submicron simulation is briefly described.

The bandstructure model of the Monte Carlo simulator is based on the solution of the $\boldsymbol{k}\cdot\boldsymbol{p}$ Hamiltonian, including spin orbit coupling and strain. The resulting bandstructure is used to calculate the density of states for scattering, allowing the non-parabolicity, anisotropy and strain to be incorporated in a natural way into the Monte Carlo transport simulator. This rigorous treatment of the band structure is far more accurate than simple alternatives employing analytical models.

In this chapter, the Monte Carlo simulator has been used to calculate the average low-field drift mobility μ_D and the macroscopic ensemble energy relaxation time τ_E. The latter can be calculated using [226]:

$$\tau_E = \left| \frac{E - E_0}{eFv} \right| \tag{7.1}$$

where v represents the saturation velocity, F is the electric field strength, and e is the elementary electronic charge. E and E_0 represent the final and initial average energy respectively of particles.

The Monte Carlo simulator may also be used to calculate the carrier temperature tensor T_H [170]:

$$k_B T_{Hij} = \left\langle \hbar \left(k_i - \bar{k}_i\right)\left(v_j - \overline{v_j}\right)\right\rangle \tag{7.2}$$

where k_B is the Boltzmann constant, $\hbar$ is the Planck constant, i and j denote x, y or z respectively. It is an analysis of which is used here to examine the validity of the hydrodynamic model for the simulation of holes in p-channel SiGe MOSFETs. Further details of the Monte Carlo simulator are not relevant to the objectives in this work, this information was provided in detail elsewhere [128, 226].

7.1.2 Hydrodynamic method

The hydrodynamic model represents a second order approximation to the Boltzmann Transport equation, after the drift diffusion approach, while being less computationally expensive than the Monte Carlo method. It can also account for non-equilibrium effects. Equations for the conservation of carriers, momentum and energy (the first three moments of the Boltzmann transport equation) are solved self consistently with Poisson's equation. In the hydrodynamic module of the commercial simulator MEDICI [158] used here, the convective term in the momentum conservation equation is neglected. The carrier distribution is assumed to follow a displaced Maxwell-Boltzmann distribution, with an elevated scalar carrier temperature $T_H > T_L$, where T_H and T_L correspond to carrier and lattice temperature respectively.

7.1.3 Drift Diffusion method

The drift diffusion model represents a first-order approximation to the Boltzmann transport equation where only the zeroth and first moments are considered. In this approximation Poisson's equation is solved self consistently with the carrier continuity equation. Additionally a Maxwell-Boltzmann distribution, with a carrier temperature

equal to the lattice temperature, is assumed for the carrier distribution. This approximation results in the current (momentum conservation) being described in a drift diffusion approximation in which current in a semiconductor is due to carrier drift (e. g. field) and diffusion (e. g. density gradients). Therefore this approach is only valid in regions where the deviation of the carriers from thermal equilibrium is small, i.e. regions of low electric fields as in large-scale devices [128].

7.2 Simulations and Investigation of Si/SiGe p-MOSFETs Down to 0.1 μm

The interest in SiGe for MOSFET applications has grown continuously, following recent experimental and theoretical demonstrations that the hole mobility in strained SiGe can be considerably higher than in Si. Strained SiGe p-MOSFETs are particularly attractive for CMOS applications as the hole mobility starts to be comparable with that of the electron mobility. This may reduce the asymmetry in the channel widths of the n and p-channel MOSFETs required for efficient CMOS operation, leading to an increase in the packing density. However, optimising the design of SiGe p-MOSFETs will require efficient models for device simulations, with known confidence limits. In this section, the simulation results for submicron Si/SiGe p-MOSFETs using drift diffusion and hydrodynamic commercial simulators are presented, with transport parameters extracted from Monte Carlo transport simulations. The Monte Carlo model is used to establish confidence limits for the drift diffusion and hydrodynamic models. The role of velocity overshoot for the enhancement of the performance potential in the SiGe devices is also investigated.

Reliable modelling of Si/SiGe MOSFETs is required in order to optimise their design and maximise performance. Traditionally drift diffusion models have been used in MOSFET design and modelling due to the speed of associated commercial simulators [158]. However, when devices are scaled to submicron dimensions, non-equilibrium carrier dynamics become increasingly important. Thus the drift diffusion model, assuming a carrier temperature equal to the lattice temperature, is no longer appropriate

and a hydrodynamic approach is required in the computer aided design process to take into account the non-equilibrium carrier dynamics and overshoot effects.

However, the application of drift diffusion and hydrodynamic models is limited without reliable transport parameters such as mobility μ and energy relaxation times τ_E, and reliable knowledge about the limitations of their validity. The range over which the models are valid can be determined by comparing with experimental results and more sophisticated, higher level models. Drift diffusion can be compared with a hydrodynamic simulation to determine the range over which it can be applied, while hydrodynamic models must be compared to either experimental results or Monte Carlo simulation. One of the important assumptions in the standard hydrodynamic model from the point of view of modelling p-MOSFETs is to assume that the carrier temperature T_H is a scalar [150]. It is known that formally T_H is a tensor, therefore the assumption of a scalar neglects the anisotropic nature of the valence bandstructure. Therefore by examining the tensorial properties of the hole carrier temperature, obtained from Monte Carlo simulation, as a function of the applied electric field, a unique insight into the validity of the hydrodynamic approach for modelling submicron p-MOSFETs is obtained.

The Monte Carlo results are presented here for the energy relaxation time and the diagonal elements of the carrier temperature tensor as a function of the electric field. Hydrodynamic and drift diffusion simulation results for holes in Si and SiGe p-MOSFETs are presented for a range of gate lengths varying from 0.5 μm to 0.1 μm.

Figure 7.1 shows the energy relaxation times for Si and compressively strained $Si_{0.8}Ge_{0.2}$ as a function of electric field at 300 K, with nominal doping (10^{15} cm^{-3}). Figures 7.2 (a) and (b) show the diagonal elements of the hole carrier temperature tensor T_H. The electric field is applied in the <100> direction, as would be the case for the field between the source and the drain in a MOSFET.

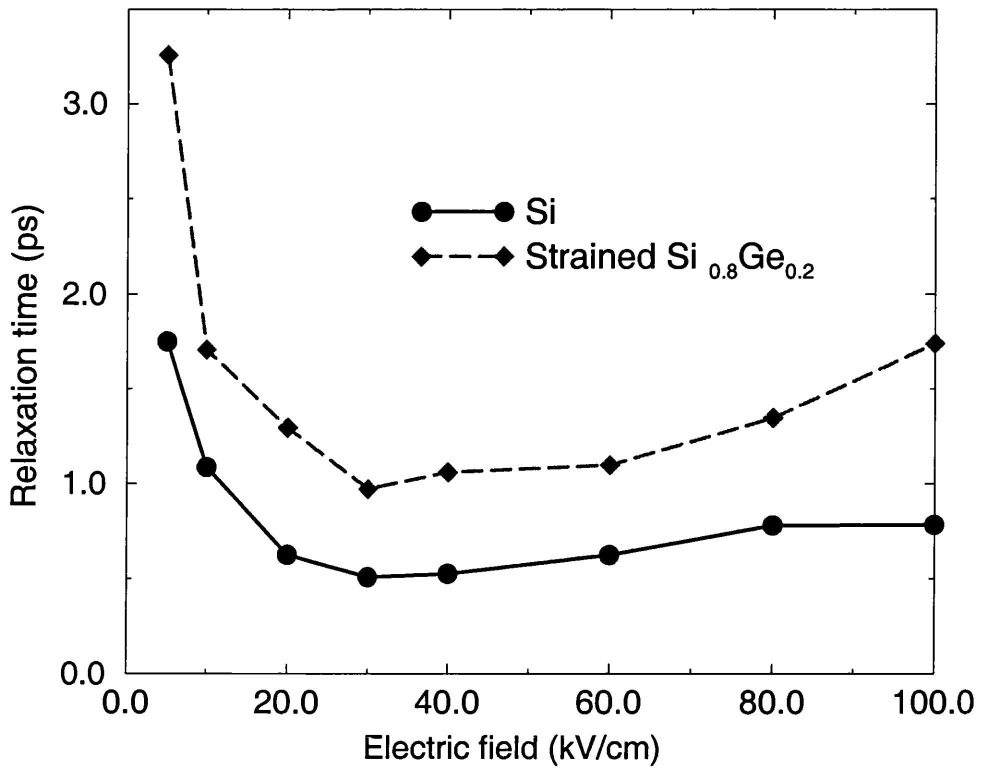


Figure 7.1 Energy relaxation times in Si and strained $Si_{0.8}Ge_{0.2}$.

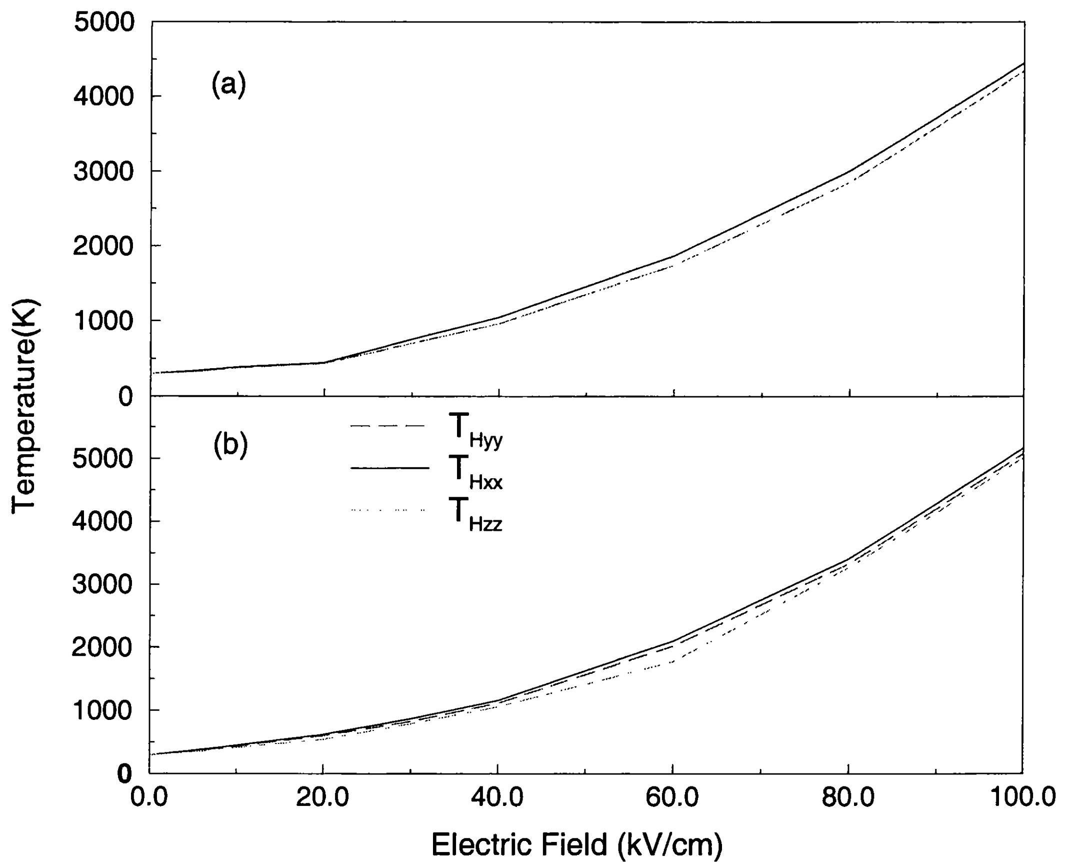


Figure 7.2 Diagonal components of T_H in (a) Si; and (b) strained $Si_{0.8}Ge_{0.2}$, respectively.

From figure 7.1 it is clear that the relaxation times for strained SiGe are higher than in Si. This is partially associated with its smaller density of states. The larger relaxation times indicate the potential for larger velocity overshoot in SiGe p-MOSFETs as compared with standard Si devices. The rise in the relaxation times has been observed before [226], and is due here to inter-valley transfer to the light and spin-split off bands. It is observed in Figures 7.2 (a) and (b) that T_{Hxx} is larger than the other components, as the electric field is applied in this direction. The spread in the temperature components is larger in strained $Si_{0.8}Ge_{0.2}$ reflecting the increased anisotropy of the valence band in this material.

Figures 7.3 and 7.4 show the saturated drain current versus effective channel length for a Si and SiGe p-MOSFET respectively. Here a constant energy relaxation time of 0.63 ps for Si and 1.29 ps for SiGe have been used, taken from Monte Carlo simulations.

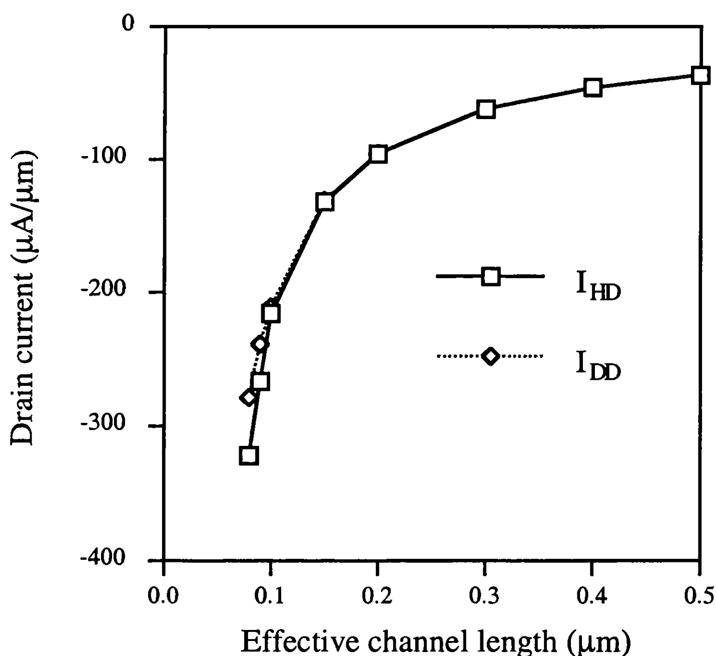


Figure 7.3 Drain current versus effective channel length for Si p-MOSFET ($V_{GS} = V_{DS} = -2V$).

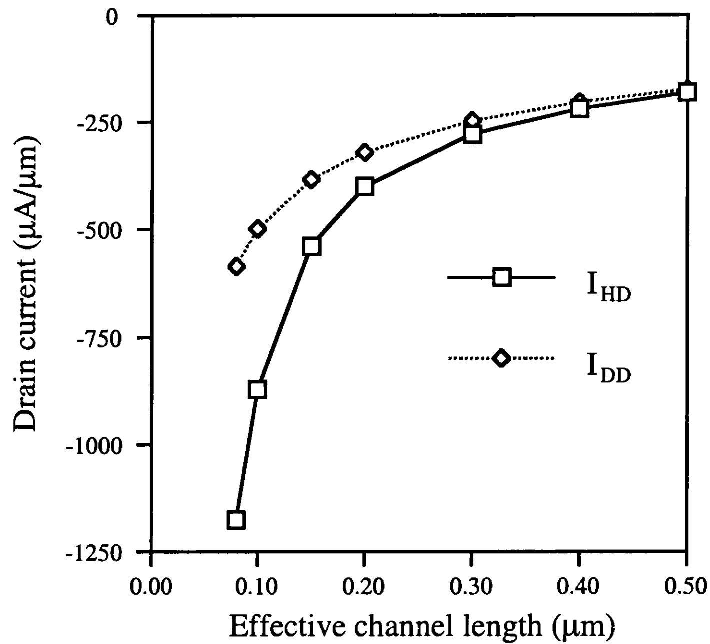


Figure 7.4 Drain current versus effective channel length for SiGe p-MOSFET ($V_{GS} = V_{DS} = -2V$).

It is clear that it is necessary to consider the hydrodynamic model for SiGe p-MOSFETs with channel lengths of 0.3 μm and smaller. However, for Si p-MOSFETs both the drift diffusion and hydrodynamic are likely to provide reasonable models down to an effective channel length of around 0.15 μm (the current generation of devices). This indicates that the velocity overshoot plays a significant role in scaled SiGe devices, as is to be expected from the large values of the energy relaxation time observed in SiGe. However, the question remains of how much confidence is there in the hydrodynamic model for short channel lengths in SiGe p-MOSFETs. This may be addressed in part by examining the electric field in the SiGe channel for two different gate lengths (0.5 μm and 0.1 μm), as shown in figures 7.5 and 7.6 respectively.

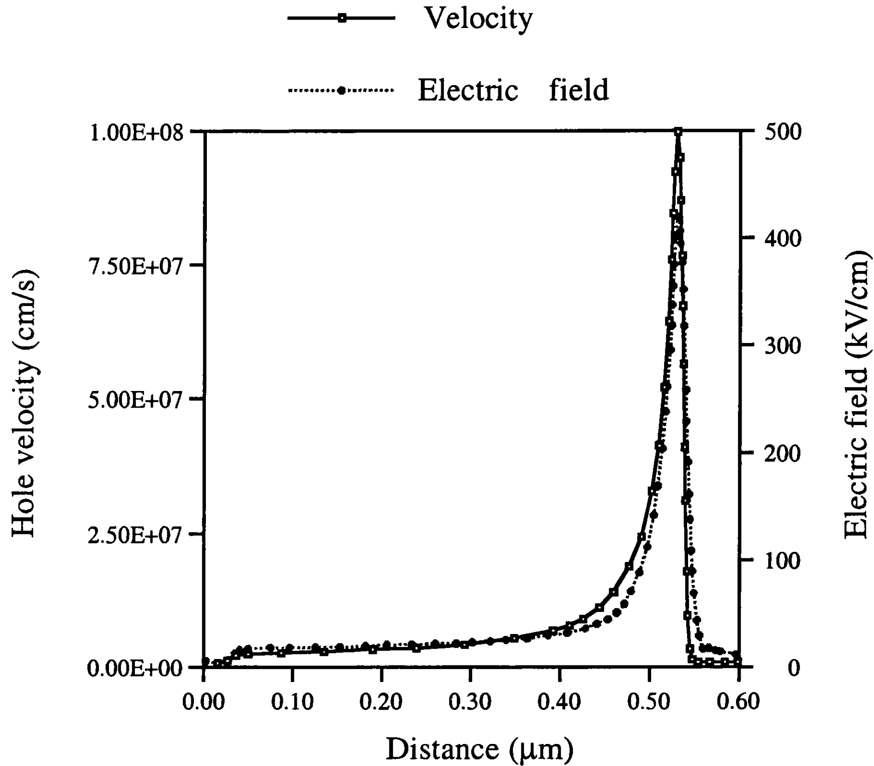


Figure 7.5 Electric field and hole velocity profiles along the channel in a 0.5 μm SiGe p-MOSFET.

The carrier dynamics at the source end of the MOSFET dominate the device operation. Therefore non-equilibrium transport effects at the source will have a strong influence on the operation of the device. It has been observed for the 0.1 μm device that the electric field at the source rises quickly to 100 kV/cm and above. For fields of this magnitude the tensorial properties of the carrier temperature becomes significant (as can be seen from figure 7.2 (b)) due to the anisotropic nature of the bandstructure. Therefore the hydrodynamic model used is unlikely to be able to represent the expected device anisotropy and more sophisticated models such as Monte Carlo simulations must be considered.

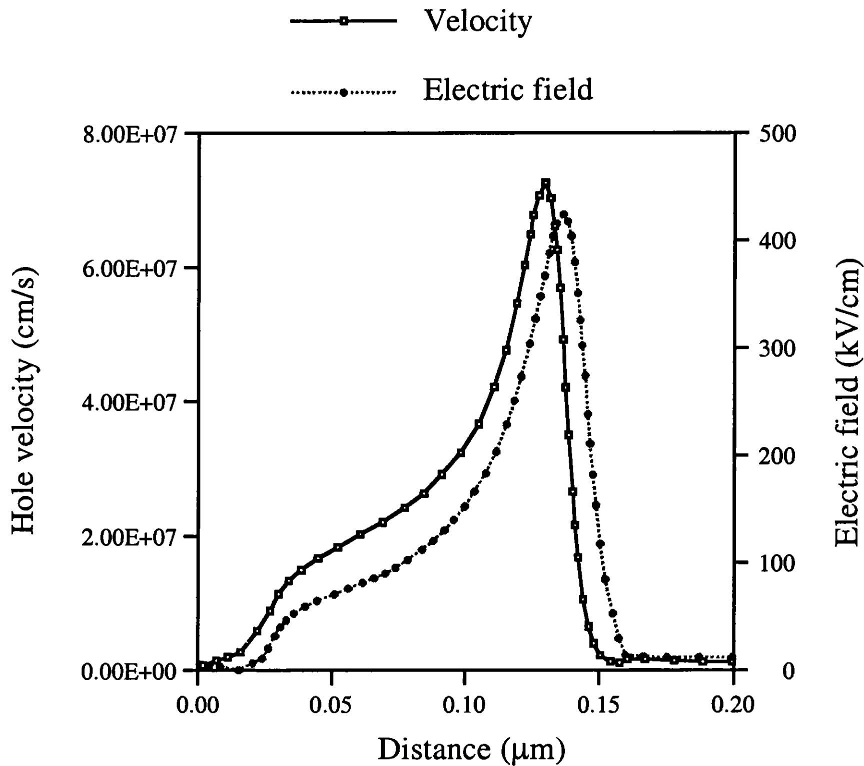


Figure 7.6 Electric field and hole velocity profiles along the channel in a 0.1 μm SiGe p-MOSFET.

7.3 Simulations and Investigation of Si p-MOSFETs Below 0.1 μm

Si MOSFET technology represents by far the largest market share of the microelectronics industry. The current generation of MOSFETs have feature sizes of around 0.15 μm. Next generation of MOSFETs will have decanano dimensions, such as gate lengths of 50 nm by 2009 and 25 nm are predicted for 2014 [4]. To date, most simulation studies have concentrated on n-MOSFETs because of their intrinsically better performance as compared to p-channel devices and the simpler bandstructure for electrons. However, there is a growing interest in studying p-MOSFETs in order to close the performance gap between n- and p-channel devices, as defined in terms of transconductance, and the possibility of including a strained SiGe channel.

As the gate lengths of Si p-MOSFETs are shrunk to deep submicron dimensions the intrinsic transconductance, g_m, continues to increase while in comparison the transconductance in n-MOSFETs tends to saturate with corresponding gate length reduction. It is speculated that the continuous improvement in p-MOSFET performance below 0.1 μm is related to the late onset of velocity overshoot effects, present at longer channel lengths in the n-channel devices.

From the investigations in Chapters 5 and 6, it is very clear that as MOSFETs are scaled to deep submicron dimensions short channel effects, which become more serious, can not avoided by tuning the parameters of the devices. New device structures are needed to prevent them. Several device structures have been used, such as lightly doped drain (LDD), shallow source/drain extension [227-231] and halo well profile.

The addition of well implants to create a non-uniform well profile to improve short channel effects has been reported [232-239]. These implants may be vertical or angled and are typically done after gate patterning. They add additional well dopants around the source and drain regions providing an increased source-to-drain barrier for current flow. The strength of the halo depends not only on the halo doping concentration, but also on the lateral confinement of the halo. Increasing the halo confinement increases the localisation of the halo effect.

The expected prevalence of non-equilibrium transport effects in sub 0.1 μm device structures means that simulation techniques based on drift diffusion and hydrodynamic models, are unlikely to be suitable for a detailed modelling of transport. Hence only an "exact" solution to the Boltzmann transport equation will supply reliable results and Monte Carlo (MC) simulation is ideally suited for this purpose. By comparing MC simulations with a carefully calibrated drift diffusion model (DD) it is possible to make a quantitative estimate of the importance of non-equilibrium transport on the device performance. Although previous Monte Carlo simulations of p-channel MOSFETs have been performed [240], they have concentrated on the effects of introducing either strained Si or SiGe into the standard p-MOSFET design. To date no MC studies have been carried out on deep sub-micron bulk Si well-tempered p-MOSFETs.

To arrive at a 50 nm channel length (see figure 7.7), a 2 nm thick gate oxide and a super-halo doping with a highly nonuniform profile in both the vertical and the lateral directions is needed. These kind of robust devices, which are very tolerant to short channel effects due to two-dimensional doping engineering employed are usually called well-tempered devices [241].

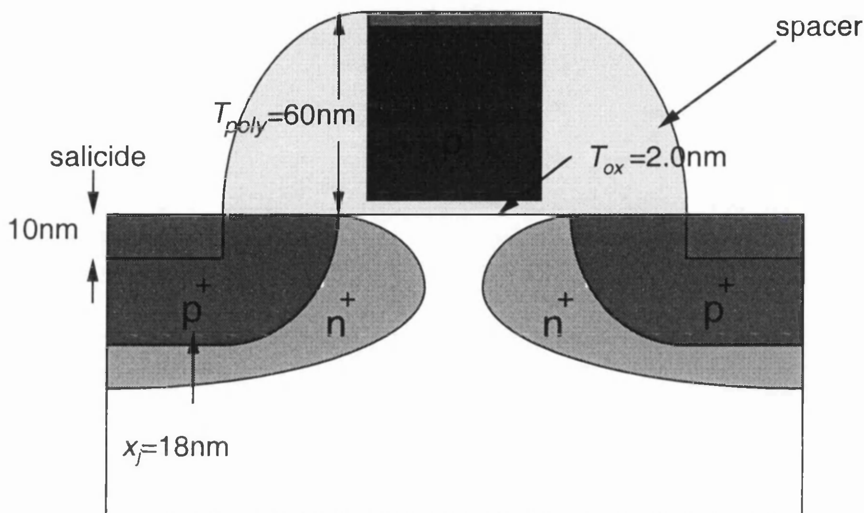


Figure 7.7 Two-dimensional schematic cross section of a 50 nm well-tempered Si p-MOSFET.

The 50 nm device is based upon the super-halo proposed by Taur and Nowak [238]. Reasonable device geometries are designed for the simulations in the deep sub-100-nm regime. However, the original design is intended for n-MOSFETs. The devices used in this section are their p-type analogue mirror images in terms of doping. To adopt this device structure, for example, n-doping is replaced with p-doping and a p-polysilicon gate is used instead of an n-polysilicon gate. The p^+-polysilicon gate has a height of 60 nm. The oxide thickness is 2 nm. The L_{eff}, which is defined between where the p-type dopings in the source and drain fall to 2×10^{19} cm^{-3}, was extracted and found to be 50 nm. L_{poly} was arbitrarily set at 85 nm. In the simulations, only the portion of the p-MOSFET up to the source and drain regions for a lateral distance L_{sd} = 57.5 nm, from the edge of the gate to the model boundary, is used. The origin for the lateral grid is at the left of the model boundary (x = 0). The interface between the gate oxide and bulk is chosen as the depthwise origin (y = 0). The source and drain junction depth is 18 nm. The source and drain contacts extend down a depth of 10 nm from the depthwise origin.

For a 25 nm device, the oxide thickness is 1.5 nm. The L_{eff}, which is defined between where the source and drain dopings fall to 2×10^{19} cm^{-3}, was extracted and found to be 25 nm. L_{poly} was arbitrarily set at 50 nm. In the simulations, only the portion of the p-MOSFET up to the source and drain regions for a lateral distance, L_{sd} = 22.5 nm, from the edge of the gate to the model boundary, is used. The other parameters are the same as in 50 nm device.

The interface scattering model in the Monte Carlo simulations is calibrated by reproducing the universal mobility results for Si p-MOSFETs [240], as shown in figure 7.8. Initially, the DD model is calibrated by comparing the I_D-V_G characteristics with the Monte Carlo simulations at a low drain bias of -0.1 V to obtain the low field mobility, shown in figure 7.9. The low drain bias ensures the absence of non-equilibrium transport effects. It has been found that a low-mobility of 200 cm^2/Vs achieves the best agreement with Monte Carlo data. The saturation velocity, V_{sat} and the fitting parameter β are calibrated to obtain the closest agreement for I_D-V_D characteristics between the DD and Monte Carlo simulations. The resulting (DD and MC) transfer and output characteristics for the 25 nm and 50 nm p-MOSFETs, are shown in figures 7.10 and 7.11 respectively.

It can be seen that the results from DD simulations are consistently slightly lower than the results obtained from MC simulations. This may be attributed to the presence of non-equilibrium transport effects and velocity overshoot in the Monte Carlo simulations, and is consistent with the increasing difference between MC and DD models, when channel lengths are shrunk. Although non-equilibrium effects are clearly present in the p-MOSFETs, with decanano dimensions, their influence on drive current is not significant, as has been observed for n-MOSFETs. Non-equilibrium transport effects become important when the electric fields are such that the carriers are able to move a significant portion of the channel length without reaching equilibrium. The velocities (or energies) in such circumstances are often higher than the equilibrium velocity field characteristics, which is one of the assumptions at the heart of the DD model. The resulting higher velocities within the MC simulations lead to higher drain current characteristics than those predicted by the DD model.

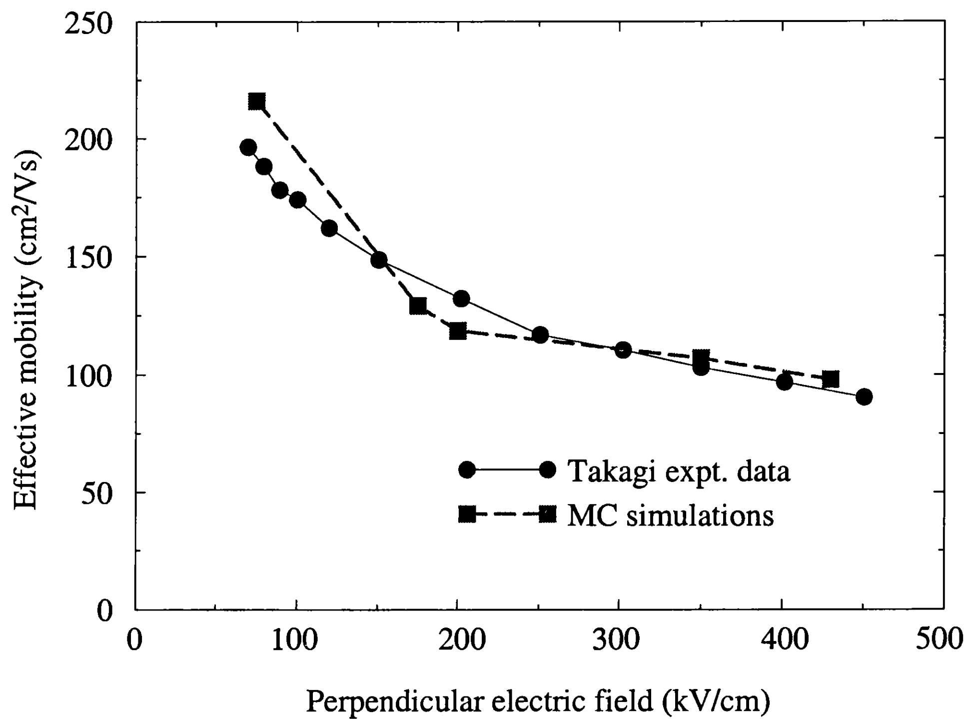


Figure 7.8 Effective mobility as a function of the perpendicular electric field.

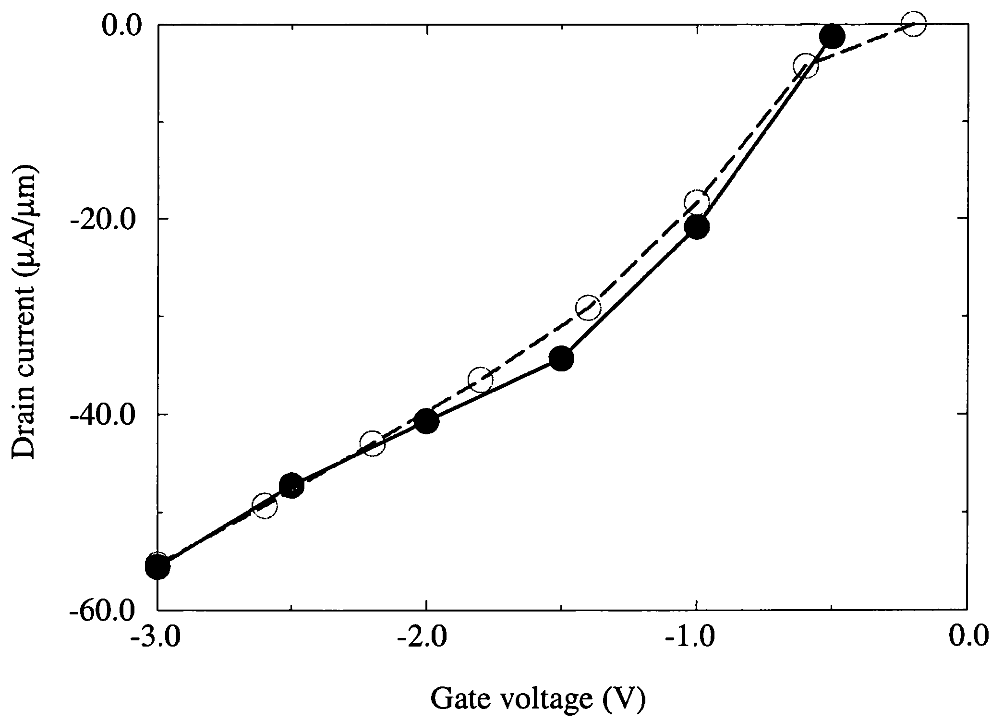


Figure 7.9 I_D-V_G data for a long channel Si p-MOSFET at V_{DS} = -0.1V. Data shown from both MC (solid symbols and line) and DD (open symbols and dashed line) models.

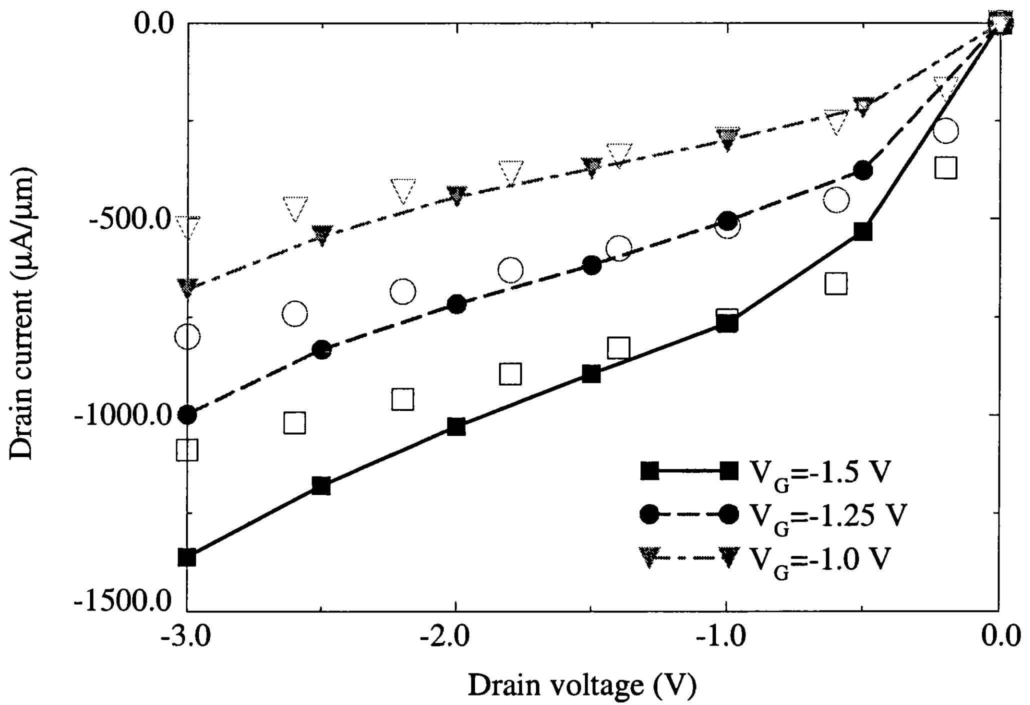


Figure 7.10 I_D-V_D simulation results for 25 nm well-tempered Si p-MOSFET, obtained from both MC (solid symbols with lines) and DD (open symbols).

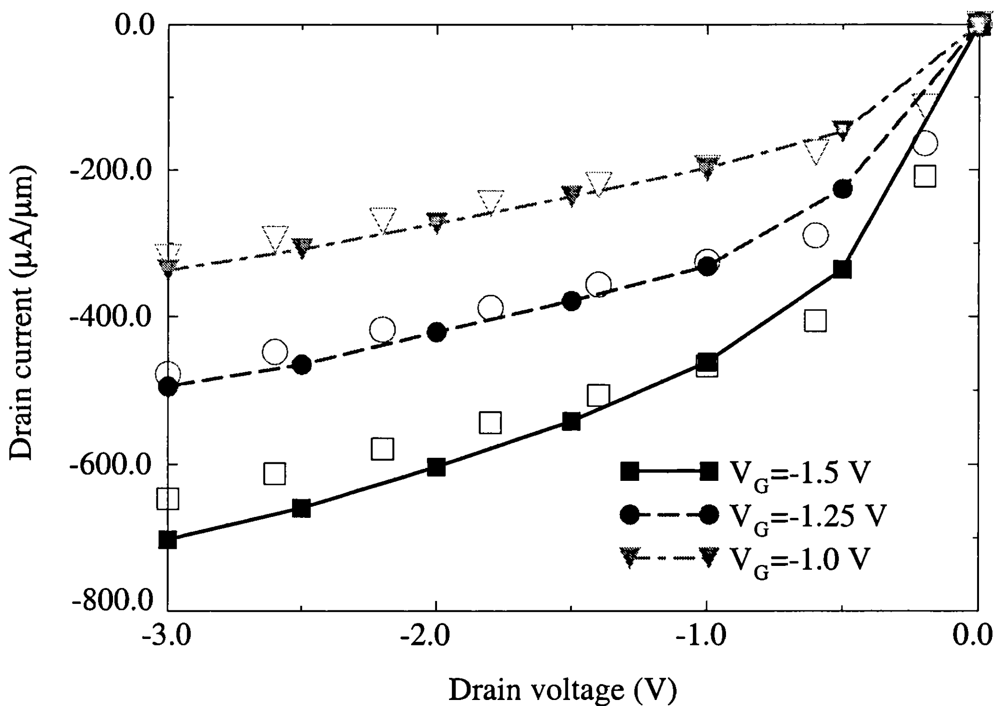


Figure 7.11 I_D-V_D simulation results for 50 nm well-tempered Si p-MOSFET, obtained from both MC (solid symbols with lines) and DD (open symbols).

7.4 Deep Submicron Well-Tempered SiGe p-MOSFETs

Figure 7.12 shows the device structure of the 50 nm well-tempered SiGe p-MOSFET. The thickness of the Si cap is 1 nm. The thickness of the SiGe channel is 10 nm and the Ge mole fraction in the channel is 20%. The thickness of the Si buffer is 5 nm to separate the channel from the delta doping. All other parameters are the same as in Section 7.3.

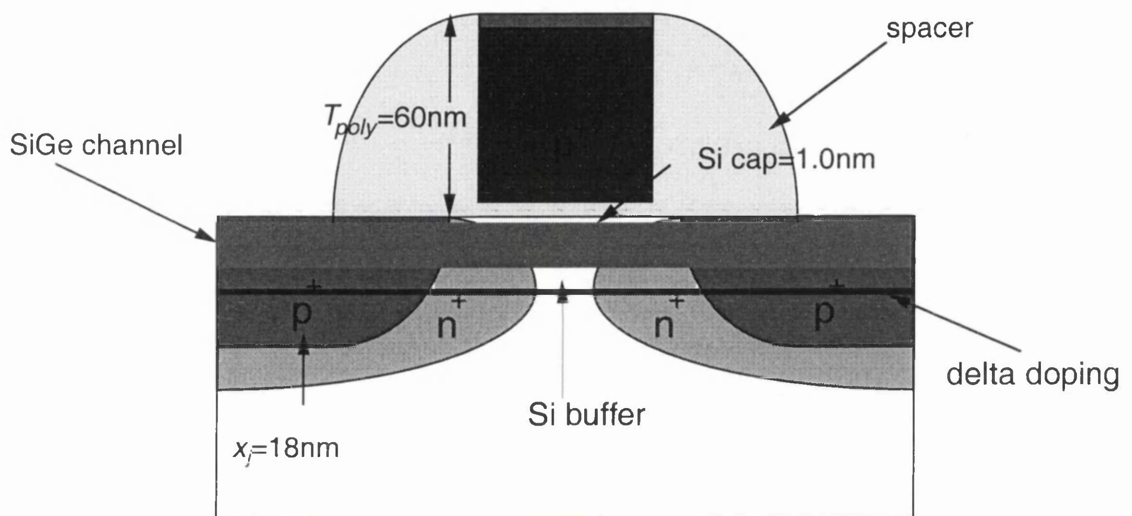


Figure 7.12 Two-dimensional schematic cross section of the 50 nm well-tempered SiGe p-MOSFET.

Here the objective is to investigate weather the well-tempered devices have better characteristics than the conventional SiGe devices. The threshold voltage control, reducing the two-dimensional effects (threshold voltage roll off), and improving the subthreshold slope are investigated.

7.4.1 Well-Tempered 50 nm SiGe p-MOSFET

A. Choice of gate material

Table 7.1 shows the threshold voltage V_{TH}, the two-dimensional effects (threshold voltage roll off) V_{TH} *roll off*, the subthreshold slope S obtained by our simulations for

different gate material. Both threshold voltage roll off and the subthreshold slope are acceptable although the effective channel length of this device is only 50 nm. Comparing the results of chapters 5 and 6, the conventional devices have to keep their effective length around 0.3 μm or larger to prevent short channel effects. The well-tempered devices supply a very good structure for reducing the size of MOSFETs.

Gate material type	n^+-polysilicon	p^+-polysilicon
V_{TH} (V_D=-0.1 V) (V)	-1.515	-0.435
V_{TH} (V_D=-1.2 V) (V)	-1.455	-0.375
V_{TH} *roll off* (mV)	109	109
S (mV/decade)	100	100

Table 7.1 V_{TH}, V_{TH} *roll off* and S obtained by our simulations for different gate material. The effective channel length is 50 nm.

However, the threshold voltages are too high for CMOS applications, especially for n^+-polysilicon condition. Usually the threshold voltages should be controlled around -0.3 V for the CMOSFETs of this size.

B. Adjusting threshold voltages by delta doping

Figures 7.13 and 7.14 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off on the delta doping concentration for a 50 nm well-tempered SiGe p-MOSFET. The threshold voltage can be easily controlled by varying the delta doping concentration. Changes in both the subthreshold slope S (unchanged at 100 mV/decade) and the two-dimensional effects V_{TH} *roll off* (from 118 mV to 145 mV), with delta doping dose variation (from 1.5×10^{12} cm^{-2} to 4.5×10^{12} cm^{-2}) are acceptable.

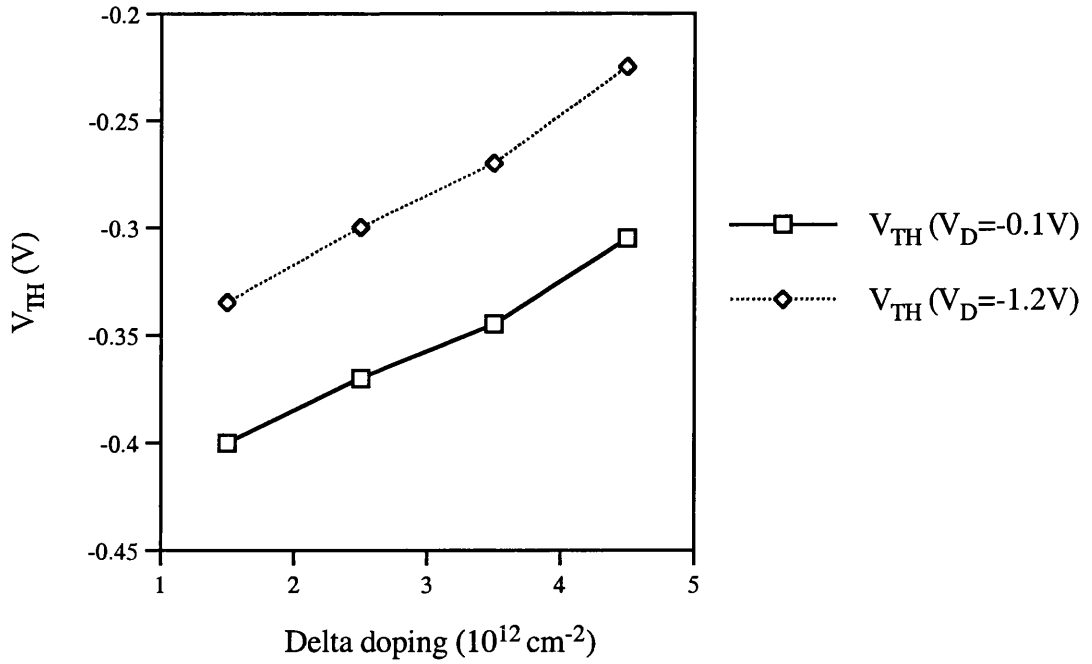


Figure 7.13 Threshold voltage versus delta doping. The gate is p^+-polysilicon and effective channel length is 50 nm.

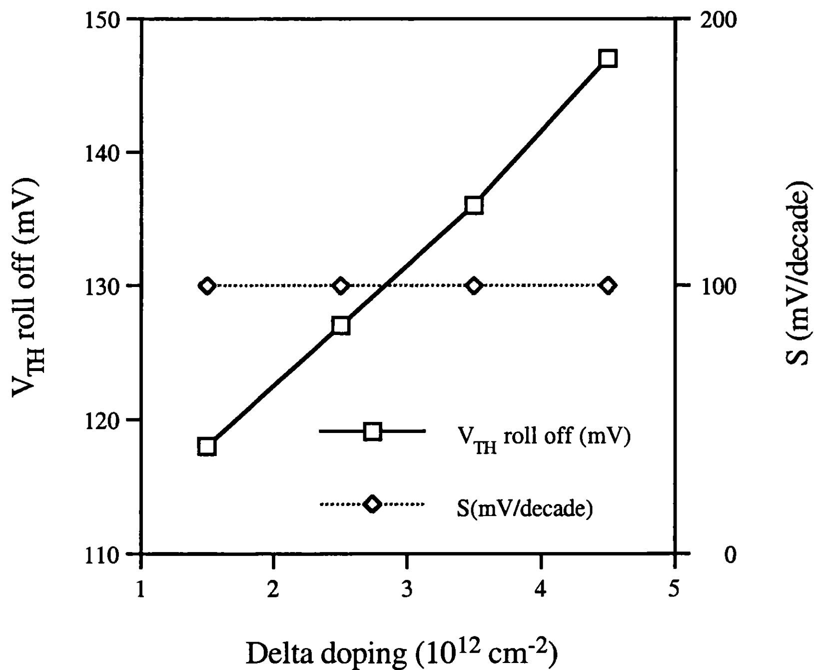


Figure 7.14 Threshold voltage roll off and subthreshold slope versus delta doping. The gate is p^+-polysilicon and effective channel length is 50 nm.

7.4.2 Well-Tempered 25 nm SiGe p-MOSFETs

A. Choice of gate material

Table 7.2 shows the threshold voltage V_{TH}, the two-dimensional effects (threshold voltage roll off) V_{TH} *roll off* and the subthreshold slope S obtained by our simulations for different gate materials. Although both threshold voltage roll off and the subthreshold slope are acceptable, they are not as good as the parameters for the 50 nm device in Section 7.4.1. However, considering the results of chapters 5 and 6, which indicated that the conventional devices have an effective length limited approximately 0.3 μm or larger to prevent short channel effects, the well-tempered devices still provide a very good structure for reducing the size of 25 nm SiGe p-MOSFETs.

Gate material type	n^+-polysilicon	p^+-polysilicon
V_{TH} (V_D=-0.1 V) (V)	-1.670	-0.585
V_{TH} (V_D=-1.0 V) (V)	-1.585	-0.497
V_{TH} *roll off* (mV)	189	195
S (mV/decade)	120	120

Table 7.2 V_{TH}, V_{TH} *roll off* and S obtained by our simulations for different gate material. The effective channel length is 25 nm.

Once again, the threshold voltages are too high for CMOS applications, especially for n^+-polysilicon condition. The delta doping will be used to control the threshold voltages around -0.3 V.

B. Adjusting threshold voltages by delta doping

Figures 7.15 and 7.16 illustrate the dependence of threshold voltage, subthreshold slope and threshold voltage roll off on the delta doping concentration for a 25 nm well-tempered SiGe p-MOSFET. The threshold voltage can be changed by varying the delta doping concentration. Although the subthreshold slope S is acceptable (except when delta doping is as high as 2.5×10^{13} cm^{-2}), the two-dimensional effects V_{TH} *roll off* (from 327 mV to 400 mV) are too large. Thus, the use of delta doping to control the threshold voltage in 25 nm well-tempered SiGe p-MOSFETs does not result in the desired performance in terms of short channel effects. Additional methods must be taken into consideration to optimise 25 nm device operation in p-channel SiGe MOSFETs.

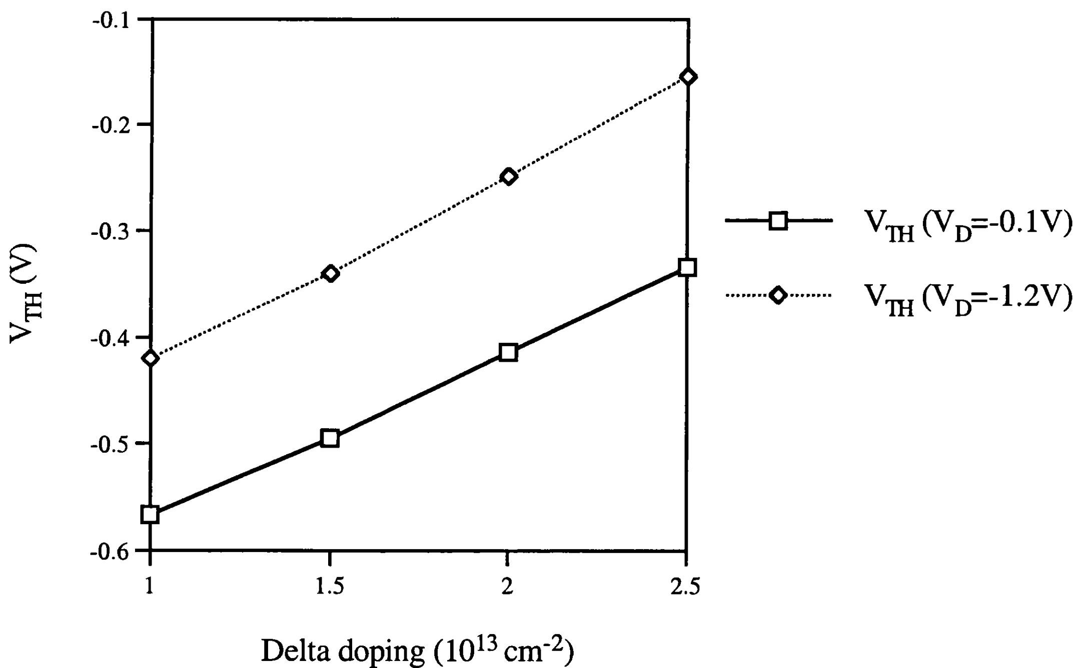


Figure 7.15 Threshold voltage versus delta doping. The gate is p^+-polysilicon and effective channel length is 25 nm.

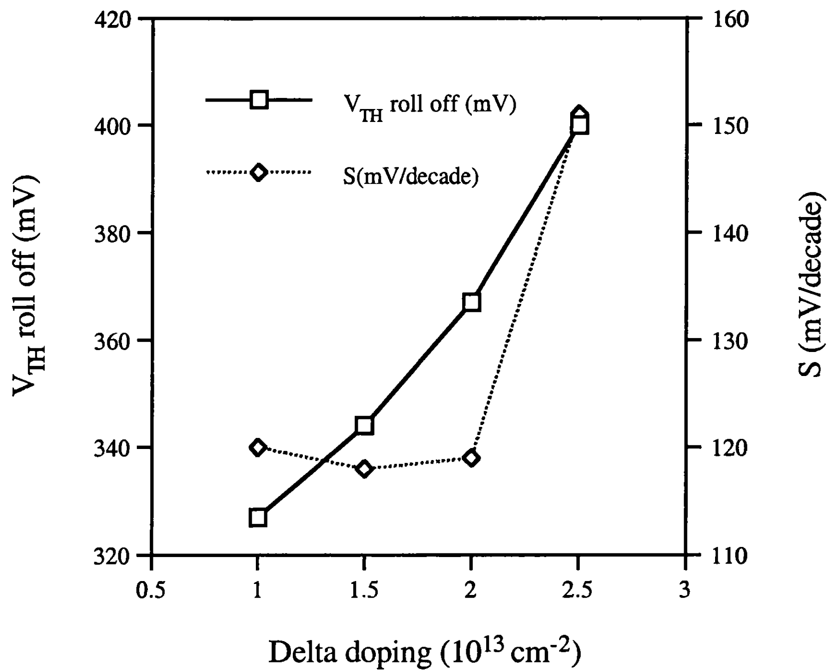


Figure 7.16 Threshold voltage roll off and subthreshold slope versus delta doping. The gate is p^+-polysilicon and effective channel length is 25 nm.

7.5 Summary

Drift diffusion and hydrodynamic simulations for Si and SiGe p-MOSFETs over a variety of gate lengths from 0.5 μm to 0.1 μm have been presented. It has been shown that while drift diffusion and hydrodynamic simulations may provide a reasonable estimate of the *I-V* characteristics for Si devices, the same can not be said for aggressively scaled SiGe devices. The resulting high fields at the source end of the devices means that non-equilibrium transport effects are significant, and that models based on an isotropic carrier temperature may no longer be appropriate, as have been shown by analysing the tensor components of the carrier temperature obtained from Monte Carlo simulation.

Two-dimensional drift diffusion and Monte Carlo simulations of well-tempered Si p-MOSFETs with gate lengths of 25 and 50 nm have been performed. However, it should

be noted that the 25 and 50 nm device designs are hypothetical and based on process technology that is still very much in the development stage. By comparing Monte Carlo simulations with carefully calibrated drift diffusion results, it has been shown that non-equilibrium transport is important for understanding the high current device characteristics in sub 0.1 μm p-MOSFETs.

The well-tempered devices can have better characteristics than the conventional SiGe devices. Both threshold voltage roll off and the subthreshold slope are acceptable although the effective channel length of this device is reduced from 50 nm to 25 nm.

In order to adjust the threshold voltage for the digital CMOS applications, p-type delta doping can be used for 50 nm well-tempered SiGe p-MOSFETs. As the delta doping makes the threshold voltage roll off too large, it can not be used for 25 nm well-tempered SiGe p-MOSFETs.

CHAPTER 8

Conclusions and Further Work

8.1 Conclusions

Throughout this work practical design problems of p-channel SiGe MOSFETs in the context of the SiGe MOS initiative supported by EPSRC has been addressed. Ultimate SiGe performance in p-channel MOSFET has also been explored. Following the efforts to deal with various design problems in SiGe p-MOSFETs suited for future applications, the conclusions from this study have been achieved and summarised below.

The methodology for the modelling of SiGe MOSFET device simulations has been outlined. There are many models around for simulating semiconductor devices: quantum approaches, Monte Carlo, hydrodynamic, energy transport, drift diffusion and compact approaches. As two extremes among these options, however, quantum model is very much still in its infancy, while compact approach does not provide sufficiently accurate results. Therefore Monte Carlo, hydrodynamic, energy transport, and drift diffusion approaches are widely used to simulate SiGe devices. Three different discretization methods, including the "finite difference method", the "finite box method" and the "finite element method", may be chosen for the simulators. These methods are used to decompose the spatial domain of the device and to solve the necessary field equations.

The $Si_{0.8}Ge_{0.2}$ p-MOSFETs fabricated especially for high-field transport studies and the $Si_{0.64}Ge_{0.36}$ p-channel MOSFETs fabricated with a CMOS compatible process in varying gate lengths and two different cap thickness have been calibrated and investigated. Enhanced low field mobility in SiGe layers compared to Si control devices has been observed. The use of a traditional drift diffusion simulator has been extended by

a careful calibration of mobility parameters with respect to measured output characteristics. It has been found that the saturation velocity becomes strongly field dependent, and increases as the channel length is reduced. The accuracy of the experiment based calibration scheme has been verified against Monte Carlo calibrated hydrodynamic and energy transport models, confirming the presence of velocity overshoot and non-equilibrium processes along the channel. The increase in saturation velocity is essential for an appropriate determination of hole velocity at the source end, subject to high fields in thick-oxide devices. The results had indicated that the potential of SiGe p-MOSFETs for velocity overshoot effects is considerably higher than Si counterparts, promising higher performance in the former at equal gate lengths in ultra-small dimensions. The influence of the thickness of the Si cap layer in SiGe p-MOSFET architecture has also been indicated. It has been found that the parallel conduction occurs more easily in thick Si cap layer than in thin one.

The effects of the punchthrough stopper, undoped buffers and delta doping for SiGe p-MOSFETs have been analysed systematically for devices of current and future generations. It has been found that the threshold voltage roll off may be avoided by using a punchthrough stopper. The maximum thickness of the undoped buffer depends strongly on the channel length. For a 0.5 μm channel length the maximum affordable thickness of the undoped buffer is 100 nm, while for a 0.1 μm MOSFET the buffer thickness must be reduced to 10 nm. In order to adjust the threshold voltage for the digital CMOS applications, p-type delta doping is required for n^+-polysilicon gate p-MOSFET. As the delta doping makes the threshold voltage roll off a more serious device issue, the delta doping dose used in these devices must be minimised.

An extensive study of the delta doped SiGe p-channel MOSFET proposed for CMOS applications has also been presented. It is easy to obtain a threshold voltage around -0.5 V, with satisfactory subthreshold slope and threshold voltage roll off for a channel length of greater than 0.2 μm, by adjusting the substrate concentration and the delta doping. The thickness of the gate oxide has a strong influence on the control of short channel effects. The smaller the thickness of the gate oxide, the better the properties of the subthreshold slope and threshold voltage roll off, thus allowing more room for

tailoring delta doping. It would be difficult to scale the SiGe p-channel devices with delta doping layers below 0.2 μm, and to retain an acceptable threshold voltage.

The two-dimensional process simulator TSUPREM-4 and the two-dimensional device simulator MEDICI have been used to optimise and design Si/SiGe hybrid CMOS technology. The necessary process parameters provided by the partners at Southampton and Warwick Universities have been outlined. The output of TSUPREM-4 has been transferred automatically to the MEDICI device simulator. This has made the simulation results more realistic and an assessment of technological parameters become possible. Throughout the simulations, it has been found that a doped buffer can be used to adjust threshold voltage and to prevent short channel effects, and p-type delta doping below the channel can be used to tune the threshold voltage. However, delta doping will increase the short channel effects. The solution requires a trade-off, and if the gate length decreases further, even this method will fail. One boron implant can be used to adjust threshold voltage and prevent short channel effects for Si/SiGe n-MOSFET. However, this method only allows crude V_{TH} control, and for more reproducible results, lower energy V_{TH} control implantation should be employed.

As a general conclusion from the design exercises on SiGe MOSFETs, the lightly doped drain structures (LDD MOSFETs) will be in all probability required in very small devices. They will decrease the lateral sideways diffusion and allow threshold voltage roll off to be minimised. These structures, however, will generally reduce drain current due to an increase in the series resistance of the drain region. Further consideration must be made of these trade-offs.

Drift diffusion and hydrodynamic simulation results for SiGe p-MOSFETs have been presented for the first time, with transport parameters extracted from the in-house full-band hole Monte Carlo transport simulator. It has been shown that while drift diffusion and hydrodynamic simulations may provide a reasonable estimate of the *I-V* characteristics for Si devices, the same can not be said for aggressively scaled SiGe devices. The resulting high fields at the source end of the devices means that non-equilibrium transport effects are significant. Therefore for holes, models based on an isotropic carrier temperature may no longer be appropriate, as it has been shown by

analysing the tensor components of the carrier temperature obtained from Monte Carlo simulation.

Two-dimensional drift diffusion and Monte Carlo simulations of well-tempered Si p-MOSFETs with gate lengths of 25 and 50 nm have been performed. By comparing Monte Carlo simulations with carefully calibrated drift diffusion results, it has been shown that non-equilibrium transport is important for understanding the high current device characteristics in sub 0.1 μm p-MOSFETs. The well-tempered devices can have better characteristics than the conventional SiGe devices. Both threshold voltage roll off and the subthreshold slope are acceptable although the effective channel length of this device is reduced from 50 nm to 25 nm. In order to adjust the threshold voltage for the digital CMOS applications, p-type delta doping can be used for 50 nm Well-Tempered SiGe p-MOSFETs. As the delta doping makes the threshold voltage roll off too large, it can not be used for 25 nm Well-Tempered SiGe p-MOSFETs.

8.2 Further Work

Although this work has shone considerable light on device design above 0.1 μm, more work is required to optimise SiGe MOSFET design in devices in deep decanano dimensions. This is mainly due to uncertainties surrounding several key technological parameters, such as junction depth, oxide thickness and delta doping. Experimental data for smaller channel length SiGe MOSFETs are needed to further investigate the non-equilibrium transport and other effects in SiGe devices (such as the two-dimensional effects V_{TH} *roll off*). This will make it possible to refine the calibration approaches, which in turn provide better estimates for DD, HD and ET simulations used in the design of advanced devices.

Monte Carlo device simulations will also be used to analyse the non-equilibrium transport in SiGe devices and to calibrate the drift diffusion simulations of the well-tempered devices. In this approach, the velocity profile along the channel and current output from Monte Carlo simulations are to be used as inputs to the calibration procedure.

Thus, Monte Carlo device simulations, normally inefficient and slow for design purpose, can be utilised to provide accurate choice of transport parameters in low-level simulations.

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