Accelerating Stresses For Life Testing of Switch-Mode Power Supplies

Anne R. Keown

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Department of Electronics and
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University of Glasgow

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Abstract

I.B.M U.K. Ltd procure Switch-Mode Power Supplies to place in the computers they manufacture. These Power Supplies are tested to ensure that they meet a specified reliability target. Due to the high Mean Time To Failure (MTTF) the test duration required to verify the MTTF is in excess of three months. In an attempt to find a way to reduce the time required to ensure this requirement is met it was decided to investigate a selection of stresses from the point of view of their effectiveness as a means of accelerating life tests. Subsequent to a theoretical exploration of the topics of Switch-Mode Power Supplies, Reliability and Accelerated Life Testing the power supplies were subjected to High Ambient Temperatures, High Relative Humidity, Power Cycling, Temperature Cycling and various conditions of electrical Stress. The effectiveness of these stresses was gauged by checking the power supplies' performance after various intervals during which they had been subjected to stress.

It was discovered that high ambient temperatures have a measureable effect on electrolytic capacitors, which is physically related to the amount of energy to which the capacitors are subjected, to the extent that several capacitors failed during the tests without other damage being done to the power supply. It is recommended that further research be undertaken with a view to developing a relationship between capacitor degradation and power supply life test duration because, since the capacitors MTTF is greater than that of the power supply, failure due to degradation would indicate that the power supply had passed its specified MTTF.

Acknowledgements

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Chapter 1:Introduction

Section 1.1:Linear Power Supplies

Electronic equipment which is powered by connection to the mains supply usually requires circuitry to convert the high voltage A.C. into low voltage D.C.

Traditionally this circuitry took the form of what is referred to as a linear power supply. Figure 1.1. is a block diagram of such a power supply.

The A.C. from the mains is passed through a step-down transformer (a). This reduces the voltage level from 240V to below 50V which is closer to the level required by devices such as transistors and integrated circuits, and is the region of 12-15V.

In some instances the equipment being powered will require voltages which are higher than that supplied by the mains e.g. D.C. voltages in the kilovolt range. In these cases a step-up transformer replaces the step-down transformer mentioned above.

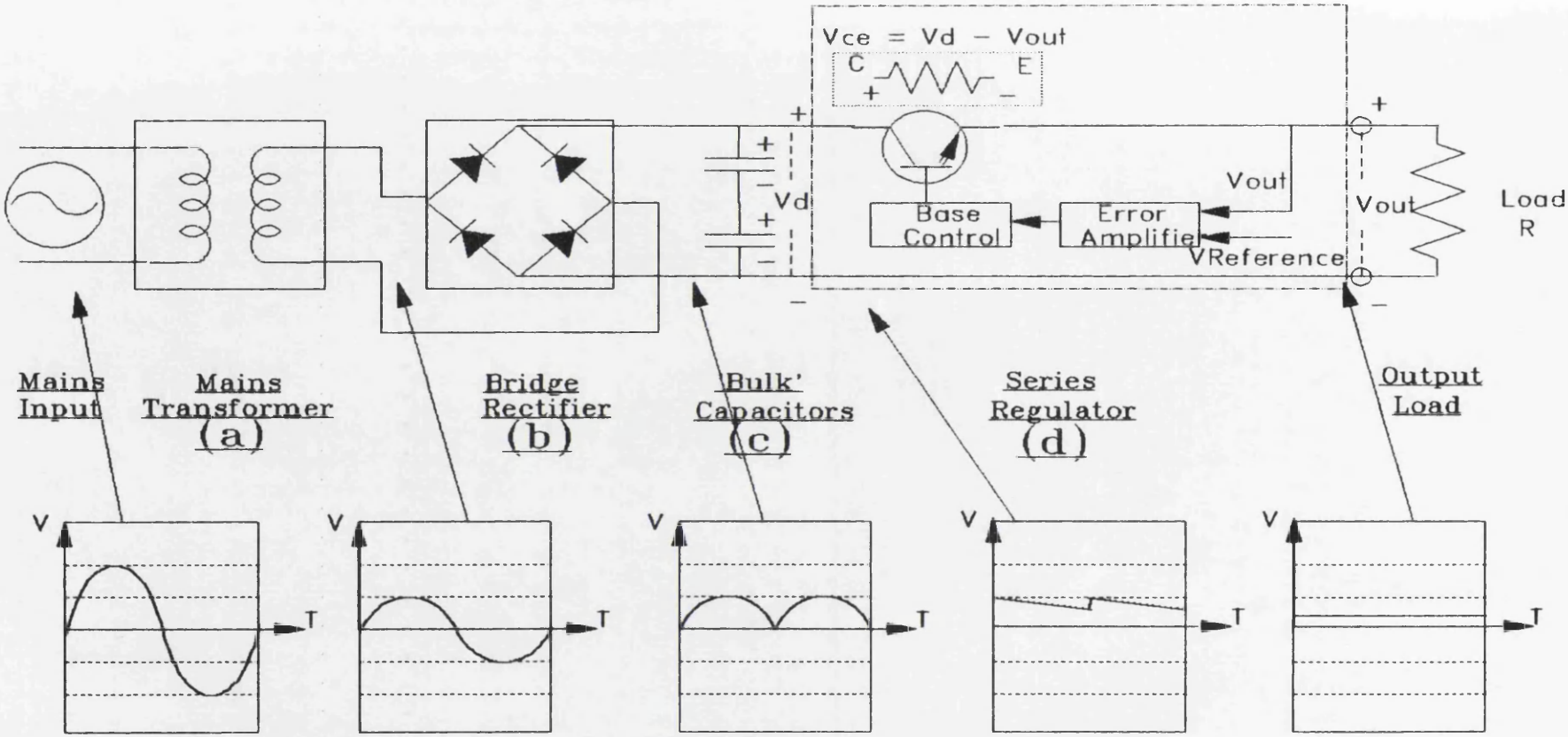
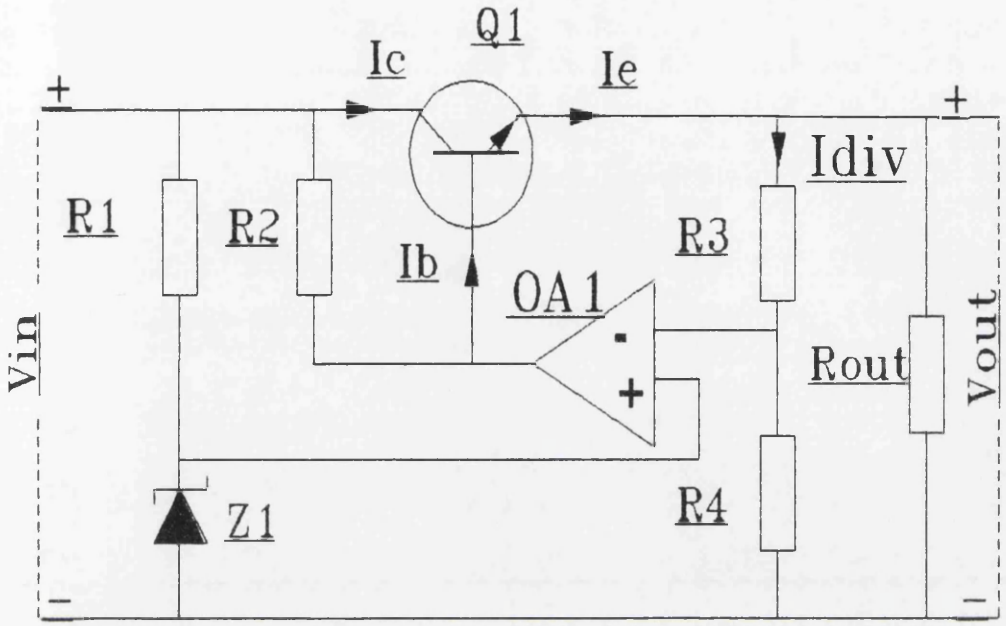


Figure 1.1
Linear Power Supply

The A.C. output of the transformer is made unidirectional, usually by a bridge rectifier (b). This, however, is still by no means the steady D.C. level required. The next stage of the circuit consists of large electrolytic capacitors (c) which smooth the output of the bridge rectifier and provide D.C. of an almost constant level. There is inevitably a degree of ripple voltage because it is unlikely that the capacitors will completely smooth the waveform.

Transformers cannot be guaranteed to produce the correct voltage level at their outputs. This can be due either to variations in the mains supply or to the fact that the transformer may not be custom built to the specific application for which it is being used. Additionally the output of the power supply can fluctuate due to changes in the electronic circuitry being supplied. Such changes can be caused by, for example, resistors changing value as they heat up. It is therefore necessary to regulate the D.C, output. This is acheived by a regulator circuit (d) such as that in Figure 1.2. The regulator can take this discrete form or appear as a single Integrated Circuit (I.C.).

Voltage Regulation



Q: Transistor **Z: Zener Diode**

R: Resistor **OA: Amplifier**

Vin: Input Voltage **Vout: Output Voltage**

Ic: Collector Current **Ib: Base Current**

Ie: Emitter Current **ß: Transistor Current Gain**

Idiv: Current through Voltage Divider

$$Ic = ß \times Ib \qquad \text{Equation 1.1}$$

$$Ie = Ib + Ic \qquad \text{Equation 1.2}$$

$$Vout = (Ie - Idiv) \times Rout \qquad \text{Equation 1.3}$$

Figure 1.2
Series Regulator

A fraction of the regulator's output voltage appears at the inverting input of a differential amplifier. The non-inverting input of the amplifier is supplied with a reference voltage at the level required by the electronic circuitry being supplied at the output; i.e. the load circuitry. The reference voltage is usually held at the correct level by a zener diode. The output of the amplifier is fed to the base of the transistor; the collector of which is supplied with the smoothed D.C. voltage. When the regulator output is too high the amplifier output falls and reduces the base current of the transistor, thereby reducing the collector current (equation 1.1), the emitter current (equation 1.2) and the output voltage (equation 1.3). When the output voltage level is too low the base current is increased.

In many cases the input voltage of the regulator can be more than 10V higher than the output. The excess created by this voltage and the current through the transistor can only be dissipated as heat and is therefore wasted energy. This, combined with losses in the large 50Hz mains transformer, make the linear power supply very inefficient. Typically the efficiency of a linear power supply is in the 30% to 60% range.

Additionally, due to the low frequency of the mains supply, the transformer and smoothing capacitors are very large which causes the linear power supply to be very bulky.

Section 1.2 Switch-Mode Power Supplies

For the above reasons the linear power supply has been superseded by the Switch-Mode Power Supply(S-MPS) in the majority of mains powered electronic products. Figure 1.3 is a block diagram of this lighter and more compact type of power supply which uses a small, high frequency transformer but no mains transformer and is more than 60% efficient.

The input passes through a filter (a) to prevent any high frequency noise present in the mains voltage entering the power supply. This filter also removes the possibility of any noise from the power supply polluting the mains. The filtered voltage is then converted into unregulated D.C. using components (b), a bridge rectifier, and (c) two large capacitors which are commonly referred to as the 'bulk caps'. The voltage output of the capacitors is approximately 400V D.C.

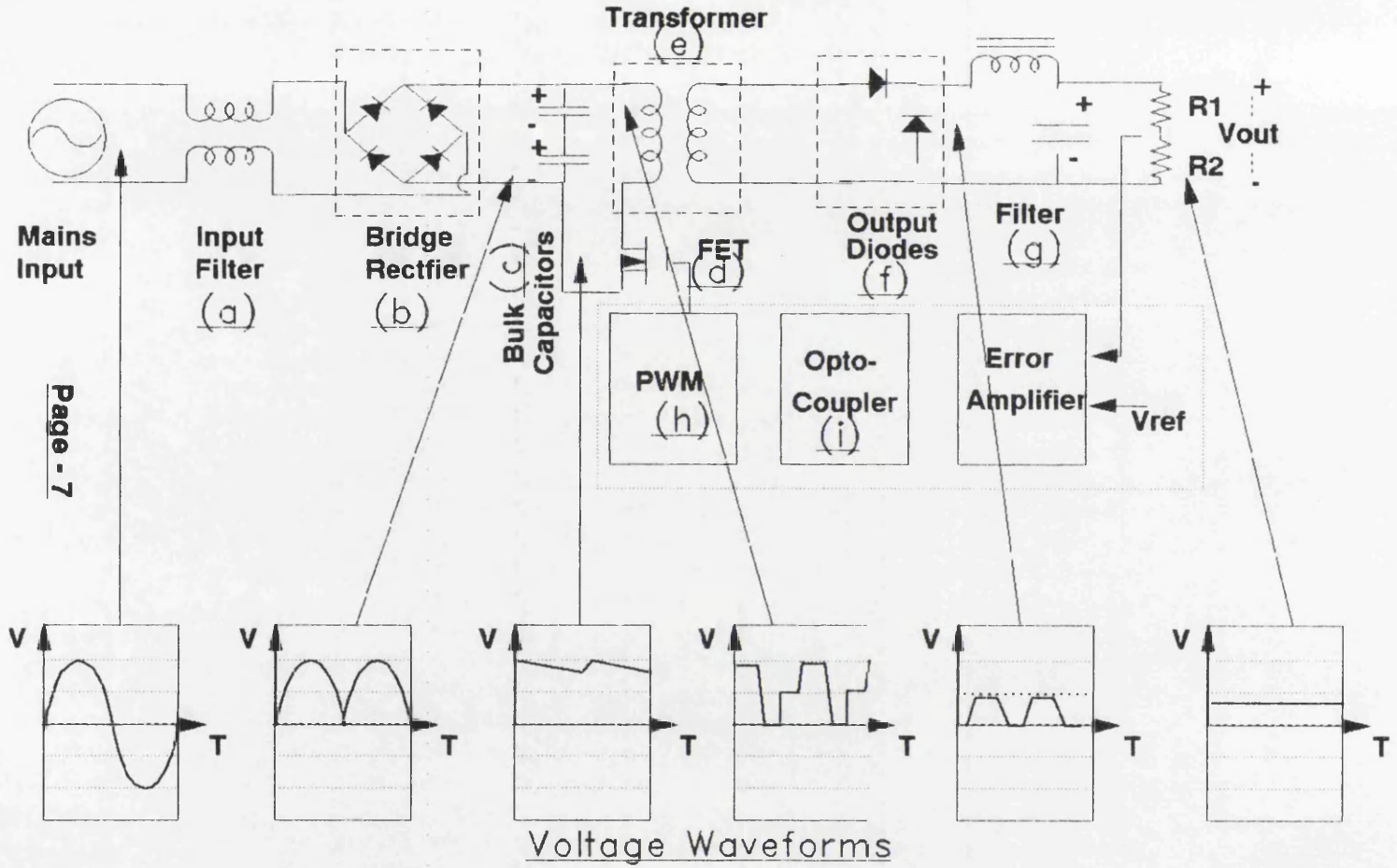


Figure 1.3
Switch-Mode Power Supply

Two capacitors are used because this allows the power supply to be used with different values of mains voltage. An explanation of how this is accomplished appears below in the section concerning the 'voltage doubling' circuitry.

This D.C. is then passed to a Field Effect Transistor (FET), component (d). This FET is the first component in the section of circuitry known as the DC to DC converter. There are several types of D.C. to D.C. converter. Each type operates in a similar manner to that described below but there are subtle differences in the way electrical energy is transferred from the input of the converter to its output. The D.C. to D.C. converter depicted in Figure 1.3 is known as a 'Forward Converter'. Other varieties of converter, i.e. converter topologies, include the Flyback and Cuk converters.

The FET acts as a switch and is controlled by component (h), a pulse width modulator (PWM). When the PWM output is high the FET is switched on and the switch is closed. This causes the D.C. level to appear at the primary of the step-down transformer, component (e). When the PWM output is low the FET is off and the switch is open. In this case 0V appears at the transformer input. The FET is switched on and off at a frequency of 50kHz or above which is the frequency of the voltage waveform which appears at the primary of the transformer.

If this waveform were allowed to reach the mains there is a possibility that it could affect other equipment being powered by that mains supply. The aforementioned input filter (a) must prevent this signal from coming in contact with the mains waveform entering the power supply.

The inductive nature of the transformer changes the 'chopped' D.C. which appears at its input into high frequency A.C., with a magnitude of approximately 50V, which appears at its output. This is rectified by what are referred to as the output diodes, components (f), and smoothed by the filter (g) which consists of an inductor and capacitor(s). The inductor serves as the main energy storage device during the switching cycle because its very nature prevents rapid changes in the direction, and size, of the current flowing through it.

The regulation of the output voltage involves feeding back that output voltage to the Pulse Width Modulator. In order to maintain the primary:secondary isolation across the transformer , which is required to avoid the possibility of lethal voltage levels appearing at the outputs , this feedback is usually via an optocoupler. The level of output voltage will determine the voltage level at both sides of the optocoupler which will in turn determine the voltage measured by the PWM.

If the output voltage level is too high, compared with the internal reference voltage of the PWM, the PWM decreases the duty cycle of the FET, i.e. the ratio of On Time:Total Switching Period. This results in a lower voltage at the output. If the output voltage is too low the duty cycle is increased.

If more than one D.C. output level is required, as is the case when the power supplies are used in computers where different voltages are needed for circuitry, disc drives and cooling fans, then the transformer used is one with multiple secondary windings. In some cases it is also necessary to provide series regulators, the same as those used in linear power supplies, to regulate the additional outputs. The need for these extra regulators is due to the fact that the PWM will be controlled by one output and will adjust the duty cycle according to the needs of that output. Even with different windings ratios on the transformer secondaries it will not be possible to achieve precisely all the various output voltages required and the extra series regulators will ensure that all supplementary output voltages are at the correct levels.

Figure 1.4 shows a circuit diagram of a commercial SMPS. The D.C. to D.C. converter, i.e. the circuitry described above, forms only a small part of the complete circuit. The other components serve, among other things, to protect the power supply from damage if a fault occurs at either the mains input , e.g. an excessive level of mains voltage, or at one of the outputs e.g. a short circuit.

Section 1.3 Voltage Doubling Circuitry

In order to allow manufacturers of power supplies, or those of products which include power supplies, to export to a variety of countries commercial power supplies include components which allow the power supply to operate whether the input voltage is the 240V used in this country or the 110V used in The United States, France etc. This set of components is referred to as the 'voltage doubling' circuitry and forms the basis of Figures 1.5(a) and 1.5(b)

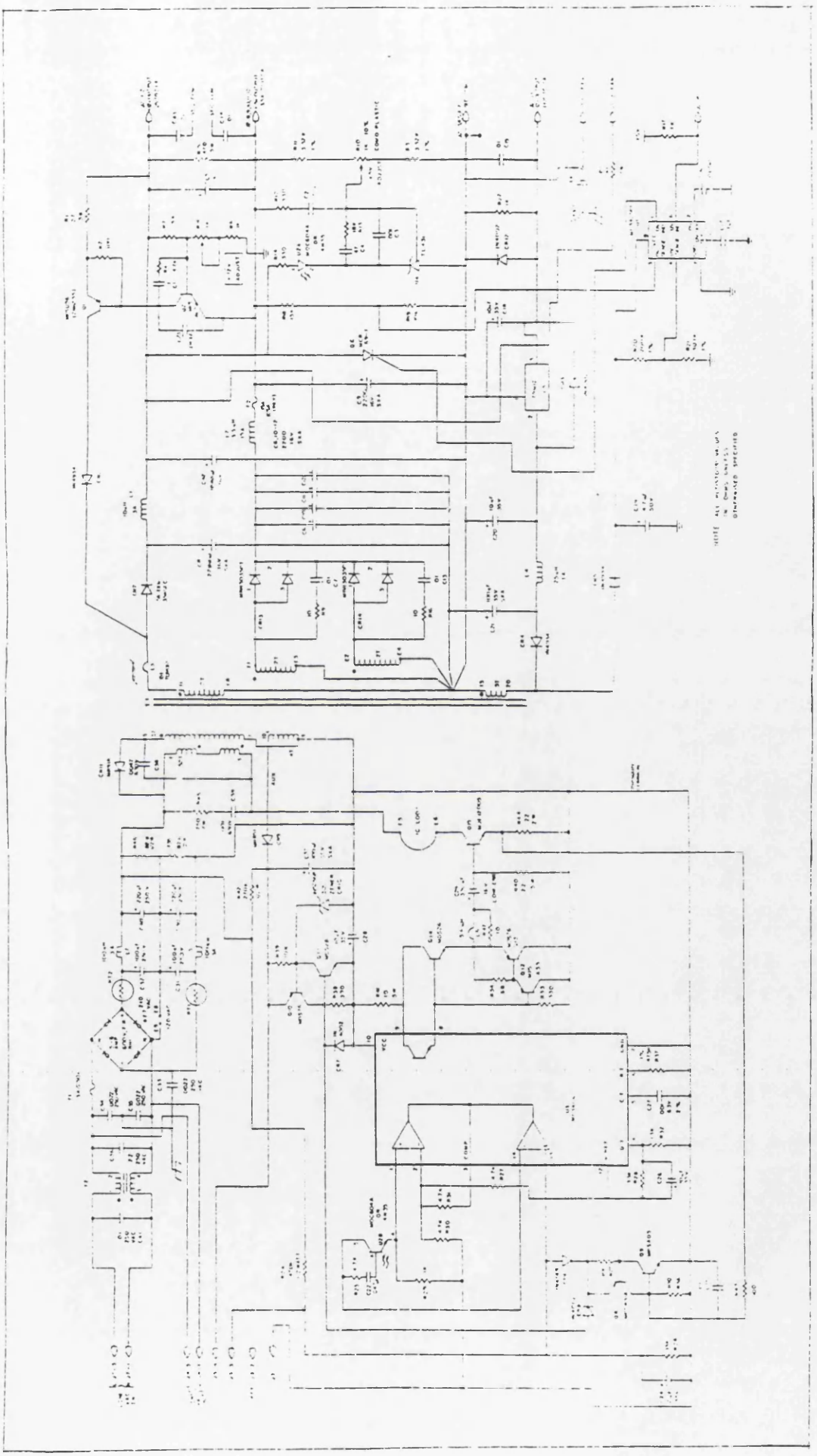


Figure 1.4
Commercial Power Supply

> indicates the path taken by current during the positive part of the A.C. cycle.

>> indicates the path taken by current during the negative part of the A.C. cycle.

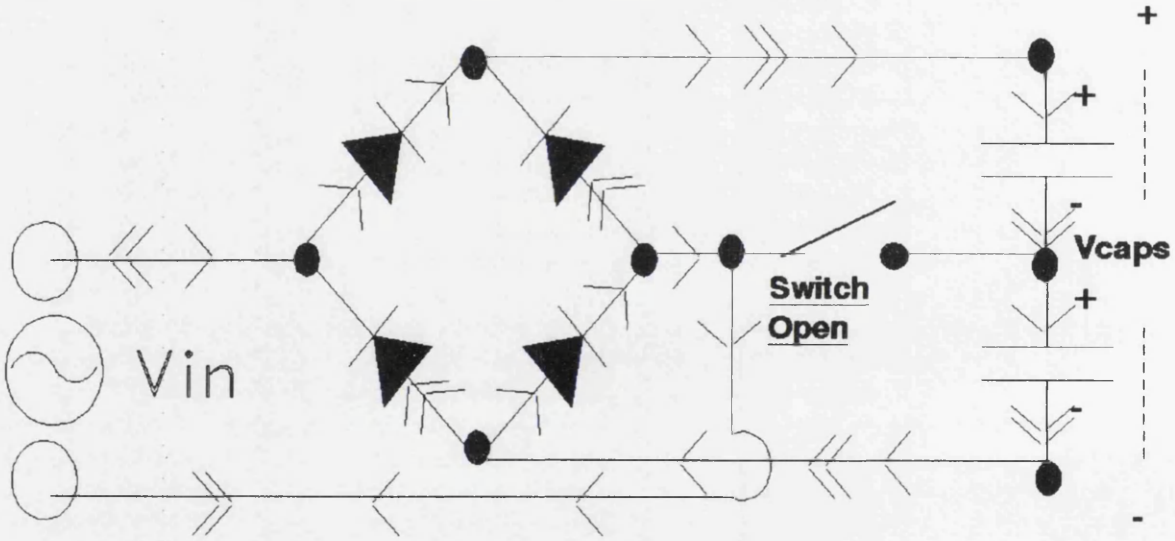


Figure 1.5 (a)

Voltage Doubling Circuitry: Vin = 240V

> indicates the path taken by current during the positive part of the A.C. cycle.

>> indicates the path taken by current during the negative part of the A.C. cycle.

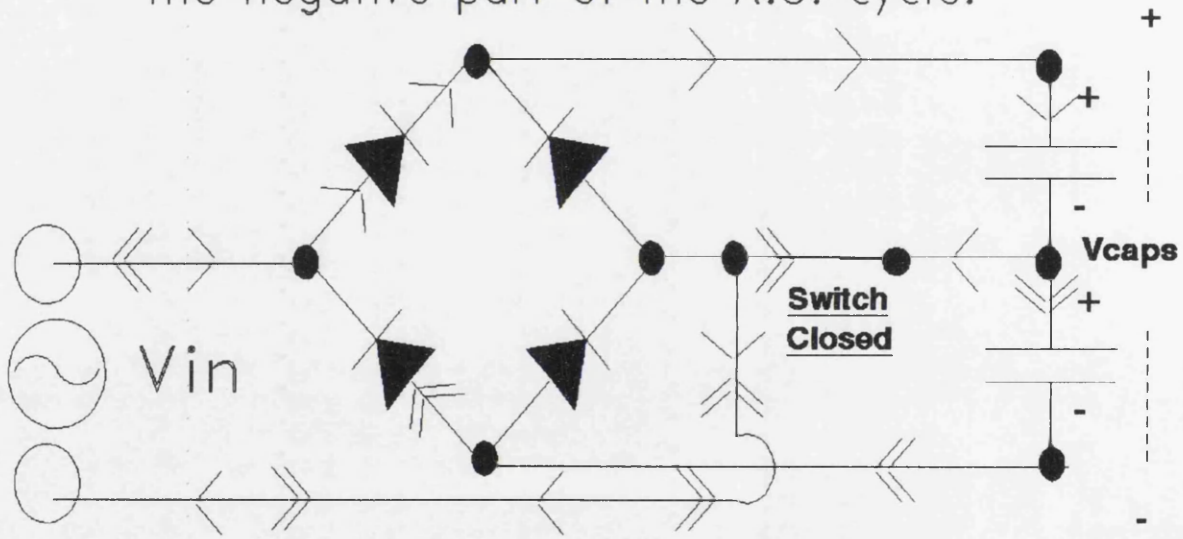


Figure 1.5 (b)

Voltage Doubling Circuitry: Vin = 110V

In cases where the power supply can detect the level of input voltage being supplied the switch takes the form of a triac which conducts only if the mains voltage is above a certain level. In other cases the user is required to set an actual physical switch depending on whether the input voltage lies in the range which includes 110V, or that which contains 240V.

When the power supply is operating from 240V the bridge rectifier operates normally and all of the rectifed 240V is shared equally by the two bulk caps at all times. This situation is depicted by Figure 1.5(a).

If the input voltage lies in the lower range the switch is closed which causes one capacitor to be charged during the positive half of the a.c. cycle and the other to be charged during the negative half. This is the case in Figure 1.5(b). In both cases the combined voltage across the capacitors is in the region of 300V.

Section 1.4: Performance Requirements

The power supplies which form the subject of this thesis are those used by IBM in computers. Most of the power supplies investigated were 118W power supplies i.e. a total of 118W could be supplied at the outputs for normal use. Samples are submitted for test, before power supplies are purchased from various vendors, to ensure that they meet the rigorous IBM specifications. Such a test can take twelve weeks. During that time the power supply is checked to ensure, for example, that it can shut down during a brief transient in the mains voltage.

An individual specification exists for every size and type of power supply IBM uses and, as well as stating the physical dimensions and performance crtieria of the power supply, contains precise details of tests which must be carried out on the power supplies together with acceptable quantatative results for these tests.

For the purposes of checking the effects of the processes documented in this thesis tests detailed in the relevant power supply specification were used. There are two areas of operation where any faults would be immediately obvious and most likely to affect the day to day operation of the equipment being supplied. The first of these is referred to as 'Regulation' and is the requirement that the voltage levels at the power supply outputs lie within the allowed ranges. The second parameter is the ripple voltage at the outputs. If the output voltage fluctuates too much due to the switching nature of the power supply then the equipment could fail to operate properly. It is the task of the filter capacitors to remove voltage ripple but there will always be a certain amount which will tend to increase as the capacitors age. Checks of regulation and ripple voltage, among other checks, formed an integral part of each of the tests documented in the pages which follow.

Chapter 2- Reliability and Accelerated Life Testing

(Relevant Background Theory)

Section 2.1 Product Reliability

It is becoming increasingly important that equipment, both mechanical[4] and electronic, can be trusted to operate at all times under all conditions in which it is used. At one extreme the consequences of equipment failure could merely be inconvenient; in contrasting situations such failures could be fatal e.g. Failures in the control system of a nuclear reactor.

In addition to the safety aspect there are also cost considerations. There are two major instances in which unreliable equipment can incur considerable expense for the owner:

The first concerns equipment situated where the cost of access for repair or servicing is prohibitive e.g. underwater cables or satellites.

The second, and that which is probably more relevant to the subject matter dealt with in this thesis, is in manufactured goods which are covered by a warranty. If a company's product breaks down within the period covered by the warranty then the company must bear the expense of repairing or replacing that product. Obviously when large numbers of the particular product are being sold the cost involved can be considerable. Additionally if that company sells products which are inclined to fail after a relatively short period their reputation, and consequently their sales figures will suffer. Customers have come to, and will continue to, expect ever increasing ever increasing operational lifetimes for the products they buy.

For these reasons a great deal of industry time and money has been put towards the investigation of equipment reliability in an attempt to find ways of predicting and lengthening the life time of manufactured goods.

In the course of these investigations certain parameters have been defined. The parameter most usually quoted in connection with the reliablilty of a device is the Mean Time To Failure (MTTF). This is a statistical measurement which is calculated by measuring the time to failure of as many samples of the device as possible and then calculating the average or mean of these.

Where a device or item of equipment is repairable the expression becomes Mean Time Between Failures (MTBF).

Regardless of which expression is used this parameter is usually represented by θ. The expression population refers to the collection of sample devices used in the test.

It is common practice when investigating the reliability of a device to plot what is known as the 'Cumulative Distribution Function' (F(t) v t). Figure 2.1 gives a list of definitions. There are a variety of common cumulative distribution functions such as the Exponential, Normal and Weibull Functions.

Cumulative Distribution Function F(t)

This is a plot of:
The probability of the device failing by time t v time t
or:
The Fraction of the total population failing by time t v time t
and has the equation:

$$F(t) = 1 - e^{-\frac{t}{\theta}} = 1 - e^{-t\,\tau} \qquad \text{Equation 2.1}$$

τ **is the failure rate or HAZARD FUNCTION which is defined below**

Reliability Function R(t)

The probability of a device surviving beyond time t
or:
The fraction of the total population surviving beyond time t

$$R(t) = 1 - F(t) = e^{-\frac{t}{\theta}} = e^{-t\,\tau} \qquad \text{Equation 2.2}$$

Probability Density Function f(t)

The probability of a device failing between t and t+dt a short time later
or:
The fraction of the population failing in that interval

$$f(t) = \frac{dF(t)}{dt} = \frac{1}{\theta} e^{-\frac{t}{\theta}} \qquad \text{Equation 2.3}$$

Hazard Function h(t)

(Instantaneous Failure Rate ( ))

The probability, or fraction of the population, which survives to time t but fails by time t+dt a short time later.

$$h(t) = \frac{f(t)}{(1-F(t))} = \frac{\frac{1}{\theta} e^{-\frac{t}{\theta}}}{e^{-\frac{t}{\theta}}} = \frac{1}{\theta} = \tau \qquad \text{Equation 2.4}$$

N.B. The relationship $\theta = 1/\tau$ only applies to the EXPONENTIAL Cumulative Distribution Function (C.D.F.)
As do the those expressions above involving equalities of θ

Figure 2.1
Reliability Definitions and Equations

The model usually used with electronic assemblies, of which Switch-Mode Power Supplies are an example, is the Exponential function the equations for which are also given in Figure 2.1.

Section 2.2:The Life of a Product.

It is a plot of h(t) v t which yields that which is probably the best known reliability curve, i.e. the 'Bathtub' Curve, which is shown in Figure 2.2.

The high initial failure rate is due to failure of products with manufacturing defects. It is common practice to age, or 'burn-in', products before they are sold in order that these failures occur while the product is still in the hands of the manufacturer. This all but eliminates the failures which occur in the field . i.e. when the product is with the customer.

As a result of burn-in the failure rate in the field should be constant, this is represented by the flat section in the middle of the curve. This period is known as the 'useful life'.

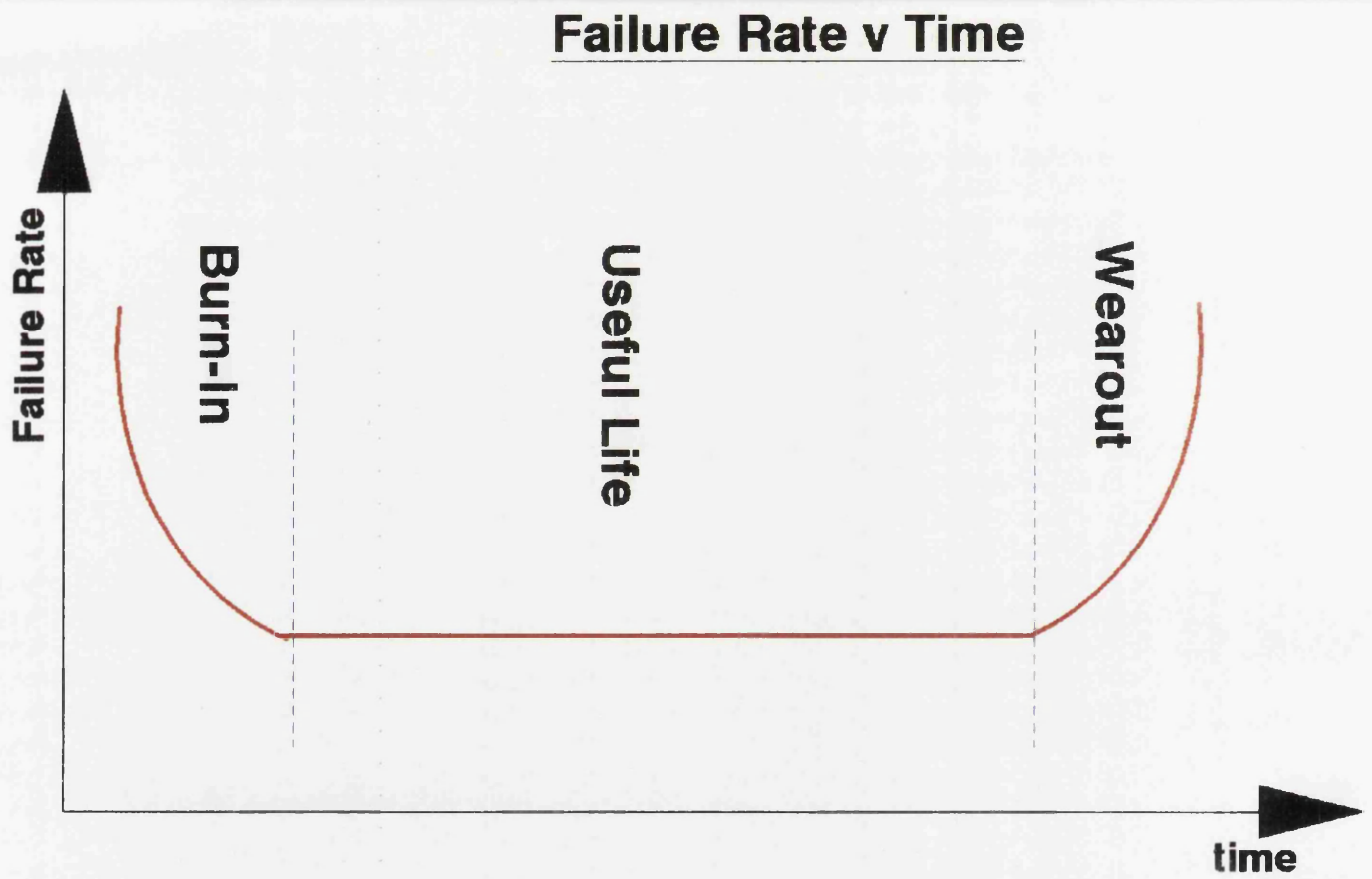


Figure 2.2 Classic Bathtub Curve

The final section of the curve is known as the wearout interval. As the products pass their useful life the number of failures starts to increase as the products literally wear out. This could be caused by, for example, corrosion of metal parts.

Section 2.3: Failure Rates and MTTFs

What a life test sets out to do is indicate the likelihood of a sufficiently high MTTF. The population undergoing life test will have passed through the burn-in process and should therefore have the constant failure rate of the 'useful life' section of the bathtub curve.

A typical MTTF for an S-MPS would be 50,000 hours, slightly over five years, but this requirement is increasing and it is not uncommon for a specification to demand an MTTF of 100,000 hours. Fortunately, because the failure rate is assumed to constant:

$$Ttotal = N * T$$

(Equation 2.5)

Where:

Ttotal = total test duration = total power-on Hours.

N = number of units being tested.

T = actual test duration = power-on hours per unit

This assumption of a constant failure rate has a very important consequence. It means for example, that instead of testing 1 unit for 1000 hours it is possible to test 10 units for 100 hours and make the same statements about MTTF etc.

It is customary when quoting failure rates/ MTTFs for a product to also give an associated confidence level. This is an indication of how accurate the MTTF figure is. i.e. the confidence levels give an indication of the uncertainty associated with the figure quoted for the MTTF. If an MTTF is stated with a confidence of 60% then this is equivalent to saying that 60% of the time the MTTF will lie within what is known as the confidence interval, a range of values surrounding the MTTF.

The Chi-Square equation relates the number of units being tested to the confidence figure, the test duration and the failure rate.

$$\tau = [\text{chi-square}(a, 2n+2)]/(2*N*T) \qquad \text{(Equation 2.6)}$$

where: τ = failure rate per power-on hour (P.O.H)

chi-square refers to chi-square distribution

1-a = Confidence level

2n+2 = Degrees of Freedom for Chi-Square

n = Number of fails during the test.

T = Test Duration in P.O.H.

N = Number of units tested.

The Chi-Square distribution gives a numerical value for each combination of confidence level and failures. A table of these values, such as that in Figure 2.3, can be found in most statistical and reliability texts. In certain cases the actual confidence level percentages or fractions are used for each column, in other cases (1-confidence level) is quoted. It is important to establish which is the case for individual tables.

Chi-Square Values

Number of Failures	Degrees of Freedom	Fractional Confidence Levels 0.5	0.6	0.7	0.8	0.9	0.95
		% Confidence Levels 50%	60%	70%	80%	90%	95%
0	1	0.455	0.708	1.07	1.64	2.71	3.84
	2	1.390	1.830	2.41	3.22	4.61	5.99
1	3	2.370	2.950	3.67	4.64	6.25	7.81
	4	3.360	4.040	4.88	5.99	7.78	9.49
2	5	4.350	5.130	6.06	7.29	9.24	11.10
	6	5.350	6.210	7.23	8.56	10.60	12.60
3	7	6.350	7.280	8.38	9.80	12.00	14.10
	8	7.340	8.350	9.52	11.00	13.40	15.50
4	9	8.340	9.410	10.70	12.20	14.70	16.90
	10	9.340	10.500	11.80	13.40	16.00	18.30
5	11	10.300	11.500	12.90	14.60	17.30	19.70
	12	11.300	12.600	14.00	15.80	18.50	21.00
6	13	12.300	13.600	15.10	17.00	19.80	22.40
	14	13.300	14.700	16.20	18.20	21.10	23.70
7	15	14.300	15.700	17.30	19.30	22.30	25.00
	16	15.300	16.800	18.40	20.50	23.50	26.30
8	17	16.300	17.800	19.50	21.60	24.80	27.60
	18	17.300	18.900	20.60	22.80	26.00	28.90
9	19	18.300	19.900	21.70	23.90	27.20	30.10
	20	19.300	21.000	22.80	25.00	28.40	31.40
10	21	20.300	22.000	23.90	26.20	29.60	32.70
	22	21.300	23.000	24.90	27.30	30.80	33.90
11	23	22.300	24.100	26.00	28.40	32.00	35.20
	24	23.300	25.100	27.10	29.60	33.20	36.40

Figure 2.3
Chi-Square Values

Instead of looking along the row for the actual number of failures, it is necessary to check the row for the corresponding degrees of freedom (D.O.F) using the relationship:

$$D.O.F. = 2(n+1)$$

(Equation 2.7)

Where n = number of actual failures

Note that n+1 is used instead of n because it is customary to assume the worst case i.e. if the test had gone on any longer another failure would have occurred immediately.

Figure 2.4 lists the various ways in which failure rate figures can appear and indicates how one converts a failure rate given in one form into the equivalent figure in another form.

Failure Rate Conversion Factors

Failure Rate (%/K)	=	F.R. * 10E+05
Failure Rate (PPM/K)	=	F.R. * 10E+09
Failure Rate (PPB/K)	=	F.R. * 10E+12

Key

F.R. = Base Failure Rate = 1/MTTF

%/K = Percentage failures per 1000 Hours*

PPM/K = Parts per million failing per 1000 hours

PPB/K = Parts per billion failing per 1000 hours

FITS = PPM/K

MTTF = Mean Time to Failure

*1000 hours of test

Figure 2.4
Failure Rate Conversion Factors

Sample Calculation

Target: To calculate the time required to verify a failure rate of 0.2% per 1000 hours, with zero failures, 60% confidence and a population of 100 units.

From Figure 2.3 the chi-square value for this combination is 1.83.

The failure rate/P.O.H (F.R.) is 0.02/100000 = 2E-07

$$T = \frac{\text{Chi-square (2,60)}}{(F.R * N * 2)} = \frac{(1.83)}{(2E\text{-}06 * 100 * 2)} = 4575 \text{ hours}$$

4575 hours = 190 days. (Approximately 6 months)

Section 2.4:Accelerated Testing

The purpose of accelerated testing is to enable manufacturers to shorten the time required to test the MTTF of their products. This is achieved by subjecting the items being tested to stress levels higher than those they would experience while being used normally. e.g. if a resistor has a temperature of 30°C under normal use conditions then it could be tested at 50°C by placing it in an oven . Other parameters which could be raised include the voltage across a device and the current through it.

It is also possible to subject the products to stresses which change over a set period of time. e.g. The oven mentioned above could have a cycle which included higher and lower temperatures than a device would normally experience. A number of equations exist[5] which relate the failure rate at one level of stress to the failure rate at another. This allows failure data from units which are operated at a higher than normal stress to be used when calculating the MTTF of units operating at the levels of stress they would experience when being used normally.

N.B. Those stresses which are applied to a product for this purpose are known as Accelerating Stresses because they accelerate the life of the products subjected to them.

The failure rates at the two stress levels are related by:

F.R.(high stress) = A.F. * F.R.(Normal Stress)

(Equation 2.8)

Where F.R. stands for failure rate and A.F. for the value of acceleration caused by the stress used. This value is referred to as the Acceleration Factor.

Probably the most commonly used of these equations is the Arrhenius Equation, as given by Jensen[5], which relates the MTTF/Failure Rate at one temperature to the MTTF/Failure Rate at another:

$$t = A \exp[Ea/kT]$$

(Equation 2.9)

Where: t = time to failure (Hours)

A = a constant relating to the cause of failure

Ea = activation energy i.e. The energy required to cause failure (e.v.)

k = Boltzmann's constant.

T = absolute temperature (K)

The Arrhenius equation is used in conjunction with failures caused by chemical processes which can include corrosion, evaporation etc.

The Arrhenius acceleration factor[5], $K_{Arrhenius}$, is calculated by dividing t_{low}, the time to failure at operating temperature (T_{low}), by t_{high}, the time to failure at high temperature (T_{high}) Therefore:

$$K_{Arrhenius} = t_{low}/t_{high} = \exp(Ea/k)((1/T_{low}) - (1/T_{high}))$$

(Equation 2.10)

The other symbols are as defined above.

This value of acceleration factor can then be used to relate the failure rates, as in Equation 2.8, using the fact that.

$$F.R.(Tlow) = F.R.(THigh)/K_{arrhenius}$$

The consequence of the above equations is that the Chi-square Equation can be applied to the results of a test carried out at high temperature to reveal the failure rate at that temperature. This failure rate can then be divided by the relevant acceleration factor yielding the true failure rate i.e. that which would occur in the field. Figure 2.5 shows a program which carries out all of the above process.

There are documented equations[6] for the other types of accelerating stresses which perform the same function for those stresses as the Arrhenius equation does for temperature stress.

```
10 'program to calculate actual failure rates
20 'based on Arrhenius
25 'COLLECT CHI-SQUARE DATA
30 DIM CHISQ(10,10)
40 FOR FAILS= 1 TO 10
50 FOR LEVEL = 1 TO 10
60 READ X
70 CHISQ(FAILS,LEVEL)=X
80 NEXT LEVEL
90 NEXT FAILS
95 COLOR 14,1
100 CLS
110 LOCATE 5,5: PRINT "Please Enter the desired confidence Level"
115 LOCATE 6,5:PRINT "(CHOOSE FROM 10,20,30,40,50,60,70,80,90,95)"
120 LOCATE 7,5:INPUT "(Type the NUMBER and 'RETURN')";CONF%
130 LOCATE 10,5: INPUT "Please enter the number of failures which ocurred"; DEAD
%
140 LOCATE 15,5: INPUT "Please enter the Total number of units on test ";POPLN%
150 LOCATE 20,5: INPUT "Please enter the Test Duration in hours";TSTTM%
200 IF CONF%=95 THEN CONF%=CONF%+5
210 ALPHA=INT(CONF%/10):FREE=DEAD%+1
220 UPPER=CHISQ(FREE,ALPHA)
230 ACCFAIL=UPPER/(2*POPLN%*TSTTM%)
235 COLOR 11,4
240 CLS
300 LOCATE 5,5:INPUT "Please enter the stress temperature level (°C)";TSTRESS
310 LOCATE 10,5:INPUT "Please enter the operating temperature level (°C)";TNORMA
L
320 LOCATE 15,5:INPUT "Please enter the activation energy (eV)";EACT
330 BRACKET=((1/(TNORMAL+273.15))-(1/(TSTRESS+273.15)))
340 INDPO=(EACT/8.617E-05)*BRACKET
350 ACCFACT=EXP(INDPO)
360 OPFAIL=ACCFAIL/ACCFACT
365 COLOR 7,4
366 CLS
367 COLOR  14,3
370 LOCATE 7,5:PRINT "The failure rate under stress is: ";ACCFAIL; " per POH"
375 COLOR 15,1
380 LOCATE 14,5:PRINT "The actual failure rate is: ";OPFAIL; " per POH"
385 KPOH = OPFAIL*100000!:FITS=OPFAIL*1E+09
386 COLOR 14,2
390 LOCATE 16,5:PRINT "Which corresponds to ";KPOH;"%/1000 hours"
391 COLOR 14,5
395 LOCATE 18,5:PRINT "Which corresponds to ";FITS;" FITS"
396 COLOR 4,4
400 COLOR 1,4:LOCATE 20,5:PRINT "Do you wish to do another calculation (Y/N)?"
415 A$=INKEY$:IF A$="" THEN GOTO 415
420 IF A$="Y" OR A$="y" THEN GOTO 95 ELSE GOTO 500
500 COLOR 7,0:CLS:SYSTEM
```

Figure 2.5 'Failure Rates' Program Listing (Programming Language: BASIC) (Part 1)

```
1000 DATA 0.211,0.446,0.713,0.102,1.39,1.83,2.41,3.22,4.61,5.99
1010 DATA 1.06,1.65,2.19,2.75,3.36,4.04,4.88,5.99,7.78,9.49
1020 DATA 2.2,3.07,3.83,4.57,5.35,6.21,7.23,8.56,10.6,12.6
1030 DATA 3.49,4.59,5.53,6.42,7.34,8.35,9.52,11.0,13.4,15.5
1040 DATA 4.87,6.18,7.27,8.3,9.34,10.5,11.8,13.4,16,18.3
1050 DATA 6.3,7.81,9.03,10.2,11.3,12.6,14,15.8,18.5,21
1060 DATA 7.79,9.47,10.8,12.1,13.3,14.7,16.2,18.2,21.1,23.7
1070 DATA 9.31,11.2,12.6,14,15.3,16.8,18.4,20.5,23.5,26.3
1080 DATA 10.9,12.9,14.4,15.9,17.3,18.9,20.6,22.8,26,28.9
1090 DATA 12.4,14.6,16.3,17.8,19.3,21,22.8,25,28.4,31.4
```

Figure 2.5
'Failure Rates' Program Listing (part 2)

Voltage Acceleration Factor[6]

$$K_{voltage} = \frac{\text{Voltage during Stress Test}}{\text{Voltage when in use}}$$

(Equation 2.11)

Humidity Acceleration Factor

$$K_{humidity} = \exp(0.00044)(Rh_{stress}^2 - Rh_{use}^2)$$

(Equation 2.12)

Where: Rh_{stress} = % Stress Level of relative humidity

R_{huse} = % Normal/Use level of relative humidity

(This is known as the 'Sim-Larson' Equation)[6]

Temperature Cycling

In the course of the project two possible equations have been found for an acceleraion factor for thermal cycling. The first of these is the Modified Coffin-Manson Equation[6]

$$K_{Thcyc} \ (dTs/dTf)^{1.9} * (Ff/Fs)^{0.333} * \exp(0.01*(Ts-Tf))$$

(Equation 2.13)

Where:

dTs = Temperature Range of Laboratory Stress cycle

dTf = Temperature Range in Field

Ff = Cycle Frequency in Laboratory

Fs = Cycle frequency in Field

Ts = Max Temperature of Laboratory Cycle

Tf = Max Temperature of Field cycle

The Thermal cycling test is the main test for checking solder joints and is a standard part of the burn-in process along with vibration testing.

Another possible equation for thermal cycling was that proposed by Nachlas[7] based on a cycle such as that in Figure 3.6 which includes separate integrated factors for the high temperature section and the ramps and has the form:

$$A.F. = \frac{1}{t_3} \int_0^{t3} [\exp\{[EaT(t)/K][(1/To)-1/T(t)]-\phi\{DT(t)/dt\}]$$

(Equation 2.13)

Where ϕ is a constant relating to the ramp stress and DT(t)/dt is the ramp rate of change of temperature.

To = temperature at the start of the temperature ramp

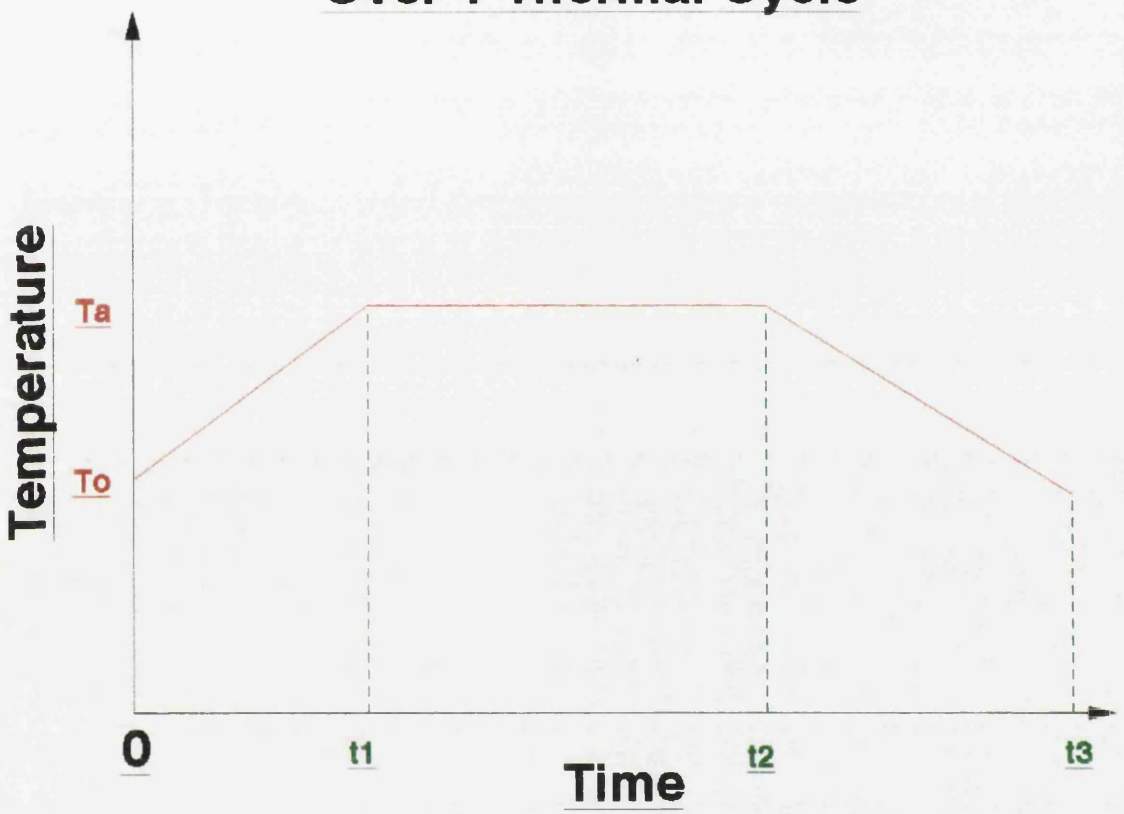
T(t) = temperature at time t

Ea = activation energy

K = Boltzmann's Constant

DT(t)/dt = rate of change of temperature at time t.

Temperature v Time
Over 1 Thermal Cycle



To = Nominal Operating Temperature

Ta = Temperature During High Temperature Dwell

Figure 2.6

Typical Thermal Cycling Test Profile

Section 2.5:Activation Energy

Several of the equations above, in which the accelerating stress is temperature based, make reference to what is known as the Activation Energy i.e. the energy required to initiate the process which causes failure.

Obviously different processes have different activation energies this means that one must talk about the activation energy of a process rather than that of a component which could have a number of chemical processes associated with it. e.g. One quotes the activation energy of corrosion of a capacitors leads rather than the activation energy of a capacitor which could also fail, in the case of an electrolytic capacitor, through evaporation of the electrolyte. This is a different process with a different activation energy.

In order to arrive at a value for activation energy for a process it would be necessary to compare failure rates at different temperatures but with the same failure mechanism.

It is for this reason that stress levels have to be carefully controlled. There is nothing to be gained in placing the samples in a temperature of 200°C if they fail due to a process which could never have occurred in the range of temperatures they would be expected to deal with when in normal use. It is even possible that if a very high temperature causes one such unrealistic failure mode to manifest itself in a relatively short period this could hide a failure mode which happens at operating stress but had not yet caused failure at the higher stress. When an activation energy is quoted for a component it will be the activation energy of the most likely cause of failure.

In the case of electronic assemblies which contain a multitude of different components with various failure modes it is not always possible to know the relevant activation energy in advance. This is especially true when dealing with a wide variety of different samples. (a range of power supplies from a variety of manufacturers are tested in the laboratory. The MTTF's are so large that it would be impractical to derive an activation energy using the method described above.

It is important to point out that a power supply will fail because one or more components fail. Apart from electrolytic capacitors which can dry out components fail for one of two reasons:

(1) The component is faulty. (The fault may take years to cause failure)
(2) The component is overstressed (The wrong component has been used for a particular application. i.e. failure is due to a design fault.)

When dealing with electronic assemblies it is common practice to work with an average activation energy. The value used in the laboratory is 0.6 eV which emerged from work done by another laboratory , namely the Product Quality and Reliability Laboratory, on electronic assemblies. Values commonly quoted for assemblies range from 0.4eV to 1.00eV. Obviously if a test was started and some failures occurred due to one process with a known activation energy that value could be substituted in place of the 0.6 eV. Jensen[5] suggests 0.4eV and some manufacturers prefer this more pessimistic value.

Section 2.6:Alternative Means of Reliability Assessment.

Another means of arriving at an MTTF for a device is by working out a weighted average based on the number of each type of component and the activation energy of the failure mode usually associated with that component.

Many companies, instead of checking assembly reliability by means of life testing, use the published failure rates for each component, muliplied by the number of components of that type, to arrive at an overall failure rate for that component. All of these failure rates are then added together to give a failure rate for the complete assembly.

The above approach is that documented in Mil-Hdbk 217[8], a system developed to give reliability guidance for usage of components in military equipment from the point of view of maintainance and spares. The main problem with this system is that the published failure rates are not always accurate and this inaccuracy increases during the multiplication process. Additionally, the failure rates are quoted for particular levels of voltage, temperature etc. so in order to use them in a real situation the actual values of voltage and temperature would have to be measured and the failure rates adjusted accordingly. In a complicated device this could prove impractically time consuming. However one of the main advantages of this Mil-Hdbk method is that it allows manufacturers to compare like with like and, in the event of field failure, gives an indication of which component is most likely to have failed. This knowledge can lead to a reduction in repair time.

Manufacturers now tend to prefer life testing for reliability verification. Not only is it a practical test of the actual products involved it can also reveal potential problem areas. For example if a component fails during a life test at a temperature only slightly above that at which it is expected to operate then that component is one that could cause problems in the field and the manufacturer would be wise to replace it with a component which gives a wider safety margin for the particular application involved.

Perhaps the essence of Reliability and Life Testing is best captured in that statement from Dummer and Winton[4] which reads "Very often the goal is to show that a device is reliable enough to meet some mission requirement; this is somewhat different from needing to know, with maximum precision, the device reliability."

Chapter 3-The Effect of Elevated Ambient Temperatures

Section 3.1: Current Laboratory Practice

The method currently used for testing S-MPS in the Engineering Laboratory at IBM consists of running the power supplies for three months in an environment where the air temperature is 60°C i.e. the power supplies are operated in a 60°C ambient. In normal use the power supplies would operate in a 25°C to 35°C ambient. The power supplies spend 45 minutes of each hour switched on and the other 15 minutes switched off. This cycle also ensures that the power supply can endure the requisite number of on/off cycles. The MTTF for the power supplies is* 500,000 hours at an operating temperature of 35°C.

Figure 3.1 shows how this figure is converted to calculate the time required to test 20 power supplies at 60°C.

This part of the thesis deals with the tests that were performed in an attempt to discover whether these life tests currently conducted at 60°C could be carried out at a higher ambient temperature. A higher Temperature would bring a higher acceleration factor and therefore a reduced test time.

* SPECIFIED AS

Sample Acceleration Factor Calculations

60 C Power Cycling

(Assume 60% Confidence)
Number of Units Tested = 20
MTTF = 500000 hours
Failure Rate = 2e-06
Number of Failures = 0
Chi-Square = Chi-Square(2,60%) = 1.830

$$T = \frac{\text{(Chi-Square(2,60\%)}}{\text{(F.R. * N * 2)}} = \frac{1.83}{0.00004}$$

Test Length at Ambient Temperature = 22875 hours

Arrhenius Equation

A.F. = exp{(Ea/k)((1/Tf)-(1/Ts))}

Tf = Tfield = Tlow; Ts = Tstress = Thigh

Ea = 0.6eV; k= 8.617e-05

Tfield = 35°C = 308.15K; Tstress = 60°C = 333.15K

A.F. = exp{(0.6/8.617e-05)((1/308.15)-(1/333.15))}

= exp((6963) * (2.435e-04)) = exp(1.69) = 5.42

Test Length at 60°C = 22875 hours / 5.42

Test Length at 60°C = 4220 hours = 175 days

Figure 3.1
'Normal' Power Cycling Acceleration Factor

Section 3.2

Highest Possible Operating Ambient Temperature

In order to obtain some idea of the maximum ambient temperature in which the power supplies would actually function it was decided to place four power supplies in an environmental chamber and gradually increase the ambient temperature until the power supplies stopped operating, either by shutting themselves down or by failure through actual damage.

The ambient temperature was increased in 10°C steps from 50°C. At each stage the power supply was powered on for 30 minutes. This allowed the various parts of the power supply to reach the temperature of the surroundings and ensured, in each case, that the power supply would run at that level of ambient temperature.

The power supplies operated for the full 30 minute period at temperatures of up to and including 100°C but when the temperature was increased to 110°C the power supplies shut down 5 to 10 minutes after they were switched on. A similar shut down ocurred at 105°C. This seemed to suggest that the power supplies involved would operate in temperatures of up to and including 100°C.

N.B. Although the power supplies shut down after a few minutes operation at temperatures above 100°C that shutdown was due to the power supplies' self-protection circuitry rather than being a result of damage. This is supported by the fact that the power supplies ran for an indefinite time when the ambient temperature was reduced which would not have been the case if the high temperatures had resulted in damage.

The operating specification for the 118W power supplies used demands that they operate normally in temperatures of up to 50°C. When the above test was being planned it was with a view to carrying out long term tests which would involve operating the power supplies for a prolonged period at 10°C below the maximum temperature at which they would function. At that time it was expected that the maximum temperature would be in the region of 80°C - 90°C. Since the tests documented in this thesis were being carried out with the ultimate aim of using them on a large scale it was necessary to take into account the thermal chamber which would be used if a large number of power supplies were to be tested simultaneously. Since the maximum temperature attainable by that chamber is 75°C It was decided to run the aforementioned long term tests at 75°C rather than the 90°C which was suggested by the fact that the power supplies would function in an ambient of 100°C. 75°C allowed for an adequate safety margin between the actual ambient for the test and the maximum abmbient in which the power supplies had operated.

Section 3.3:Temperatures of Individual Components

A power supply consists of a series of discrete electronic components all with different actual and maximum operating temperatures. The designer of a power supply will choose components which not only fulfill the required function for their position in the power supply but do so without exceeding their maximum rated values for voltage, current, power and temperature.

If a life test resulted in the components operating at temperatures which exceded their maximum rated values the result could be unrealistic failure modes due to components being overheated.

For this reason it was decided to measure the temperature of various components within the power supply at various values of ambient temperature and compare the operating temperatures at each value of ambient temperature.

These measurements were carried out with three main objectives in mind.

1) To discover the operating temperatures of the principal components of a S-MPS.

2) To establish the existence, or lack thereof, of a connection between the temperatures of the individual components and the ambient temperature of the power supply's operating environment.

3) To find out if it is possible to predict the maximum temperature in which the power supply can operate, without the internal components exceding their maximum temperature, by measuring the temperatures of these components while the power supply is operating at room temperature.

The components used for these checks were as follows:

The two switching FETs

The Voltage Doubling Triac

The +5V and +12V Channel Output Diodes.

(The above components are all mounted on heatsinks)

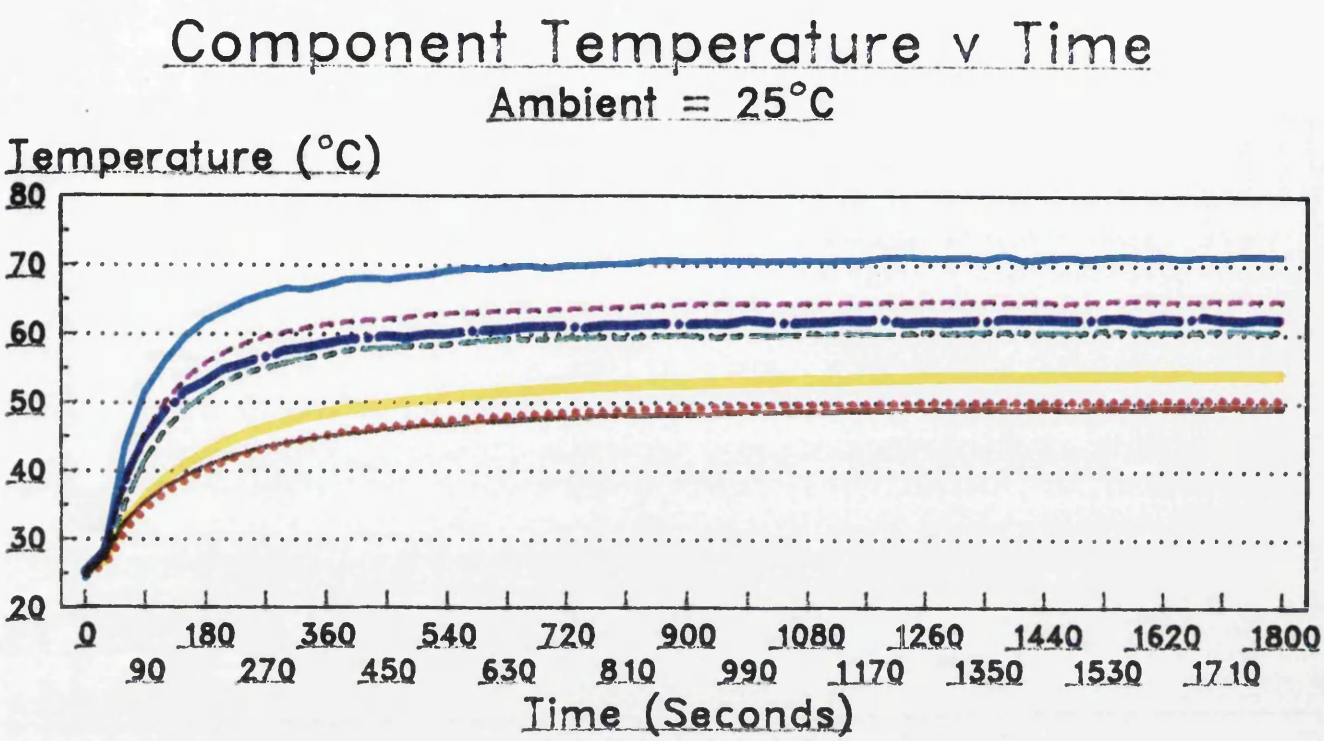
The Pulse Width Modulator chip.

One +5V channel Output/Filter Capacitor

The Air Temperature inside the power supply case.

Two power supplies were chosen and thermocouples were attached to these components in each power supply. The power supplies were switched on in an ambient temperature of 25°C ,i.e. on the bench, for 30 minutes and during this time the thermocouple outputs were stored at 30 second intervals by a data logger. The ambient temperature of the air surrounding the power supplies was logged along with the other temperatures.

These measurements were repeated in ambient temperatures of 50°C, 60°C, 75°C, 90°C and 100°C and the resultant plots of the logged thermcouple temperatures appear in Diagram 3.2.



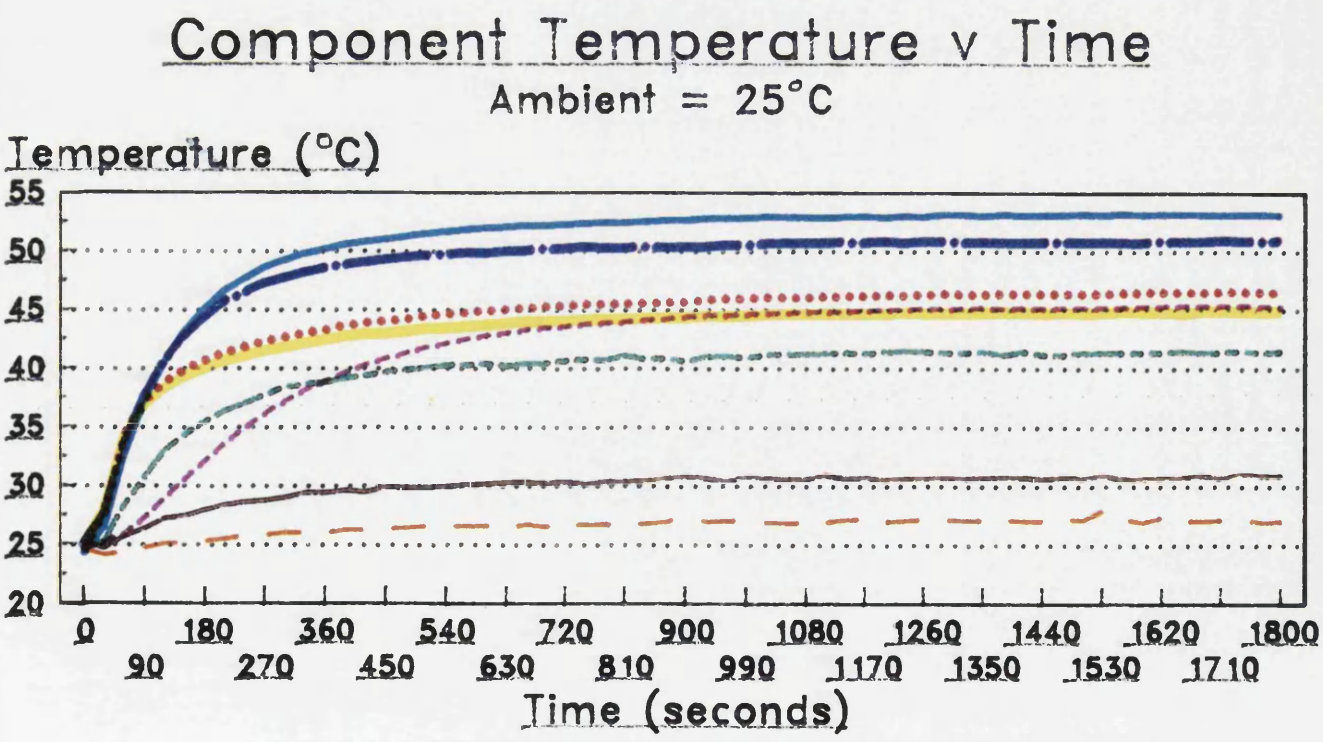
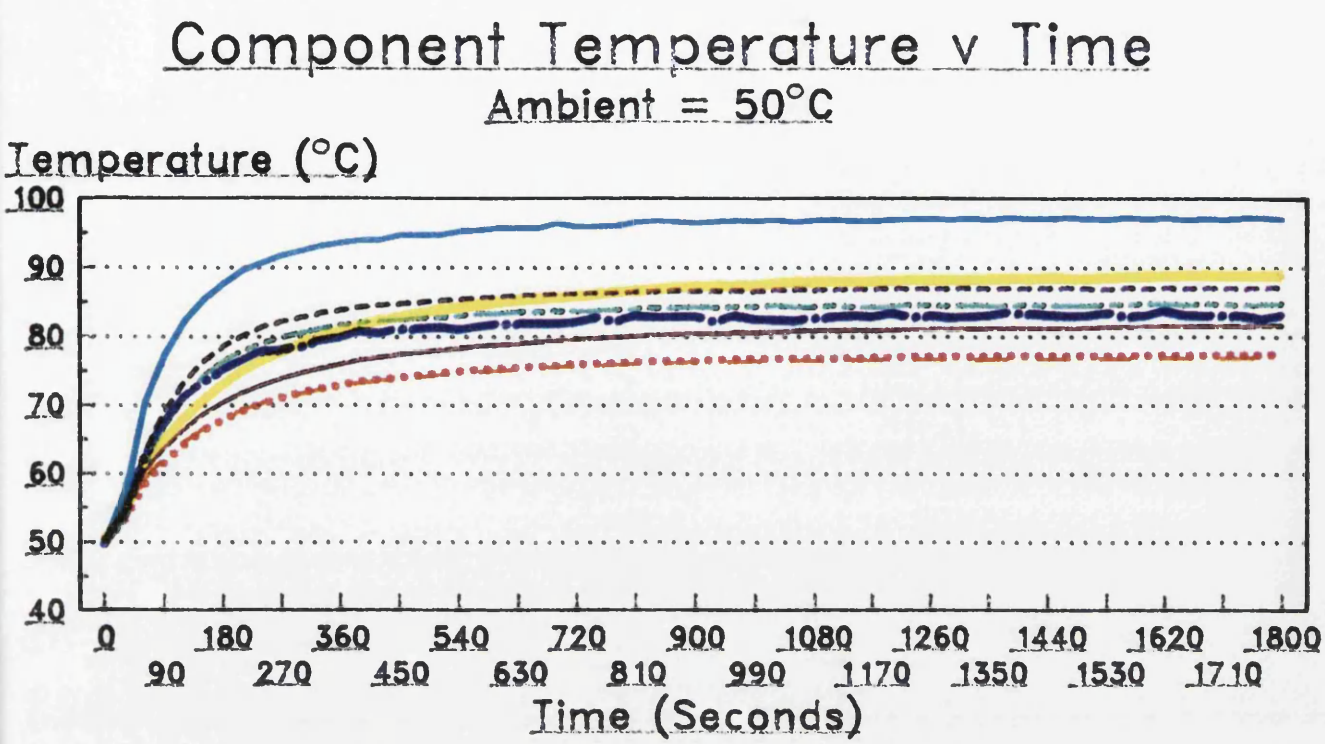


Figure 3.2
Component Temperatures At Various Ambients



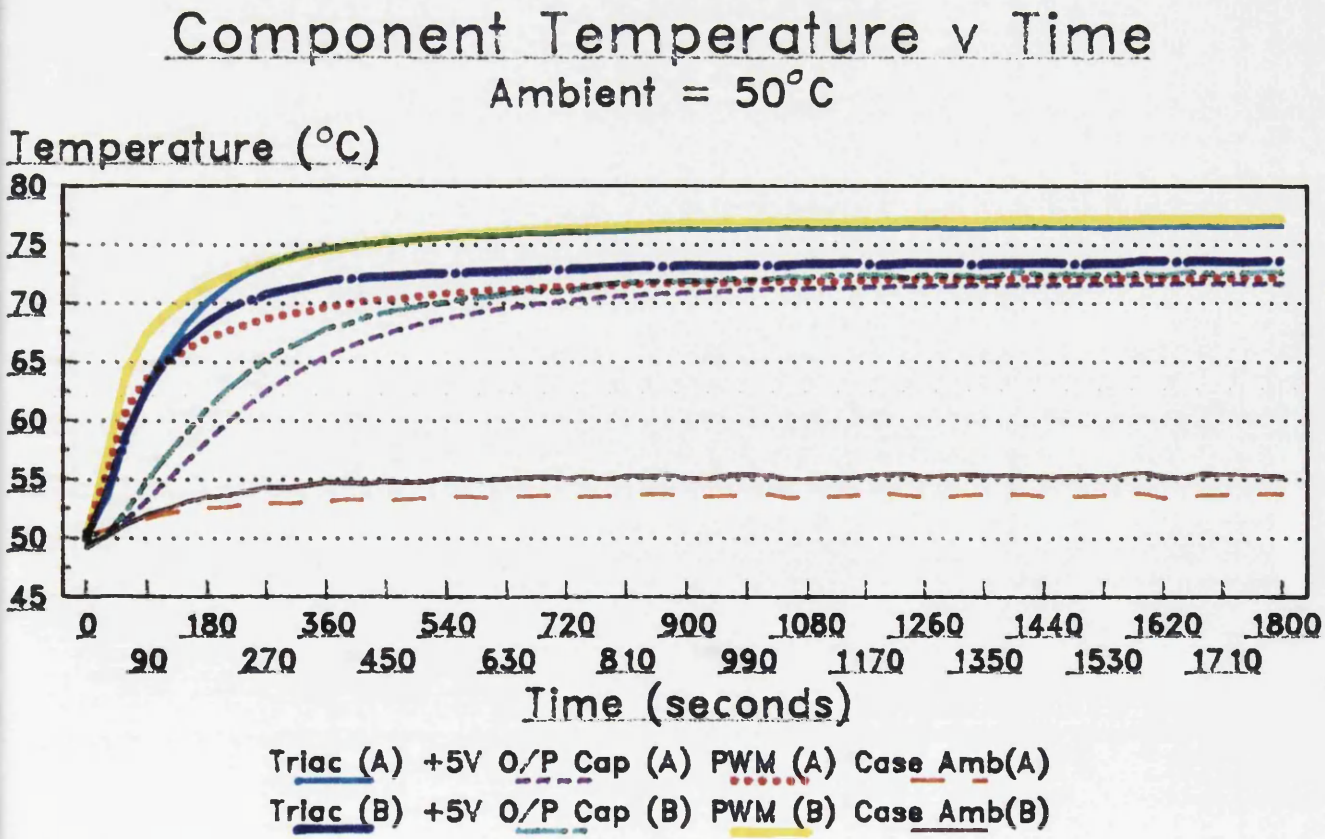
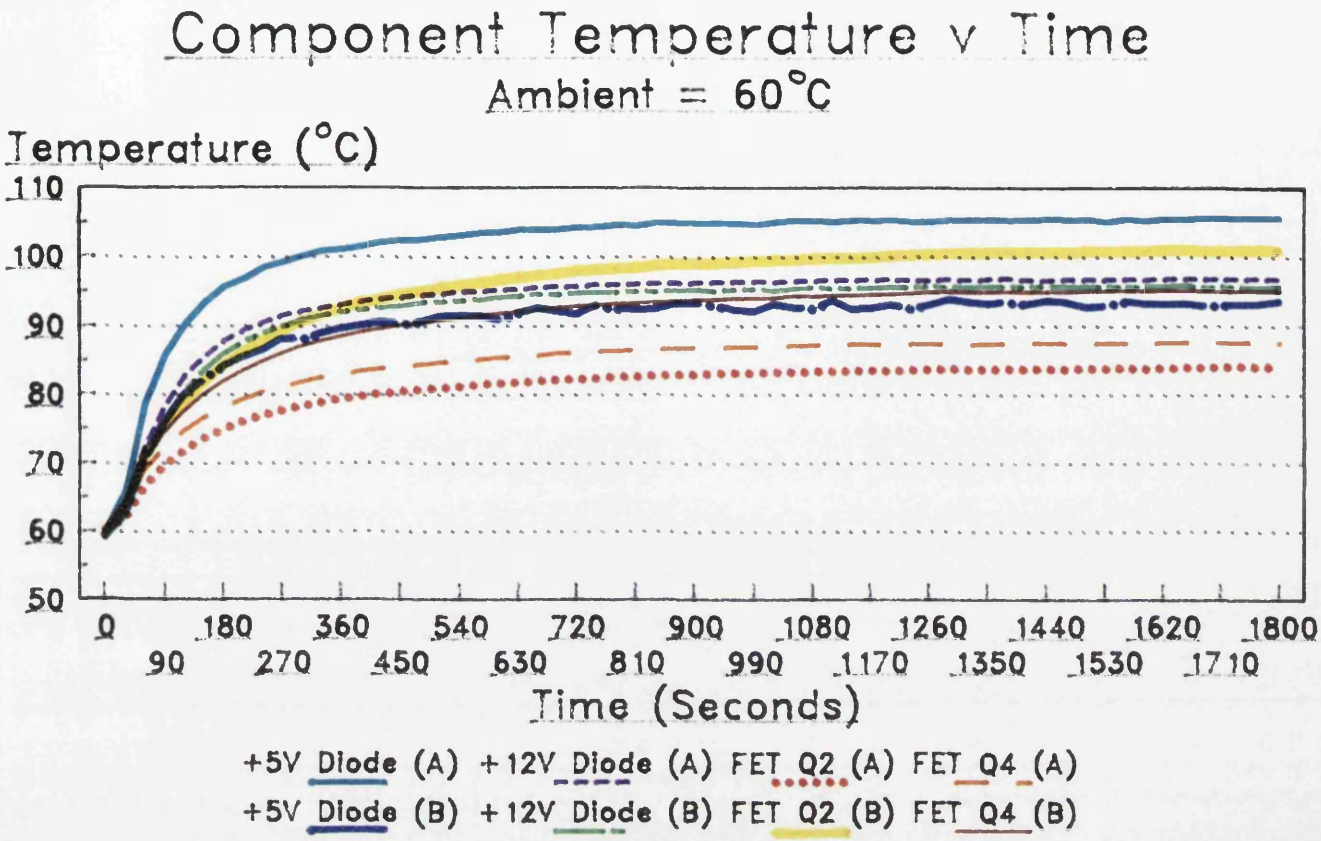
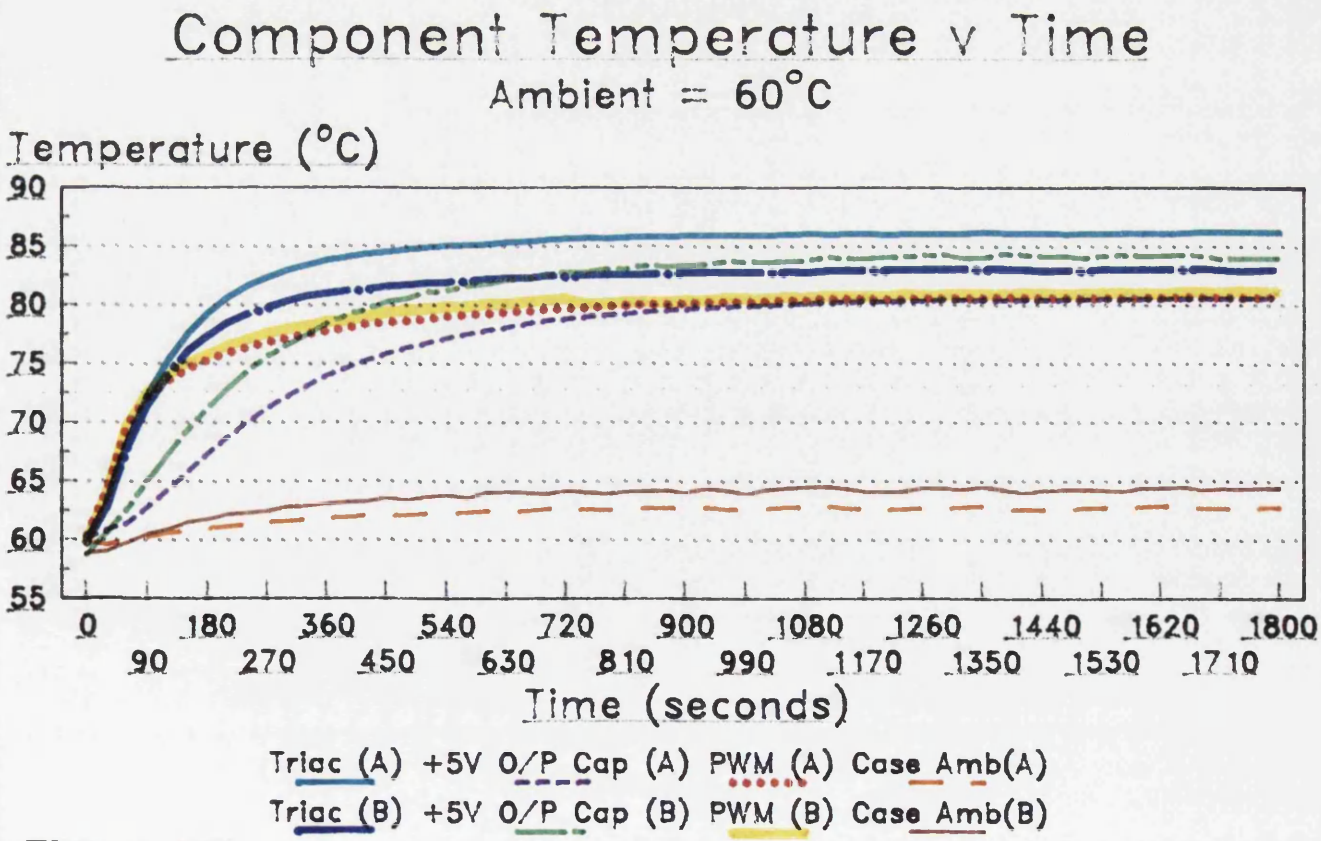


Figure 3.2
Component Temperatures At Various Ambients





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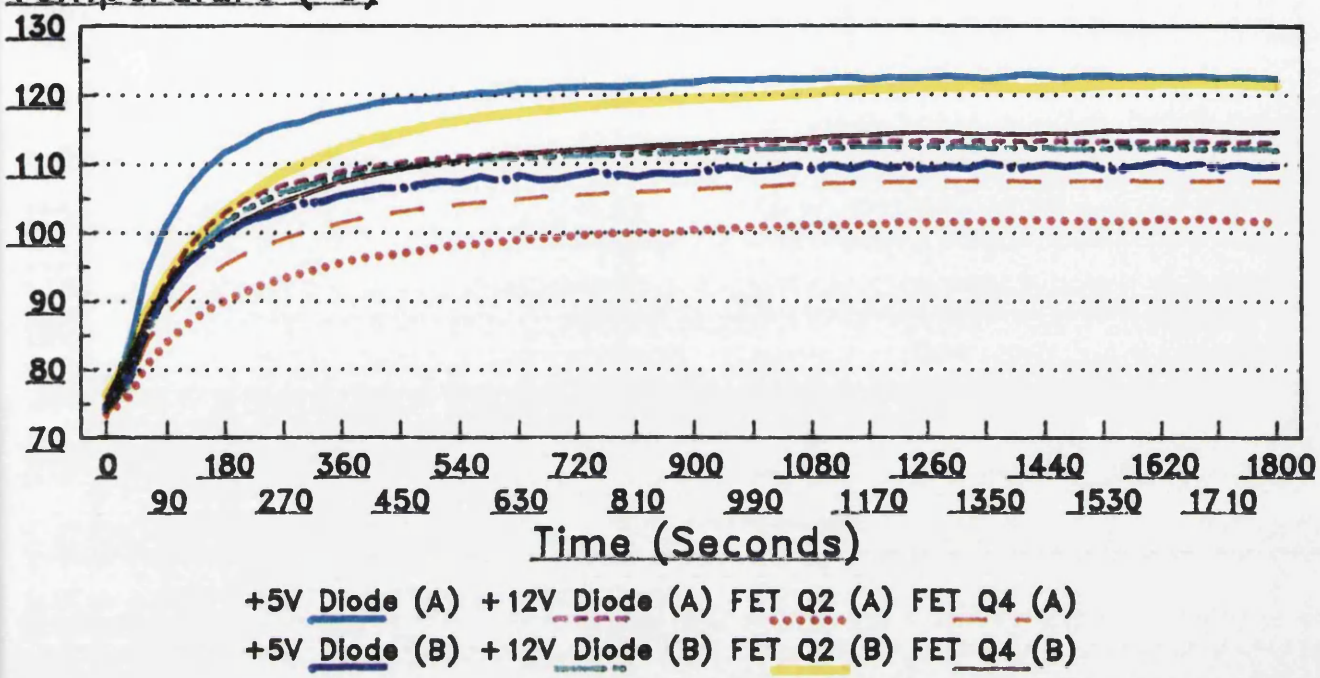
Component Temperatures At Various Ambients



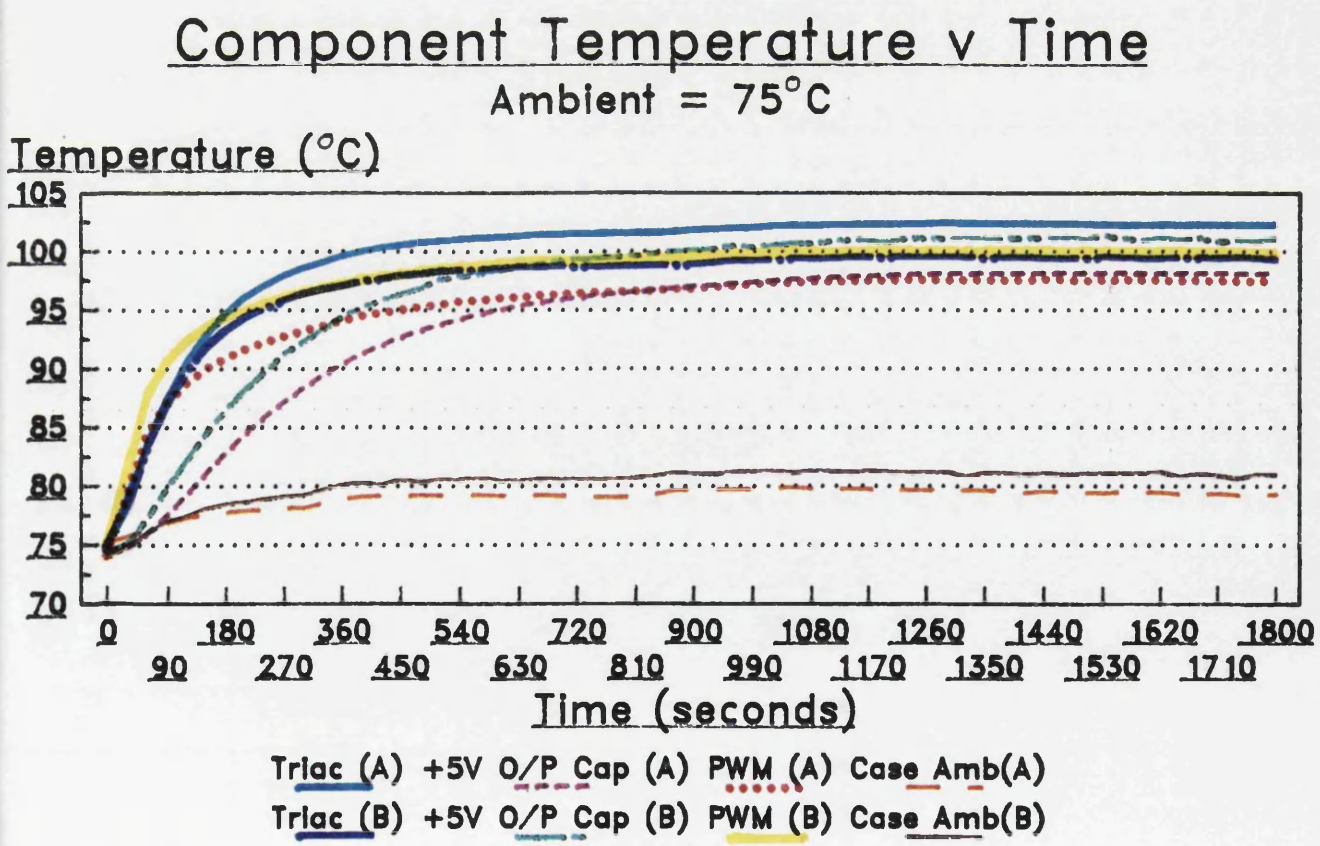
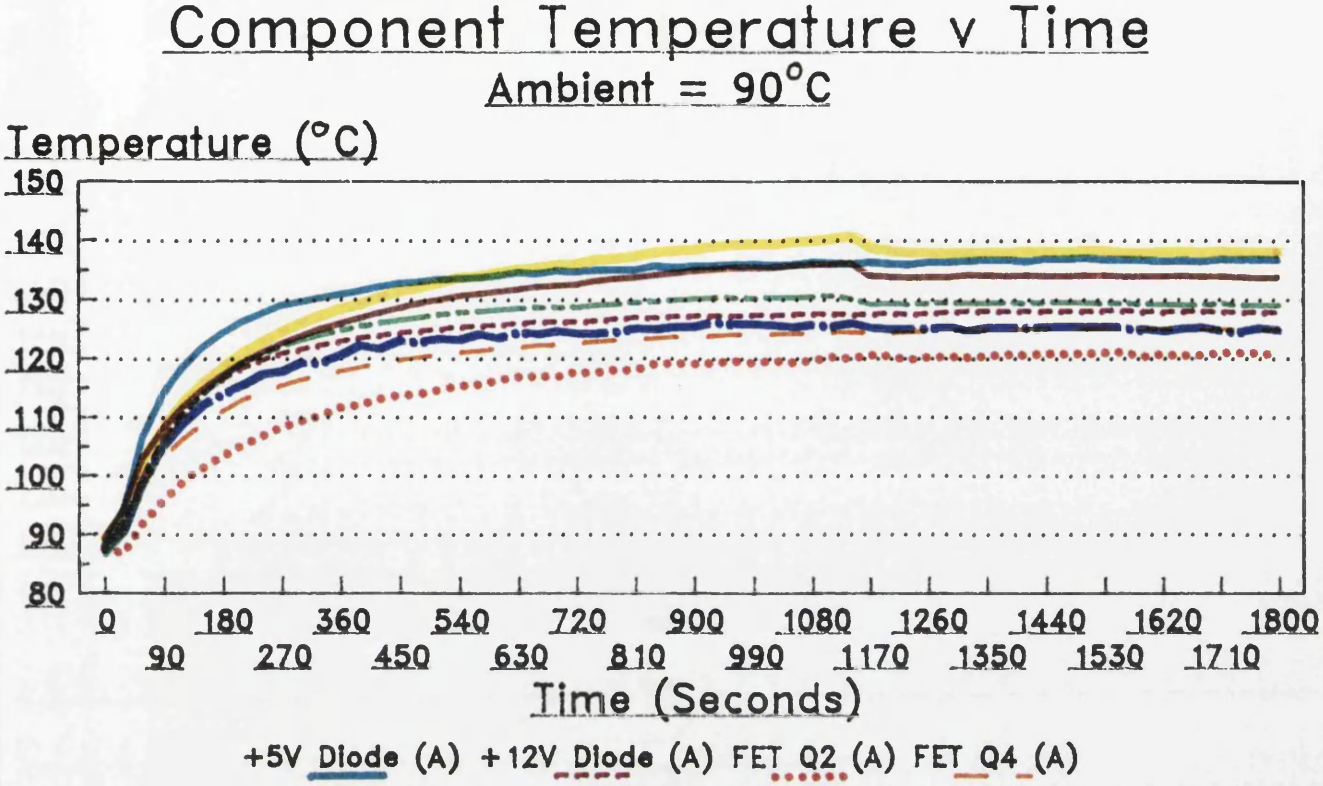


Figure 3.2
Component Temperatures At Various Ambients



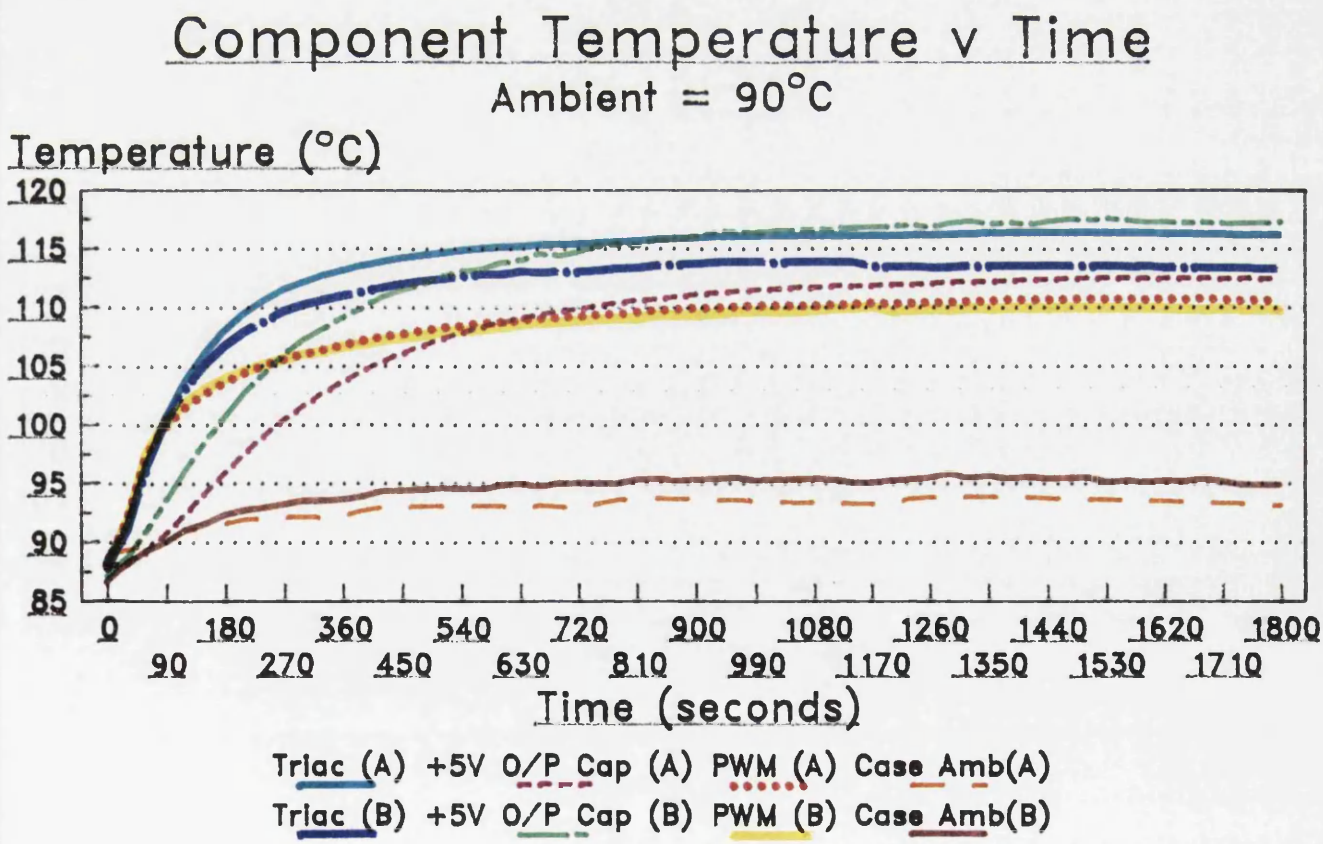


Figure 3.2
Component Temperatures At Various Ambients

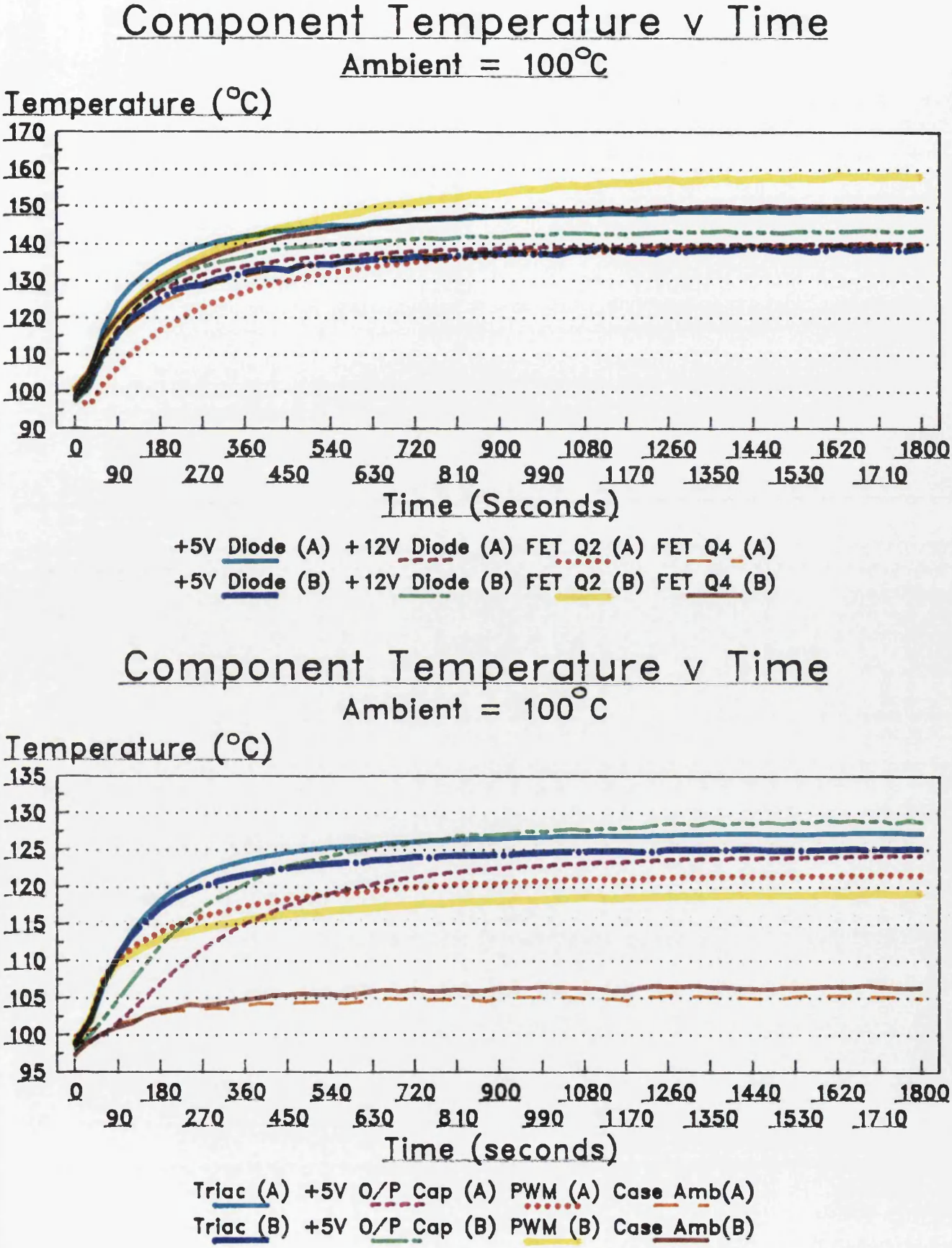
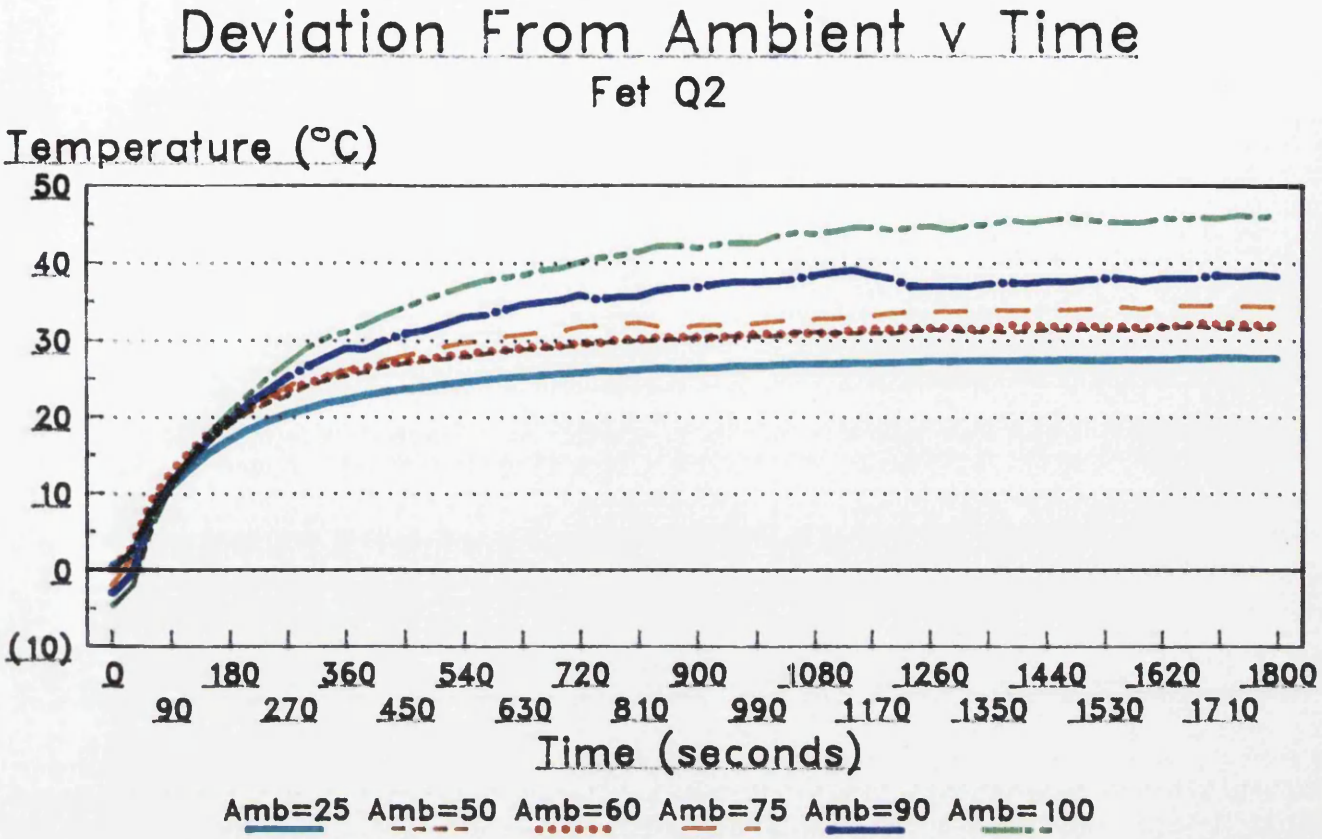


Figure 3.2
Component Temperatures At Various Ambients

Between each of the elevated temperature stages the power supply was checked for damage by measuring the regulation and ripple voltages of each output channel. This was to ensure that temperature changes were authentic and not due to component damage. The voltages of several of the power supply outputs were also logged, by the datalogger, throughout the test

In order to examine the possibility of a relationship between component temperature and ambient temperature plots were also made of average deviation of component Temperature from ambient temperature versus time. These were produced using the temperatures logged for the previous section and form the basis of Figure 3.3. The graphs indicate whether the deviation of component temperature from ambient temperature is dependent on the ambient temperature.



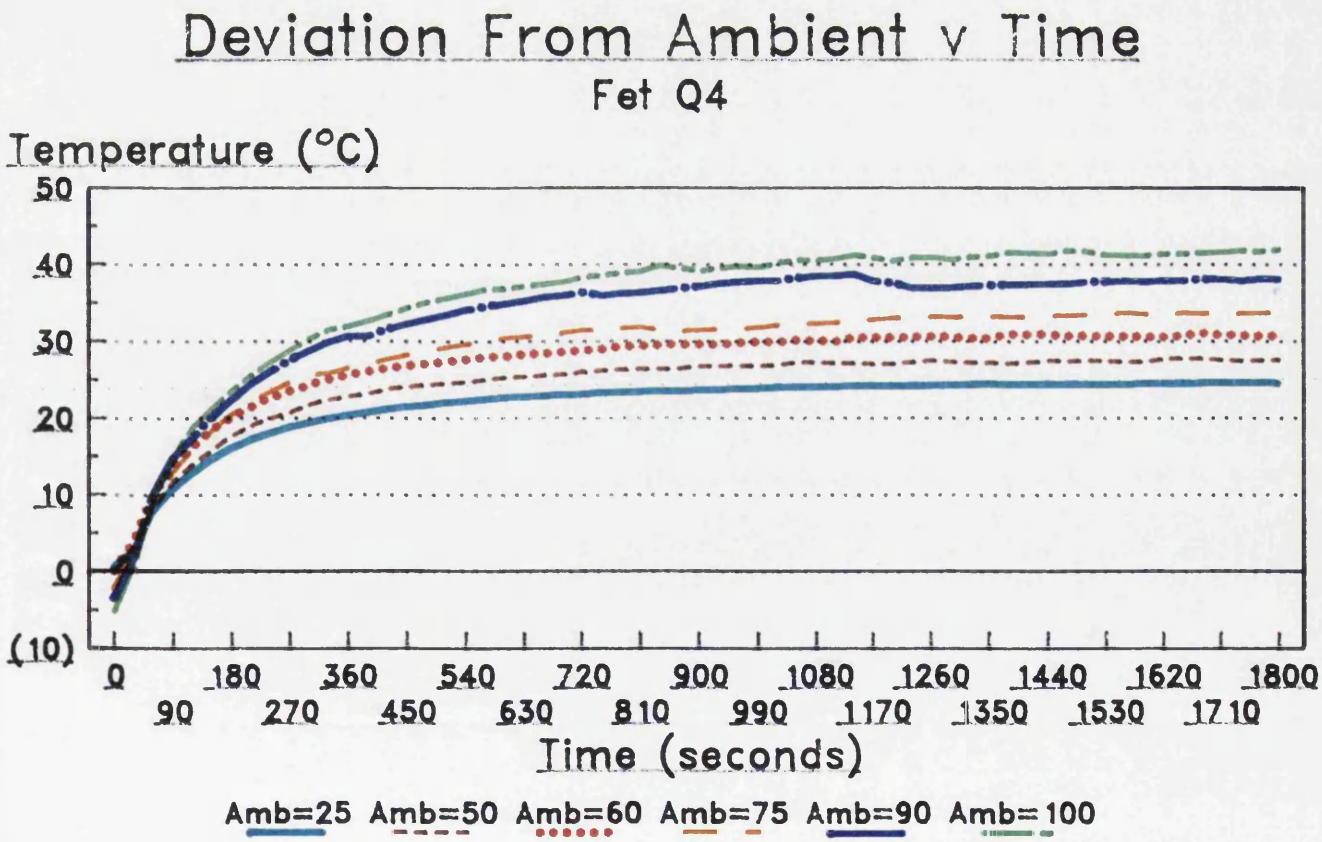
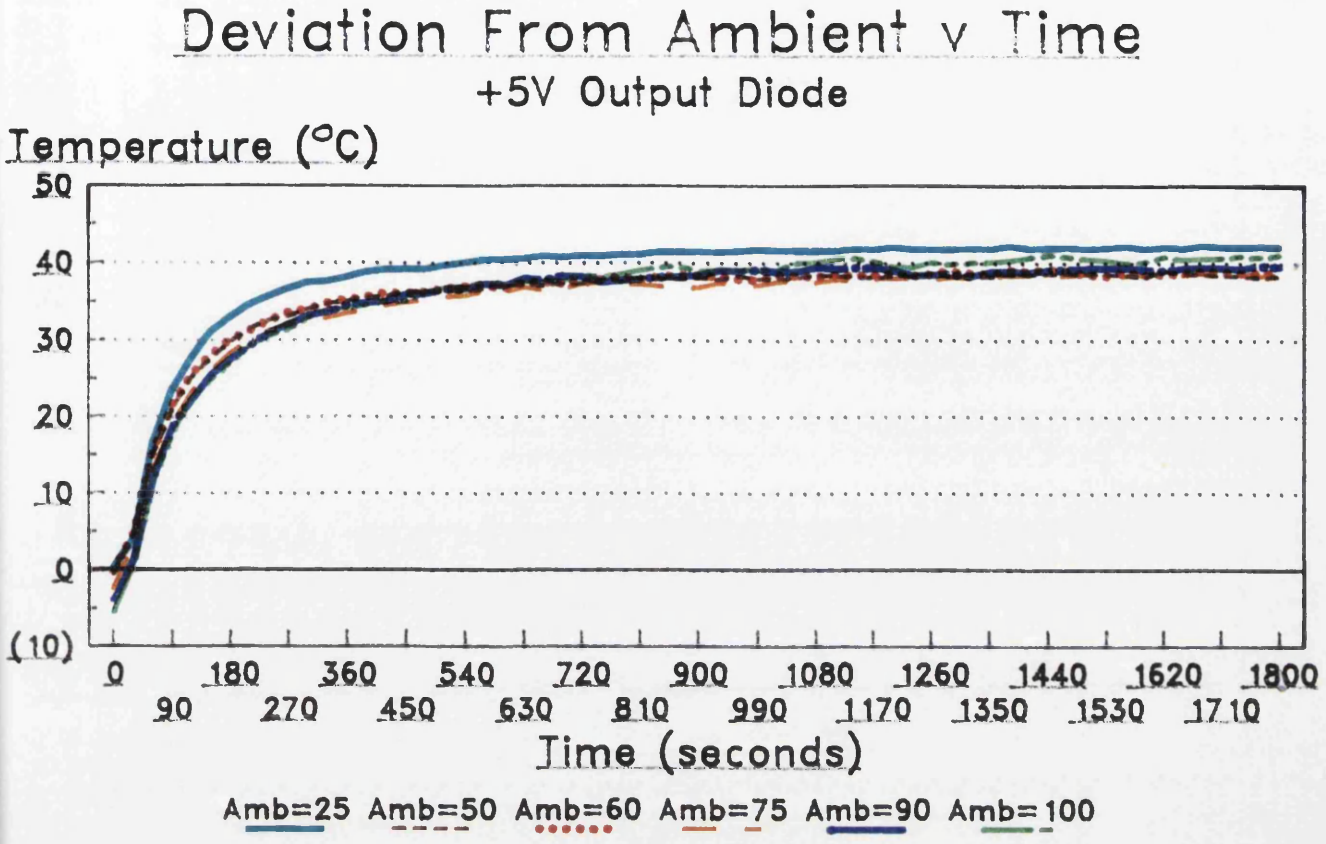


Figure 3.3
Deviation of Component Temperature From Ambient



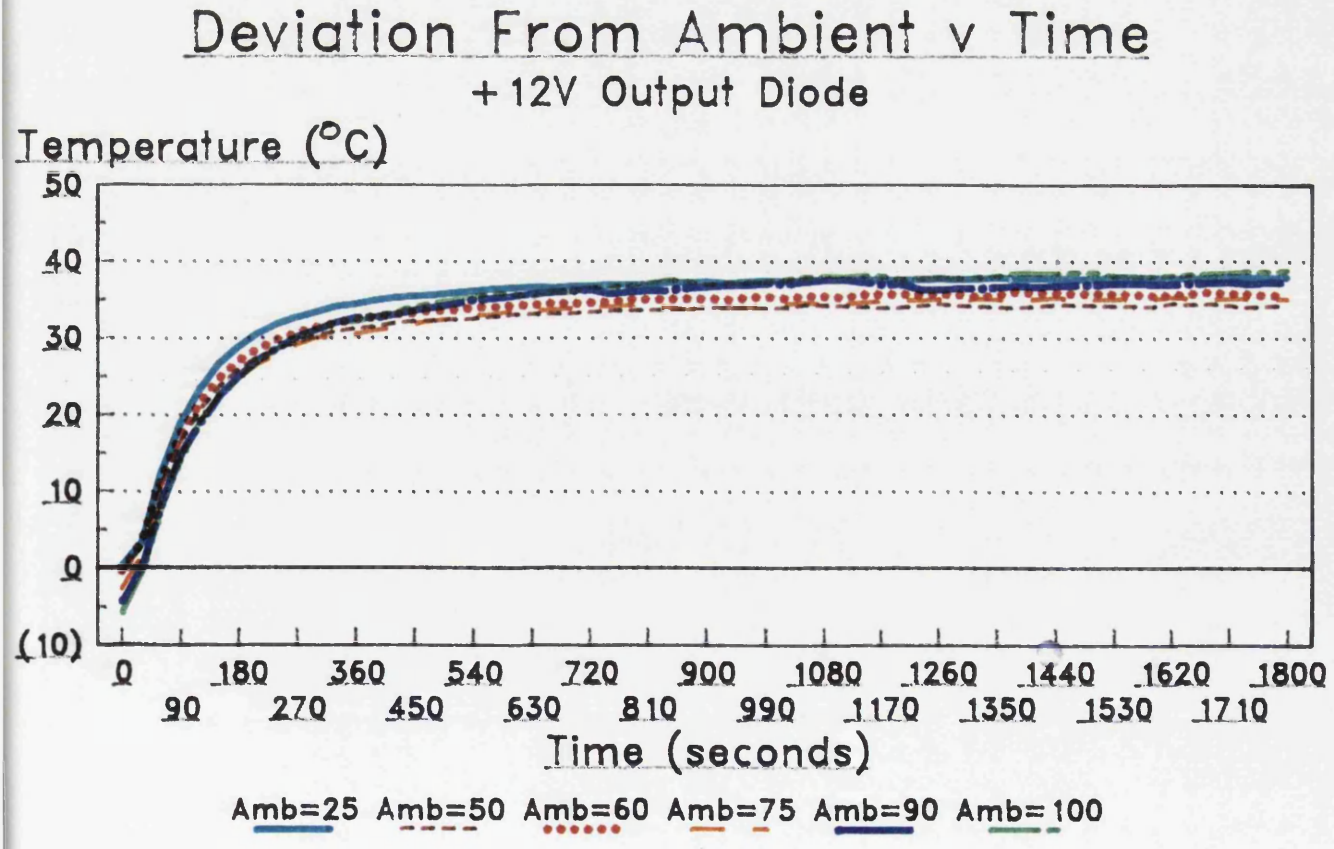
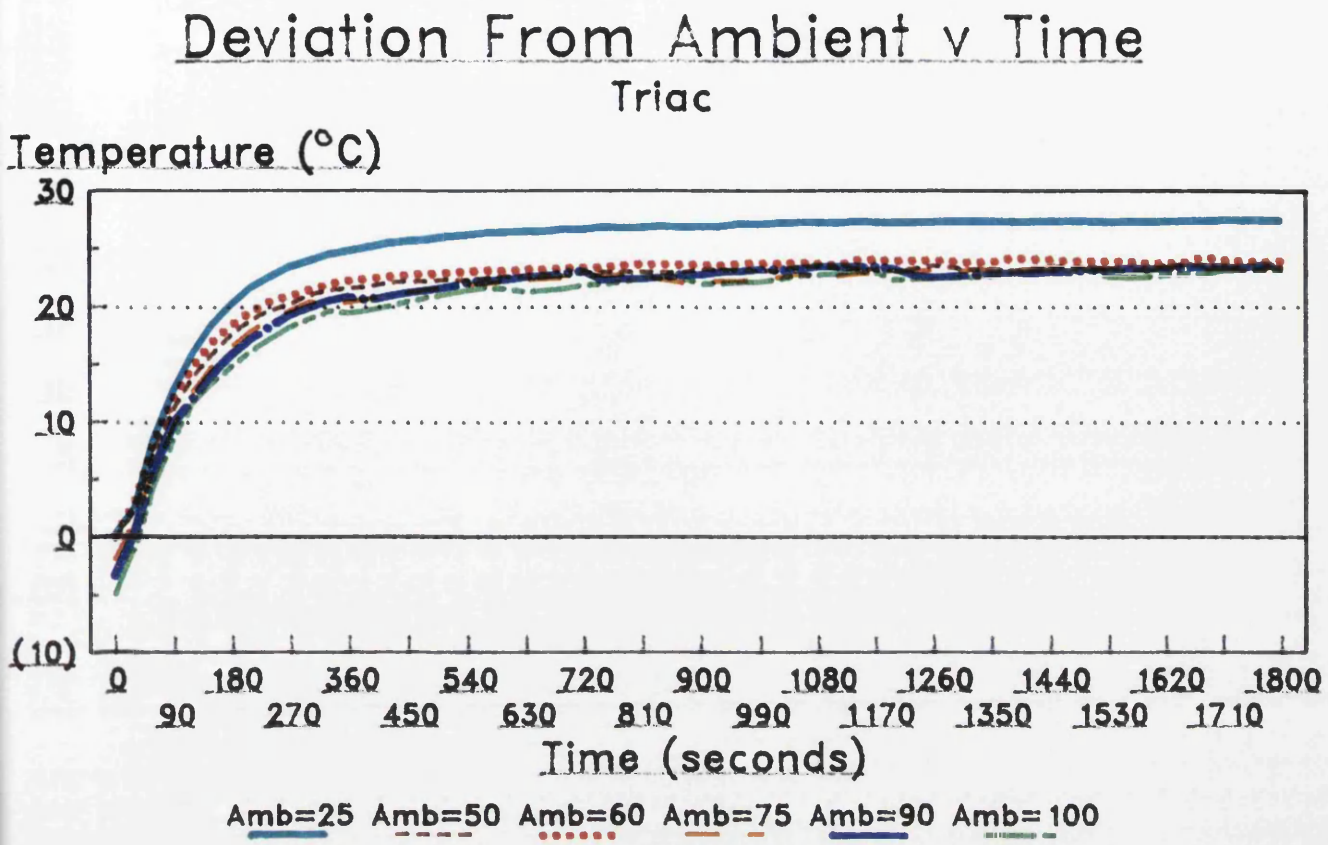


Figure 3.3
Deviation of Component Temperature From Ambient



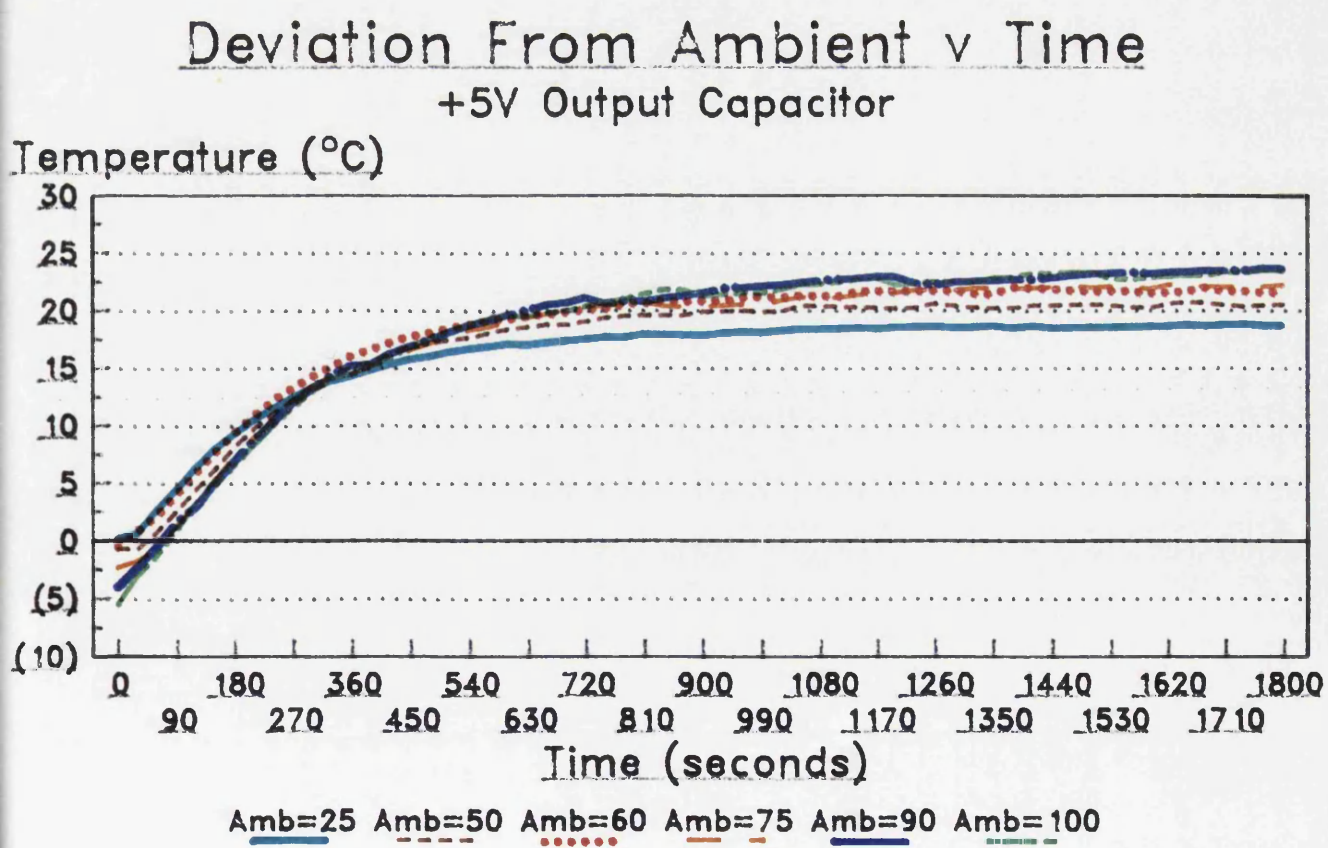


Figure 3.3
Deviation of Component Temperature From Ambient

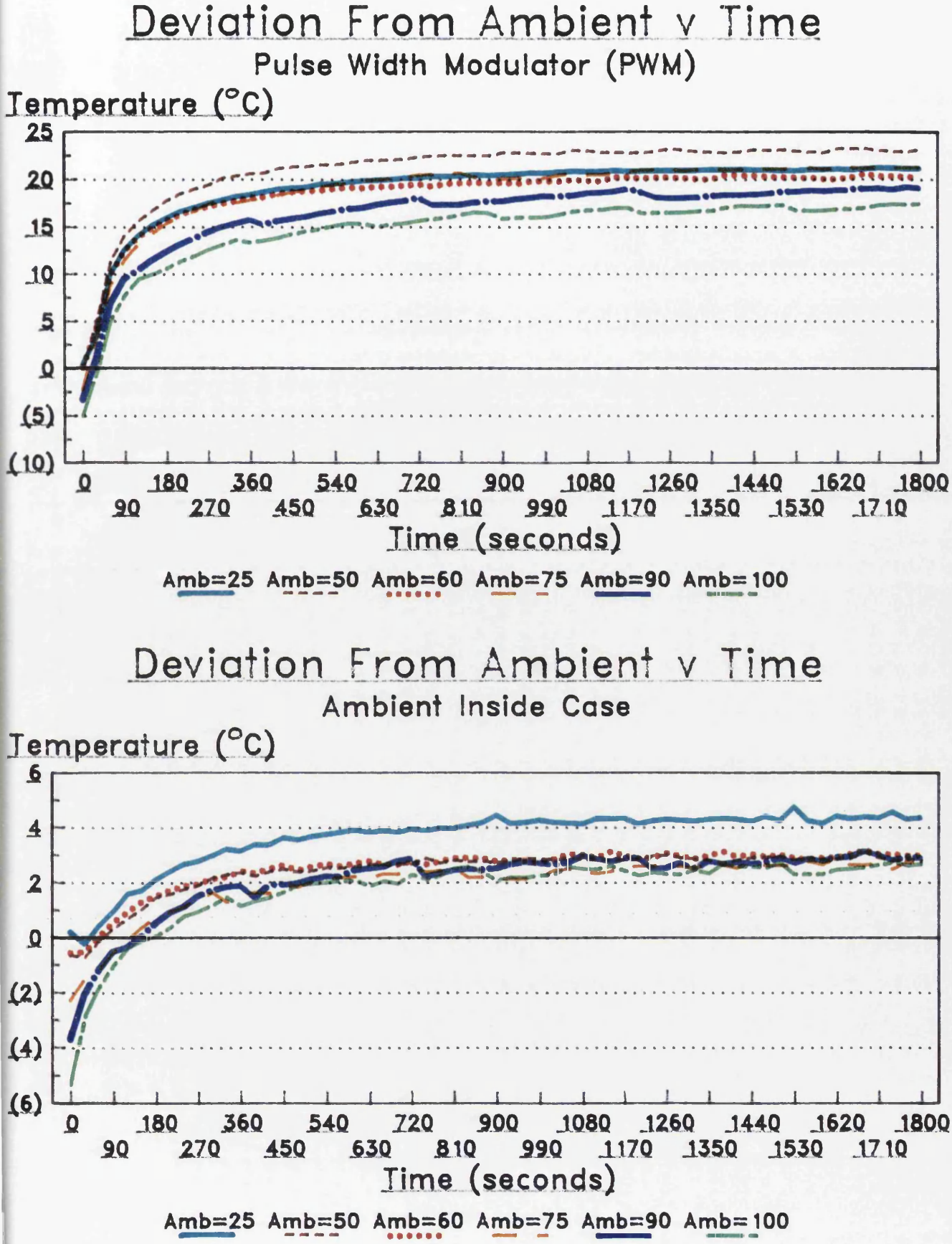


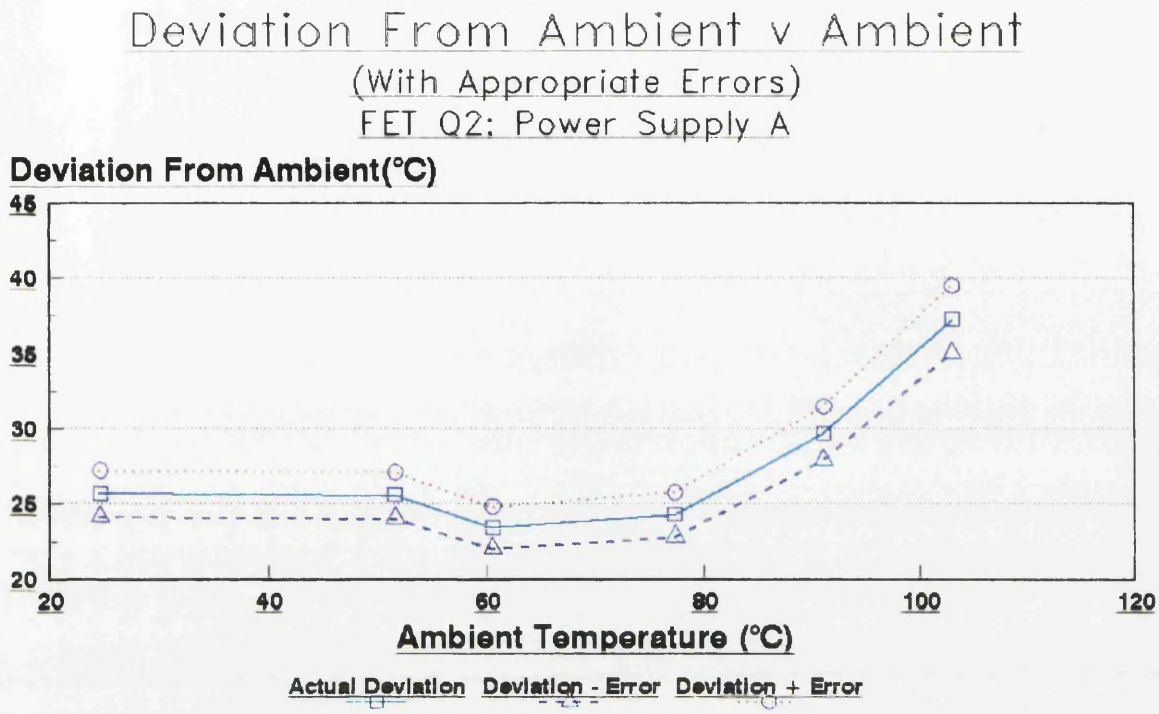
Figure 3.3
Deviation of Component Temperature From Ambient

It is worth noting that this test was originally carried out with one power supply. On that occasion the temperatures recorded for the components mounted on heatsinks were exceptionally low when compared with those seen during the observations of warm up after the power supply was switched on. It was discovered that this was due to the adhesive which had been used to attach the thermocouples to the components. This adhesive is thermally conductive and the had been applied in such a way that it increased the surface area of the component which was in contact with the heatsink. The consequence of this was that more of the components heat was being lost through conduction than would ordinarily be the case and the component temperature was lower than it would actually be in normal circumstances. For this reason it would seem advisable to work with the worst case, i.e. highest, actual temperatures recorded for each component in the two power supplies.

In these tests the comparisons of the average results are still valid because if there was an error due to this kind of measurement problem it would be present at all the ambient temperatures and therefore cancels out when the deviations from each value of ambient temperature are compared with each other.

On examination of the graphs in Figure 3.3 it would appear that the assumption which has previously been made in the lab. i.e. if the ambient temperature is increased the temperature of the components changes by the same amount, is, on the whole, valid. There are, however, certain points which should be taken into account.

In the case of the FETs it would appear that as the ambient temperature is raised so is the deviation from ambient. For FET Q2 the built in 3% error in the thermocouples causes a 6% error in the deviation from ambient. The graphs in Figure 3.4 show the "Deviation of Average Final Temperature From Ambient Temperature v Ambient Temperature", with associated error. The final temperatures being the temperatures of FET Q2, in power supplies A and B respectively, 30 minutes after the power supplies were switched on.



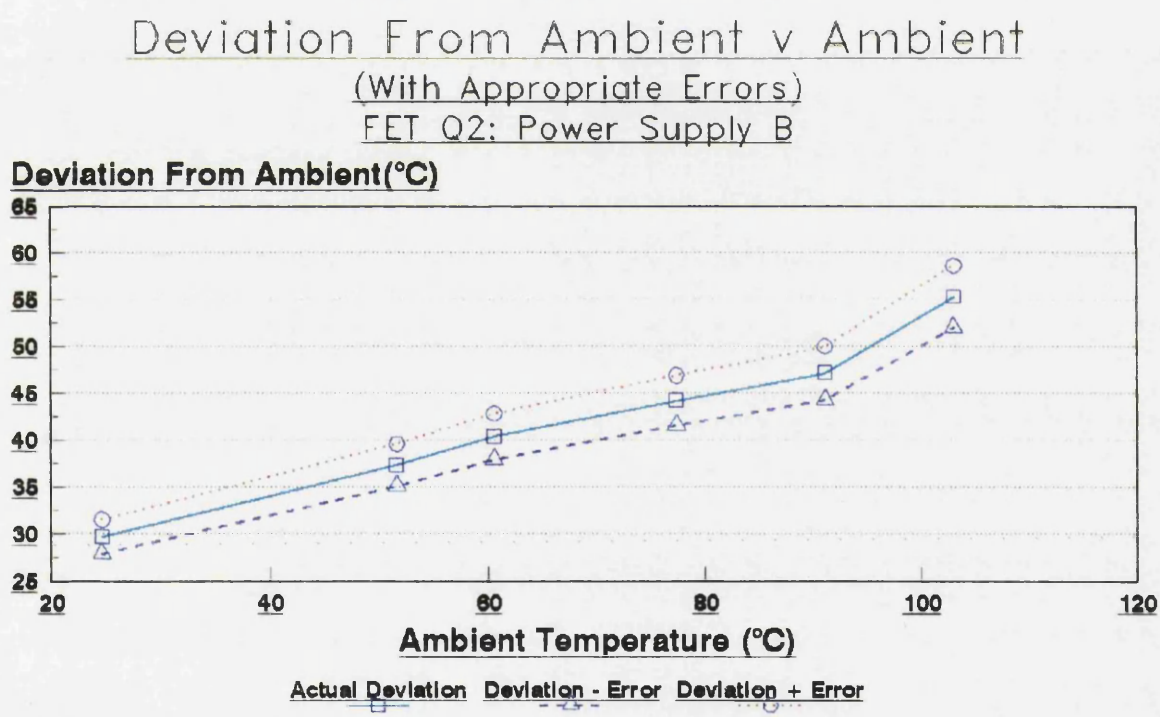
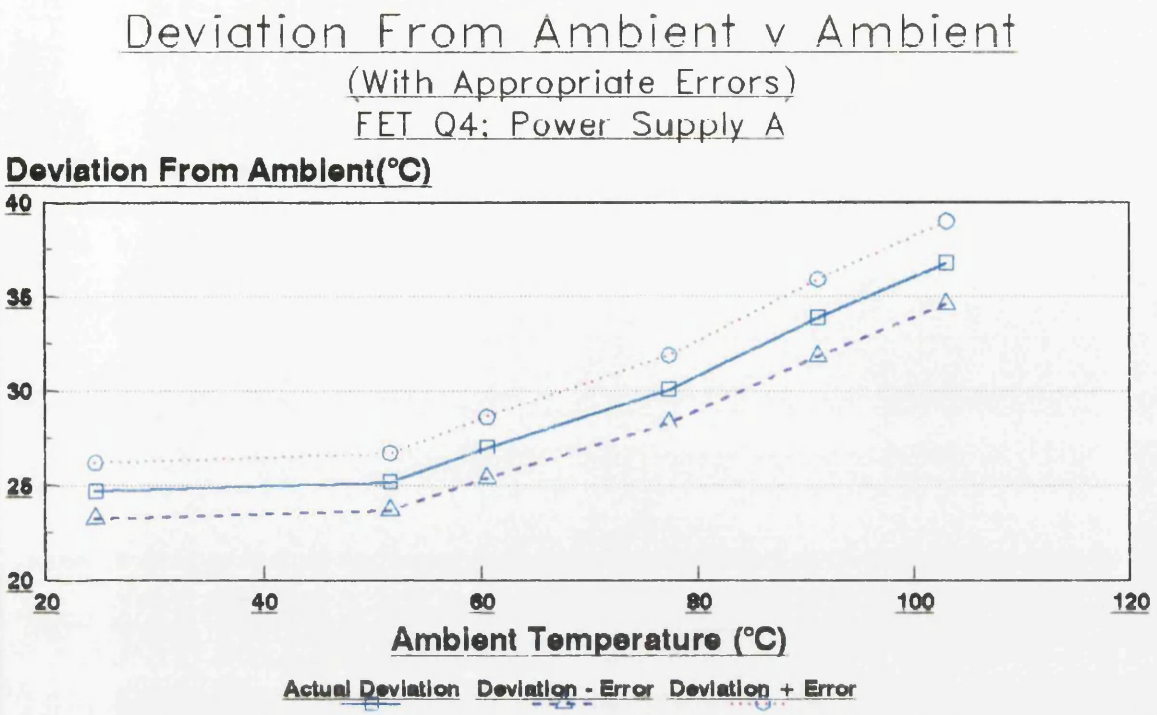


Figure 3.4
FET Q2; Deviations From Ambient Temperature

As can be seen from the graph for FET Q2 in power supply A when the associated 3% thermocouple errors are taken into account the assumption that the deviation from ambient temperature is constant appears to be true for ambient temperatures up to approximately 70°C. At ambient temperatures above 70°C the deviation of component temperature from ambient temperature increases as the ambient temperature increases. Unfortunately, however, this trend is not reflected in the measurements taken for the corresponding component in power supply b.

The graphs in Figure 3.5 show the distributions in the case of FET Q4. With this component, even when thermocouple errors are taken into account, the deviation of component temperature from ambient temperature tends to increase with ambient temperature over the complete range of ambient temperatures used. An error of 20% would be required for the assumption to hold at ambient temperatures of up to 75°C.



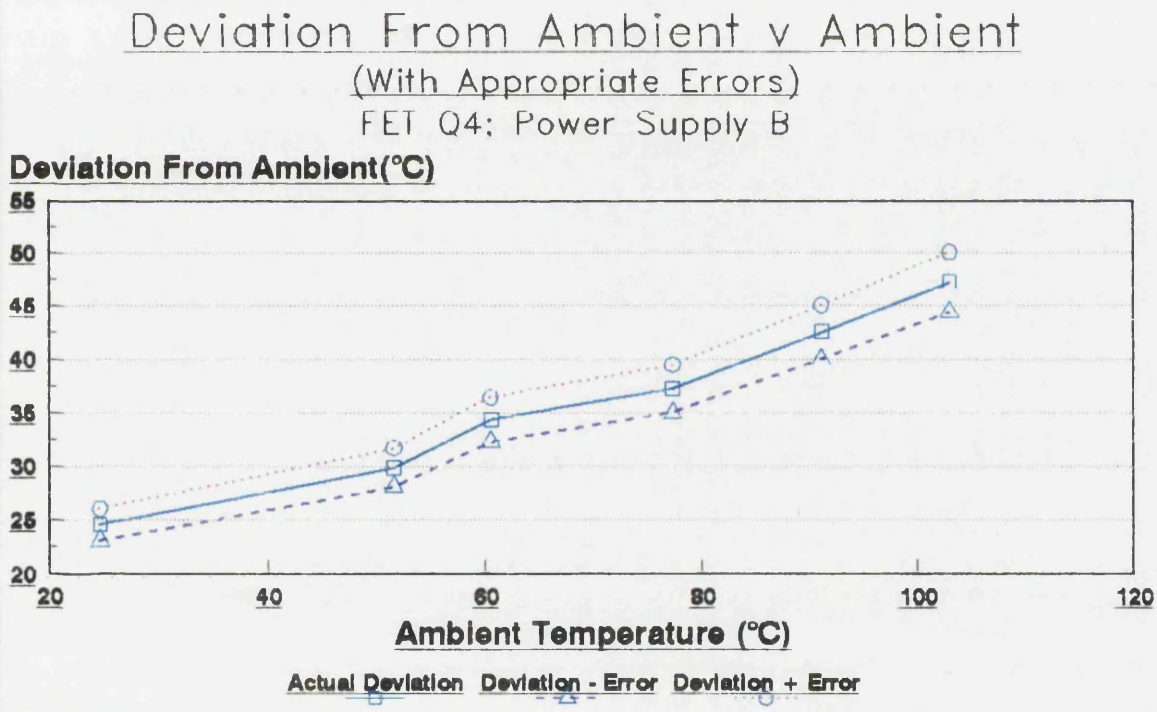


Figure 3.5
FET Q4; Deviations From Ambient Temperature

The deviations for the FETs show the widest spread of all the components. On examination of the +5V Output Diode it can be seen that there is almost no change in the deviation from ambient temperature across the 25°C to 100°C range of ambient temperatures. This trend is, on the whole, reflected in the behaviour of the other principal components. The various parts of Figure 3.6 show, with appropriate errors the deviations from ambient, at each of the temperatures used, for the main components tested.

The ambient inside the case was measured mainly to find out its actual value from the point of view of correcting for the plastic cover used during thermal imaging. It would seem that the ambient inside the case is between 2.8°C to 4.2°C above the temperature of the power supply's surroundings.

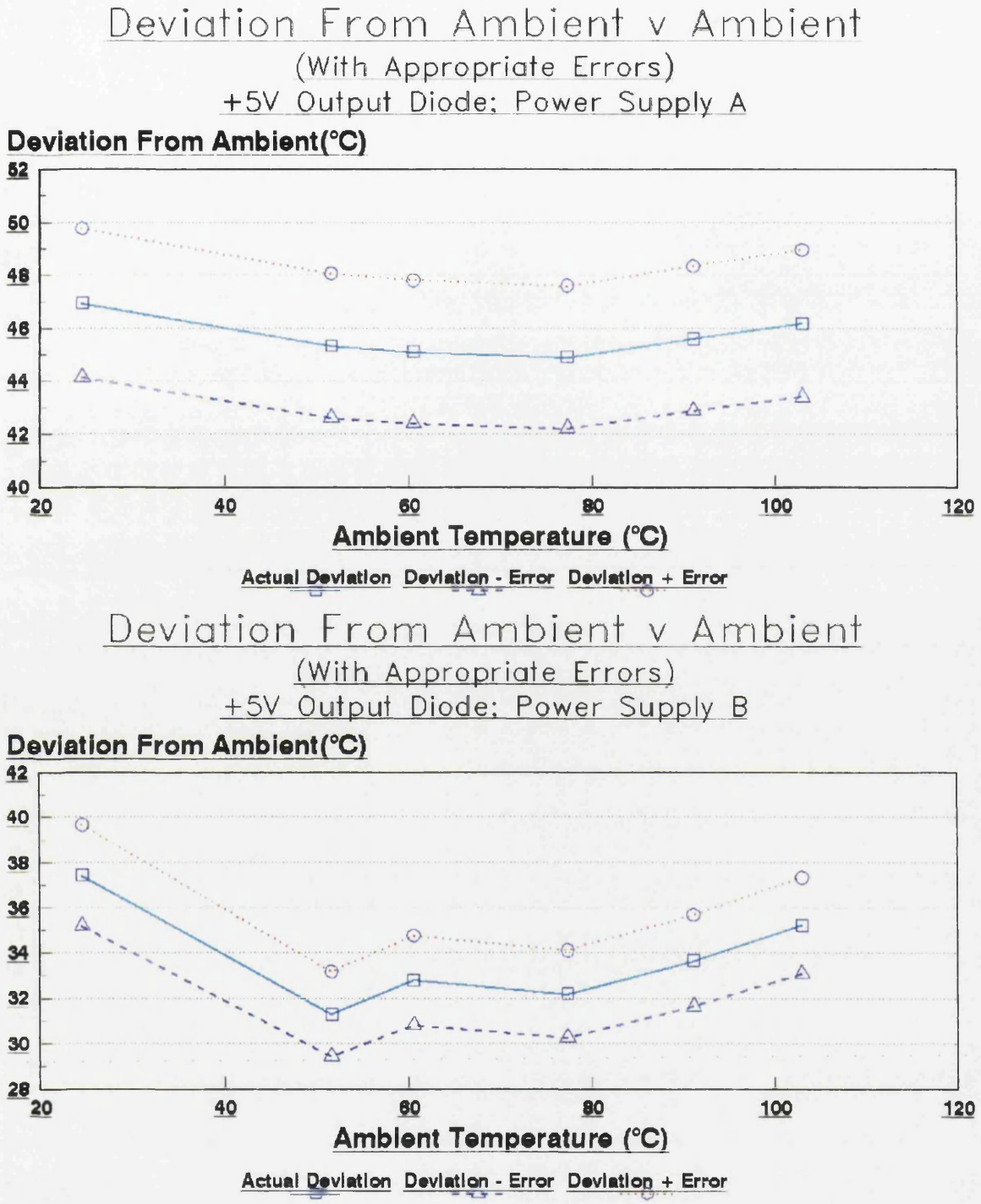
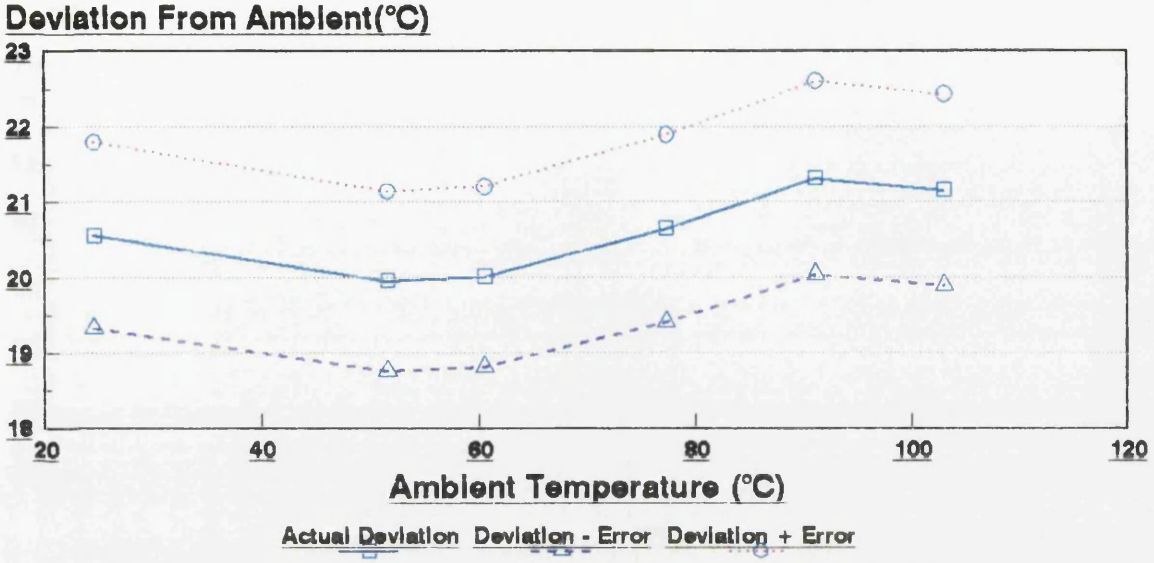


Figure 3.6(a)
+5V Output Diode; Deviations From Ambient.

Deviation From Ambient v Ambient

(With Appropriate Errors)

+5V Output Capacitor; Power Supply A



Deviation From Ambient v Ambient

(With Appropriate Errors)

+5V Output Capacitor; Power Supply B

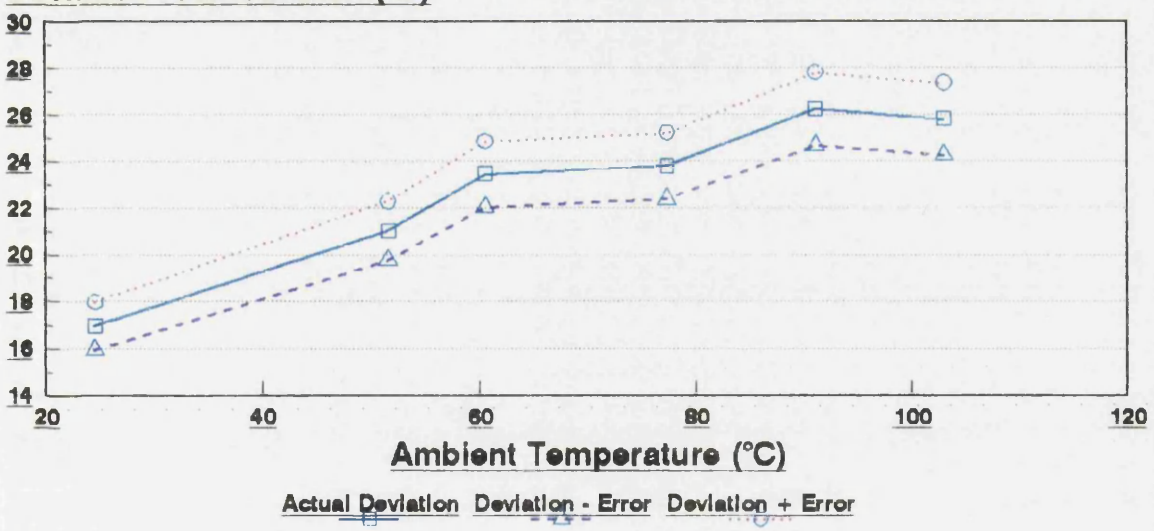


Figure 3.6(b)

+5V Output Cap'r; Deviations From Ambient.

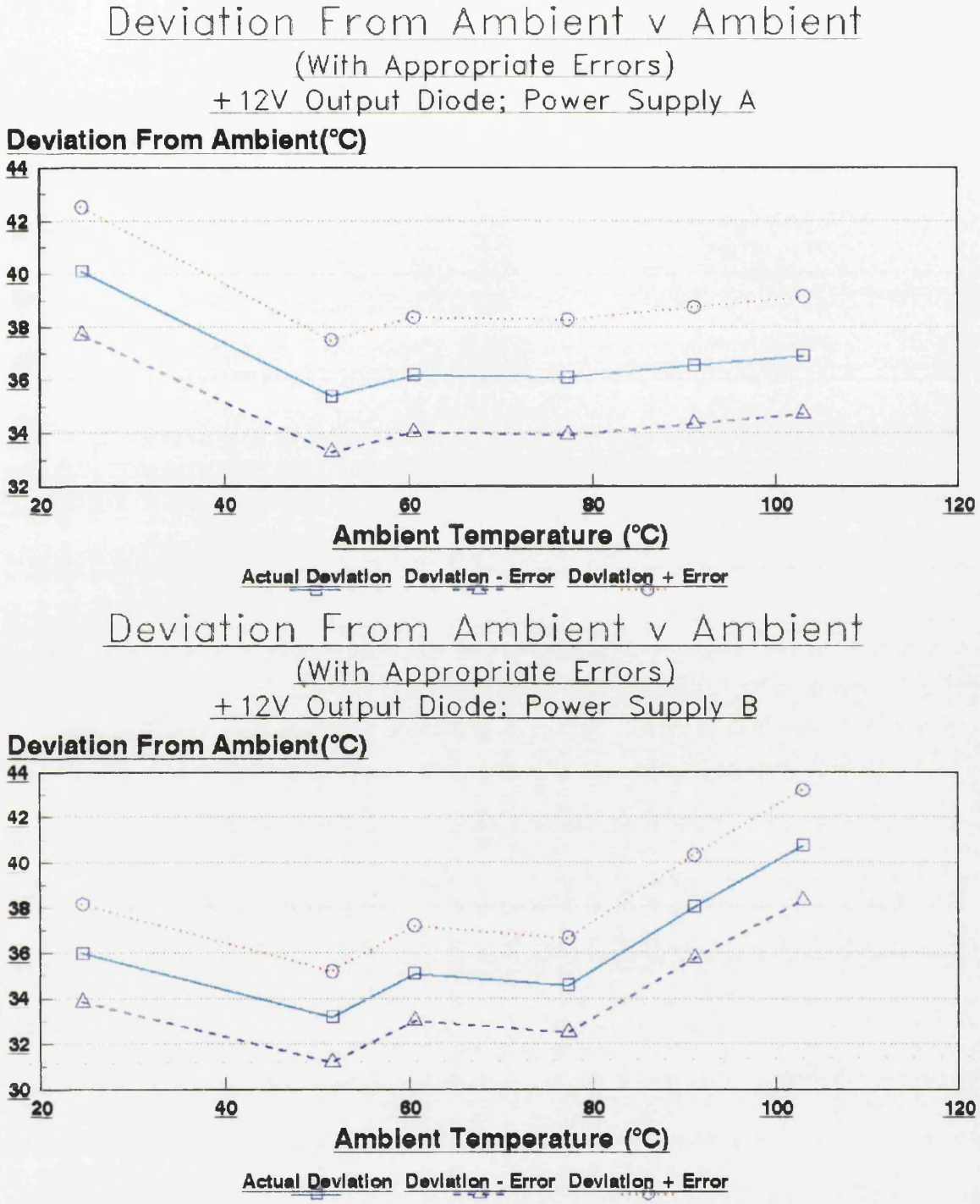
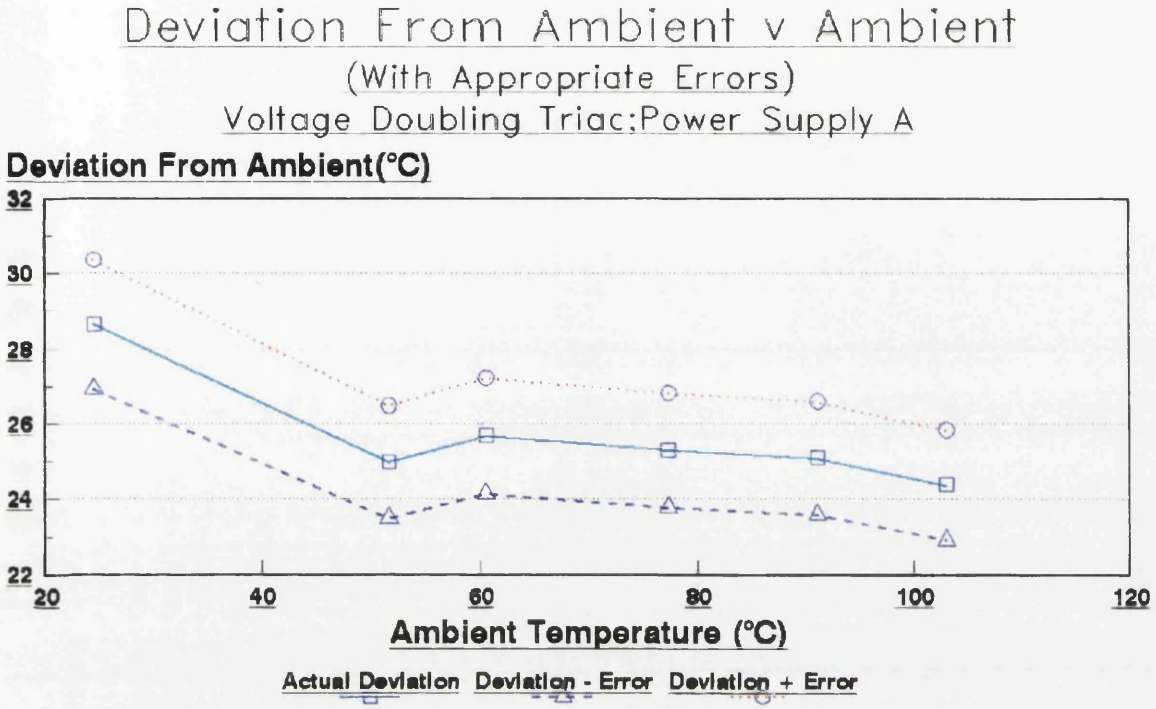


Figure 3.6(c)
+12V Output Diode; Deviations From Ambient.



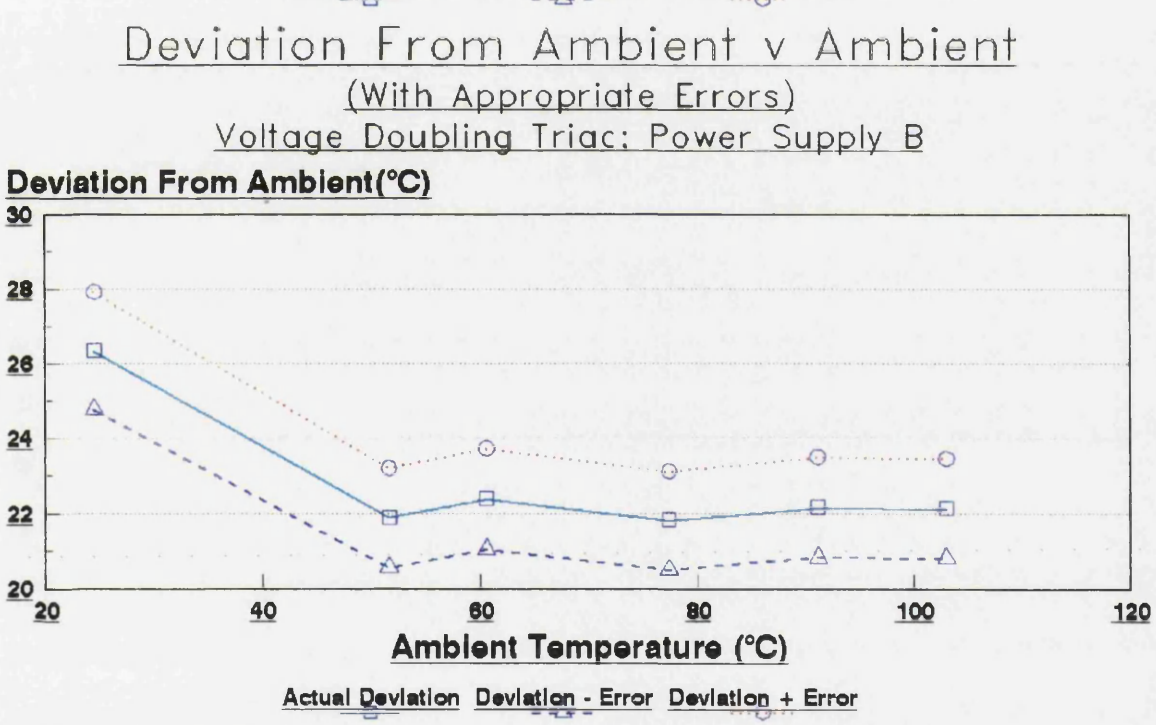
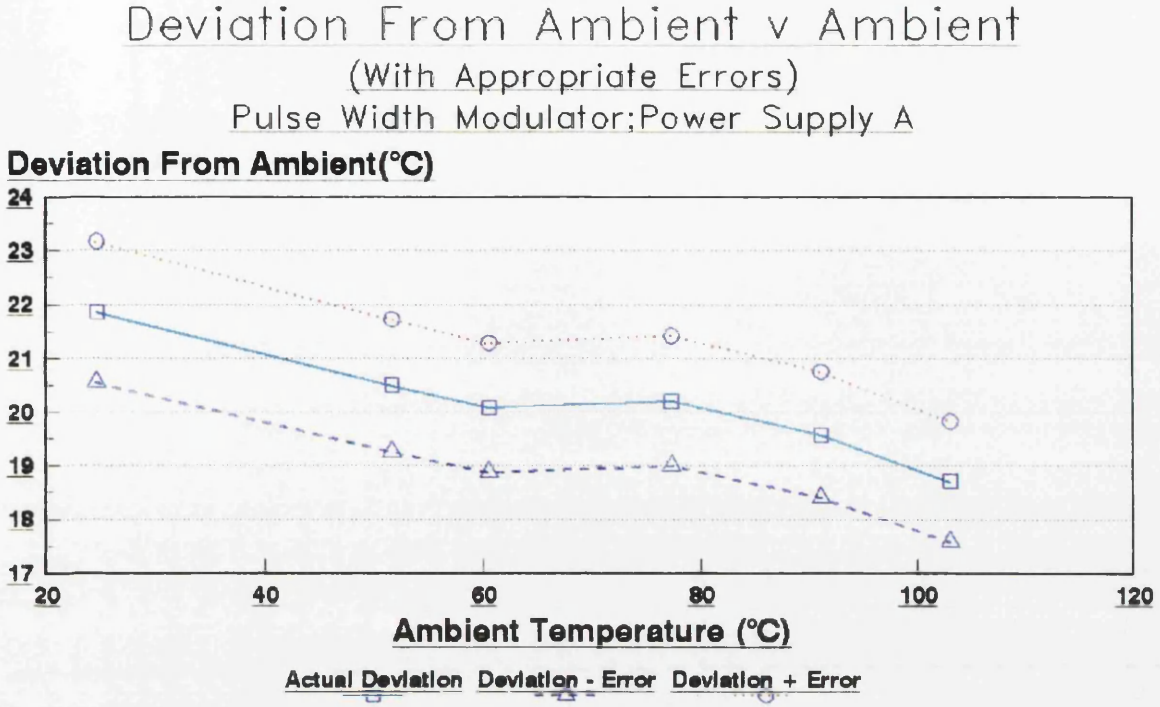


Figure 3.6(d)

Voltage Doubling Triac; Deviations From Ambient.



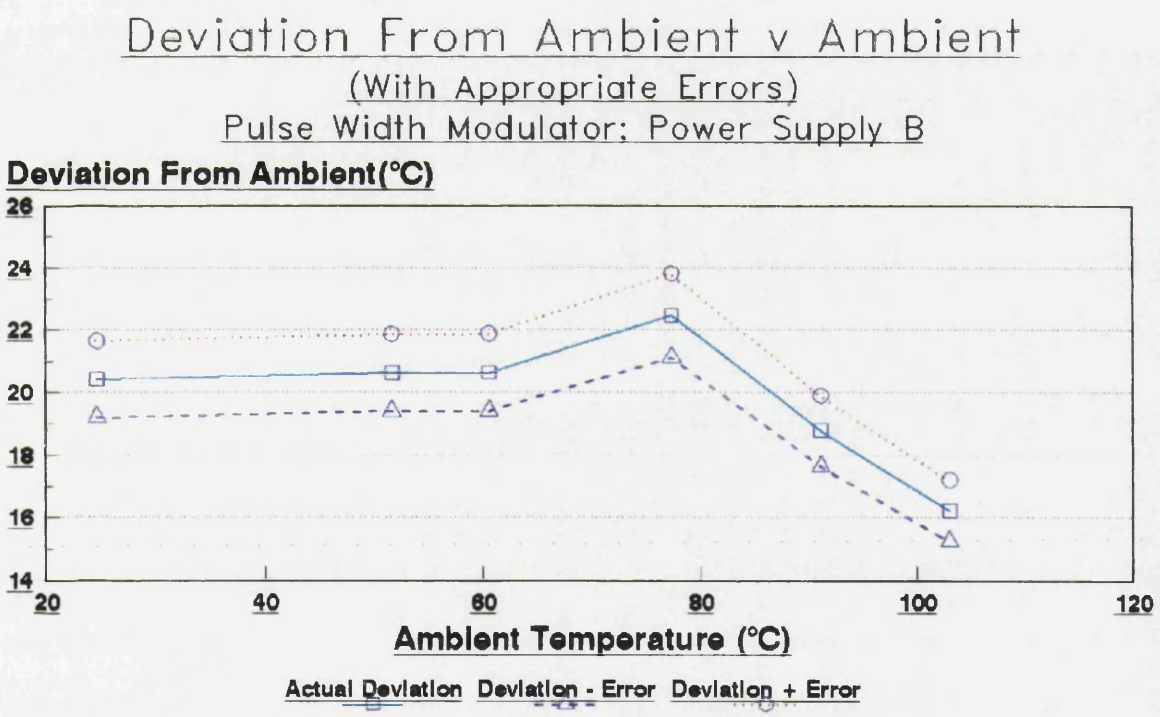


Figure 3.6(e)
PWM; Deviations From Ambient.

Figure 3.7(a) shows the average value of the +5V output of the power supplies during the various high temperature tests. The main purpose of logging the output voltages was to reveal whether the voltages became unstable, or had values outwith the specified limits at any particular value of ambient temperature. Neither phenomenon is apparent in the case of the +5V output. The +12V and -12V outputs, as shown in Figure 3.7(b) showed some fluctuation but remained within their specified limits.

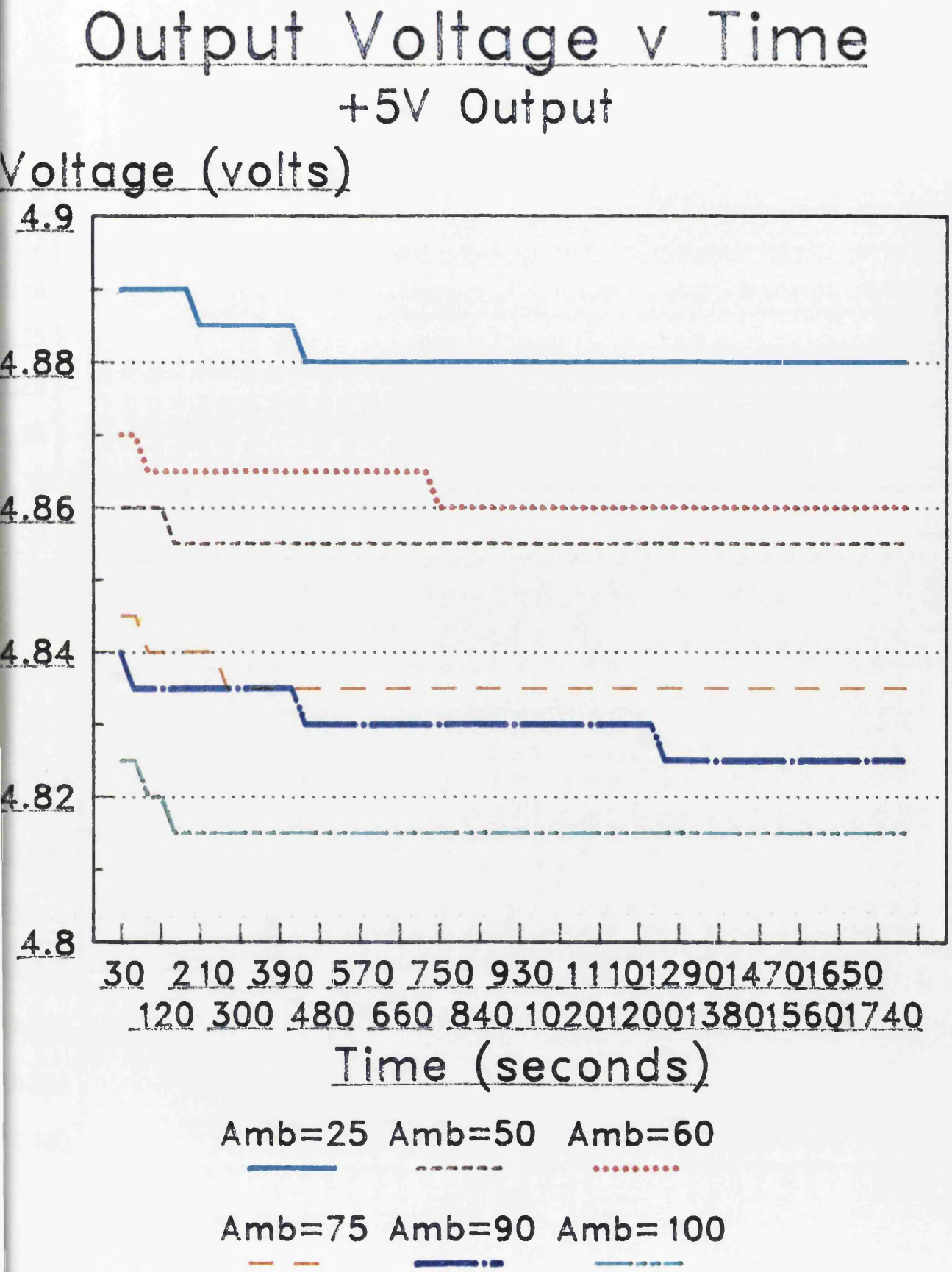
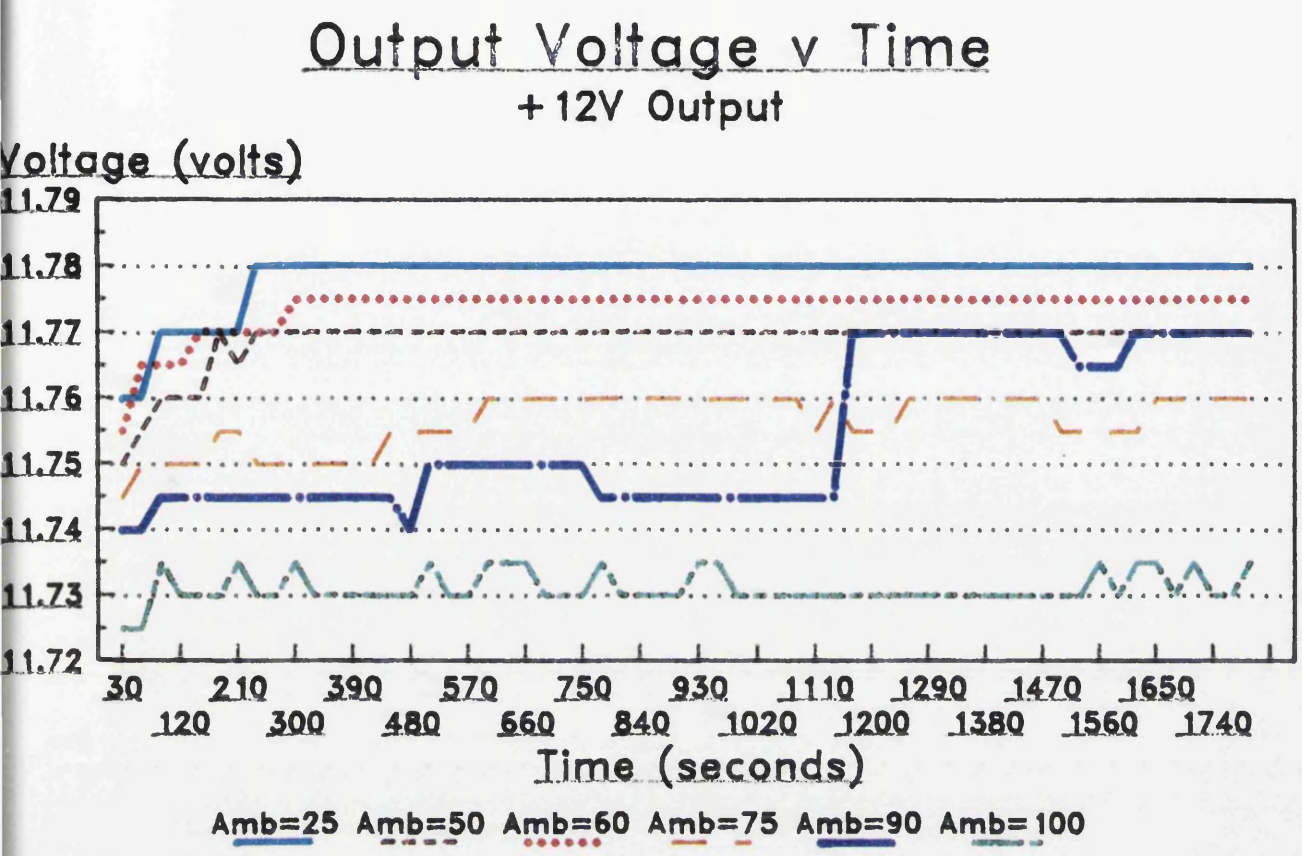


Figure 3.7(a)
Averaged +5V Output Voltages



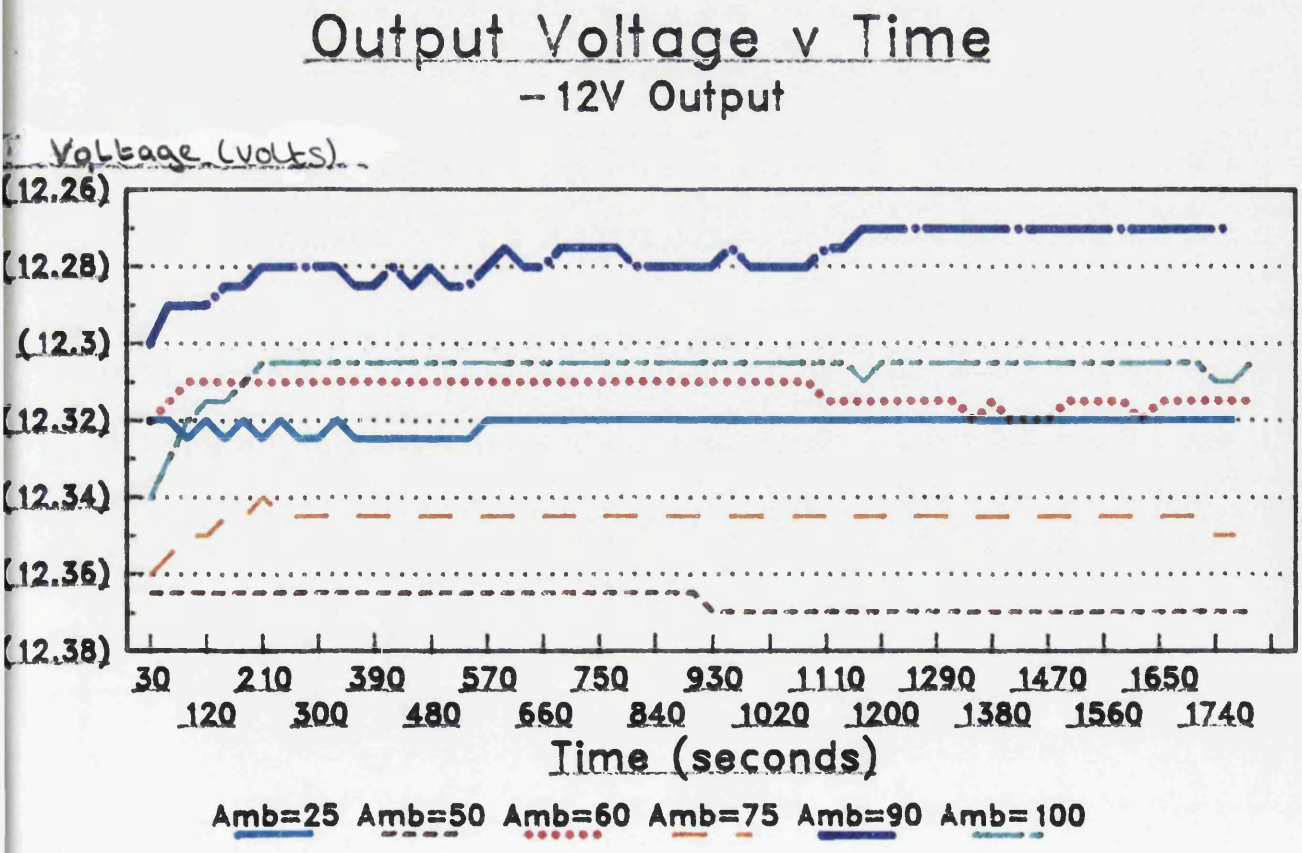


Figure 3.7(b)
Averaged +12V and -12V Output Voltages

Conclusions

The initial assumption, which was that a change in the temperature of a power supply's environment causes an equivalent change in the individual component temperatures, would, on the whole, appear to be valid up to an ambient temperature of 75°C for most components provided the measurements include the built-in errors of the thermocouples. The exception to this is the FETs where the deviation from ambient increases with ambient temperature. The worst case is FET Q4 where it would seem that the assumption would hold if the error in the deviation were increased to 17%. Such an assumption would allow component temperatures at higher ambients to be predicted if their values at a 25°C ambient were known. Although this assumption appears to be valid; if it were to be a critical factor in a test further verification would be advisable.

If the failure of the FET temperatures to follow the trend exhibited by the temperatures of the other components were due to a systematic error in the measurement of the FET temperatures; and if this error could be found and eliminated, then it is possible that the FET temperatures would mirror the trend adopted by the temperatures of the other components.

Section 3.4: Temperature Analysis By Thermal Imager

If it were decided in the future to make use of the aforementioned trends to establish the maximum, safe operating ambient temperature for a previously untested power supply then it would perhaps be worth investigating the accuracy with which the temperatures of individual components could be measured using a thermal imager.

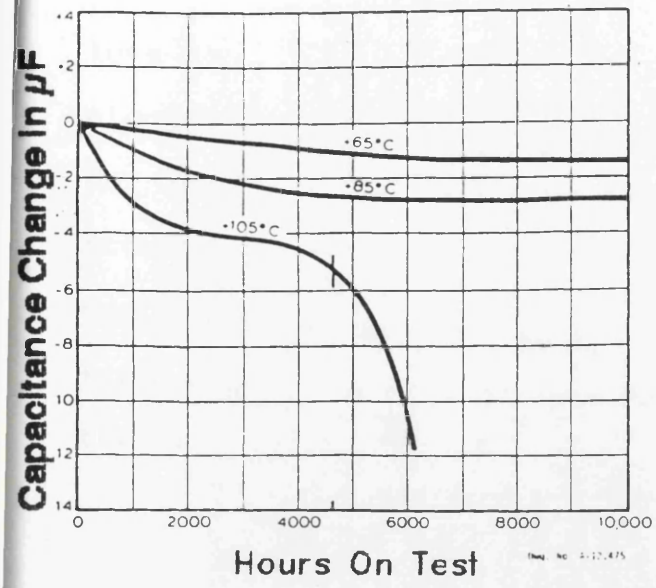
Each power supply which comes into the laboratory undergoes thermal analysis as a matter of course and if the relevant temperatures could be determined with sufficient accuracy in this manner then there would be no need for the time consuming task of attaching thermocouples to components.

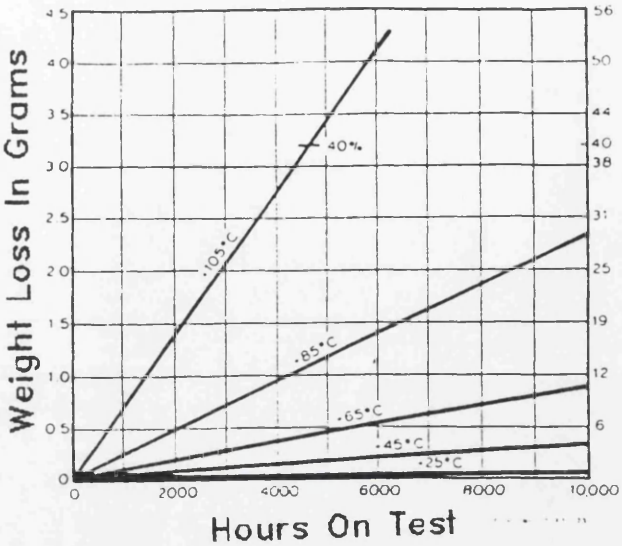
Section 3.5:The Effect of Elevated Temperature on Electrolytic Capacitors

This set of tests came about from an interest in the possible use of measurements made on the electrolytic capacitors to give an idea of true test lengths.

The thinking behind this was as follows: If a direct relationship could be found between capacitor weight loss and time under test at different temperatures then it should be possible to use before and after weights from capacitors involved in the life test to give a true idea of the actual life test length by knowing how long it takes for such a weight loss to take place under the conditions experienced by the capacitor both while in test and while in actual use.

Figure 3.8 shows published manufacturer's data in the form of tables relating capacitor weight loss to useful life at various operating temperatures. One of the main purposes of this experiment was to see if those results could be reproduced.





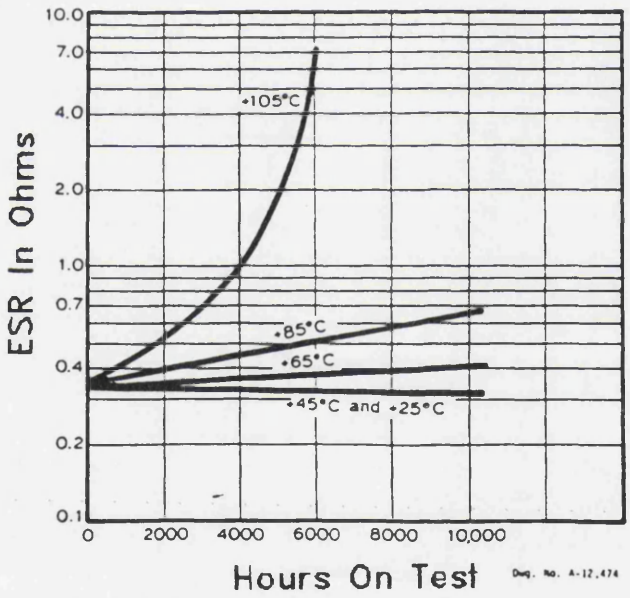


Figure 3.8

Manufacturer's Capacitor Degradation Data

Additionally, since the cause of the weight loss is a specific process i.e. evaporation of capacitor electrolyte, the activation energy of this process could be used with the Arrhenius equation to give an acceleration factor for the test used. Figure 3.9 demonstrates how the activation energy can be calculated from the manufacturer's data. In this case the energy is that required to evaporate a certain mass of electrolyte.

There is another possible use of data relating to electrolytic capacitors: A typical capacitor life is in excess of 80,000 hours at 55°C. At present power supply MTTFs are in the region of 50,000 hours at 35°C. (35°C being the ambient temperature inside the case of an operating computer)

If the power supply was tested to the point where the capacitors had undergone 80,000 hours at 35°C, i.e. had demonstrated weight loss corresponding to 80,000 hours at 35°C, or the accelerated equivalent, and the power supply had not failed then The MTTF target would seem to have been satisfied.

Electrolytic Capacitor Activation Energy

(Activation energies refer to the energy required per molecule to participate in a reaction)

Weight Loss is directly proportional to reaction rate as given by the Arrhenius Equation: $K = A \exp(-E/kT)$

Therefore: $W(t) = B \exp(-E/kT)$

Where W(t) is the weight loss after t hours at a temperature of TK

$$W1(t) = B \exp(-E/kT1)$$

$$W2(t) = B \exp(-E/kT2)$$

$$\text{and } W1(t) = 2 * W2(t)$$

$$\text{then } 2 = (\exp(-E/kT1)/\exp(E/kT2)) = \exp(E/k)((1/T2)-(1/T1))$$

$$\text{and } \ln 2 = E/k((1/T2)-(1/T1))$$

$$E = \frac{\ln 2 * k}{((1/T1)-(1/T2))}$$

Take the following values: T1 = 105°C = 378.15K
(See Figure 3.8)
T2 = 85°C = 358.15K
k = 8.617e-05

$$E = \frac{0.693 * 8.617e\text{-}5}{(1.476e\text{-}04)}$$

Capacitor Activation Energy = 0.4eV

Figure 3.9
Capacitor Activation Energy Calculation

The first investigation in this area involved placing three sets of capacitors at each of 25°C, 60°C and 75°C. On a weekly basis the following measurements were made for each capacitor:

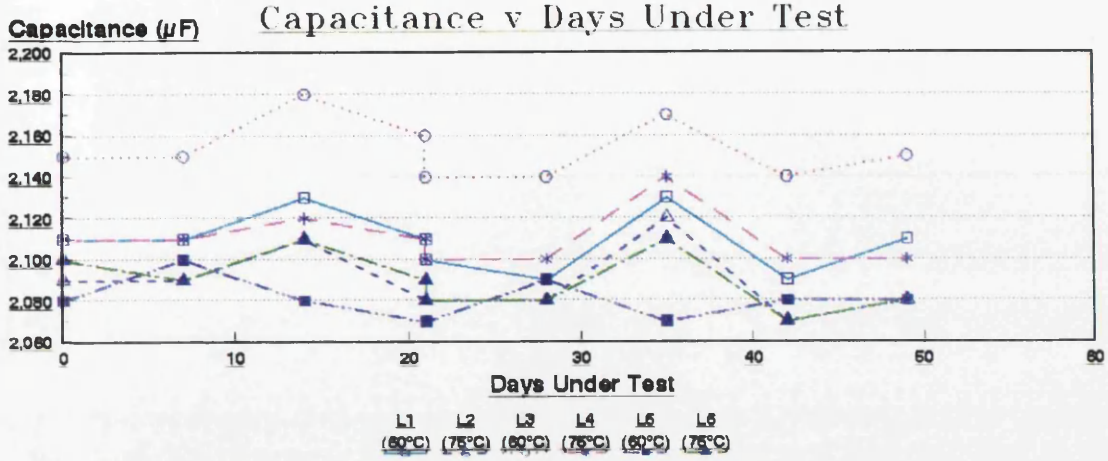
Weight

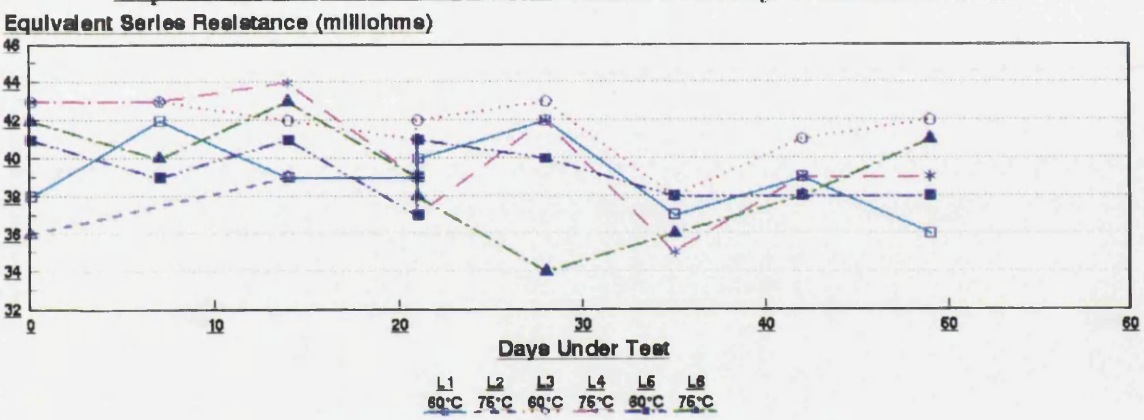
Capacitance

Equivalent Series Resistance.

The results of the measurements taken at 60°C and 75°C appear in Figure 3.10. Unfortunately most of the variables did not change appreciably over the test period except, that is, the weights and capacitances of the smaller capacitors which decreased steadily during the test. Their Equivalent Series Resistances, however, did not exhibit the increase which should have accompanied such a trend. However, examination of the manufacturer's data, which was obtained subsequent to the test being carried out reveals that at the temperatures involved no discernible changes could be expected before the test had been running for approximately 2000 hours.

Large Capacitors





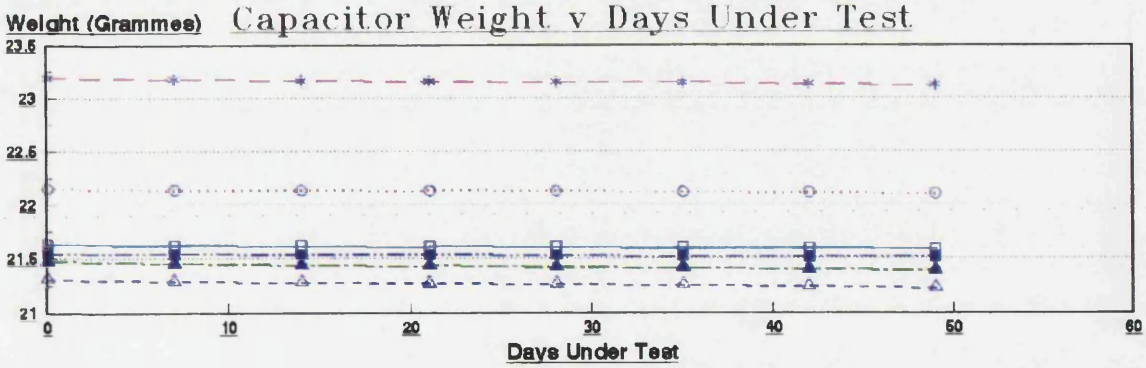
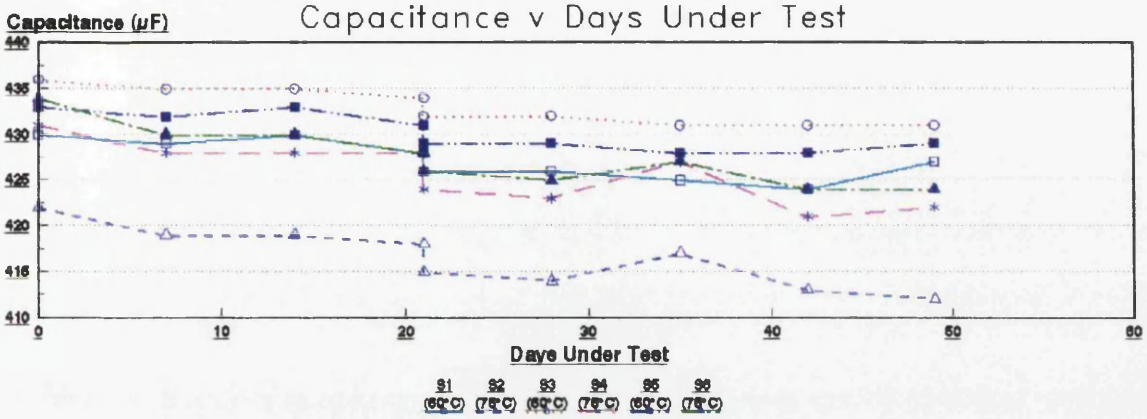
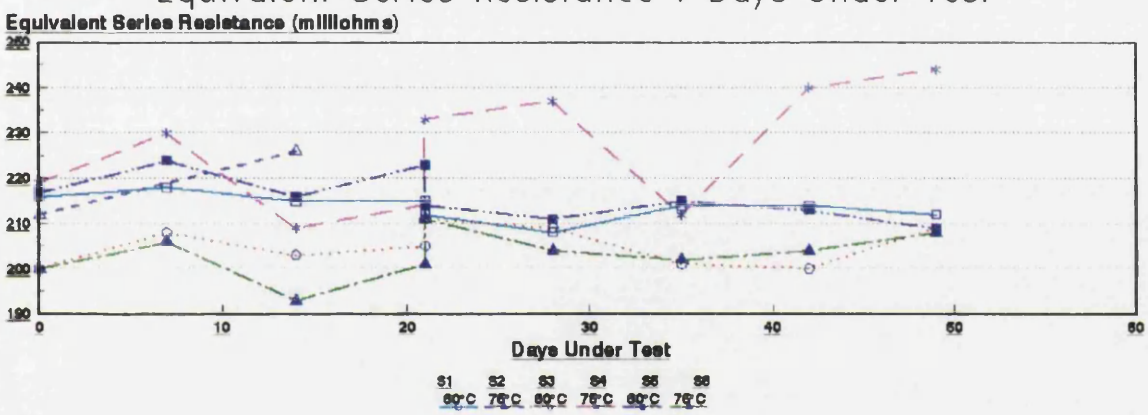


Figure 3.10(a)

Data From Capacitor Measurements

Small Capacitors





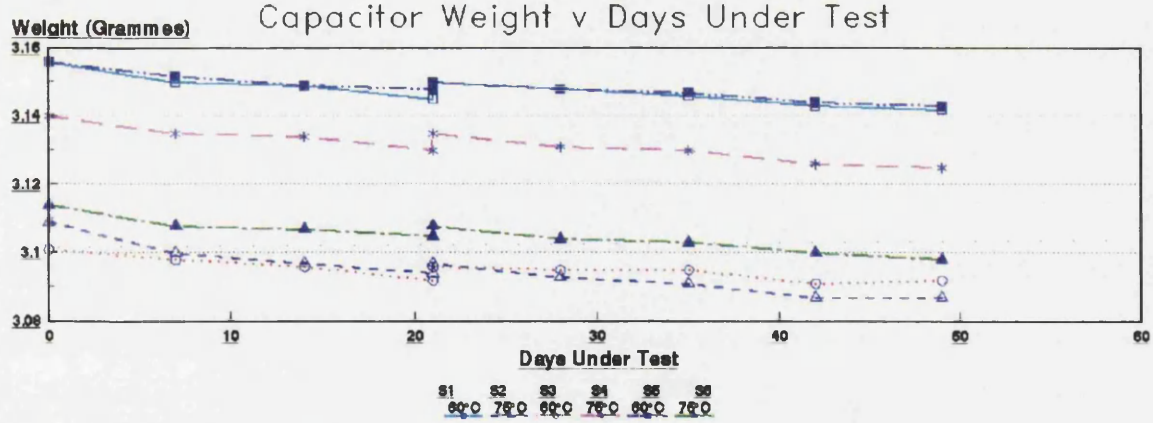


Figure 3.10(b)
Data From Capacitor Measurements

Concurrent with this test two other investigations, also related to capacitor degradation and the effects of elevated ambient temperature were taking place.

The first of these involved running two power supplies non-stop in an ambient temperature of 75°C.

The second test cycled four power supplies on and off, with 2 power supplies being cycled at each of 2 different on/off cycles: One cycle switched the Power supplies on for 20 seconds and then off for 20 seconds. The other cycle switched the power supplies on for 60 minutes and off for 15 minutes.

Figure 3.11 contains the regulation and ripple voltage results for the constant high ambient test and Figure 3.12 shows the corresponding results for the units which were cycled. It was discovered during the course of the test that the ambient temperature in which the power supplies were switched on had a significant influence on output ripple voltage measurements. Thereafter steps were taken to ensure as far as possible that the power supplies were always switched on at the same ambient temperature.

Constant High Ambient Test
Output Voltage Regulation Results
Output Voltage v Hours Under Test

	Unit 1 +12V	Unit 2 +12V	Unit 1 +5V	Unit 2 +5V	Unit 1 -5V	Unit 2 -5V	Unit 1 -12V	Unit 2 -12V
0	11.88	11.95	5.04	5.04	-5.07	-5.09	-12.21	-12.33
96	11.89	12.23	5.04	5.01	-5.06	-5.12	-12.22	-12.76
240	11.88	12.21	5.04	5.03	-5.06	-5.10	-12.24	-12.74
528	11.88	12.23	5.02	5.00	-5.07	-5.09	-12.20	-12.70
696	11.85	12.29	5.03	5.01	-5.07	-5.09	-12.17	-12.94
888	11.87	12.22	5.02	5.02	-5.07	-4.99	-12.20	-12.63
1008	11.83	12.20	4.98	5.01	-5.08	-5.06	-12.22	-13.02
1128	11.86	12.12	5.01	5.02	-5.06	-5.09	-12.18	-12.70

Output Ripple Voltage
Specified Maximum Values

Output Channel	+12V	+5V	-5V	-12V
Ripple Voltage(mV)	80	50	100	100

Constant High Ambient Test
Output Voltage Ripple Results
Ripple Voltage v Hours Under Test

	Unit 1 +12V	Unit 2 +12V	Unit 1 +5V	Unit 2 +5V	Unit 1 -5V	Unit 2 -5V	Unit 1 -12V	Unit 2 -12V
0	33.00	38.00	9.00	7.00	12.00	10.00	39.00	39.00
96	33.00	45.00	10.00	6.00	11.00	11.00	35.00	43.00
240	38.00	60.00	10.00	12.00	13.00	18.00	42.00	52.00
528	24.00	40.00	10.00	10.00	12.00	15.00	34.00	44.00
696	45.00	95.00	12.00	10.00	10.00	19.00	38.00	55.00
888	40.00	70.00	9.00	9.00	9.00	10.00	28.00	35.00
1008	45.00	90.00	10.00	10.00	9.00	18.00	40.00	55.00
1128	44.00	90.00	8.00	9.00	10.00	17.00	35.00	45.00

Figure 3.11 High Ambient Test Regulation and Ripple Results

High Ambient Power Cycling
Output Regulation

	Unit_1 +12V	Unit_2 +12V	Unit_3 +12V	Unit_4 +12V	Unit_1 +5V	Unit_2 +5V	Unit_3 +5V	Unit_4 +5V	Unit_1 -5V	Unit_2 -5V	Unit_3 -5V	Unit_4 -5V	Unit_1 -12V	Unit_2 -12V	Unit_3 -12V	Unit_4 -12V	
24	11.88	11.96	11.94	11.94	5.03	5.07	5.010	5.03	(5.04)	(5.03)	(4.97)	(5.02)	(12.12)	(12.24)	(12.24)	(12.23)	
192	11.88	11.96	11.94	11.93	5.03	5.05	5.030	5.03	(5.04)	(5.03)	(4.97)	(5.02)	(12.10)	(12.24)	(12.21)	(12.23)	
336	11.87	11.94	11.93	11.93	5.03	5.05	5.025	5.03	(5.03)	(5.02)	(4.98)	(5.02)	(12.11)	(12.24)	(12.21)	(12.15)	
504	11.88	11.93	11.92	11.92	5.03	5.05	5.010	5.03	(5.04)	(5.02)	(4.97)	(4.99)	(12.11)	(12.25)	(12.24)	(12.22)	
672	11.88	11.93	11.93	11.94	5.01	5.05	5.030	5.03	(5.02)	(5.03)	(4.98)	(4.99)	(12.07)	(12.21)	(12.22)	(12.11)	
864	11.87	11.91	11.89	11.93	5.02	5.05	5.010	5.03	(5.02)	(5.04)	(5.01)	(5.01)	(12.04)	(12.22)	(12.23)	(12.31)	75 C Start
864	11.83	11.94	11.88	11.91	5.01	5.07	5.040	5.04	(5.03)	(5.02)	(4.98)	(4.98)	(12.09)	(12.25)	(12.21)	(12.30)	10 C Start
864	11.83	11.93	11.89	11.96	5.00	5.05	5.030	5.04	(5.01)	(5.02)	(4.98)	4.98	(12.12)	(12.23)	(12.23)	(12.24)	25 C Start

Ambient Temperature when PSU Switched on

Units 1 and 2: 20 seconds on, 20 seconds off
Units 3 and 4: 60 minutes on, 15 minutes Off

High Ambient Power Cycling
Output Ripple Voltage

	Unit_1 +12V	Unit_2 +12V	Unit_3 +12V	Unit_4 +12V	Unit_1 +5V	Unit_2 +5V	Unit_3 +5V	Unit_4 +5V	Unit_1 -5V	Unit_2 -5V	Unit_3 -5V	Unit_4 -5V	Unit_1 -12V	Unit_2 -12V	Unit_3 -12V	Unit_4 -12V	
24	28	40	38	21	12	5	5	5	15	12.0	8	6	37	40	44	27	
192	28	38	36	30	6	6	8	8	10	12.0	10	7	38	40	36	27	
336	28	37	36	20	6	7	6	9	14	11.5	10	6	40	38	34	28	
504	28	38	34	30	5	6	8	9	14	11.0	8	6	38	38	37	28	
672	29	36	36	31	7	6	6	7	14	14.0	9	8	34	38	34	24	
864	31	40	36	30	4	8	7	10	13	12.0	10	8	35	35	36	36	75 C Start
864	67	38	90	79	4	8	10	9	15	8.0	14	7	44	32	58	35	10 C Start
864	50	54	68	50	6	7	12	8	13	14.0	13	7	44	40	47	34	25 C Start

Ambient Temperature when PSU Switched on

Figure 3.12
High Ambient Power Cycling Regulation and Ripple Checks.

A trial run of one of the tests used revealed that capacitor failure, i.e. where the capacitance drops to approximately 40% of its listed value, is accompanied by a visible change in the appearance of the capacitor. Figure 3.13 shows external and internal photographs of both functional and failed capacitors.

As well as investigating the effects of each of these tests in their own right; by monitoring regulation, ripple voltage and capacitor appearance on a weekly basis; the cycling tests were also compared to each other, and the thermal cycling test in the next chapter, with respect to effectiveness in increasing ripple voltage and capacitor equivalent series resistance and decreasing capacitance.

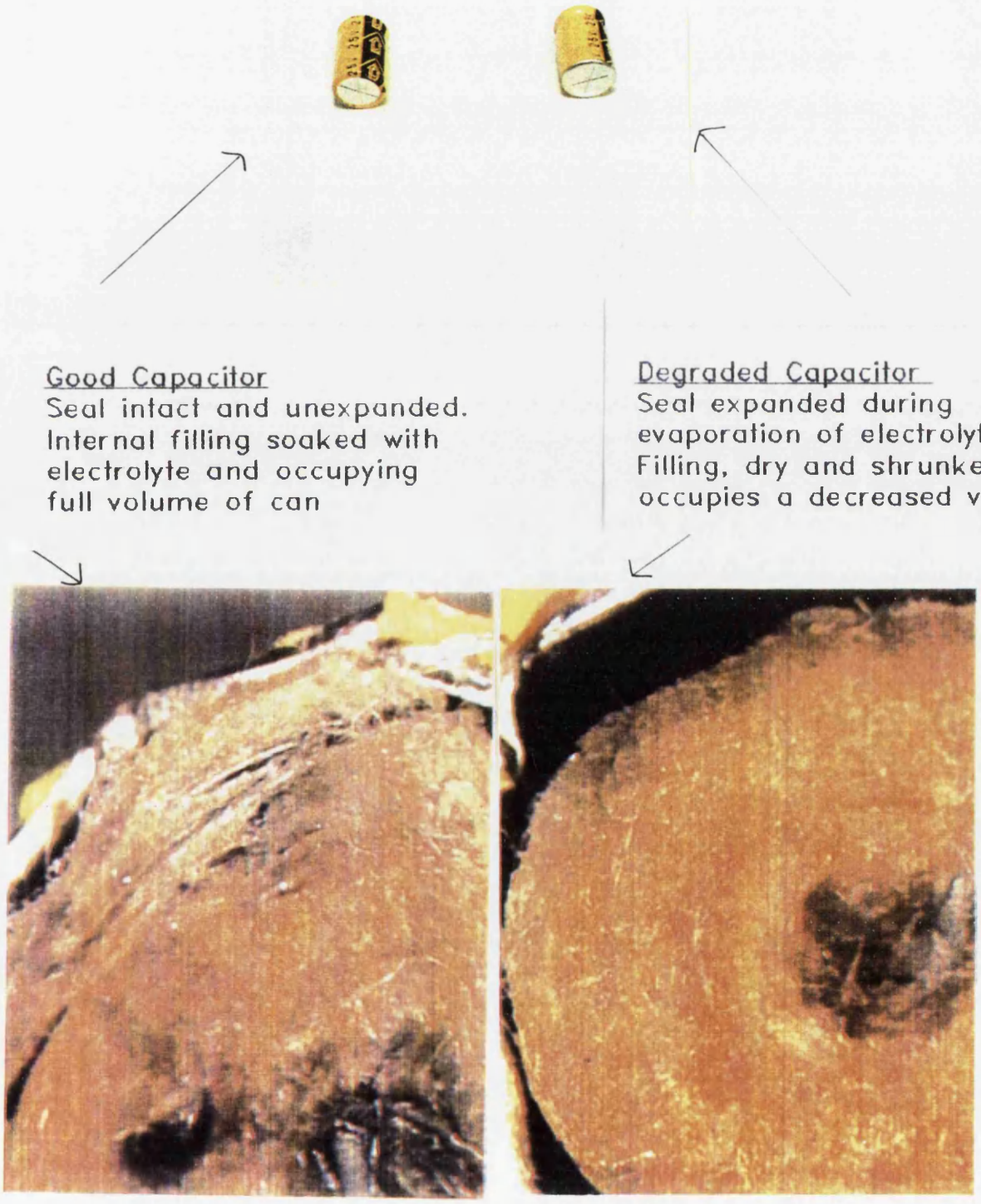


Figure 3.13

Good and Degraded Capacitors

This test involved taking an unstressed power supply, checking its regulation and ripple values with its own output capacitors in place and then replacing these with the output capacitors of the units which had been stressed. The comparison was made thus to ascertain whether the observed increase in ripple voltage in the stressed units was due to the output capacitors, the suspected cause, or due to other components in the power supply. By selecting one power supply and making the capacitor values the only variable, by slotting different capacitors into the same support circuitry, then any changes which took place could only have been caused by the change of capacitors. The results of those comparisons involving cycled units are shown in Figure 3.14. As can be seen from the tables 3 out of the 4 units involved in High Ambient Power Cycling emerged from the test with +12V output ripple values much higher than those achieved with the untested unit. The values of capacitance for the corresponding output capacitors are significantly less than 40% of the rated values for those components and the equivalent series resistance values were much higher than those of the unstressed unit; another indication of capacitor degradation.

High Ambient Power Cycling

Results of Measurements on Capacitors

Capacitance(μF)

	Nominal Value	Unit 11 Untested Unit	Unit 1 20 seconds on/20 off	Unit 2 20 seconds on/20 off	Unit 3 60 minutes on/15 off	Unit 4 60 minutes on/15 off
+12V O/P Capacitor	470	438.0	128.6	427.0	171.8	103.7
+5V O/P Capacitor	470	447.0	449.0	443.0	434.0	298.0
-5V O/P Capacitor	47	44.3	43.4	44.4	37.0	38.8
-12V O/P Capacitor	100	98.2	93.2	90.1	88.5	91.3
Input Capacitor	470	412.0	409.0	433.0	458.0	448.0

High Ambient Power Cycling

Results of Measurements on Capacitors

Equivalent Series Resistance (milliohms)

	Unit 11 Untested Unit	Unit 1 20 Seconds on/20 off	Unit 2 20 seconds on/20 off	Unit 3 60 minutes on/15 off	Unit 4 60 minutes on/15 off
+12V O/P Capacitor	178	3,906	242	4,200	1,220
+5V O/P Capacitor	174	249	260	287	338
-5V O/P Capacitor	3,170	4,460	4,180	4,360	5,300
-12V O/P Capacitor	1,040	880	1,470	1,510	1,160
Input Capacitor	191	159	156	163	163

Figure 3.14
Characteristics of Stressed and Unstressed Capacitors

Additionally, in order to have some idea of the degree of thermal stress which the test caused to the capacitors measurements were taken, during the High Ambient Power Cycling test of the temperatures of the capacitors over 1 cycle. The results of these measurements appear in Figure 3.15. Note that the +12V Output capacitor, that which showed most evidence of degradation, is the hottest of all the output capacitors. Although these measurements were not repeated for the power supplies which were constantly switched on the temperatures of the capacitors in those units would be equivalent to the stabilised temperature of the capacitors in the cycled units during the period of their cycle in which the power was switched on. Figure 3.16 gives an estimated graph of the temperatures of the capacitors in the units which were constantly switched on. Due to equipment and time constraints it was not possible to make the corresponding measurements for those unit with the 20 seconds on/20 seconds off cycle and there are sufficient variables involved to ensure that any estimate would be highly speculative.

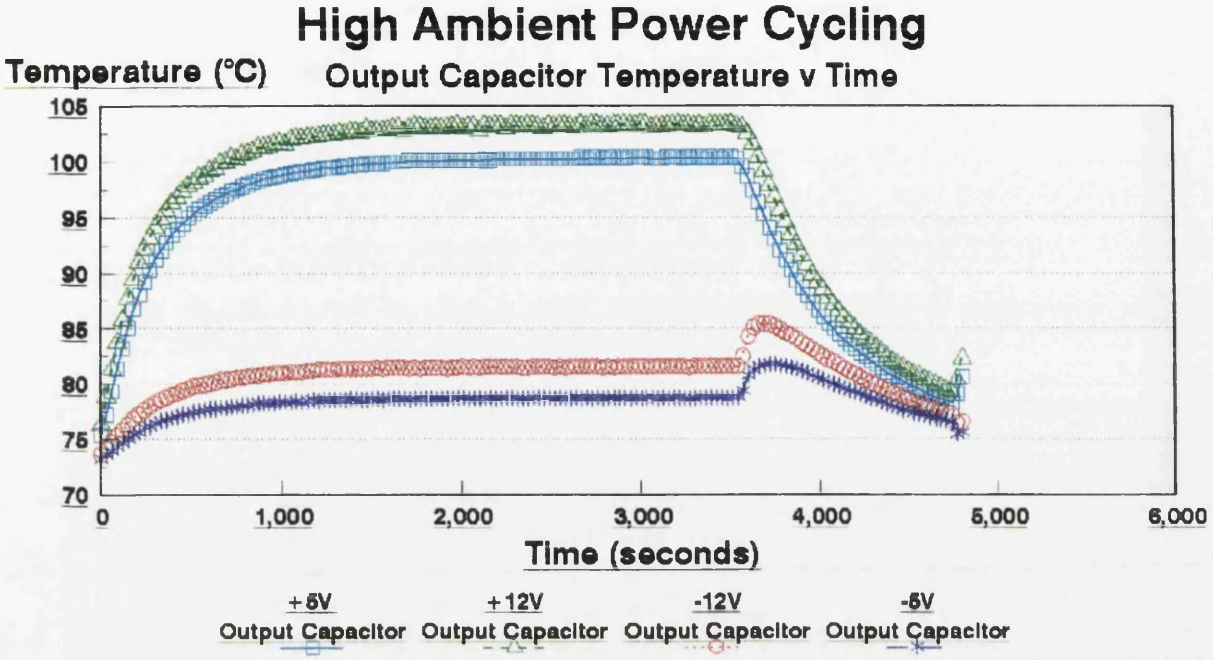


Figure 3.15 Capacitor Temperatures
High Ambient Power Cycling

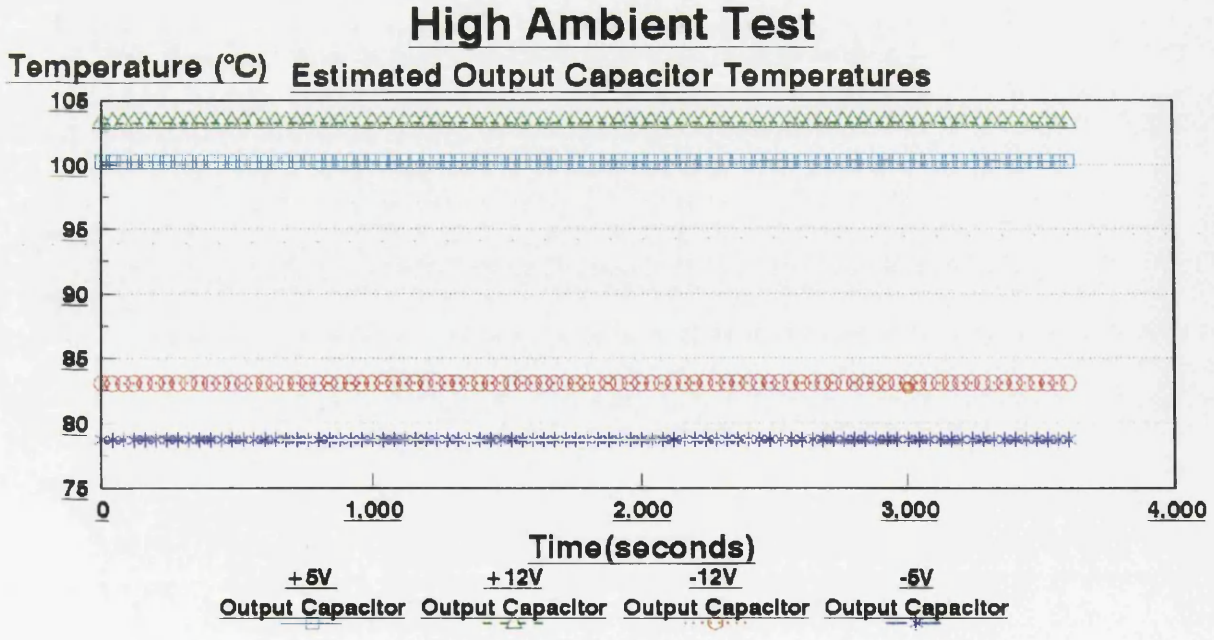


**Figure 3.16 Estimated Capacitor Temperatures
High Ambient Test**

Sample Acceleration Factor Calculations
High Ambient Power Cycling

Fraction of Total Period spent On: 60/75 = 0.8
Fraction of Total Period spent Off: 15/75 = 0.2

Arrhenius Acceleration Factor

$$A.F. = \exp(Ea/k)((1/Tf)-(1/Ts))$$

Tf = Tfield = Tlow; Ts = Tstress = Thigh

Whole Power Supply

Off: **Tf = 298.15 Ts = 348.15 Ea = 0.6 k = 8.6×10^{-5}**

On: **Tf = 308.15 Ts = 358.15 Ea = 0.6 k = 8.6×10^{-5}**

A.F.(off) = 28.47 A.F.(on) = 23.09

Weighted Average Acceleration Factor = 24.166

+12V Output Capacitor

Off: **Tf = 298.15 Ts = 349.55 Ea = 0.6 k = 8.6×10^{-5}**

On: **Tf = 326.55 Ts = 376.55 Ea = 0.6 k = 8.6×10^{-5}**

A.F.(off) = 30.52 A.F.(on) = 16.29

Weighted Average Acceleration Factor = 19.136

Figure 3.17
High Ambient Power Cycling Acceleration Factor

Conclusions

Although this is a topic which would seem to merit further investigation, from the point of view of possibly developing a definitive relationship between electrolytic capacitor parameters and required power supply test duration, it is possible at this stage to make the following observations:

1)Evaporation of electrolyte is a physical process, requiring an amount of energy which can be calculated.

2)A high ambient temperature causes, in any time period, a proportional amount of heat energy, to be passed to objects, e.g. electrolytic capacitors, in surroundings with such an ambient, thus influencing the temperature of those objects.

3) The higher the average temperature of the capacitors, over a period of time, the higher the amount of energy passed to the electrolyte of those capacitors.This results in faster evaporation, and capacitor degradation, thus accelerating the life of the capacitor and shortening the time required to test any units in which the electrolytic capacitors are being used to gauge the effectiveness of a life test.

4) The most effective use of high ambient temperature, as an accelerating stress, would seem to be a test which maximises the average temperature of the power supplies during its duration, while making sure that other components are not stressed beyond their design limits and therefore being possible sources of artificial and misleading failures.

Chapter 4-Cycle Based Tests

This chapter will document the evaluation of the processes listed below from the point of view of their effectiveness as accelerating stresses for life tests:

Power Cycling.

High Humidity.

Temperature Cycling.

Section 4.1:Power Cycling

This test came about as a result of interest in the effects of the laboratory practice of switching the power supplies on and off once every hour. (The power supplies spent 15 minutes off for every 45 minutes on). One of the reasons for such cycling is that the power supplies must, under test, be put through a minimum number of on/off cycles. The aim of the test was to discover how the length of a power supply's life was affected by the number of on/off cycles experienced in each hour.

The first requirement of this test was to discover the minimum length of on/off cycle which would subject the power supply to a realistic amonut of stress, typical of what it would experience in actual usage. For the purposes of reliability calculations power cycling is treated as a form of thermal cycling. This is because the current which flows through devices when power is applied to them causes the devices to heat up. When the power is removed the devices cool down to the temperature of the environment in which the power supply is placed.

By monitoring the power supply with a thermal imager as it heated up after switch on, and cooled down upon being switched off, minimum times for both transitions were determined. This process utilised the image analysis software of the computer controlled imagers which will supply extreme or statistical temperature values for part or all of the image captured.

As can be seen from Figure 4.1, which consists of the graphs for the aforementioned temperature transitions when the power supply was switched on and off, the temperature curve, in each case, begins with a steep ramp which has a duration of approximately two minutes. With power cycling being viewed as a form of temperature cycling this initial steep ramp seemed to correspond to the period of maximum stress. Consequently the observations of maximum and average temperature appeared to indicate that a minimum time of two minutes was required for each 'on', or 'off', transition.

However, since the purpose of a life test is for the power supplies to be on for as many hours as possible, it seemed reasonable for each power supply to spend a greater percentage of each cycle 'on' than it did 'off'. Hence, the minimum cycle time decided upon was five minutes of which the power supply would spend three minutes switched on and two minutes switched off.

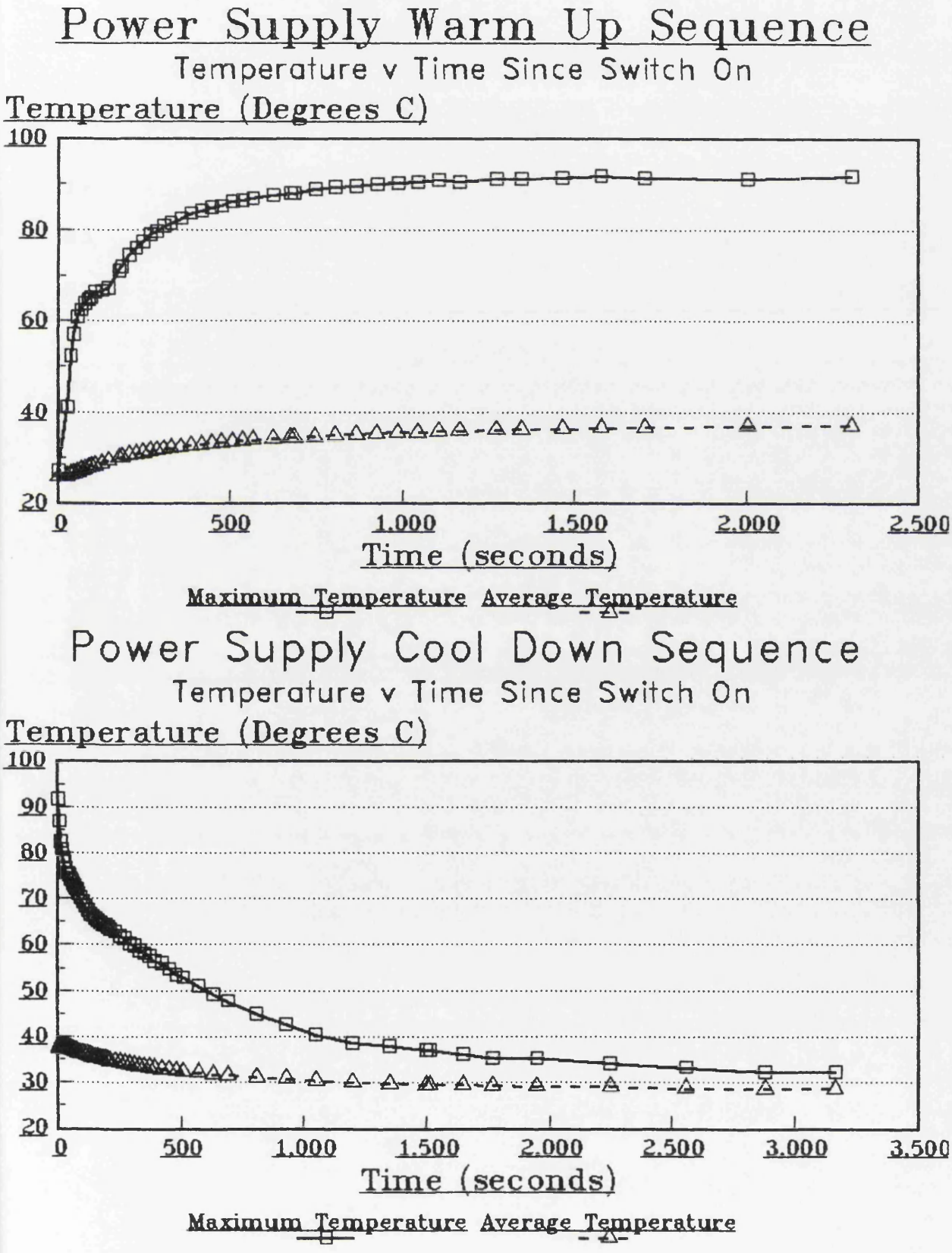


Figure 4.1 Power Supply Warm Up and Cool Down Sequences

At the time of this test there was available in the laboratory a batch of power supplies which had just undergone a full life test. It was decided to use these power supplies for the power cycling test for two main reasons:

1) The power supplies were 'tried and tested' under the same environmental conditions as those which would be present during the Power Cycling test so that any failures which occurred during the test would be directly attributable to power cycling.

2) The fact that these power supplies had already undergone a full life test as well as a 'burn in' meant that these power supplies were almost certainly at that stage in their life which corresponded to the constant failure rate section of the 'bathtub' curve. Consequently failures which occurred during the test would be representative of failures which might occur 'in the field'.

The Power Cycling test which actually took place involved five units being cycled at each of the following cycle times:

Cycle Number	Total Duration	On Time	Off Time	Cycles/ Hour
1	5 minutes	3 minutes	2 minutes	12
2	10 minutes	8 minutes	2 minutes	6
3	30 minutes	28 minutes	2 minutes	2
4	60 minutes	58 minutes	2 minutes	1

The same 'off' time was used for each cycle length because it was observed that no matter how long a power supply had been switched on there was always an initial fast temperature drop, with a duration in the region of 2 minutes, when it was switched off.

In an attempt to introduce an extra acceleration factor common to all the power supplies involved the test was carried out in an environmental chamber set at 60°C. The power supplies were connected to resistive loads which were set such that the combined output wattages for all the outputs of any one power supply amounted to 118W. Figure 4.2 gives an estimate of the resultant acceleration factor experienced by the power supplies based on the Modified Coffin-Manson equation (2.13)

In order that the test could run unattended a program was written which used an IEEE interface card to drive power relays which, in turn, switched the power supplies on and off by connecting them to and disconnecting them from the mains power.

Alternative Power Cycling Acceleration Factor

Modified Coffin–Manson Equation

$$A.F. = \left(\frac{dTs}{dTf}\right)^{1.9} \times \left(\frac{Ff}{Fs}\right)^{0.33} \times \exp(0.01(Ts-Tf))$$

Tlow field = 25°C Thigh field = 35°C dTf = 10°C

Tf = 35°C = 308.15K

Tlow stress = 25°C Thigh Stress = 70°C dTs=45°C

Ts = 70°C = 343.15

(Thigh (field) = Ton(field) = 35°C = 25°C + 10 = Ta + 10

so: Thigh (stress) = Ta(stress) + 10°C = 60°C +10°C = 70°C)

Ff = 1/day : Fs = 1/hour = 24/day

Acceleration Factor

$$A.F. = \left(\frac{45}{10}\right)^{1.9} X \left(\frac{1}{24}\right)^{0.33} X \quad \exp(0.01(343.15-308.15))$$

= 17.4 X 0.35 X exp(0.35) = 8.64

Acceleration Factor = 8.64

Figure 4.2 Coffin_Manson Acceleration Factor For Power Cycling

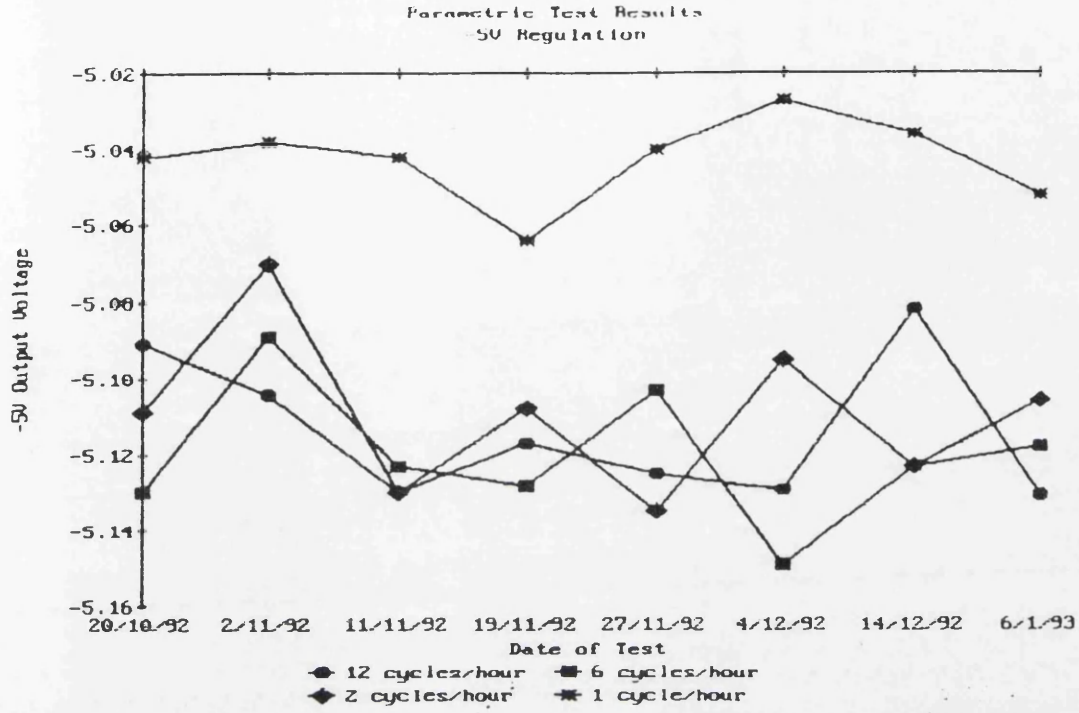
A scanner which reads in sequence the voltage of its inputs, which can number up to 30, was used to monitor the +5V outputs of each power supply every time the five minute cycle was started. Theoretically this gave any failure times to within five minutes. Every time the outputs were read the results were fed to a data file which was stored on computer.

At various intervals, usually weekly, the test was stopped, at the point in the overall cycle when ALL the power supplies were switched off. This allowed one power supply from each group (cycle duration) to be extracted for the purposes of undergoing various parametric tests; the results of which were logged and stored in a database of results.

The purpose of the parametric tests was to find out if any of the measurements made on the power supplies follwed a trend or gave indication of iminent failure. Figure 4.3 shows a typical database entry and Figures 4.4 show the weekly results of the parametric tests.

Date:	16/2/93
Power Supply No.	
Test Name:	
Test Strength:	82
+12 V Regulation (Volts):	11.2
+5V Regulation (Volts):	5.03
−5V Regulation (Volts):	−5.1
−12V Regulation (Volts):	−11.95
+12V Ripple (mVolts):	105
+5V Ripple (mVolts):	80
−5V Ripple (mVolts):	
−12 V Ripple (mVolts):	
+12 V Step Response (Volts):	
Change Frequency (Hz):	
Switching Frequency (kHz):	56
Efficiency (%):	74.4
Common Mode Noise (mVolts):	
Days Under Test:	0

Figure 4.3 Power Cycling Tests
Typical Database Entry



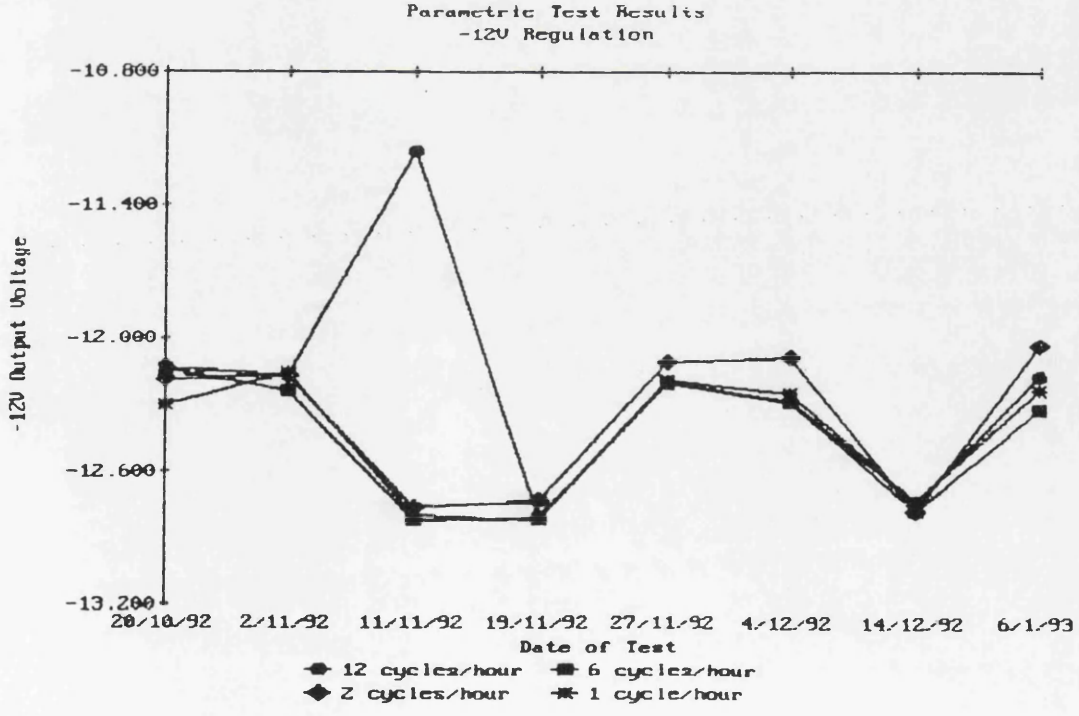
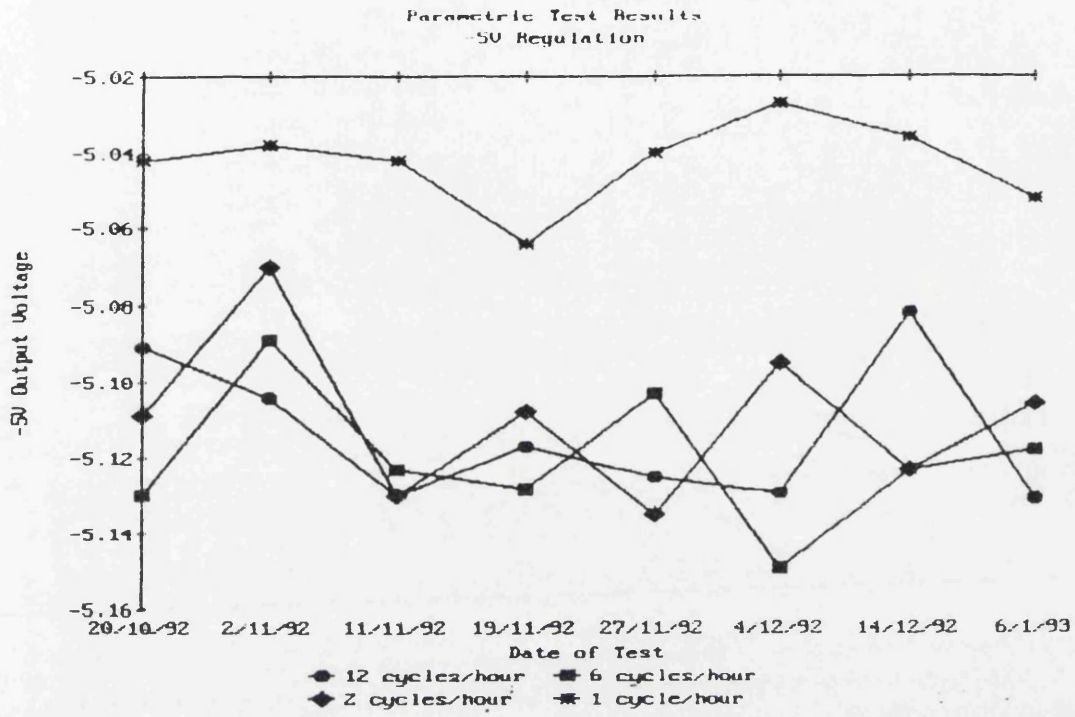


Figure 4.4

Power Cycling Parametric Test Results



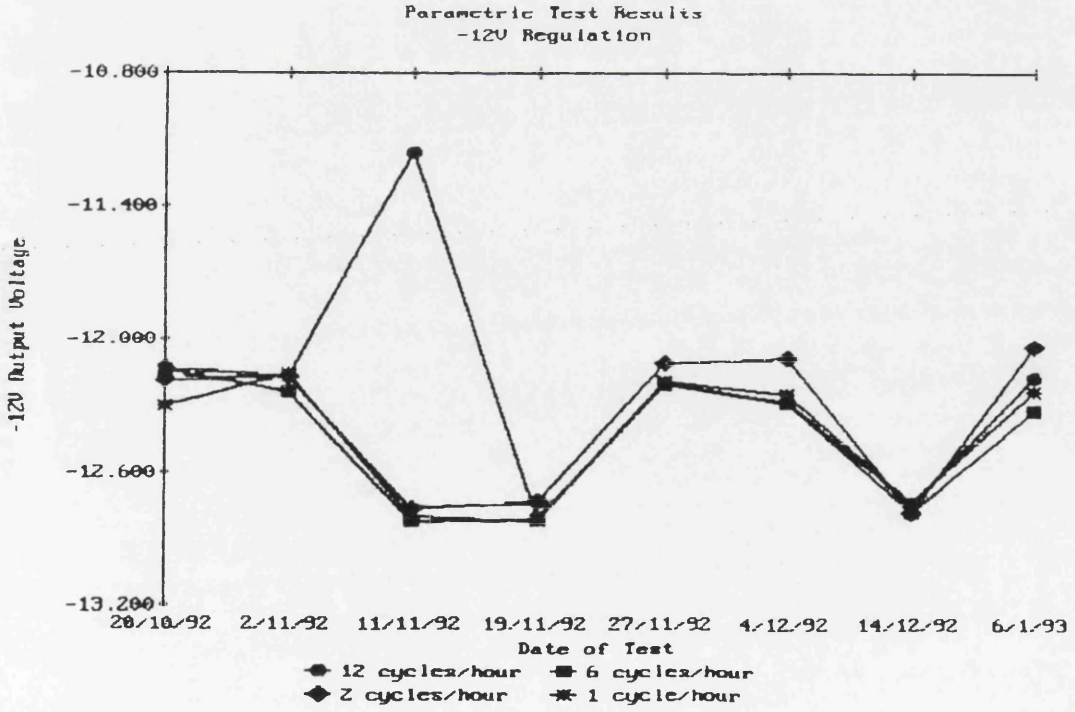
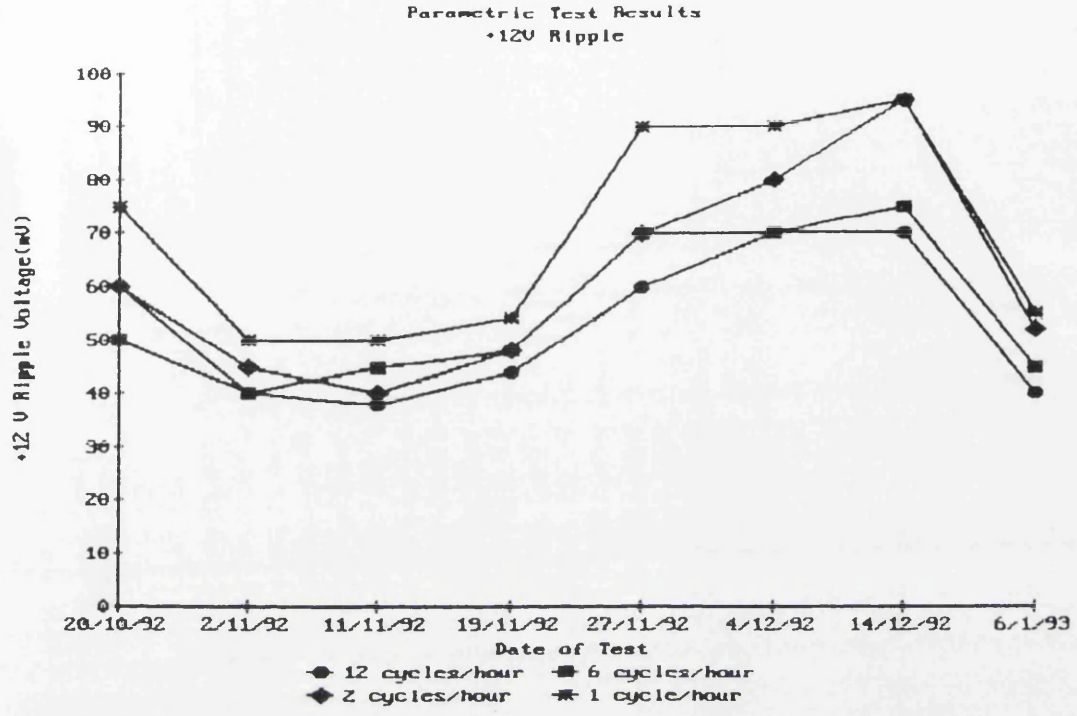


Figure 4.4

Power Cycling Parametric Test Results



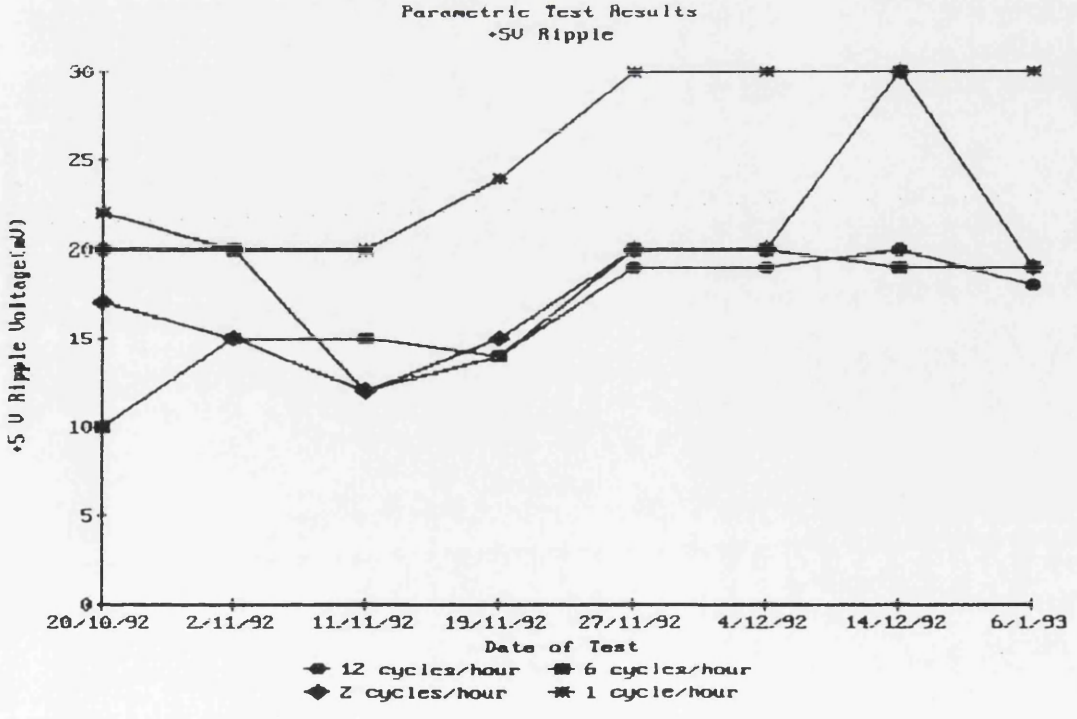
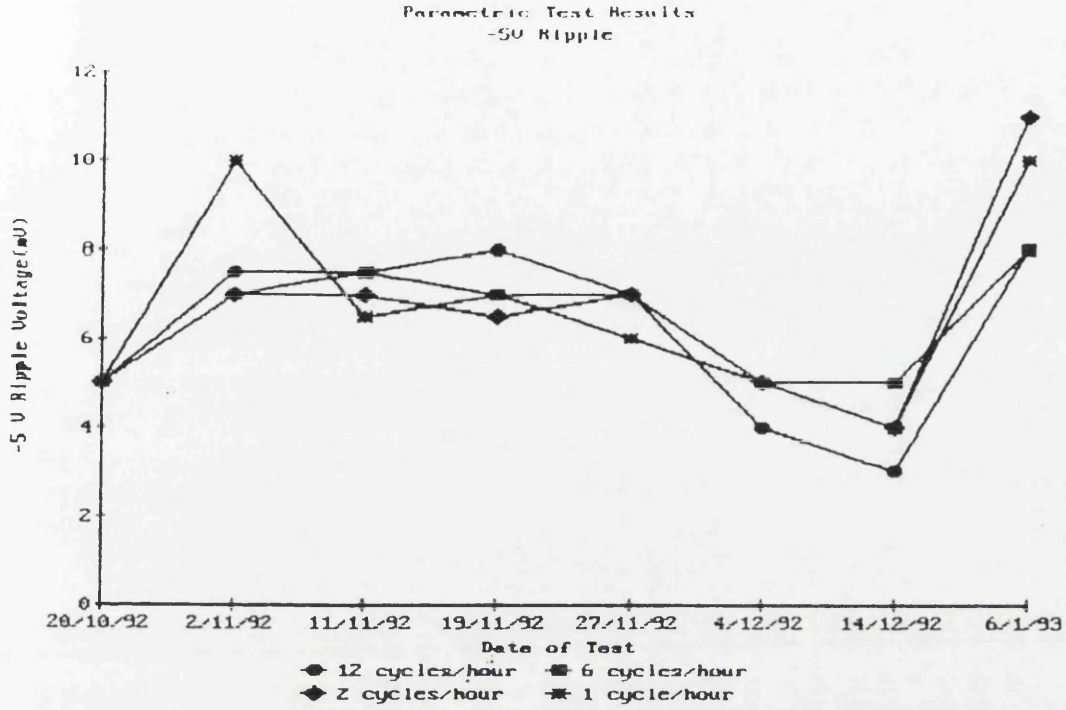


Figure 4.4

Power Cycling Parametric Test Results



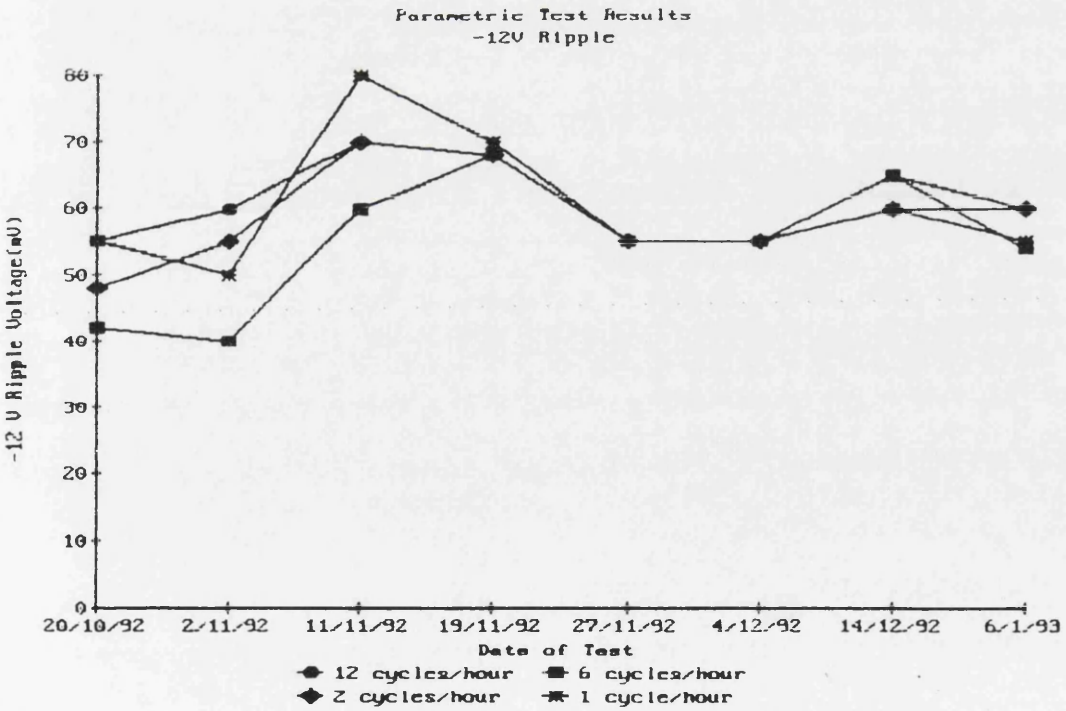


Figure 4.4

Power Cycling Parametric Test Results

Results

It had been hoped that this test would produce a trend of failures which would identify one particular cycling frequency as producing more failures in a shorter time. The test was run for approximately three months, which is the length of a standard life test. The actual number of hours involved amounted to 1355 and in this time the test produced two failures.

Unit 41 which was being cycled twice per hour failed after 314 hours.

Unit 74 failed after 1355 hours and was being cycled six times per hour.

Attempts to find the primary cause of failure of these units were inconclusive.

The only parametric result which gives any indication of following a trend is the +5V ripple voltage which in all of the units seems to increase at first and then level off. The final value of +5V ripple voltage for the unit undergoing 1 cycle per hour is considerably higher than all the others (13mV higher). Whereas at the start of the test there was a difference of only 2mV between the 1 cycle/hour unit and 12 cycle/hour unit.

Conclusions

Due to the low number of failures which occurred it is impossible to single out any one cycling frequency as being particularly effective. It had been hoped that one of the groups of power supplies would have produced a number of failures and if this had happened it would have suggested that future life tests should employ cycling at that rate.

Instead of this the results would seem to suggest that the current practice of the power supplies spending 45 minutes of each hour on and 15 minutes off is as good as any and in fact means that the power supplies spend a greater percentage of the test on than they would do if the 12 cycles/hour or 6 cycles/hour frequencies were used. Additionally the Modified Coffin-Manson equation indicates that as cycling frequency is increased the temperature cycling acceleration factor decreases despite the fact that a higher cycling frequency might reasonably be expected to be more stressful, and hence give rise to a greater acceleration factor, than cycling less often.

The only possible change which the results seem to suggest is that the 'off' time of 15 minutes could be significantly reduced to as little as 2 minutes which would been that the power supplies would spend 58 minutes of each hour on (96%) instead of 45 minutes (75%). Theoretically life tests could then take 78% of the time they do at present.

It is important to note however that each type power supply to be life tested should be investigated to determine the minimum time required for it to cool down. Since it is standard practice to examine each type of power supply with a thermal imager, to check among other things for unreasonably hot components, such a check of warm up and cool down times would not add significantly to the total time required to approve and life test a sample of power supplies.

Section 4.2:The Effect of Increased Humidity

As mentioned in Chapter Two increased humidity is a commonly used means of accelerating life tests. It is used primarily when life testing integrated circuits with plastic packages. The failure mechanism most often related to moisture is corrosion due to moisture entering components.

Absolute humidity is the amount of moisture the air is capable of holding. Figure 4.5 shows how absolute humidity varies with temperature. As air temperature increases so does the capacity of the air to hold moisture. Relative Humidity is the percentage of moisture in the air compared with the maximum possible amount of moisture in the air for that particular air temperature. When the air is holding all the water it can relative humidity is 100%. This condition is known as the Dew Point and results in condensation. It is important to remember that rainfall comes about as a result of clouds, groups of condensed water particles, forming at a height where the relative humidity is 100%.(Whenenough particles have collected to cause the mass of the cloud to be more than the air can support rainfall occurs) . However, the temperature at cloud level, which is say 1000 M, is much lower than the temperature at ground level. So even when it is raining the relative humidity at ground level is not 100%.

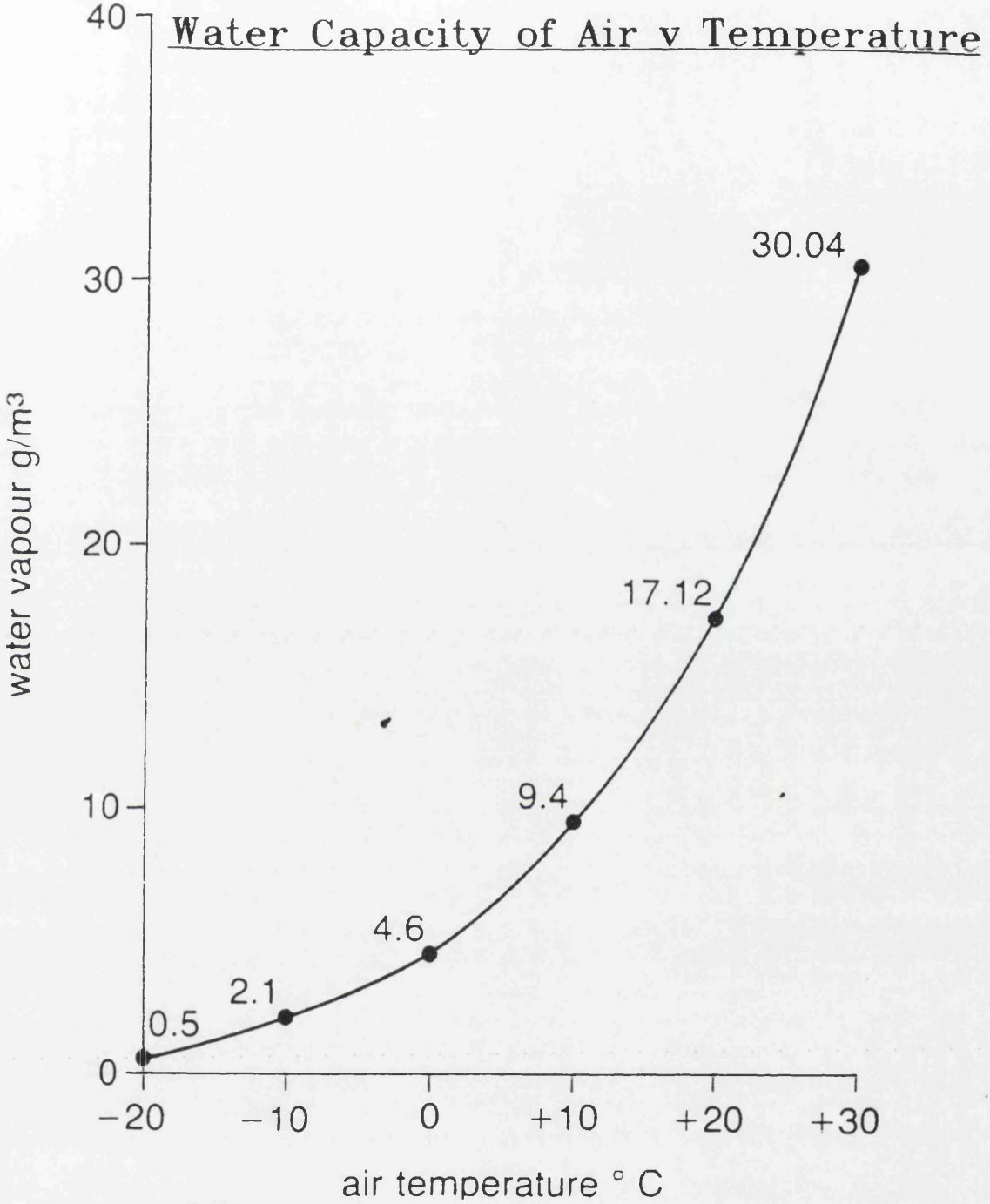


Figure 4.5

Water Capacity of Air Versus Temperature

Sample Calculation

Temperature at Ground level: 7°C

Lapse rate: 6.5°C/1000M

Temperature at cloud level 0.5°C

Absolute Humidity at Cloud level: 5g/m3

Absolute Humidity at Ground level: 8g/m3

Relative humidity at ground level: 5/8 = 62.5%

Rainfall when the temperature at sea level is 25°C would correspond to a relative humidity at sea level in the region of 71%

The power supplies tested in the lab are required to operate in relative humidities of up to 80%.

The primary motivation for carrying out this test was a desire to find out what, if any, would be the effect of running the power supplies in a higher relative humidity than that which they would normally encounter.

Working from the 80% relative humidity requirement laid down in the specification it was decided initially to run four power supplies each at relative humidities of 82%, 85%, 90% and 95%. Four seemed the most reasonable number of power supplies to place in the environmental chamber which would be used.

The program which was used to control the on/off cycling during the power cycling test was adapted for the purposes of this test.

The initial four power supplies were operated on a cycle consisting of 58 minutes on, 2 minutes off at an air temperature of 50°C and a relative humidity of 82%. The loads at the outputs of the power supplies amounted to a total of 118W per power supply. i.e. the maximum rated output for those power supplies. The input voltage supplied to the power supplies was 110V. Figure 4.6 gives an estimate for the associated acceleration factor based on Equation 2.12.

Humidity Acceleration Factor (A.F.)

Sim Larson Equation

$$A.F. = \exp(0.00044) * (Rhstress^2 - Rhuse^2)$$

Best Case Scenario

Rhstress = %Relative humidity at stress = 95%

Rhuse = %Relative Humidity in field = 80%

A.F. = exp(0.00044) * (9025 - 6400)

= 1 * (2625) = 2625

Worst Case Scenario

Rhstress = %Relative humidity at stress = 82%

Rhuse = %Relative Humidity in field = 80%

A.F. = exp(0.00044) * (6724 - 6400)

= 1 * (324) = 324

Figure 4.6
Humidity Acceleration Factor

It quickly became apparent that the power supplies were producing more heat in the chamber than the chamber could succesfully dissipate. Consequently the temperature in the chamber tended to rise to the point at which the maximum internal temperature for the chamber was reached and the chamber shut down.

In an attempt to circumvent this the duty cycle of the power supplies were reduced until they were spending only 45 minutes of each hour on and spending the other 15 minutes off. Despite this the internal chamber temperature continued to cause the chamber to shut down.

Eventually the output loads of the power supplies were reduced so that each output was attached to its minimum rated load.

As a result of this the chamber now ran without cutting out but the temperature tended to remain in the vicinity of 60°C to 70°C.

After 1 week the power supplies were extracted from the test and put through a series of parametric tests on the bench. In order to ensure that the power supplies would still operate from voltages in the 220V range the power supplies were given an input voltage of 240V. One power supply failed immediately. On examination it was discovered that the input fuse of the power supply was open circuit. When the fuse was replaced and the power supply switched on once more the input smoothing capacitors also known as the bulk caps underwent catastrophic failure rendering the power supply unsafe for any further investigation work.

This test ran at 82% relative humidity from 25/3/1993 to 5/4/1993 and during that time the test was actually in progress for 114 hours. At this point, having established that the power supplies would operate at 82% relative humidity it was decided to test another four power supplies in at 95% relative humidity. It was reasoned that if significant failures occurred at this very stressful condition then more precise investigations would be justified at the intervening values of 85% relative humidity and 90% relative humidity. If nothing significant happened at 95% relative humidity then the test would be abandoned.

Again the power supplies were extracted for parametric testing after 1 week and again one unit failed immediately due to a blown input fuse. This time the fuse was replaced with a quick blow fuse and the cause of failure was eventually traced to the resistors forming the potential divider which determined which input voltage was being used. One of these resistors was found to be open circuit

This resistor was extracted and examined using standard and electron microscopy. Photographs which resulted from this appear in Figure 4.7. Initial examination seemed to suggest the possibility that the leads of the resistor had become detached from the internal wire. It was later discovered that the same problem had occurred in units received by the production line. On that occasion X-rays of the resistors involved revealed that the internal wire had broken.

The test which was carried out at 95% relative humidity ran between 13/4/1993 and 11/6/1993. The only failure which occurred took place after the first week of testing. During this period the power supplies spent a total of 336 hours at test conditions. Due to the absence of further failures at what was a very high level of stress, and due to the facilities being required for another test it was decided to abandon the investigation at that point.

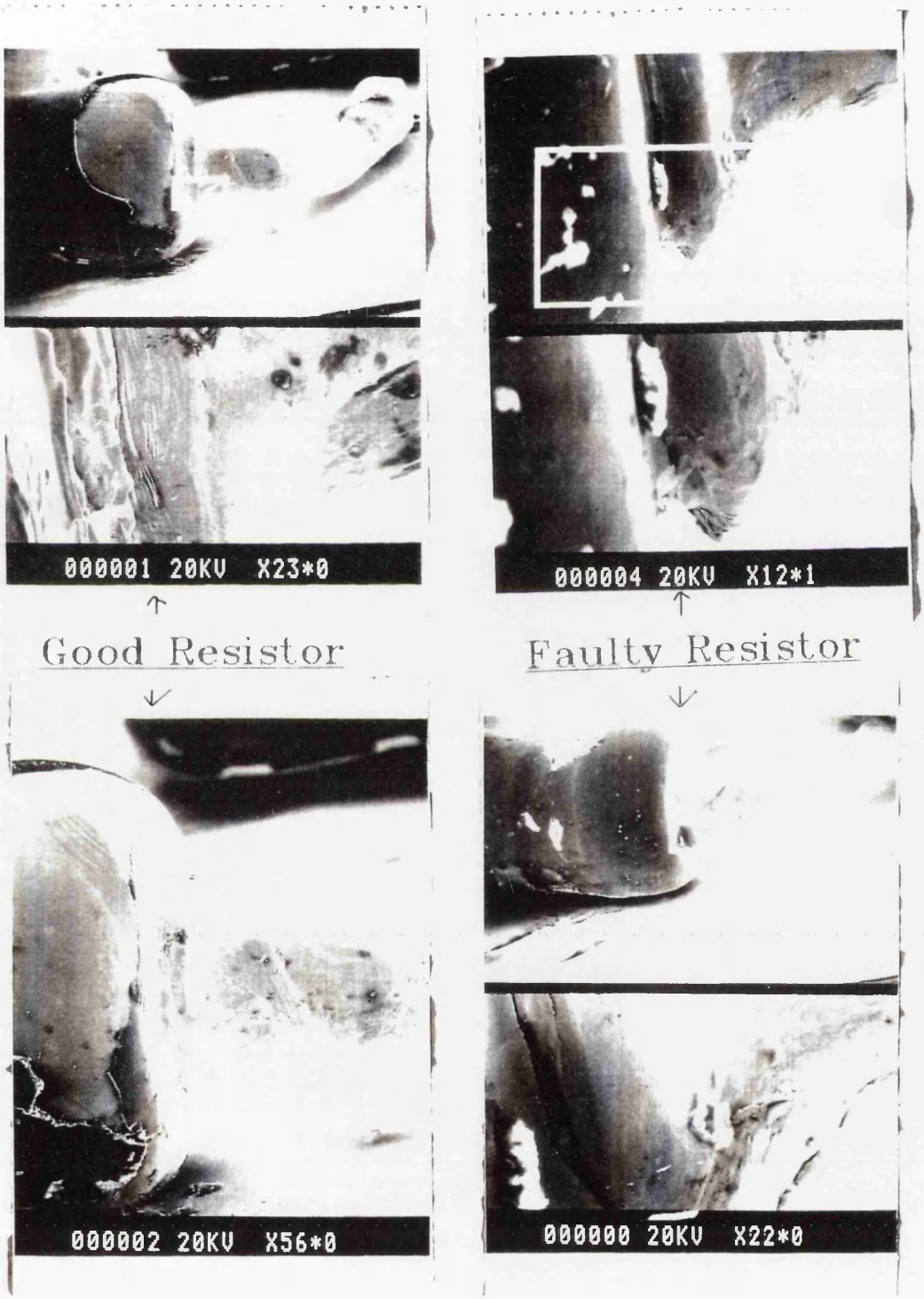


Figure 4.7

Good and Damaged (Open Circuit) Resistors

Conclusions

Despite the two failures which ocurred there is no real indication that this test would bring any benefits in terms of shortening the time required for life testing. There are three main reasons for this.

1) The reduction in output load caused a significant drop in the temperature of the power supplies' components So even though the acceleration factor due to humidity was increased the acceleration factor due to temperature was decreased due to the lower load (see chapter 5).

2) The two failures which did occur came about as a result of a failure mode which also caused failures in power supplies undergoing routine testing on the production line. There is nothing to suggest that the power supplies which failed under the humidity conditions above would not have failed under normal operating conditions. In fact a failure of the type described is more likely to be caused by expansion and contraction due to changes in temperature than it is to be caused by increased humidity levels.

3) The facilities do not exist in the lab for large scale testing of this type and the above results do not seem to support investment in such facilities. The chamber which was used was as big as any of the other chambers capable of producing conditions of controlled relative humidity and as mentioned above even four power supplies generated more heat than the chamber could ventilate and consequently caused the internal temperature to rise. A typical life test would involve twenty or more power supplies so the chamber would have to be much bigger but it would also have to dissipate more heat so it is likely that the same problems would be encountered. Additionally there would have to be some means of providing the chamber with its own water supply and recycling any water which the chamber disposed of. The chamber involved in the test used 75% of the water in it's supply tank every day and consequently could not be left to run unsupervised over the weekend. Consequently 2 days out of every 7 were lost.

Due to the specification requirement that the power supplies should be able to operate in environments with up to 80% relative humidity it is advisable to test at least two of each type of power supply in such an environment to ensure that they can meet such a requirement.

Section 4.3:Thermal Cycling

Thermal Cycling figures significantly in the majority of industrial burn-in processes. It has proved invaluable on many occasions for detecting weak components before the products containing them were sold. It is also the principal test for revealing weak solder joints.

It does this by making use of the fact that changes in heat will lead to expansion and contraction of the various materials in the assembly at different rates. Two adjacent materials e.g. a printed circuit board and a component lead, expanding at different rates places mechanical strain on solder joints and will eventually cause bad joints to crack. Such stress could also, therefore, accelerate the degradation of any components with structural defects i.e. accelerate their life and cause them to fail in a shorter time than would be required were the component subjected to only the stress associated with normal usage. The breakdown of the component would in turn cause failure of the complete electronic assembly, in this case the power supply being tested.

The Temperature Cycling test used was heavily influenced by the results of the investigations into the effects of elevated ambient temperature. Additionally the approach adopted has its origins in the events surrounding the humidity tests documented above. Specifically, it was decided to begin the test with the severest cycle possible using the available equipment. However the severity of the cycle took into account the conditions in which the power supplies had been seen to operate as well the conditions in which the specification required them to be able to operate.

This investigation also involved four power supplies. A environmental chamber which could be controlled by computer was selected and four spare power supplies, of the same type as would be used in the actual test were placed in the chamber. This was done for the purpose of deciding on the actual cycle to be used for the test, the codes which would have to be sent to chamber and the times at which the codes would have to be sent.

Because of the manner in which the power supplies had affected the temperature inside the chanber during the humidity test it was reasonable to assume that they would do the same in this test and would therefore influence the time taken by the chamber to change between extremes of temperature. Since these times would in turn dictate the cycle profile the initial planning of the cycle had to be carried out by observing how the chamber, with the power supplies operating as they would during the test responded to the commands sent by the computer to the chamber.

The cycle profile was eventually decided upon and is shown in Figure 4.8. A program was written to take the chamber and power supplies through this profile on an hourly basis. A portable data-logger was used to monitor at hourly intervals the +5V outputs of the power supplies in the test.

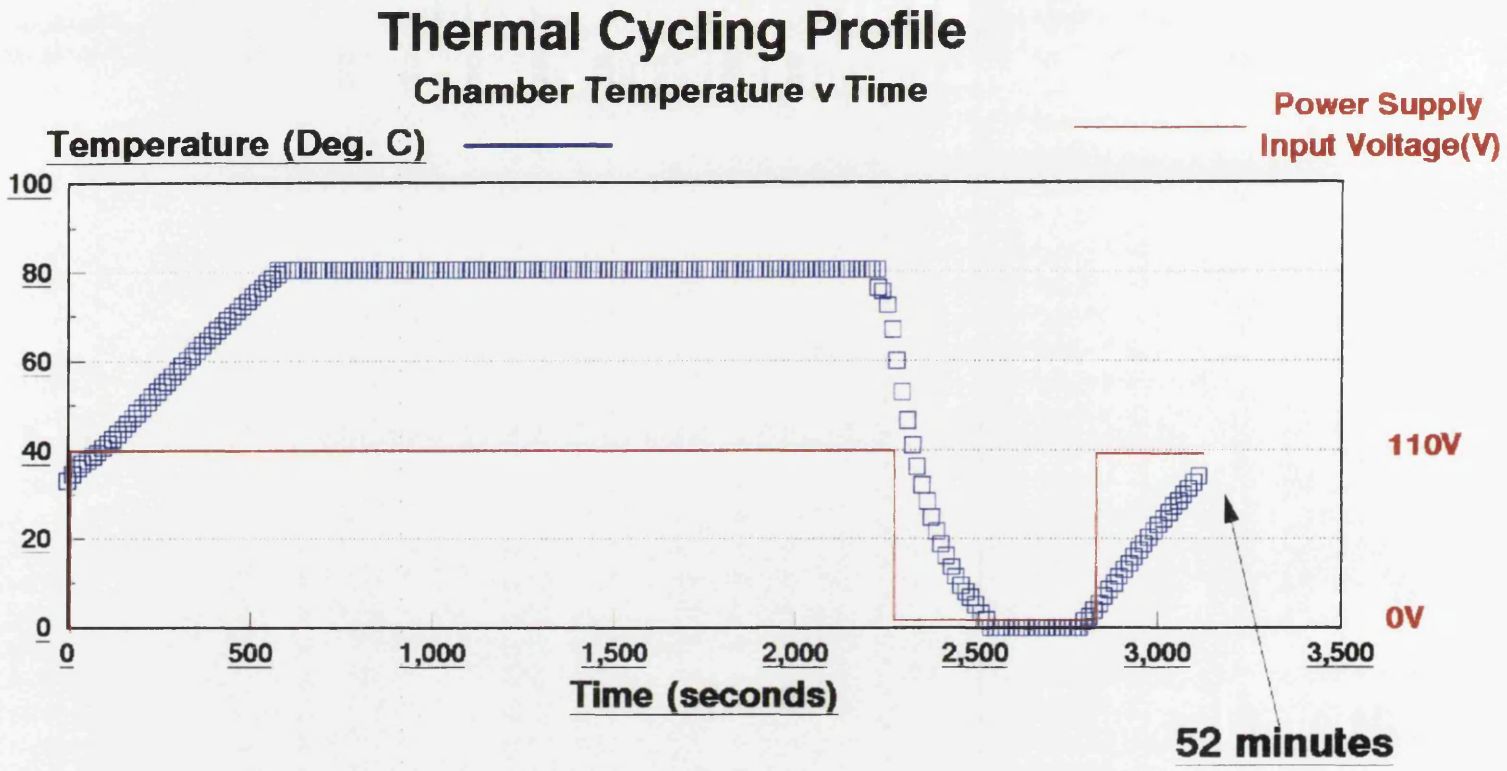


Figure 4.8
Thermal Cycling Chamber Temperature Profile

The first test ran in all for 600 hours at the end of which there was some evidence of capacitor degradation. The capacitors involved were examined in the same way as those taken from power supplies which had undergone the elevated ambient test, i.e. they were placed in a power supply with known output ripple voltages in order to see how these measurements changed when the relevant capacitors changed. The results of this comparison appear in Figure 4.9

In light of this the test was repeated. On the second occasion, for the purposes of more closely monitoring the effect of the test on the power supplies involved, all four power supplies were extracted on a weekly basis and parametric tests were performed the results of which appear in Figure 4.10. On these occasions the capacitors were also examined for the changes in physical appearance which had been found to accompany capacitor degradation.

Thermal Cycling Test
Measurements on Capacitors
Capacitance(μF)

	Nominal	Untested	Unit 1	Unit 2
+12V O/P Capacitor	470	438.0	113.8	430.0
+5V O/P Capacitor	470	447.0	385.0	442.0
-5V O/P Capacitor	47	44.3	36.7	43.8
-12V O/P Capacitor	100	98.2	91.2	92.5
Input Capacitor	470	412.0	442.0	456.0

Thermal Cycling Test
Measurements on Capacitors
Equivalent Series Resistance (milliohms)

	Untested	Unit 1	Unit 2
+12V O/P Capacitor	178	7,480	275
+5V O/P Capacitor	174	775	231
-5V O/P Capacitor	3,170	6,300	4,360
-12V O/P Capacitor	1,040	1,110	1,510
Input Capacitor	191	201	163

Figure 4.9
Thermal Cycling Capacitor Comparisons

Temperature Cycling

Output Regulation

Output Voltage (V) v Hours Under Test

	Unit 1 +12V	Unit 2 +12V	Unit 3 +12V	Unit 4 +12V	Unit 1 +5V	Unit 2 +5V	Unit 3 +5V	Unit 4 +5V	Unit 1 -5V	Unit 2 -5V	Unit 3 -5V	Unit 4 -5V	Unit 1 -12V	Unit 2 -12V	Unit 3 -12V	Unit 4 -12V
21.25	12.09	11.88	11.83	11.92	5.10	5.03	5.04	5.04	(5.10)	(5.01)	(5.00)	(5.11)	(12.34)	(12.19)	(12.13)	(12.11)
85	12.09	11.88	11.82	11.82	5.10	5.06	5.03	5.04	(5.10)	(5.00)	(5.01)	(5.10)	(12.34)	(12.18)	(12.13)	(12.11)
200.6	12.06	11.91	11.85	11.83	5.10	5.03	5.02	5.02	(5.09)	(4.99)	(5.01)	(5.07)	(12.35)	(12.12)	(12.13)	(12.07)
323.85	12.09	11.85	11.91	11.83	5.09	5.02	5.03	5.03	(5.10)	(5.00)	(4.99)	(5.10)	(12.33)	(12.12)	(12.17)	(12.10)
447.1	12.04	11.82	11.89	11.83	5.09	5.03	5.03	5.02	(5.10)	(4.99)	(4.97)	(5.10)	(12.32)	(12.09)	(12.16)	(12.04)
595	12.26	11.81	11.88	11.87	5.06	5.03	5.03	4.99	(5.09)	(5.01)	(4.98)	(5.09)	(12.71)	(12.14)	(12.19)	(12.52)

Thermal Cycling

Output Ripple Voltage

Ripple Voltage (millivolts) v Hours Under Test

	Unit 1 +12V	Unit 2 +12V	Unit 3 +12V	Unit 4 +12V	Unit 1 +5V	Unit 2 +5V	Unit 3 +5V	Unit 4 +5V	Unit 1 -5V	Unit 2 -5V	Unit 3 -5V	Unit 4 -5V	Unit 1 -12V	Unit 2 -12V	Unit 3 -12V	Unit 4 -12V
24	28	40	38	21	12	5	8	8	15	12.0	8	6	37	40	44	27
192	28	36	36	30	6	6	8	8	10	12.0	10	7	38	40	36	27
336	28	37	36	29	6	7	6	9	14	11.5	10	6	40	38	34	26
504	28	38	34	30	5	6	8	9	14	11.0	9	6	38	38	37	28
672	29	36	36	31	7	6	6	7	14	14.0	9	5	34	35	34	24
864	31	40	36	30	4	8	7	10	13	12.0	10	8	35	35	36	36

Figure 4.10
Results Of Regulation and Ripple Measurements

While the power supplies were undergoing Thermal Cycling thermocouples were attached to a selection of the capacitors, since these were the components around which the test had, primarily, been structured, in an attempt to discover how the temperatures of these components changed during the test. The graphs which were composed using these figures appear in Figure 4.11. Figure 4.12 uses these results, in conjunction with the Modified Coffin-Manson equation to give an estimate of the acceleration factor due to Thermal Cycling.

Two of the power supplies involved in the second test failed inexplicably; but their failure corresponded to a dip in the local mains supply which damaged the A.C. source supplying them. Prior to this, however, there was again evidence of capacitor degradation, reflected in the ripple voltage recorded on the +12V channels and the physical appearance of one of the capacitors as shown in the photograph in Figure 4.13.

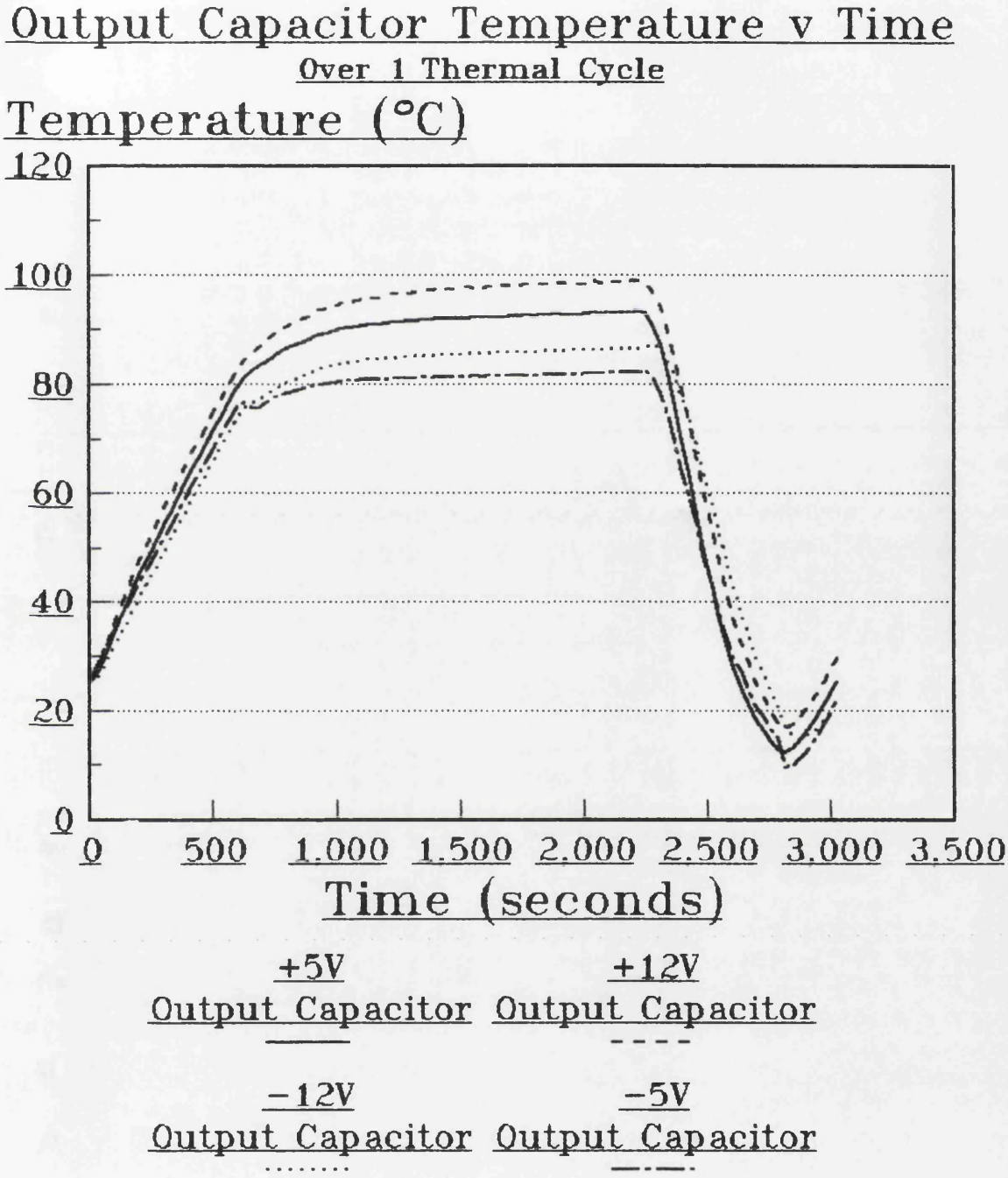


Figure 4.11
Capacitor Temperatures During Thermal Cycling

Sample Acceleration Factor Calculations
Thermal Cycling Test

Modified Coffin-Manson Equation

$$A.F. = \left(\frac{dTs}{dTf}\right)^{1.9} \times \left(\frac{Ff}{Fs}\right)^{0.33} \times \exp(0.01(Ts-Tf))$$

Whole Power Supply

Stress Conditions: On Temperature = 85 degrees; Off Temperature = 0 degrees
Cycle Frequency = 1 per 51 minutes

dTs = 85 degrees; Fs = 1/51; Ts = 85 degrees

Field Conditions:On Temperature = 35 degrees; Off Temperature = 25 degrees
Cycle Frequency = 1 per 24 hours = 1 per 1440 minutes

dTf = 10 degrees; Ff = 1/1440; Tf = 35 degrees

$$A.F. = \left(\frac{85}{10}\right)^{1.9} \times \left(\frac{51}{1440}\right)^{0.33} \times \exp(0.01(85-35))$$

$$= 58.33 \times 0.332 \times 1.65 = \boxed{31.95}$$

+12V Output Capacitor

Stress Conditions: On Temperature = 99 degrees; Off Temperature = 16.7 deg.
Cycle Frequency = 1 per 51 minutes

dTs = 72.3 degrees; Fs = 1/51; Ts = 99

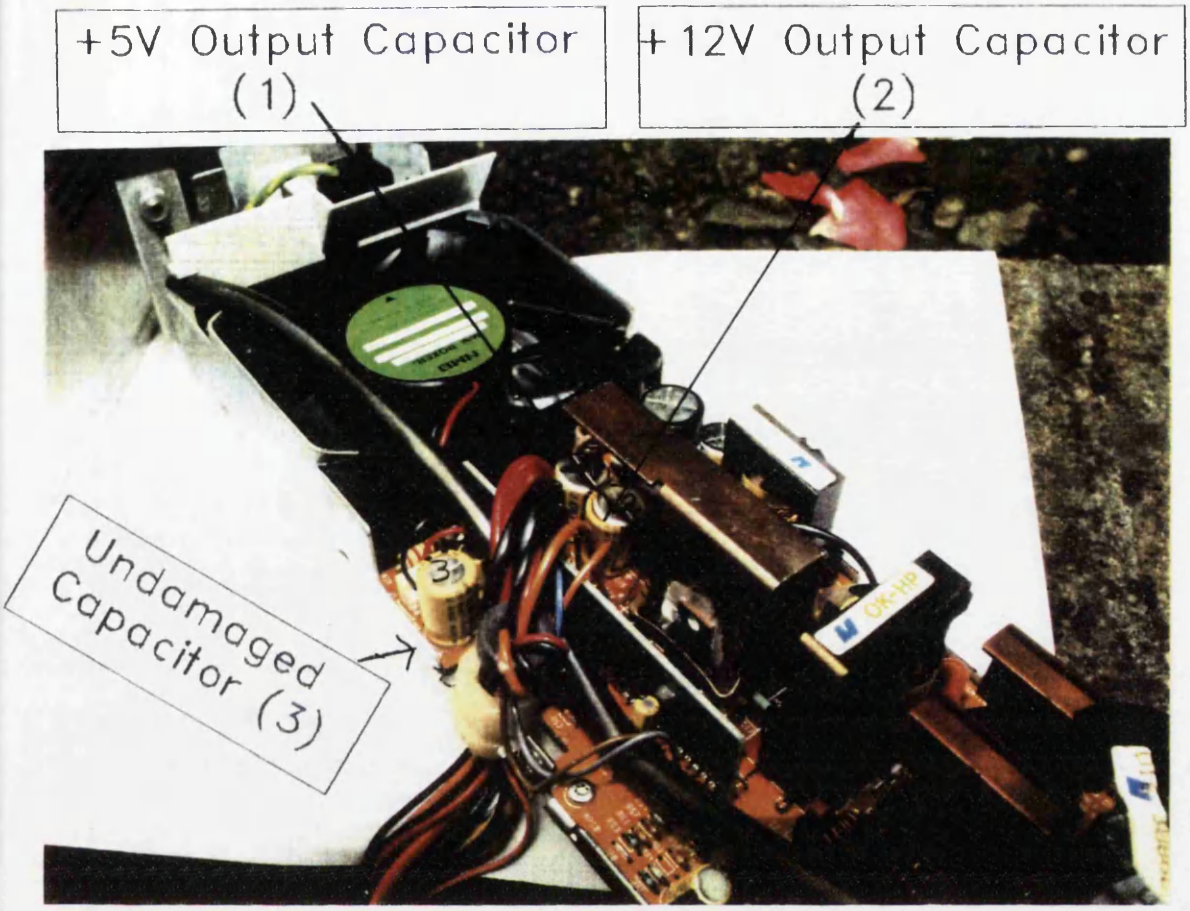
Field Conditions:On Temperature = 47 degrees; Off Temperature = 25 degrees
Cycle Frequency = 1 per 24 hours = 1 per 1440 minutes

dTf = 22 degrees; Ff = 1/1440; Tf = 47 degrees

$$A.F. = \left(\frac{72.3}{10}\right)^{1.9} \times \left(\frac{51}{1440}\right)^{0.33} \times \exp(0.01(99-47))$$

$$= 42.89 \times 0.332 \times 1.68 = \boxed{23.92}$$

Figure 4.12: Thermal Cycling Acceleration Factors



The +12V and +5V output capacitors both show signs of degradation however it is more apparent on the +12V capacitor which has a higher operating temperature.

Figure 4.7

Capacitor Degradation During Thermal Cycling

Conclusions

The capacitor degradation which occurred appears to justify the initial decision to investigate thermal cycling as a means of accelerating life tests.

When this test was originally planned the intention had been, if the thermal cycling proved to be effective, to investigate how dependent that effectiveness was on the rate of change of temperature during the sections in which the temperature was increasing or decreasing and the temperatures at which the power supply spent large parts of the cycle. Any further investigations into Thermal Cycling would have taken this form. Unfortunately, due to time constraints no other investigations were possible.

Chapter 5-The Effect of Electrical Stresses

The reasons for these tests were twofold. Primarily they were carried out in an attempt to discover the best electrical conditions under which to run the long term tests such as high ambient tests and thermal cycling. Additionally it was hoped that a combination of electrical parameters could be found which would cause the power supplies on the bench to experience the same temperatures as those in thermal chambers.

For the latter reason investigations were also carried out into the effect of interfering with the natural cooling processes of the power supplies by covering up cooling fans and ventilation slats.

Since the power supplies are electrical devices it was decided to investigate the effect of varying the electrical conditions under which they operated. There two main ways of doing this:

1) Varying the Input Voltage. Since the power supplies are expected to work on two ranges of input voltage (90V to 137V and 180V to 265V) it was decided to see which voltages within these ranges corresponded to the most stressful operating conditions for the power supply.

2) Varying the Output Loads. Each output channel of the power supply is expected to be able to supply specified values of voltage and current to the product in which the power supply is installed. Even though the voltage of each channel will remain the same the current will change according to the value of the load on that channel. In the case of the power supplies used for these tests the combined loads on the four channels should demand up to 118W at any one time. It is however possible to increase the current of each channel beyond that which will give a total output power of 118W although there is an upper limit to such an increase. By observing the effects of varying the output loads of the various channels it was hoped to find a load combination which would increase the operating stress on the power supply without causing permanent damage.

Section 5.1: The Effect of Varying Input Voltage

As a prelude to the tests documented below several power supplies were operated at an input voltage of 270V with the output loads set at the maximum values under which the power supply would operate without being shut down by the current limiting circuitry.

The activity had as its consequence the damage of several FETs. In order to find the primary failure mode of these devices they were examined by an electron microscope. This inspection revealed that the FETs had failed due to electrical damage rather than the heat caused by the electrical stress.

Figure 5.1 consists of photographs of a damaged and an undamaged FET. The scarring on the semiconductor surface of the damaged FET, which is most pronounced in the vicinity of the electrical contacts has been seen in the past on FETs known to have failed due to electrical damage. Thermal damage shows up as discolouration of the semiconductor layer.

Although the conditions which brought about the damage reported above were too severe to be of use in an actual life test they did serve to indicate that certain combinations of Input Voltage and Output Load did stress the power supply and this led to more quantitaive investigations of the stress caused by a variety of these combinations.

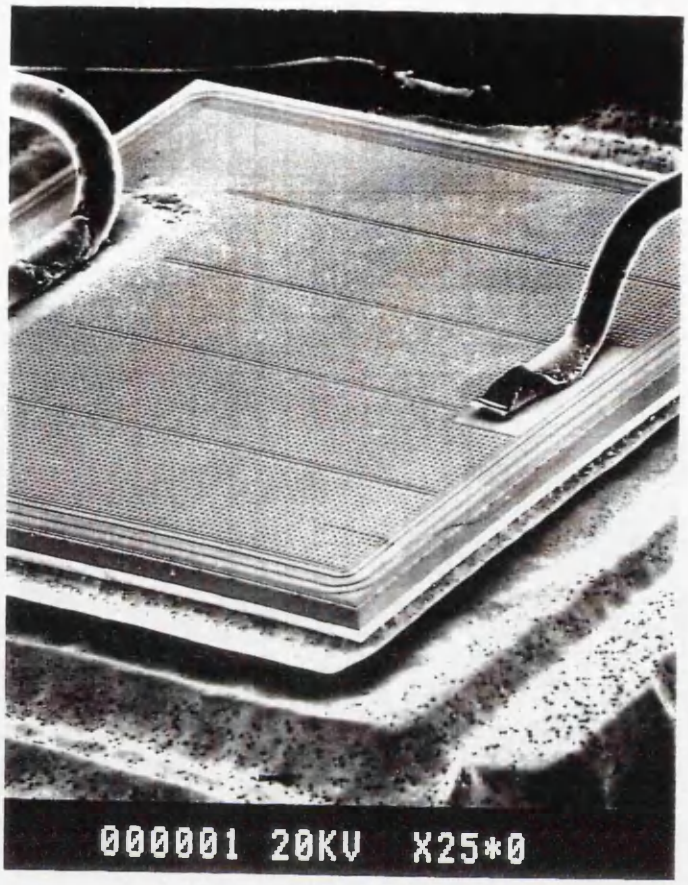
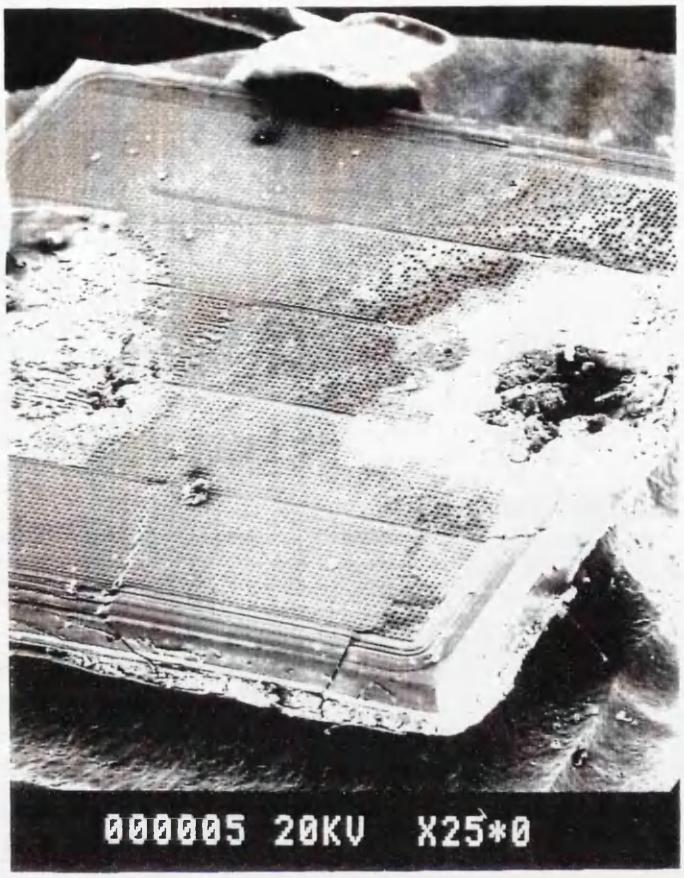


Figure 5.1(a)
Undamaged FET



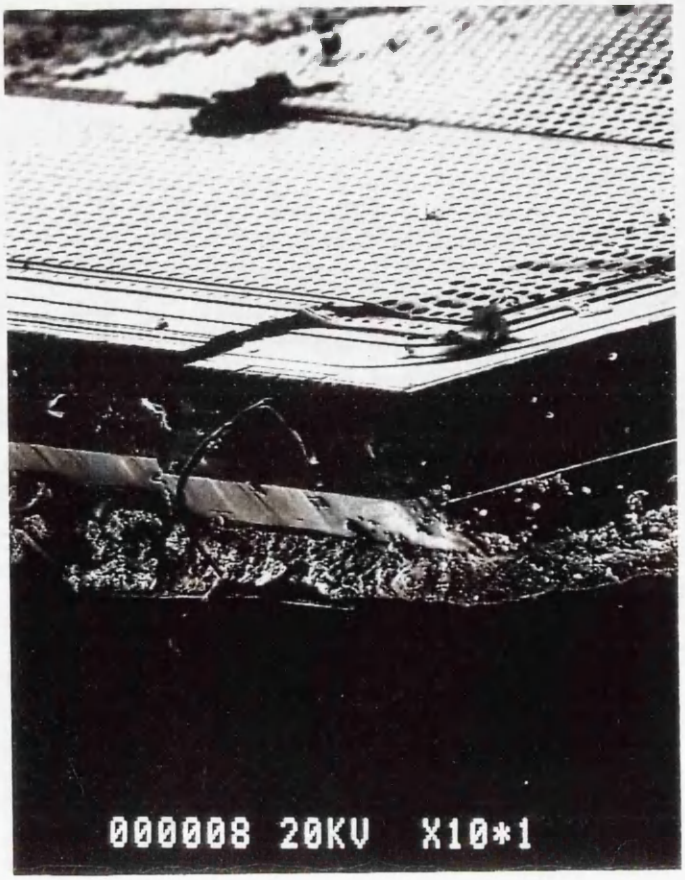


Figure 5.1(b)
Electrically Damaged FET

In each case the stress was measured in terms of the temperature of various components under each test condition. This was done initially with the Thermal Imager which suggested that low input voltages and higher loads resulted in higher component temperatures.

The component whose temperature varied most over the changes of input voltage and output load was the main switching Field Effect Transistor (FET) in the D.C. to D.C. converter. Consequently when the tests became more quantitative a thermocouple was attached to the FET and its temperature was monitored throughout as the input voltage and output loads were varied.

It was decided that the most objective way to compare the thermal effects of the various stress conditions was to record the temperature reached, in each case, a designated number of minutes after the power supply was switched on. The warm up time used initially was three minutes.

Any Operating condition - Temperature relationship had to be justified in terms of what was causing it. This was done as follows:

Having set up the apparatus as shown in Figure 5.2 the voltage and current waveforms for the FET were monitored on an oscilloscope. The mathematical functions in the oscilloscope allowed these two waveforms to be mulitiplied together, to give a value for instantaneous power, and to be integrated to give energy at time t. The temperature rises were a result of the power dissipation in the FET.

For most of each switching cycle the FET is either completely on or completely off. In the former condition the voltage across the FET, the Drain-Source voltage (V_{DS}) is very small, approximately 2V. In the latter case the current(I) through the FET is 0 Amps. For each of these conditions, therefore, the power (VDS * I) produced in the FET is zero or very small. Significant power is only dissipated when the FET in a state of transition, i.e. in the process of switching on or off. During such transitions both voltage and current have significant non-zero values.

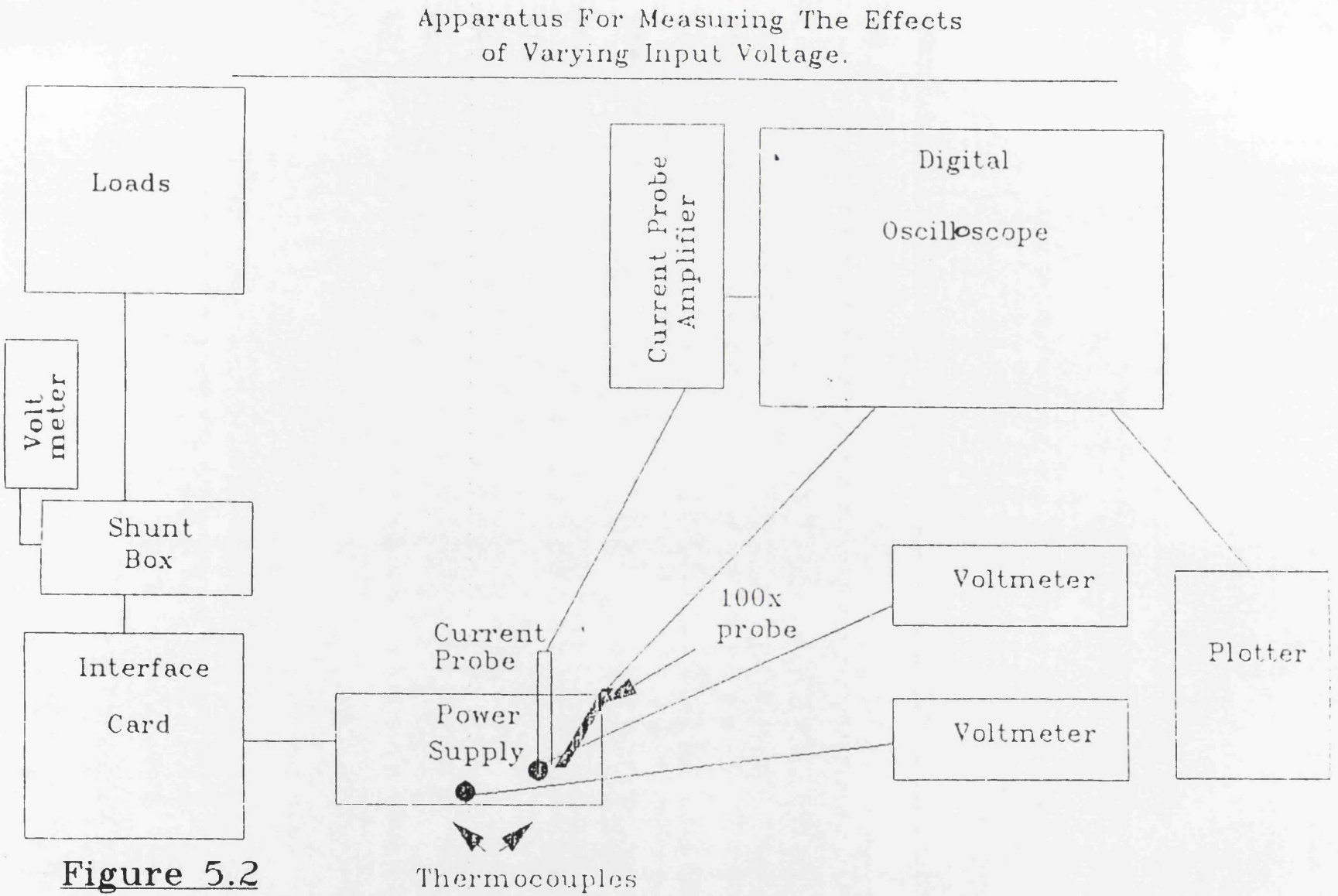


Figure 5.2

Apparatus For Measuring FET Power

By calculating the energy dissipated over a complete switching cycle and multiplying the result by the switching frequency it is possible to obtain the energy dissipated per second, i.e. the dissipated power, and this should be directly related to the temperature reached by the FET. Figure 5.3 shows a typical set of curves as produced by the Oscilloscope.

Results

The first test carried out was that which compared the effect of different values of input voltage on FET temperature and power dissipation.

The initial three minute temperature test (The power supply was switched on when the FET temperature was 30°C and allowed to run for three minutes at which point the temperature and power dissipation of the FET were recorded) suggested that an input voltage of 90V gave rise to the highest power dissipation. The power curves however did not support this but instead suggested that maximum power dissipation took place in the higher voltage range and towards the higher values thereof.

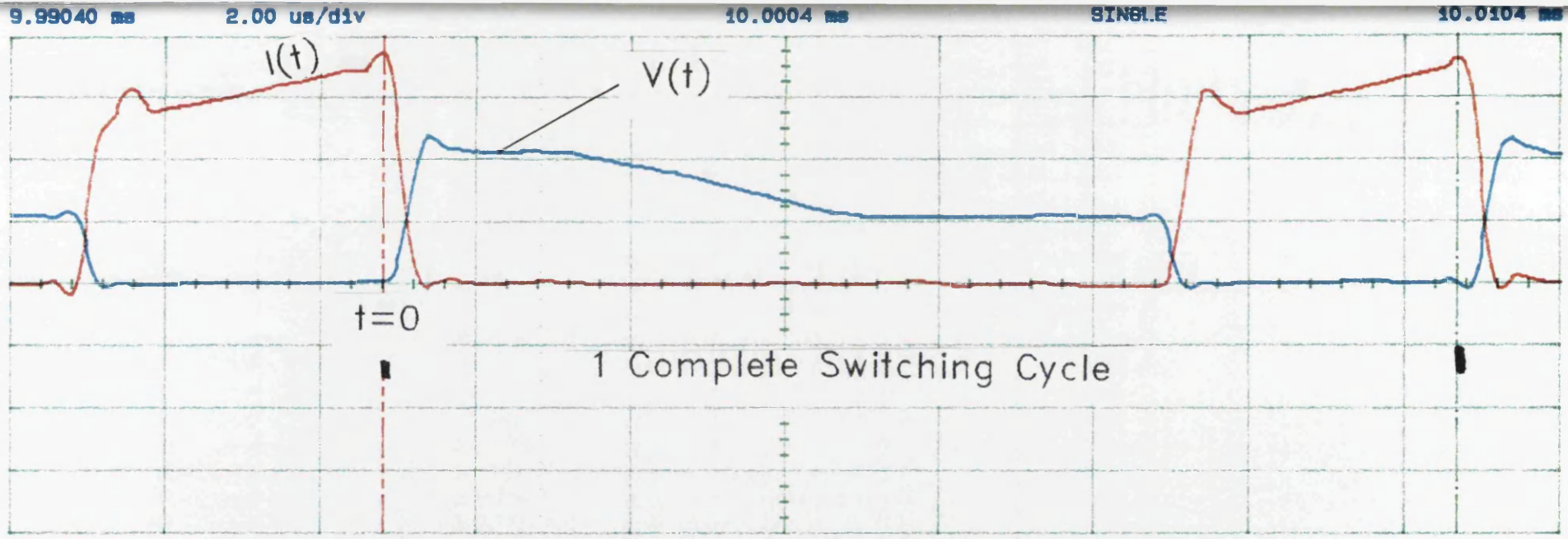
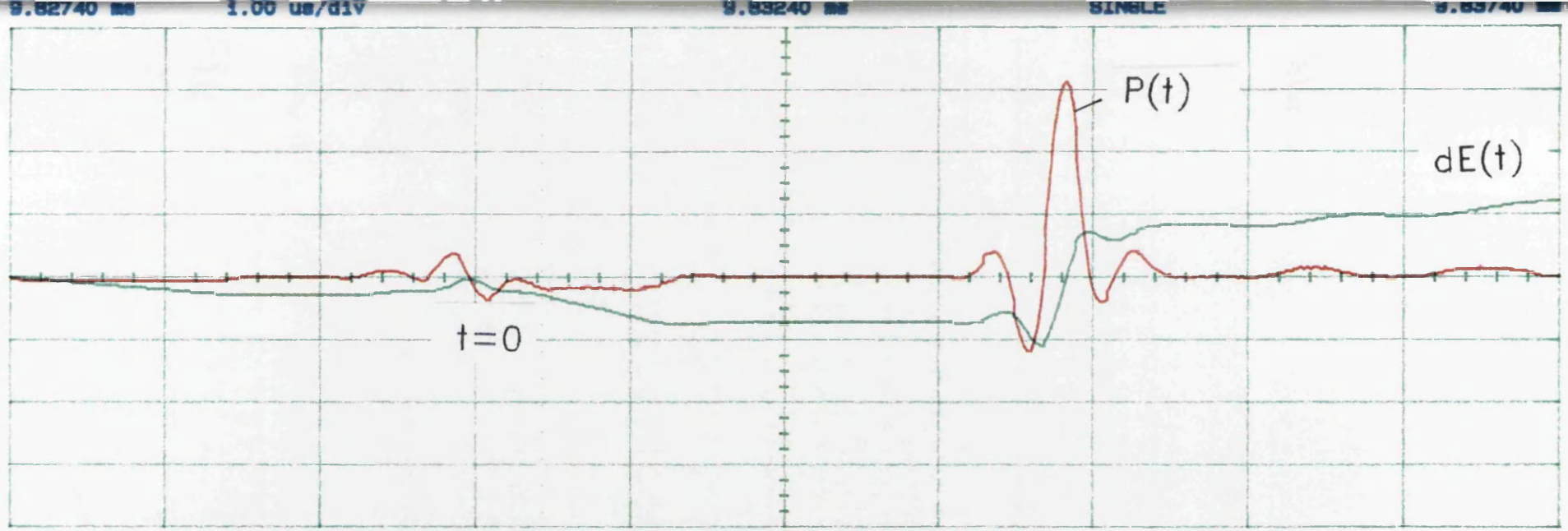


Figure 5.3(a)

FET Voltage and Current Waveforms



	Sensitivity	Offset	Timebase	Delay	Sampling
WMemory 3	1.00 V/div	0.00000 V	1.00 us/div	9.85300 ms	Repetitive
WMemory 4	313 nV/div	0.00000 V	1.00 us/div	9.85300 ms	Repetitive

Trigger Mode: Edge
On the Positive Edge of Channel1
Trigger Level(s)
Channel1 = 0.00000 V (noise reject ON)
HoldOff = 40.000 ns

Figure 5.3(b)

FET Power and Energy Waveforms

Method For Calculating Average Power Dissipation

Step 1 Use Oscilloscope to measure FET voltage and current. over 1 complete FET Switching cycle (Figure 5.3 (a)) and produce traces of v(t) and i(t) v t.

Step 2 Use Oscilloscope's Mathematical Fucntions to multiply each point on the voltage trace with the corresponding point on the current trace and produce a trace of instantaneous power over 1 complete FET switching cycle. P(t) v t (Figure 5.3 (b))

Step 3 Use Oscilloscope's Mathematical Functions to integrate the curve from step 2 above and produce a trace of dE(t) v t where dE(t) is the Increase in Energy since t=0 (Figure 5.3 (b))

Step 4 Calculate Total Increase in Energy over 1 cycle by measuring the 'height' finally reached by the Energy Curve. Remember to add on all fluctuational since these also represent increases in Energy.

Step 5 Repeat for 1 other FET cycle.

Step 6 Take Average of Energy 'heights' reached.

Step 7 Calculate actual energy in J using 1mm represents 1.5 J. (Calculated using constant power section of cycle)

Step 8 Multiply by FET cycling frequency to get Joules/second i.e. Power in Watts.

Figure 5.3(c)
Explanation of FET Power Calculations

It was suggested by someone who had carried out similar tests on other power supplies that the elevated low range temperatures could be attributed to the heat contribution from the voltage-doubling triac which was mounted on the same heatsink as the FET. To confirm this a thermocouple was attached to the triac and its temperatures was measured, under each low range voltage condition, five minutes after the power supply under test was switched on.

This relationship comes about from the fact that the power dissipated by the triac, and therefore its operating temperature are proportional to the product of RMS current flowing through the triac, which is the input current of the power supply, and the voltage across it, which is the input voltage; i.e. the power supplys input power. The triac only conducts when the power supply is operating in the low voltage range. Figure 5.4 relates the recorded triac temperatures to their corresponding values of input voltage and current.

The comparisons of FET temperature and dissipated power were therefore repeated with the input voltages used being restricted to those in the upper voltage range. This meant that any rises in temperature were due entirely to the FET. On this occasion, however, the stabilisation time (the time for which the power supply was switched on before measurements were made) was extended to five minutes. The temperatures recorded subsequent to this corresponded to the observed power dissipations. For each value of input voltage in the high voltage range the power supply was switched on, and the measurements made, twice to confirm that the results were correct. Figure 5.5 relates FET Temperature to the calculated value of dissipated power and as can be seen from the figures contained therein the rises in FET Temperature with Input Voltage are matched by the rises in dissipated power.

Triac Temperature v Input Voltage
(5 Minutes after Power Supply Switch On)

	Input Current (A)	Input Power (W)	Triac Temperature (°C)
Vin = 88.9V	2.66	170.5	45.0
Vin = 101.6 V	2.49	180.6	45.0
Vin = 114.8 V	2.33	184.0	43.0
Vin = 136.5 V	2.00	187.0	36.5

Figure 5.4
Triac Temperature v Input Voltage

FET Temperature v Input Voltage
(5 Minutes after Power Supply Switch On)

	Input Current (A)	Input Power (W)	Triac Temperature (°C)	Average FET Power (W)
Vin = 180	1.64	173.5	61.25	6.61
Vin = 263.7	0.92	147.7	61.75	7.49
Vin = 285.5	0.84	150.6	64.50	8.29

Figure 5.5
FET Temperature v Input Voltage

Section 5.2:Examination By Thermal Imager

Having used thermocouples to examine individual component temperatures under varying input voltages conditions it was decided to use the thermal imager to gauge the effects of such variation on the temperature of the power supply as a whole. The same method was used to compare the effectiveness of the highest available volatge in each input voltage range.

In order that the various conditions could be compared the tests were performed as follows:

Five components on the power supply were selected and allocated 'spots'. This means that computer constantly monitored and displayed, using the 'spot temperature' facility, the actual temperature of these components. The computer was instructed to produce a temperature plot i.e. to record the spot temperatures at 15 second intervals and display these on the screen as line graphs. The consequence of this was a Temperature v Time plot for each of the selected components which showed clearly the time, and value, at which the temperature of each component stabilised.

An initial run revealed that the power supply had stabilised within ten minutes of being switched on. Consequently all subsequent checks adhered to the following schedule:

Time	Action
H:M:S	(H: Hours, M: Minutes, S: seconds)
X:Y:0	Start Plot
X:Y+1:0	Start Power Supply
X:Y+11:0	Print thermal status and curve
X:Y+16:0	Freeze thermal image and record extreme and statistical temperature values.

Results

The results appear in Figure 5.6. and a typical photograph showing thermal status with the relevant plot of temperature log appears in Figure 5.7.

Thermal Imaging Data

Principal Component Temperatures
At Various Input Voltages

	FET Temperature Degrees C	Triac Temperature Degrees C	PWM Temperature Degrees C	+5 V Diode Temp. Degrees C	+12 V Diode Temp. Degrees C
Vin = 90 V	63.0	49.4	40.6	63.0	49.4
Vin = 137 V	57.2	43.7	32.6	63.0	48.0
Vin = 230 V	58.6	44.0	38.5	62.7	46.2
Vin = 265 V	56.9	43.3	39.3	61.2	47.6
Vin = 280 V	57.8	43.0	40.6	64.0	47.3

Thermal Imaging Data

Principal Component Temperatures
At Various Input Voltages

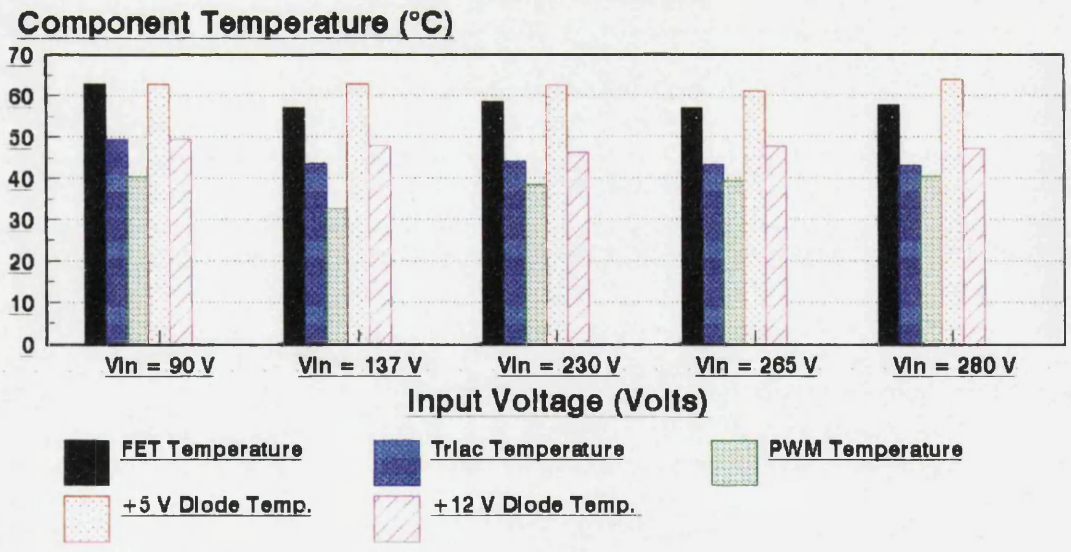


Figure 5.6

Thermal Imaging Data

Figure 5.7

Thermal Imager Temperature Plot

Section 5.3: The Effect of Varying Output Load

Having established a relationship between FET Temperature and Input Voltage the next task was to examine the effects, on that same temperature, of changing the power supply's output load while keeping the input voltage constant. The following factors were of particular interest:

1) Is an increased +5V Load more effective, i.e. does it result in a greater FET temperature, than a +12V load increase where both increases bring about the same overall increase in output power?

2) Is a step load more effective than a steady D.C. load of the same average value?

Again for each load combination two measurements were made of the FET temperature five minutes after switch on and the power dissipated by the FET. i.e. The power supply was switched on twice under each condition of output load.

Results

The results of these investigations appear in Figure 5.8.

FET Temperature v Output Load

	Condition	Input Power (W)	Input Current (A)	+12V Current (A)	+5V Current (A)	Output Power (W)	FET Temperature (C)	Average FET Power (W)
Normal Load		148.5	0.83	3.23	9.62	92.70	39.50	12.83
Elevated +12V Load	Constant	161.3	0.88	3.99	9.49	100.14	41.00	13.26
Elevated +12V Load	Step Load	160.9	0.88	3.99	9.50	100.19	42.00	15.97
Elevated +5V Load	Constant	177.2	0.98	5.05	9.49	111.96	42.00	15.54
Elevated +5V Load	Step Load	184.4	1.01	3.26	14.11	113.52	43.75	16.43

Figure 5.8 FET Temperature and Power Dissipation For Various Output Loads

The current limiting circuitry of the power supply limited the size of the step load, which could be applied to the +12V output, to 3.99 Amps. Therefore in order to compare this load with a D.C. load it was necessary to use a D.C. load of 3.99A despite the fact that the +12V output could be as high as 5.05A.

The +5V current could have values of up to 19A but in order to compare its effects with those of the +12V output the highest load which was used drew a current current of 14.11A.

As can be seen from Figure 5.8 the effects of an elevated +5V load and an elevated +12V load which both result in the same output power are almost identical. However due to the fact that a higher +5V load is possible an increase in +5V current to a value close to that at which the power supply would shut down would be the most effective load to use.

The other result from this test is the fact that a step load is considerably more effective, with respect to raising FET temperature than a D.C. load of the same average value.

As a consequence of the above tests, including those in which the input voltage was varied, it was decided that the most effective electrical combination to use in the course of life testing would be an input voltage of 90-110V with the maximum rated output load placed on each channel. Such a set of conditions would ensure that all the components operated at as a high a temperature as possible and at the same time would remove the possibility of component damage due to excessive electrical stress.

Section 5.4:The Effect of interfering With Airflow

The tests documented below were those carried out in an attempt to discover if it was possible to recreate, by changing the ventilation capabilities of a power supply, the same thermal conditions as a power supply would experience in a thermal chamber at 60°C.

In the event of this being possible the laboratory could in theory double the capacity of its life testing facilities because as many units could be tested 'on the bench' as could be placed in the chamber.

As can be seen from Figure 5.9 a power supply is cooled by a fan and a series of ventilation slats. The fan pulls air in from the surroundings which blows across the components and out through the slats.

The tests performed consisted of covering the vents, and or the fan, with adhesive tape and monitoring, with thermocouples, the temperature of critical power supply components while the power supply was operating. Such tests were carried out using various combinations of input voltage and output load and the results appear in Figure 5.10.

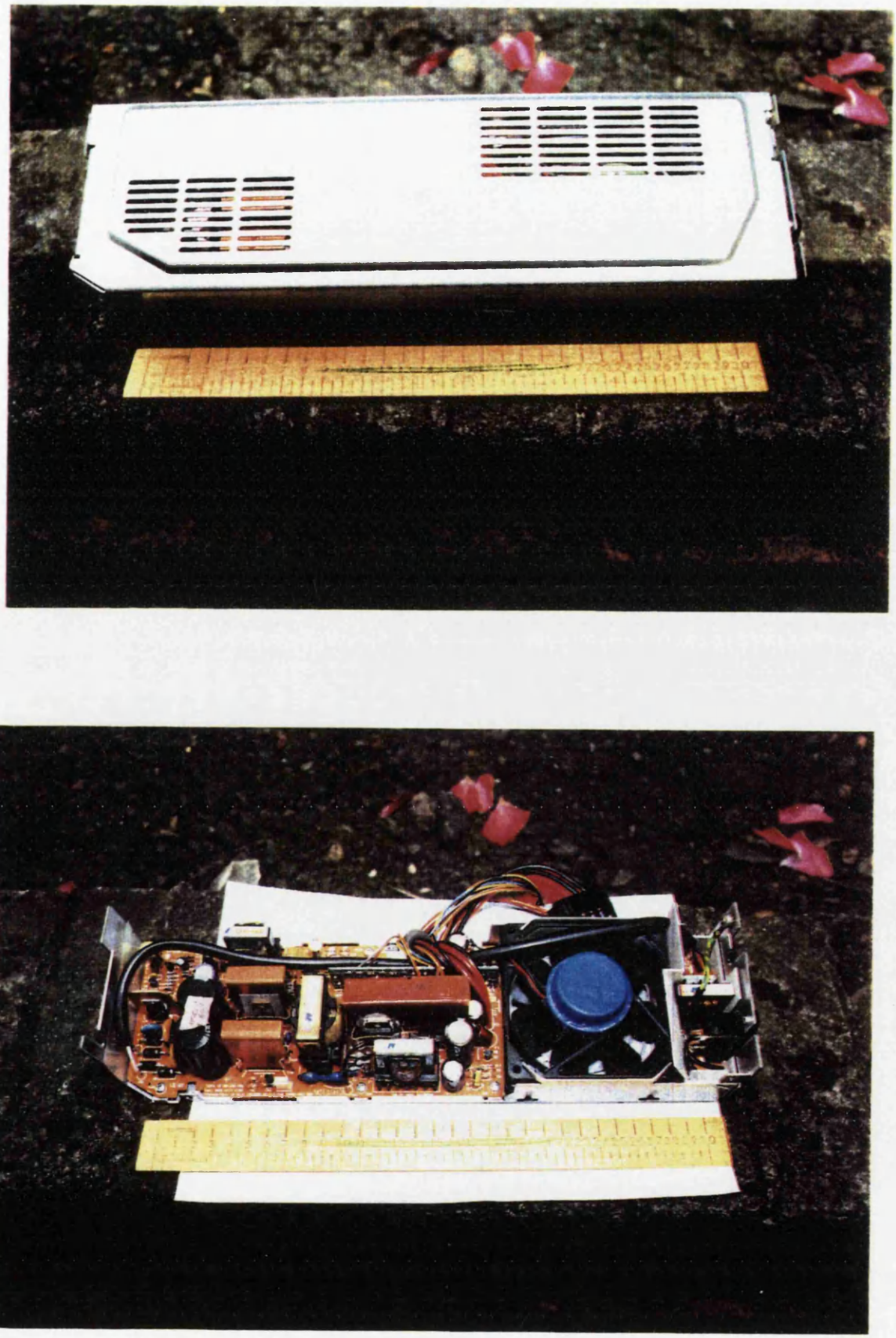


Figure 5.9

Power Supply Ventilation System

As can be seen through examination of the graphs in Figure 5.10 instead of the various covers bringing about an overall increase in temperature resembling that which would result from placing the power supplies in an elevated ambient their effect is instead to bring about an increase in the temperatures of the components which is considerably less than that caused by an increased ambient temperature. This is based on a comparison of temperatures of components after the power supply has been switched on for equivalent periods of time i.e At the same number of minutes after switch on.

Additionally: the temperature profiles for the components of power supplies in elevated ambient temperatures indicated that a final stabilisation temperature was achieved approximately 10 minutes after the power supply was switched on. In the case of power supplies with various levels of covering the component temperatures do not stabilise but continue to rise.

The combination of covering and load which brought the component temperatures closest to those values seen in a 60°C ambient consisted of a cover which blocked the fan and the ventilation slats; in combination with an elevated +5V load.

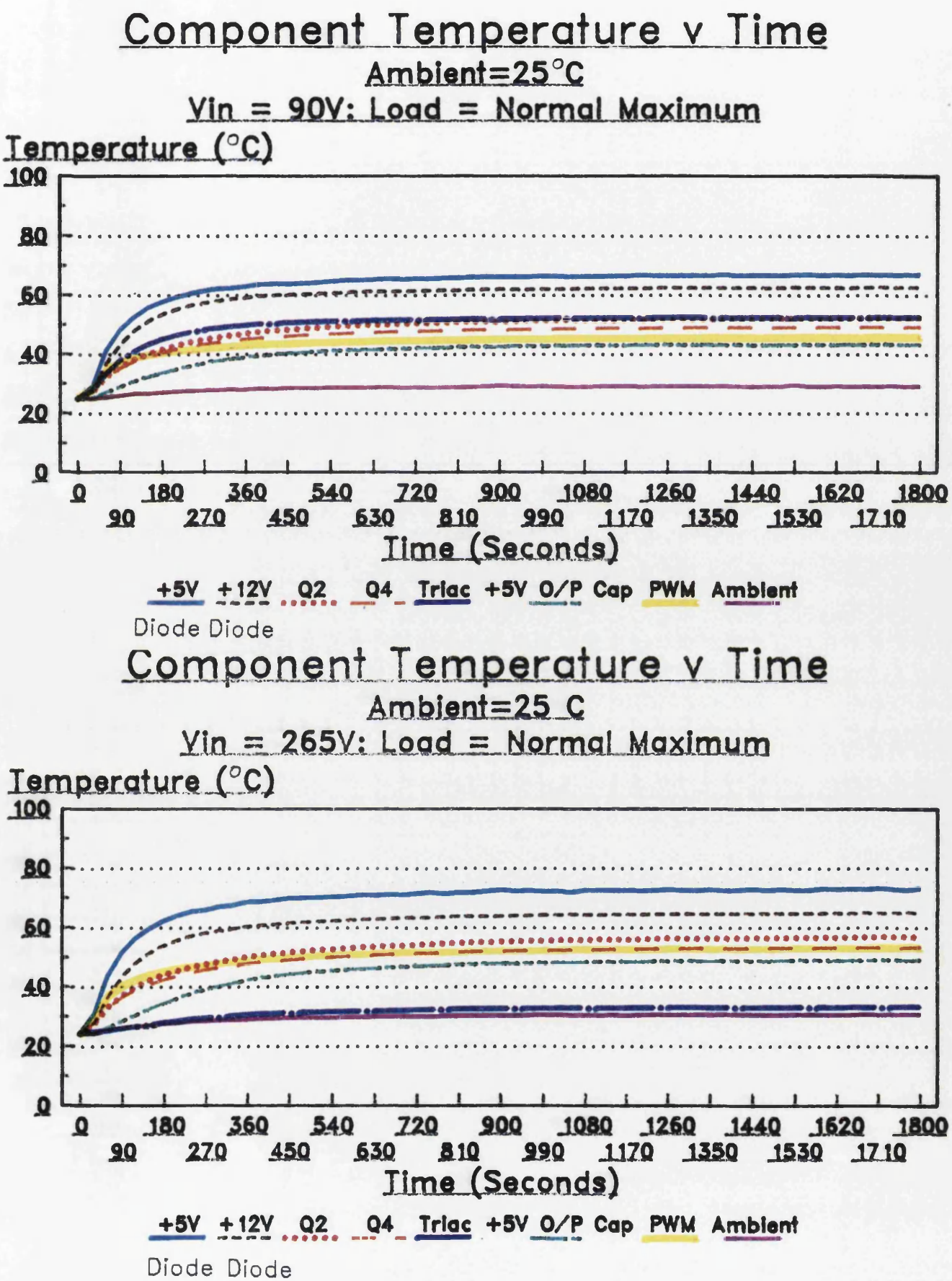
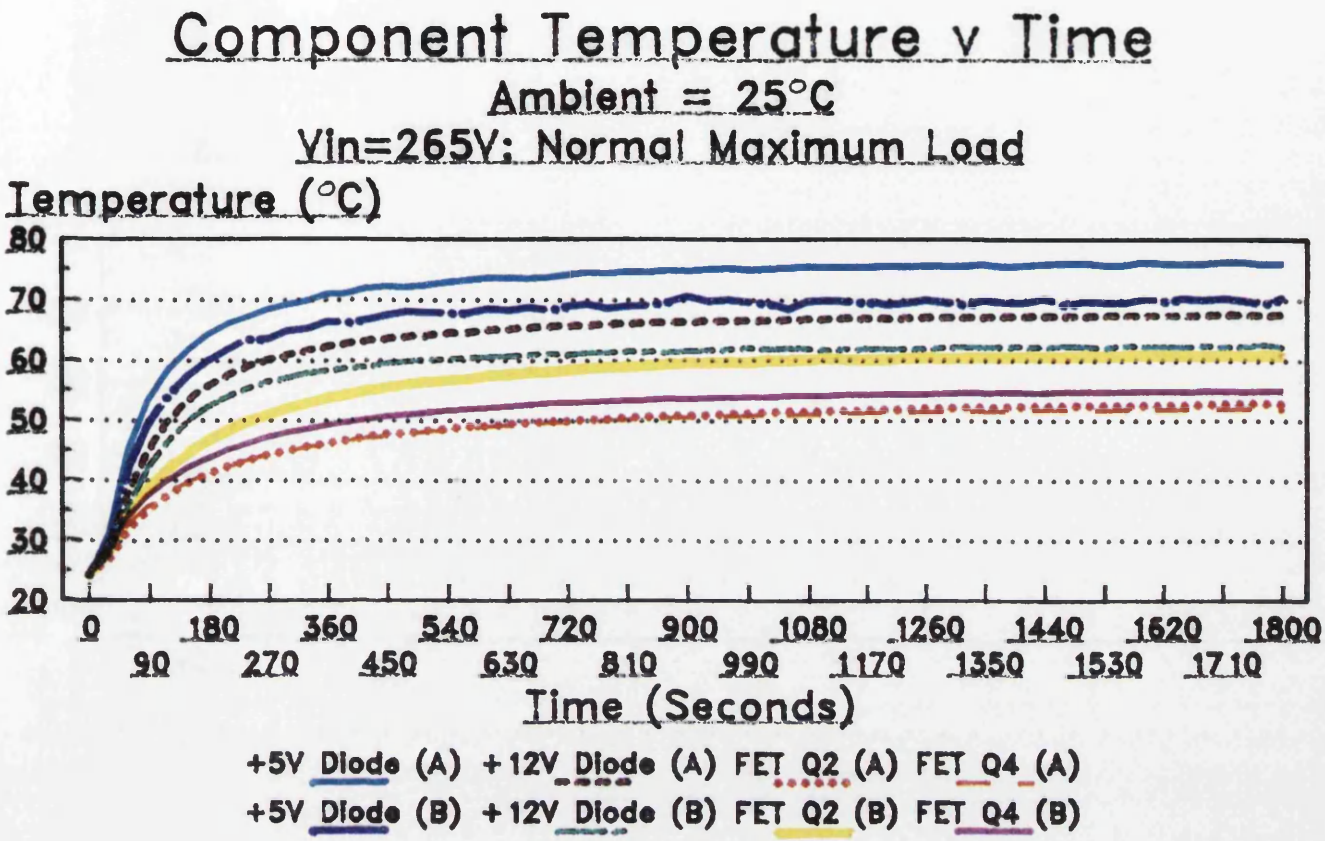


Figure 5.10 Component Temperatures Under Various Ventilation Conditions



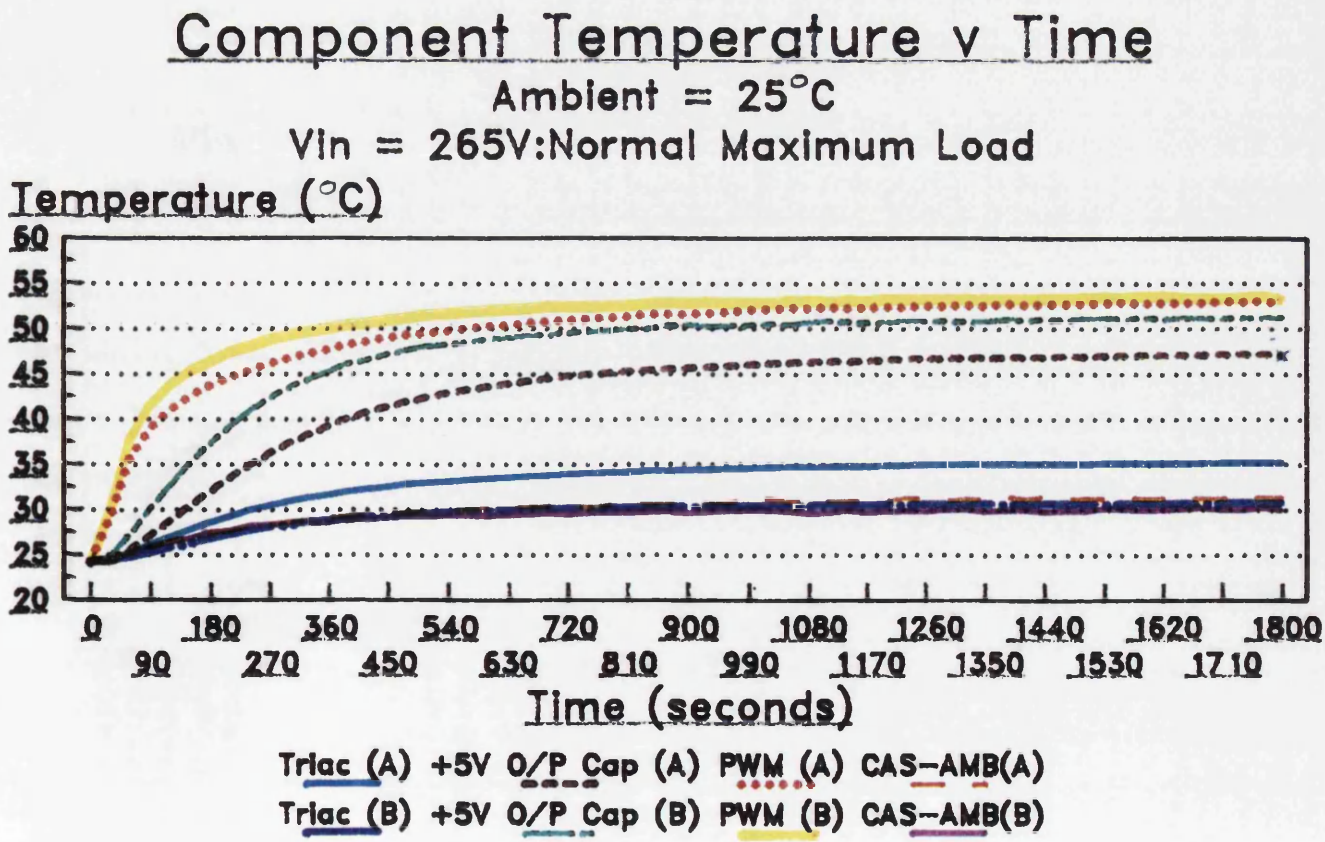
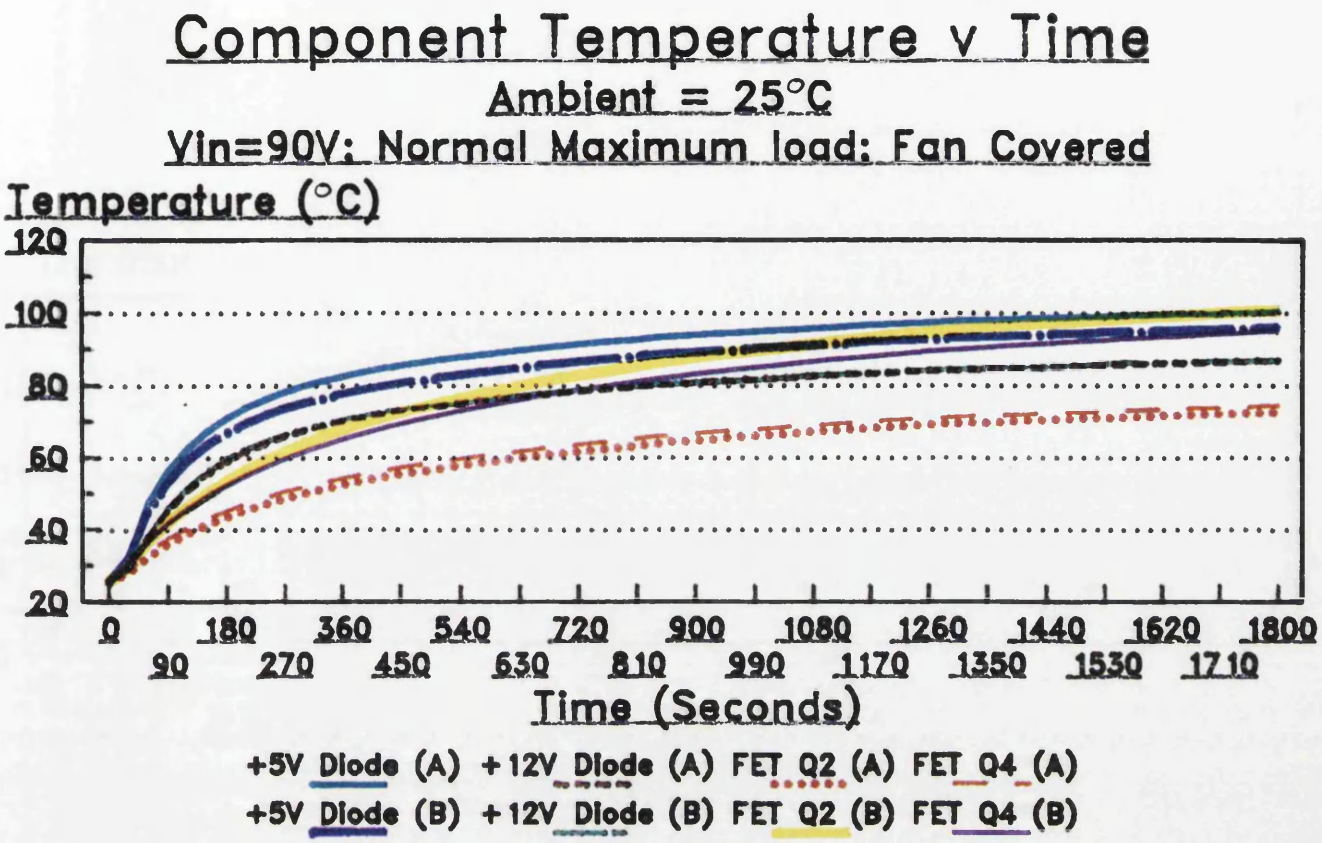


Figure 5.10 Component Temperatures Under Various Ventilation Conditions



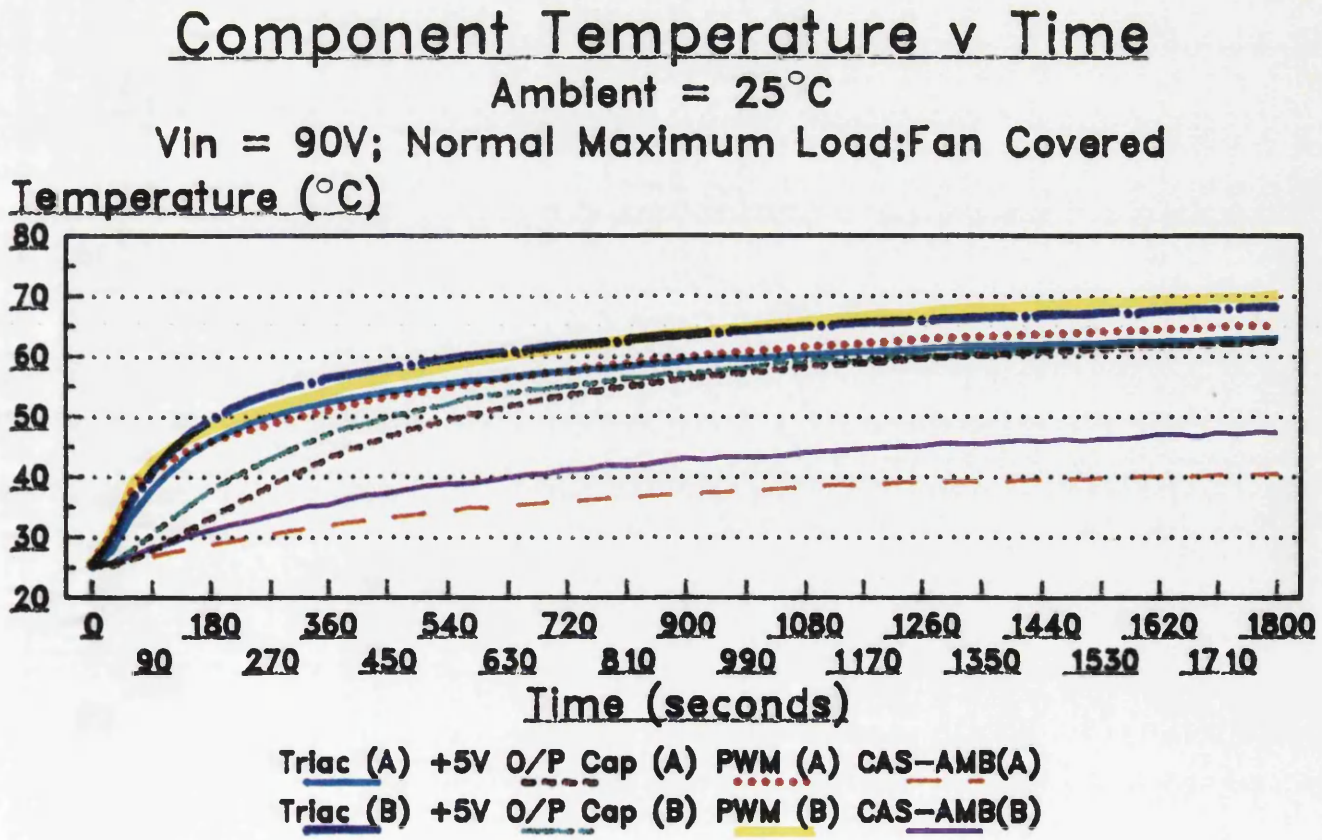
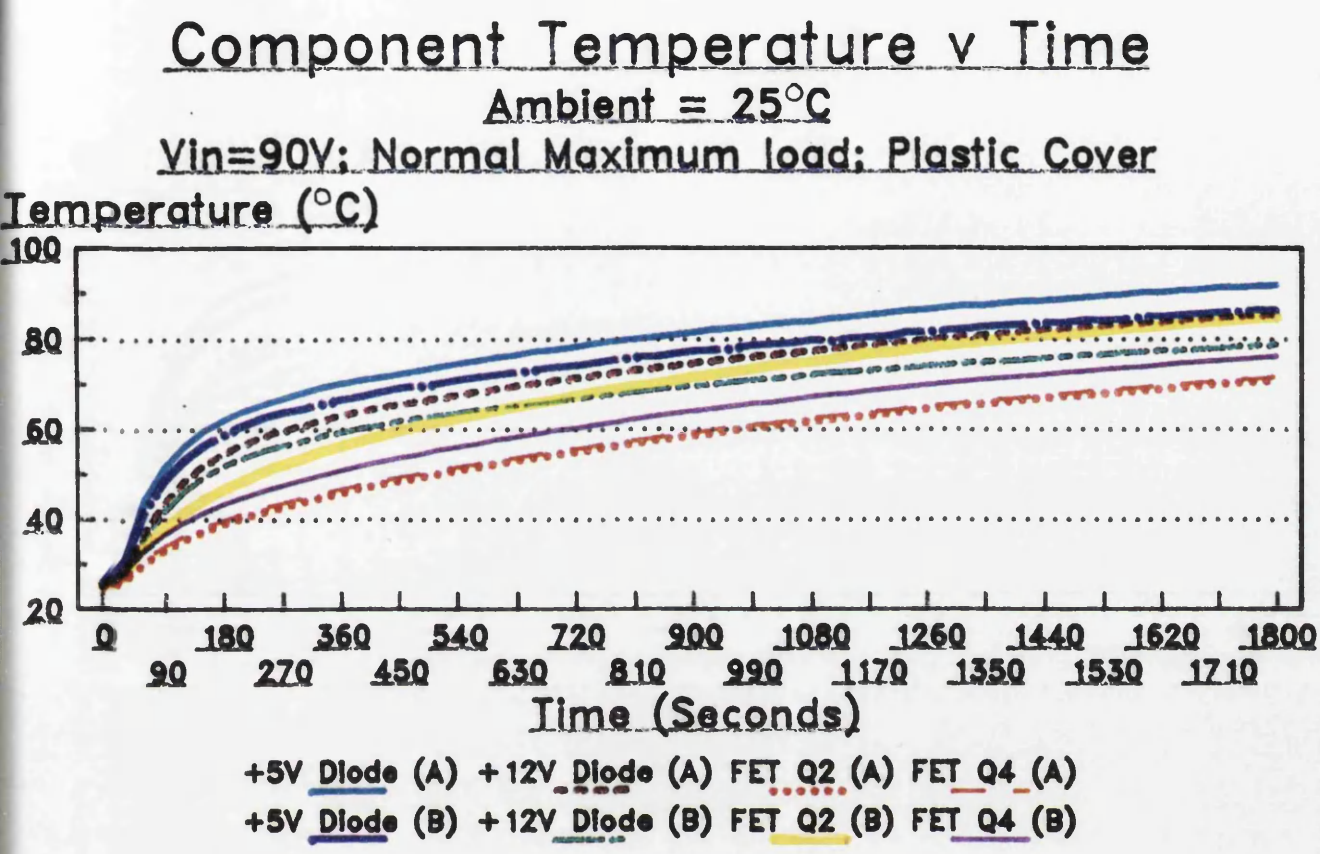
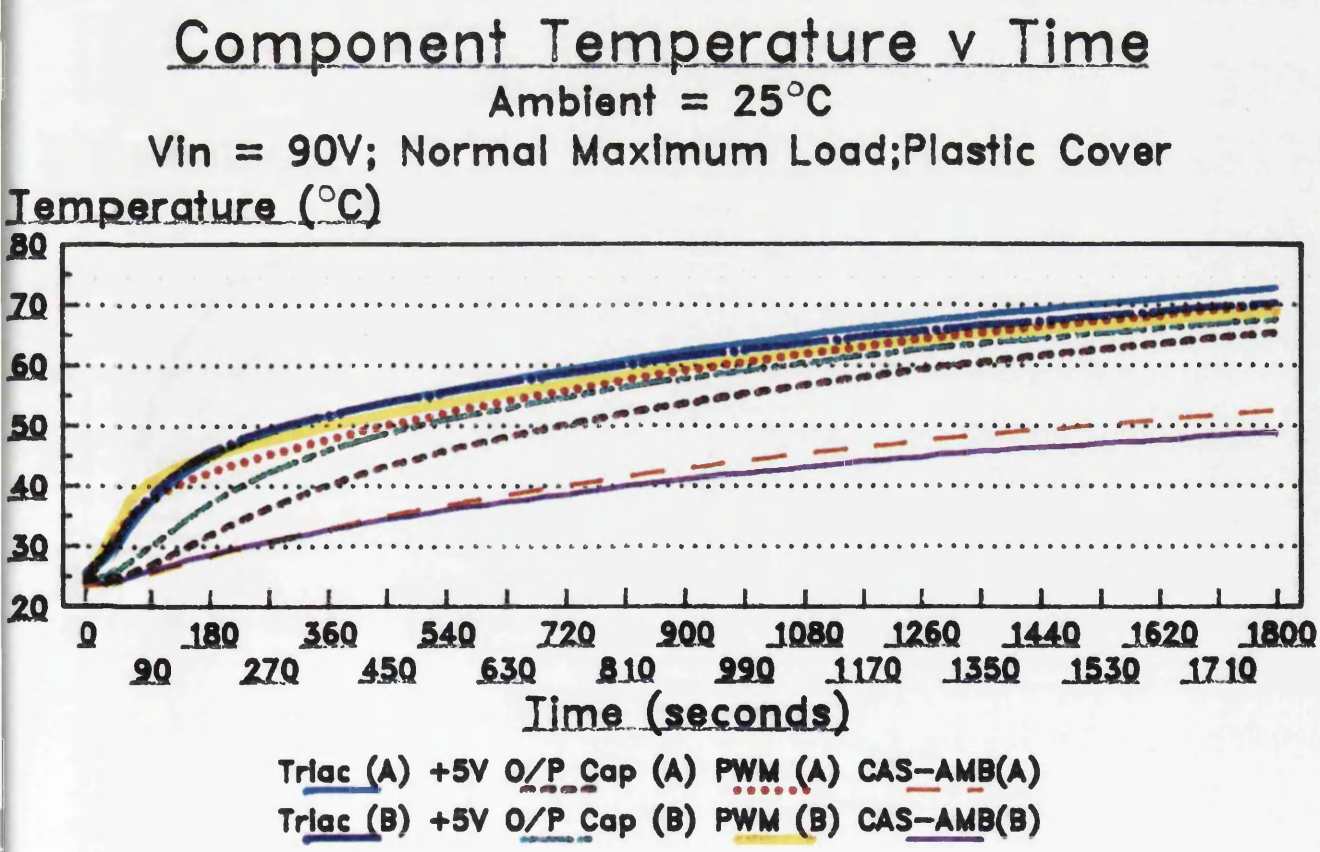


Figure 5.10 Component Temperatures Under Various Ventilation Conditions





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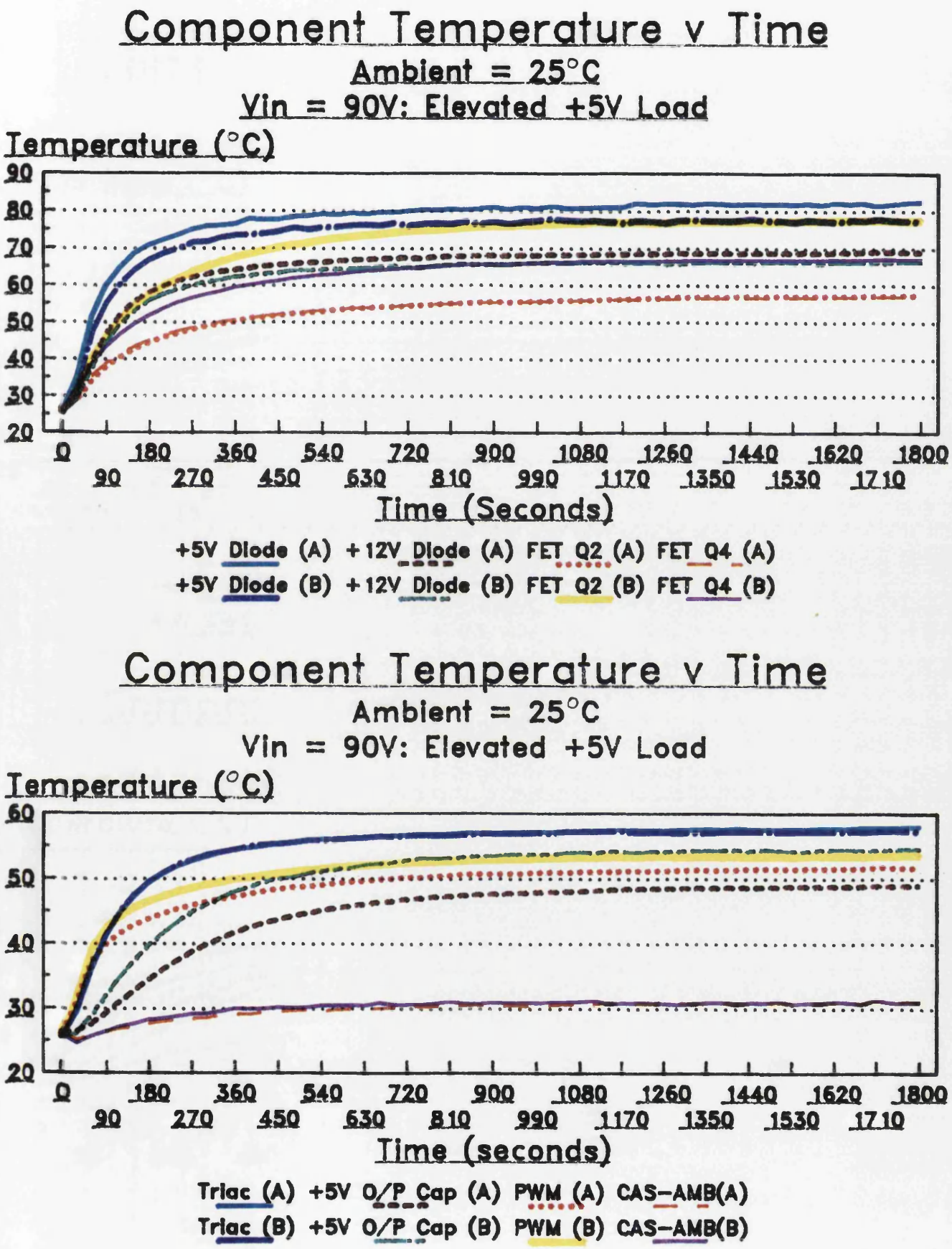
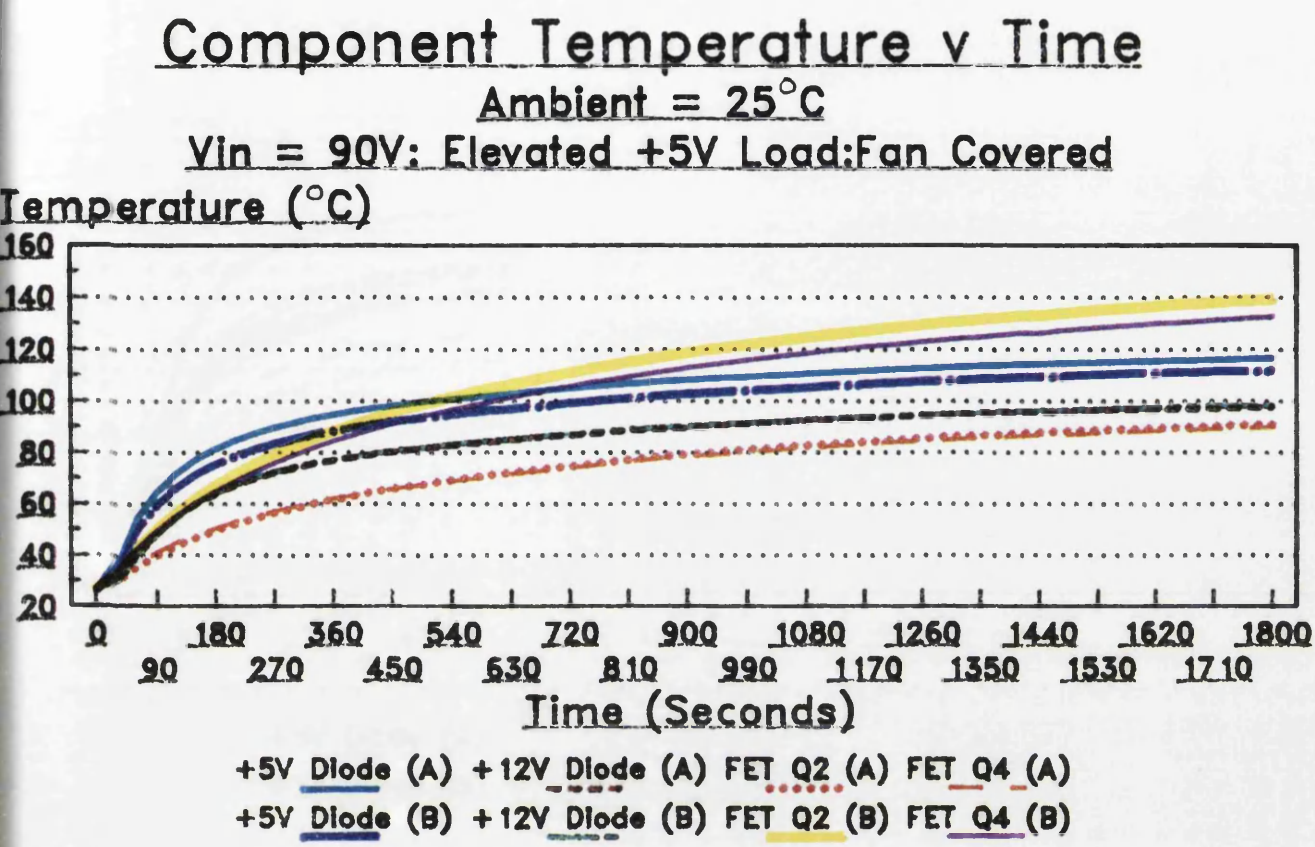


Figure 5.10 Component Temperatures Under Various Ventilation Conditions



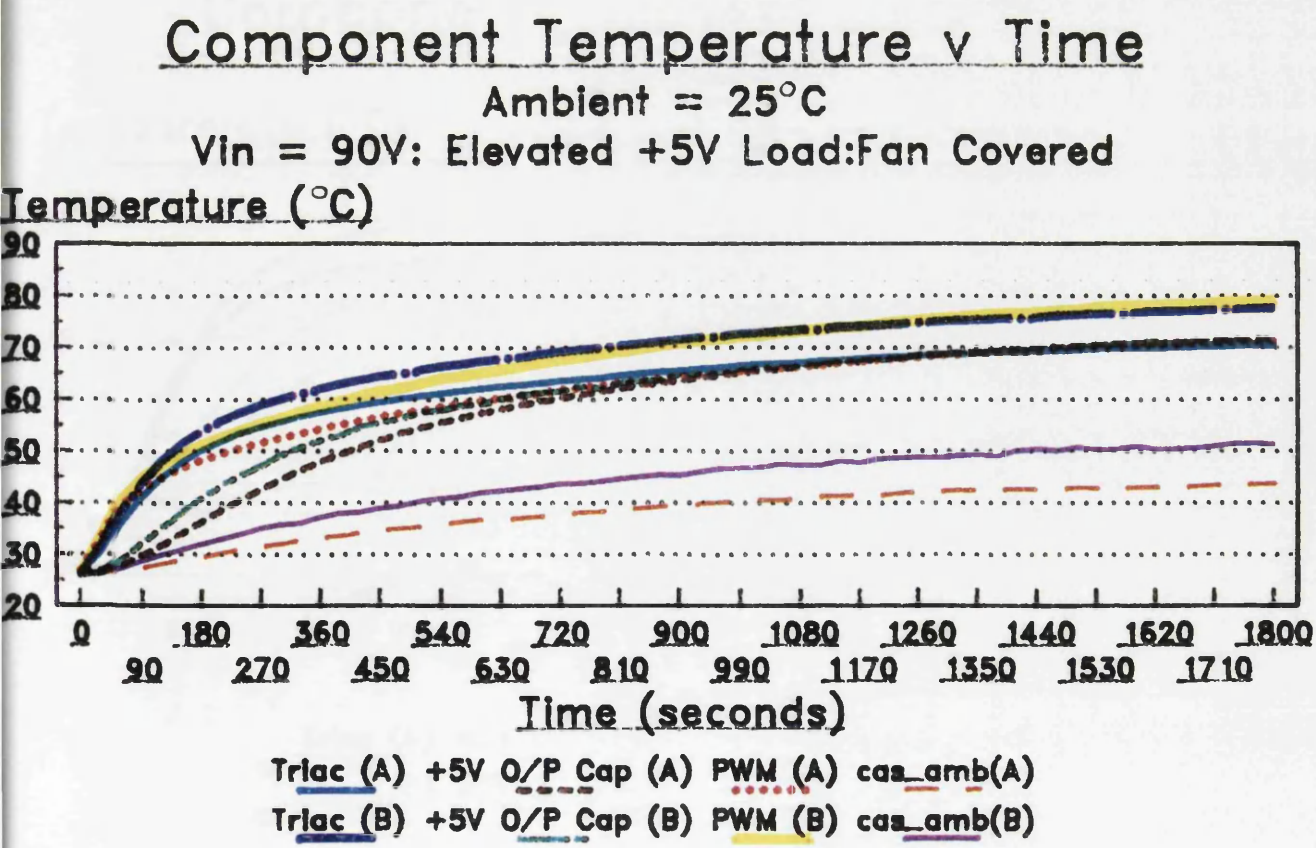
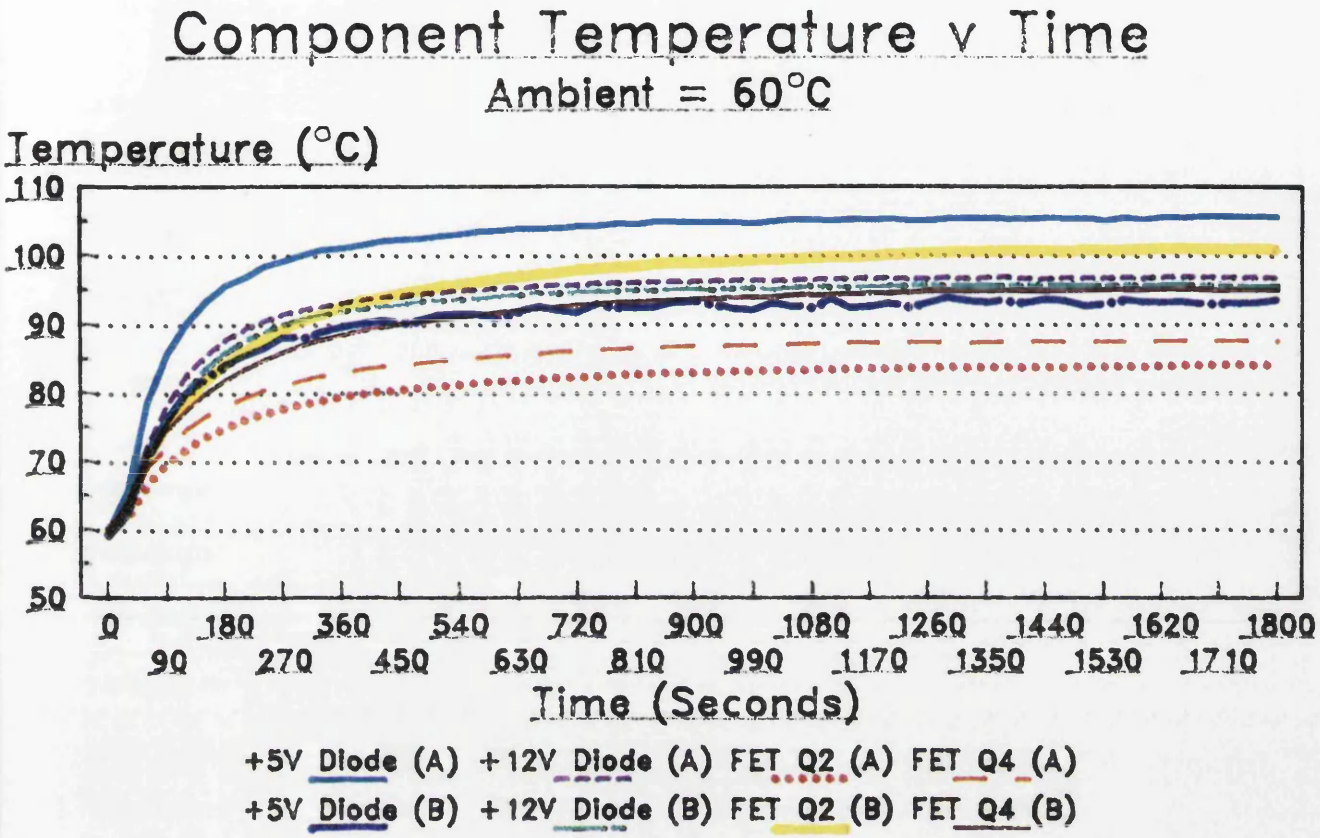


Figure 5.10 Component Temperatures Under Various Ventilation Conditions



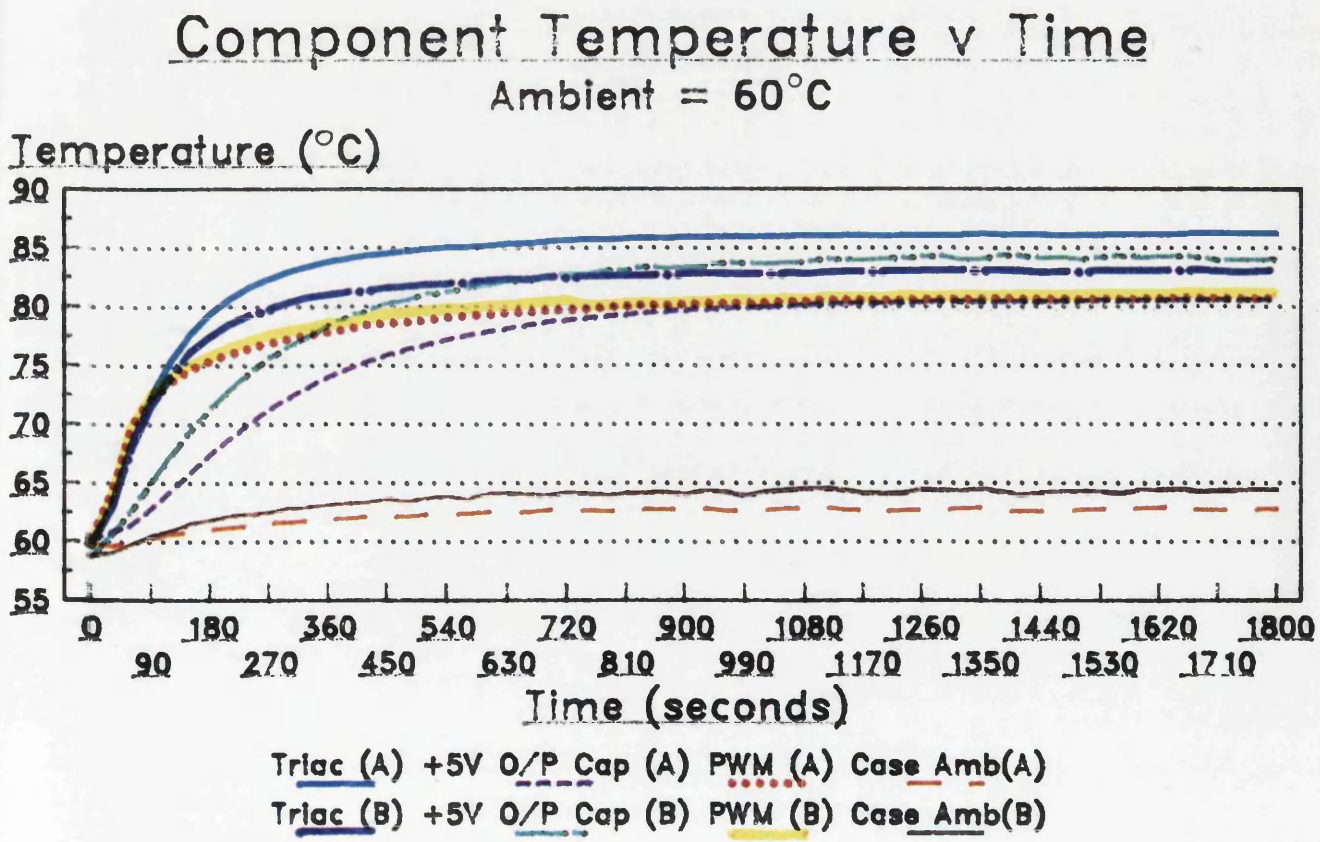


Figure 5.10 (TARGET CONDITIONS)
Component Temperatures Under Various Ventilation Conditions

The component temperatures climbed steadily until they reached and passed those measured in a 60°C ambient. The FET tempertures eventually reached a point at which the FETs suffered catastrophic failure due to heat damage.

A photograph of a FET which failed due to heat damage is shown in Figure 5.11. As mentioned above such damage is indicated by discolouration of the semiconductor layer of the FET. Also present in this case is a series of pits on that same surface. These indicate if this FET had not failed due to heat damage it was in iminent danger of failing due to the electrical damage brought about by the increased +5V Load over a prolonged period of time.

Figure 5.11
Heat Damaged FET

Conclusions

There does not apppear to be a combination of electrical and ventilation conditions which, when imposed upon a power supply, truly replicate the conditions encountered in a thermal chamber at a steady elevated ambient temperature.

Chapter 6-Conclusions

Based on the outcomes of the various tests documented it would seem that those tests which involve placing the power supplies in an elevated ambient temperature, either for prolonged periods or as part of a temperature cycle, hold the most promise as possible means of accelerating life tests.

As was mentioned in Chapter 3; "The Effects of Elevated Ambient Temperatures", if a test can be found which accelerates the life of a power supply's electrolytic capacitors to the point at which the power supply fails because these capacitors have failed, provided the capacitors have a longer life expectancy and MTTF than the power supply, then the manufacturer will safely be able to claim that the power supply has fulfilled its reliability expectations.

The tests documented in that chapter, and the effect that these tests had on the capacitors involved reveal that elevated temperatures do lead to breakdown of capacitors, by means of evaporating electrolyte. Which, as was mentioned, is a process which requires a definite amount of energy to be supplied. The more energy that can be supplied to the capacitors at any time the faster the electrolyte will evaporate.

The two means of applying this energy are:

1) Heat by means of elevated ambient Temperatures
2) Heat by means of Electrical Energy.

The tests revealed that electrical conditions, other than those documented in the power supply specification tended to bring about failure of the FETs . In other words it is unadvisable to supply any more energy, or apply any more stress, by electrical means, to a power supply than it would normally encounter.

This suggests that the most promising means of increasing the energy to, and the evaporation of, the capacitor electrolyte is through increasing the amount of heat energy supplied to the capacitors, by means of an elevated ambient temperature.

This suggests the following main conclusions: regarding the work documented above and any further research which may result from it.

1) Those tests involving the power supplies being exposed to CONSTANT HIGH AMBIENT TEMPERATURES would seem potentially more promising than those which include high ambient temperature as part of a temperature cycle. Since the object of the exercise appears to be to apply as much energy to the power supply in as short a time as possible it makes little sense to spend part of a test applying this energy and the rest of the test removing it. It is also worth considering the cost of operating heaters to increase the temperature then fans to decrease it only to raise it again a short time later. It would seem more logical, not to mention less expensive and easier to implement, to maintain a continuous high temperature which constantly contributes to eletrolyte evaporation. For similar reasons the power supplies should spend as much time powered on as possible; although any test must allow for verification that the power supply can survive the required number of switching cycles as quoted in the relevant specification.

Although Temperature Cycling has been used for a number of years as part of the array of reliability tests it is used mainly as a means of checking for faults in solder joints. It is reasonable to continue to use the test in this manner, testing a limited number of units from each batch for indications of this type of fault. As it happens such a test is carried out, by the Product Quality and Reliability Laboratory, on all computers, and therefore the power supplies therein, before they are shipped.

The same could be said for High Humidity testing. The value of such a test, especially when the difficulty of maintaining it over long periods is considered, seems to be as a check that the power supplies can tolerate conditions of high humidity, such as might be found in tropical climates.

2) As a consequence of what has been discussed above future work should probably be concerned with finding an optimum temperature, for each power supply, at which to conduct high ambient tests. This would be a temperature which applied as much heat as possible to the capacitors while not exceding the maximum rated values of any of the components on the power supply. For the power supplys used a temperature of 75°C seemed to meet these requirements.

In connection with this a way should be found to quickly analyse every power supply to be tested in terms of operating temperatures of components. It is reasonable to assume that such operating temperatures will vary from power supply to power supply and manufacturer to manufacturer. It is analyses such as these which will indicate the optimum temperatures mentioned above for each individual power supply.

Such investigations could involve experimenting with thermal imaging equipment to discover if component operating temperatures can somehow be thus obtained, with sufficient accuracy, and used to quickly decide upon an optimum ambient test temperature for each power supply received into the Engineering Laboratory.

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((Unless otherwise indicated the source number matches the number given in the body of the text at the point where the source is referred to.)

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