Fabrication and Characterisation of Short Gate Length Heterojunction Field Effect Transistors

thesis by

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Abstract

This thesis is concerned with the fabrication and characterisation of short gate length heterojunction field effect transistors (HFETs). Devices with gate lengths in the range 80-200nm were fabricated on three different material structures containing two dimensional electron gases (2DEGs). The layer structures were based on:

i) $Al_{0.25}GaAs/GaAs$ with an $Al_{0.25}GaAs$ back confining barrier 300Å from the 2DEG

ii) pseudomorphic $Al_{0.3}GaAs/In_{0.15}GaAs/GaAs$ with a 150Å $In_{0.15}GaAs$ channel layer

iii) pseudomorphic $In_{0.52}AlAs/In_{0.65}GaAs/InP$ with a 100Å $In_{0.65}GaAs$ channel layer

Magnetoresistance studies showed the 2DEGs of the three materials had very different transport properties. This permitted an investigation of the dependence of high frequency device performance on material structure to be performed.

To investigate the dependence of gate resistance on device performance, HFET's with conventional and T-gate structures were fabricated. The 80nm footprint T-gate process developed in the course of this work reduced the gate resistance by a factor of five compared with conventional 80nm footprint structures.

High frequency characterisation of devices up to 60GHz showed the following main results:

i) 80nm gate length $In_{0.52}AlAs/In_{0.65}GaAs/InP$ HFETs with rf transconductances up to 1100mS/mm. This translates to an effective channel velocity of $2.4x10^5ms^{-1}$.

ii) 80nm devices with f_T's of up to 275GHz were fabricated on the InAlAs/InGaAs/InP layer structure. Such f_T's were nearly twice those of similar gate length devices fabricated on both the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs structures.

iii) From the f_T measurements, the effective carrier velocity in the device channel was extracted. Effective velocities in excess of $2.0x10^5ms^{-1}$ were extracted for the InAlAs/InGaAs/InP devices, indicating significant velocity overshoot in the channel of this layer structure.
The large indium content of the channel gives a large Γ-L valley energy separation whilst reducing the electron effective mass. Both these effects increase the probability of velocity overshoot, and are most probably the cause of the large effective velocities deduced for the $In_{0.65}GaAs$ channel devices.
There was no conclusive evidence of overshoot in devices fabricated on either the AlGaAs/InGaAs/GaAs or AlGaAs/GaAs structures.

iv) For the materials of this study, it was deduced that effective velocity was the dominant transport property in determining device f_T at a given gate length. Neither the low field mobility or 2DEG carrier concentration were found to govern device f_T.

v) Both device DC and RF output resistance can be increased by increasing the potential barrier below the 2DEG and thus improving electron confinement to the channel.

vi) The 80nm footprint T-gate structure increases device gain by up to 6dB at 60GHz compared to a conventional 80nm gate device.

vii) Although the f_T's of the InAlAs/InGaAs/InP HFETs were much larger than those of the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs HFET's, the f_{max} of conventional gate structure devices fabricated on all three materials were around 80GHz. The f_{max} of 80nm T-gate InAlAs/InGaAs/InP devices was 180GHz, clearly showing that gate resistance dominates short gate length device high frequency gain.

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Acknowledgements

This is the only bit most people read, so I hope YOU get a mention, otherwise people will wonder, "Why wasn't so and so mentioned in Iain's acknowledgements ? "

I wish to thank the late John Lamb and his successor Peter Laybourn for providing the world class research facilities of the department without which, the work of this thesis could not have been envisaged, let alone undertaken. I am grateful to Steve Beaumont for allowing me to register for this PhD in the first place (I think !), for reading the drafts so quickly, and for giving me so much intellectual freedom in deciding the course of this work.

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In the course of this PhD, there were two occasions when I REALLY felt like quitting but was persuaded to continue by two people. After quenching the magnet for the third time, Alex Ross promptly stuffed the insert back into the cryostat and told me to try again. The results of Chapter Three are testament to this persistence. Thanks Alex, where is the T-Shirt ?

I'll never forget the trauma of annealing the ohmic contacts on the thirty two device chips. Susan Ferguson kept me calm whilst we fought to get rid of the strange black blobs that just kept appearing in the device source drain gaps. At the time, I saw the whole project slipping away as there was no more material, time or motivation to start again. In the end we won, and the high frequency device results ensued. Lets just say I'm quite grateful Susan, OK ? Oh, and thanks for sorting out the photies too !

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Chapter 1 Introduction

1.1 The Heterojunction Field Effect Transistor (HFET, HEMT, MODFET, etc etc)

The Heterojunction Field Effect Transistor (HFET) is one of the most developed III-V semiconductor transistors whose operation depends on the use of a heterojunction formed between two different materials eg AlGaAs/GaAs or InAlAs/InGaAs.

In the HFET, the material structure is designed to physically separate electrons from their parent donors, leading to large electron mobilities as ionised impurity scattering is reduced. In addition, a large electron concentration is formed at a well defined plane close to the surface of the material structure.

Worldwide HFET research has led to various acronyms for the device, as shown in Table 1.1. The different names originate from the material aspect which each group thought to be important in determining device performance.

Acronym	Name	Material Aspect	Originator
HEMT	High Electron Mobility Transistor	High Electron Mobility	Fujitsu
MODFET	Modulation Doped FET	Material Doping Technique	Cornell, Illinois, Rockwell
TEGFET	Two-Dimensional Electron Gas FET	Current Transport Mechanism	Thomson CSF
SDHT	Selectively Doped Heterojunction Transistor	Material Doping Technique	AT&T Bell Labs

Table 1.1 - Heterojunction Field Effect Transistor Names and their Origins

The device structure of an HFET is identical to that of the Metal-Semiconductor Field Effect Transistor (MESFET) where current flow through a uniformly doped channel layer is modulated by a Schottky gate contact. In the case of the HFET, current flows under the gate contact via the high mobility channel. This, and other more subtle effects described in Chapter 2, results in improved high frequency noise and gain characteristics compared to conventional GaAs MESFETs.

HFET devices are used in very high speed digital applications[1.1], but in this area there is strong competition from the Heterojunction Bipolar Transistor (HBT)[1.2]. The large base resistance of the HBT[1.3] means it cannot match the high frequency noise performance of the HFET, so most HFET applications are in analogue circuitry operating at microwave and millimetre wave frequencies.

The use of high quality material systems and high resolution lithography techniques such as electron beam lithography permit HFET devices with operating frequencies above 100GHz to be fabricated. In the last year, circuits containing HFETs with bandwidths of up to 100GHz have begun to appear[1.4].

The aims of this thesis are to understand the material and device parameters which most influence the high frequency device performance of HFETs with gate lengths in the range 80-200nm. With such an understanding, it will be possible to enhance both the material structure and the device design currently in use, with the long term aim of producing circuits for operation at millimetre wave frequencies.

There are many potential applications of circuits operating above 60GHz. Earth-satellite and inter-satellite communication links benefit from the low noise properties of circuits containing HFET's. With

the exception of the 94GHz window, where HFET circuits will play an important role in low noise receivers, atmospheric attenuation suggests future applications of millimetre wave circuits will be mostly terrestrial.

One area of interest is in short distance line of sight communication systems, particularly in built-up areas where the laying of cables maybe impractical and expensive. Moving to higher frequencies results in narrower beams. This reduces the risk of interference between two signals of the same frequency, and also reduces the influence of the environment (eg large buildings) on signal propagation.

Part of the European DRIVE project, aimed at improving road safety and increasing transport efficiency across Europe, includes the implementation of collision avoidance radar systems operating at 94GHz and communication between vehicles and roadside transducers at 60GHz. Even now, microwave transceivers are used in road toll collection systems in Scandinavian countries.

In the field of optical communications systems, driver circuitry will be required for semiconductor optical modulators which are capable of >100GHz operation. HBT's may prove to be a more attractive candidate for such applications, but there seems to be no general consensus among the Optoelectronic Integrated Circuit community, as both HBT's and HFET's are currently being integrated with optical components[1.5-1.8].

1.2 Synopsis of Thesis

Following this brief introduction to the HFET and its potential millimetre wave applications, Chapter 2 introduces some theory of HFET operation, laying the basis for the remainder of the thesis. In addition, a review of the current state of the art in HFET performance is included. Chapter 3 describes the material structures used in the project, and presents results on the transport properties of them.

Chapter 4 follows with the complete HFET fabrication process where emphasis is placed on gate lithography techniques. Chapter 5 first presents the results of DC and RF device characterisation then discusses the importance of material structure choice and device design, if sub-100nm gate length HFET devices are to be optimised. The findings of the thesis are concluded in Chapter 6 together with suggestions for future work.

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Chapter 2 Theory of HFET Operation

Introduction

As the work of this thesis is based on short gate length heterojunction field effect transistors (HFETs), this chapter first describes the formation of a heterojunction. The basic properties of the heterojunction which are important to (HFET) device operation are presented with a simple analytic model which elucidates the physics governing the formation of the two Dimensional Electron Gas (2DEG) at a heterojunction interface. Next, the operation of the HFET device is considered, and figures of merit for device operation at both DC and high frequency introduced. The dependence of the figures of merit on layer structure and device design are stressed. The effects of reducing the gate length of the HFET and the related device scaling issues are then discussed.

In the final sections, the importance of material choice for optimal device performance based on the electron transport properties of a number of currently available material systems is considered. This discussion is concluded with a survey of state of the art HFET performance for a number of material systems.

2.1 Introduction to Heterojunctions

A heterojunction is formed at the interface between two dissimilar semiconductor materials. The concept of the heterojunction is almost as old as the transistor itself, with Schockley proposing in 1957 that such a structure be used as the base emitter junction of a bipolar transistor[2.1]. It was not until semiconductor crystal growth technologies such as molecular beam epitaxy (MBE) matured, that it became possible to grow semiconductor interfaces with abrupt changes in material composition on an atomic monolayer scale. Such growth technologies now allow the properties of heterojunctions to be exploited.

Until recently, the production of a defect free, abrupt heterojunction by MBE required that the lattice constants of the component materials be similar, or lattice matched. (As will be described in Section 2.8.3, current growth technologies allow interfaces to be grown between non-lattice matched materials, the so called strained layer or pseudomorphic systems). Figure 2.1.1 shows the lattice constant and energy band gap of a number of III-V semiconductor compounds.

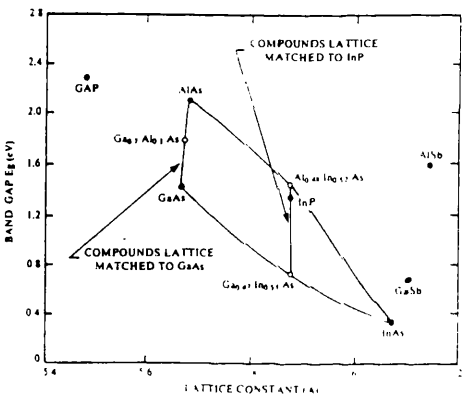

Figure 2.1.1 - Lattice Constant and Band Gap of a Number of III-V Semiconductors

The lattice constants of GaAs and $Al_xGa_{1-x}As$ are almost equal (within 1%) for all Al concentrations. This allows high quality, defect free GaAs/AlGaAs heterojunctions to be grown by MBE and as a result, the electrical properties of the heterojunction formed in this material system have been extensively studied[2.2]. Work has also been performed on other lattice matched systems such as $Ga_{0.47}In_{0.53}As/InP$[2.3] and the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ interface[2.4] which is lattice matched to InP.

A model for an ideal, abrupt heterojunction which allows most transport phenomena to be adequately explained was proposed by Anderson in 1962[2.5]. This is described below.

Figure 2.1.2(a) shows the energy band diagram of two isolated semiconductors with different electron affinities χ, work functions ψ, and energy band gaps E_g. Measured with respect to the vacuum level, the difference in conduction band edge energies of the two materials is ΔE_C, the valence band energy difference is ΔE_V, and the difference in band gap is ΔE_g. Figure 2.1.2(a) shows that $\Delta E_C = (\chi_1 - \chi_2)$ and $\Delta E_V = \Delta E_g - \Delta E_C$.

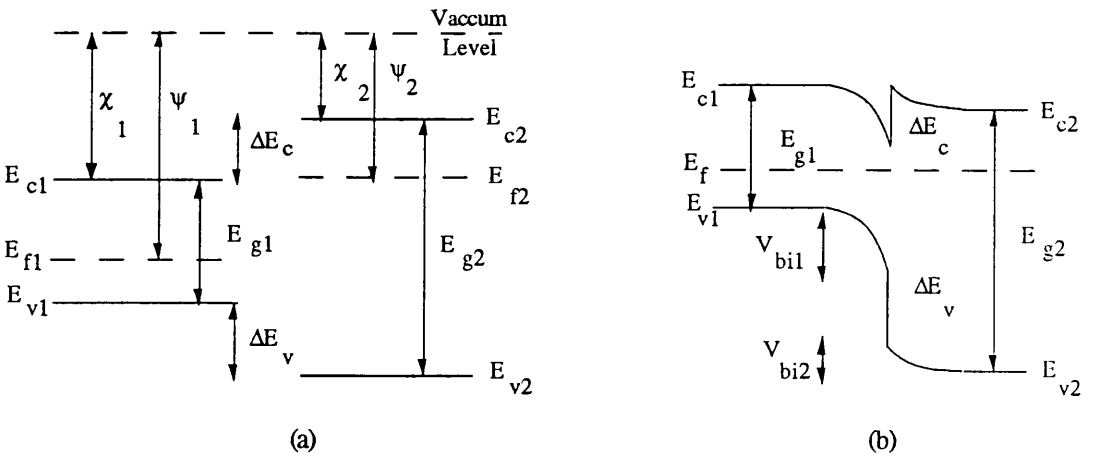

Figure 2.1.2 - Band Diagram for the Formation of a Heterojunction

When the two semiconductors are brought into intimate contact the heterojunction is formed and the equilibrium band diagram of Figure 2.1.2(b) results since the Fermi Level must coincide on each side of the interface. The total built-in voltage of the junction $V_{bi} = V_{bi1}+V_{bi2}$, is the potential resulting from charge transfer across the interface.

2.1.1 The AlGaAs/GaAs Modulation Doped Heterojunction

Studies of the electrical transport properties of heterojunctions which finally led to the invention of the HFET were stimulated by the AlGaAs/GaAs structure proposed by Esaki and Tsu in 1969[2.6] - the so called modulation doped heterostructure. It was not until 1978 however, that such a structure was realised by MBE[2.7]. In this structure, the heterojunction is formed at the interface of n-type AlGaAs and undoped GaAs. Figure 2.1.3(a) shows the energy band diagrams of the isolated n-type AlGaAs and undoped GaAs. Bringing the two materials into intimate contact results in the equilibrium conduction band diagram of the structure shown in Figure 2.1.3(b).

As a result of their greater energy, electrons in the n type AlGaAs diffuse across the interface and accumulate in the undoped GaAs, close to the interface.

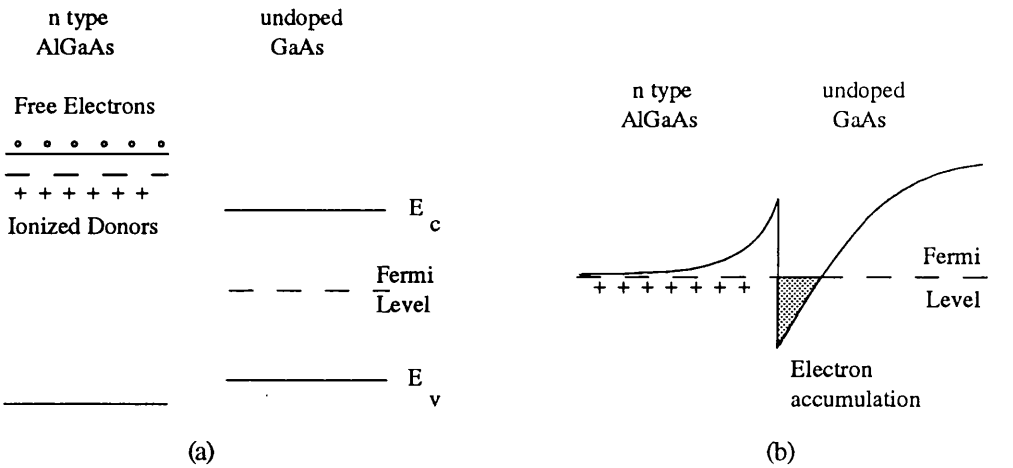

Figure 2.1.3 - Formation of Electron Accumulation Layer at an AlGaAs/GaAs Heterojunction interface using the Modulation Doping Technique

Equilibrium is reached when the diffusion is balanced by the electric field resulting from the dipole formed between the ionised donors and free electrons. The energy stored in the dipole is approximately equal to the conduction band offset ΔE_c.

The first feature to note in the modulation doped heterojunction is that the electric field in the undoped GaAs caused by the electron accumulation layer is very strong (~10^7 Vm^{-1}), and so confines the electrons in a very narrow, quasi-triangular notch of around 150-200Å close to the interface. This dimension is commensurate with the electron wavelength resulting in quantisation of the electron momentum in the direction perpendicular to the interface. As shown in Figure 2.1.4, this leads to quantisation of the electron energy into discrete sub-bands in the accumulation region, so that the minimum electron energy is raised above the conduction band edge.

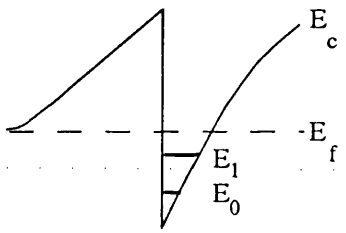

Figure 2.1.4 - Quantisation of Electrons in Accumulation Layer of Modulation Doped Heterojunction

The electrons are free to move in the plane parallel to the interface however, and so are 2 dimensional in nature. For this reason, the electron accumulation layer is usually known as a 2 Dimensional Electron Gas (2DEG). The electron distribution within the triangular well is determined by the energy level wavefunctions. A solution of Schroedingers equation[2.81] shows the 2DEG is formed around 50-70Å below the interface forming the heterojunction.

The other feature of this structure is that electrons are in the undoped GaAs, and are spatially separated from the donor atoms fixed in the AlGaAs. This spatial separation reduces the Coulombic interaction between the electrons and their parent donors - known as ionised impurity scattering - which results in an increase in the electron mobility of such structures, particularly in conditions where ionised impurity scattering is the dominant mobility limiting mechanism. Electron mobilities at AlGaAs/GaAs heterojunction interfaces are higher than those found in undoped GaAs. This is due to screening of the few impurities in the undoped GaAs by the carriers in the accumulation layer.

The incorporation of an undoped AlGaAs 'spacer' layer between the doped AlGaAs and GaAs, as shown in Figure 2.1.5, further suppresses the Coulombic interaction by increasing the spatial separation of the donors and carriers.

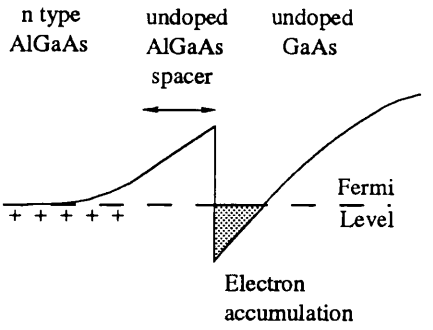

Figure 2.1.5 - Modulation Doped Heterojunction with Spacer Layer to Further Reduce Ionised Impurity Scattering

Table 2.1.1 shows recently measured mobilities as a function of temperature for both undoped GaAs and AlGaAs/GaAs heterojunctions. At low temperatures, where ionised impurity scattering is the dominant scattering mechanism, the heterojunction structure produces very high electron mobilities.

	Mobility (cm^2/Vs)			
Material	1.5K	4K	70K	300K
Undoped GaAs[2.8]		$5x10^4$	$2.11x10^5$	8500
AlGaAs/GaAs	$8.5x10^6$[2.9]	$3.5x10^6$[2.10]	$1.9x10^5$[2.11]	8200[2.11]

Table 2.1.1 - Mobility of Undoped bulk GaAs and an AlGaAs/GaAs 2DEG Structure

The large electron mobility was initially perceived as being directly transferable into improved FET device performance, and was the initial motivation for studying HFETs based on modulation doped heterostructures[2.12].

2.1.2 Model to Determine 2DEG Carrier Concentration at a Heterojunction

Once high quality 2DEG systems could be produced reliably, studies were undertaken to investigate the dependence of mobility and 2DEG carrier concentration on the layer structure parameters such as spacer layer width[2.13], AlGaAs doping concentration[2.14] and conduction band offset[2.15] (variable by varying the Al mole fraction in the AlGaAs layer). It was found that increasing the spacer layer thickness increased the mobility whilst reducing the 2DEG carrier concentration. In addition, the 2DEG carrier concentration could be increased by increasing either the conduction band offset or the AlGaAs doping concentration.

In an effort to explain these observed effects, a simple model, based on a solution of Poisson's Equation, showing the dependence of the 2DEG carrier concentration on the layer structure parameters discussed above, is now considered using the energy band diagram of the heterojunction shown in Figure 2.1.6.

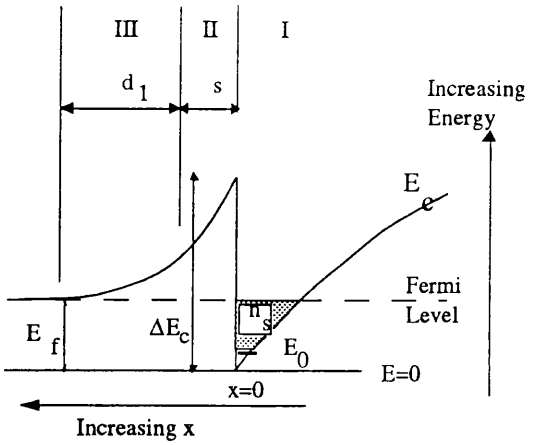

Figure 2.1.6 - Conduction Band Diagram of Modulation Doped Heterojunction

The 2DEG carrier concentration is n_S, the undoped AlGaAs spacer layer thickness is s, the n type AlGaAs has doping concentration N_d. At distance d_1 from the spacer layer, the electric field in the doped AlGaAs falls to zero. Assume that:

i) 1 energy level, E_0, in the notch is occupied

ii) the Fermi Level coincides with the conduction band edge in the AlGaAs (a valid assumption if the AlGaAs doping concentration is close to degeneracy, a doping level of around $5x10^{17}cm^{-3}$),

iii) the relative permitivity, ε, of GaAs and AlGaAs are equal :

In region I (undoped GaAs), at the AlGaAs/GaAs interface (x=0), Gauss's Law gives

$$F(0) = \frac{-qn_s}{\varepsilon}$$

where F is the electric field.

In region II (undoped AlGaAs), at the interface (x=0), matching of the electric field gives

$$F(0) = \frac{-qn_s}{\varepsilon}$$

In Region II, From Poisson's Equation, where V is the electrostatic potential,

$$\frac{d^2V}{dx^2} = 0 \text{ as the spacer layer is undoped.}$$

But,

$$\frac{dV}{dx} = -F(x) = \text{constant} = \frac{qn_s}{\varepsilon}$$

$$\therefore V(x) = \frac{qn_s x}{\varepsilon} + \text{constant}$$

But

$$V(0) = \frac{-\Delta E_c}{q}$$

$$\therefore V(x) = \frac{qn_s x}{\varepsilon} - \frac{\Delta E_c}{q}$$

so that, at x=s,

$$F(s) = \frac{-qn_s}{\varepsilon}$$

and

$$V(s) = \frac{qn_s s}{\varepsilon} - \frac{\Delta E_c}{q}$$

Now move the origin so that x=0 is at the interface between the undoped and doped AlGaAs. Then at x=0,

$$F(0) = \frac{-qn_s}{\varepsilon}$$

$$V(0) = \frac{qn_s s}{\varepsilon} - \frac{\Delta E_c}{q}$$

In Region III (doped AlGaAs) from Poissons Equation,

$$\frac{d^2V}{dx^2} = \frac{-qN_d}{\varepsilon}$$

so that

$$V(x) = -\frac{qN_d x^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(x + s) - \frac{\Delta E_c}{q} \qquad (2.1.1)$$

and

$$F(x) = \frac{qN_d x}{\varepsilon} - \frac{qn_s}{\varepsilon} \qquad (2.1.2)$$

At $x = d_1$, $F(d_1) = 0$, so that

$$N_d d_1 = n_s \qquad (2.1.3)$$

In other words, the charge that diffuses to the 2DEG does so from between the spacer layer and the point at which the electric field becomes zero in the doped AlGaAs.

Considering Figure (2.1.6) energy conservation gives

$$\frac{-E_f}{q} = V(d_1)$$

so that

$$E_f = \frac{q^2 N_d d_1^2}{2\varepsilon} + \Delta E_c - \frac{q^2 n_s}{\varepsilon}(d_1 + s) \qquad (2.1.4)$$

Using (2.1.3)

$$E_f + \frac{q^2 n_s}{\varepsilon}\left(\frac{n_s}{N_d} + s\right) - \frac{q^2 n_s^2}{2\varepsilon N_d} = \Delta E_c$$

ie

$$E_f + \frac{q^2 n_s s}{\varepsilon} + \frac{q^2 n_s^2}{2\varepsilon N_d} = \Delta E_c \qquad (2.1.5)$$

Assuming single subband occupation, the Fermi energy can be calculated from the 2 dimensional density of states function D_s

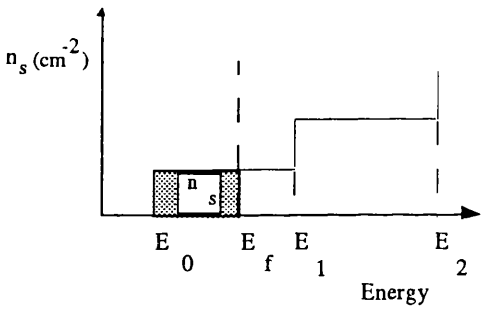

Figure 2.1.7 - 2 Dimensional Density of States Function

As the density of states in 2-D is constant in a given subband (Figure 2.1.7) the sheet electron concentration n_S is simply the integral under the density of states function from the minimum sub-band energy E_o to the Fermi energy E_f

$$n_S = (E_f - E_o) D_S \qquad (2.1.6)$$

where

$$D_s = \frac{8m^*}{\pi h^2}$$

m^* is the electron effective mass, and h is Plancks Constant.

The energy of the i^{th} subband in a triangular potential well above the conduction band edge can be shown to have the form[2.16],

$$E_i = (\tfrac{1}{2})(i + \tfrac{3}{4})^{\frac{2}{3}} \left(\frac{3q^2 h n_s}{2\varepsilon (m^*)^{\frac{1}{2}}} \right)^{\frac{2}{3}} \qquad (2.1.7)$$

Combining (2.1.6) and (2.1.7) and assuming single subband occupation, gives the following expression for the Fermi energy :

$$E_f = \frac{n_s \pi h^2}{8m^*} + \frac{1}{2}\left(\frac{3q^2 h n_s}{2\varepsilon (m^*)^{\frac{1}{2}}}\right)^{\frac{2}{3}} \qquad (2.1.8)$$

Substituting (2.1.8) in (2.1.5) , gives the following 6th order polynomial for $(n_s)^{1/3}$

$$\frac{q}{2\varepsilon N_d}\left(n_s^{\frac{1}{3}}\right)^6 + \left(\frac{qs}{\varepsilon} + \frac{\pi h^2}{8qm^*}\right)\left(n_s^{\frac{1}{3}}\right)^3 + \frac{1}{2}\left(\frac{q}{m^*}\left(\frac{3h}{2\varepsilon}\right)^2\right)^{\frac{1}{3}}\left(n_s^{\frac{1}{3}}\right)^2 - \frac{\Delta E_c}{q} = 0 \qquad (2.1.9)$$

Solving this expression for n_S gives the dependence of 2DEG carrier concentration on the variables in epitaxial layer design namely, conduction band offset ΔE_C, AlGaAs doping concentration N_d, and AlGaAs spacer layer thickness, s.

Figures 2.1.8 and 2.1.9 show the variation of n_S with these parameters.

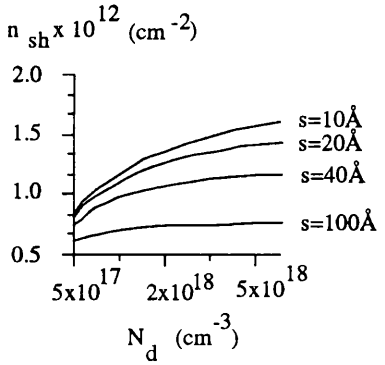

Figure 2.1.8 - Dependence of n_s on N_d and s for ΔE_c = 0.3eV

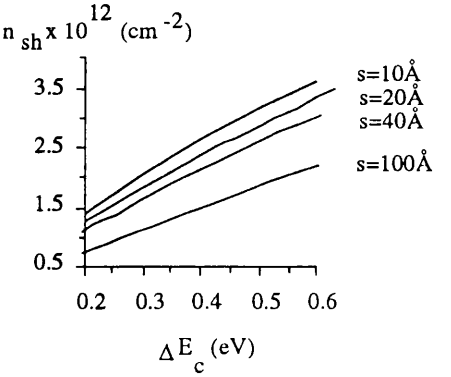

Figure 2.1.9 - Dependence of n_s on ΔE_c and s for $N_d = 3x10^{18}cm^{-3}$

From Figures 2.1.8 and 2.1.9, the 2DEG carrier concentration n_s

i) increases with increasing conduction band offset ΔE_c as the energy stored in the dipole formed as a result of the charge transfer is approximately given by the conduction band offset.

ii) decreases with increasing spacer layer thickness as charge transfer across the interface is most efficient if the distance the carriers have to travel is reduced.

iii) increases with increasing AlGaAs doping level as more carriers are available for charge transfer across the interface at small distances from the interface where the charge transfer is efficient.

2.1.3 Modulation of 2DEG Concentration using a Schottky Contact

Having established that the 2DEG carrier concentration can be varied by changing material parameters such as spacer layer thickness, interest turned to the question of whether the accumulation layer could be controlled externally, by using for example a Schottky contact. Again a solution of Poisson's equation, this time with a Schottky contact placed on top of a layer structure containing a modulation doped heterostructure, provides insight into possibilities of external charge control of a 2DEG formed at a heterojunction. A typical layer structure is shown in Figure 2.1.10. The conduction band diagram of the system is shown quantitatively in Figure 2.1.11.

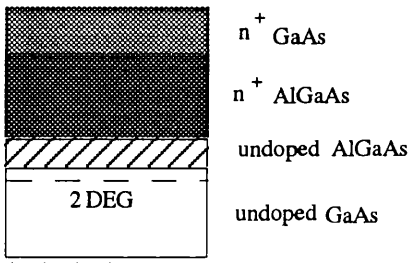

Figure 2.1.10 - Heterostructure with Schottky Contact to Provide External Control of the 2DEG Electron Concentration

In addition to the heterojunction structure previously considered, a layer of n-type GaAs is grown on top of the doped AlGaAs layer to prevent the formation of a surface aluminium oxide layer when the structure is removed from the high vacuum MBE growth chamber. As most layer structures for the fabrication of HFET devices include a doped GaAs cap to reduce the contact resistance, the following analysis assumes the capping layer to be doped.

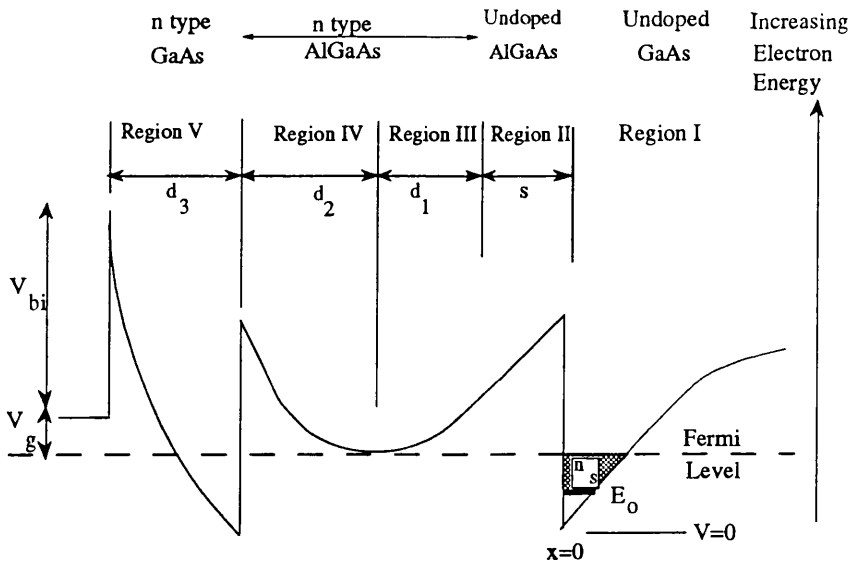

Figure 2.1.11 - Conduction Band Diagram of AlGaAs/GaAs Modulation Doped Heterostructure with Schottky Contact

The doped AlGaAs layer is depleted of electrons by two separate sources - the layer supplies the 2DEG with carriers as discussed previously and is also affected by surface depletion from the Schottky barrier.

At present, it will be assumed that the doped AlGaAs layer thickness is such that the two depletion regions meet.

The solution of Poissons Equation for the above structure is identical to that described in Section 2.1.2 up to the distance $x = d_1 + s$, at which the electric field due to depletion of the doped AlGaAs layer resulting from the formation of the 2DEG falls to zero.

At $x = d_1 + s$, the voltage and electric field given by are Equations (2.1.1) and (2.1.2) ie

$$V(d_1 + s) = \frac{-qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) - \frac{\Delta E_c}{q}$$

$$F(d_1 + s) = \frac{qN_{d1}d_1}{\varepsilon} - \frac{qn_s}{\varepsilon}$$

The analysis now proceeds as before,

Move the origin to $x = d_1 + s$ ie in the region of doped AlGaAs at the junction of the two depletion regions so that

$$V(0) = \frac{-qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) - \frac{\Delta E_c}{q} \qquad (2.1.10)$$

Solving Poissons Equation in Region IV and using (2.1.10) gives

$$F(x) = \frac{qN_{d1}x}{\varepsilon}$$

and

$$V(x) = \frac{-qN_{d1}x^2}{2\varepsilon} - \frac{qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) - \frac{\Delta E_c}{q}$$

so that

$$F(d_2) = \frac{qN_{d1}d_2}{\varepsilon}$$

and

$$V(d_2) = \frac{-qN_{d1}d_2^2}{2\varepsilon} - \frac{qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) - \frac{\Delta E_c}{q}$$

Next move the origin once more ie $x \Rightarrow x + s + d_1 + d_2$

At x=0,

$$F(0) = \frac{qN_{d1}d_2}{\varepsilon} \qquad (2.1.11)$$

and at the GaAs cap side of the interface $x = 0^+$,

$$V(0_+) = \frac{-qN_{d1}d_2^2}{2\varepsilon} - \frac{qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) \qquad (2.1.12)$$

Solving Poissons Equation in Region V, and using (2.1.11) and (2.1.12) gives

$$V(x) = \frac{-qN_{d2}x^2}{2\varepsilon} - \frac{qN_{d1}d_2x}{2\varepsilon} - \frac{qN_{d1}d_2^2}{2\varepsilon} - \frac{qN_{d1}d_1^2}{2\varepsilon} + \frac{qn_s}{\varepsilon}(d_1 + s) \qquad (2.1.13)$$

At the surface, the potential boundary condition is

$$V = V_{bi} + V_g - \frac{E_f}{q} \qquad (2.1.14)$$

Where V_{bi} is the built in surface potential and E_f is the Fermi Energy with respect to the bottom of the conduction band at the heterointerface.

Equating (2.1.13) and (2.1.14), using Equation (2.1.3) and calling the doped AlGaAs thickness $d = d_1 + d_2$, yields

$$V_{bi} + V_g - \frac{E_f}{q} = \frac{-qN_{d2}d_3^2}{2\varepsilon} - \frac{qN_{d1}d_3}{\varepsilon}\left(d - \frac{n_s}{N_{d1}}\right) - \frac{qN_{d1}}{2\varepsilon}\left(d^2 - \frac{2dn_s}{N_{d1}} + \frac{2n_s^2}{N_{d1}^2}\right) + \frac{qn_s}{\varepsilon}\left(\frac{n_s}{N_{d1}} + s\right) \qquad (2.1.16)$$

In other words, the 2DEG sheet electron concentration can be varied by varying the potential applied to the Schottky contact on the surface of the structure. Figure 2.1.12 shows the dependence of the 2DEG concentration on applied gate voltage for the layer structure shown in Table 2.1.2 obtained by solving (2.1.16).

Parameter	ΔE_c (eV)	s (Å)	N_{d1} (cm^{-3})	d (Å)	N_{d2} (cm^{-3})	d_3 (Å)
Value	0.25	30	$1x10^{18}$	250	$1x10^{18}$	200

Table 2.1.2 - Parameters used in Solution of (2.1.16)

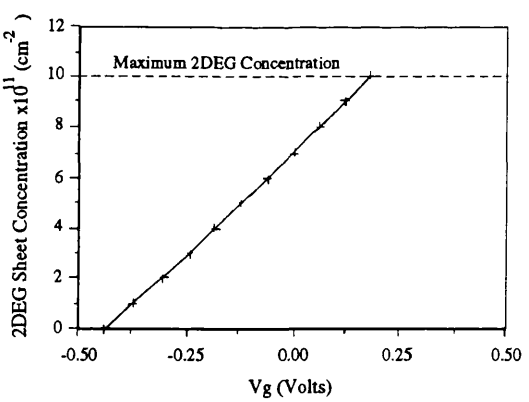

Figure 2.1.12 - Dependence of 2DEG Carrier Concentration of Applied Gate Voltage for Material System of Table 2.1.2

The 2DEG concentration can be varied from complete annihilation to the maximum concentration determined by the conduction band offset, spacer layer thickness and AlGaAs doping level which, for the parameters of Table 2.1.2 was calculated to be $1.0x10^{12}cm^{-2}$ using Equation (2.1.9). In the region

between maximum 2DEG concentration and complete annihilation, assuming the Fermi level energy is independent of applied gate bias, there is a linear dependence of sheet electron concentration with gate voltage as can be seen by differentiating (2.1.16). Differentiation yields

$$-\frac{dV_g}{dn_s} = \frac{q}{\varepsilon}(d_3 + d + s)$$

or, with $h = d_3 + d + s$

$$-\frac{dV_g}{dn_s} = \frac{qh}{\varepsilon} \qquad (2.1.17)$$

That is, the system behaves like a parallel plate capacitor, where the plates of the capacitor (separated by a distance $h = d_3 + d + s$) are the Schottky contact and the 2DEG.

2.1.4 Parallel Conduction

A layer of undepleted material is formed in the doped AlGaAs region if the Schottky contact is forward biased more than required to establish the maximum possible 2DEG concentration. This undepleted region of doped AlGaAs is usually termed the "parallel conduction" region, because there is free charge available for conduction in parallel with the 2DEG. The formation of the parallel conduction layer occurs when the doped AlGaAs layer is so thick that the depletion regions due to the 2DEG and the surface potential do not join, as shown in Figure 2.1.13.

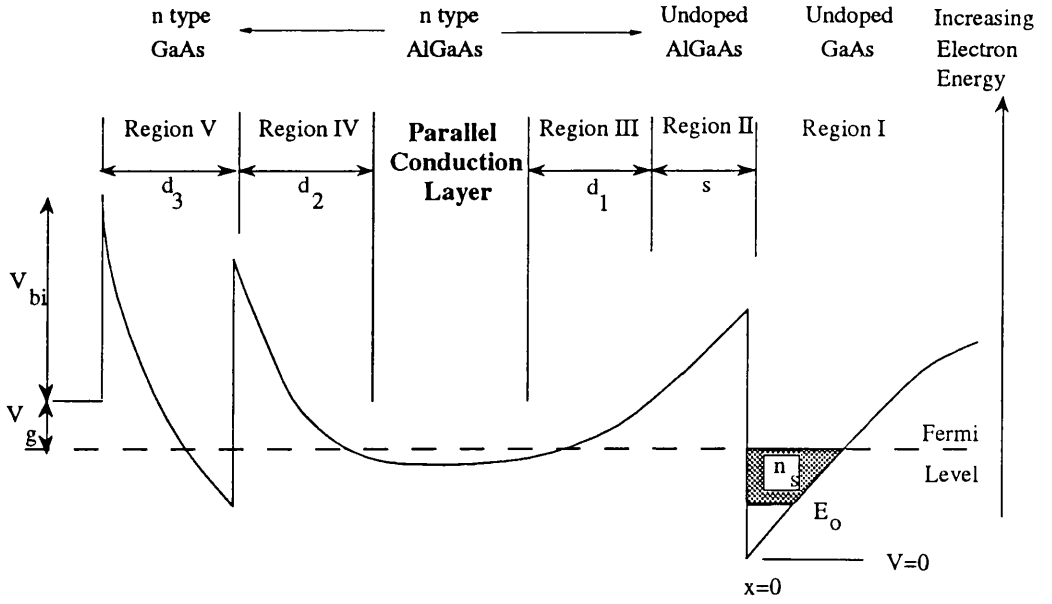

Figure 2.1.13 - AlGaAs/GaAs Heterostructure with Parallel Conduction

In this case, the 2DEG carrier concentration will not be modulated by the application of a voltage to a surface Schottky contact until all excess carriers have been depleted from the parallel conducting layer by reverse biasing the Schottky. As will be described in Section 2.7, parallel conduction has both advantages and disadvantages to the operation of HFET's.

2.1.5 Summary of Basic Heterostructure Properties

The simple analytical models presented above are useful for predicting general trends observed in heterojunction systems and so are invaluable as introductory tools to understanding the physics of such systems. However, simplifying assumptions have been made in the models which compromise the validity of any quantitative results obtained. In particular, the reduced dimensionality of the electron accumulation region requires that the Schroedinger equation be solved if the true spatial electron distribution is to be determined. This electron distribution should then be used in the evaluation of Poisson's Equation to correctly calculate the conduction band profile. Only by self-consistently solving Poissons Equation and Schroedingers Equation is it possible to model the system accurately, taking into account such effects as electron tunnelling into the undoped AlGaAs spacer layer.

The simple models presented above do account for the general trends observed in 2DEG systems namely,

- n_s increases with increasing ΔE_C
- n_s decreases with increasing spacer layer thickness.
- n_s increases with increased AlGaAs doping level.
- n_s can be modulated by varying the bias on a Schottky contact placed on the surface of a heterostructure material system and that, to first order, the whole system can be envisaged as a parallel plate capacitor.

Armed with the above facts, a significant amount of progress can be made towards understanding the operation of HFET's and optimising their design, as will now be explained.

2.2 The Heterojunction Field Effect Transistor (HFET)

The following terminology is equally applicable to any heterojunction based field effect transistor, but it is easiest to explain by considering a specific example, the AlGaAs/GaAs HFET. This is a 3 terminal device shown schematically in Figure 2.2.1.

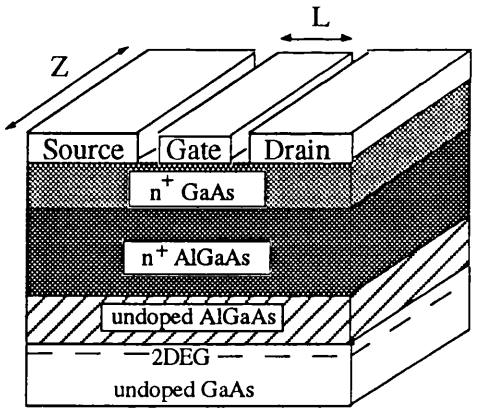

Figure 2.2.1 - The Heterojunction Field Effect Transistor (HFET)

This material structure was described in Section 2.1.3, with a 2DEG formed at the undoped GaAs/AlGaAs interface. Current passes between the ohmic source and drain contacts via the 2DEG by applying a positive voltage to the drain with respect to the source (which is usually grounded). The amount of current passing through the 2DEG is determined by the sheet electron concentration beneath the Schottky

gate contact of length L, which is placed between the source and drain contacts. As shown in Section 2.1.3, the sheet electron concentration in a 2DEG structure below a Schottky contact can be modulated by varying the bias on the Schottky (again with respect to the source). As the drain bias is dropped across the device, the 2DEG carrier concentration at a given position under the gate is influenced by the sum of the gate bias and the contribution of the drain bias at that position, ie the 2DEG carrier concentration varies along the length of the gate, being smallest at the drain end where the drain bias contribution is greatest. By reverse biasing the gate until the 2DEG is annihilated and no current can flow between source and drain, the device is deemed to be "pinched off".

If the gate is forward biased sufficiently, a channel of undepleted carriers will be established in the doped AlGaAs layer, and in such a case, there are two paths by which current can travel from source to drain:

i) via the 2DEG

ii) through the doped, undepleted AlGaAs via the parallel conduction layer.

The output characteristic of a HFET is shown in Figure 2.2.2.

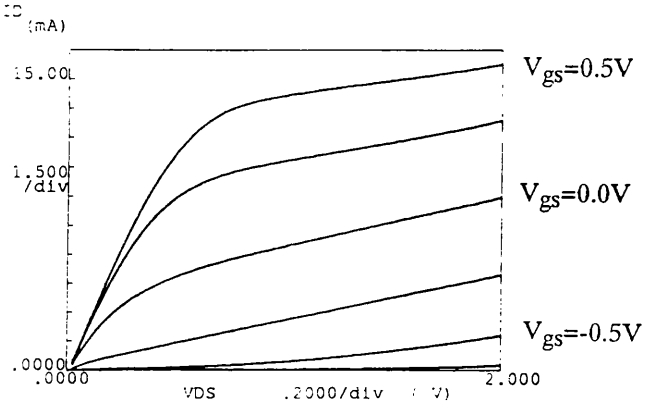

Figure 2.2.2 - Output Characteristic of an HFET

It can be seen that there is a family of curves, each associated with a given gate bias (V_{gs}). The drain-source current (I_{ds}), drain-source voltage (V_{ds}) relationship falls into 2 distinct regions. At low V_{ds}, the characteristic is ohmic, ie a linear relationship exists between I_{ds} and V_{ds}. In this region, as V_{ds} and hence the electric field is increased, the carrier velocity in the 2DEG and hence the drain source current is increased. There comes a point however, when the scattering events experienced by the carriers (predominantly optical phonon and intervalley scattering in the 2DEG at room temperature) causes a saturation of the carrier velocity. Any subsequent increase in energy of the carriers supplied by increasing the field is lost to the crystal lattice. Hence, the second region of the characteristic is at higher V_{ds} (and thus electric field) in which I_{ds} is independent of V_{ds}.

The current in this region can be written as :

$$I_{ds} = Z\, q\, v_{eff}\, n_s \qquad (2.2.1)$$

where q is the elemental charge, v_{eff} is the effective velocity of carriers in the 2DEG channel, n_s is the 2DEG sheet electron concentration (a function of Schottky gate bias) and Z is the device width.

2.3 Basic Device Figures of Merit

An important figure of merit for a FET is the transconductance (g_m) which is defined as

$$g_m = \left.\frac{dI_{ds}}{dV_{gs}}\right|_{V_{ds}}$$

This is a hybrid gain term showing the change in output current for a given change in input voltage. The transconductance can be re-expressed in terms of more basic parameters which are a function of the material system as follows,

Differentiating 2.2.1 above

$$dI_{ds} = q\, v_{eff}\, Z\, dn_s \qquad (2.3.1)$$

Now, (2.1.17) gave

$$-\frac{dV_g}{dn_s} = \frac{qh}{\varepsilon}$$

where h is the Schottky gate/2DEG separation.

Combining (2.3.1) and (2.1.17) gives

$$g_m = \frac{\varepsilon v_{eff} Z}{h} \qquad (2.3.2)$$

ie the transconductance is proportional to the effective velocity in the channel.

The g_m is also inversely proportional to the gate/2DEG separation.

Another important FET parameter is the output conductance (g_o) defined as :

$$g_o = \left.\frac{dI_{ds}}{dV_{ds}}\right|_{V_{gs}} = \frac{1}{R_{out}}$$

where R_{out} is the output resistance.

The voltage gain of the device is defined as $A_v = \frac{\delta V_{ds}}{\delta V_{gs}} = \frac{g_m}{g_o}$

As previously described in Section 2.1.3, the Schottky gate/2DEG system can be thought of as a parallel plate capacitor. For the gate structure of Figure 2.2.1, the gate capacitance can be written as

$$C_g = \frac{L_{eff}\varepsilon Z}{h} \qquad (2.3.3)$$

where L_{eff} is the effective gate length of the device. Due to fringing effects at the edge of the gate L_{eff} is greater than the physically defined gate length, L.

2.3.1 Parasitic Resistances

By reconsidering Figure 2.2.1, it can be seen that there are regions of semiconductor between the edges of the gate contact and the edges of the source and drain contacts. The sheet resistance of these regions contribute to the source and drain resistances of the device. An additional contribution arises from the finite resistance of the ohmic contacts to the semiconductor structure. The drain source voltage can then be re-expressed as

$$V_{ds} = V'_{ds} + I_{ds}(R_s + R_d)$$

where V_{ds} is the applied external drain source voltage, V'_{ds} is the drain source voltage dropped across the gate region and R_s and R_d are the parasitic source and drain resistances.

Between the gate and source contacts

$$V_{gs} = V'_{gs} + I_{ds} R_s \qquad (2.3.4)$$

where V_{gs} is the applied external gate source voltage and V'_{gs} is the voltage across the gate source Schottky contact.

Differentiating (2.3.4) gives,

$$dV_{gs} = dV'_{gs} + dI_{ds} R_s \qquad (2.3.5)$$

Substituting (2.3.5) in the transconductance expression (2.3.2) results in

$$g_m^{ext} = \frac{g_m^{int}}{1 + g_m^{int} R_s} \qquad (2.3.6)$$

where $g_m{}^{int}$ is the internal device transconductance. Thus, the measured transconductance is always smaller than the actual intrinsic device transconductance.

2.4 HFET's at RF

Most HFET applications are found at microwave and millimetre wave frequencies, particularly as low noise amplifiers In most applications, the FET is operated in the common source mode, ie the gate and drain contacts of the device are DC biased with respect to the source, resulting in operation at a given point on the DC output characteristic. An RF input signal (superimposed on the DC bias), is then supplied to the gate of the device with the output RF signal detected at the drain contact as shown in Figure 2.4.1.

To model the response of a FET at microwave frequencies, the device can be considered as a collection of lumped circuit elements, each of which has some physical significance in the FET device. The FET can be broken down into 2 regions, the intrinsic and extrinsic (or parasitic) parts of the device, as shown in Figure 2.4.1. This also shows the physical positioning of the components used in the equivalent circuit model.

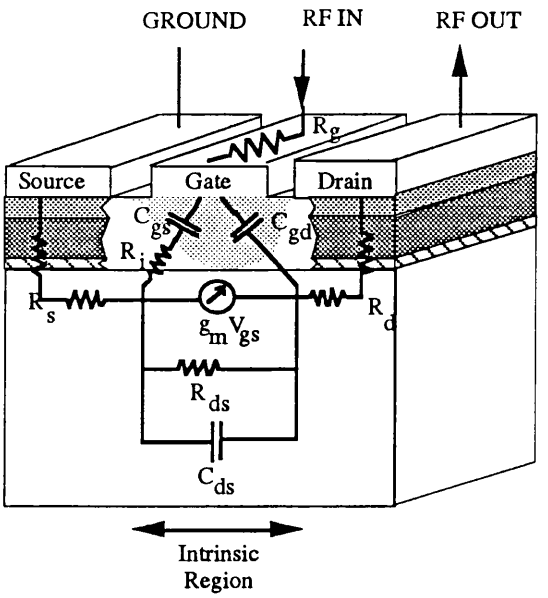

Figure 2.4.1 - Position of Equivalent Circuit Components in a HFET

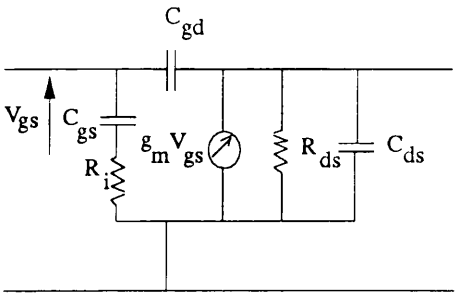

Figure 2.4.2 - Intrinsic Equivalent Circuit of HFET

The intrinsic area of the device is associated with the region below the gate. This region can be modelled as a capacitor C_{gs} in series with a resistor R_i. These lumped elements represent the effect of the distributed capacitor/resistor network along the length of the 2DEG under the gate. 2 D confinement means the capacitance is essentially constant along the channel. The varying sheet electron concentration caused by the drain bias variation along the length of the gate, results in the sheet resistance of the channel changing with position. In addition to the gate capacitance and intrinsic channel resistance, the intrinsic device gain is represented by a current generator of value $g_m V_{gs}$, where g_m is the intrinsic transconductance and V_{gs} is the voltage dropped across the gate capacitance. This follows from the definition of transconductance. The finite output conductance of the FET can be represented by placing a resistor, R_{ds} in parallel with the current generator. The capacitance C_{ds} in parallel with R_{ds} originates from the doped source and drain regions separated by the depletion region under the gate. Finally, the part of the gate capacitance beyond the drain end of the gate due to the depletion region caused by the drain bias is modelled as C_{gd}, the feedback capacitor. Taking the components from Figure 2.4.1, the intrinsic device equivalent circuit can be constructed as shown in Figure 2.4.2.

The extrinsic components of the circuit can be added by considering Figure 2.4.1. Between the source contact and the edge of the gate region of the device is a parasitic resistor R_s composed of 2 parts:

i) the contact resistance between the contact and the semiconductor

ii) the sheet resistance of the semiconductor between the edges of the source and gate contacts.

Both these resistances should be minimised by optimising the ohmic contact technology and reducing the semiconductor sheet resistance by having a large electron mobility and carrier concentration in the region. The drain region of the device produces parasitic resistances in the same way as the source region, resulting in the parasitic resistance R_d.

The gate resistance R_g, is modelled in series with the gate capacitance. As will be discussed in detail in Chapter 5, the gate resistance has a significant effect on device performance.

Adding the extrinsic components to the equivalent circuit results in the final model shown in Figure 2.4.3.

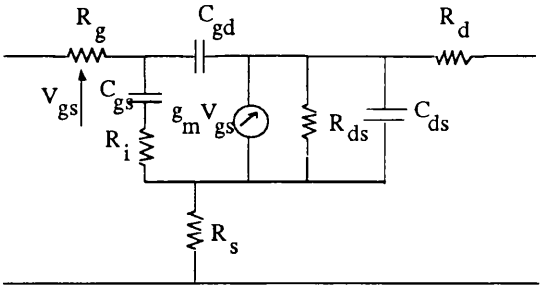

Figure 2.4.3 - Extrinsic Equivalent Circuit of HFET

The equivalent circuit model can be used to gain insight into the high frequency performance of a FET, in particular, which components should be optimised to maximise device performance.

Before continuing with a discussion of the figures of merit for a device at RF, the concept of Scattering Parameters used in microwave measurements is introduced.

2.5 Scattering Parameters

The RF measurement system used throughout this work was a Wiltron 360 Automated Vector Network Analyser capable of measuring Scattering Parameters (S-Parameters) up to 60GHz. S-Parameters are the elements of a matrix describing input and output power levels of a 2-port device, and are used in preference to h,y or z parameters at microwave frequencies. S-Parameters are chosen because they are easiest to measure at frequencies where transmission line methods have to be used.

In Figure 2.5.1, a_1, b_1, a_2, and b_2 are signals into and out of Ports 1 and 2 respectively.

a and b are defined as the square root of power, so $(a_1)^2$ is the power incident at Port 1 and $(b_2)^2$ is the power out of Port 2.

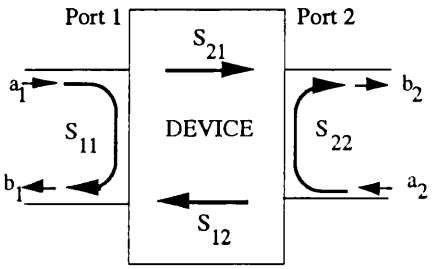

Figure 2.5.1 - S-Parameters of a 2 Port Device

The output and input signals can be related by

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

When $a_2 = 0$,

$$S_{11} = \frac{b_1}{a_1} \text{ and } S_{21} = \frac{b_2}{a_1}$$

and when $a_1 = 0$,

$$S_{12} = \frac{b_1}{a_2} \text{ and } S_{22} = \frac{b_2}{a_2}$$

Thus

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

To measure S_{11} or S_{21}, a_2 must be set to zero. This can be achieved in a microwave system by terminating the output of the 2 port under test with the characteristic impedance of the measurement system (usually 50Ω). No power is reflected back into the device. To measure any of the S-Parameters, it is only necessary to present the input or output of the 2 port with the characteristic impedance. This is particularly important when measuring over a large bandwidth, as the characteristic impedance is independent of frequency. This shows the advantage of using S-Parameters to characterise a 2 port at very high frequency. To measure h,y or z parameters, the ports of the device have to be presented with open or short circuits, which are very difficult to maintain over a large bandwidth because of the small signal wavelength.

Using well known conversion formulae[2.18] it is possible to convert from S-parameters to h,y or z parameters.

2.6 RF Figures of Merit

There are a number of figures of merit for any device operating at high frequency:

i) the device f_T

ii) the maximum available gain (MAG) at a given frequency

iii) the maximum frequency of operation, f_{max}

iv) the noise figure, NF.

2.6.1 Transition Frequency, f_T

The f_T (transition frequency) of a device is defined as the frequency at which the short circuit current gain falls to unity ie $i_{out} / i_{in} = 1$ with $v_{out} = 0$, or using the hybrid parameter matrix to represent the device as a 2 port, $h_{21} = 1$. The h parameters of the device can be derived from S-parameters. An expression for f_T can be derived from the equivalent circuit model when the output (the drain) is shorted to ground (the source). Using the intrinsic equivalent circuit of the HFET (Figure 2.4.2) with the output shorted :

$$i_{out} = g_m V_{gs}$$

and

$$i_{in} = j\omega (C_{gs} + C_{gd}) V_{gs} = j\omega C_g V_{gs}$$

thus

$$\frac{i_{out}}{i_{in}} = \frac{g_m}{j\omega C_g} \qquad (2.6.1)$$

or

$$|h_{21}| = \frac{g_m}{2\pi f C_g}$$

so that

$$f_T = \frac{g_m}{2\pi C_g} \qquad (2.6.2)$$

Where f is the frequency of operation.

Note that $|h_{21}|$ is inversely proportional to frequency, so a plot of $|h_{21}|$ in dB against log(f) will decrease at 20dB/Decade of frequency until it reaches the frequency axis at $f = f_T$.

Substituting the expressions for g_m and C_g derived earlier (2.3.2 and 2.3.3), gives

$$f_T = \frac{v_{eff}}{2\pi L_{eff}} = \frac{1}{2\pi\tau_{eff}} \qquad (2.6.3)$$

Where τ_{eff} is the effective transit time under the gate of the device, ie the f_T gives a measure of the effective velocity of carriers under the gate of a device.

By including the parasitic elements, the expression for f_T becomes more complicated[2.19],

$$f_T = \frac{g_m}{2\pi[(C_{gs} + C_{gd})(1 + \frac{R_s + R_d}{R_{ds}}) + g_m C_{gd}(R_s + R_d)]}$$

It can be seen that the gate resistance has no effect on device f_T.

To study the effects of the parasitic source and drain resistances on the device f_T , a modelling package such as Touchstone can be used. Here, the h parameters, and thus f_T can be evaluated by calculating the frequency response of the equivalent circuit. Touchstone allows the circuit topology to be user defined, and the element values to be varied. The dependence of f_T on parasitic resistances was studied using the circuit shown in Figure 2.6.1.

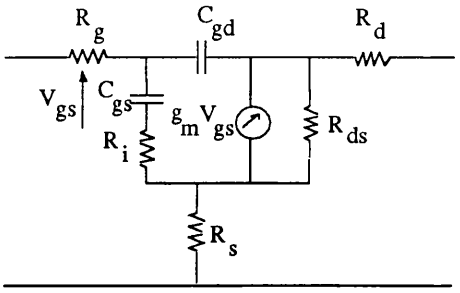

Figure 2.6.1 - Equivalent Circuit used to Determine f_T Dependence on R_s and R_d

Element	R_g	C_{gs}	C_{gd}	R_i	R_{ds}	g_m
Value	20Ω	40fF	10fF	10Ω	200Ω	35mS

Table 2.6.1 - Element Values of Equivalent Circuit

The intrinsic element values, typical of a 100nm gate length HFET, are shown in Table 2.6.1.
First, R_s and R_d were set to zero, and the intrinsic f_T evaluated. Then, R_s and R_d were varied in the range 0-50Ω. The results of this analysis are shown in Figure 2.6.2.

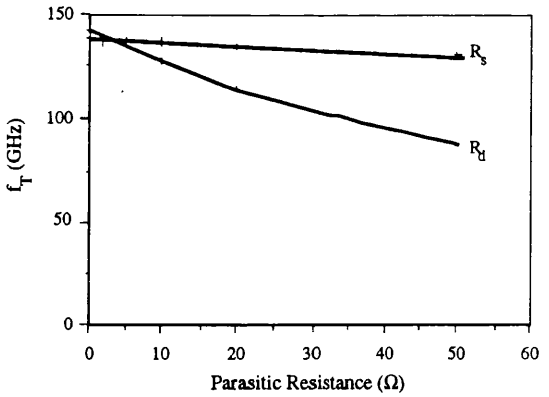

Figure 2.6.2 - Dependence of f_T on R_s and R_d

Typical values of R_s and R_d are around 5Ω so it can be seen that the f_T is insensitive to the effects of parasitic source and drain resistances.

As discussed above, the f_T of a device is related to the transit time of carriers under the gate of the device. It has been argued[2.20] that the total transit time consists of a number of delays associated with the gate region of the device

$$\tau_{eff} = \tau_i + \tau_{ch} + \tau_d$$

where,

τ_i is the intrinsic transit time L_g / v_{eff} ie the time to transit the metallurgic gate length

τ_{ch} is the channel charging delay time - the time constant associated with the charging of the gate capacitance via the channel resistance R_i

τ_d is the drain delay - the time to transit the depletion region extending beyond the drain end of the gate caused by the drain bias, and giving rise to an increase in the effective gate length of the device
($\tau_d \sim (L_{eff} - L_g) / v_{eff}$)

By considering the origin of each of these delays, the device f_T can be maximised by

i) minimising the gate length and increasing the effective velocity of the carriers.

ii) maintaining a large current density to reduce the charging time of the channel.

iii) minimising the depletion region extension at the drain end of the gate.

2.6.2 The Maximum Available Gain, MAG and Maximum Frequency of Operation, f_{max}.

In Section 2.6.1, an expression for device current gain was derived. To determine power gain (G_p), the device has to be presented with a load.

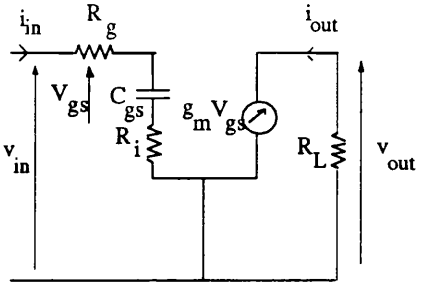

Figure 2.6.3 - Equivalent Circuit to Determine Power Gain

Consider the first order equivalent circuit of Figure 2.6.3, with the output connected to a load R_L.

First, the voltage gain $G_v = \left|\frac{v_{out}}{v_{in}}\right|$ is derived.

From Figure 2.6.3,

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_L}{1 + j\omega C_g (R_g + R_i)}$$

ie

$$\left|\frac{v_{out}}{v_{in}}\right| = \frac{g_m R_L}{[1 + \omega^2 C_g^2 (R_g + R_i)^2]^{\frac{1}{2}}}$$

In the limit of $[\omega C_g (R_g + R_i)]^2 > 1$

$$G_v \approx \frac{g_m R_L}{\omega C_g (R_g + R_i)} = \frac{f_T}{f} \frac{R_L}{R_g + R_i} \qquad (2.6.4)$$

The power gain is defined as the product of the current and voltage gains. Combining Equations (2.6.1), (2.6.2) and (2.6.4) gives,

$$G_p = \frac{g_m^2 R_L}{\omega^2 C_g^2 (R_g + R_i)} = \left(\frac{f_T}{f}\right)^2 \frac{R_L}{R_g + R_i}$$

For a HFET with output resistance R_{ds}, maximum power gain would be obtained when $R_L = R_{ds}$, then

$$G_p = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4(R_g + R_i)}$$

The frequency at which the maximum power gain falls to unity, f_{max}, can be defined as

$$f_{max} = \frac{f_T}{[4\frac{(R_g + R_i)}{R_{ds}}]^{\frac{1}{2}}}$$

Similar analyses using the complete extrinsic equivalent circuit of Figure 2.4.3 yield[2.21]

$$f_{max} = \frac{f_T}{2\left(\frac{(R_g + R_i + R_s}{R_{ds}} + 2\pi f_T R_g C_{gd}\right)^{\frac{1}{2}}}$$

and Maximum Available Gain (MAG), the maximum power gain with the input and output simultaneously and conjugately matched as[2.22]

$$MAG = \frac{(f_T / f)^2}{4(\frac{R_g + R_i + R_s}{R_{ds}}) + 4\pi f_T C_{gd}(2R_g + R_i + R_s)}$$

From these expressions, it can be observed that to produce a device with a large MAG and high f_{max}, the device f_T must be maximised whilst the parasitic resistances R_g and R_s must be minimised. In addition the output resistance R_{ds} of the device must be maximised.

As the gate length is reduced to increase the f_T, the gate resistance can become very large[2.23], seriously limiting the device f_{max}. Considerable effort has been made in this project to reduce the gate resistance of short gate length devices as will be discussed in detail in Chapter 4.

2.6.4 Summary of Requirements to Produce HFET with Optimum High Frequency Performance

In summary, to produce a high quality high frequency device, both material and device issues have to be addressed. The material should have :

i) large effective carrier velocity

ii) large carrier concentration

iii) high mobility

Device issues are :

i) short gate lengths with small gate resistance are required

ii) parasitic source and drain resistances must be minimised by optimising ohmic contact technologies and having a small sheet resistance. The above material requirements will minimise the sheet resistance contribution to the parasitic source and drain resistances.

iii) output conductance must be minimised.

2.7 Reducing the Gate Length of a FET - Scaling Rules

As shown in Section 2.6, to increase f_T and thus the MAG and f_{max}, whilst reducing the noise figure of a HFET, the gate length of the device should be reduced. The electron beam lithography system used in the course of this work has previously been employed to fabricate FET's with gate lengths as small as 30nm[2.27]. However, if short gate length HFET device performance is to be maximised, a number of other device features must also be scaled along with the gate length.

As the gate length is reduced, the 2DEG should be formed closer to the surface, as, for efficient device operation, a ratio of around 3:1[2.28] should be maintained between the gate length and the gate-to-channel spacing ie a gate length of 50nm necessitates a gate to 2DEG spacing of around 15-20nm. Only with this ratio can the device gate capacitance be expected to scale with gate length. Thus, in short gate length HFET devices, thin AlGaAs spacer layers (2-5nm), and thin, heavily doped donor layers (~30nm $4x10^{18}$ Si atoms cm^{-3}) are employed. Advances in MBE growth technology allow the 2DEG/gate separation to be minimised by the use of δ doping[2.29]. Thus, all the electrons required to form the 2DEG can be supplied from a few monolayers of Si doping, rather than 15-20nm of Si doped AlGaAs. 2DEG's with sheet concentrations of $5x10^{11}cm^{-2}$ have been formed 15nm from the surface using such structures[2.30].

As mentioned in Section 2.6.3, the parasitic source and drain resistances of the HFET must be minimised

to maximise the power gain of the device. A significant contribution to R_s and R_d can arise from the sheet resistance of the semiconductor regions between the source and drain contacts and the edges of the gate. The sheet resistance can be reduced by designing the structure to include a parallel conduction layer so that, in the parasitic source and drain regions, the total sheet resistance is that of the 2DEG in parallel with that of the parallel conduction layer.

If the gate was placed directly on the surface of such a structure, the device performance would be degraded as transport through the doped AlGaAs would occur. To prevent this, material is etched away in the gate region prior to gate deposition as shown in Figure 2.7.1.

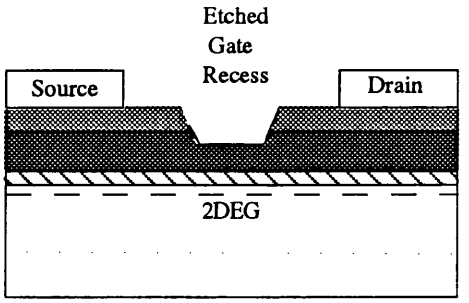

Figure 2.7.1 - Gate Recessed HFET Structure

This has an additional benefit of reducing the effect of surface states on device performance[2.31].

The surface of GaAs has a built-in voltage of around 0.7V (the surface is pinned mid band-gap) because of the effect of dangling bonds, the surface oxide layer etc. This built-in voltage is not dissimilar to the Schottky barrier height of most metals on GaAs (typically 0.7-0.8V). Thus, although a gate may be lithographically defined to be 100nm for example, the effective electrical length of the gate (as viewed by carriers in the channel) will be much greater, as the effect of the gate is smeared out by the presence of the surface states as shown in Figure 2.7.2.

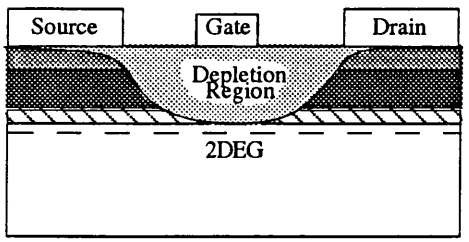

Figure 2.7.2 - Surface States Increase the Effective Gate Length of a HFET

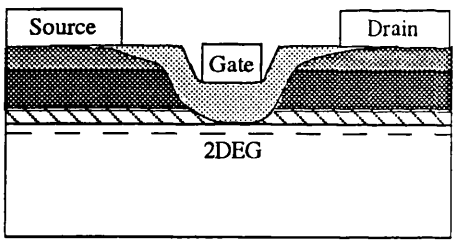

Figure 2.7.3 - Gate Recessing Reduces the Influence of Surface States

By recessing the gate as described above, parallel conduction may be used to reduce the device access resistances. In addition, the effect of the surface states can be reduced as shown in Figure 2.7.3.

2.7.1 Buffer Conduction

In an HFET, the majority of the drain source bias is dropped across the gate. Very large electric fields are experienced by the carriers which gain significant energy as a result. This gain in energy is often sufficient to allow the electrons to free themselves of the confining barrier in the GaAs formed due to the

band bending caused by the local electron accumulation, and so a significant carrier concentration can establish in the undoped GaAs region below the 2DEG. When in this region, the carriers cannot be modulated by the gate as the remaining 2DEG screens the gate potential, and so a degradation in transconductance results[2.32]. A second consequence of buffer conduction is that as the drain source bias is increased, the field under the gate increases, and more carriers are injected into the buffer, further increasing the buffer current. This effect causes a decrease in device output resistance R_{ds}, thus reducing f_{max} and reducing the voltage gain of the device.

Buffer conduction can be reduced by introducing an undoped AlGaAs layer below the 2DEG. This confines the carriers to the channel as a result of the GaAs/AlGaAs conduction band offset[2.33]. Such a structure is shown in Figure 2.7.4, where the single heterojunction confining the 2DEG has now been replaced by a quantum well.

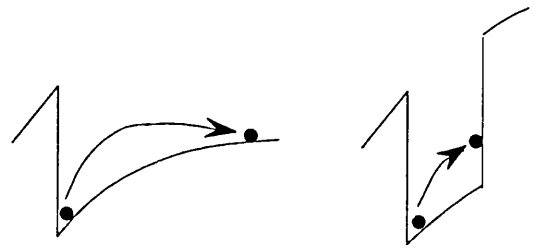

Figure 2.7.4 - Reducing Buffer Conduction using an AlGaAs Confining Barrier Below the 2DEG

The disadvantage of this structure is the poor quality of the interface produced by the growth of the undoped GaAs on top of the undoped AlGaAs buffer. This is due to surface roughness in MBE grown AlGaAs because of the poor surface mobility of the Al species on the growing surface[2.34]. However, with careful optimisation of the MBE growth conditions, it is possible to produce a high quality "reverse" AlGaAs/GaAs interface[2.35], and so improve carrier confinement to the 2DEG in short gate length HFETs.

2.8 Material Systems for HFETs

Throughout the course of this chapter, where a specific material system has been required to more easily explain a phenomenon of HFET operation (eg to show the modulation of the 2DEG carrier concentration by the application of bias to a Schottky contact in Section 2.1.3), the AlGaAs/GaAs material system was used as an example. However, there are currently a number of material systems available for HFET fabrication based on both GaAs and InP[2.36], as discussed in this section.

2.8.1 Velocity-Field Characteristic of III-V Semiconductors

Consider first, two ohmic contacts to a layer of uniformly doped n type GaAs. When a voltage is applied between the contacts, a longitudinal electric field is created which causes the electrons to drift in response to it. The velocity of electrons in the channel in response to the applied electric field is shown in Figure 2.8.1.

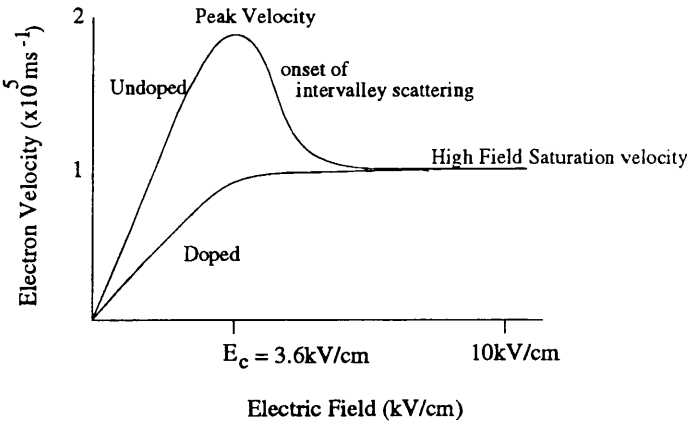

Figure 2.8.1 - Velocity/Field Characteristic of GaAs

The peak velocity of $2x10^5 ms^{-1}$ and the region of negative differential mobility following it apply only in very lightly doped material[2.37]. The negative differential mobility is caused by intervalley transfer in GaAs (the band structure of III-V semiconductors show them to have one central valley (the Γ valley) and a number of satellite valleys at higher energies (the L and X valleys)). At low fields and electron energies, most carriers populate the lowest energy Γ valley, where the electron effective mass is smallest ($0.067m_0$ in GaAs). Increasing the applied electric field, electrons in the Γ valley accelerate until, at the critical field E_c, they have sufficient energy (0.3eV in GaAs) to transfer to the upper L valley, which has a higher electron effective mass ($0.12m_0$ in GaAs), and thus a lower mobility than in the Γ valley ($\mu = q \tau / m^*$, where τ is average time between scattering events and m^* is the effective electron mass). This redistribution of electrons in the Γ and L valleys causes the overall transport properties of the material to be the weighted average of the two valleys' transport properties and is responsible for the region of negative differential mobility[2.38]. At high electric fields, an equilibrium is established for inter-valley transfer and the high field electron velocity saturates at around $1.0x10^5 ms^{-1}$.

At the doping concentrations used in most uniformly doped GaAs channel FETs, ionised impurity scattering at low fields increases the rate of electron momentum randomisation without affecting the total energy of the electrons, as ionised impurity scattering is an elastic scattering mechanism. This results in a reduction in mobility as shown in Figure 2.8.1. The total electron energy is unchanged by ionised impurity scattering so intervalley scattering still occurs at roughly the same electric field strength as in the low doped case. Thus, the final saturation velocity is unaffected by ionised impurity scattering.

The 300K low field mobility of the semiconductor is influenced most by the ionised impurity and optical phonon scattering rates, and also the effective mass of electrons in the Γ valley. The peak velocity of a given material is dominated by the energy separation between the Γ and L valleys. A large Γ-L valley energy separation allows electrons to accelerate for longer in the Γ valley and attain a higher velocity before being scattered to the satellite valleys. The high field saturation velocity is governed by the intervalley scattering rates which determine the equilibrium distribution of electrons in the Γ and L valleys.

Table 2.8.1 shows the effective mass of the Γ valley (with respect to the electron mass m_0) m^*_Γ/m_0, the low field mobility μ_0, the peak velocity v_p, the Γ-L valley energy separation $\Delta E_{\Gamma L}$ and the high field

saturation velocity v_{sat} for a number of III-V semiconductors at 300K.

Material	$m^*\Gamma/m_o$	μ_o (cm^2/Vs)	v_p (ms^{-1})	$\Delta E_{\Gamma L}$ (eV)	v_{sat} (ms^{-1})	Refs
Undoped GaAs	0.067	8500	$2.1x10^5$	0.33	$1.0x10^5$	[2.21]
$1x10^{18}$n type GaAs	0.067	2000	$1.1x10^5$	0.33	$1.0x10^5$	[2.21, 2.37]
AlGaAs/GaAs 2DEG	0.067	7500	$1.8x10^5$	0.27	$1.0x10^5$	[2.37]
undoped InP	0.077	4600	$3.0x10^5$	0.61	$1.0x10^5$	[2.21, 2.39]
undoped $In_{0.15}Ga_{0.85}As$	0.062	6500			$1.0x10^5$	[2.39]
undoped $In_{0.53}Ga_{0.47}As$	0.041	10900	$3.0x10^5$	0.55	$0.7x10^5$	[2.39]
undoped InAs	0.022	33000	$3.5x10^5$	0.87		[2.21, 2.39]

Table 2.8.1 - Properties of a Number of III-V Semiconductor Materials (Reference to Figure 2.1.1 shows $In_{0.53}GaAs$ to be lattice matched to InP)

The correlations between effective mass and low field mobility, and between $\Delta E_{\Gamma L}$ and peak velocity can be clearly seen in each material system. In addition, it is interesting to note that the high field saturation velocity in all materials is around $1.0x10^5 ms^{-1}$.

2.8.2 Velocity Overshoot

The velocity field characteristic of Figure 2.8.1 is a stationary characteristic which is valid for constant applied electric fields (both in space and time). However, if the electric field is increased suddenly, the electrons have to respond to this change. In such cases, as often occur in the gate region of a FET, non-stationary effects can become important. In III-V semiconductors, the static saturation velocity arises from the establishment of an equilibrium distribution of electrons in the Γ and L valleys. However, there is a finite relaxation time associated with the intervalley transfer scattering mechanism. Over time durations commensurate with the onset of intervalley scattering, electrons in the Γ valley can be accelerated to velocities above the maximum velocity of the stationary velocity/field curve, before relaxing to a saturated velocity. Figure 2.8.2 shows a Monte Carlo simulation of this effect[2.40], where an ensemble of electrons in GaAs is subjected to a step in electric field of $70kVcm^{-1}$ for 1 ps.

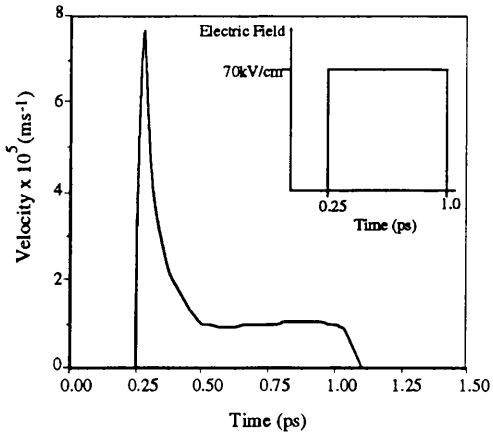

Figure 2.8.2 - Velocity Overshoot of Electrons in GaAs

The ensemble average velocity increases to around six times the steady state saturation value in a fraction of a picosecond. Later, as the scattering processes come into effect, the velocity is reduced to the stationary high field value. This effect, known as velocity overshoot, may influence device performance if the distance carriers have to travel in a device is comparable to the product of the duration of the overshoot and the average velocity during the overshoot period. An overshoot duration of 1ps and an average velocity of $1.0x10^5 ms^{-1}$ for that period (a pessimistic value), result in an enhanced velocity distance of 0.1μm.

Numerous studies on the non-equilibrium transport properties of many III-V semiconductor systems have been made by the Monte Carlo method[2.41-2.43]. All show that in the time interval of 0-1ps, carrier velocity is enhanced over the steady state saturation value. The general trend observed is that as the electric field is increased, electrons accelerate more quickly but the duration of the overshoot is reduced. Further, the effect is more pronounced for material systems with low effective masses and large Γ-L energy separations.

Many Monte Carlo simulations of HFETs have been performed and all show the velocity overshoot effect in the device channel[2.43-2.45]. The effect has been predicted to increase the frequency response of an HFET as the gate length is reduced, particularly if the mobility of the carriers is high (ie low doping as would be found in a 2DEG system, or small effective mass) and a large Γ-L valley energy separation exists.

From Table 2.8.1, 2DEG material systems based on InAs, $In_{0.53}GaAs$ and InP should be the most favourable for utilising the velocity overshoot effect as they have small effective mass and a large energy difference between the Γ and L valleys.

The path to the realisation of HFET's fabricated using such material systems is next described.

2.8.3 Evolution of Material Structures for HFET Fabrication

As it was the first heterostructure material system to be studied, it was natural that the initial HFET devices were fabricated with an AlGaAs/GaAs heterostructure. However, a limitation to this material system was found to be the presence of the DX centre, an electron trap formed in silicon doped AlGaAs, which was observed for aluminium mole fractions of greater than 20%[2.46]. It was found that for 25% Al mole fraction, 50% of silicon donor electrons were trapped and unable to contribute to conduction, whilst at 40% Al mole fraction, 90% of the Si donor electrons were trapped. Thus the largest 2DEG carrier concentration in an AlGaAs/GaAs heterojunction could be formed with 25-30% Al mole fraction. The conduction band offset at the heterojunction is 0.2eV and the maximum 2DEG carrier concentration around $1.0x10^{12} cm^{-2}$[2.47].

Adding small concentrations of indium to the GaAs channel was known to decrease the band gap of the channel, thus increasing the conduction band offset and hence the sheet electron concentration[2.48]. A further advantage resulting from this growth technique was that the electron effective mass was reduced as the indium concentration was increased[2.48]. The addition of 10% indium however causes significant lattice mismatch to the GaAs substrate, resulting in strain in the grown layer[2.49]. By careful control of the growth temperature and InGaAs layer thickness, it is possible to produce a thin, high quality, defect free strained layer of InGaAs grown on GaAs[2.50]. The InGaAs layer takes on the lattice constant of the

GaAs substrate, and thus the term 'pseudomorphic layer system' was coined. Layers of $In_{0.2}GaAs$ 130Å thick and $In_{0.35}GaAs$ 50Å thick have been grown on GaAs with good transport properties[2.51]. The thin InGaAs channel layer is grown on top of a GaAs buffer so that the channel in such a pseudomorphic structure is in fact a quantum well. The presence of the potential barrier below the channel enhances carrier confinement to the 2DEG which reduces device output conductance.

As shown in Section 2.8.2, the large Γ-L valley energy separation and small effective mass of $In_{0.53}GaAs$ and InP layers are highly attractive transport properties which, on first sight should result in superior HFET device performance. In the last 5 years, InP based materials become available to the device designer[2.52]. InGaAs is lattice matched to InP for 53% indium, whilst the larger band gap InAlAs is lattice matched to InP for 52% indium concentration[2.48]. The $In_{0.52}AlAs/In_{0.53}GaAs$ heterojunction has a conduction band offset of 0.5eV, and this fact combined with the high doping efficiency of Si in InAlAs ($N_d > 1x10^{19}cm^{-3}$ is possible[2.53]) has resulted in 2DEG carrier concentrations of up to $4.0x10^{12}cm^{-2}$ [2.53].

Again, it is possible to increase the indium concentration in the channel by growing a pseudomorphic structure resulting in larger conduction band offsets and higher 2DEG carrier concentrations[2.54]. Indeed, recently InAs channel structures have been begun to appear[2.55].

As will be discussed next, there is clear evidence that the InAlAs/InGaAs/InP material systems are currently the most attractive for HFET devices with the highest frequency of operation reported for such structures.

2.9 Review of Current State of the Art HFET Devices

In view of all that has gone before in this Chapter, it should now be clear which material and device issues have to be addressed to improve the figures of merit discussed in Section 2.6 above, namely f_T, MAG, f_{max} and Noise Figure. Device f_T can be improved by reducing the gate length and also by increasing the effective velocity of carriers in the channel. MAG and f_{max} can be improved by firstly having a large f_T, but in addition it is necessary to minimise the device parasitics. In particular, the gate resistance and output conductance have to be minimised as the gate length is reduced. From Section 2.6, if the above criteria to increase f_T and f_{max} are followed, a low noise device should almost automatically result.

The review of HFET device performance which follows was obtained from a survey of the open literature since 1986.

Table 2.9.1 shows the highest reported f_T (split into 4 gate length ranges <100nm, 100-200nm, 200-500nm and >0.5μm) for a number of classes of device - namely AlGaAs/GaAs HFET's, pseudomorphic $AlGaAs/In_xGaAs/GaAs$ (x<0.25 HFETs, lattice matched $InAlAs/In_xGaAs/InP$ (x=0.53) HFETs and pseudomorphic $InAlAs/InGa_xAs/InP$ (x>0.53) HFET's. In order that some comparison can be made between classes, the effective velocity $v_{eff} = 2\pi f_T L_g$ is also tabulated.

Material	Gate Length (μm)	f_T (GHz)	$2\pi f_T L_g$ (ms^{-1})	Ref
$Al_{0.25}GaAs/GaAs$	0.08	130	$0.66x10^5$	[2.56]
$Al_{0.27}GaAs/GaAs$	0.1	113	$0.71x10^5$	[2.57]
Al0.30GaAs/GaAs	0.25	82	$1.28x10^5$	[2.58]
$Al_{0.30}GaAs/GaAs$	0.3	48	$0.91x10^5$	[2.59]
$In_{0.15}GaAs/GaAs$	0.12	130	$0.98x10^5$	[2.56]
$In_{0.25}GaAs/GaAs$	0.2	120	$1.51x10^5$	[2.60]
$In_{0.53}GaAs/In_{0.52}AlAs/InP$	0.1	170	$1.29x10^5$	[2.61]
$In_{0.53}GaAs/In_{0.52}AlAs/InP$	0.15	200	$1.88x10^5$	[2.62]
$In_{0.53}GaAs/In_{0.52}AlAs/InP$	0.2	170	$2.14x10^5$	[2.63]
$In_{0.53}GaAs/In_{0.52}AlAs/InP$	0.7	50	$2.20x10^5$	[2.64]
$In_{0.8}GaAs/In_{0.52}AlAs/InP$	0.05	340	$1.05x10^5$	[2.65]
$In_{0.65}GaAs/In_{0.52}AlAs/InP$	0.08	275	$1.38x10^5$	[2.56]
$In_{0.62}GaAs/In_{0.52}AlAs/InP$	0.15	250	$2.36x10^5$	[2.66]
$In_{0.6}GaAs/In_{0.52}AlAs/InP$	0.5	64	$2.00x10^5$	[2.67]
$InAs/In_{0.52}AlAs/InP$	0.6	58	$2.19x10^5$	[2.68]
$In_{0.77}GaAs/In_{0.52}AlAs/InP$	1.3	39	$2.45x10^5$	[2.69]
$In_{0.65}GaAs/In_{0.52}AlAs/InP$	1.4	34	$2.99x10^5$	[2.70]

Table 2.9.1 - State of the Art HFET f_T Results

To allow further comparison, an envelope of the highest effective velocity for each class of device is plotted as a function of gate length in Figure 2.9.1.

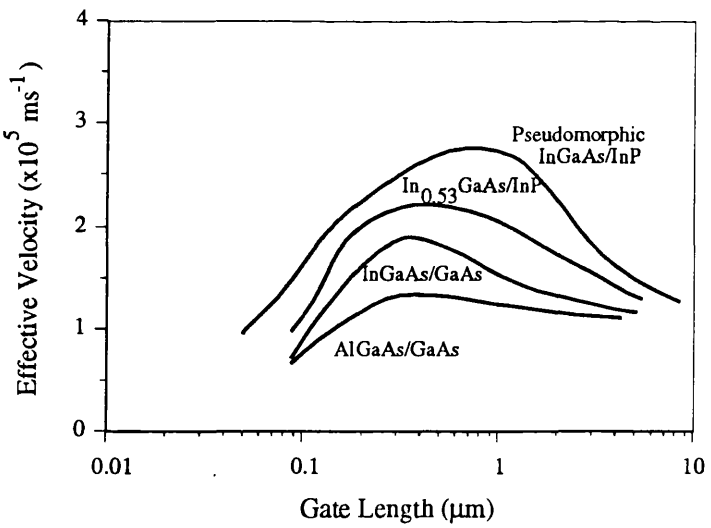

Figure 2.9.1 - Effective Velocity as a Function of Gate Length for HFETs

As discussed by Kohn[2.71], the effective velocity extracted from f_T measurements using the simple

expression $v_{eff} = 2 \pi f_T L_g$ falls into three regions as the device gate length is reduced. At long gate lengths, the electron transport in the device channel is collision dominated, as the channel length is greater than the overshoot distance discussed in Section 2.8.2. As the gate length is reduced, overshoot effects begin to become apparent, and the extracted effective velocity increases. At the shortest gate lengths, the device is dominated by parasitics in particular, the gate capacitance does not scale with gate length as fringing capacitances become a significant contribution to total gate capacitance, and thus the extracted effective velocity falls. Figure 2.9.1 shows this general trend to be true, with the overshoot region extending up to 1.5μm gate length devices for InGaAs/InP material, presumably because of the advantageous transport properties discussed in Section 2.8.2. In addition, in the overshoot regime, the extracted values of electron velocity are seen to increase with a reduction of electron effective mass and increasing Γ-L valley energy separation.

A survey of recent HFET results would thus seem to indicate that velocity overshoot is indeed occurring in sub-micron gate length HFET devices, with the phenomenon more pronounced for InP based material systems, as expected from the foregoing discussion of material transport properties.

In an effort to yield the 'true' electron velocity in the channel of the device and remove the contribution of parasitic capacitances from sub-100nm gate length devices, Nguyen et al[2.65] removed the delays associated with the bond pad capacitance and fringing capacitance from the total delay of the device ($\tau_{tot} = \tau_{pad} + \tau_{intrinsic} + \tau_{fringe} + \tau_{drain}$). A total gate capacitance of 40fF was measured for their 50nm T-gate device of which 25fF was deemed to originate from pad and fringing capacitances (10fF and 15fF respectively). Analysis of the corrected data led to an effective channel velocity of $2.6 \times 10^5 ms^{-1}$, which was found to be constant in the gate length range 0.05-0.15μm, perhaps as a result of reducing the time over which overshoot occurs, as the electric field strength is increased.

Whilst a valid analysis, great care has to be taken to accurately determine the parasitic contributions to the gate capacitance as the total device capacitance is so small for sub-100nm gate length devices.

Considering now the ability of HFETs to provide power gain at high frequencies, Figure 2.9.2 shows the maximum available gain as a function of frequency for a number of different devices reported in the open literature since 1987[2.56,2.72-2.76]. For comparison, device results for HFETs fabricated in the course of this work are included.

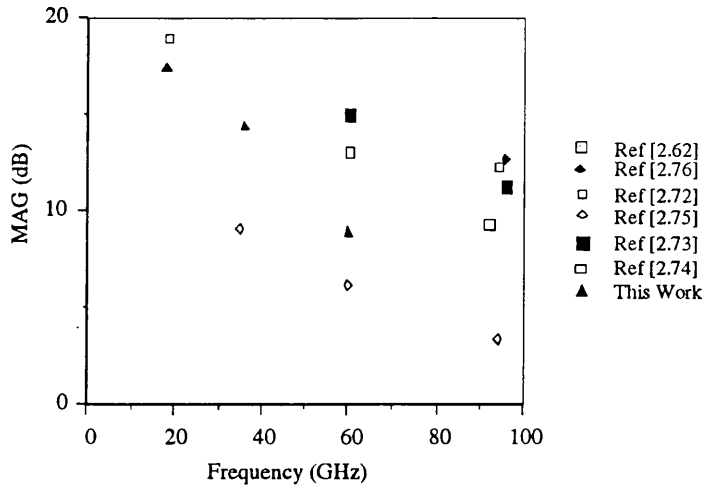

Figure 2.9.2 - Maximum Available Gain as a Function of Frequency for a Number of State of the Art HFETs

State of the art HFET's are currently capable of producing 10dB power gain at 100GHz.

The final figure of merit is the noise figure. It is not straightforward to measure the noise figure of a device at millimetre wave frequencies because of the uncertainties over the noise contributions of test fixtures and transitions in the measurement equipment. However, a number of groups have conducted such studies and Figure 2.9.3 shows noise figure and associated gain of reported devices in the 60-94GHz bandwidth.

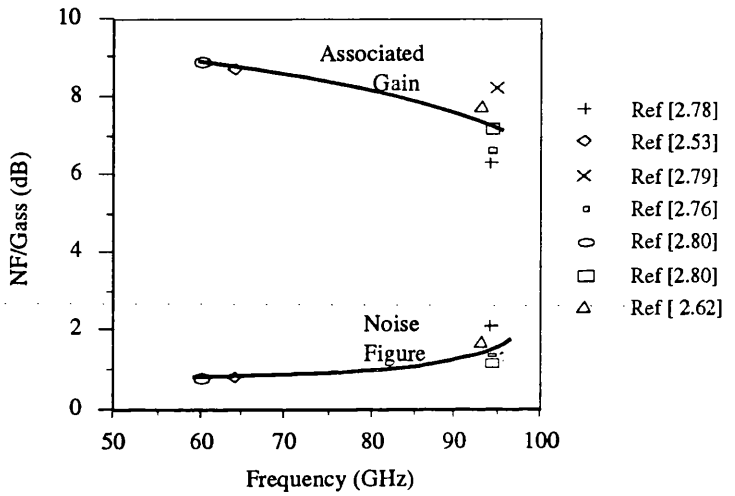

Figure 2.9.3 - Noise Figures of HFETs at Millimetre Wave Frequencies

Figures 2.9.2 and 2.9.3 show devices with low noise performance and power gain up 100GHz are currently available, and such individual devices are now being incorporated into MMICs operating at around 100GHz, such as the amplifier reported by Majidi-Ahy et al[2.77] with 8dB gain over the frequency bandwidth 75-100GHz. Without doubt, further millimetre wave MMIC's will start to appear in the next year.

Chapter Summary

This chapter has considered the theory of HFET operation. The aim has been to produce simple models which, whilst not giving detailed qualitative analysis, show the underlying physics of HFET device operation. The heavy dependence of HFET performance on material choice and device design has been stressed throughout. With this background, the rest of the work of this thesis can be understood. Next, the structures and transport properties of the HFET layer structures used in this work are presented.

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Chapter 3 Material Characterisation

Introduction

In this chapter, the molecular beam epitaxy (MBE) layer structures used in the fabrication of the HFETs of this project are described. In addition, the results of the characterisation techniques employed to evaluate the material transport properties are presented.

3.1 Material Structures used in this Study

To recap from Chapter 2, the material requirements for a low noise, high frequency HFET are:

i) large 2DEG electron concentration to provide large current and hence efficient charging of device capacitances

ii) large carrier mobility to reduce parasitic source and drain resistances

iii) large effective electron velocity to reduce transit delay under the gate

iv) well confined 2DEG to give optimum transconductance and reduce output conductance

In the course of this project, 2DEG based material structures suitable for the fabrication of HFETs were sourced from three MBE Groups :

i) AlGaAs/GaAs from Glasgow University MBE Group

ii) AlGaAs/InGaAs/GaAs from Norwegian Telecom Research, Kjeller

iii) InAlAs/InGaAs/InP from University of Michigan

The general material structure required for a HFET is shown in Figure 3.1.1.

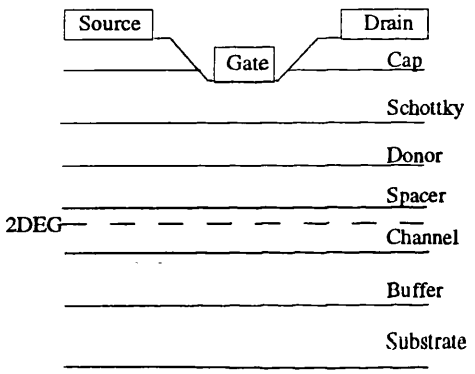

Figure 3.1.1 - General HFET Material Structure

Before discussing the composition of each of the MBE wafers used in the course of this project, it is useful to consider the general requirements of each of the layers of the HFET material structure of Figure 3.1.1, starting with the substrate.

3.1.1 Substrate

The substrate governs which materials may constitute each of the layers of Figure 3.1.1. The substrates used in this study were (100) oriented Semi-Insulating (SI) GaAs and InP. For the MBE wafers used in this project, lattice matching requirements restricted the choice to those shown in Table 3.1.1.

Substrate	Large Band Gap Material	Small Band Gap Material	
	Lattice Matched	Lattice Matched	Pseudomorphic
GaAs	Al_xGaAs x=0.25 or x=0.30	GaAs	$In_{0.15}GaAs$
InP	$In_{0.52}AlAs$	$In_{0.53}GaAs$	$In_{0.65}GaAs$

Table 3.1.1 - Large and Small Band Gap Materials grown on GaAs and InP Substrates used in this Study

The large band gap materials are used for the Schottky, donor, spacer and barrier layers of Figure 3.1.1 while the small band gap materials are utilised for the formation of the cap and channel layers.

3.1.2 Buffer Layer

The output conductance of a FET is affected by the confinement of electrons to the channel[3.1]. The degree of confinement can be modified by introducing a buffer layer of large band gap material resulting in a potential barrier at the channel/buffer interface[3.2].

3.1.3 Channel Layer

The channel consists of an undoped layer of small band gap material in which the 2DEG is formed at the interface with the spacer layer. In pseudomorphic systems, the width of the lattice mismatched channel layer is determined by its ability to accommodate strain without forming dislocations.

3.1.4 Spacer Layer

A thin spacer layer (<50Å) of large band gap material is incorporated to reduce the effect of remote ionised impurity scattering whilst still maintaining a large 2DEG carrier concentration.

3.1.5 Donor Layer

The donor layer supplies the 2DEG (and surface states) with electrons. It consists of either a uniformly doped layer of large band gap material ($\sim 3 \times 10^{18} cm^{-3}$ for short gate length HFETs) or a ∂ doped layer. The layer is generally heavily doped to allow the gate to be placed close to the 2DEG (typically <300Å) - a requirement if short channel effects are to be reduced.

3.1.6 Schottky Layer

To improve the quality of the Schottky gate contact, a layer of large band gap material with low doping concentration ($< 3 \times 10^{17} cm^{-3}$) is often incorporated. When the gate recess is performed, the gate metal is deposited on this layer. The combination of a lightly doped layer and a large band gap material decreases the gate leakage current as the tunnelling probability is reduced.

3.1.7 Cap Layer

Generally, the capping layer is heavily doped ($\sim 3 \times 10^{18} cm^{-3}$ silicon (Si) donors) to aid the formation of low resistance ohmic contacts. In addition, a heavily doped cap screens the effect of surface states from the 2DEG. It has been observed that increasing the cap doping to greater than $3 \times 10^{18} cm^{-3}$ results in an increase in the contact resistance of a gold/germanium/nickel (Au/Ge/Ni) ohmic contact as the in-diffused Ge autocompensates the Si donors[3.3]. The capping material has no aluminium (Al) component as exposed Al oxidises when the wafer is removed from the MBE growth chamber resulting in a surface of poor stability. Further, the formation of a surface aluminium oxide layer is capable of reducing ohmic contact quality.

The material structures used in the course of this project are now considered in detail.

3.2 AlGaAs/GaAs from Glasgow University MBE Facility

As described in Section 2.6.1, the presence of a back confining barrier should reduce the output conductance of a short gate length HFET. To test this theory, an AlGaAs/GaAs 2DEG structure with an AlGaAs buffer layer was investigated.

The transport properties of GaAs grown on AlGaAs are poor as MBE grown AlGaAs has a rough surface[3.4]. The growth of the 'reverse' GaAs/AlGaAs interface has to be optimised if an AlGaAs buffer layer is to be placed close to a 2DEG without affecting its transport properties[3.5]. The optimisation of the buffer layer growth conditions is now described.

3.2.1 Optimisation of the Growth of the AlGaAs Buffer Layer

To determine whether the introduction of an AlGaAs buffer layer degraded the transport properties of the 2DEG, a single heterojunction structure was grown and characterised as a control. Subsequent layers' transport properties were compared to this. The layer structure and conduction band diagram are shown in Table 3.2.1 and Figure 3.2.1 respectively. The conduction band diagram was obtained from a self-consistent Poisson/Schroedinger solution of the layer structure using a 1 dimensional solver developed at the University of Santa Barbera. The Poisson Solver runs on an Apple Macintosh with a Maths coprocessor.

Layer	AlGaAs/GaAs A254
Cap	200Å $6x10^{18}$ GaAs
Schottky	-
Donor	500Å $3x10^{18}$ $Al_{0.25}GaAs$
Spacer	20Å undoped $Al_{0.25}GaAs$
Channel	300Å undoped GaAs
Buffer	5000Å undoped GaAs
Substrate	SI (100) GaAs

Table 3.2.1 - Layer Structure of 'Control' HFET

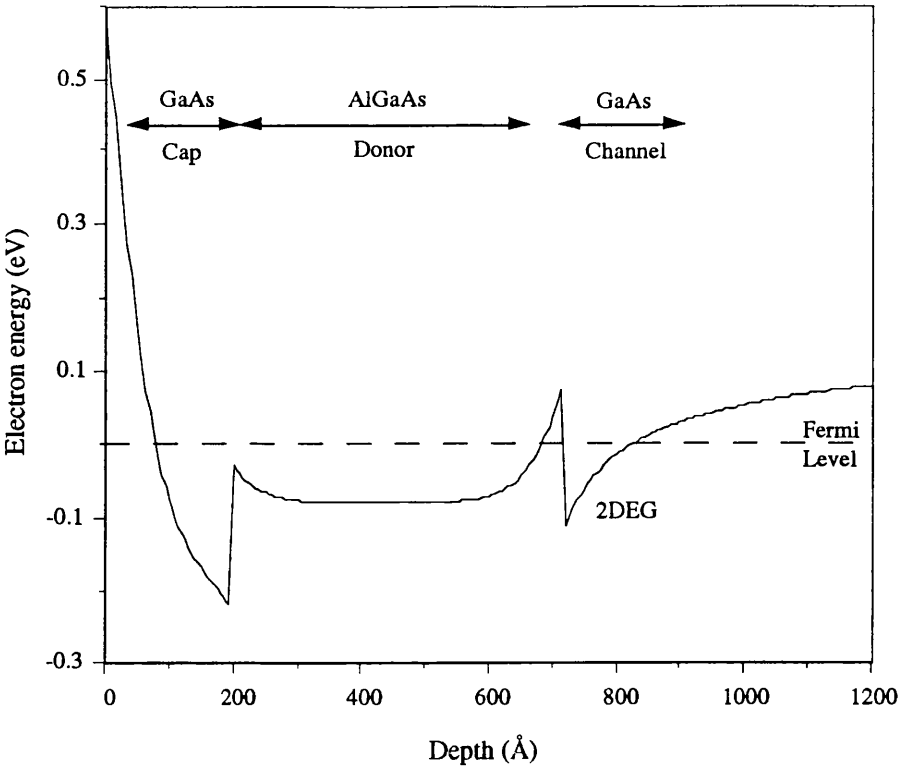

Figure 3.2.1 - Conduction Band Diagram of `Control' HFET Structure

The substrate was SI (100) GaAs. On this a 0.5μm undoped GaAs buffer was grown . Here, the "buffer" and "channel" layers of Figure 3.1.1 are combined - alternatively, the channel can be thought of as being of infinite thickness. Above this a 20Å undoped AlGaAs spacer layer was grown. The $Al_{0.25}GaAs$ layer was doped n-type to $3x10^{18}$ Si atoms cm^{-3} to provide electrons for the 2DEG whilst allowing a reasonable Schottky gate breakdown characteristic to be maintained.

Ideally, a larger Al mole fraction in the AlGaAs layers would be employed to increase the conduction band offset and hence 2DEG carrier concentration but, as described in Section 2.7.3, the DX centre causes a reduction in the number of shallow Si donors able to provide electrons as the Al concentration is increased. 25% aluminium concentration results in a reasonable compromise between 2DEG carrier concentration and the ability of the donor layer to supply electrons. The donor layer is 50nm thick, resulting in a region of parallel conduction designed to reduce parasitic access resistances. In this structure, the "donor" and "Schottky" layers of Figure 3.1.1 are combined. Finally, the GaAs cap layer was doped to $6x10^{18}$ cm^{-3} to minimise the ohmic contact resistance to the structure. When this layer was designed, the dependence of ohmic contact resistance on capping layer doping concentration discussed in Section 3.1.7 was not appreciated.

The substrate growth temperature was 675°C for all layers and the growth rate 1μm/hour for GaAs and 1.43μm/hour for AlGaAs.

3.2.2 Dependence of 2DEG Transport Properties on the Proximity of the Back Confining Barrier

To study the dependence of an AlGaAs back confining barrier on material transport properties, three layers with identical spacer, donor, capping layers and growth conditions to the control layer were grown. The difference between these layers and the control layer was the presence of an $Al_{0.25}GaAs$ back barrier, at distances of 300Å, 450Å and 600Å respectively from the heterojunction resulting in the formation of a quantum well structure shown in Figure 3.2.2.

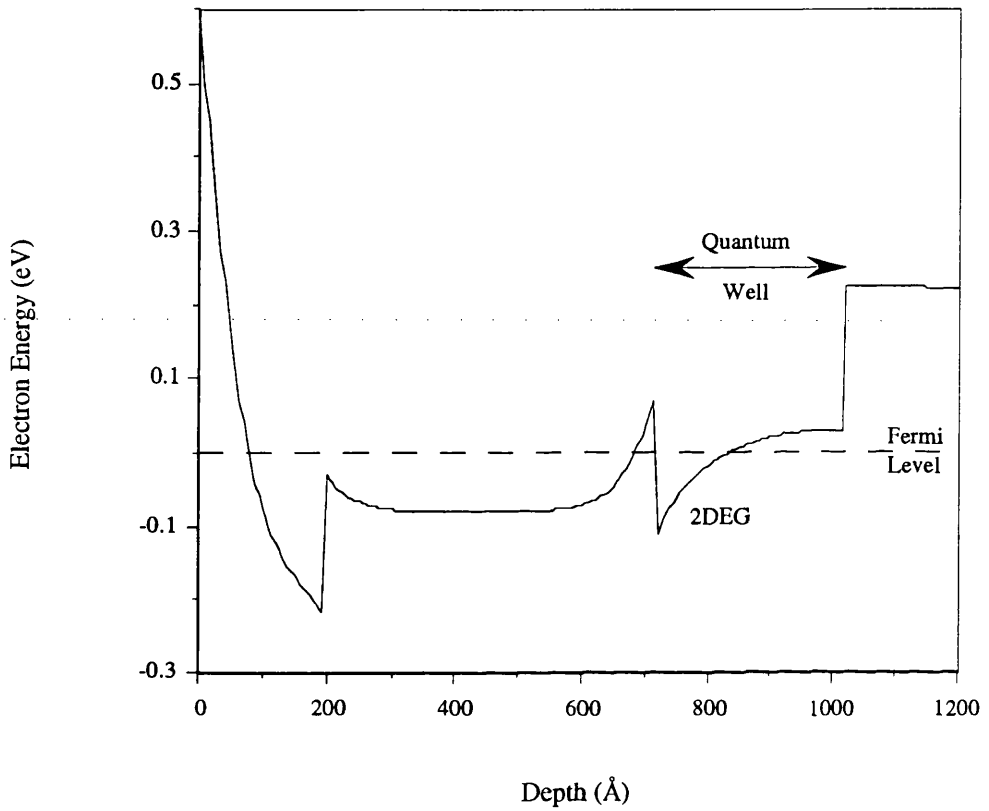

Figure 3.2.2 - Addition of AlGaAs Buffer to form Quantum Well HFET

In all three structures, the buffer layer was grown as an AlAs/GaAs superlattice which reduces surface roughness[3.5]. The basic cell of the superlattice consisted of 8 monolayers of GaAs followed by 4 monolayers of AlAs resulting in a superlattice with an effective band gap equivalent to bulk AlGaAs of 25% Al concentration. The superlattice was formed by growing 100 periods of the basic GaAs/AlAs cell. The superlattice buffer provides a confining potential barrier of 0.2eV below the 2DEG. To further reduce surface roughness, growth was interrupted for 30 seconds between the superlattice and channel layers[3.6]. The substrate temperature was fixed at 675°C for all layers, and the superlattice grown at 1μm/hour.

3.2.3 Evaluation of Layers by Studying Hall Mobility and Carrier Concentration

The 4 layers described above will be referred to by their growth numbers as shown in Table 3.2.2.

Quantum Well Width (Å)	Layer Number
300	A251
450	A252
600	A253
Control (∞)	A254

Table 3.2.2 - Wafer Numbers of Quantum Well Structures

Van der Pauw structures were defined by electron beam lithography (as described in Section 4.9.1) on each of the 4 layers. Hall mobility and sheet carrier concentration were measured as a function of temperature from 300K to 4K in a continuous flow He cryostat with a fixed magnetic field of 0.2T. The samples were cooled to 4K in the dark and mobility and carrier concentration measured as a function of temperature. At 4K, the sample was illuminated with white light, and the mobility and carrier concentration were remeasured whilst heating the sample back to room temperature.

Figures 3.2.3 and 3.2.4 were obtained from the control sample A254. The room temperature carrier concentration and mobility in the dark are $1.5x10^{12}cm^{-2}$ and $6780cm^2/Vs$ respectively. As the structures contain parallel conduction, a simple Hall Effect measurement averages the transport properties of the 2DEG and the parallel conduction layer. This results in an overestimation of the 2DEG carrier concentration and an underestimation of the mobility if the results are ascribed to conduction in the 2DEG alone. As will be shown in Section 3.3, a magnetic field dependant Hall Effect measurement allows the transport properties of the two conducting layers to be individually determined.

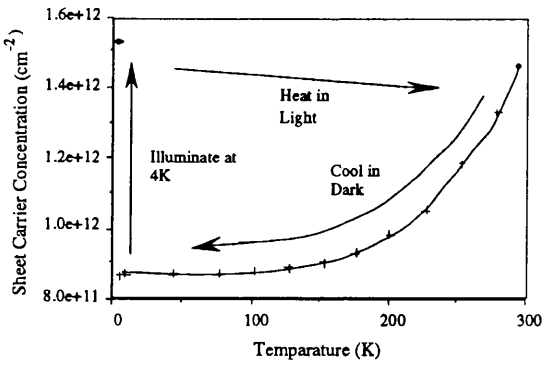

Figure 3.2.3 - A254 Carrier Concentration as a Function of Temperature in Light and Dark

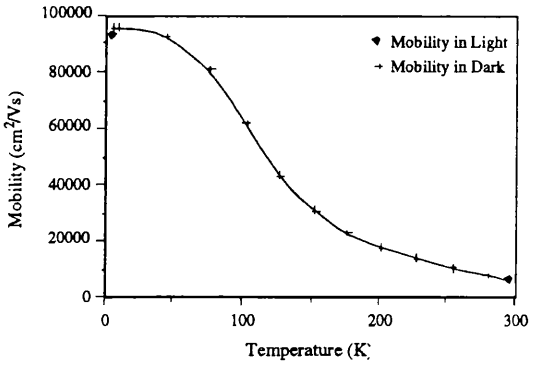

Figure 3.2.4 - A254 Mobility as a Function of Temperature and Illumination

On cooling in the dark, the mobility of the A254 sample rises as optical-phonon scattering effects are reduced. The carrier concentration falls as electrons are trapped in DX centres in the doped AlGaAs layer with insufficient thermal energy to surmount the emission barrier[3.7]. At 4K, on illumination the mobility increases slightly, while the carrier concentration is restored to its room temperature value as electrons are released from DX centres by optical excitation.

Figures 3.2.3 and 3.2.4 are in stark contrast to the data obtained from the quantum well samples, Figures 3.2.5-3.2.10.

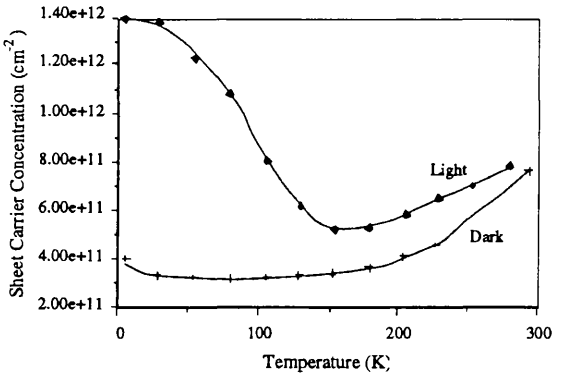

Figure 3.2.5 - A251 Carrier Concentration as a Function of Temperature and Illumination

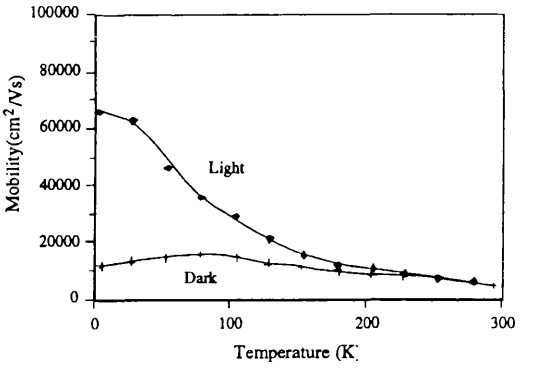

Figure 3.2.6 - A251 Mobility as a Function of Temperature and Illumination

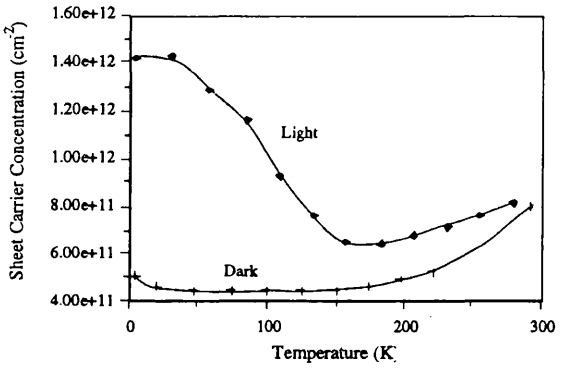

Figure 3.2.7 - A252 Carrier Concentration as a Function of Temperature and Illumination

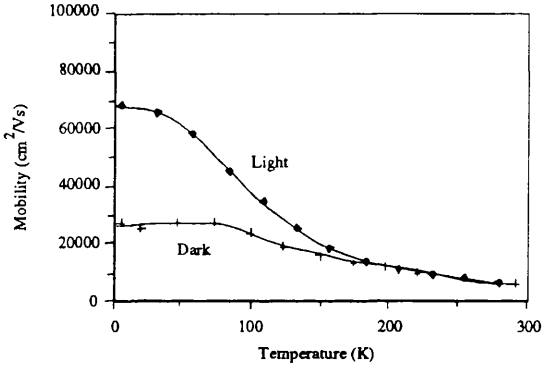

Figure 3.2.8 - A252 Mobility as a Function of Temperature and Illumination

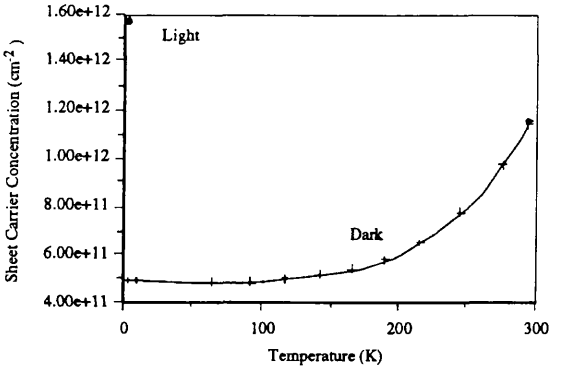

Figure 3.2.9 - A253 Carrier Concentration as a Function of Temperature and Illumination

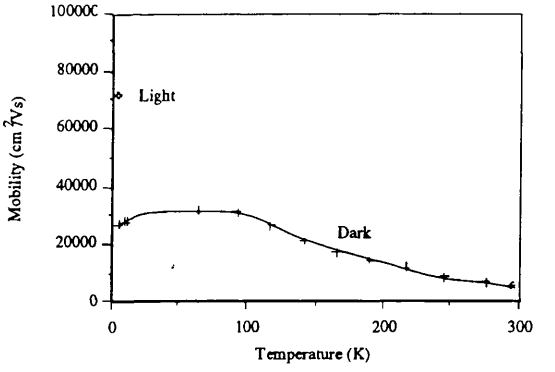

Figure 3.2.10 - A253 Mobility as a Function of Temperature and Illumination

On cooling in the dark, the carrier concentration in these samples is reduced to a level below that of the control sample, indicating charge trapping in addition to DX centre capture in the AlGaAs donor layer. Whilst the mobility increases on cooling in the dark, it does not reach the value of the control sample. Charge trapping and mobility limitation are most severe in A251, the 300Å quantum well structure, where the reverse interface is closest to the 2DEG. This observation leads to the conclusion that the

interface between the GaAs channel and the GaAs/AlAs buffer layer is of low quality and causes significant amounts of trapped charge and a reduction of the carrier mobility in the dark at low temperatures.

In all the quantum well structures, illumination at 4K restores the carrier concentration and mobility to the level of the control sample showing that once trapped charge is freed, it screens the effect of the mobility degrading mechanisms in the reverse interface.

The mobility and carrier concentration as a function of temperature and illumination are summarised in Table 3.2.3 for the 4 layers.

		300K				4K			
		Light		Dark		Light		Dark	
Layer	Well Width	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})
A251	300Å	5920	$7.8x10^{11}$	4900	$7.6x10^{11}$	65200	$1.4x10^{12}$	13300	$4.2x10^{11}$
A252	450Å	6460	$8.2x10^{11}$	5680	$8.0x10^{11}$	68200	$1.4x10^{12}$	31000	$5.4x10^{11}$
A253	600Å	5500	$1.1x10^{12}$	5500	$1.1x10^{12}$	71100	$1.6x10^{12}$	35300	$5.6x10^{11}$
A254	∞	6750	$1.5x10^{12}$	6780	$1.5x10^{12}$	92700	$1.5x10^{12}$	86500	$8.8x10^{11}$

Table 3.2.3 - Hall Mobility and Carrier concentration at 300K and 4K in Light and Dark for the 4 Quantum Well Structures

Clearly, the quality of the reverse interface in the quantum well samples was poor.

The temperature and illumination dependant Hall measurements give a simple and quick (around 3 hours) test for determining whether material is suitable for device fabrication.

The transport properties of the 300Å quantum well sample were most severely affected by the presence of the reverse interface, so further optimisations were performed using a structure similar to that of A251.

The next layer, A332, was grown without.interrupts, a growth temperature of 675°C and a growth rate of 1μm/hour for the superlattice. The temperature and light dependence of the mobility and carrier concentration are shown in Figures 3.2.11 and 3.2.12.

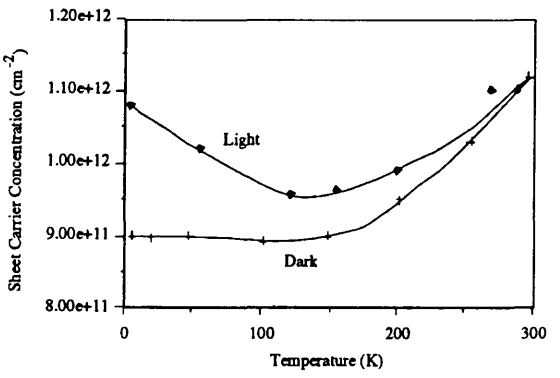

Figure 3.2.11 - A322 Carrier Concentration as a Function of Temperature and Illumination

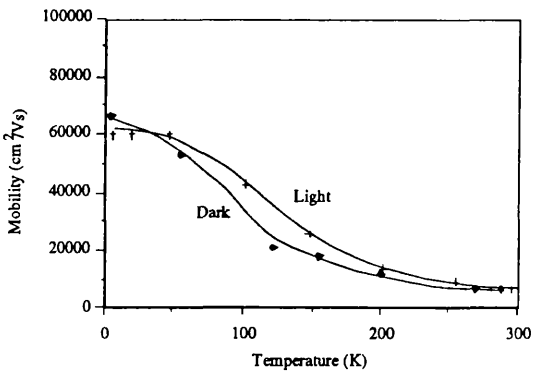

Figure 3.2.12 - A332 Mobility as a Function of Temperature and Illumination

Compared with A251, this structure shows little degradation of the carrier concentration on cooling in the dark. The carrier concentration at 4K in the dark was $9x10^{11}cm^{-2}$, similar to that of A254, the control sample. Whilst the mobility is still lower than in the control structure ($59,500cm^2/Vs$ compared with $92,700cm^2/Vs$) it was felt that this layer was of sufficiently good quality that short gate length HFET fabrication could proceed on it. By removing the interrupt during the growth of the superlattice buffer, a high quality reverse interface AlGaAs/GaAs interface was produced. Though the reason for this is unclear, it is possible that background contamination in the MBE growth chamber (eg carbon) was incorporated into the layer structures during the growth interrupts.

3.3 Magnetic Field Dependant Resistivity Evaluation

All layers used in this work were designed to have parallel conduction to reduce parasitic access resistances in the device. To operate the HFET most effectively, the gate is placed on etched material so that the donor layer material under the gate region of the device is fully depleted. To stop the gate recess etch at the appropriate depth (determined by monitoring the saturated drain source current of a HFET device), it is useful to know the maximum carrier concentration of the 2DEG. In addition, if a correlation of material properties and high frequency device performance is to be performed, it is necessary that the 2DEG mobility and carrier concentration be determined.

A simple Hall Effect measurement averages the transport properties of the 2DEG and the parallel conduction layer, so a technique to determine uniquely the transport properties of both the 2DEG and the parallel conducting layer was required.

This can be achieved using the method shown in Appendix 3.1. With a Hall Bar structure, the magnetic field dependence of the longitudinal and transverse resistivities ρ_{xx} and ρ_{xy}, can be fitted using only the mobility and carrier concentration of the 2DEG and parallel conduction layers as fitting parameters.

35μm wide Hall Bar structures with longitudinal voltage probe spacings of 300μm were fabricated using electron beam lithography as described in Section 4.9.1. The completed structures were wire bonded to ceramic chip carriers and put in a cryostat with a superconducting magnet whose field could be varied from 0-6 Tesla. ρ_{xx} and ρ_{xy} were simultaneously measured at 300K in the dark using a constant longitudinal current of 50μA and a lock-in technique. The measured data was fitted to the model described in Appendix 3.1 using a simple program written with MathCAD. The measured data was fitted by varying the mobility and carrier concentration parameters of the model. There is a very strong convergence, making fitting a relatively easy procedure. A least squares error function was calculated and the procedure terminated when the error was less than 1%.

Measured and fitted data for the Hall sample from layer A254 is shown in Figure 3.3.1. A similar study and analysis was performed on A332, as shown in Figure 3.3.2.

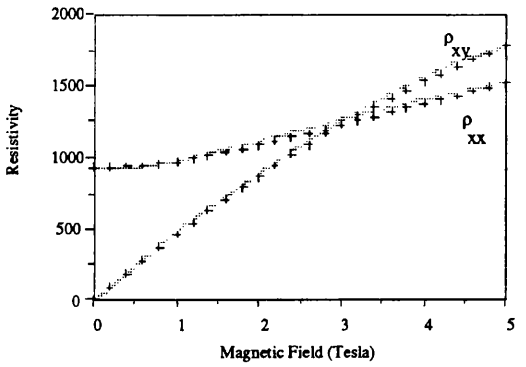

Figure 3.3.1 - Measured and Fitted Magnetoresistance Data of A254

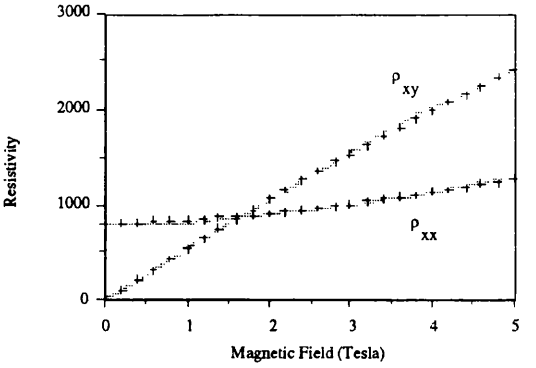

Figure 3.3.2 - Measured and Fitted Magnetoresistance Data of A322

Table 3.4.1 summarises the room temperature mobility and carrier concentration of the 2DEG and parallel conduction layers deduced for A254 and A332.

	2DEG		Parallel Conduction	
Layer	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})
A254	6050	$8.85x10^{11}$	750	$1.85x10^{12}$
A332	7200	$9.9x10^{11}$	700	$9.0x10^{11}$

Table 3.3.1 - 2DEG and Parallel Conduction Transport Properties of A254 and A322

The 2DEG mobility and carrier concentration are similar to values obtained from similar layer structures with 20Å spacer layers.[3.12]. In a previous magnetoresistance study[3.13], AlGaAs doped at $1.0x10^{18}cm^{-3}$ was found to have a mobility of $1000cm^2$/Vs. The higher AlGaAs doping level of A322 and A254 may account for the lower mobility observed in this study.

From the doping levels of A254 and A322, the parallel conduction sheet electron concentration should be around $1.8x10^{13}cm^{-2}$, assuming the surface potential is 0.7V. The low value obtained could be due to a large DX centre population in the doped AlGaAs layer, or that the silicon doping level in either the cap or the donor layers was lower than specified.

The small parallel conduction sheet concentration gives a sheet resistance of around 800Ω/sq, which will increase the parasitic access resistances of the HFETs. In addition, a larger gate/2DEG separation will be required, reducing device scaling at short gate lengths. These effects will be discussed further in Chapter 5.

3.4 AlGaAs/InGaAs/GaAs from Norwegian Telecom Research, Kjeller

The layer structure of the material obtained from Norwegian Telecom Research, TF141 is shown in Table 3.4.1. The conduction band diagram, calculated using the 1D Poisson Solver is shown in Figure 3.4.1.

Layer	AlGaAs/InGaAs/GaAs TF141
Cap	400Å $3x10^{18}$ GaAs
Schottky	400Å $2x10^{17}$ $Al_{0.3}GaAs$
Donor	17Å $3x10^{12}$ δ doped GaAs
Spacer	50Å undoped $Al_{0.3}GaAs$
Channel	160Å undoped $In_{0.15}GaAs$
Buffer	5000Å undoped GaAs
Substrate	SI (100) GaAs

Table 3.4.1 - Layer Structure of TF141 the AlGaAs/InGaAs/GaAs HFET

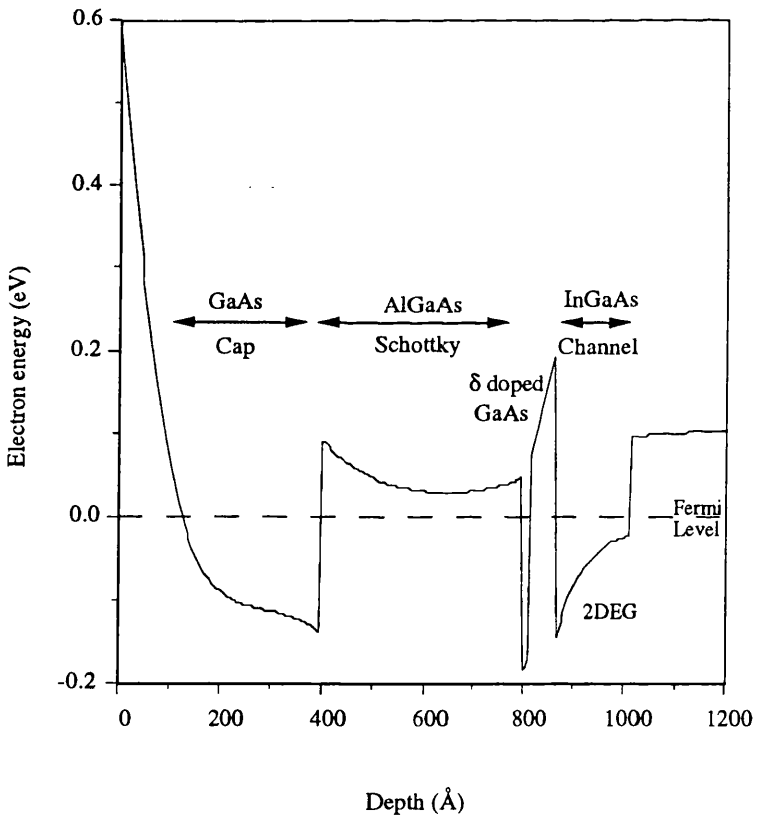

Figure 3.4.1 - Conduction Band Diagram of TF141

The 400Å GaAs capping layer is relatively thick compared with A332. The "Schottky" and "donor" layers are separate in this structure so that the gate is deposited on the $2x10^{17}cm^{-3}$ doped AlGaAs layer. The carriers for the channel are supplied by the ∂ doped region which sits in a layer of GaAs. This avoids carrier loss to the DX centre which results from ∂ doping an AlGaAs region. The strained InGaAs channel has 15% indium concentration and is 160Å thick, less than the critical thickness for such a

strained channel[3.8]. The GaAs buffer provides a confining potential of 0.1eV below the 2DEG. Magnetic field dependant magnetoresistance studies were performed on this layer. The measured and fitted resistivities are shown in Figure 3.4.2.

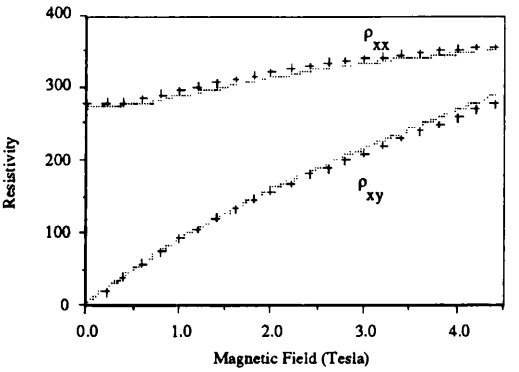

Figure 3.4.2 - Measured and Fitted Magnetoresistance of TF141

The transport properties of the 2 conducting layers are summarised in Table 3.4.2 below.

	2 DEG		Parallel Conduction	
Characterisation Technique	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})
Magnetoresistance	6600	$1.4x10^{12}$	1250	$1.0x10^{13}$
Wet Etch	6100	$1.6x10^{12}$	-	-

Table 3.4.2 - Comparison of Mobility and 2DEG Carrier Concentration Evaluated by Successive Etch and Fitted Magnetoresistance Techniques

The 2DEG carrier concentration is larger than in A322 as the conduction band offset is greater. The lower 2 DEG mobility may result from random alloy scattering and the effects of strain in the $In_{0.15}GaAs$ channel. The parallel conduction sheet concentration for the structure was calculated to be $0.9x10^{12}cm^{-2}$, assuming a surface potential of 0.7eV.

Part of the material characterisation performed by Norwegian Telecom Research consists of a mobility and carrier concentration profile through the layer structure by successively wet chemical etching and measuring the Hall Effect on a Van der Pauw structure. Assuming the peak mobility occurs when the surface depletion edge reaches the 2DEG, and transport is then through the 2DEG alone, this measurement allows a comparison to be made with the magnetoresistance technique. As shown in Table 3.4.2, within experimental error (assumed to be around 10% for the extraction technique and 5% for the etching method), the data agree. This validates the magnetoresistance extraction technique.

3.5 InAlAs/InGaAs/InP from University of Michigan

The InAlAs/InGaAs/InP layer structure, MB1 is shown in Table 3.5.1. The conduction band diagram of the structure is shown in Figure 3.5.1.

Layer	InAlAs/InGaAs/InP MB1
Cap	150Å $5x10^{18}$ $In_{0.53}GaAs$
Schottky	250Å undoped $In_{0.52}AlAs$
Donor	150Å $5x10^{18}$ $In_{0.53}GaAs$
Spacer	50Å undoped $In_{0.52}AlAs$
Channel	100Å undoped $In_{0.65}GaAs$ 400Å undoped $In_{0.53}GaAs$
Buffer	3000Å undoped $In_{0.52}AlAs$
Substrate	SI (100) InP

Table 3.5.1 - Layer Structure of MB1, an InAlAs/InGaAs/InP HFET

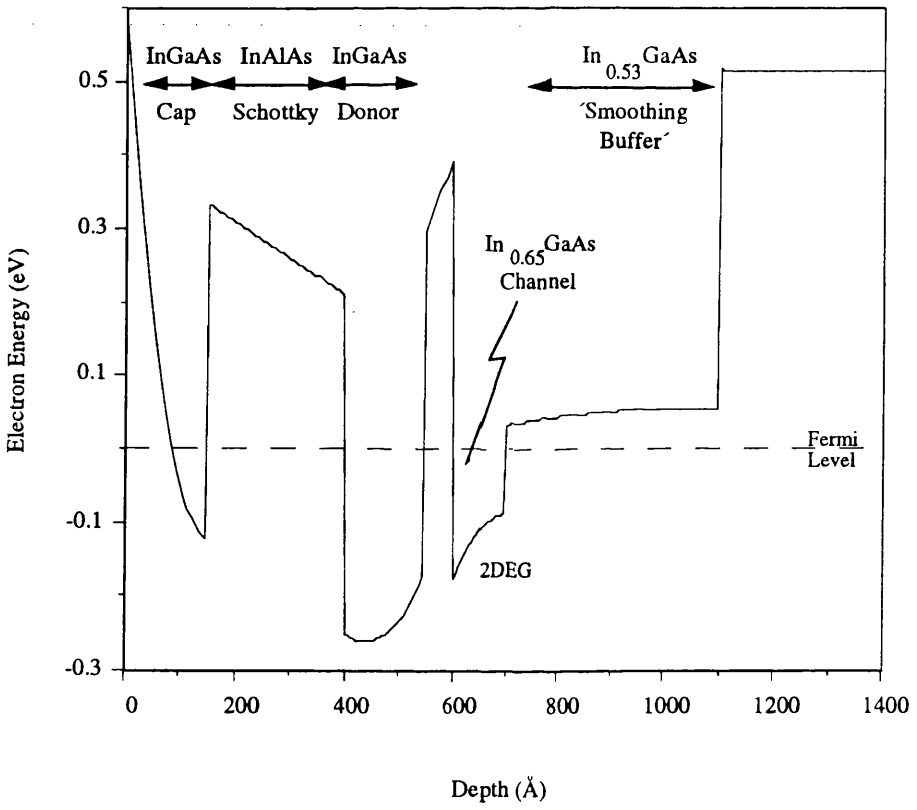

Figure 3.5.1 - Conduction Band Diagram of MB1

The cap layer is very heavily doped ($5x10^{18}cm^{-3}$) $In_{0.53}GaAs$, which has a band gap of 0.71eV. The combination of heavy doping and small band gap result in a very low breakdown voltage of the cap layer - a phenomenon discussed further in Section 4.8.6.3.

The Schottky layer is undoped $In_{0.52}AlAs$ lattice matched to InP. The donor layer is uniformly doped $In_{0.53}GaAs$. The $In_{0.65}GaAs$ strained layer channel is 100Å thick, again less that the critical thickness for lattice relaxation at this indium concentration[3.8]. Difficulties in the growth of high quality $In_{0.52}AlAs$ necessitate the introduction of a "smoothing" layer of lattice matched $In_{0.53}GaAs$ above the $In_{0.52}AlAs$ buffer[3.10] before the $In_{0.65}GaAs$ channel is grown. Thus, the potential barrier below the

2DEG is approximately 0.1eV.

A Hall Bar was fabricated on this material and the magnetoresistance characterisation performed. The measured and modelled field dependant resistivities are shown in Figure 3.5.2.

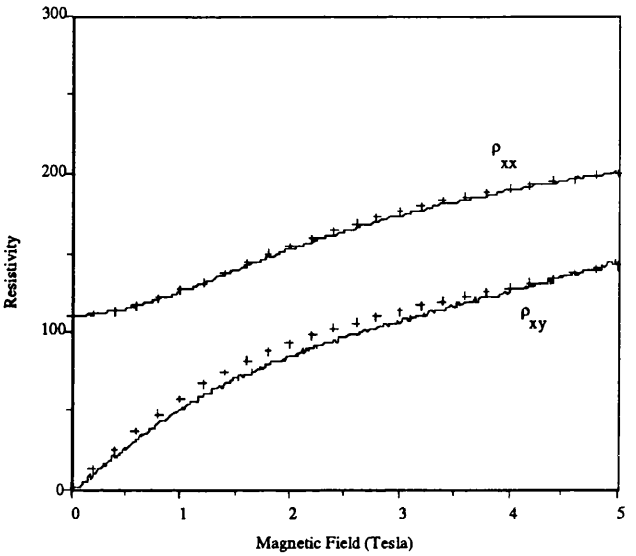

Figure 3.5.2 - Measured and Fitted Magnetoresistance of MB1

The fitting parameters are shown in Table 3.5.2 below.

2DEG		Parallel Conduction	
μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})
9200	$3.8x10^{12}$	800	$2.8x10^{13}$

Table 3.5.2 - 2DEG and Parallel Conduction Transport Properties of MB1

The conduction band offset at the heterojunction is around 0.6eV and results in the large 2DEG carrier concentration. The high 2DEG mobility is caused by the small effective mass of $In_{0.65}GaAs$. Using a built in surface voltage of 0.3eV[3.14], the parallel conduction sheet concentration should be around $7x10^{12}cm^{-2}$. The reason for the large measured concentration is not obvious. Uncertainties in accurately determining the barrier height to heavily doped $In_{0.53}GaAs$ causes further confusion.

3.6 Summary of Transport Properties of Layers used for HFET Fabrication in the Course of this Project

In the course of this project, 3 different 2DEG based layer structures were sourced. The characterisation techniques outlined in this chapter have shown the structures to be suitable for the fabrication of HFET devices. The layer structures used for HFET fabrication are summarised in Table 3.6.1.

Layer	AlGaAs/GaAs **A322**	AlGaAs/InGaAs/GaAs **TF141**	InAlAs/InGaAs/InP **MB1**
Cap	200Å $6x10^{18}$ GaAs	400Å $3x10^{18}$ GaAs	150Å $5x10^{18}$ $In_{0.53}GaAs$
Schottky		400Å $2x10^{17}$ $Al_{0.3}GaAs$	250Å undoped $In_{0.52}AlAs$
Donor	500Å $3x10^{18}$ $Al_{0.25}GaAs$	17Å $3x10^{12}$ δ doped GaAs	150Å $5x10^{18}$ $In_{0.53}GaAs$
Spacer	20Å undoped $Al_{0.25}GaAs$	50Å undoped $Al_{0.3}GaAs$	50Å undoped $In_{0.52}AlAs$
Channel	300Å undoped GaAs	160Å undoped $In_{0.15}GaAs$	100Å undoped $In_{0.65}GaAs$ 400Å undoped $In_{0.53}GaAs$
Buffer	1000Å undoped GaAs/AlAs superlattice effective x=0.25	5000Å undoped GaAs	3000Å undoped $In_{0.52}AlAs$
Substrate	SI (100) GaAs	SI (100) GaAs	SI (100) InP

Table 3.6.1 - Layer Structures used in the course of this Project

The transport properties of the 3 layers are very different, permitting an investigation of the dependence of high frequency HFET performance on material structure. The transport properties of the layers used for subsequent HFET device fabrication are summarised in Table 3.6.2 below.

	2 DEG Transport Properties		Parallel Conduction Layer Transport Properties	
Layer	μ (cm^2/Vs)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	n_{sh} (cm^{-2})
A332	7200	$9.9x10^{11}$	700	$9.0x10^{11}$
TF141	6600	$1.4x10^{12}$	1250	$1.0x10^{13}$
MB1	9200	$3.8x10^{12}$	800	$2.8x10^{13}$

Table 3.6.2 - Transport Properties of 2DEG and Parallel Conduction Layers Used in this Study

Appendix 3.1 - Derivation of Magnetic Field Dependant Resistivities in Transport System of 2 Conducting Paths

This analysis follows the work of Battersby et al.[3.11]

Consider single carrier conduction for two parallel layers in the Hall Bar configuration, as shown in Figure A3.1

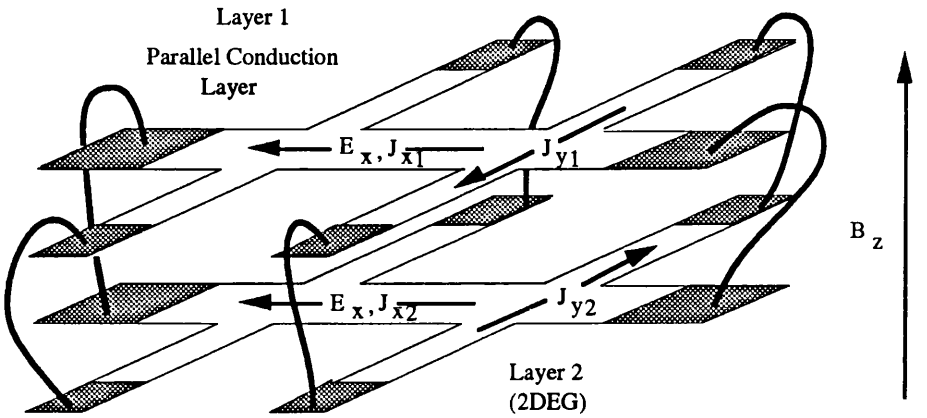

Figure A3.1 - Depiction of Hall Bar fabricated on layer structure with both a 2DEG and a Parallel Conduction Layer. The two conducting layers are joined only at the annealed ohmic contacts of the Hall Bar.

This system can represent an HFET layer structure if layer 1 is ascribed to the parallel conduction region and layer 2 to the 2DEG. The two layers are connected only by the ohmic contacts of the Hall Bar geometry. Applying a longitudinal electric field E_x, results in a circulating longitudinal current J_x. As the carrier concentration and mobility of the two layers are different, on the application of a perpendicular magnetic field B_z, the transverse Hall Field E_y developed in each layer is different. This results in the flow of a transverse current J_y when the magnetic field B_z is applied, even when the system reaches equilibrium.

Two resistivities can be defined:

$$\rho_{xx} = \frac{E_x}{J_x}$$

and

$$\rho_{xy} = \frac{E_y}{J_x}$$

In each layer i, the resistivities defined above can be related to the carrier concentration and mobility as

$$\rho_{xx_i} = (n_{sh_i} q \mu_i)^{-1}$$

$$\rho_{xy_i} = B (n_{sh_i} q)^{-1}$$

Inserting these expressions into the tensor relation between the current density and the electric field in

each layer i, $J = \sigma E$ results in :

$$\begin{bmatrix} J_{x_i} \\ J_{y_i} \end{bmatrix} = \frac{\tau_i n_i q^2}{m_i^*} \begin{bmatrix} \frac{1}{1+\mu_i^2 B^2} & \frac{-\mu_i B}{1+\mu_i^2 B^2} \\ \frac{\mu_i B}{1+\mu_i^2 B^2} & \frac{1}{1+\mu_i^2 B^2} \end{bmatrix} \bullet \begin{bmatrix} E_{x_i} \\ E_{y_i} \end{bmatrix}$$

Where τ_i is the average scattering rate of the i^{th} layer, m_i^* is the effective mass of electrons in the i^{th} layer, q is the elemental charge and μ_i is the mobility of the i^{th} layer.

Using $\omega_{ci}\,\tau_i = \mu_i B$, where ω_{ci} is the cyclotron frequency for the i^{th} layer this equation becomes

$$\begin{bmatrix} J_{x_i} \\ J_{y_i} \end{bmatrix} = \frac{n_i q^2}{m_i^*} \begin{bmatrix} \frac{\tau_i}{1+\omega_{ci}^2 \tau_i^2} & \frac{-\omega_{ci}\tau_i^2}{1+\omega_{ci}^2 \tau_i^2} \\ \frac{\omega_{ci}\tau_i^2}{1+\omega_{ci}^2 \tau_i^2} & \frac{\tau_i}{1+\omega_{ci}^2 \tau_i^2} \end{bmatrix} \bullet \begin{bmatrix} E_{x_i} \\ E_{y_i} \end{bmatrix}$$

If the fields in both layers are identical then this equation can be resolved into x and y components as follows :

$$J_{x1} = \sigma_{xx1} E_x + \sigma_{xy1} E_y$$

$$J_{y1} = -\sigma_{xy1} E_x + \sigma_{xx1} E_y$$

$$J_{x2} = \sigma_{xx2} E_x + \sigma_{xy2} E_y$$

$$J_{y2} = -\sigma_{xy2} E_x + \sigma_{xx2} E_y$$

The currents in the y direction are equal in magnitude but opposite in direction ie

$$J_{y1} = -J_{y2}$$

Thus

$$\frac{E_y}{E_x} = \frac{\sigma_{xy1} + \sigma_{xy2}}{\sigma_{xx1} + \sigma_{xx2}}$$

In addition,

$$J_x = J_{x1} + J_{x2} = E_x \left\{ \sigma_{xx1} + \sigma_{xx2} + \left(\frac{E_y}{E_x} \right) \left(\sigma_{xy1} + \sigma_{xy2} \right) \right\}$$

Combining the above two equations gives

$$\sigma_{xx} = \frac{E_x}{J_x} = \frac{\sigma_{xx1} + \sigma_{xx2}}{\left(\sigma_{xx1} + \sigma_{xx2}\right)^2 + \left(\sigma_{xy1} + \sigma_{xy2}\right)^2}$$

Now using the notation

$$\beta_i = \mu_i B$$

and

$$\rho_{oi} = \frac{m_i^*}{\tau_i n_{s_i} q^2}$$

and

$$\rho_i(B) = \rho_{oi}(1 + \mu_i^2 B^2)$$

leads to

$$\rho_{xx} = \frac{\rho_1(B)\rho_2(B)\left[\rho_1(B) + \rho_2(B)\right]}{\left[\rho_1(B) + \rho_2(B)\right]^2 + \left[\beta_2\rho_1(B) + \beta_1\rho_2(B)\right]^2}$$

ρ_{xy} can be derived from ρ_{xx} using the fact that

$$\rho_{xy} = \left(\frac{E_y}{E_x}\right)\rho_{xx}$$

So that

$$\rho_{xy} = \frac{\rho_1(B)\rho_2(B)\left[\beta_2(B)\rho_1(B) + \beta_1(B)\rho_2(B)\right]}{\left[\rho_1(B) + \rho_2(B)\right]^2 + \left[\beta_2\rho_1(B) + \beta_1\rho_2(B)\right]^2}$$

Thus it can be seen that ρ_{xx} and ρ_{xy} are magnetic field dependant, and the variables are only the mobility and carrier concentration of each of the conducting layers.

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Chapter 4 Device Fabrication

Introduction

This chapter describes the processes and techniques used to fabricate short gate length HFET's. It begins with an overview of the Electron Beam (E-Beam) Lithography System used in this project. The properties of E-Beam resists together with the development process subsequent to E-beam exposure are then discussed. The metallisation technique used to deposit the various contact layers is next described. Having established the basic techniques, the complete process to fabricate a short gate length HFET including process control monitors (PCM's) is detailed.

The fabrication of sub-100nm T-Gates, an important process developed in the course of this project to reduce device gate resistance is given considerable emphasis in the device fabrication discussion.

Finally the fabrication of the remaining structures required for the work of this project:

i) Van der Pauw and Hall Bar samples for material characterisation

ii) calibration standards for the Vector Network Analyser calibration procedure

are described.

4.1 Electron Beam Lithography

Electron Beam Lithography (EBL) offers a number of advantages over other techniques such as optical and X-ray lithography. The most notable is the resolution of the fabricated structure. The resolution limit of optical lithography is set by diffraction of the exposing light around the edges of a mask in contact with the substrate. Even by working with exposing wavelengths far into the ultra-violet, the resolution limit is still around 0.3μm[4.1]. By reducing the exposure wavelength using X-Rays, it is possible to increase the resolution to below 0.1μm[4.2], but the masking technology is rather fragile[4.3]. In comparison, because the electron wavelength is very small (the electron wavelength is 0.25Å for 50kV electrons), the resolution of EBL is limited more by the quality of electron optics and the ultimate resolution of the resists and pattern transfer techniques used. These factors currently limit the resolution of EBL to around 10nm[4.4], but practically, structures in the range 50nm-100nm can be easily and reproducibly fabricated[4.5]. A further advantage of EBL is flexibility of pattern definition due to direct computer control of the writing process. It is a relatively easy task to convert data from a CAD package to drive the scan coils of an E-Beam machine and thus the time from design to pattern definition on a sample is very short. In addition, it is not necessary to generate a new mask every time a modification to the pattern is required. This flexibility is advantageous in a research environment.

These attributes meant that EBL was used throughout this project to fabricate all levels of all structures, even where pattern resolution was not critical. The disadvantage however is that scanning is sequential and so sample exposure can be very time consuming, particularly if (as is usually the case) a large device array is being fabricated.

4.2 The Electron Beam Lithography System

The EBL system used in this work is based on a modified Philips PSEM 500 Scanning Electron Microscope (SEM). The complete system is shown in Figure 4.2.1. Whilst the modifications have been described in detail elsewhere[4.6,5], it is useful to summarise the operation of the system, as it constrains device design.

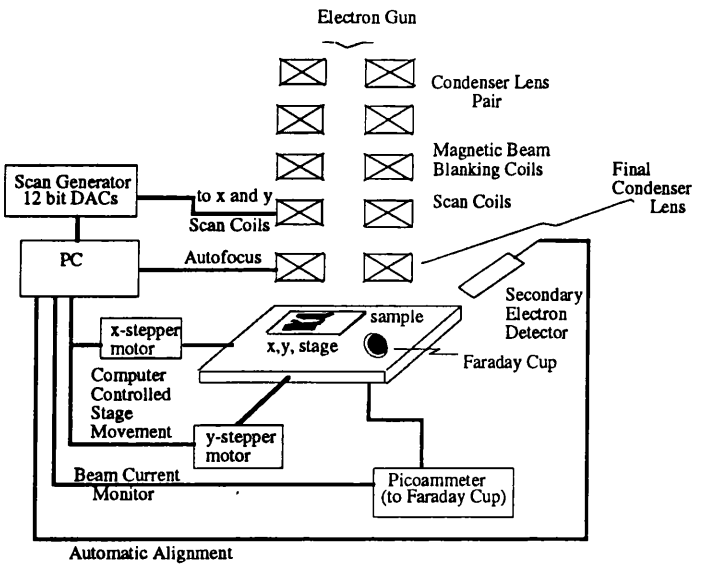

Figure 4.2.1 - Schematic of Complete EBL System used in the Project

The EBL system consists of the PSEM 500 whose scan coils are under computer control via the Scan Generator, a 12 bit Digital to Analogue Converter and raster generator. In addition, the final condenser

lens excitation current can be computer controlled to permit automatic focussing[4.7]. The sample is mounted on an x,y stage, also under computer control. This allows automatic alignment of a pattern to a previously defined level (eg aligning a gate contact in the gap between source and drain contacts)[4.8]. A further requirement for automatic alignment is that the Secondary Electron Detector be connected to the computer to allow alignment mark auto-registration. A Faraday Cup is interfaced to a PicoAmmeter to monitor the current in the electron beam. The magnetic beam blanking coils deflect the electron beam to prevent unwanted sample exposure.

The main features of the PSEM 500 are :

i) The size of the electron spot at the focal plane can be selected between 1μm and 80Å.

ii) The magnification of the microscope can be varied between 20x and 80,000x. Magnification controls the writing field size, eg at 640x magnification, the frame size is 210μmx170μm.

iii) Continuous manual variable magnification (vari-mag) allows fine adjustment of the frame size in both x and y directions.

iv) The accelerating voltage is 50kV.

The exposure procedure will be described in Section 4.6, following a discussion of electron beam resists.

4.3 E-Beam Resist

In EBL, E-beam resists act as pattern transfer media to the substrate. In the course of this work, two E-beam resists were used:

i) Poly-Methyl Methacrylate (PMMA)

ii) A co-polymer of Methyl Methacrylate and Methacrylic Acid P(MMA/MAA)

Both are positive E-beam resists, meaning areas resist subjected to electron beam exposure are selectively removed during the development process leaving windows in the resist film.

The pattern transfer technique is illustrated in Figure 4.3.1.

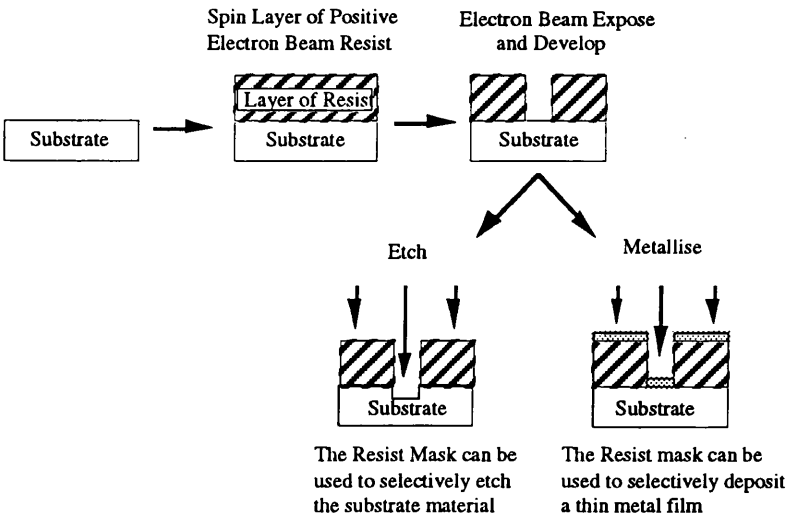

Figure 4.3.1 - Substrate Patterning using PMMA as the Transferring Media

The sample of semiconductor is coated with a layer of PMMA by first dispensing a small quantity of PMMA dissolved in a suitable solvent (generally Chlorobenzene or Xylene) on the sample with a pipette, and then spinning it at high speed (typically around 5000rpm) to coat the sample uniformly. The sample

is then baked in an oven at 180°C to evaporate the casting solvent leaving the PMMA coating. By varying the amount of PMMA dissolved in the solvent, the final resist layer thickness can be controlled. After exposure and development, the window in the resist film can be used for selective etching or metal deposition using the lift-off process.

PMMA consists of long chain polymer molecules of varying length and molecular weight[4.9]. The effect of the electron beam on PMMA is to break bonds in the polymer chains reducing the average molecular weight. The development process is based on selective dissolution of polymer chains below a certain molecular weight. The developer employed in this project was a mixture of 4-methyl pentan-2-one (MIBK) and Propanol (IPA). The relative concentration of the components governs the efficiency of removal of the short chain molecules. Generally a ratio of between 1:1 and 3:1 IPA:MIBK was used, with the actual concentration depending on the resist layer thickness.

PMMA's with different average molecular weights can be selected, and thus E-beam resists of different sensitivity can be produced. As shown in the contrast curves of Figure 4.3.2, PMMA with a large average molecular weight (mw) requires a greater exposure dose than a low mw PMMA to fully develop out the pattern.

The contrast curve represents the percentage of resist remaining after development as a function of electron beam exposure dose. It can be seen quite clearly that the critical exposure dose for complete dissolution of a PMMA resist layer depends on the average molecular weight of the PMMA used.

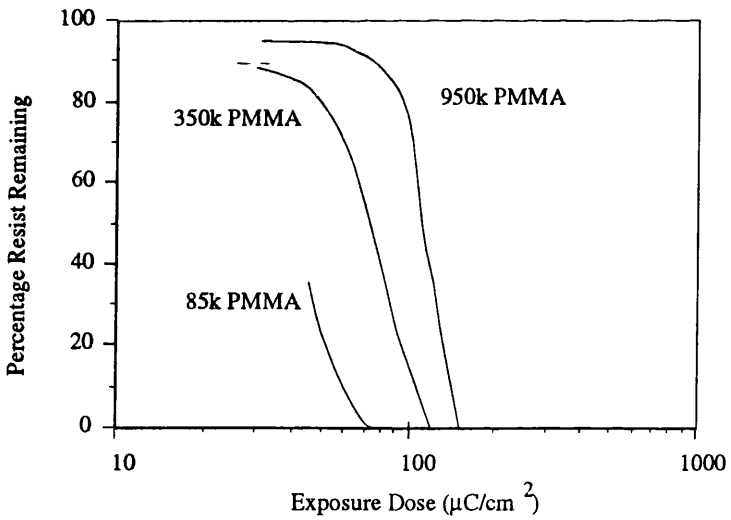

Figure 4.3.2 - Contrast Curves for PMMA's of Different Molecular Weights

4.4 Lift-Off

A further feature of PMMA is the ease with which it can be removed from substrates. PMMA dissolves readily in acetone - a property exploited in the lift-off procedure. Figure 4.4.1 shows a window that has been opened in a PMMA layer as a result of E-beam exposure and development. If a layer of metal is deposited on this structure and the whole sample placed in acetone, the remaining resist dissolves removing the metal sitting on it. Using this lift-off technique, it is possible to selectively pattern substrates with metal.

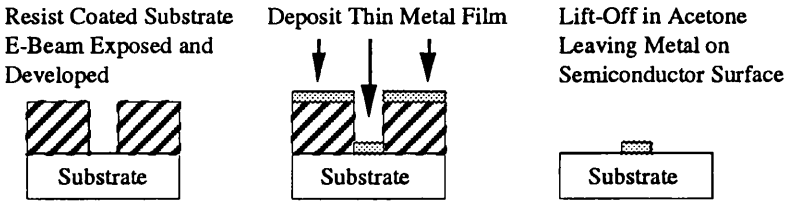

Figure 4.4.1 - Lift-Off using PMMA to Pattern Substrate with Metal

4.5 Bi-Layer Resist System

The reliability of the lift-off technique can be improved considerably by using a bi-layer resist structure[4.10], as shown in Figure 4.5.1. Here, a layer of high molecular weight PMMA (low sensitivity) is spun on top of a PMMA layer of lower molecular. E-beam exposure and development results in an overhang resist profile. On metallisation, the resist profile ensures the deposited film is discontinuous, permitting unwanted areas of metal to be easily removed.

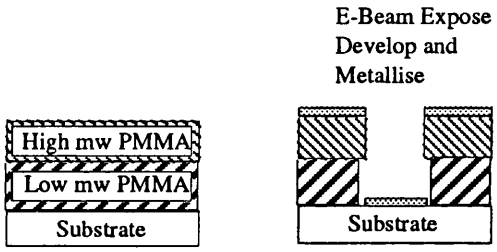

Figure 4.5.1 - Lift-Off using a PMMA Bi-layer Technology

The bi-layer resist system was used throughout this project, with the thicknesses of the component layers selected according to the resolution of the pattern and the amount of metal required to be lifted-off.

4.6 Exposure Procedure

4.6.1 Information Required by the EBL System

The PSEM 500 magnification determines the maximum possible area of sample which can be exposed to the E-beam without moving the stage. The magnifications and corresponding frame sizes used in this project are shown in Table 4.6.1. As the scan generator has 12 bit DAC's, each frame consists of 4096x4096 individually addressable pixels, whose size also depends on the magnification as shown in Table 4.6.1. A high resolution pattern requires a small pixel size, so a large magnification must be used. The frame size of a pattern is thus determined by the resolution.

Magnification	Frame Size(μm^2)	Pixel Size (nm^2)
320x	435x330	106x80
640x	210x170	50x40
1250x	115x90	28x21
2500x	56x42	14x10

Table 4.6.1 - Frame and Pixel Sizes for PSEM 500 Magnifications

Using a CAD package developed 'in-house', patterns consisting of rectangles or trapezia are generated. The output from the CAD package, the 'pattern file', contains the top left and bottom right pixel co-ordinates of the rectangles or trapezia and also an exposure dose which is assigned to each of the pixels. The exposure dose is chosen to fully remove resist from the exposed area on development.
If an array of devices is to be fabricated, it is possible to drive the x,y stage from one position to the next and expose pattern files at each exposure site. The 'position file' contains x,y coordinates for the stage movement with respect to a position defined when the lithography system is initialised and also identifies the 'pattern file' to be scanned at each site. When the system is running, the beam blanking coils are energised between sites as the stage is moved, but not between individual rectangles in the position file. This overcomes beam settling errors at the start of each rectangle.

4.6.2 Exposure

The electron beam spot size is chosen with regard to the required resolution. Generally, the spot size is slightly smaller than the pixel size. Initially, the substrate holder is moved until the Faraday Cup is imaged. The electron beam is focussed into the Faraday Cup and the beam current measured with the PicoAmmeter. The beam current information is fed to the computer which is also told the magnification at which the pattern is to be written. The computer can then calculate the required dwell time of the electron beam at each pixel to be addressed so that the pixel receives the electron dose requested in the 'pattern file'. When writing commences, the dwell time information and rectangle corner coordinates are fed to the scan generator. The stage is then moved to a reference point (usually the bottom left corner of the chip). The beam blanker is energised, and the scanning initiated.

4.7 Metal Deposition

As discussed in Section 4.4, metal deposition and lift-off are important techniques for the fabrication of HFET's. The metal deposition system used throughout this project was a Plassys MEB 450 Evaporator. The amount and rate of metal deposition were controlled using a quartz crystal thickness monitor mounted alongside the sample. Using this metallisation system, it was possible to deposit gold, germanium, nickel, titanium and nichrome in a high vacuum environment (typically $9x10^{-7}$-$1x10^{-6}$ mbar). A load lock permitted these pressures to be achieved 10 minutes after the sample was placed in the evaporator. The combination of the advanced control system and high vacuum of the Plassys evaporator resulted in high reliability of the metal deposition process particularly where metal thicknesses and base pressures were critical.

4.8 Fabrication Of HFET's

The complete HFET fabrication process is now described. The device consists of 6 levels of lithography - alignment marks, isolation, ohmic, wiring, bondpad and gate definition. The devices were designed to be compatible with the on-wafer Cascade Microwave Probes used in high frequency characterisation. This required a coplanar waveguide type structure tapered from probing pads with a signal-ground pitch of 100μm. A SEM micrograph of a completed device is shown in Figure 4.8.1. To reduce the gate

resistance and the effect of stray capacitance at the end of the gate lines, a two finger gate topology was chosen.

Figure 4.8.2 shows a micrograph of a finished device chip. The source pads of adjacent devices overlap, resulting in a continuous groundplane. It was envisaged that a large groundplane would provide a good reference for the microwave measurements. Also evident in Figure 4.8.2 are the isolation process control monitor (PCM) structures in the bottom right corner.

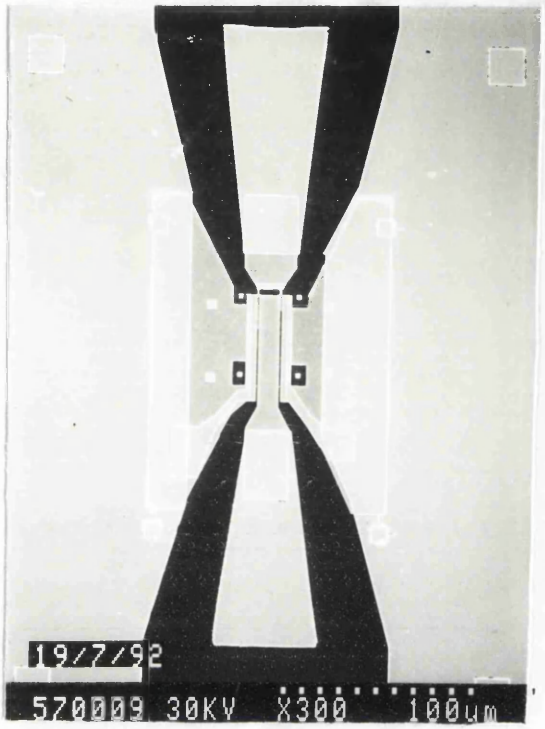

Figure 4.8.1 - SEM Micrograph of HFET Device

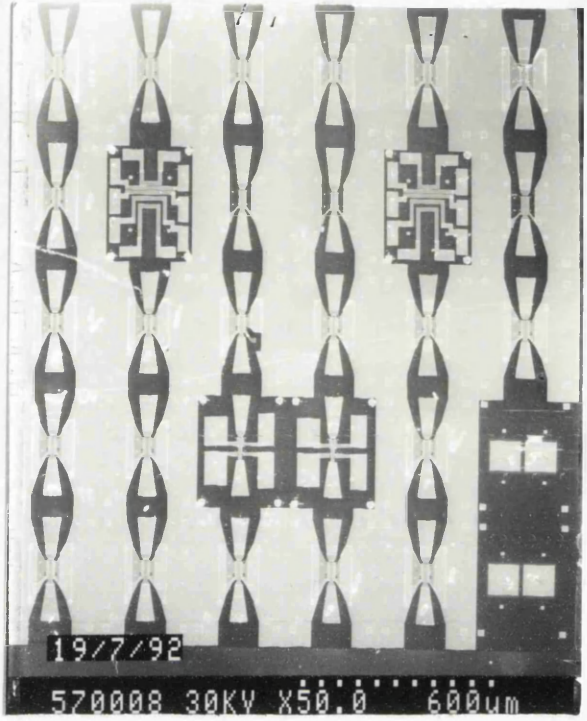

Figure 4.8.2 - SEM Micrograph of Completed Device Chip showing HFETs and PCMs

4.8.1 Level 1 - Alignment Marks

Global registration marks were first defined to allow alignment of the isolation, ohmic and bondpad levels. The pattern is shown in Figure 4.8.3.

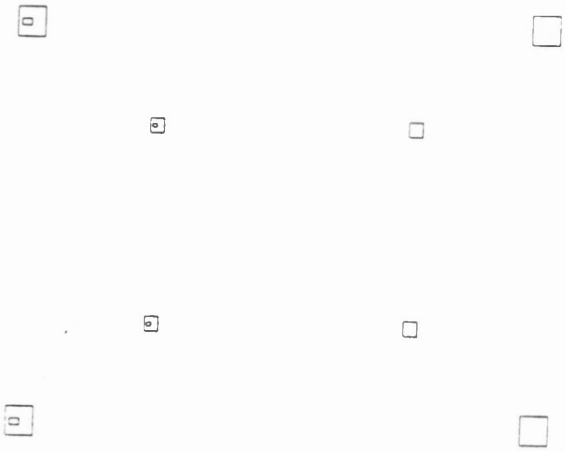

Figure 4.8.3 - Alignment Mark Pattern

The pattern was stepped out on a 6x5 array resulting in 30 device sites on each chip. The pattern consists of alignment marks for a 320x magnification frame (the magnification at which the isolation and bondpad levels are written), and marks for a 640x frame, (the ohmic level). The alignment mark metallisation was a gold/germanium/nickel (AuGeNi) based ohmic contact recipe. This was used because four isolation process control monitors (PCM's) were also defined at this level. Each of these PCM structures consists of two 75μm^2 pads separated by 10μm. Once annealed, the ohmic contact provides a low resistance contact to the semiconductor structure. By monitoring the current passing between the PCM pads as a function of isolation etch time, it is possible to determine when the active layer has been etched through, and etching should be terminated. This is discussed further in Section 4.8.2.
The resist used and PSEM 500 magnification and spot size are as follows:

Resist - Bilayer	5800Å 85k mw PMMA (10% BDH)[§] spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	320x
Varimag	1.0, 1.0
Spot Size	640Å
Developer	2.5:1 IPA:MIBK at 23°C for 30s

Prior to metal deposition, the sample was barrel ashed for 1 minute in oxygen to remove any residual organic contamination. The sample surface was then de-oxidised in 2.5:1 H_2O:HCl for 30s, blown dry in nitrogen and immediately loaded into the Plassys evaporator. A pressure of $2x10^{-6}$ mbar was reached in around 10 minutes. The ohmic metallisation deposited was:

70nm	Au
25nm	Ge
10nm	Ni
180nm	Au

a recipe optimised for the AlGaAs/GaAs structures as will be described in Section 4.3.
The metal was lifted-off in warm acetone (heated to around 45°C in a water bath) and annealed on a carbon strip annealer in Ar:H_2 95:5 forming gas at 300°C for 30 seconds. As high quality ohmic contacts were not a requirement for this process, the annealing temperature was not optimised.

[§]At each level, the resist components and their thicknesses will be given. As this thesis may be used for reference purposes in the Nanoelectronics Group in future, the resist will also be defined in terms more familiar to the workers there ie resist type is BDH - 85,000 molecular weight (mw) PMMA obtained from BDH or ELV - 350,000 (mw) PMMA from Du Pont. The thickness will also be inferred from the percentage weight of PMMA in the casting solvent which is O-Xylene for concentrations below 10% and Chlorobenzene otherwise.

The requirements for the process were that:

i) the contact morphology be smooth, thus allowing the automatic alignment routine to function without difficulty at subsequent levels.

ii) the PCM allowed some current to flow between the pads, so that device isolation could be checked.

4.8.1.1 Alignment

All subsequent levels of lithography require alignment. The automatic alignment system was used throughout, but it was still necessary to initialise this system by performing one manual alignment to instruct the system where the alignment marks on the sample should be positioned with respect to the field of view of the SEM. Alignment was performed by scanning a raster pattern over the metal alignment marks on the sample. The alignment marks contained significant amounts of gold, and thus had a high contrast compared with the substrate.

Three types of alignment pattern were used, each providing successively greater alignment accuracy.

The first two alignment schemes, the coarse and fine alignment patterns, were used for all levels. The final, very-fine alignment pattern was used for gate definition where high accuracy was required as described in Section 4.8.6.

The coarse alignment pattern is shown in Figure 4.8.4. It consists of two gratings with a low exposure dose, thus minimising unwanted exposure of the resist.

Figure 4.8.4 - Course Alignment Pattern

Figure 4.8.5 - Fine Alignment Pattern

The coarse alignment pattern was scanned and the stage moved until the top left and bottom right alignment marks were positioned in the centre of the gratings.

The fine alignment pattern, shown in Figure 4.8.5, was then scanned.

This consisted of a border around each of the four alignment marks. The border overlapped the edge of the marks by 10%. The sample was moved until the marks were central within the border by changing the x,y position and rotation of the sample, and adjusting the vari-mag of the SEM.

Having manually aligned the sample, the automatic alignment system was initialised and subsequent sites were aligned under computer control.

4.8.2 Level 2 - Isolation

The aim of device isolation is to confine current to an area of semiconductor by selective removal of the surrounding conducting layers. Current flow in the isolated area can subsequently be modulated by the application of voltage to various contacts placed on the isolated region. Further, the application of voltages to contacts on nearby devices should have no effect on the device characteristics - obviously this is of considerable importance to circuit performance.

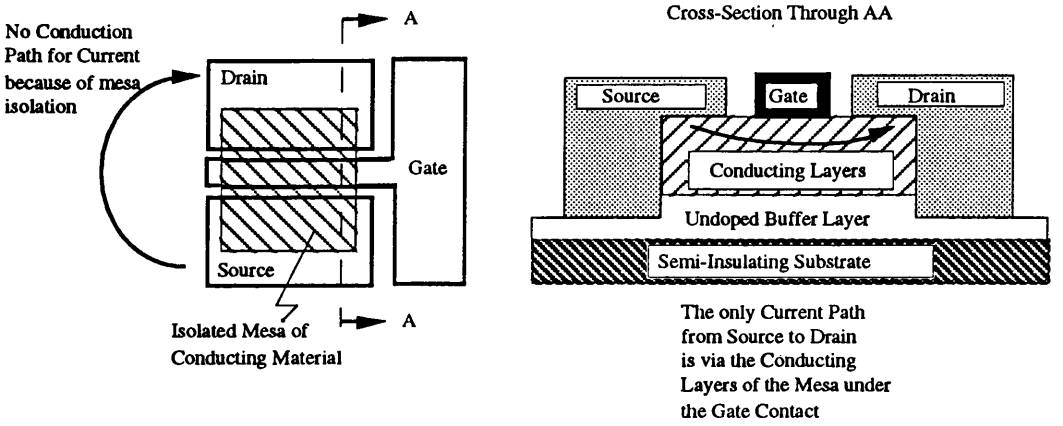

Figure 4.8.6 - Mesa Isolation Technique for HFET

4.8.2.1 Isolation Methods

It is possible to isolate a semiconductor device in a number of different ways:

i) Isolation can be performed using the mesa isolation technique depicted in Figure 4.8.6. Here current is confined by removing material everywhere except in selected areas.

Using this method, the gate stripe has to surmount one edge of the mesa allowing the gate signal to reach the active material. The height of the etched mesa can be minimised by monitoring the current flowing between the ohmic contact pads on the isolation PCM structure when the device isolation is performed. The pads for the device are deposited on non-conducting material, thus minimising parasitic pad capacitance.

ii) An alternative technique, trench isolation, is shown in Figure 4.8.7 for a Hall Bar structure. In this method, a trench surrounding the device is used to confine the current by etching through the conducting layer. If this method is used to isolate a HFET, the gate stripe has to cross the edge of the trench twice (down into the trench from the gate pad, and back up out of the trench onto the isolated area)- a requirement which reduces gate yield (step coverage yield) as the gate stripe can often be discontinuous where it crosses an edge. Further, the bond pads are sitting on active material, which may lead to larger parasitic capacitances between the pads.

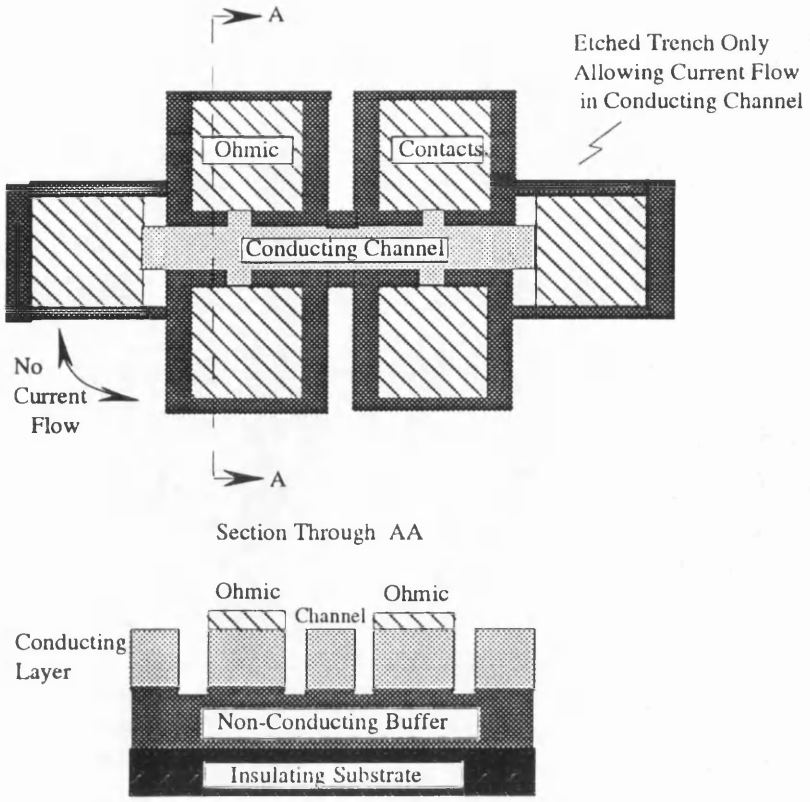

Figure 4.8.7 - Example of Trench Isolation

For these reasons, mesa isolation was used for HFETs.

4.8.2.2 Mesa Isolation Mask

The options for fabricating a suitable isolation mask were next addressed. Ideally, a negative resist (resist remains only in the exposed area after development) mask would have been used to minimise writing time. However, after exposure and development, negative E-beam masks are very difficult to remove using solvents, as the exposure process cross-links the polymer chains. It is possible to remove a negative resist by oxygen ashing or oxygen reactive ion etching, but this introduces damage into 2DEG structures[4.12].

Previous FET work in the Nanoelectronics Group had used a Metal on Polymer (MOP) isolation mask[4.13], but complete removal of this mask also required the use of an oxygen ashing step. For this reason, PMMA was used as the mask for mesa isolation. It was necessary to expose all of the chip with the exception of the mesa region - a fairly time consuming business. The pattern is shown in Figure 4.8.8. The mesa of the HFET device was 40μm wide, as the gate level was subsequently written at 2500x magnification (50x40μm frame size).

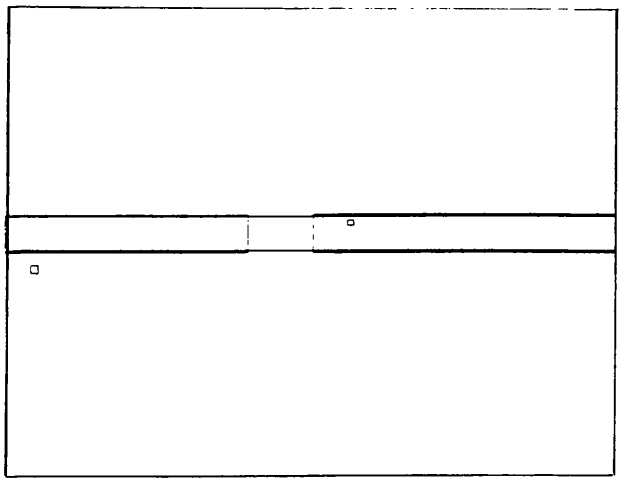

Figure 4.8.8 - Mesa Isolation Pattern

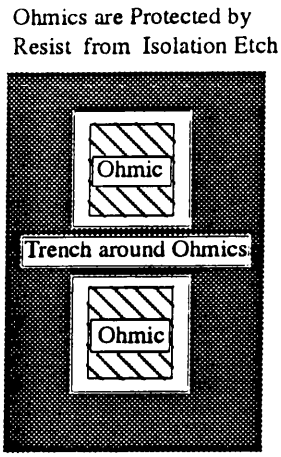

Figure 4.8.9 - Isolation Pattern for Isolation PCM

Figure 4.8.9 shows the isolation pattern for the isolation PCM. It was found that the etch rate of the wet chemical mesa isolation etch was enhanced in regions of exposed ohmic contact metal. Therefore it was necessary to protect the pads, particularly their edges, from the etch if a true indication of the degree of isolation across the chip was to be gained from the PCM's.

As well as isolation structures for HFETs, an isolation structure for the Transmission Line Model (TLM)[4.14] PCM used to evaluate the ohmic contact resistance (described in Section 4.8.3) was written. This consisted of a 10μmx200μm bar.

The resist and SEM exposure conditions are shown below:

Resist - Bilayer	5800Å 85k mw PMMA (10% BDH) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake overnight 180°C
Magnification	320x
Spot Size	250nm
Developer	2.5:1 IPA:MIBK at 23°C for 30s

The resist was baked overnight to give good adhesion to the substrate, so that the etch would not undercut the resist. A bilayer was used to reduce the likelihood of etch penetration through pin-holes in the mask.

4.8.2.3 Isolation Etch

Devices had previously been isolated using a Methane/Hydrogen Reactive Ion Etching (RIE) technique[4.15]. At the time device isolation was being performed in the current study, the ElectroTech 340 RIE machine used for CH_4/H_2 etching was unreliable. Thus it was impossible to reproducibly fabricate mesas of the minimum height required to isolate devices whilst still achieving gate step coverage. In addition, it was impossible to completely isolate samples of the InGaAs/InAlAs/InP structure (MB1) as the etching resulted in the formation of a surface conducting layer. Figure 4.8.10

shows a plot of current measured between two 75μm wide pads separated by 10μm as a function of etch depth (measured using a talystep). The structures were etched using

i) CH_4/H_2 with a gas flow rate of 5:25cc/min (methane:hydrogen) and a power of 80W giving a DC bias of around 700V

ii) $H_3PO_4:H_2O_2:H_2O$ 1:1:100 (a well known wet etch for InP based layer structures)[4.16].

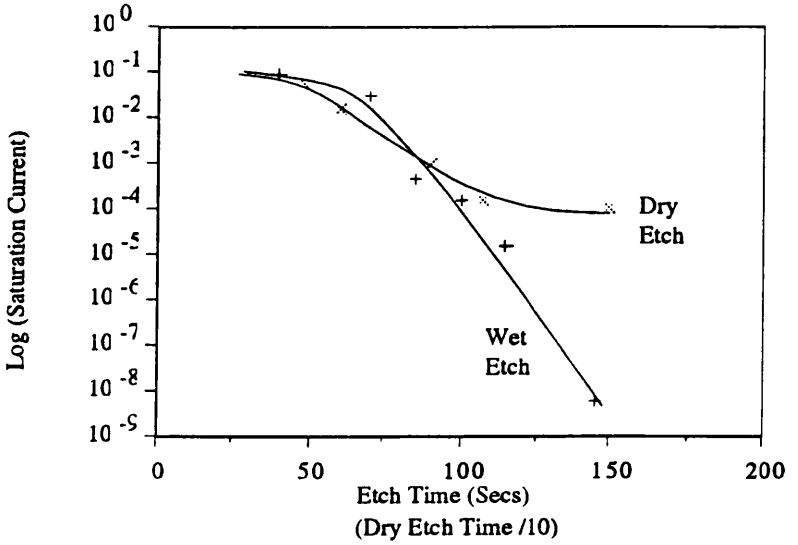

Figure 4.8.10 - Saturation Current as a Function of Etch Time for Wet and Dry Isolation Etching Techniques

Whereas the wet etch isolation current falls to around 10nA, the dry etched isolation current saturates at around 100μA. The mechanism for this effect is not understood, but precluded the formation of mesas using CH_4/H_2 RIE. For this reason, wet chemical etching was used for device isolation.

The etch chosen for isolation of both GaAs and InP based structures was $H_3PO_4:H_2O_2:H_2O$ 1:1:100. This was found to etch at around 300Å/min for all structures, and to produce smooth etched surfaces.

4.8.3 Level 3 - Ohmic Contacts

The ohmic contact level shown in Figure 4.8.11 was written at 640x magnification to allow the 1.1μm source/drain gap to be defined.

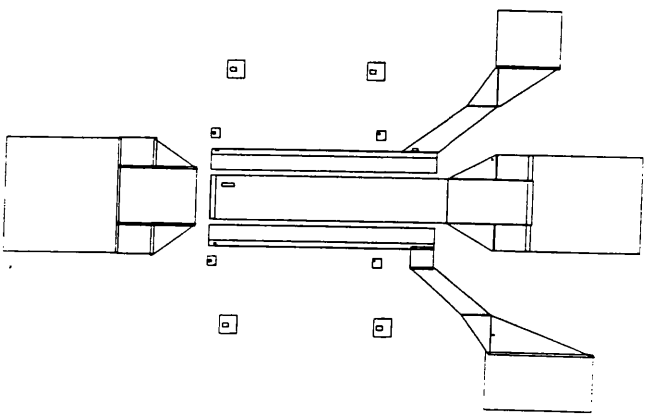

Figure 4.8.11. - Ohmic Pattern

In addition, alignment marks for the gate level were written as part of the ohmic level. The resist and SEM writing conditions are shown below:

Resist - Bilayer	5800Å 85k mw PMMA (10% BDH) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	640x
Spot Size	640Å
Developer	2.5:1 IPA:MIBK at 23°C for 30s

In addition to the device ohmic contacts, the TLM PCM's (Figure 4.8.12), which consisted of 10μm bars of ohmic metallisation crossing the TLM mesa with spacings of 1, 2, 5 and 10μm, were written.

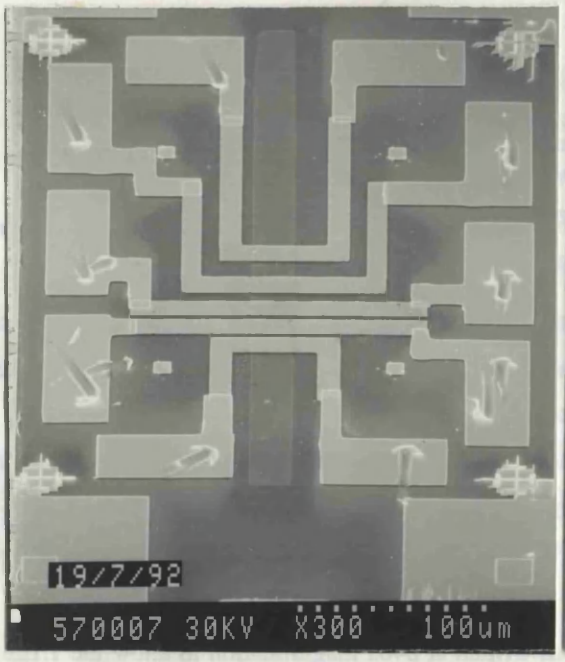

Figure 4.8.12 - SEM Micrograph of TLM PCM

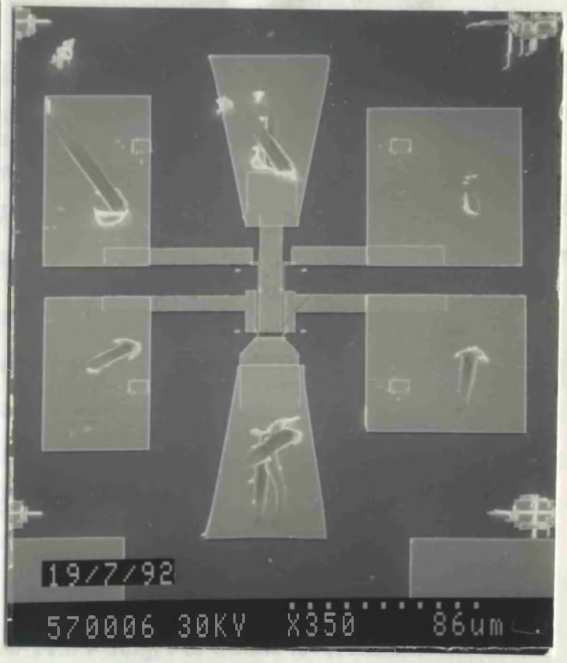

Figure 4.8.13 - SEM Micrograph Overview of Gate Resistance PCM

This PCM allowed the ohmic contact resistance of the ohmic metallisation to the layer structures to be determined using the Transmission Line Method[4.14].

The ohmic level of the gate resistance PCM was also defined. This structure, shown in Figure 4.8.13, was used to make a 4-terminal measurement of DC end-to-end gate resistance. To ensure the length of the gates in this PCM were identical to those of the HFETs, the resistance is measured on gate structures aligned in a 1.1μm source drain gap.

After development, the samples were ashed in oxygen for 1 minute and de-oxidised in 4:1 H_2O:HCl for 30 seconds and then immediately loaded into the Plassys evaporator.

4.8.3.1 Ohmic Contact Metallisations

The ohmic contact recipe for the InP based structure was obtained from the layer growers in Michigan[4.17] and was found to work well without modification. From the substrate, the metallisation was:

Ge	70nm
Au	140nm
Ni	50nm
Ti	20nm
Au	70nm

The ohmic metallisation for the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs devices evolved from that previously developed for 2DEG structures in the Nanoelectronics Group[4.18]. The thickness of the top layer of gold in this contact was adjusted so that the total metallisation thickness was equal to the InP based material ohmic contact so that any planarisation effects of the gate resist thickness in the source drain gap of devices would be independent of layer structure. From the substrate, the contact recipe was:

Au	70nm
Ge	25nm
Ni	10nm
Au	180nm

Both of the ohmic metallisations were developed with the aim of producing a low contact resistance, smooth morphology ohmic contact. The morphology was of considerable importance, as good morphology makes gate alignment easier to accomplish.

The ohmic contact was lifted-off in warm (45°C) acetone.

4.8.3.2 Ohmic Contact Annealing and TLM Evaluation

Once deposited and lifted-off, the ohmic contacts were annealed on a silicon substrate in a Jipilec Rapid Thermal Annealer. Annealing was carried out in a N_2 atmosphere.

The annealing cycle consisted of

i) a 10 second ramp from room temperature to the annealing temperature

ii) an anneal at an optimised temperature for an optimised time

iii) a 10 second ramp down from the annealing temperature to room temperature again

The cycle was optimised by annealing a number of TLM test samples metallised along with the device chips at various temperatures for different durations. The TLM test patterns were fabricated on each of the three material structures.

Optimum annealing conditions, determined by measuring the contact resistance are shown in Table 4.8.1. The ohmic contact resistance and sheet resistance measured on the device chips is also shown.

Layer	Temp. (°C)	Time (s)	R_c (Ωmm)	R_{sheet} (Ω/sq)
A322	360	30	0.46	775
TF141	340	30	0.05	250
MB1	360	60	0.11	140

Table 4.8.1 - Optimum Annealing Temperature and Contact Resistance for MBE Layers used in this Study

The contact resistance of A322 chips was larger than the optimised value of 0.2Ωmm obtained on the test samples. The reasons for the lack of reproducibility are unclear.

Although its resistance was small, the contact morphology on the TF141 layer structure was poor in comparison with the other layers as shown in Figures 4.8.14. This poor morphology made gate alignment on the TF141 devices very awkward.

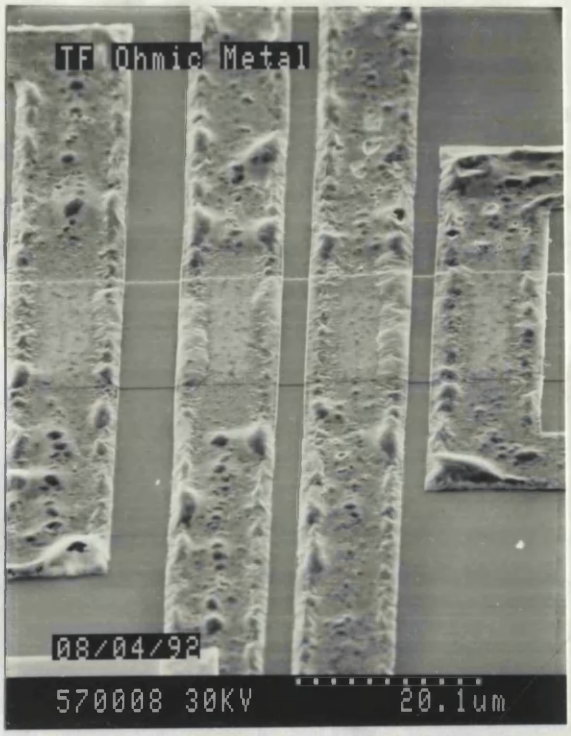

Figure 4.8.14 - SEM Micrograph of Annealed Ohmic Contact to TF141 showing poor Morphology

4.8.4 Level 4 - Wiring Level

One of the limitations of the EBL system is that over a period of around two hours, the beam current decreases appreciably. This drop in beam current results in pattern underexposure.

To achieve the resolution to produce a 1.1μm source drain gap, it was necessary to write the ohmic contact level using a 640Å spot size. It was only possible to write the basic ohmic contact pattern on the mesas of a device chip with this spot size in two hours. Thus the ohmic contacts still had to be joined to the large area bondpads. Due to their size, the bondpads were written at low magnification with a large spot size to minimise writing time, limiting the resolution of the pattern and its alignment. For these reasons, pattern overlay errors may have been encountered if the bondpad was aligned directly to the ohmic level. Thus, definition of most of the groundplane of the device - the wiring level, was written between the ohmic and bondpad levels. The wiring level is shown in Figure 4.8.15, and extends the ohmic contact to join the subsequently defined bondpad level. There are small holes in the wiring level so that the gate alignment marks can still be seen.

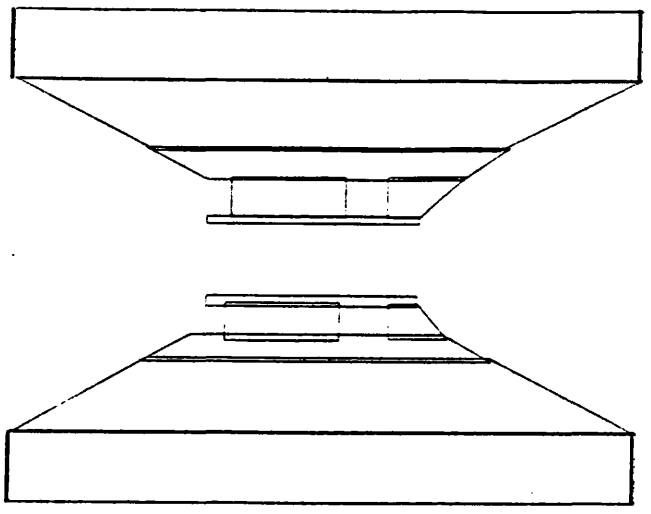

Figure 4.8.15 - Wiring Level

The resist and SEM writing conditions used are shown below:

Resist - Bilayer	5800Å 85k mw PMMA (10% BDH) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	640x
Spot Size	125nm
Developer	2.5:1 IPA:MIBK at 23°C for 30s

After development, the sample was oxygen ashed for 1 minute and de-oxidised in 4:1 H_2O:HCl for 30 seconds before metallisation which consisted of :

Ti	30nm
Au	200nm

Lift-off was performed in warm acetone.

4.8.5 Level 5 - Bondpad Level

The HFET devices were designed to be compatible with Cascade Microtech rf probe heads suitable for on wafer S-parameter characterisation. The probe heads have a coplanar structure with characteristic impedance of 50Ω to the probe tips. The probe tip pitch was 100μm. The bondpad pattern shown in Figure 4.8.16 consists of source (top and bottom), gate (left) and drain (right) pads in a coplanar configuration with the source contact acting as the groundplane of the device.

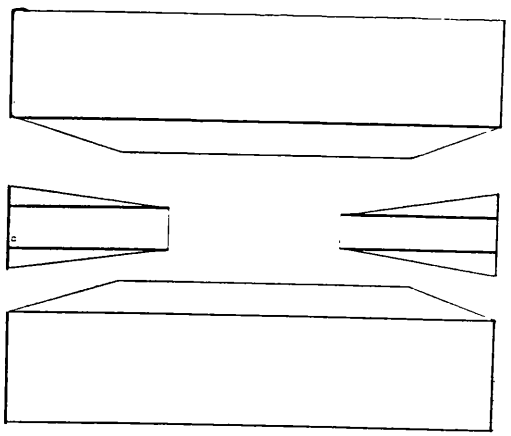

Figure 4.8.16 - Bondpad Level

The device separation on the chip was designed so that the source contacts of adjacent devices overlapped resulting in a large area groundplane across the whole the chip (Figure 4.8.2). The width to space ratio of the tapering gate and drain pads was designed to give a coplanar waveguide structure with characteristic impedance (Z_o) of 50Ω all the way to the active part of the HFET. The ratio of the probe pad width (S) to the spacing between the pad and the groundplane (W) as a function of distance along the tapering pad was calculated to be 1.4 using the formula[4.19]

$$Z_o = 30\pi \frac{[K(k') / K(k)]}{[(\varepsilon_r + 1)/2]^{\frac{1}{2}}} \quad - -$$

where

$$k = \frac{S}{(S + W)}$$

and

$$k' = (1 - k^2)^{\frac{1}{2}}$$

with K(k) a complex integral of the first kind and ε is the dielectric constant of GaAs. The formula assumes a groundplane of infinite extent.

A thick resist layer was used to lift-off 0.5μm of metal thus ensuring good contact between the probe tips and the bondpad. The resist and SEM writing conditions were:

Resist - Bilayer	11000Å 85k mw PMMA (15% BDH) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	320x
Spot Size	250nm
Developer	1:1 IPA:MIBK at 23°C for 30s

Prior to metal deposition, the sample was ashed in oxygen for 1 minute and deoxidised in 4:1 H_2O:HCl for 30 seconds before being metallised with :

Ti	30nm
Au	500nm

The metallisation was lifted off in warm acetone.

4.8.6 Level 6 - Gate Level

The gate level of the HFET is the most critical in the fabrication procedure, as both the gate length and the gate recess depth significantly influence the performance of the completed device. Generally, short gate length structures (<100nm) require the use of thin resist layers to achieve the desired resolution[4.20]. This reduces the amount of gate metal that can be lifted-off, and so increases the value of the gate resistance of the device, limiting device performance. In the course of this work, devices with sub-100nm footprint conventional (or pyramidal) gate structures as well as sub-100nm footprint T-gate structures have been successfully fabricated. The route to the definition of these gate structures will be described next. The gate recess etch process is then detailed. Finally in this section, the resistances of the gate structures (measured using the gate resistance PCM) are presented.

4.8.6.1 Gate Alignment

The alignment pattern shown in Figure 4.8.17 was used to position the gate accurately.

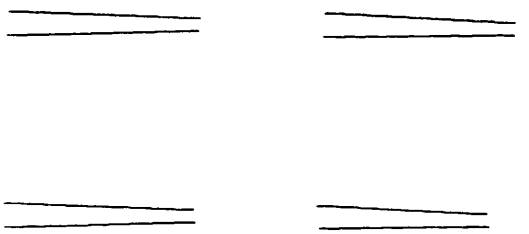

Figure 4.8.17 - Very Fine Gate Alignment Pattern

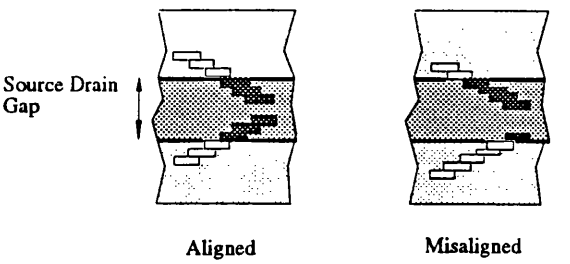

Figure 4.8.18 - Alignment Using Gate Alignment Strategy

Consider one of the four groups of lines in the alignment pattern. Each line is composed of staggered segments as shown in Figure 4.8.18.

The alignment method uses differences in signal intensity when the lines are scanned across the edges of a source drain gap of a sacrificial device on the chip. When segments of each line scans over ohmic metal, a bright signal from the gold in the contact is obtained. When segments are scanned in the source drain gap the signal is darker, as the substrate is being imaged. When aligned, the high contrast signal from

scanning over ohmic metal will be of the same length (ie the number of segments scanning ohmic metal in the two lines is equal). If misaligned however, the length of the bright part of the lines will be different. Using all four sets of vernier patterns allows high accuracy gate alignment to be performed.
As before, having manually aligned the sample, the automatic alignment system was initialised, and subsequent alignment performed under computer control.

4.8.6.2 Pyramidal Gate Definition

To study the dependence of gate length on device performance, 200, 120 and 80nm gate length HFET's were fabricated, as previous work had indicated that poor scaling limited device performance for gate lengths below 80nm[4.21]. For these linewidths, a relatively thick bilayer resist can be used for gate definition which allows around 200nm of gate metal to be lifted-off. The resist and SEM writing conditions were:

Resist - Bilayer	5800Å 85k mw PMMA (10% BDH) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	2500x
Spot Size	8nm
Developer	2.5:1 IPA:MIBK at 23°C for 30s

A series of exposure tests showed the required gate lengths could be produced using the pattern of Figure 4.8.19 with the following exposure parameters :

Linewidth (nm)	Exposure (μCcm^{-2})	No. of Pixels
200	2500	8
120	2500	4
80	2500	2

Table 4.8.2 - Exposure Dose and Pixel Size of Features to Produce Linewidths of 200nm, 120nm and 80nm

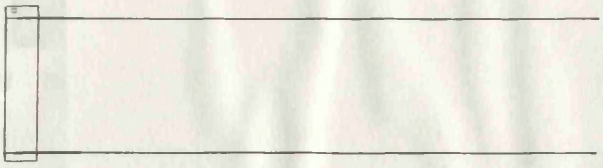

Figure 4.8.19 - Gate Level

An additional 8 pixel gate feed on the left of the gate lines is included in the 2 and 4 pixel (80nm and 120nm) structures to improve step coverage yield onto the mesa.

Micrographs of the three different gate lengths are shown in Figures 4.8.20-22. It was only possible to achieve these linewidths repeatedly if the astigmatism of the electron beam was minimised at the start of each gate lithography session. In addition, the automatic focussing system was used to ensure accurate focussing at every site.

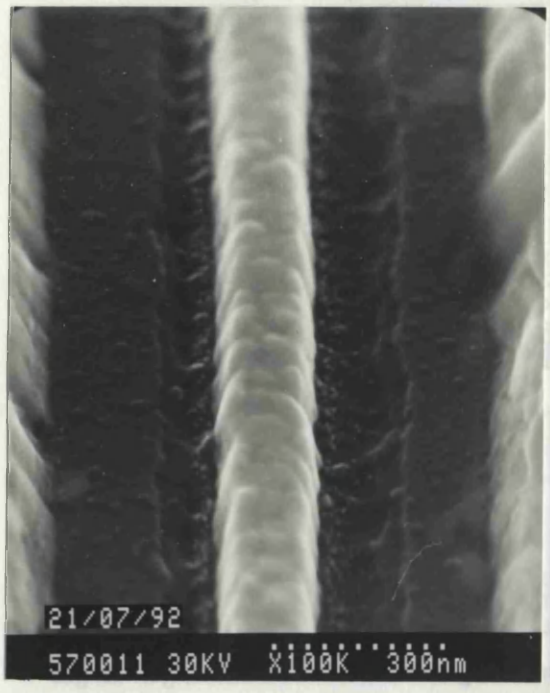

Figure 4.8.20 - SEM Micrograph of 200nm Pyramidal Gate

Figure 4.8.21 - SEM Micrograph of 120nm Pyramidal Gate

Figure 4.8.22 - SEM Micrograph of 80nm Pyramidal Gate

4.8.6.3 T-Gate Definition

To reduce the resistance of the gate stripe whilst maintaining a small footprint in contact with the semiconductor, the T-gate structure can be implemented[4.22]. By utilising the properties of resists of different sensitivities, it is possible to achieve the desired structure, as shown in Figure 4.8.23

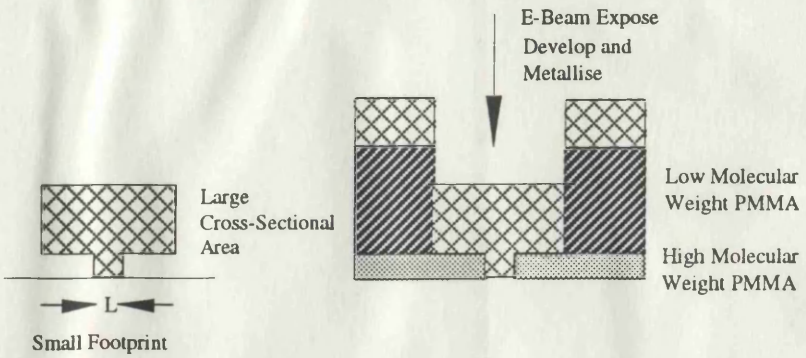

Figure 4.8.23 - T-gate Fabrication Using PMMA's of Different Sensitivity

In essence, it is only necessary to spin a layer of high sensitivity resist on a layer of low sensitivity. In practice, whilst slightly more complex, the employed strategy has the same philosophy.

The resist structure used was a tri-layer system as shown in Figure 4.8.24. The bottom, gate length defining layer was a thin layer of 350k mw PMMA. The middle layer was a thick layer of a co-polymer of methylmethacrylate and methacrylic acid P(MMA/MAA)[4.24] which has a greater sensitivity than PMMA. The top layer was a thin layer of 85k mw PMMA incorporated to provide an overhang resist profile and improve lift-off yield.

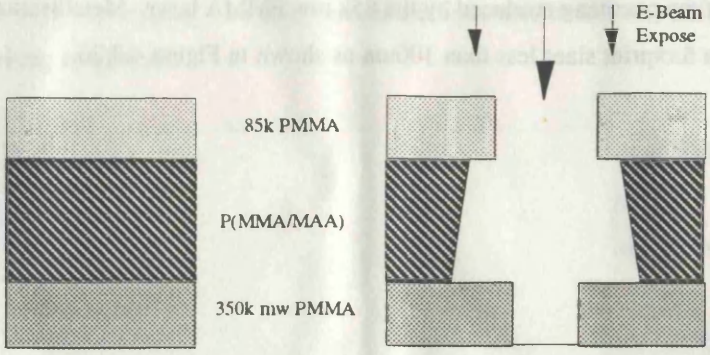

Figure 4.8.24 - The Tri-Layer Resist Structure Used in this Project to Fabricate T-Gate Structures

A central line was written with an exposure sufficient to develop out the sub-100nm footprint. To increase the area of the top of the 'T', side lines of low exposure dose were written. The large sensitivity difference between P(MMA/MAA) and 350k mw PMMA allowed a side line exposure to be chosen which caused the exposed P(MAA/MAA) to be removed on development without affecting the footprint size. Initial exposure test were conducted on a planar substrate with the following resist and SEM parameters:

Resist - Tri-layer	1000Å 350k mw PMMA (4% ELV) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	3000Å P(MMA/MAA) (9% CoPoly) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	500Å 85k mw PMMA (2.5% BDH) spun at 5000rpm for 60s
	Bake 4 hours 180°C
Magnification	2500x
Spot Size	8nm
Developer	2.5:1 IPA:MIBK at 23°C for 40s

The exposure strategy is shown in Figure 4.8.25.

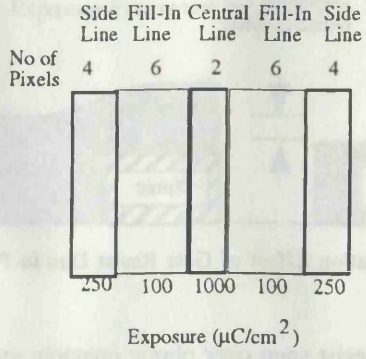

Figure 4.8.25 - Exposure Strategy for Realisation of T-Gate Structures

In addition to the central 2 pixel line exposure of 1000μCcm^{-2} and the 4 pixel line side line exposure of 250μCcm^{-2}, the 6 pixel spacing between the central and side lines was also exposed with 100μCcm^{-2} to

reduce the size of the overhang produced by the 85k mw PMMA layer. Metallisation and lift-off resulted in structures with footprint sizes less than 100nm as shown in Figure 4.8.26.

Figure 4.8.26 - SEM Micrograph of 100nm T-Gate on a Planar Substrate

However, it proved impossible to successfully implement this process in a HFET because of resist planarisation in the source drain gap. Figure 4.8.27 shows the effect of a small source drain gap on resist thickness.

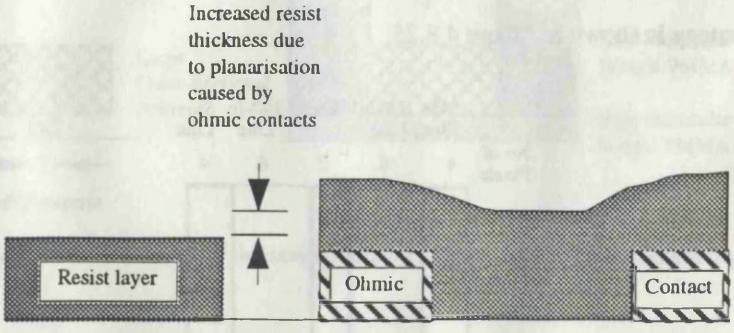

Figure 4.8.27 - Planarisation Effect of Gate Resist Due to Presence of Ohmic Contacts

Cross-sectional SEM studies of resist spun over ohmic contacts separated by 1.1μm indicated that the 4500Å thick resist layer optimised for T-gate fabrication on a planar substrate was around 6600Å thick in the source drain gap. The process failed because of the increase in resist thickness.

To overcome this problem, the resist concentrations and spin speeds were altered until each of the individual T-gate resist components was of the required thickness when measured in cross-section in a source drain gap. To allow reproducibility of the process, the resist components' thicknesses as spun on

a planar substrate were talystepped. The layer thicknesses measured in this way are given below together with the SEM writing conditions:

Resist - Tri-layer	540Å 350k mw PMMA (2.5% ELV) spun at 5000rpm for 60s
	Bake 1 hour 180°C
	2100Å P(MMA/MAA) (~6% CoPoly) spun at 6000rpm for 60s
	Bake 1 hour 180°C
	460Å 85k mw PMMA (2.5% BDH) spun at 6000rpm for 60s
	Bake 4 hours 180°C
Magnification	2500x
Spot Size	8nm
Developer	2.5:1 IPA:MIBK at 23°C for 40s

The co-polymer was diluted in cellosolve until the planar layer thickness was 2100Å. This was calculated to be approximately 6% weight by volume.

It was necessary to re-optimise the exposure doses for T-gates in source drain gaps. In order that the resist planarisation effect be included in the optimisation, exposure tests were performed in source drain gaps by aligning gates to test structures whose ohmic metal thickness was identical to that of the HFET devices. To determine the resist profile in the source drain gap, the test structures were cleaved and examined in cross-section using an SEM.

The optimised exposure conditions shown in Table 4.8.3 produced the resist profile shown in Figure 4.8.28. A lifted off 80nm footprint T-gate aligned in a source drain gap is shown in Figure 4.8.29.

	Exposure ($\mu C/cm^2$)
Centre Line	750
Side Line	250
Fill In Line	100

Table 4.8.3 - Exposure Parameters for T-Gate in Source Drain Gap

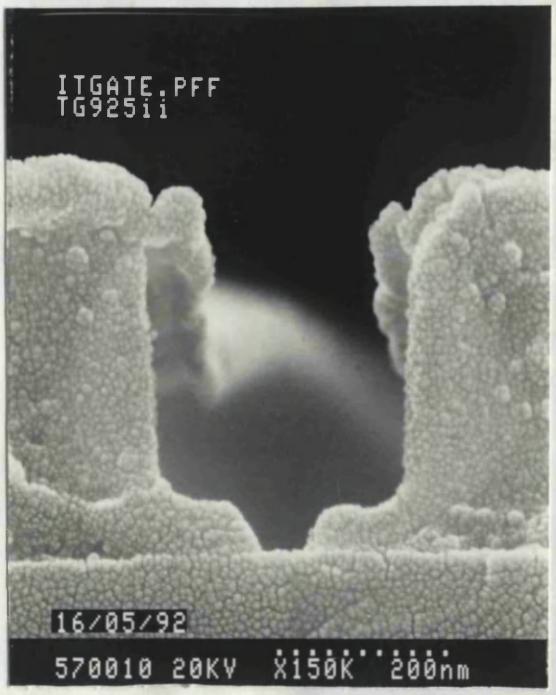

Figure 4.8.28 - SEM Micrograph of Resist Profile in Source-Drain Gap

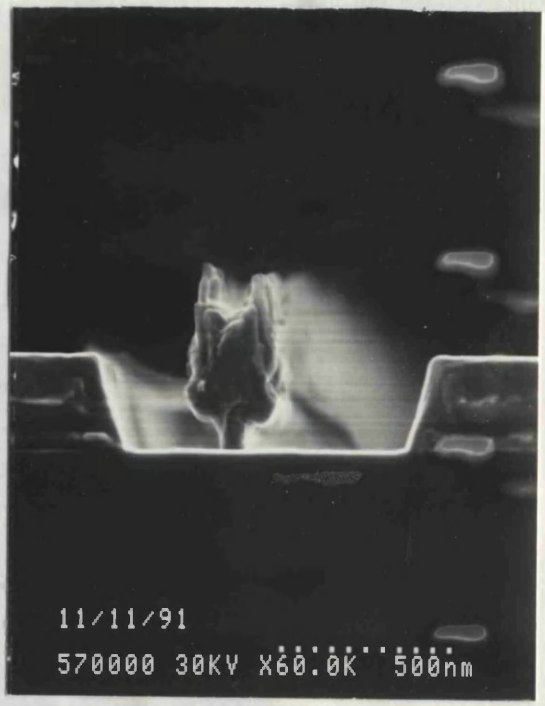

Figure 4.8.29 - SEM Micrograph of Lifted of 80nm Footprint T-Gate in Source Drain Gap

Across a $10mm^2$ chip, considerable variation of the resist thickness in source drain gaps was observed. Figures 4.8.30 and 4.8.31 show identical exposure conditions for 2 different sites where the resist thicknesses in the source drain gaps are 390nm and 460nm respectively. The process had insufficient lattitude to cope with this variation in resist thickness.

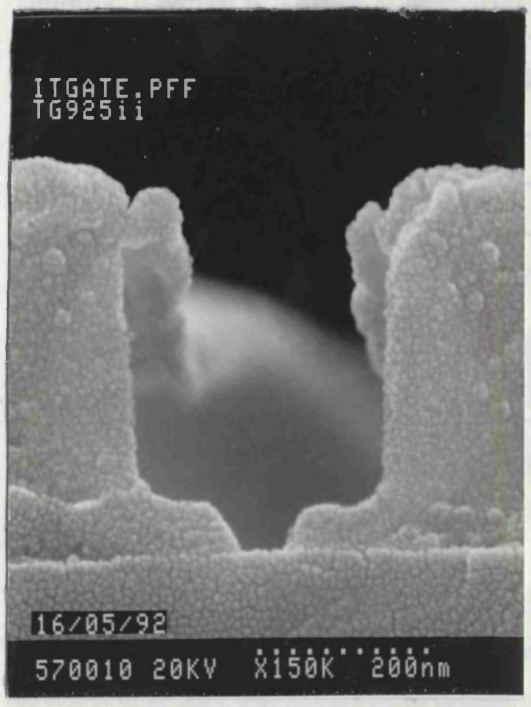

Figure 4.8.30 - SEM Micrograph Showing Lack of T-Gate Process Latitude

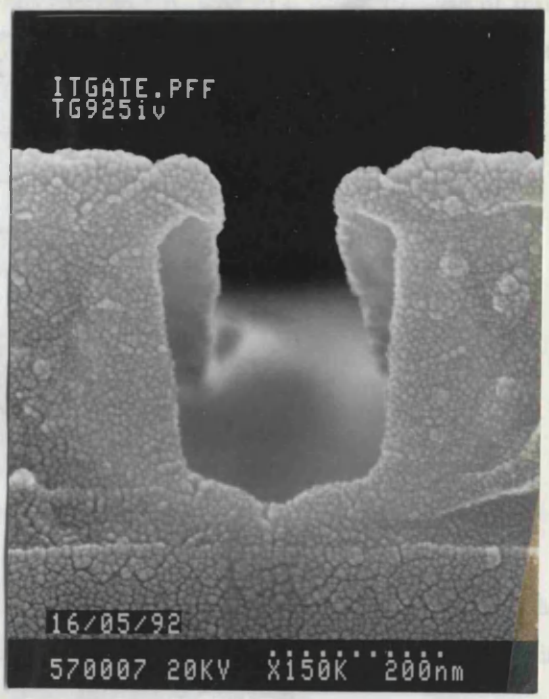

Figure 4.8.31 - SEM Micrograph Showing Lack of T-Gate Process Latitude

Although a sub-100nm T-gate process has been developed and demonstrated in the course of this work, it is of low yield and is not yet sufficiently advanced to be incorporated into circuits.

4.8.6.4 Gate Recess Etching

As discussed in Section 2.7, an HFET technology incorporating a gate recess etch results in a reduction in parasitic access resistance, and also reduces the influence of surface states on device performance. Gate recess etching was performed using 5:1:200 (95%)H_2SO_4:(35%)H_2O_2:H_2O for the GaAs based samples and 1:1:200 (70%)H_3PO_4:(35%)H_2O_2:H_2O for the InP based samples. 500ppm of a wetting agent (Fluorad FC-93) was added to each etch[4.24]. This had been found to improve the uniformity of gate recess etching. In addition, beakers containing IPA and water were also prepared.

The samples were first rinsed in water, then IPA and placed in the etch for 45 seconds. After etching, the samples were rinsed in water and IPA before finally being blown dry with nitrogen.

Several devices on each chip were probed through the gate resist, and the saturated drain current measured using an HP4145B parameter analyser. From the 2DEG sheet electron concentration evaluated by the magnetoresistance technique and assuming

i) an average carrier velocity of $1.0x10^5 ms^{-1}$

ii) the barrier height of the Schottky gate metal and a free surface were similar

a target saturation current to stop etching was calculated for the 80μm wide devices as shown in Table 4.8.4.

Material	A322	TF141	MB1
Target Current (mA)	12.7	18.0	48.6

Table 4.8.4 - Target gate Recess Currents for Materials Used in this Study

For the GaAs based devices, the samples were subjected to repeated etching until this target current was reached. This took around 75 seconds for devices fabricated on A322 and 180-240 seconds for devices on TF141. Figure 4.8.32 shows the saturated drain current as a function of etch time for two A322 device chips.

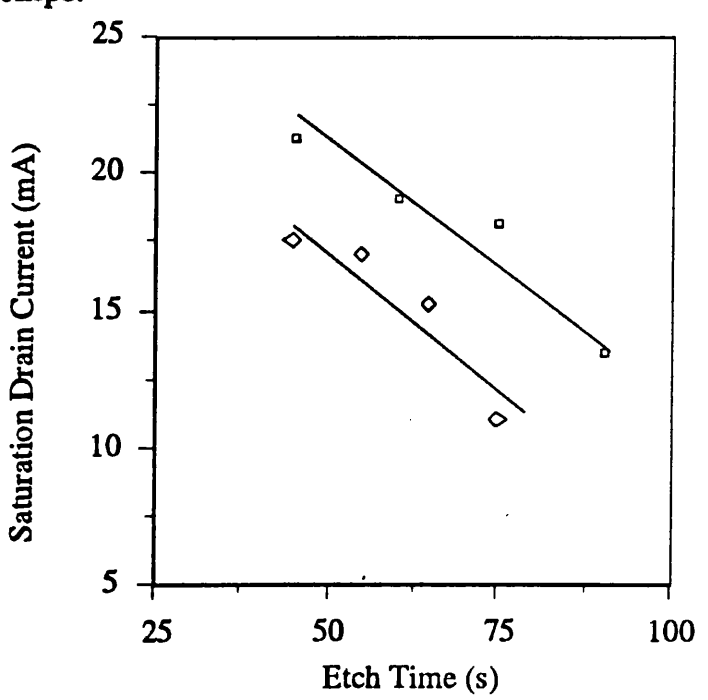

Figure 4.8.32 - Saturation Current as a function of Gate Recess Time for Two A322 Chips

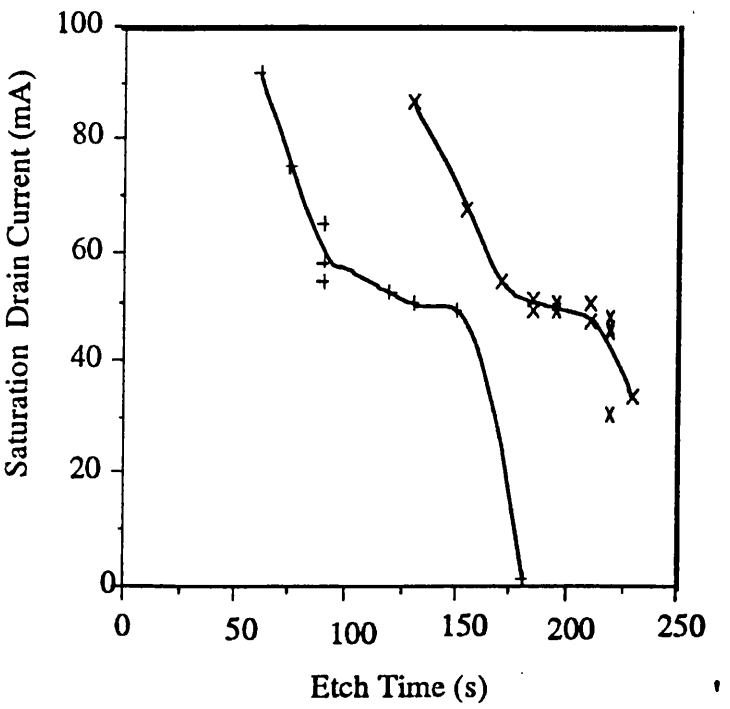

Figure 4.8.33 - Saturation Current as a function of Gate Recess Time for Two TF141 Chips

One of the limitations of gate recessing using a wet chemical etch is the variable initiation time of the etching process. As well as being chip dependant, the initiation time can also vary from device to device on a chip, resulting in the spread in the data shown in Figure 4.8.32.
Figure 4.8.33 shows the saturation drain current as a function of etch time for two TF141 device chips.
In an effort to explain the shoulder in the curves, a simple analytic model was developed which involved repeatedly solving Poissons Equation for the layer structure as material was removed from the surface. The Poisson solution gave free carrier concentrations in each layer and allowed the saturated current to be calculated as a function of etch time based on the following assumptions :

i) A constant etch rate of 20nm per minute independent of the material being etched
ii) A constant carrier velocity of $1.0x10^5 ms^{-1}$ independent of the material
iii) No carrier diffusion included
iv) No quantisation effects included
v) A surface potential of 0.7V for both GaAs and AlGaAs
vi) Complete ionisation of all donors

As shown in Figure 4.8.34, this simple model allows the observed effect to be simulated. Figure 4.8.34 also includes a simulation of the structure using the self-consistent Poisson/Schroedinger solver from the University of Santa-Barbara. A constant etch rate of 20nm per minute and a constant carrier velocity of $1.0x10^5 ms^{-1}$ were assumed in the self-consistent solution.

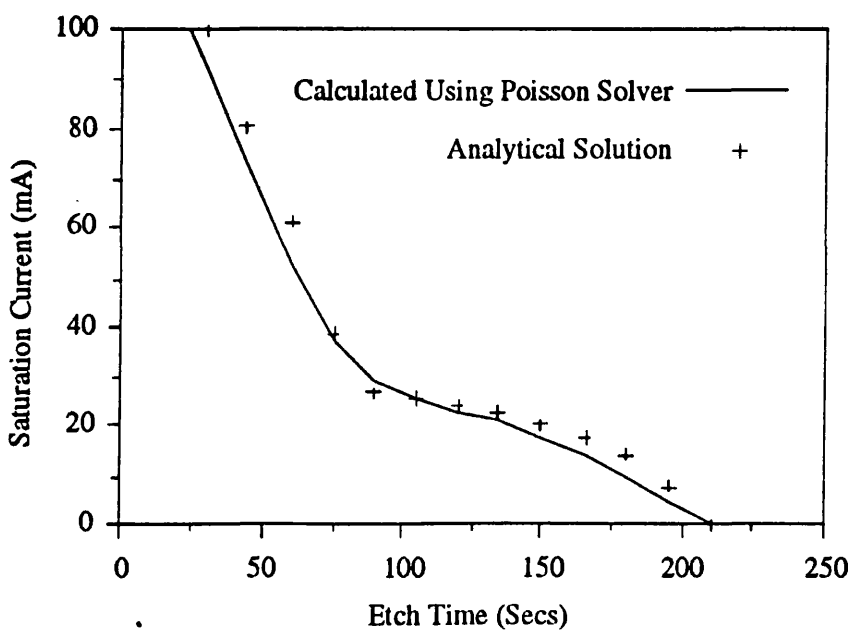

Figure 4.8.34 - Simulated Saturation Current dependence on Gate Recess Time for TF141

The presence of the shoulder results from the doping concentrations and thicknesses of the GaAs cap and the AlGaAs Schottky layers of the structure as well as the presence of the δ doped layer.
The saturation current falls at 1.25mA/s when the n^+ GaAs cap layer is being etched. This continues until 220Å of the cap is removed, at which time the surface depletion region reaches the AlGaAs Schottky layer. When a further 30Å of the cap have been removed, the Schottky layer is fully depleted as it is not heavily doped. Thus the surface depletion layer is around 550Å thick when it reaches the δ doped region. The situation is now analogous to a parallel plate capacitor, as shown in Figure 4.8.35.

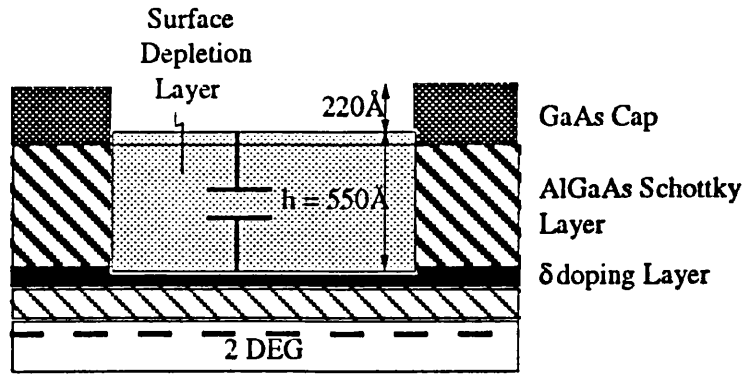

Figure 4.8.35 - Capacitance Model to Explain the Shape of Figure 4.8.34

The capacitance per unit area is

$$\frac{\varepsilon}{h} = \frac{qn_{\delta 1}}{V} \qquad (4.8.1)$$

where

$n_{\delta 1}$ is the charge concentration which must be supplied to the capacitor from the δ doped layer

h is the surface / δ doped layer spacing

V is the built-in surface potential

The charge in the δ doped layer which can still contribute to the saturation current is,

$n_{\delta doping} - n_{s2DEG} - n_{\delta 1}$

where

$n_{\delta doping}$ is the original δ doped layer sheet concentration of $3.0 \times 10^{16} m^{-2}$

n_{s2DEG} is the 2DEG concentration of $1.4 \times 10^{16} m^{-2}$, which was supplied by the δ doped layer.

At a separation of h = 550Å, when the surface depletion region reaches the δ doped region, Equation 4.8.1, can be used to show the saturation current changes by only 0.07mA/s.
As etching continues, the surface/δ doped layer separation is reduced and the change in saturation current increases. However, even when the δ doped region is fully depleted, the saturation current still only changes at 0.2mA/s.
Having fully depleted the δ doped layer, the surface depletion edge quickly reaches the 2DEG. As etching continues, the 2DEG is depleted of charge until finally, the whole layer is fully depleted.

The interesting point to note from Figure 4.8.33 is that the shoulder occurs at around 50mA, whereas the shoulder in both the calculated solutions lies at around 25mA. This discrepancy could be due to :

i) The saturation velocity of the materials is greater than $1.0 \times 10^5 ms^{-1}$

ii) The δ doped layer is close to 5×10^{12} cm^{-2} rather than $3 \times 10^{12} cm^{-2}$

The MBE growers place an upper limit of 30% error on the determination of the δ doped sheet electron concentration, thus a lower estimate of the effective carrier velocity of $1.8 \times 10^5 ms^{-1}$ can be determined from this analysis.
The curves of Figure 4.8.33 are displaced from one another in time showing that the etch initiation time is variable.

Termination of the gate recess etching in the InP based samples was complicated by the fact that until the cap layer was removed, it was impossible to saturate the drain current of the HFET test devices without the surface breaking down catastrophically. Thus, recess etching of these samples was terminated when the drain source current saturated without the devices blowing up, rather than aiming for the target current.

Immediately prior to gate metal deposition, the samples were de-oxidised in 1:1:200 H_3PO_4:H_2O_2:H_2O for 5 seconds. (All samples had exposed layers containing aluminium after the gate recess etching was terminated, so it was not possible to deoxidise using HCl)

Samples were metallised with:

Ti	30nm
Au	200nm

This was lifted-off in warm acetone.

4.8.6.5 Measurement of Gate Resistance

Using the gate resistance PCM, shown in detail in Figure 4.8.36, the resistance of each of the gate lengths of pyramidal and T-gate structures was determined using a 4 terminal resistance measurement.

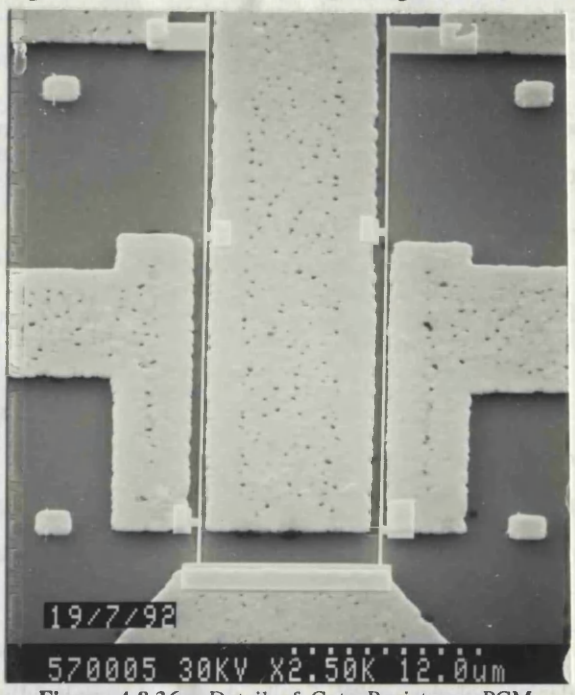

Figure 4.8.36 - Detail of Gate Resistance PCM

The results are shown in Table 4.8.4.

Gate Structure	Gate Length (nm)	Resistance (Ωmm^{-1})
Pyramidal	200nm	850
Pyramidal	120nm	1750
Pyramidal	80nm	5000
T-Gate	80nm	700

Table 4.8.4 - Measured Gate Resistance for Pyramidal and T-Gate Structures of Different Footprint Sizes

This shows the advantage of using a T-gate structure to reduce the gate resistance, with almost an order of magnitude reduction in resistance for 80nm footprint structures.

4.9 Ancillary Structures Fabricated for the Project

A number of other structures were fabricated in the course of this work:

i) Hall Bars and Van Der Pauw structures for material characterisation

ii) calibration chips consisting of open circuits, short circuits, thru lines and 50Ω loads to allow the Vector Network Analyser to be calibrated with reference planes as close to the active part of the HFET's as possible, to reduce parasitic effects associated with the bondpads.

4.9.1 Hall Bars and Van Der Pauw Structures

Hall bars and Van Der Pauws were fabricated using two levels - a trench isolation level aligned to an ohmic contact level. The two levels for each structure are shown in Figure 4.9.1. The ohmic contacts were metallised and annealed using the optimised recipes described earlier. Trench isolation was performed using 5:1:200 H_2SO_4:H_2O_2:H_2O for 5 minutes. Samples were mounted and wire bonded to a ceramic chip carrier before being placed in a cryostat.

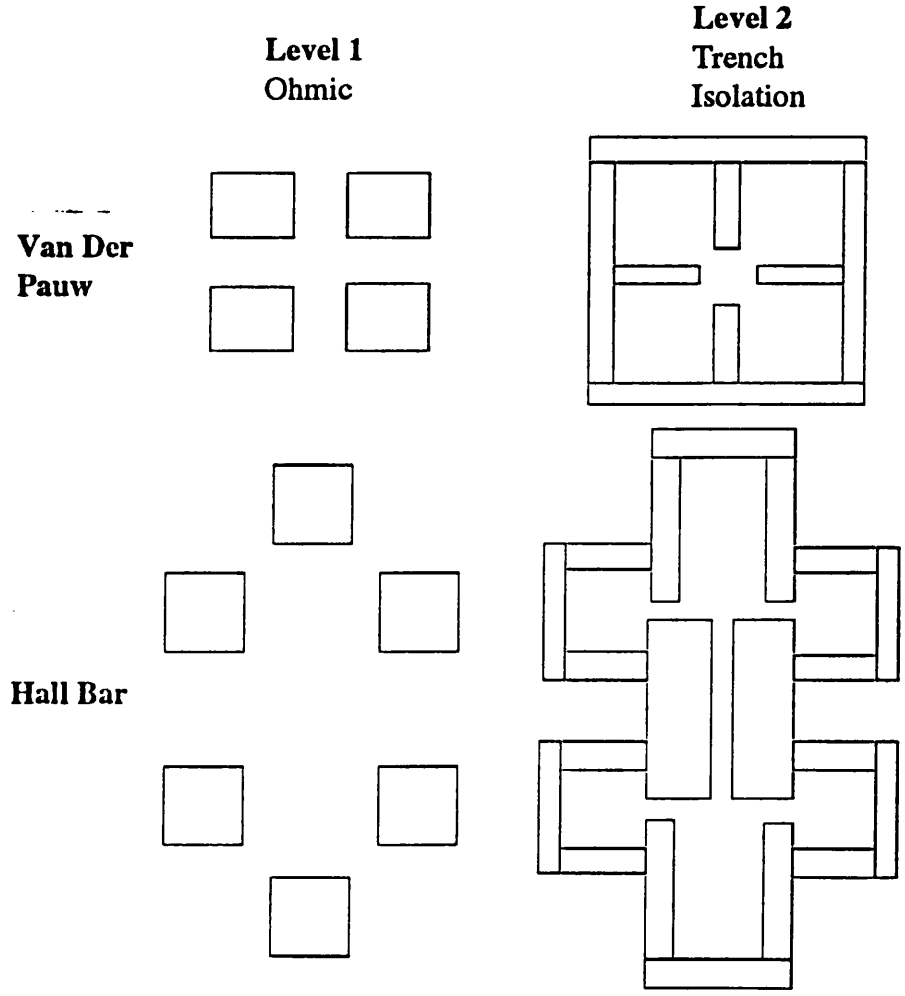

Figure 4.9.1 - Van Der Pauw and Hall Bar Structures
used in the Material Characterisation Studies of Chapter 3

4.9.2 Vector Network Analyser Calibration Standards

Accurate calibration of the Vector Network Analyser is required if the RF performance of short gate length HFETs is to be correctly determined. Calibration using either the Line-Reflect-Match (LRM) or Short-Open-Load-Thru (SOLT) techniques[4.25] require that the Network Analyser be presented with a number of calibration standards to allow it to generate an error model to determine the losses and

frequency response of cables, connectors, transitions etc. in the measurement system. The calibration standards required by the Wiltron 360 Network Analyser were an Open circuit, a Short circuit, a Thru line and a 50Ω Load. By fabricating calibration standards on a semi-insulating GaAs chip with a Bondpad layout identical to that of the HFET's, it is possible to calibrate out the effects of the bondpads to within a few microns of the active part of the device. The configuration of the pads of the calibration standards are shown in Figure 4.9.2.

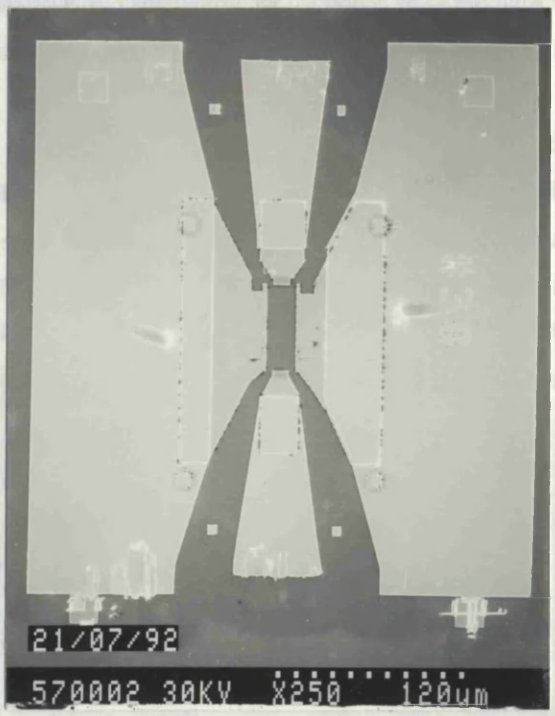

Figure 4.9.2 - SEM Micrograph of Calibration Chip Pad Configuration (note small alignment marks in gap between signal pads and groundplane)

The standards were fabricated using the resists, SEM conditions and metallisation procedures described earlier. One modification to the bondpad pattern was the inclusion of small square alignment marks deposited in the gaps between the signal pads and the groundplane. When performing the calibration, the probes were aligned so they initially contacted the sample at the ends of the signal pads. They were allowed to overtravel on the pads until they lined up with the alignment marks placed 25µm from the edge of the pads. This technique allows identical coupling between the probe head and the pads for all calibration standards as it has been noted that repeatability of probe placement is critical if a high quality calibration is to be generated[4.26]. In addition, this procedure ensured that the contact between the probes and the pads was good whilst conforming to the manufacturers specification for probe overtravel. Figures 4.9.3-4.9.5 shows details of the Open, Short and Thru standards.

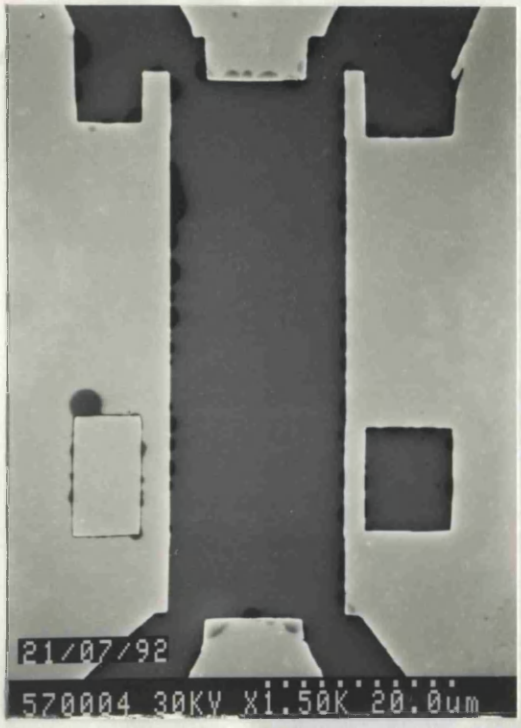

Figure 4.9.3 - Detail of Open Circuit Calibration Standard

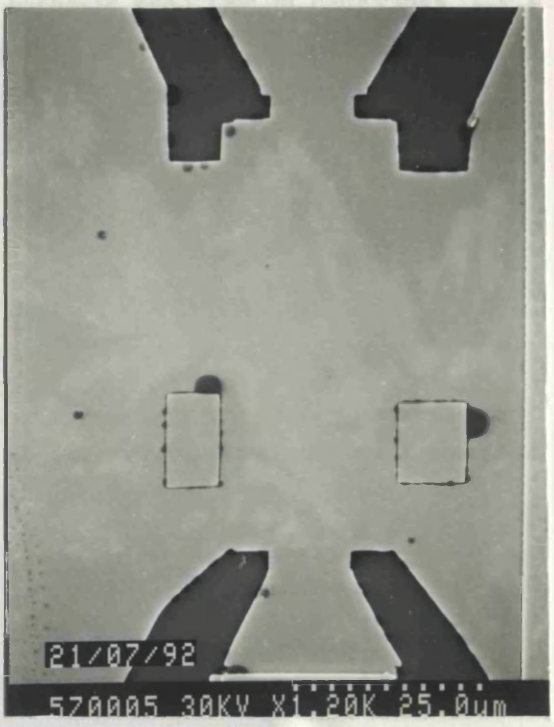

Figure 4.9.4 - Detail of Short Circuit Calibration Standard

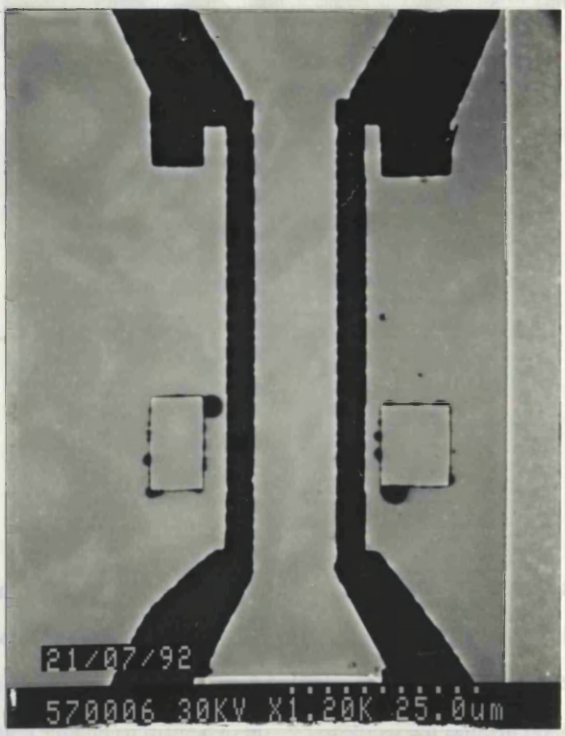

Figure 4.9.5 - Detail of Thru Line Calibration Standard

Once calibrated, the measurement reference planes coincide with the end of the signal input and output pads of the Open Circuit.

4.9.2 Fabrication of 50Ω Load Standard

The 50Ω load standard was fabricated by connecting the input and output signal pads to the groundplane via two 100Ω resistors in parallel as shown in Figure 4.9.6.

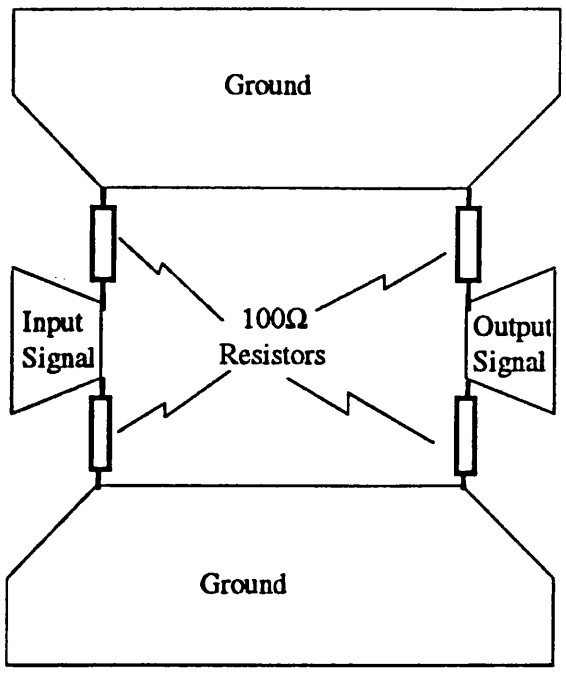

Figure 4.9.6 - Schematic of 50Ω Calibration Standard

The resistors were fabricated using a Nickel Chromium (NiCr) alloy evaporated in the Plassys evaporator. Initially, the sheet resistance of the NiCr as a function of film thickness was determined (Figure 4.9.7).

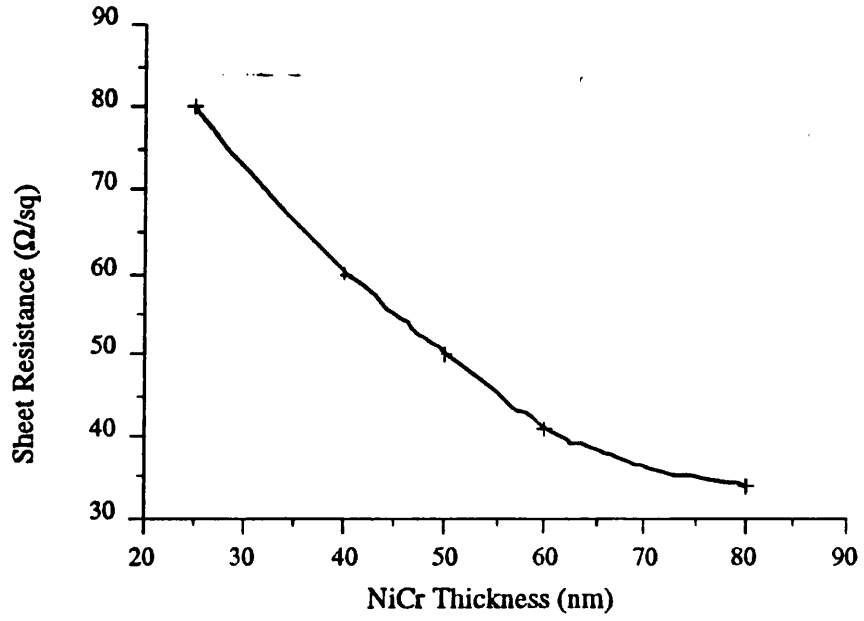

Figure 4.9.7 - Nichrome Sheet Resistance measured as a Function of NiCr Layer Thickness

100Ω resistors were obtained with a NiCr film thickness of 50nm and a linewidth of 1.5μm. It was found that the evaporated NiCr sheet resistance changed with time, probably because the NiCr charge in the evaporator was not eutectic, so it proved necessary to produce a number of load standards with different linewidths bracketed around the designed value of 1.5μm to ensure that resistors of suitable value could be fabricated. Load standards in the range 48Ω to 51Ω were fabricated and used in Network Analyser Calibration. Figure 4.9.8 shows a low angle SEM micrograph of the 50Ω Load calibration standard.

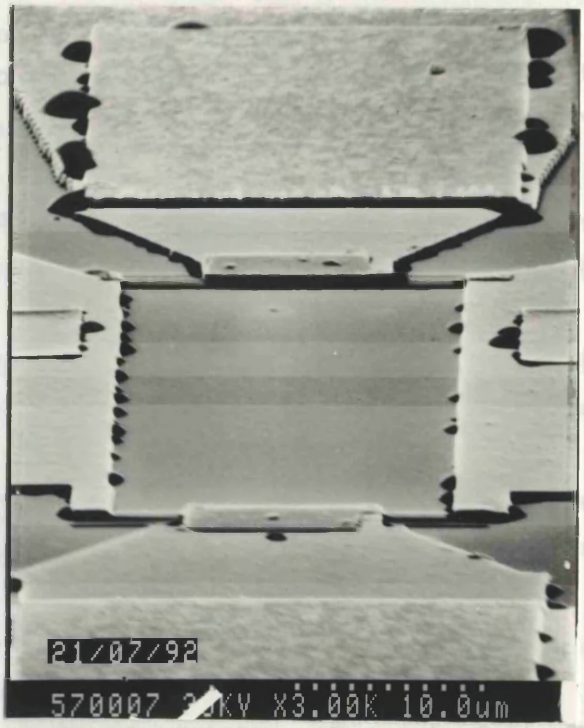

Figure 4.9.8 - Detail of 50Ω Load Calibration Standard

Chapter Summary

This chapter has detailed the fabrication processes used to produce short gate length HFETs with both conventional gates and T-gates. The solution to problems encountered have been highlighted so that in future, such difficulties can be avoided by others.

The characterisation and evaluation of the fabricated devices are now described in Chapter 5.

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Chapter 5 Results

Introduction

The results of DC and high frequency (RF) HFET device characterisation are presented in this chapter. First, the gate length dependence of the HFET DC characteristics are shown. Next, the RF measurement system and problems encountered during calibration of the Vector Network Analyser are discussed. The RF device transconductance and device f_T, obtained from measurements of device S-parameters are then presented, together with an analysis which suggests the effective carrier velocity in the channel of a device is the material transport property which determines the f_T.

Using Touchstone, equivalent circuit models for device operation are extracted and the circuit elements used to deduce that:

i) the RF output resistance is governed by the conduction band offset below the 2DEG of the material structures.

ii) MB1 devices exhibit velocity overshoot effects with extracted effective velocities in excess of $2.0 \times 10^5 ms^{-1}$. TF141 and A322 devices show no conclusive evidence of overshoot effects.

iii) the gate resistance of sub-100nm T-gates is five times lower than for pyramidal gate structures of similar footprint sizes, and results in devices with up to 6dB more Maximum Available Gain at 60GHz

Finally, from the device f_{max}, the gate resistance is shown to be the most influential device parameter in determining the high frequency gain characteristics of short gate length HFETs.

5.1 DC Device Characterisation

The DC device characteristics were obtained using an HP4145B Parameter Analyser. All measurements were made through the Wiltron 360 Network Analyser Test Set using Cascade on-wafer probe heads as the filters in the test set removed mains spikes capable of destroying devices. $I_{ds}(V_{ds},V_{gs})$ and $g_m(V_{gs})$ characteristics of devices fabricated on all three materials for each of the three gate lengths (pyramidal structure) are shown in Figures 5.1.1-5.1.9.

The small drain source saturation voltage (~0.3V) of the HFETs fabricated on the InAlAs/InGaAs/InP (MB1) layer reflects the high electron mobility of the structure. The I(V) characteristics obtained from MB1 devices are dependent on the direction of the gate and drain bias sweeps, the duration of the bias sweeps and the sample illumination. These phenomena point to the existence of traps in this material. Figures 5.1.10 and 5.1.11 show the gate bias dependence of the transconductance of an 80nm gate length device fabricated on MB1 measured in the dark. In Figure 5.1.10, the drain bias is fixed at 0.5V and the gate voltage swept from -1V to +1.2V. In Figure 5.1.11, the drain bias was kept at 0.5V and the gate voltage swept from +1.2V to -1V. Such trapping related effects made evaluation, comparison and interpretation of the gate length dependence of the DC device properties (transconductance, output resistance and threshold voltage shift) impossible and thus any analysis of the DC characteristics of MB1 devices is excluded. As will be shown in Section 5.6.1 however, comparison of RF device performance is possible because the traps cannot respond to the high frequency signals.

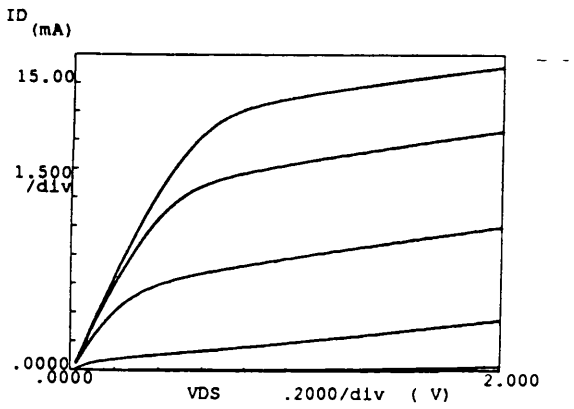

Figure 5.1.1(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 200nm Gate Length A322 HFET (V_{gs} start, 0.5V, stop -0.75V, step -0.25V)

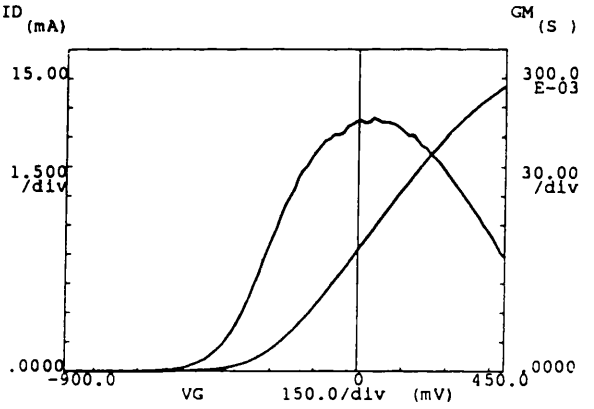

Figure 5.1.1(b) $g_m(V_{gs})$ Characteristic of 200nm Gate Length A322 HFET (V_{ds} = 1.25V)

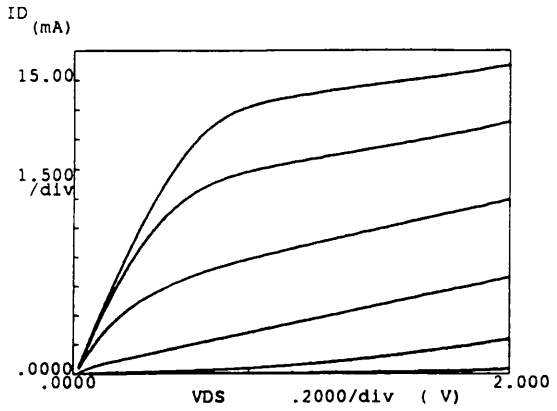

Figure 5.1.2(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 120nm Gate Length A322 HFET (V_{gs} start, 0.5V, stop -0.75V, step -0.25V)

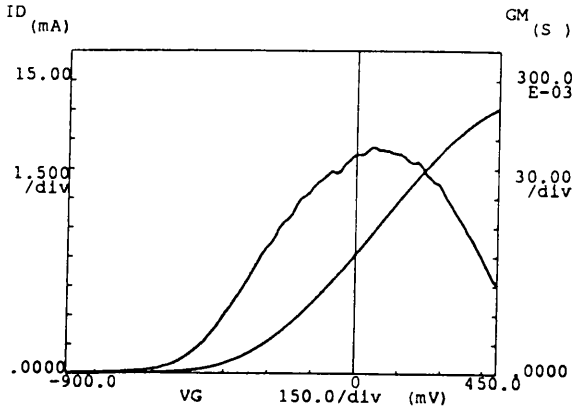

Figure 5.1.2(b) $g_m(V_{gs})$ Characteristic of 120nm Gate Length A322 HFET (V_{ds} = 1.75)

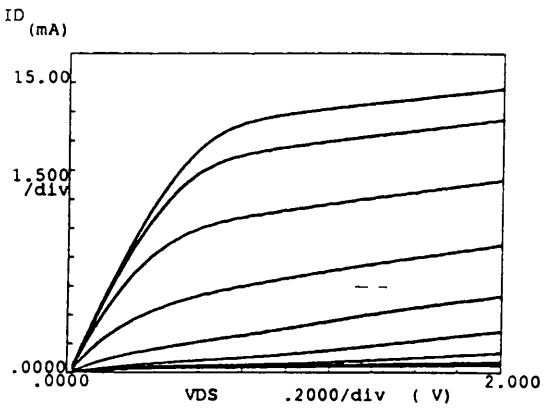

Figure 5.1.3(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 80nm Gate Length A322 HFET (V_{gs} start, 0.25V, stop -2.0V, step -0.25V)

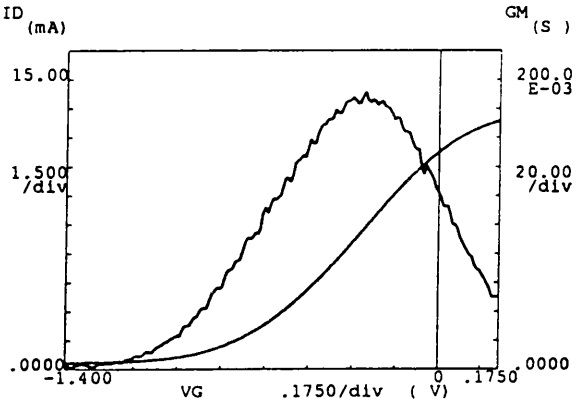

Figure 5.1.3(b) $g_m(V_{gs})$ Characteristic of 80nm Gate Length A322 HFET (V_{ds} = 0.8V)

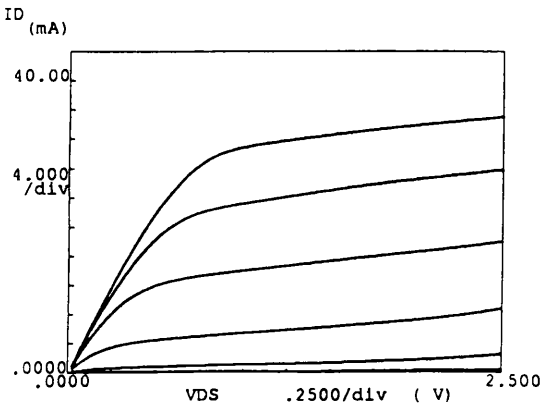

Figure 5.1.4(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 200nm Gate Length TF141 HFET (V_{gs} start, 0.5V, stop -0.75V, step -0.25V)

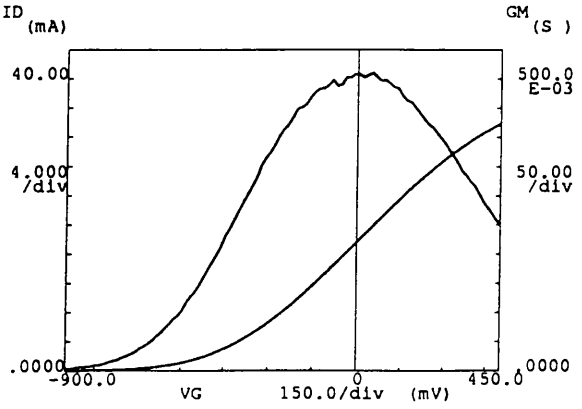

Figure 5.1.4(b) $g_m(V_{gs})$ Characteristic of 200nm Gate Length TF141 HFET (V_{ds} = 1.75V)

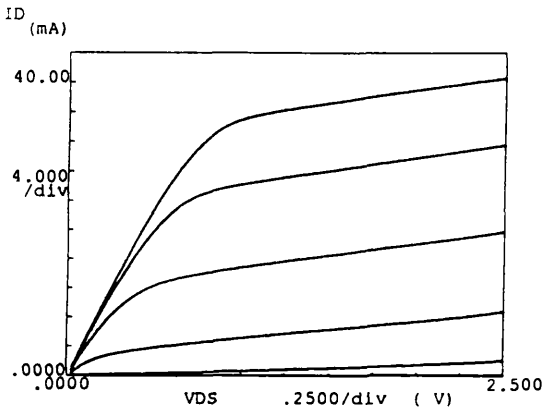

Figure 5.1.5(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 120nm Gate Length TF141 HFET

(V_{gs} start, 0.5V, stop -0.50V, step -0.25V)

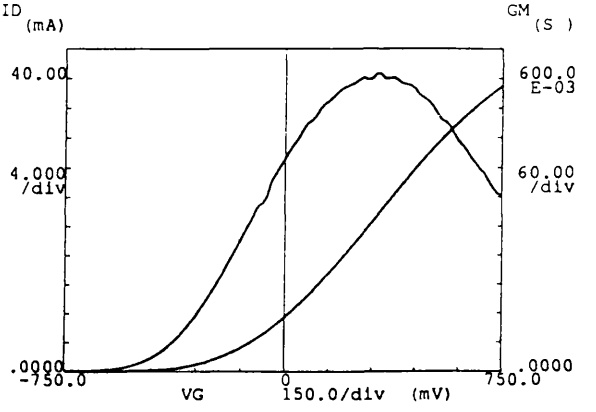

Figure 5.1.5(b) $g_m(V_{gs})$ Characteristic of 120nm Gate Length TF141 HFET

(V_{ds} = 2.0V)

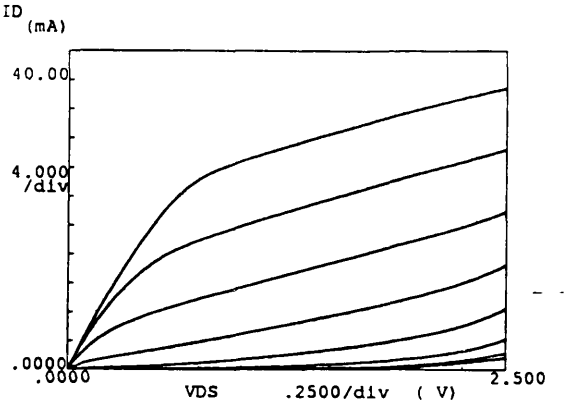

Figure 5.1.6(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 80nm Gate Length TF141 HFET

(V_{gs} start, 0.0V, stop -1.75V, step -0.25V)

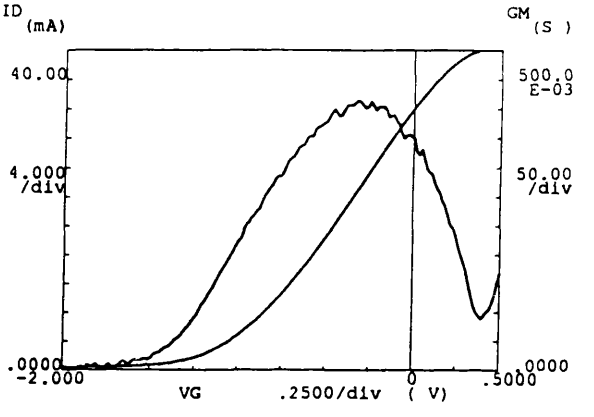

Figure 5.1.6(b) $g_m(V_{gs})$ Characteristic of 80nm Gate Length TF141 HFET

(V_{ds} = 2.0V)

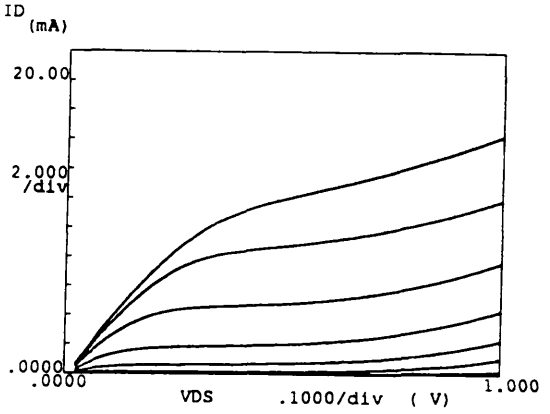

Figure 5.1.7(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 200nm Gate Length MB1 HFET

(V_{gs} start, 0.5V, stop -1.25V, step -0.25V)

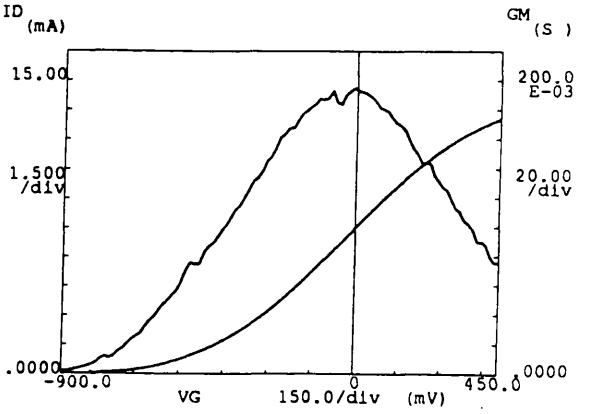

Figure 5.1.7(b) $g_m(V_{gs})$ Characteristic of 200nm Gate Length MB1 HFET

(V_{ds} = 0.6V)

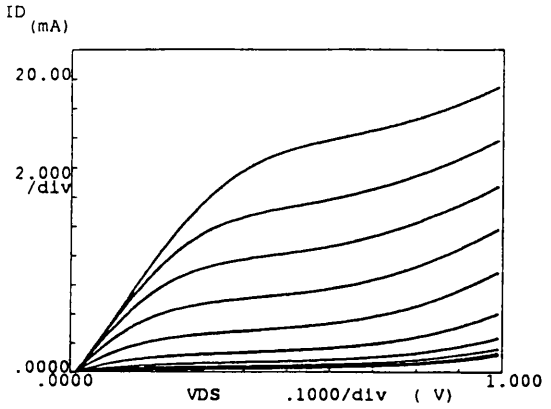

Figure 5.1.8(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 120nm Gate Length MB1 HFET (V_{gs} start, 0.75V, stop -1.5V, step -0.25V)

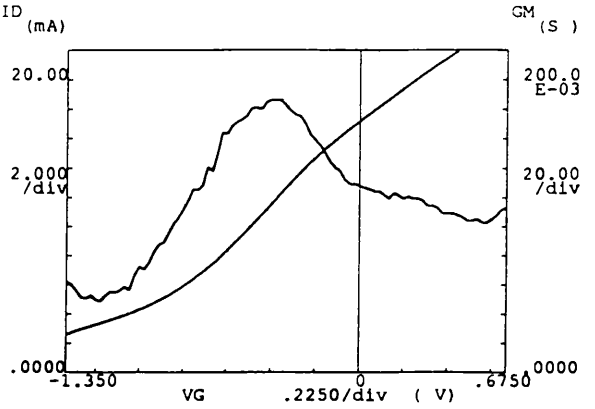

Figure 5.1.8(b) $g_m(V_{gs})$ Characteristic of 120nm Gate Length MB1 HFET (V_{ds} = 1.2V)

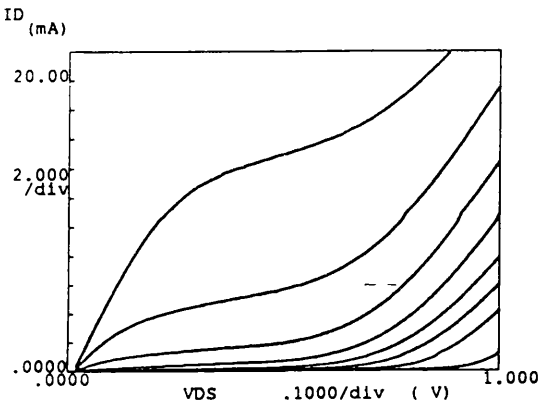

Figure 5.1.9(a) $I_{ds}(V_{ds},V_{gs})$ Characteristic of 80nm Gate Length MB1 HFET (V_{gs} start, 1.0V, stop -0.75V, step -0.25V)

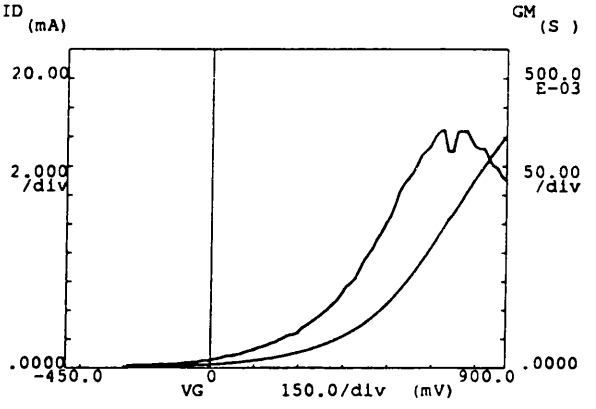

Figure 5.1.9(b) $g_m(V_{gs})$ Characteristic of 80nm Gate Length MB1 HFET (V_{ds} = 0.5V)

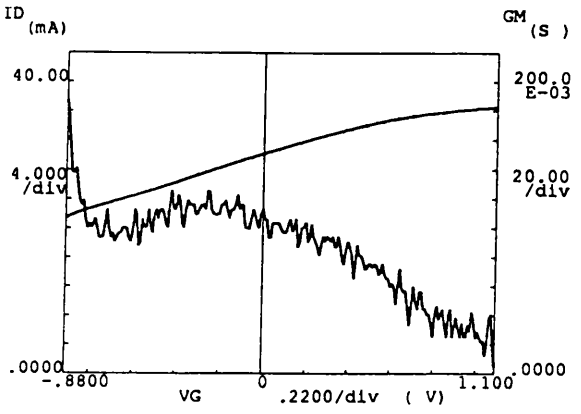

Figure 5.1.10 $g_m(V_{gs})$ Characteristic of 80nm Gate Length MB1 HFET sweeping Vgs -1V to 1.2V

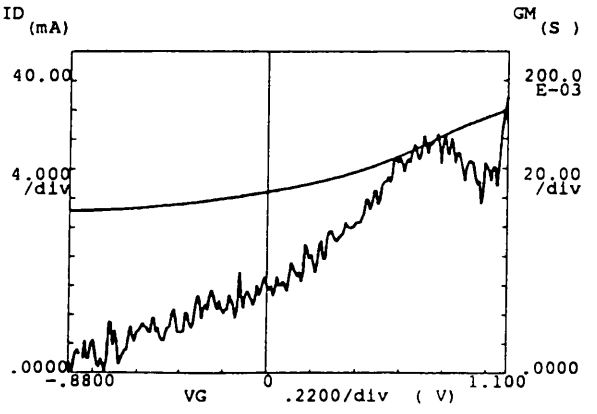

Figure 5.1.11 $g_m(V_{gs})$ Characteristic of 80nm Gate Length MB1 HFET sweeping Vgs 1.2V to -1V

A comparison of the DC properties of devices fabricated on the AlGaAs/GaAs (A322) and AlGaAs/InGaAs/GaAs (TF141) layers can be performed, however. Table 5.1.1 summarises the DC characteristics obtained from devices of the three different gate lengths fabricated on A322 and TF141.

Layer	A322			TF141		
Gate Length (nm)	g_{mmax} (mS/mm)	V_{span} (V)	R_{out} (Ω)	g_{mmax} (mS/mm)	V_{span} (V)	R_{out} (Ω)
200	260	0.5	850	500	0.7	400
120	230	0.6	650	600	0.7	350
80	190	0.8	450	470	1.3	150

Table 5.1.1 - DC Characteristics of Devices Fabricated on A322 and TF141

Each of the quantities in Table 5.1.1 will now be discussed in detail.

5.1.1 DC Transconductance, g_{mmax}

The transconductance values shown in Table 5.1.1 are extrinsic and were obtained by biasing the devices to obtain maximum transconductance. Using the contact resistance and sheet resistance values obtained from the TLM Process Control Monitors (Section 4.8.3), Equation (2.3.6) can be used to calculate the maximum intrinsic transconductance. Table 5.1.2 compares extrinsic and intrinsic values.

Layer	A322		TF141	
R_c (Ωmm)	0.46		0.05	
R_{sh} (Ω/sq)	775		250	
R_s (Ω)	9.6		1.9	
Gate Length (nm)	$g^{ext}_{m_{max}}$ (mS/mm)	$g^{int}_{m_{max}}$ (mS/mm)	$g^{ext}_{m_{max}}$ (mS/mm)	$g^{int}_{m_{max}}$ (mS/mm)
200	260	325	500	540
120	230	280	600	660
80	190	220	470	505

Table 5.1.2 - Maximum Extrinsic and Calculated Intrinsic Transconductance for A322 and TF141 HFETs

Devices fabricated on A322 suffer from large DC source resistance due to the high resistance of the ohmic contacts and the large sheet resistance of the material structure. The relatively small values of transconductance of the A322 devices result from the lower than expected AlGaAs donor layer doping concentration discussed in Section 3.3. Figure 5.1.12 shows a plot of maximum intrinsic transconductance against the gate voltage at which the maximum transconductance occurs for three A322 device chips.

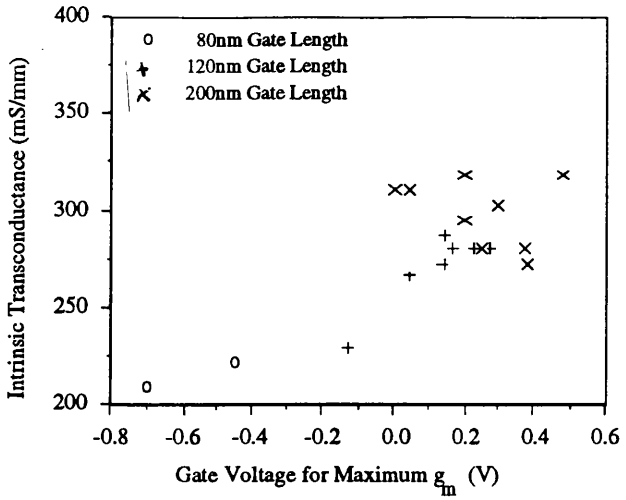

Figure 5.1.12 - Maximum Transconductance Dependence on Gate Voltage for Three A322 Device Chips

Devices of equal gate length were fabricated together on the same chip, and so have roughly the same gate recess depth. It is clear from Figure 5.1.12 that the recess depth is the dominant factor in determining the device transconductance, with the most deeply recessed devices (those whose maximum transconductance is obtained by forward biasing the gate) having the largest transconductance.

The DC data of devices fabricated on A322 shows no increase in device transconductance with decreasing gate length. There is thus no obvious evidence of velocity overshoot as the gate length is reduced in these devices, however it would be necessary to accurately determine the gate recess depth of the devices to calculate the effective carrier velocity from the intrinsic transconductance values. Due to their small size (40μm wide active region), it was impossible to cleave through the gate region of the devices to determine the gate recess depth by SEM examination.

The δ doped structure of TF141 allows the gate to be placed closer to the 2DEG than in A322, resulting in intrinsic transconductances of up to 660mS/mm. As with A322 devices, the maximum intrinsic transconductance is determined by the gate recess depth as shown in Figure 5.1.13.

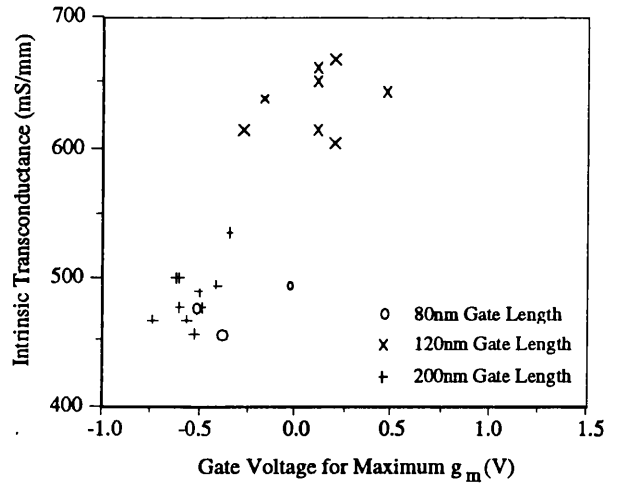

Figure 5.1.13 - Maximum Transconductance Dependence on Gate Voltage for Three TF141 Device Chips

As before, devices of the same gate length have similar transconductance as the devices on each chip are recess etched to roughly the same depth.

5.1.2 Output Resistance and Voltage Span

To study the effect of reducing the gate length on DC device performance, two figures of merit

i) the device output resistance (R_{out})

ii) the gate voltage span (V_{span})

are shown in Table 5.1.1.

V_{span} is defined as the difference between the gate voltage for maximum transconductance and the gate voltage needed to reduce the drain source current to 100μA. The gate voltage span, which is a measure of the threshold voltage shift, is used as other measures of threshold voltage shift such as extrapolation of the $I_{ds}(V_{gs})$, $I_{ds}^{1/2}(V_{gs})$, or $\log(I_{ds})(V_{gs})$ plots are all heavily gate recess depth dependant.

The output resistance and voltage span data of Table 5.1.1 are reproduced in Figures 5.1.14 and 5.1.15.

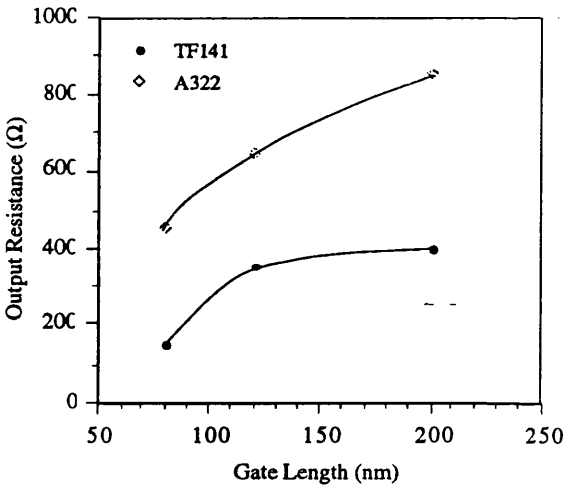

Figure 5.1.14 - Output Resistance as a Function of Gate length for A322 and TF141 Devices

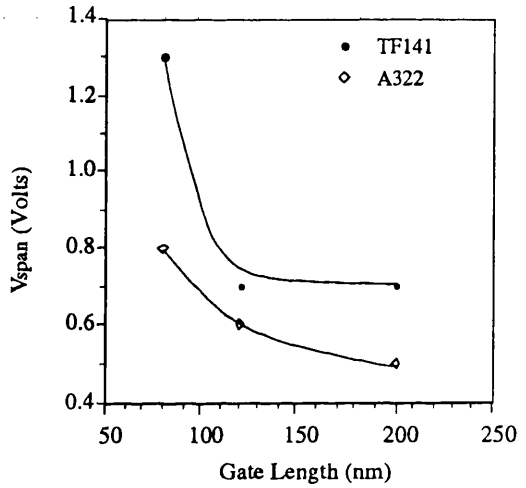

Figure 5.1.15 - V_{span} as a Function of Gate length for A322 and TF141 Devices

As the gate length is reduced, the output resistance of TF141 and A322 devices decreases indicating a reduction in electron confinement to the 2DEG channel. The degradation is more significant for the TF141 devices. Similarly, the gate voltage span in the TF141 devices is greater than in the A322 devices at each gate length, and increases rapidly as the gate length is reduced below 120nm, again indicating poorer confinement in the TF141 devices. This reduction in carrier confinement can be correlated with the potential barrier at the conduction band offset below the quantum well in the two layer structures. This barrier is 0.20eV for A322 and 0.11eV for TF141. Thus for devices with gate lengths in the range 200-80nm, increasing the potential barrier below the quantum well channel of the layer structure increases carrier confinement and reduces output resistance and threshold voltage shift. This effect will be shown to hold for RF output resistance in Section 5.6.1.

5.2 RF Device Characterisation

The RF measurement system is shown schematically in Figure 5.2.1.

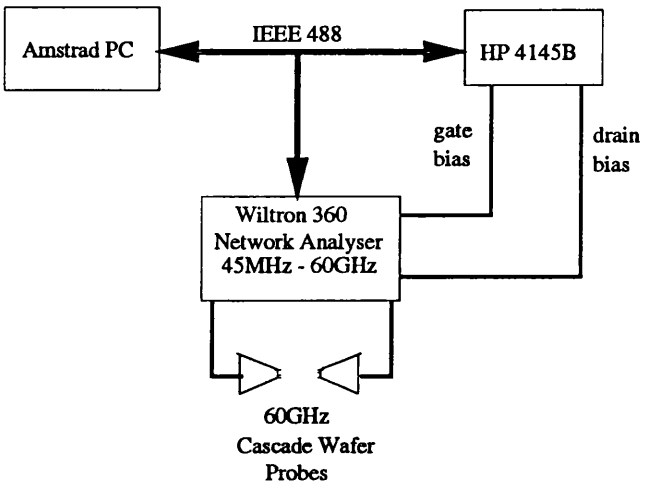

Figure 5.2.1 - RF Measurement System

The Wiltron 360 Network Analyser, configured to measure from 45MHz to 60GHz, is under the control of the PC via an IEEE-488 interface. In addition, the PC controls the gate and drain biases applied to the device by the HP4145B through the Wiltron test set and a pair of Cascade on-wafer probes. The probes, semi-rigid connecting cables and all relevant connectors are suitable for the propagation of microwave signals up to 60GHz. When operating, the PC instructs the HP4145B to set the bias condition, controls the measurement of device S-parameters by the Wiltron Network Analyser and receives the measured S-parameters via the IEEE-488 interface. The S-parameters are then converted to a format suitable for use in Touchstone and also to display figures of merit such as device f_T, Maximum Available Gain (MAG) and y_{21} (the RF device transconductance).

Calibration of the Network Analyser was performed using the Short-Open-Load-Thru (SOLT) technique with the calibration standards fabricated on SI GaAs substrates. A power level of 0dBm was applied at the input and output ports for all measurements, with 250x averaging used for the calibration and 10x averaging for device measurement.

Typical S-parameter results obtained on a THRU line after calibration were :

S_{11} and S_{22} < -40dB from 45MHz to 60GHz

S_{12} and S_{21} < 0.2dB ripple around 0dB from 45MHz to 60GHz

Initially, a calibration standard chip with a continuous groundplane similar to that of the device chips was used. The continuous groundplane was used in an attempt to improve the quality of the measured S-parameters (particularly S_{12}, which is very small for the short gate length devices fabricated (short gate length and small device width)). However, significant losses in the device S-parameters were observed, and in an effort to explain the losses, a calibration chip with a discontinuous groundplane was fabricated and used to perform device calibration.

Having performed an SOLT calibration using the discontinuous groundplane calibration chip, a Short Circuit calibration standard was measured on it. The magnitude of S_{11} and S_{22} obtained from the Short are shown in Figure 5.2.1. As expected, the reflected S-parameters show a magnitude of close to 0dB

from 0-60GHz with the measurement quality degrading at the higher frequencies as the cables, connectors and probe heads reach their operating limit.

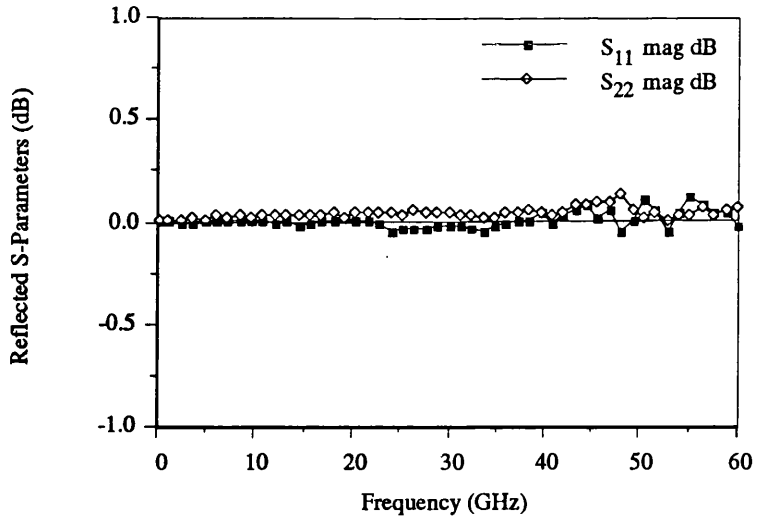

Figure 5.2.2 - S_{11} and S_{22} from Short Calibration Standard with Discontinuous Groundplane (calibration Performed using Discontinuous Groundplane Standards)

Next, using the same calibration, S_{11} and S_{22} of a Short on the continuous groundplane calibration chip was measured (Figure 5.2.3). Whilst the measurement quality is slightly poorer, S_{11} is still within 0.2dB of the expected 0dB over the entire frequency range. However, in the frequency range 20-40GHz, S_{22} shows losses down to -0.5dB.

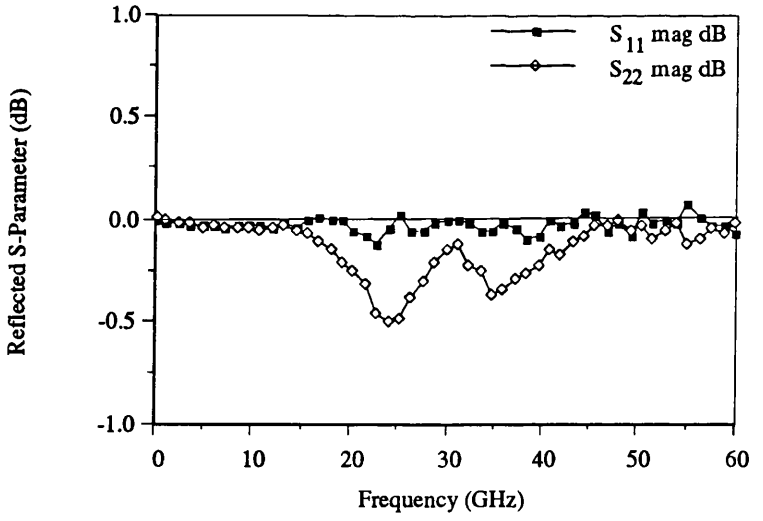

Figure 5.2.3 - S_{11} and S_{22} from a Short Standard on the Continuous Groundplane Chip Measured using Calibration Performed with Discontinuous Groundplane Calibration Chip

In an effort to determine if the observed losses were due to the output side of the measurement system, the continuous groundplane chip was rotated through 180° and the S-parameters remeasured. Figure 5.2.4 shows S_{11} and S_{22} measured on the rotated chip. Whilst the measurement quality is poorer because of small asymmetries in the Short calibration standard under rotation, the losses now appear in

S_{11} indicating that they result from the groundplane geometry rather than one side of the measurement system (probe head, connectors, cables, test set).

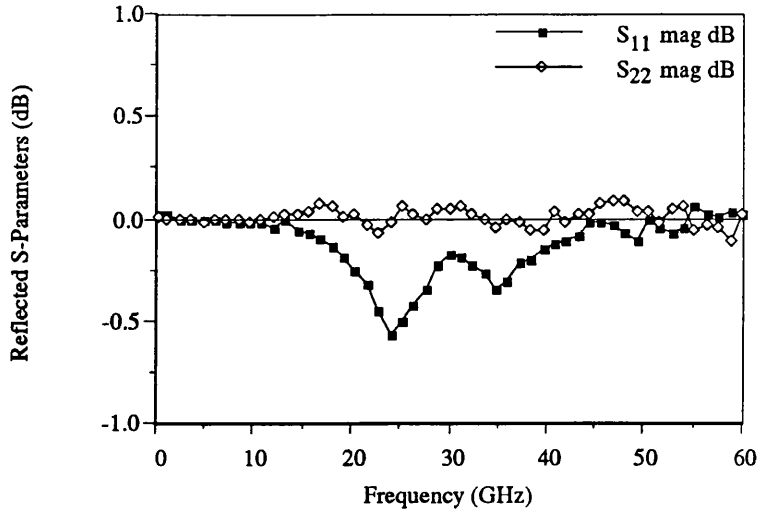

Figure 5.2.4 - S_{11} and S_{22} from rotated Short Standard on Continuous Groundplane Chip measured using Calibration Performed with Discontinuous Groundplane Calibration Chip

A possible explanation of the above is that the continuous groundplane layout supports non-coplanar waveguide modes of microwave propagation, and the geometry of the drain side of the devices allows microwave energy to be coupled from the probe heads into these modes. Because the modes are non-coplanar, energy cannot be coupled back into the probe heads at either the output or the input sides. It is not possible to calibrate out these coupling losses using either the continuous or discontinuous groundplane calibration structures but using the latter, the losses are reduced. That the coupling loss is observed only at the output side of this particular device layout structure (despite that fact that the output and input pad configurations are virtually identical) suggests the particular layout chosen will barely support the mode propagation causing the observed losses. To overcome this problem in future, both HFET devices and calibration standards should be fabricated with a discontinuous groundplane structure.

Typical S-parameters measured on a 120nm gate length TF141 device after calibration using the discontinuous groundplane calibration chip are shown in Figures 5.2.5-5.2.8 All S-parameters are perturbed by the losses described above, with S_{12} most affected. Whilst slightly compromising the quality of the measured device S-parameters, the losses do not seriously affect any subsequent analysis performed on the device S-parameters.

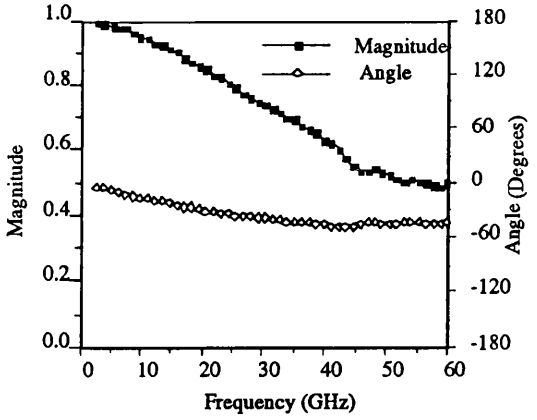

Figure 5.2.5 - Magnitude and Angle of S_{11}

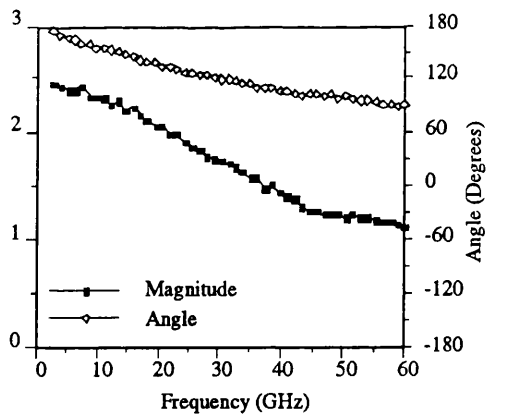

Figure 5.2.6 - S_{21} Magnitude and Angle

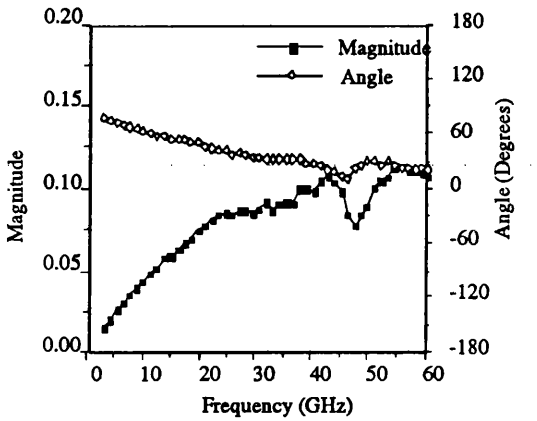

Figure 5.2.7 - S_{12} Magnitude and Angle

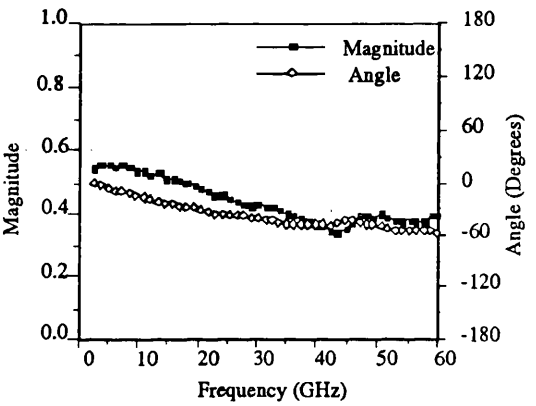

Figure 5.2.8 - S_{22} Magnitude and Angle

5.3 Comparison of DC and RF Transconductance

The device RF transconductance y_{21}, can be evaluated by converting from S-parameters to Y-parameters using well known formulae[5.1]. The DC and RF transconductances for devices of each gate length on each material structure are shown in Table 5.3.1.

	DC Transconductance (mS/mm)			RF Transconductance (mS/mm)		
Gate Length (nm)	A322	TF141	MB1	A322	TF141	MB1
200nm	255	510	200	220	460	500
120nm	235	610	200	215	560	550
80nm	200	460	450	150	400	1100

Table 5.3.1 - Comparison Between DC and RF Transconductance for Devices of Different Gate lengths on the Three Material Structures

The devices fabricated on both A322 and TF141 have RF transconductances smaller than the DC values because a new value of drain current cannot be fully established until the gate capacitance has been charged by changing the gate voltage.

This results in a frequency dependent transconductance of the form $g_m(f) = g_{mDC} \exp(-j\, 2\pi f \tau_{gm})$, where τ_{gm} is the charging delay. In contrast, the devices fabricated on MB1 exhibit larger RF than DC transconductances. This phenomenon has been attributed to the presence of traps in the material[5.2] (The probability of trap depopulation can be increased by the application of an electric field. When charge is depleted from the 2DEG by reverse biasing the gate of a device, trapped charge can be freed to contribute to the drain current, resulting in a decrease in the device transconductance). At DC and low frequencies, the traps can respond to the gate modulation, reducing the device transconductance, whilst at high frequency (>10MHz) the trap capture and emission rate is smaller than the frequency of the applied gate modulation, and so the traps are unable to respond to the input signal.

RF extrinsic transconductances of up to 1100mS/mm were obtained from 80nm gate length devices fabricated on MB1.

From experience gained during the gate recess and metallisation process, the gate metallisation of working devices fabricated on MB1 must be deposited on the undoped $In_{0.52}AlAs$ Schottky layer of the structure (Deposition of the gate on either the doped $In_{0.53}GaAs$ cap or $In_{0.52}AlAs$ donor layers gives a poor Schottky gate contact with large gate leakage currents - too large in fact for the gate to act as a Schottky contact at all) As stated in Section 2.1.1, the 2DEG is located around 50Å below the heterojunction interface. Combining the above facts with the layer structure of MB1, it can be concluded that the minimum gate/2DEG separation in working MB1 devices is 250Å.

For extrinsic transconductances of 1100mS/mm, and a gate/2DEG separation of 250Å, Equation (2.3.2) ($g_m = \varepsilon Z v_{eff} / h$) yields an effective velocity of $2.4 \times 10^5 ms^{-1}$. As discussed in Section 2.8.1, the static saturated electron velocity in InGaAs is around $0.7\text{-}1.0 \times 10^5 ms^{-1}$. The effective carrier velocity deduced from the RF transconductance data is around three times that of the static value, and is evidence of the existence of velocity overshoot in these devices.

5.4 Evaluation of Device f_T

Device f_T was evaluated by extrapolating a plot of h_{21} against frequency at 20dB/decade as shown in Figures 5.4.1-5.4.3. The drain and gate biases were chosen to maximise the device f_T. The extrapolation was performed from data in the 10-20GHz frequency range, as the measured S-parameters were not compromised by either the quality of measurement at these frequencies or the losses described in Section 5.2.

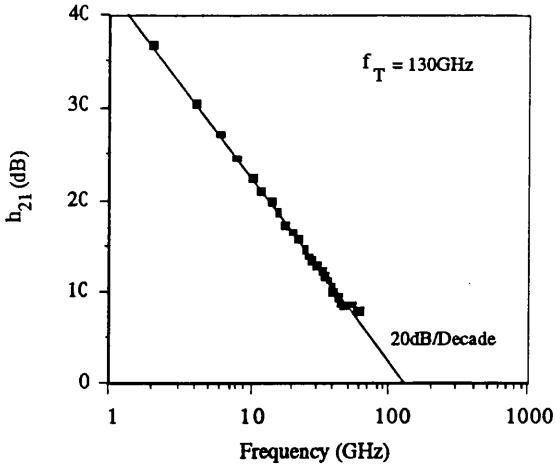

Figure 5.4.1 - h_{21} vs Frequency of 120nm Pyramidal Gate TF141 Device

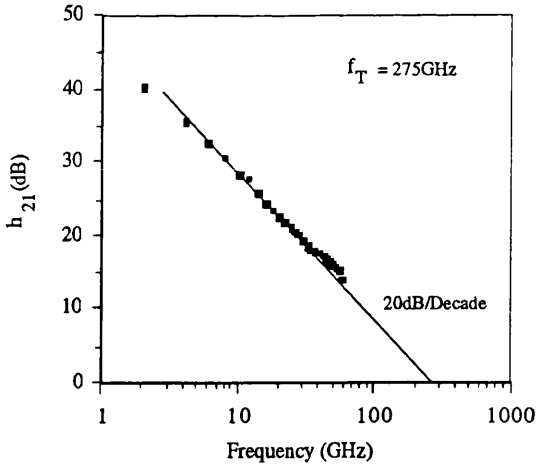

Figure 5.4.2 - h_{21} vs Frequency of 80nm Pyramidal Gate MB1 Device

Figure 5.4.1 was obtained from a 120nm pyramidal gate InGaAs/GaAs HFET with an f_T of 130GHz while Figure 5.4.2 shows the h_{21}(frequency) plot for an 80nm pyramidal gate InGaAs/InAlAs/InP HFET with an f_T of 275GHz.

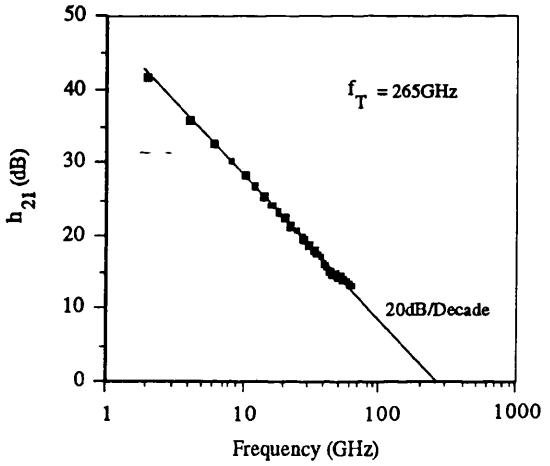

Figure 5.4.3 - h_{21} vs Frequency of sub-100nm T-Gate MB1 Device

Figure 5.4.3 was obtained from a sub-100nm T-gate InGaAs/InAlAs/InP HFET with an f_T of 265GHz. Whilst not physically measured, comparison with the f_T of 80nm pyramidal gate devices would indicate the footprint of the sub-100nm T-gate device fabricated to be in the range 80 - 90nm.

f_T's were extrapolated for devices fabricated on each material structure for each of the three gate lengths. Figure 5.4.4 shows a graph of f_T against inverse gate length for each of the 3 materials studied.

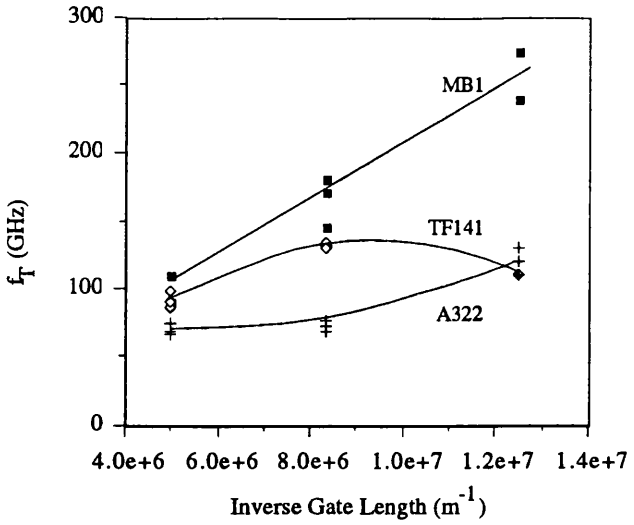

Figure 5.4.4 - f_T against Inverse Gate Length for Devices Fabricated on A322, TF141 and MB1

Equation (2.6.3) ($f_T = \frac{v_{eff}}{2\pi L_{eff}}$) suggests a linear relationship should exist between the device f_T and the inverse gate length if the gate capacitance scales with gate length. This can be seen to hold for the MB1 devices but not for A322 and TF141 devices.

For the MB1 devices, the linear relationship between f_T and inverse gate length suggests the devices are well scaled, even at the shortest gatelengths. The layer structure of MB1 allows the gate to be placed close to the 2DEG (around 250Å gate/2DEG separation) and as the donor layer is highly doped, the extension of the gate depletion region into the gate drain region of the device is small, so that the effective gate length is similar to the metallurgical gate length.

For the A322 devices, the non-linear dependence of f_T on inverse gate length results from poor scaling of the gate capacitance. Using the DC intrinsic transconductance data together with Equation (2.3.2) ($g_m = \varepsilon Z v_{eff} / h$) and an effective carrier velocity of $1.0 \times 10^5 ms^{-1}$, gate/2DEG separations of around 350Å for the 200nm gate length devices, 400Å for the 120nm gate length devices, and 500Å for the 80nm were calculated. These devices do not meet the L/h = 3 criterion for gate lengths below 120nm, and is a result of the lower than expected AlGaAs donor layer doping level.

Solving Equation (2.3.2) ($g_m = \varepsilon Z v_{eff} / h$) with an effective velocity of $1.0 \times 10^5 ms^{-1}$ and the DC transconductance data of TF141 HFETs yield a gate/2DEG separation of around 200Å in these devices. This means the gate recess depth in TF141 devices is roughly 650Å. As the gate recessing technique employed an isotropic wet chemical etch, it was expected that the recess trench width W, would be significantly larger than the metallurgical gate length L_g as shown schematically in Figure 5.4.5.

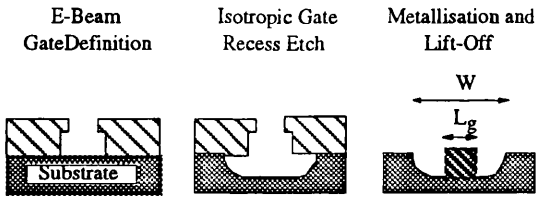

Figure 5.4.5 - A Deeply Recessed Gate has a Recess Trench Significantly Greater than the Metallurgical Gate Length

This hypothesis was confirmed by performing an SEM examination of the gate recess area of the TF141 devices. Table 5.4.1 shows the metallurgical gate length and the recess trench width for each gate length.

Gate Length (nm)	Recess Trench Width (nm)
200	300
120	320
80	350

Table 5.4.1 - Gate Length and Recess Trench Width for TF141 Devices

As described in Section 2.7, a HFET device with a large recess trench compared to the metallurgical gate length is analogous to an unrecessed device, where the presence of surface states increases the effective gate length as seen by electrons in the device channel.

In terms of the device equivalent circuit, these effects means the total gate capacitance does not scale with gate length, even although the gate/2DEG separation obeys the simple L / h = 3 requirement. Consequently the device f_T does not increase linearly with decreasing gate length.

Equation (2.6.3) ($f_T = \frac{v_{eff}}{2\pi L_{eff}}$) suggests the effective channel carrier velocity can be deduced from the device f_T and the effective gate length. Figure 5.4.6 is a plot of effective carrier velocity in the channel, calculated from the f_T, assuming the effective gate length of the device is the metallurgical gate length measured using an SEM. This will underestimate the carrier velocity since no account is taken of the extension of the depletion region on the drain side of the gate which increases the effective gate length seen by electrons in the device channel. This gate length extension into the drain region of the device will be discussed in Section 5.6.2, as it can be inferred from the value of C_{gd}, the gate-drain capacitance which can be obtained from the equivalent circuit extraction package, Touchstone.

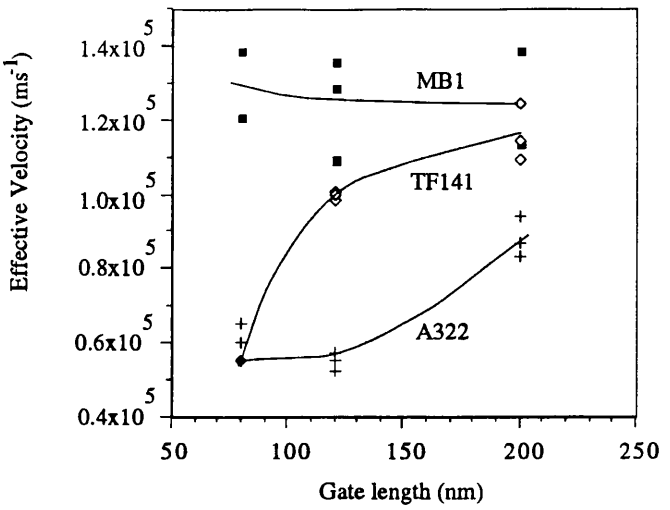

Figure 5.4.6 - Effective Velocity Extracted from Measured f_T as a Function of Gate Length for Devices Fabricated on all Three Material Structures

When derived from the device f_T, the effective velocity of the MB1 devices is largely independent of gate length and suggests the devices are well scaled even at the shortest gate lengths as discussed above. The effective velocity has a minimum value of around 1.2-1.3x10^{5}ms^{-1}, above the saturated electron velocity of 0.7-1.0x10^{5}ms^{-1} observed in both measurement[5.3] and Monte Carlo simulation[5.4] of the transport properties of InGaAs/InP structures. This result supports the observation of overshoot in the electron velocity in the channel of 80nm gate length HFETs fabricated on the MB1 layer as described in Section 5.3. The value of effective velocity obtained from the f_T analysis is smaller than from the y_{21} data as the metallurgical gate length, rather than the effective gate length, was used in the calculation.

Referring again to Figure 5.4.6, it can be seen that for the devices fabricated on both A322 and TF141, the effective velocity evaluated using this analysis falls as the gate length is reduced for the reasons outlined above. It is not that the effective velocity of carriers in the channel is actually reducing with gate length, rather that the value of carrier velocity extracted from a measurement of the device f_T is smaller because the gate capacitance does not scale with gate length.

In an attempt to correlate material transport properties with HFET RF performance, the 200nm gate length device f_T and material transport properties of all three material structures were collected (Table 5.4.2). The effective carrier velocity data was calculated using $f_T = v_{eff} / 2 \pi L_g$

Material	f_T (GHz)	Ids (mA)	n_{sh} (cm^{-2})	μ (cm^2/Vs)	v_{eff} (ms^{-1})
A322	75	7	9.9x10^{11}	7200	0.9x10^5
TF141	90	15	1.4x10^{12}	6600	1.2x10^5
MB1	110	12	3.8x10^{12}	9200	1.4x10^5

Table 5.4.2 - 200nm Gate Length Device f_T and Material Transport Properties of all Three Material Structures

By comparing the results for the A322 and TF141 devices, it is obvious that the 2DEG mobility plays no role in limiting the device f_T for the material structures of this study. In addition, 200nm gate length MESFET's have been fabricated in the Nanoelectronics Group at the University of Glasgow as part of an

ESPRIT collaboration[5.5]. These devices were fabricated on bulk doped $5x10^{17}cm^{-3}$ GaAs with a mobility of around $3000cm^2/Vs$ and have an f_T of 70GHz.

From the extracted effective velocity (which is a lower limit), and the measured drain current at the bias condition for maximum device f_T, it is possible to determine an upper limit to the carrier concentration in the channel of the HFETs using $I_{ds} = q\, v_{eff}\, n_s\, Z$, as shown in Table 5.4.3 below :

Material	$n_{sh\ channel}$ (cm^{-2})
A322	$6.1x10^{11}$
TF141	$9.8x10^{11}$
MB1	$6.7x10^{11}$

Table 5.4.3 - Calculated Maximum Channel Electron Concentration

Although the 2DEG in each of the materials has the capability of supporting the carrier concentration shown in Table 5.4.2, due to non-ideal gate recessing the fabricated HFETs have the channel electron concentrations shown in Table 5.4.3. By considering Tables 5.4.2 and 5.4.3 it is clear that the channel electron concentration is not the parameter which limits the device f_T. For the materials studied in this project, it can be concluded that the effective velocity is the dominant transport property in determining device f_T.

5.5 Touchstone Equivalent Circuit Analysis

To generate RF equivalent circuits of the HFETs, the measured S-parameters were analysed using the Touchstone software package. S-parameter data up to 40GHz was fitted to the standard FET equivalent circuit shown in Figure 5.5.1 for devices of each gate length on each material structure.

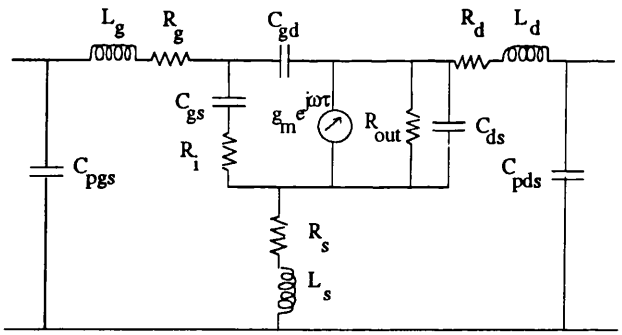

Figure 5.5.1 - HFET Equivalent Circuit used to Fit S-parameter Data

The strategy adopted when fitting the measured S-parameters to the equivalent circuit model was to provide the model with initial estimates of as many of the circuit elements as possible, thus minimising the chance of arriving at a physically meaningless solution.

First estimates of R_{out}, C_{gd}, g_m, C_{gs} and Rg were obtained as follows :

i) The output resistance was calculated from 45MHz S_{22} data.

ii) A first estimate of Cgd was obtained by fitting S12 by eye.

iii) g_m was set equal to y_{21}, calculated from the S-parameters at 1GHz

iv) Cgs was approximated using the expression $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

v) Having determined an initial value for C_{gs}, R_g was estimated from S_{11} and the frequency dependence of the Maximum Available Gain

vi) Drain, source and gate inductances were given initial values of 1pH

vii) Parasitic pad capacitances were first set to 1fF

Initially, all parameters were allowed to vary whilst a least squares fit was performed. When the error function reduced to less than 1%, a Quasi-Newton approximation was used until the minimum error function was found. Typically, fits of better than 0.5% were achieved.

Figures 5.5.2-5.5.9 show measured and fitted S-parameter magnitude and phase angle as a function of frequency for a 120nm device fabricated on TF141.

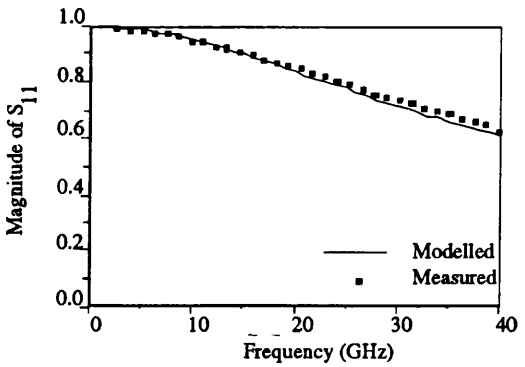

Figure 5.5.2 - Modelled and Measured Magnitude of S_{11}

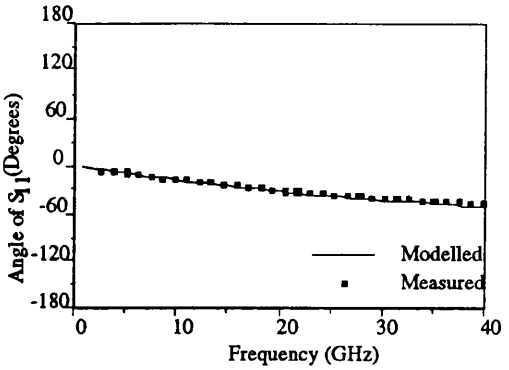

Figure 5.5.3 - Modelled and Measured Angle of S_{11}

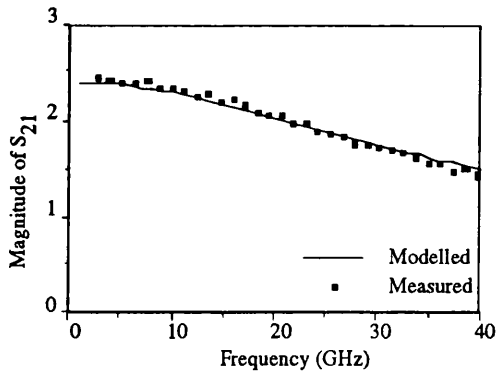

Figure 5.5.4 - Modelled and Measured Magnitude of S_{21}

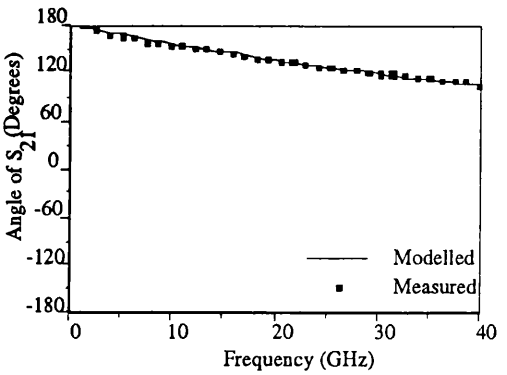

Figure 5.5.5 - Modelled and Measured Angle of S_{21}

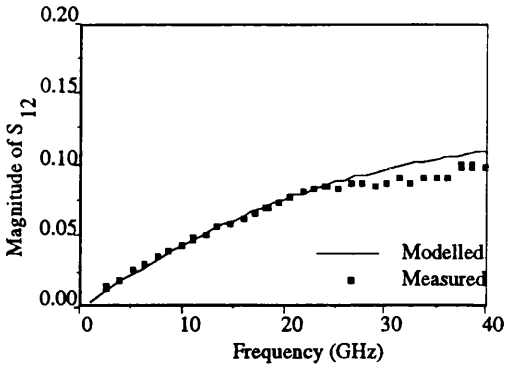

Figure 5.5.6 - Modelled and Measured Magnitude of S_{12}

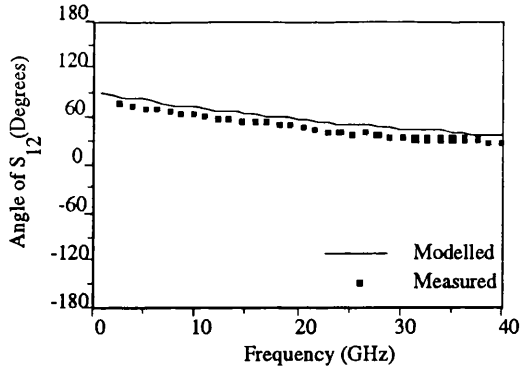

Figure 5.5.7 - Modelled and Measured Angle of S_{12}

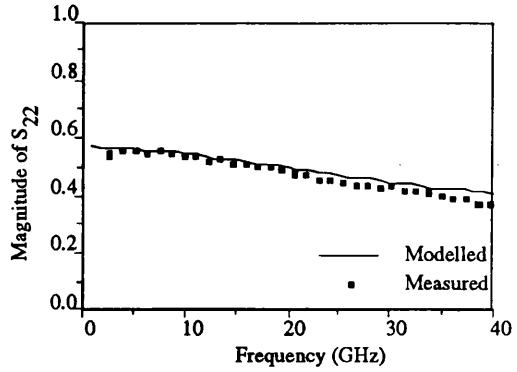

Figure 5.5.8 - Modelled and Measured Magnitude of S_{22}

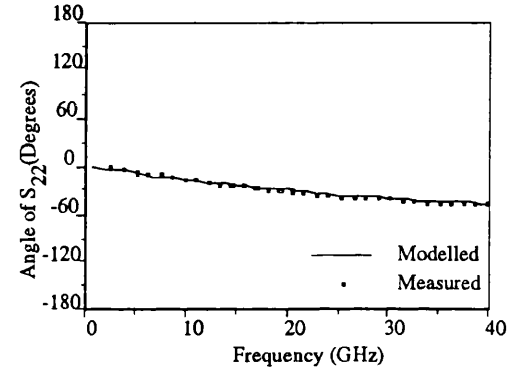

Figure 5.5.9 - Modelled and Measured Angle of S_{22}

The resulting equivalent circuit is shown in Figure 5.5.10.

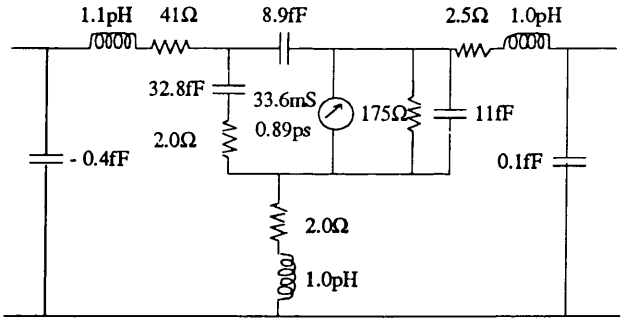

Figure 5.5.10 - Equivalent Circuit derived from Touchstone Modelling of 120nm TF141 Device

The main aims of the Touchstone modelling were to extract the circuit elements required to calculate the maximum frequency of oscillation (f_{max}) of the devices, and also to look for material and/or gate length dependence of the equivalent circuit elements.

5.6 Comparison of Elements of the Device Equivalent Circuit

5.6.1 Output Resistance

In Section 5.1.2, device DC output resistance was correlated with the potential barrier at the conduction band offset in the quantum well below the 2DEG. Figure 5.6.1 shows the gate length and material dependence of the RF output resistance and shows clearly the advantage of the extra carrier confinement achieved by using the 0.2eV AlGaAs confining back barrier in A322.

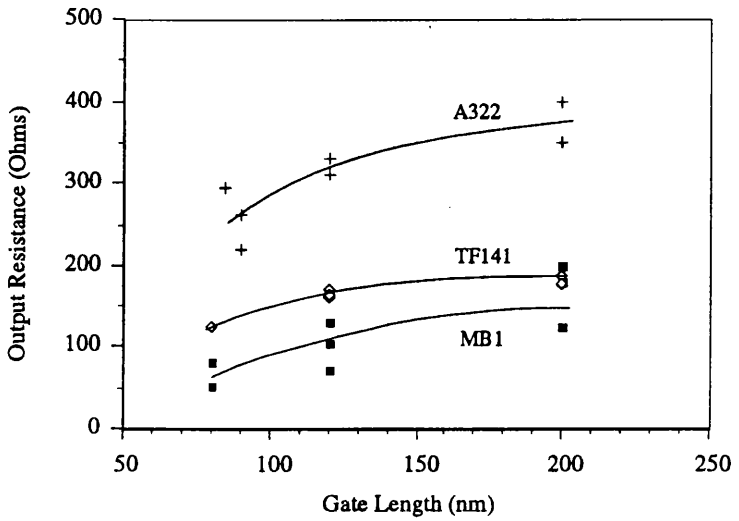

Figure 5.6.1 - Output Resistance of Devices Fabricated on A322, TF141 and MB1

This result further corroborates the data presented in Section 5.1.2 and allows a comparison with the properties of devices fabricated on MB1.

A potential barrier of 0.1eV exists 150Å below the 2DEG in MB1. A further barrier of 0.5eV is also present 500Å below the 2DEG. The extracted values of R_{out} indicate the 0.1eV barrier below the 2DEG in MB1 determines the device output resistance. It is also interesting to note that the potential barrier between the 2DEG channel and the undoped spacer layer above the channel is smallest for A322 and largest for MB1. This shows that carrier transfer from the 2DEG to the donor layer above the channel is not a significant mechanism in determining device output resistance for the materials and gate lengths of this study.

5.6.2 Gate Capacitance and Transconductance

As they are closely linked via the gate/2DEG separation, the extracted gate capacitances and transconductance are considered together.

Figures 5.6.2 shows C_{gs} and C_{gd} as a function of gate length for devices fabricated on A322.

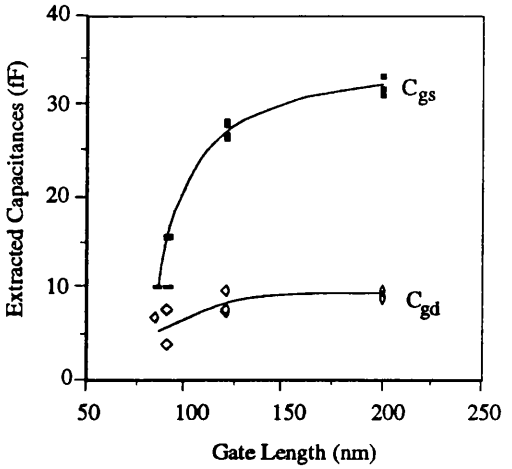

Figure 5.6.2 - Gate Source and Gate Drain Capacitances of A322 Devices as a Function of Gate Length

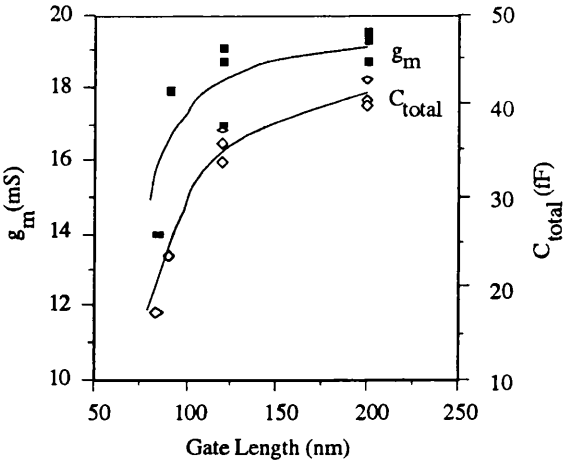

Figure 5.6.3 - Extracted Transconductance and Total Gate Capacitance of A322 Devices as a Function of Gate Length

On first inspection, C_{gs} appears to scale well with gate length, 80nm gate length devices having C_{gs} of around 10fF and the 200nm gate length devices a C_{gs} of 30fF. However, the gate recess-depth in the 80nm gate length devices is greater than the 200nm gate length devices. Figure 5.6.3 shows the transconductance and total gate capacitance (C_{gs} + C_{gd}) of the A322 devices. The transconductance of the 80nm gate length devices is smaller than the 120nm and 200nm devices as the gate/2DEG separation of the 80nm devices is larger. As both the gate-recess depth and the gate length are varying in the devices, it is difficult to make any direct comparisons of the transconductance and capacitance values of the various devices.

The 120nm gate length A322 devices have unusually large values of C_{gs} for reasons which are not understood. This results in the strange f_T/inverse gate length dependence of the A322 devices shown in Figure 5.4.4.

C_{gd} is nearly constant over the entire gate length range, and for the shortest gate lengths, C_{gs} and C_{gd} are almost equal. The contribution of C_{gd} to the total gate capacitance (C_{gs} + C_{gd}) causes the non-linear dependence of the f_T on gate length discussed in Section 5.4, and the resulting decrease in the extracted effective velocity as the gate length is reduced.

Figure 5.6.4 shows the gate length dependence of C_{gs} and C_{gd} for TF141 devices.

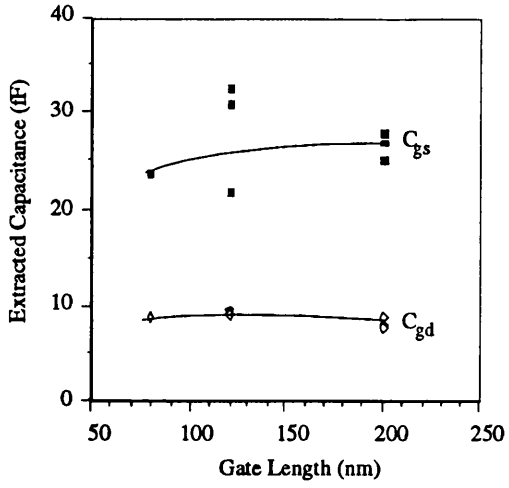

Figure 5.6.4 - Gate Source and Gate Drain Capacitances of TF141 Devices as a Function of Gate Length

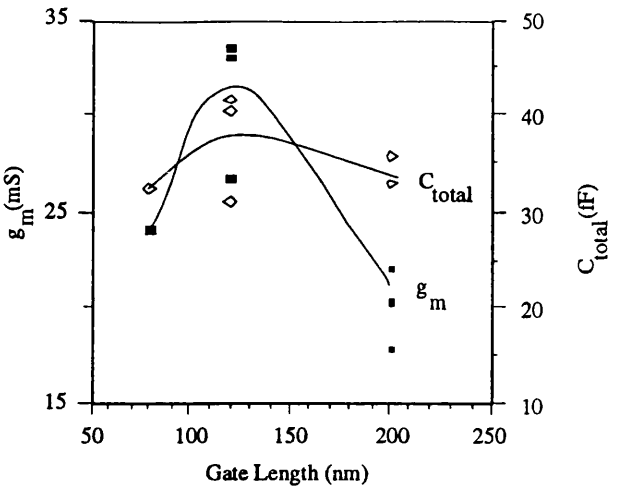

Figure 5.6.5 - Extracted Transconductance and Total Gate Capacitance of TF141 Devices as a Function of Gate Length

As for the A322 devices, C_{gd} is almost constant over the entire gate length range. In the 120nm gate length devices, C_{gs} is greater as these devices are more deeply recessed. Figure 5.6.5 shows the g_m of the 120nm gate length devices to be largest as the gate/2DEG separation is smallest in these devices. C_{gs} has only a small gate length dependence because the gate recess trench is much wider than the metallurgical gate length in these devices resulting in a large effective gate length but again, variations in the gate recess depth from device to device make analysis of the extracted capacitance and transconductance values difficult.

Figure 5.6.6 shows the gate length dependence of C_{gs} and C_{gd} for MB1 devices.

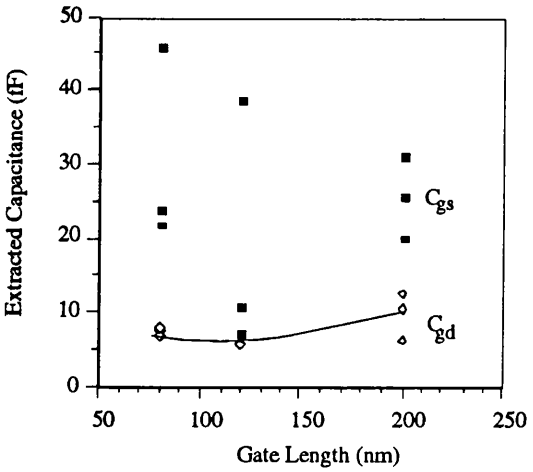

Figure 5.6.6 - Gate Source and Gate Drain Capacitances of MB1 Devices as a Function of Gate Length

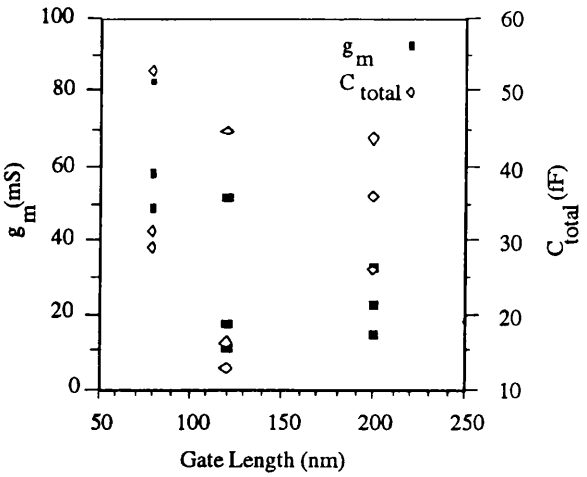

Figure 5.6.7 - Extracted Transconductance and Total Gate Capacitance of MB1 Devices as a Function of Gate Length

The large spread in C_{gs} values at each gate length reflects the lack of control in the gate recessing of these devices. It is possible that the gates of MB1 devices sit anywhere between 250Å and 500Å from

the 2DEG as the only criterion for stopping the gate recess etching was that the device did not breakdown catastrophically when the drain bias was applied.

A correspondingly large scatter in the extracted g_m values is also observed (Figure 5.6.7).

Equivalent circuit modelling has shown that C_{gd} contributes significantly to the total gate capacitance and so it is unreasonable to expect the total gate capacitance to scale with gate length. The values of effective carrier velocity extracted from the f_T data in Section 5.4 assume the gate capacitance scales with gate length and makes no correction for the extension of the gate depletion region at the drain end of the gate. It has been shown that the extension of the gate depletion region beyond the drain end of the gate, X, can be approximated from[5.6]

$$C_{gd} = \frac{2\varepsilon Z}{1 + \frac{2X}{L_g}}$$

where Z is the device width, L_g is the metallurgical gate length and C_{gd} is the gate-drain capacitance. Using this analysis, it is possible to estimate the effective gate length of the devices $L_{eff} = L_g + X$ and to use this value of L_{eff} together with the f_T data to extract the effective carrier velocity.

Based on this approximation, the effective electron velocity obtained from the gate length dependant f_T data can be recalculated (Figure 5.6.8).

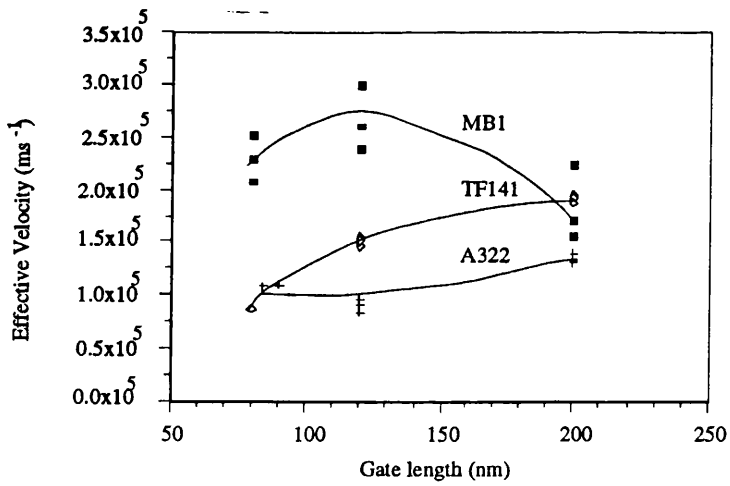

Figure 5.6.8 - Extracted Effective Channel Velocity of Devices on A322, TF141 and MB1 Including Extracted Gate Depletion Region Extension beyond the Drain end of the Gate

The recalculated effective velocity of A322 devices is around $1.0\text{-}1.2\text{x}10^5\text{ms}^{-1}$, independent of gate length. This is similar to the static saturation velocity of electrons in this material, and it can be concluded that the A322 devices show no velocity overshoot effects.

The effective velocity of the 200nm gate length TF141 devices is around $1.6\text{x}10^5\text{ms}^{-1}$. This value of velocity is greater than the static saturated electron velocity, and indicates that some velocity overshoot may be occurring in these devices. The extracted effective velocity still falls as the gate length is reduced because the gate source capacitance does not scale with gate length. The wide gate recess trench results in

an effective gate length larger than the metallurgical gate length even if depletion region extension beyond the drain end of the gate is accounted for.

The effective velocity extracted from the MB1 devices shows further evidence of significant velocity overshoot in these devices. Effective velocities of up to $3.0x10^5 ms^{-1}$ for 120nm gate length devices are extracted using this method. Even by correcting for gate length extension into the gate drain region, the extracted effective velocity falls as the gate length of the MB1 devices is reduced from 120nm to 80nm. This may result from a lack of scaling of the gate source capacitance with gate length. Even so, an average effective channel velocity of $2.2x10^5 ms^{-1}$ is extracted for the 80nm gate length devices.

To verify this analysis, the drain delay resulting from the depletion region extension at the drain end of the gate was extracted using the method described by Moll et al.[5.8].

In this analysis, the total delay $\tau_{tot} = 1/f_T$ is plotted as a function of gate and drain biases as shown in Figures 5.6.9 and 5.6.10 for a 200nm gate length TF141 device.

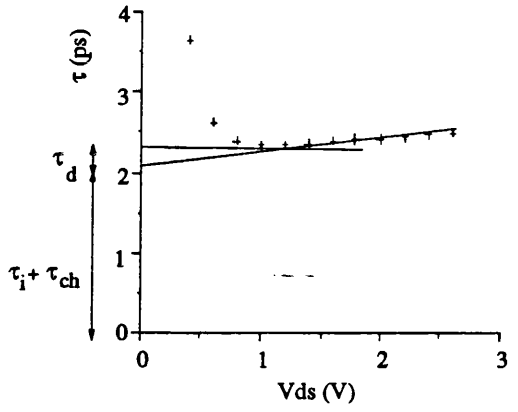

Figure 5.6.9 - Total Delay as a Function of Drain Bias for 200nm Gate Length TF141 Device

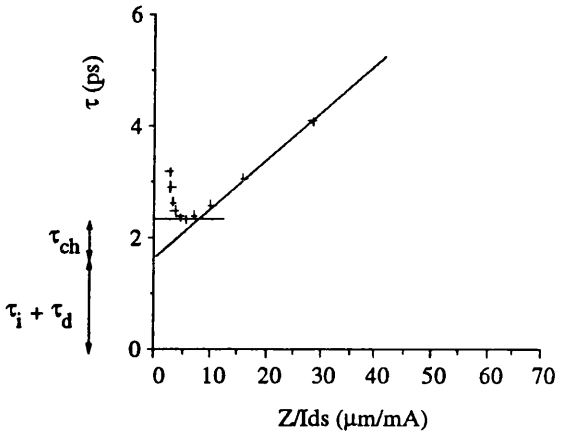

Figure 5.6.10 - Total Delay as a Function of Inverse Drain Current for 200nm Gate Length TF141 Device

The total delay is assumed to consist of three parts:

i) The intrinsic delay, τ_i associated with transport under the gate.

ii) The charging delay, τ_{ch} associated with charging the gate capacitance using the drain current.

iii) The drain delay, τ_d, associated with transiting the depletion region beyond the end of the gate.

In Figure 5.6.9, the total delay increases at drain biases greater than the maximum f_T bias condition. It is assumed that this results from increasing drain delay as the depletion region beyond the gate end of the drain is enlarged. At $V_{ds} = 0$, the drain depletion region extension is zero ie no drain delay, so extrapolation of the linear part of the total delay yields the sum of the charging and intrinsic delays. The difference between the total delay at the bias condition for maximum f_T and the extrapolated delay is the drain delay at maximum f_T.

In Figure 5.6.10, the total delay is plotted as a function of inverse drain current. At $1/I_{ds} = 0$, the current is infinite, so the charging delay is zero. The extrapolated delay is thus the sum of the drain and intrinsic delays. In this case, the difference between the total delay at maximum f_T and the extrapolated delay is the charging delay.

Having independently evaluated the drain and charging delays, the intrinsic delay can be deduced. As four measurements have been made to determine three unknowns, all the delay values can be checked for self-consistency.

From the drain bias plot,

$\tau_d = 0.2ps$ and $\tau_i + \tau_{ch} = 2.1ps$

From the inverse drain current plot,

$\tau_{ch} = 0.7ps$ and $\tau_i + \tau_d = 1.6ps$

This gives $\tau_i = 1.4ps$

Similar extractions were performed on devices at each gate length on all three material structures. The drain delays obtained are shown in Table 5.6.1

Gate Length (nm)	A322	TF141	MB1
200	0.2ps	0.2ps	0.4ps
120		0.2ps	
80	0.3ps	0.2ps	0.2ps

Table 5.6.1 - Drain Delay for each Gate Length on Each Material Structure

In some of the shorter gate length devices, it was impossible to extract self-consistent delays. This is probably because the analysis is 1-dimensional, an assumption which becomes less valid as the gate length is reduced. In addition, at the shortest gate lengths, the delays are so small that errors in the extrapolation significantly affect the delay values obtained.

However, the drain delay is in the range 0.2- 0.4ps for all devices.

If the drain delay is subtracted from the total delay, the effective velocity can be recalculated from the f_T data, as shown in Figure 5.6.11.

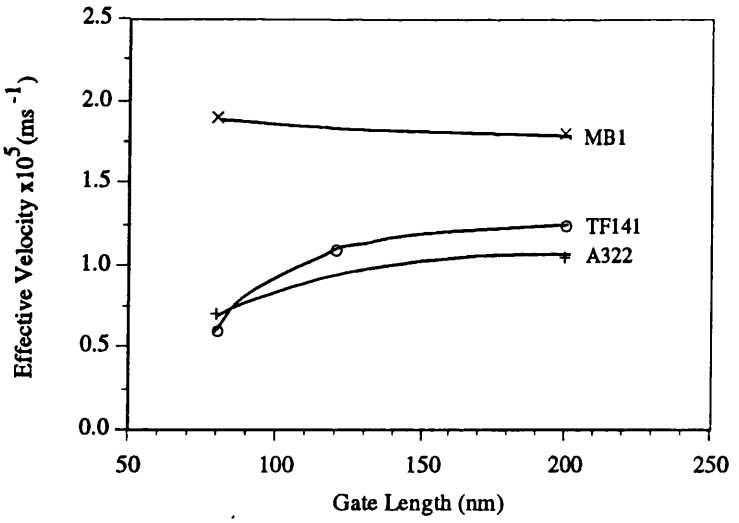

Figure 5.6.11 - Effective Channel Velocity calculated from Drain Delay Data

Using the drain delay data, the extracted effective velocities are smaller than when using the feedback capacitance technique. A322 devices have effective channel velocities up to $1.05x10^5$ ms^{-1}, TF141 devices up to $1.25x10^5$ ms^{-1}, and MB1 devices up to $1.95x10^5$ ms^{-1}.

The large difference between the extracted velocities obtained by the two methods reflects the difficulty in accurately determining the magnitude of the depletion region extension beyond the drain end of the gate. However, a number of qualitative conclusions can be drawn from the analyses.

There is no conclusive evidence for the existence of channel velocities in excess of the static saturated velocity in either the A322 or TF141 devices.

Both analyses however, indicate an enhancement of velocity in the MB1 devices over the static saturation velocity. This fact, taken together with the rf transconductance data from 80nm gate length MB1 devices indicate velocity overshoot is occurring in the shortest gate length MB1 devices. The analyses indicate the effective channel velocity for the 80nm gate length MB1 devices lies in the range 2.0 - $2.5x10^5$ ms^{-1}.

The reasons for the velocity overshoot are related to the large indium content in the channel layer. As discussed in Section 2.8.2, increasing the indium concentration decreases the electron effective mass whilst increasing the Γ-L valley energy separation. These phenomena increase the probability of the occurrence of velocity overshoot.

5.6.3 Gate Resistance

The extracted RF gate resistance for pyramidal gate and T-gate devices is shown in Figure 5.6.12. The T-gate structure significantly reduces the gate resistance. For comparison, the predicted RF gate resistance, calculated from the DC end to end gate resistance measured in Section 4.8.6.4 is presented in Table 5.6.2.

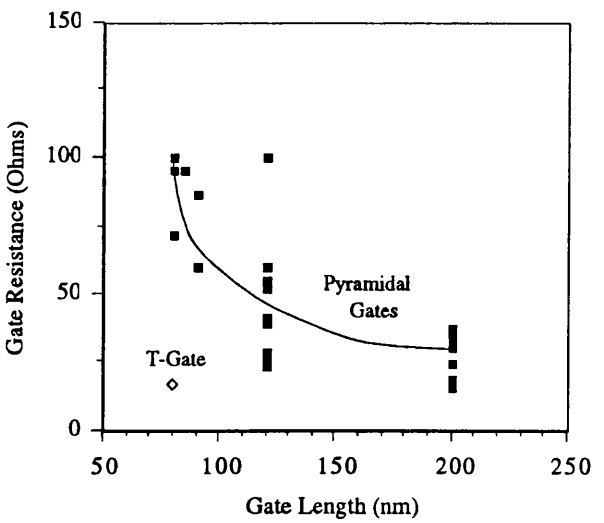

Figure 5.6.12 - Extracted Gate Resistance as a Function of Gate Length for Both Pyramidal and T-Gate Structures

Gate Length (nm)	Extracted R_g (Ω)	Predicted R_g (Ω)
200	24.8	5.6
120	47.1	11.7
80	87	33.3
T-Gate	16.5	4.7

Table 5.6.2 - Extracted and Predicted Gate Resistance based on 4 Terminal DC Gate Resistance Measurement

The large discrepancy between the predicted and extracted gate resistances is difficult to resolve. As shown in Figure 5.6.13, the gate resistance is composed of two parts:

i) the resistance of the gate on the mesa

ii) the resistance of the feed from the gate pad to the mesa

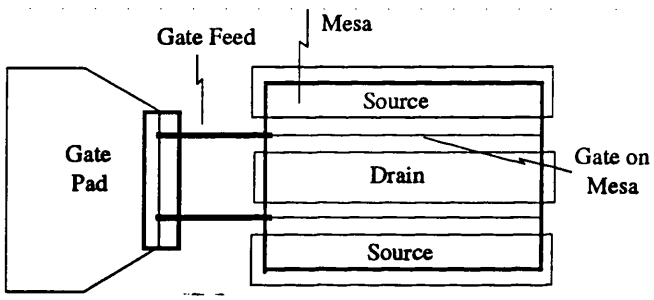

Figure 5.6.13 - Contributions to Gate Resistance

The predicted resistance values in Table 5.6.2 are calculated for the part of the gate on the mesa.
The feed is 200nm wide, and was used in 80nm and 120nm pyramidal gate devices to improve step coverage yield. The gate pad/mesa spacing is 5μm, so the feed should contribute roughly 5Ω to the predicted 120nm and 80nm gate length values. This still doesn't reconcile the extracted and predicted values. Closer inspection of Table 5.6.2 shows an almost linear relationship between the RF and DC gate resistances as a function of gate length. This can be written as $R_{gRF} = 2.4\ (R_{gDC} + 7.5)$ ie there is an extra contribution due to the feed (around 7.5Ω), but that the whole resistance is scaled when the gate resistance is evaluated at RF. The origin of such an effect is unclear, but if real, warrants further investigation as gate resistance dominates the Maximum Available Gain and f_{max} of short gate length HFET's.

5.7 Maximum Available Gain (or Maximum Stable Gain) and f_{max}

The device Maximum Available Gain (MAG) was calculated from the measured S-parameters using the equation[5.7]

$$MAG = \frac{S_{21}}{S_{12}}(K + \sqrt{K^2 - 1})$$

where

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|}$$

and

$$D = S_{11}S_{22} - S_{12}S_{21}$$

For K < 1, the device is only conditionally stable, ie matching with certain source and load impedances could result in device oscillation. For this condition, the Maximum Stable Gain (MSG) defined as

$$\left|\frac{S_{21}}{S_{12}}\right|$$

is evaluated. Figure 5.7.1 is a typical plot of gain against frequency for a 200nm gate length InGaAs/AlGaAs/GaAs device showing the region of conditional stability. The Touchstone modelled gain is also included in Figure 5.7.1 showing that the frequency range of conditional stability can be accurately modelled.

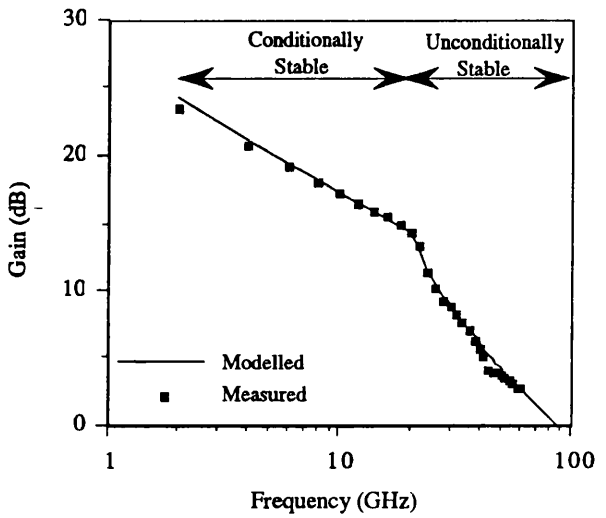

Figure 5.7.1 - Measured and Touchstone Modelled Maximum Available Gain as a Function of Frequency for 200nm Gate Length Pyramidal Gate TF141 Device

Figure 5.7.2 compares the gain of an 80nm pyramidal gate with an f_T of 275GHz and an 80nm footprint T-gate device with an f_T of 265GHz.

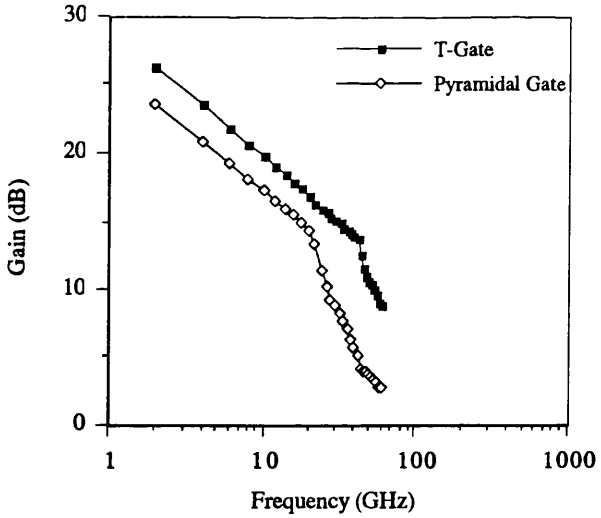

Figure 5.7.2 - Comparison of MAG for 80nm Pyramidal Gate MB1 Device and sub-100nm T-Gate MB1 Device

The gate resistance clearly has a significant influence on the device gain. At 60GHz, the pyramidal gate device has a MAG of 2.9dB, whilst the T-gate device has a MAG of 8.8dB. As the gate resistance is reduced from 90Ω to 15Ω, the frequency of critical stability increases as the input reflection coefficient is smaller. The device is thus capable of sustaining oscillation to higher frequencies.

From the equivalent circuit elements obtained from Touchstone, the maximum frequency of oscillation f_{max} of each of the devices was evaluated using the expression[5.7],

$$f_{max} = \frac{f_T}{2\left(\frac{(R_g + R_i + R_s}{R_{ds}} + 2\pi f_T R_g C_{gd}\right)^{\frac{1}{2}}}$$

Device f_{max} as a function of gate length is shown in Figure 5.7.3.

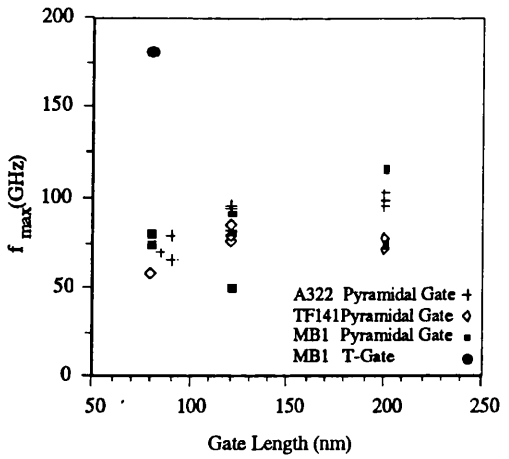

Figure 5.7.3 - f_{max} for both Pyramidal and T-Gate Structures of Various Gate Lengths on A322, TF141 and MB1 Devices

Figure 5.7.3 shows the influence gate resistance has on HFET gain at high frequency. The 80nm footprint T-gate device fabricated on MB1 has an f_{max} of 180GHz compared to an f_{max} of 80GHz for an 80nm pyramidal gate device fabricated on identical material.

Although the three materials studied have very different transport properties, it is impossible to exploit the advantages of one material system over another if the gate resistance of the devices is large. In Section 5.6, it was concluded that the effective velocity of carriers in the channel of MB1 devices was almost double that of devices fabricated on A322 and TF141 for gate lengths around 100nm yet, from Figure 5.7.3, the f_{max} of all the pyramidal gate devices are similar irrespective of material structure (and almost irrespective of gate length too). If devices are required to provide gain at and above 100GHz, it is imperative that the gate resistance be minimised, as only then can material properties capable of producing f_T's of 275GHz be fully exploited.

Chapter Summary

The DC and RF results obtained from the HFETs fabricated in the course of the project have been presented and discussed in this chapter.

The main results are :

i) Devices with intrinsic DC transconductance of up to 660mS/mm have been fabricated on TF141.

ii) The 0.2eV potential barrier below the 2DEG in the A322 layer structure improves carrier confinement and so DC device output resistance.

iii) From the DC transconductance data, there is no evidence of velocity overshoot in A322 or TF141, but difficulties in determining the gate-recess depth precluded a complete analysis.

iii) The MB1 layer displayed significant trapping effects which made analysis of DC device properties impossible.

iv) RF transconductances of up 1100mS/mm were measured on 80nm gate length MB1 devices. This translates to a minimum effective velocity of $2.4x10^5 ms^{-1}$, and indicates velocity overshoot is occurring in these devices.

v) 80nm gate length HFETs fabricated on MB1 have f_T's of up to 275GHz

vi) Sub-100nm T-Gate devices also fabricated on MB1 have f_T's of 265GHz

vii) From an analysis of the f_T of 200nm gate length devices on all three materials, it has been concluded that the effective carrier velocity in the channel is the transport property that limits device f_T. For the materials of this study, neither low field mobility or 2DEG carrier concentration were found to be significant in determining the device f_T for 200nm gate length devices.

viii) Device RF output resistance obtained from Touchstone equivalent circuit modelling is determined by the potential barrier below the 2DEG of the structures for all three materials of this study, and is worst for MB1 devices. A322 devices are best. The output resistance decreases with gate length for all devices.

ix) An estimate of the depletion region extension beyond the drain end of the gate allowed the effective gate length of the devices to be calculated. This permitted the effective channel velocity to be determined. Such an analysis yielded channel velocities in excess of $2.0x10^5$ ms^{-1} in MB1

devices. As the static electron saturation velocity is around $1.0x10^5$ ms^{-1}, this is further evidence of velocity overshoot in MB1 devices. Neither A322 or TF141 devices showed conclusive evidence of overshoot.

The large indium concentration in the MB1 channel layer increases the Γ-L valley energy separation while decreasing the electron effective mass. Both these effects increase the probability of the occurrence of velocity overshoot and are probably the cause of the large velocities extracted from MB1 devices.

x) 80nm footprint T-gate devices have gate resistance 5 times lower than pyramidal gate structures of similar footprint sizes.

xi) T-gate devices fabricated on MB1 were measured to have 8.8dB gain at 60GHz compared with 2.9dB gain for pyramidal gates on the same material.

xii) The low gate resistance of the sub-100nm footprint T-gate structure led to devices with f_{max} of 180GHz compared with f_{max} of 80GHz for pyramidal gate structures with a similar footprints size.

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Chapter 6 Conclusions and Future Work

6.1 Conclusions

The aims of this thesis were to determine the material and device properties which influence the high frequency performance of short gate length HFET's.

To study the material dependence, three MBE grown structures were used:

i) a conventional $Al_{0.25}GaAs/GaAs$ quantum well structure with an $Al_{0.25}GaAs$ confining barrier 300Å below the 2DEG

ii) a pseudomorphic $Al_{0.22}GaAs/In_{0.15}GaAs/GaAs$ structure with a 160Å $In_{0.15}GaAs$ strained channel

iii) a pseudomorphic $In_{0.52}AlAs/In_{0.65}GaAs/InP$ structure with a 100Å $In_{0.65}GaAs$ strained channel

Therefore, 2DEG's with different transport properties allowed the material dependence of high frequency device properties to be studied.

High frequency HFET performance dependence on gate length was investigated by fabricating conventional 'pyramidal' gates in the range 80 - 200nm. In addition, to study the effect of the gate resistance, devices with sub-100nm T-gate structures were fabricated. 80nm footprint T-gate structures were found to have 1/5 of the gate resistance of conventional 80nm footprint gates.

High frequency studies of devices showed the following main results :

i) 80nm gate length HFETs with f_T's of up to 275GHz were fabricated on the InAlAs/InGaAs/InP layer structure. Such f_T's were nearly twice those of similar gate length devices fabricated on both the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs structures.

ii) From the f_T measurements, it was possible to extract the effective carrier velocity in the device channel. Effective velocities in excess of $2.0x10^5 ms^{-1}$ were deduced for the InAlAs/InGaAs/InP structure, indicating significant velocity overshoot. No conclusive evidence of overshoot was observed in devices fabricated on either the AlGaAs/InGaAs/GaAs or AlGaAs/GaAs structures.

iii) The use of the T-gate structure increased the device gain by up to 6dB at 60GHz compared to a conventional gate device.

iv) Although the f_T's of the InAlAs/InGaAs/InP HFETs were much larger than those of the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs HFET's, the f_{max} of conventional gate structure devices fabricated on all three materials were similar because the large gate resistance dominated the device performance.

These results show that both the material and device structures influence the high frequency performance of short gate length HFET's.

Considering material structure first, there is evidence both from this project and elsewhere[6.1], that the use of an InGaAs channel in a HFET results in high effective carrier velocities, and thus larger device f_T's for a given gate length compared with GaAs channel structures. As discussed in Section 2.8.2, increasing the In content of the InGaAs channel increases the Γ-L valley energy separation whilst reducing the electron effective mass. Both these properties increase the velocity overshoot effect, which is most probably the cause of the large effective velocities extracted from f_T measurements of devices with high indium concentration (>53%) InGaAs channel HFET's. For the materials used in this study, it was

deduced that the effective velocity was the dominant transport property in determining device f_T at a given gate length. Neither the low field mobility or the 2DEG carrier concentration were found to govern device f_T.

It was also shown that both device DC and RF output resistance could be increased by increasing the potential barrier below the 2DEG and thus improving electron confinement to the channel.

It can be concluded that the criteria for a channel with a large effective carrier velocity and a well confined 2DEG are:

i) the channel layer be high In concentration (>53%) InGaAs

ii) a potential barrier of at least 0.2eV be formed around 300Å below the 2DEG

In addition to the general material requirements of the channel, it is important that device f_T and consequently f_{max} scale with gate length. This places two requirements on the gate capacitance region of the device:

i) The gate/2DEG separation should be around 20-30nm if sub-100nm gate length devices are to be fabricated. The layer structure should thus include a δ doped donor layer.

ii) The gate footprint should fill the gate recess trench, so the gate recess etch should be anisotropic, as may be achieved using dry etching. The use of a dry etched gate recess will be discussed in Section 6.2.

A fundamental limit to *total* gate capacitance scaling results from the contribution of the gate drain capacitance C_{gd}, which does not scale with gate length. As shown in Section 5.6.2, C_{gd} can contribute up to 40% of the total gate capacitance for an 80nm gate length device.

It is only possible to take advantage of an optimised material structure if a low resistance gate is achieved, as this study has shown that gate resistance dominates high frequency device gain, particularly for short gate lengths. The importance of reducing the gate resistance cannot be over-emphasised. Devices with sub-100nm footprint gates for operation at 100GHz and above, even with T-gate structures, will probably require multiple gate lines and air-bridge techniques to exploit fully the potential of the material structures described above.

6.2 Future Work

To build upon the findings of this project, with the eventual aim of producing circuits operating at and above 100GHz, research should be conducted in four areas :

i) Material Optimisation

ii) Dry Etched Gate Recess Techniques

iii) Improvement of sub-100nm T-Gate Process

iv) Further High Frequency Testing

Each of these areas will now be considered in more detail.

i) Material Optimisation

To further test the theory that neither mobility or carrier concentration determine device f_T, a bulk doped $In_{0.53}GaAs$ MESFET layer should be grown on InP. To achieve reasonable gate breakdown characteristics, such a structure will require an $Al_{0.52}InAs$ Schottky layer similar to the MB1 layer. The high frequency performance of devices fabricated on the MESFET layer should be compared with those fabricated on an $In_{0.53}GaAs$ channel 2DEG structure.

There is little doubt that increasing the indium concentration of the InGaAs channel improves device performance, so perfection of the MBE growth of InAs channel structures should be a high priority. As it is not lattice matched to InP, the InAs channel thickness will be determined by its ability to accommodate strain when it is grown. It is most likely that an InAs channel layer would be incorporated into a 2DEG InAlAs/InGaAs/InP HFET structure.

ii) Dry Etched Gate Recess Techniques

The issue of device uniformity has to be addressed if short gate length HFETs are to be incorporated into circuits. Lack of uniformity is mainly caused by variations in gate recess depth, and so a technique to reproducibly perform the gate recess etch is essential. The use of selective dry etching techniques, such as the CCl_2F_2 etch chemistry for the GaAs/AlGaAs system, allows good device uniformity to be achieved. CCl_2F_2 etches GaAs but not AlGaAs resulting in etch selectivities of up to 2000:1[6.2]. Such etching techniques allow device uniformity to be determined by the MBE layer structure. An analogous etch chemistry for InAlAs/InGaAs/InP systems which selectively etches InGaAs over InAlAs should be developed if InAlAs/InGaAs/InP HFET's are to be used in circuits.

iii) Improvement of Sub-100nm T-Gate Process

In this project, the yield of sub-100nm T-Gate devices was low. As gate resistance must be minimised, further effort should be directed towards improving the yield of the process. In Glasgow, this can be done by using the EBPG-5 Beamwriter for T-Gate definition, as the focus and astigmatism correction, critical parameters for successful definition of sub-100nm footprint gate structures, are under computer control.

iv) Further High Frequency Testing

An important figure of merit for any high frequency transistor is its noise figure. Due to lack of time and suitable equipment, no noise studies were performed on the devices fabricated in this project.

This is something which should be remedied. Additionally, spot frequency rf device characterisation, say at 60GHz, 94GHz and 120GHz to determine device gain and noise behaviour should be conducted. This is not a simple undertaking, as test fixtures and transitions to go from the coplanar waveguide structure of the HFET devices to the rectangular waveguide measurement system will be required. However, it is necessary to characterise devices at their intended operation frequency.

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