DESIGN OF A LOW POWER EXTERNAL CAPACITOR-LESS LOW-DROPOUT REGULATOR WITH GAIN-COMPENSATED ERROR AMPLIFIER

A Thesis

by

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ABSTRACT

This thesis introduces a gain-compensated external capacitor-less low-dropout voltage regulator with total 5.7 uA quiescent current at all load conditions. The two-stage gain-compensated error amplifier is implemented with a cross-couple pair negative resistor to make the LDO achieve higher gain (> 50 dB) with very low bias current (< 1.3 uA). The LDO can achieve 52 dB loop gain at no load condition, 64 dB at 1 mA and 54 dB at 100 mA load. During transients (0 A to 100 mA) the undershoot is optimized to 98.6 mV with 100 ns rising and falling time through a differentiator circuit to boost the LDO's transient response. The phase margin of the proposed LDO is 55° at 1 mA and 79.27° at max load (100 mA). Figure of merit (FOM) of this work is 2.79 fs which is very small.

DEDICATION

In dedication to my family, my girlfriend and my faith of being a great engineer.

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Contributors

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NOMENCLATURE

LDO	Low-dropout
MOSFET	Metal-oxide-semiconductor field-effect transistor
PMOS	P-type metal-oxide-semiconductor
NMOS	N-type metal-oxide-semiconductor
PMIC	Power management integrated circuit
IOT	Internet of things
DC	Direct current
AC	Alternating current
RF	Radio frequency
PSRR	Power supply rejection ratio
FVF	Flipped voltage follower
ESR	Equivalent series resistance
FOM	Figure of merit
OPAMP	Operational amplifier
OTA	Operational transconductance amplifier
PCB	Printed circuit board
ADC	Analog digital converter
LHP	Left half plane
RHP	Right half plane

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1. INTRODUCTION

Power management IC (PMIC) is used everywhere nowadays such as mobile devices, automotive, internet of things (IOT) hardware, particularly wearables. In a integrated power management unit (PMU), there are different modules with different supply voltage while the system only has one constant input voltage. Therefore, the voltage regulators are needed to supply different voltages for sorts of applications. As shown in Fig 1.1, there are multiple different applications with different voltage regulators. Switching regulators are commonly used in boosting DC voltage (boost-converter) or stepping down DC voltage (buck-converter). For example, LED drivers usually need higher voltage (10-20 V) than the supply voltage (about 3 V) so the boost converter is introduced to provide this higher voltage to drive the LED. The input of high voltage analog, digital and RF blocks can be directly from LDOs. However, other ports such as low voltage analog, RF block and digital block are regulated by multiple buck converters followed by low-dropout (LDO) regulators. The combination of switching converters and LDOs plays an important role in providing a clean and precise voltage supply with high efficiency and low quiescent current.

With the increasing development of system on chip solutions, on chip low-dropout linear regulator (LDO) with very low quiescent current is becoming more and more popular. Traditional LDO has a large output capacitor in the uF range which requires an additional pin on the chip. Capacitorless LDO is more and more popular nowadays because the output capacitor is in the range of pF so it is widely used in SOC chip designs and internet of things (IOT). There also comes some problems such as bad stability, large undershoot during transients and bad power supply rejection ratio (PSRR). Another increasing trend for SOC designs and IOT is extended battery life which is crucial for the wearables, portable devices and battery-powered applications.

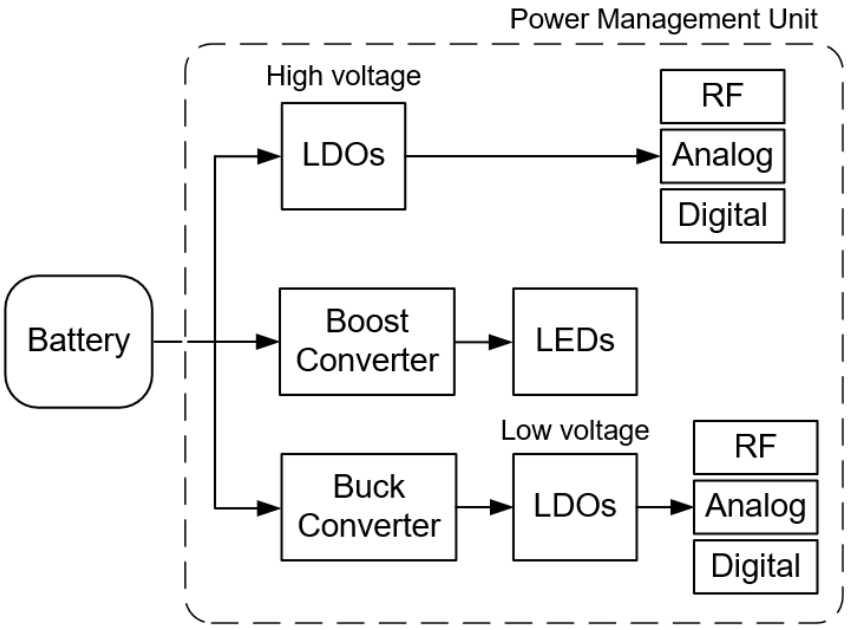

Figure 1.1: Power management unit block

1.1 Voltage Regulator Architectures

Fig. 1.2 shows the different output voltage conditions as time is elapsing. The battery's voltage is decreasing with respect to time while the switching regulator and linear regulator can maintain a constant voltage as long as the battery voltage is larger than their output voltages. However, the output voltage of the switching regulator has noticeable ripple as a result of the rapidly switching between on and off causing the charging and discharging of the large output capacitor. The linear regulator does not have this ripple problem because the pass element is continuously on and there is a negative feedback to compare the output voltage with the reference voltage then regulating the constant output voltage.

As mentioned earlier, voltage regulators are critical parts to produce a constant ripple-free voltage for any input and load changes in power management. There are basically two types of voltage regulators. One is switching regulator, the other is linear regulator.

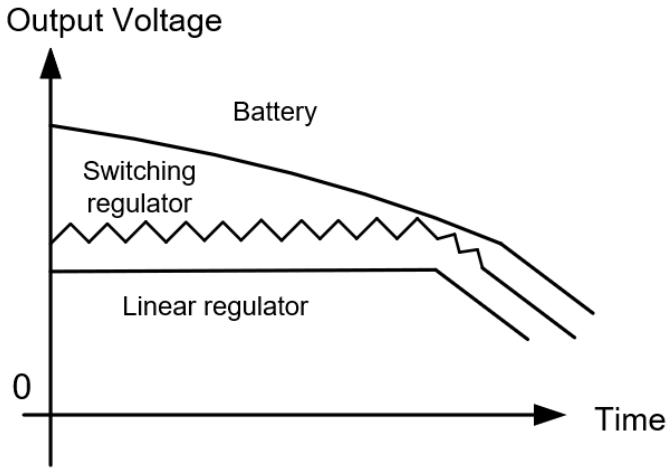

Figure 1.2: Output voltage after battery and different regulator

1.1.1 Switching Regulator

Considering the high efficiency when converting the DC input voltage to different direct current (DC) output voltages, the switching regulators are the best way. The block diagram of switching regulators is shown in Fig. 1.3. The controller provides a regulated constant output voltage by sensing the output, comparing the output with the reference voltage and then creating the control signal to the controller to regulate the input voltage. The basic switching regulator architectures include a step-down (buck) converter, a step-up (boost) converter or a step-up or step-down (buck-boost) converter depending on the relationship between the input voltage and the output voltage. The switching regulators use a switching element that switches on and off to maintain a constant output voltage.

1.1.2 Linear Regulator

From Fig. 1.4, a linear regulator is functioning by comparing the reference voltage and feed-back voltage from the voltage divider, the linear regulator is able to output a clean and constant voltage. Compared with switching regulators, the linear regulator act as a variable resistor which

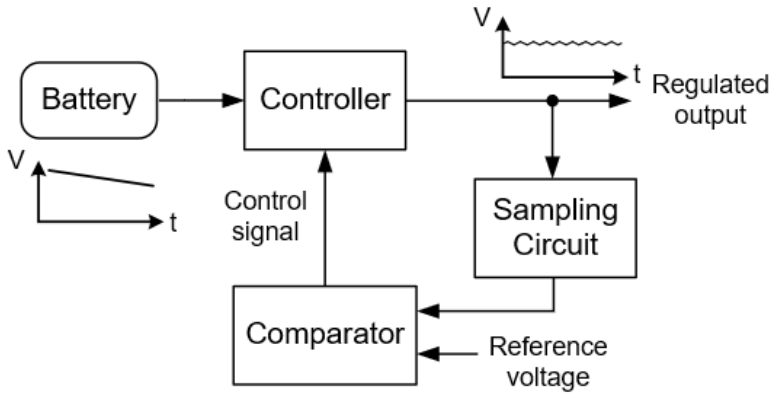

Figure 1.3: Typical block diagram of a switching regulator

result in lower efficiency since the output voltage is always lower than the input voltage. However, the linear regulator has a noiseless output and fast transient response to the load. The LDO is the most frequently used linear regulator to provide a clean and constant voltage at the output with very low quiescent current and small drop out voltage between the input and the output.

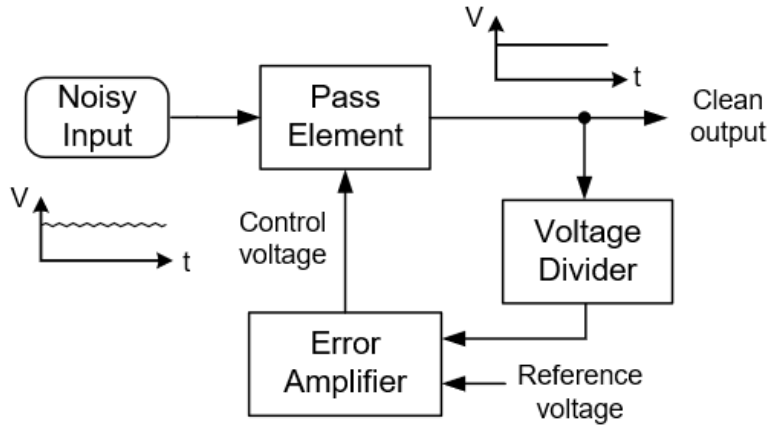

Figure 1.4: Typical block diagram of a linear regulator

1.2 Literature Review and Motivation

Since the customers nowadays appreciate the longer battery time, more compact and cheaper portable devices, designing high-performance capless LDOs with very low quiescent current is becoming more and more important in power management. In IOT applications, efficiency is very critical therefore a lot of techniques in power management are proposed to prolong the battery life-time [1][2]. PSRR is also essential for LDO to reject the supply ripple and noise. Researchers proposed additional circuits to cancel the noise coupled through the gate source capacitor and the equivalent resistor of the pass transistor[3]. To achieve very fast transient response for capacitor-less LDOs , some researchers are using flipped voltage follower (FVF) topology to provide a low voltage capacitor-less LDO with very fast settling time during transients[4]. However, it is not suitable in applications such as IOT and mobile phones since the quiescent current is in the range of mA which is 1000 times larger than low power LDOs. In the meanwhile, the open loop gain of FVF topology is small which degrades the accuracy of the output voltage.

Seen from all the previous work, improvement of the transient response without large output capacitor can be improved by sensing the output undershoot then feedback to the gate of the pass element or increasing the slew rate adaptively[5]. To solve the main trade-off between low quiescent current and fast transient response, a differentiator can be used to boost the slew rate only when there is a large output transient [6][7]. This consumes little power and improves the transient performance of the LDO. Another important trade-off is achieving a high loop gain when consuming very low quiescent current for the error amplifier in the LDO. Since the accuracy of LDO's output is highly dependent of the open loop gain, an approach of achieving a decent loop gain (> 50 dB) while consuming low quiescent current should be created. Furthermore, achieving good stability for a range of low load to full load without the ESR zero requires a robust compensation method. These challenges are the main motivation for this research to achieve a stable high gain LDO with fast transient response and low power consumption for full load range (0 A to 100 mA) with a low FOM.

2. LOW-DROPOUT VOLTAGE REGULATOR FUNDAMENTALS

LDO is a typical negative feedback system to create the clean constant output voltage which is shown in Fig. 2.1. When the output voltage goes up, the operational amplifier (opamp) amplifies the voltage difference then the gate voltage of the pass element goes up. The pass element will provide less current to the output so that the output voltage drops to maintain a constant output voltage. This feedback network makes the LDO's output voltage precise and resilient to the load and line transients. Since the voltage provided by switching regulators is noisy the LDO is required to provide a clean voltage while consuming little power and small drop out voltage.

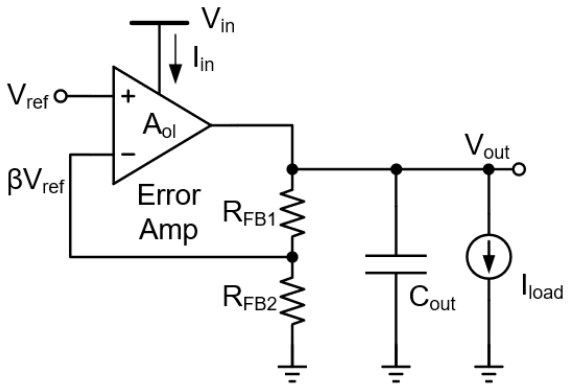

Figure 2.1: Block diagram of a typical LDO

The basic equation of an LDO is shown in equation 2.1. A_{ol} is the open-loop gain of the LDO and it is critical in the accuracy of the output voltage. The larger the open loop gain is, the more accurate the output voltage will be. Assume the product of the feedback factor β and open loop gain A_{ol} is much larger than 1, the output voltage is independent of the open loop gain as shown in equation 2.2. β is defined by the feedback resistors which can be shown in equation 2.3.

$$V_o = \frac{A_{ol}}{1 + \beta A_{ol}} V_{ref} \tag{2.1}$$

$$V_o \approx \frac{1}{\beta} V_{ref} \tag{2.2}$$

$$\beta = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \tag{2.3}$$

The drain current of the pass transistor is dependent on the load current. From the equation 2.4, if the drain current of the pass transistor is predetermined, the size of the LDO can be calculated assuming the overdrive voltage which is the voltage difference between the source gate voltage and the threshold voltage is determined.

$$I_d = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{sg} - V_{th})^2 \tag{2.4}$$

At no load condition, this bias current is defined by the output voltage and the feedback resistors. In order to minimize the quiescent current, the feedback resistors are usually large (100 kΩ to 1MΩ). This will make the voltage between source and gate small which may turn some transistors of the error amplifier into triode region. At max load current, the gate voltage is tuned by the feedback network and the error amplifier. The feedback resistors scale down the output voltage and the feedback voltage is compared with the bandgap reference voltage throught the error amplifer to control the pass transistor's gate voltage so that providing the load current.

2.1 LDO Design Parameters

LDO parameters mainly include two aspect: steady-state performance parameters and dynamic-state performance parameters. These parameters will be presented in this section.

2.1.1 Dropout Voltage

The dropout voltage defines the voltage difference between the input and the output when the LDO stops to regulate the input voltage as the input voltage decreases. From Fig. 2.1, as the

input voltage increases from zero, the operation region of the pass transistor changes from off to triode and to saturation finally. In saturation region, the LDO can regulate the output voltage with a constant value. However, the output voltage drops as the input voltage decreases when the pass transistor is in triode region.

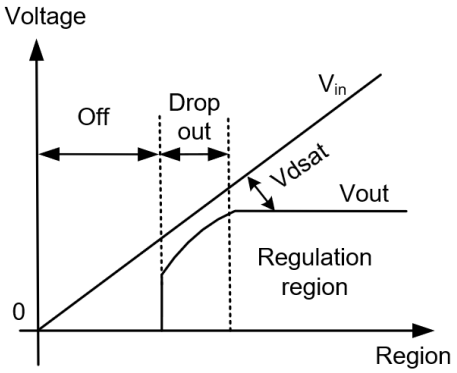

Figure 2.2: Input-output voltage characteristics of a typical LDO

2.1.2 Quiescent Current

Quiescent current is the total input current delivered to the LDO when the load current is zero. It consists of the bandgap reference current, the bias current of the error amplifier and the voltage divider current shown in equation 2.5. In Fig. 2.1, the total current going into the LDO minus the total output load current is the quiescent current of the LDO.

$$I_q = I_{in} - I_{load} \tag{2.5}$$

Minimized quiescent current is critical to an LDO with low power consumption and high efficiency. It should be mentioned that the quiescent current increases dramatically with the load current if the pass element is a bipolar transistor because the bipolar transistor is a current-driven device instead

of voltage-driven device. Therefore, it is essential to use MOS transistor in LDO if low power consumption is critical especially in IOT devices.

2.1.3 Efficiency

LDO's power efficiency is determined by the input and output voltage, load current and quiescent current as shown in equation 2.6. From the equation 2.6, V_O is the LDO's output voltage, I_{load} is the LDO's output load current, V_{in} is the input voltage going into the LDO and I_q is the quiescent current of the LDO.

$$\eta = \frac{V_o I_{load}}{V_{in}(I_q + I_{load})} \tag{2.6}$$

It is obvious that the power efficiency highly depends on the dropout voltage and quiescent current of an LDO. Especially in advanced technology with lower supply voltage, the quiescent current in the denominator plays a more important role in both power efficiency and current efficiency. Assuming the quiescent current is much less than the load current which means the quiescent current can be ignored in this case, the efficiency can be close to 100% when the output voltage is close to the input voltage. However, small difference between the input and the output requires the really large pass transistor which means the response of the LDO is bad because of the large parasitic capacitor at the gate of the pass transistor.

2.1.4 Line and Load Regulation

Line regulation is the indication of an LDO's ability to maintain a constant output voltage when input voltage changes shown in Fig. 2.3. The input voltage of an LDO can changes from nominal value to a higher value such as 1.1 V to 1.5 V in this paper. The output voltage will changes as well. The smaller the calculated line regulation is, the better the steady state performance is. The

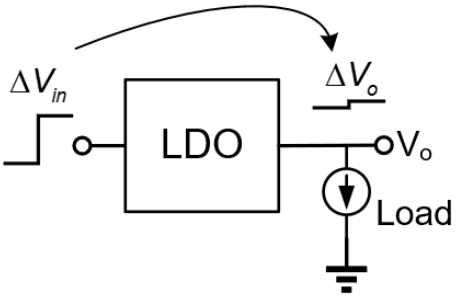

Figure 2.3: Line regulation diagram

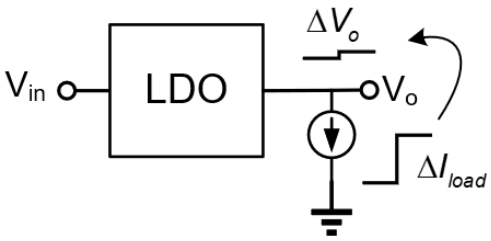

Figure 2.4: Load regulation diagram

equation is shown in equation 2.7.

$$Line\ regulation = \frac{\triangle V_o}{\triangle V_{in}} = \frac{V_{o(vin,max)} - V_{o(vin,min)}}{V_{in,max} - V_{in,min}} \approx \frac{g_{mp} r_{op}}{\beta A_{ol}} + \frac{\triangle V_{ref}}{\beta V_{in}} \tag{2.7}$$

Line regulation mainly depends on the closed loop gain of the LDO. The accuracy usually gets worse if the load current increases since the gain decreases with the load current increase. To improve the line regulation of an LDO, increasing the closed loop gain is essential.

Similar to the line regulation, the load regulation is the LDO's ability to maintain a constant output voltage for any load current change shown in Fig. 2.4, as expressed in equation 2.8.

$$Load\ regulation = \frac{\triangle V_o}{\triangle I_{load}} = \frac{V_{o(Iload,max)} - V_{o(Iload,min)}}{I_{load,max} - I_{load,min}} = \frac{r_{op}}{1 + \beta A_{ol}} \tag{2.8}$$

Load regulation is closely related to the loop gain of the LDO and the equivalent output impedance, so a large loop gain with small output impedance under all load conditions is critical to achieve a high load regulation performance. It should be mentioned that under different load the gate voltage of the pass element changes correspondingly which may drive the transistors in error amplifier into triode region so that deteriorating the loop gain of the LDO. Line regulation and load regulation are both DC performance of the LDO instead of transient effects.

2.1.5 Power Supply Rejection Ratio (PSRR)

PSRR is a measure of attenuating the noise and ripple from the input to affect the output which can be expressed in equation 2.9. A good PSRR at higher frequency will make the LDO have better ability to reject the input noise at that specific frequency range. This is critical for LDOs because the switching frequency of the switching regulator is above 100 kHz and the LDO should be able to reject the high frequency ripple and noise from the switching regulator.

$$PSRR = 20\ log_{10}\frac{V_{in}}{V_{out}} \approx \frac{1}{A_{ol}(s)} \tag{2.9}$$

Since the output voltage of switching regulators has noticeable ripple at switching frequency, the PSRR of an LDO is instrumental in regulating the noisy supply voltage to provide a clean and noiseless voltage. As a result of the decreasing loop gain beyond the bandwidth, the PSRR will deteriorate at frequency larger than the bandwidth which can be seen in Fig. 2.2.

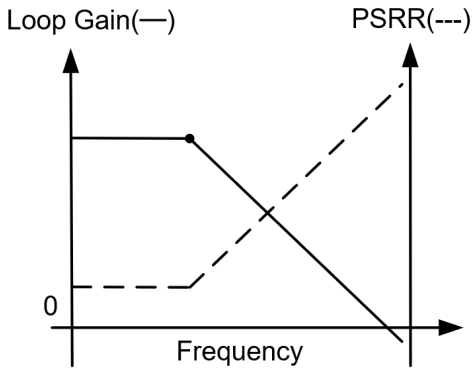

Figure 2.5: PSRR with frequency

Fig 2.5 shows the relationship between the PSRR and the loop gain of the LDO. Since the PSRR is inversely proportional to the open loop gain, the decrease of the loop gain will make the PSRR worse as well. To improve the PSRR performance of an LDO, a large gain-bandwidth is

critical which can be seen from the equation 2.9.

2.1.6 Load Transient

Load transient response of an LDO is an indication of the ability to supply load current without large undershoot or overshoot when there is a current step at the output. The equation 2.10 defines the maximum voltage variation during transients[8]. The transient response of an LDO is highly dependent on the maximum load current ($I_{o,max}$), system bandwidth ($\triangle t_{bw}$), output capacitor (C_o), bypass capacitor (C_b) and the voltage across the ESR of the output capacitor ($\triangle V_{ESR}$). For a conventional LDO with a huge output capacitor, a large output capacitor with a small ESR helps improve load transient response which is shown in Fig. 2.6. However, external capacitor-less LDO does not have that large capacitor with ESR. Even though there is no $\triangle V_{ESR}$ part in capacitor-less LDO, the output on-chip capacitor is really small so that the undershoot and overshoot during transients is huge.

$$\triangle V_{tr} = \frac{I_{o,max}}{C_o + C_b} \triangle t_{bw} + \triangle V_{ESR} \tag{2.10}$$

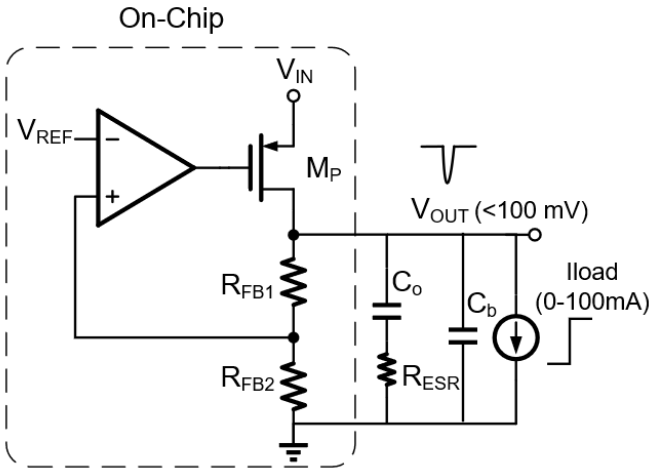

Figure 2.6: Macro model of the uncompensated load transient

Many applications require LDO to have a good transient response such as powering DSPs, microcontrollers and digital IC circuits. If the LDO's output has a large spikes during transients, some applications such as low-voltage CPUs will malfunction even latch up. The slew rate of the error amplifier before the pass transistor is critical to the transient response of the LDO. It is because the gate of the pass transistor usually has a huge parasitic capacitor which needs a large current to drive.

2.2 LDO Classification

Depending on the type of the output capacitor with different compensation mechanism, LDOs can be classfied into two type: Conventional LDO with huge output capacitor and external capacitor-less LDO with small on-chip capacitor. This section will analyze the two different LDO and explain the trade-offs.

2.2.1 Conventional LDO Architecture

The conventional LDO topology is shown in Fig. 2.7. A conventional LDO is composed of a pass element, an error amplifier, a bandgap reference, a feedback network and a large output capacitor with equivalent series resistance (ESR). The error amplifier, pass element, feedback network and bandgap reference are integrated on chip. The huge output capacitor with ESR is off chip and needs an additional pin for the connection. The error amplifier is a high gain opamp comparing the bandgap reference voltage with the scaled down output voltage which is obtained by the feedback resistors. The accuracy of the output voltage is highly dependent on the open loop gain of the LDO since a small difference between reference and scaled down output will be amplified by the error amplifier to adjust the output voltage. For example, an LDO with 60 dB open loop gain may have error less than 0.1%. To ensure a high accuracy of the LDO, the error amplifier should have a large gain.

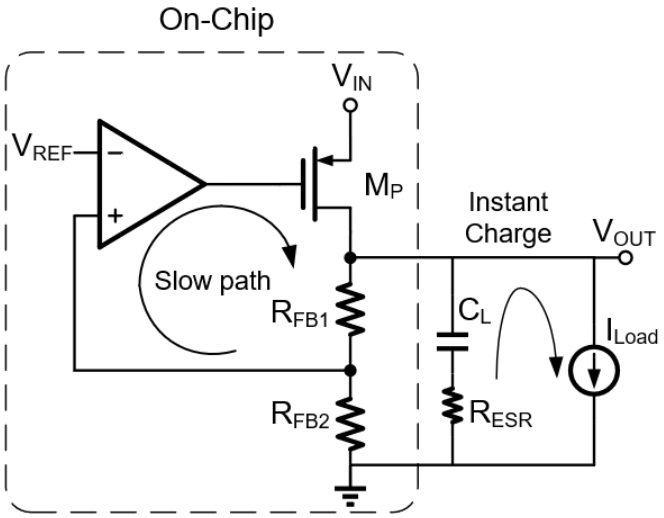

Figure 2.7: Conventional LDO current path during transients

This conventional LDO architecture can achieve good stability because there is a left half plane (LHP) zero introduced by the ESR of the output capacitor. Fig. 2.8 shows that the LHP zero will cancel the effect of the second pole P_2 assuming the ESR is chose correctly to make sure the system have a good phase margin which is usually larger than 60°. From the equation 2.11, the dominant pole ω_{p1} is inversely proportional to the output load current shown in equation 2.12 which means as the load changes the dominant pole moves a lot causing variable bandwidth under different load conditions.

$$H = \frac{A_{ol}(1+\omega_z)}{(1+\omega_{p1})(1+\omega_{p2})} \tag{2.11}$$

$$\omega_{p1} = \frac{1}{R_o C_o} \approx \frac{\lambda I_{load}}{C_o} \tag{2.12}$$

Another advantage of this conventional LDO is that it can achieve a really good transient response as a result of the huge off-chip capacitor. It is because the large capacitor provides an instant current path into the load before the gate of the pass element is adjusted through the slow path loop during fast load transient shown in Fig. 2.7. The fast path is from the output capacitor to the load and the slow path is from the feedback network and error amplifier to the pass element

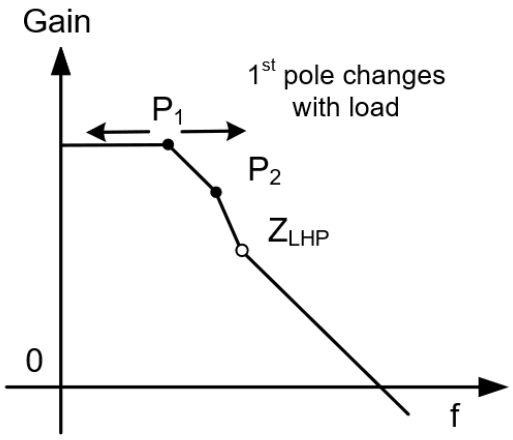

Figure 2.8: Frequency response of the conventional LDO

and then the load. Since it takes much longer for the error amplifier sinking or sourcing current to adjust the output voltage, the large output capacitor can provide a fast path for the instant load current need. However the huge off-chip capacitor consumes a really large area and an external pin for the chip which needs large space in printed circuit board (PCB).

2.2.2 External Capacitor-less LDO Architecture

Compared with the conventional LDO, the capacitor-less LDO topology which shown in Fig. 2.9 only has a small on-chip capacitor in the range of 50 pF to 100 pF. It should be noticed that the small on-chip capacitor with the ESR contributing an LHP zero is not pratical because the unity gain frequency is usually in the range of kHz and the ESR should be in the range of MΩ which consumes a really large area and will lead to a large undershoot during load transients. From Fig. 2.10, there are two poles and no LHP zeros before the unity gain frequency and the load current changes the second pole by more than one decade. From the equation 2.13, the second pole ω_{p2} is the output pole which has a wide range as the output load current goes from minimum to maximum. The worst case happens when there is no load at the output so that the output pole is at low frequency to yield a bad phase margin of the LDO. Without any compensation methods, the

LDO has a really bad phase margin especially at low load condition. As the load current increases, the second pole moves to a much higher frequency above the unity gain frequency so that the phase margin is larger than 60°.

$$H = \frac{A_{ol}(1+\omega_{z_m})}{(1+\omega_{p1})(1+\omega_{p2})} \tag{2.13}$$

To have a good phase margin at low load condition, it needs an additional compensation network

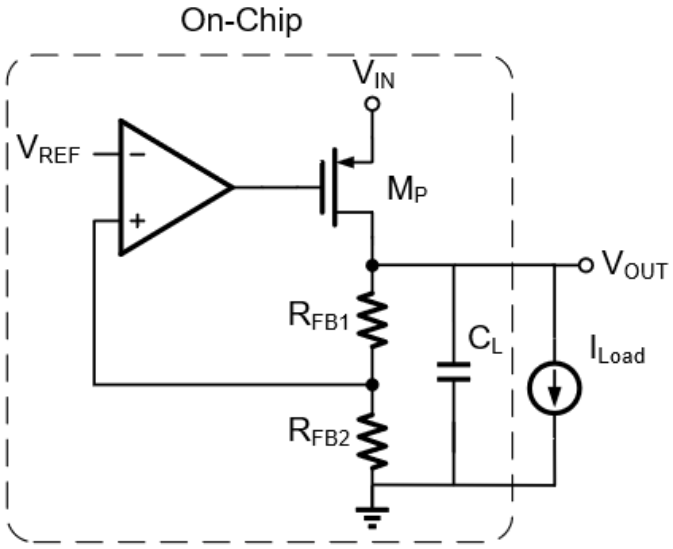

Figure 2.9: External Capacitor-less LDO

to compensate the phase margin or adjust the parameters of the whole system to make the second pole beyond the unity gain frequency. The Fig 2.11 shows a compensation method of miller compensation with a nulling resistor. The nulling resistor R_{null} is in series with the miller capacitor C_c across the gate and drain of the pass transisitor. This single miller capacitor with a nulling resistor modifies the location of the RHP zero gm/C_{gd} which is shown in equation 2.14. The original zero will be pushed to LHP if the resistance of the nulling resistor is larger than 1 over transconductance of the pass transistor.

$$\omega_{z_m} = \frac{1}{(1/g_{mp} - R_{null})C_c} \tag{2.14}$$

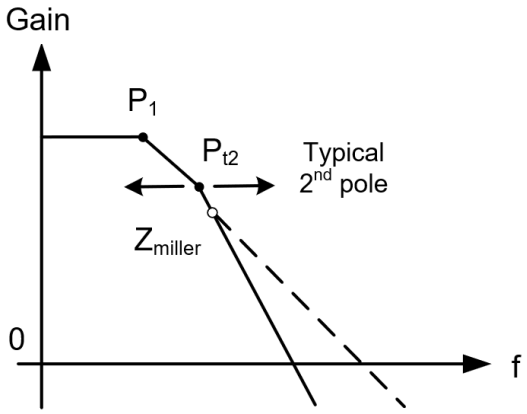

Figure 2.10: A typical AC response of a capacitor-less LDO with an LHP zero

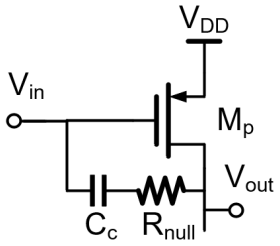

Figure 2.11: Miller compensation with a nulling resistor

As for the transient response of the external capacitor-less LDO, a large undershoot or overshoot will be generated for the load changing from minimum load to maximum load with 100 ns rising and falling time. It is because the small on-chip capacitor cannot provide an instant current through a fast path to compensate the huge change of load current during a short rising time because the overshoot voltage is inversely proportional to the size of the output capacitor. Therefore, it takes much longer time which is mainly depending on the LDO's bandwidth for the LDO to adjust the output voltage causing the large spikes during transients. This problem is catastrophic for most of applications such as analog digital converter (ADC). If the undershoot is too large, it will make the ADC malfunction and affect the accuracy of the whole system.

3. LOW POWER EXTERNAL CAPACITOR-LESS LDO DESIGN

From the previous sections, there are mainly two trade-offs when designing a low power external capacitor-less LDO. The first trade-off is achieving high gain with very low bias current going through the error amplifier. The second one is to achieve good transient response and good stability without large output capacitor with LHP zero introduced by the ESR.

3.1 Design Challenges

To design a low power and external capacitor-less LDO, there are some essential challenges which is shown in Fig. 3.1. The first one is that low power consumption deteriorates both dc and ac performance of an LDO. To achieve a low power consumption, the error amplifier inside the LDO can only have limited biasing current which is about 1.3 uA in this work. This limited biasing current makes the error amplifier have a large output impedance which contributes to a pole residing at very low frequency, which degrades the LDO's bandwidth, stability and transient response. The small biasing current also leads to a large output impedance of the error amplifier because the current is inversely proportional to the current as shown in equation 3.1. The large output resistance combined with the large parasitic gate capacitance of the pass transistor constitutes to a very low frequency pole which is usually the dominant pole. The lower frequency the dominant pole is at, the worse stability the LDO has.

$$r_{ds} = \frac{1}{\lambda I_D} \tag{3.1}$$

Furthermore, the limited power constraints the LDO's accuracy at the output because the gain of the error amplifier is proportional to the bias current. Little power consumption leads to the small open loop gain of the LDO, which deteriorate the LDO's dc performance such as load and line regulations.

Another critical challenge is caused by the small on-chip capacitor. As mentioned earlier,

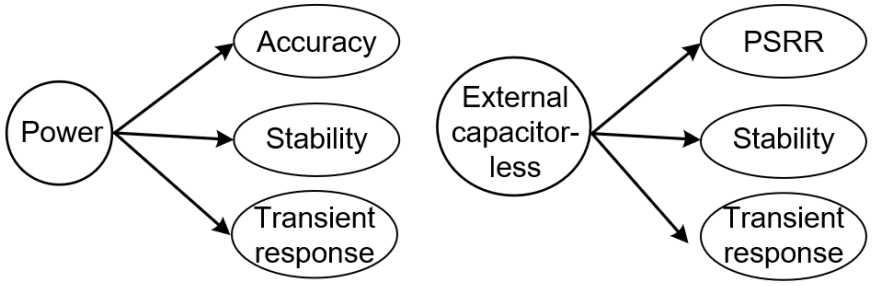

Figure 3.1: Low power external capacitor-less design trade-offs

the conventional LDO has a huge off-chip output capacitor with an ESR. The equivalent series resistor contributes to a LHP zero cancelling the second pole of the LDO, which is beneficial in stability. For transient response, the huge output capacitor reduces the undershoot whenever there is a fast load transient. It is because the huge capacitor provides a fast path for the current following to the load instantly until the LDO can react to the output load transient and adjust the current through the pass transistor. However, the external capacitor-less LDO only has one small on-chip capacitor without an ESR. The small output capacitor makes the pole at the gate of the pass transistor become the dominant pole while the output pole becomes the non-dominant pole. Since the output pole changes with the load condition, the compensation for the stability of the LDO is necessary especially at no load condition where the non-dominant pole is at very low frequency which makes the phase margin of the whole system very small. What's more, the small on-chip capacitor cannot provide a fast current path for any fast load changes which causes large undershoot during output load transients. PSRR is also an essential performance which is degraded in external capacitor-less LDO. This paper mainly focuses on the compensation of the open loop gain and transient response with low power and no external capacitor.

3.2 External Capacitor-Less LDO System Architecture

The uncompensated LDO architecture is shown in Fig. 3.2. The uncompensated LDO composes of a two-stage error amplifier, one PMOS pass transistor, a feedback network with two feedback resistors and one on-chip 50 pF capacitor. The output current load is modeled as an ideal current source. Without any compensation for the gain and transient response, the open loop gain at 100 mA load is only 41.8 dB causing a bad PSRR with -25 dB at 100 kHz operating frequency. The undershoot during fast load transient from 0 A to 100 mA is 900 mV with a 100 ns rising time which is catastrophic to the following analog or digital blocks. Therefore, the open loop gain of the error amplifier should be compensated to improve the PSRR, accuracy, load regulation and line regulation. The transient-enhanced circuit which is a differentiator-based slew rate boosting circuit in this work is introduced.

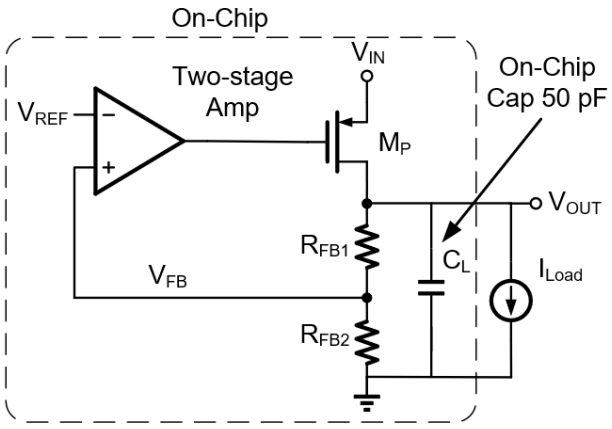

Figure 3.2: Macro model of the uncompensated LDO

The macro model of the compensated external capacitor-less LDO with low power consumption is shown in Fig. 3.3. The LDO has a two-stage error amplifier with cross-coupled pair negative resistors and a differentiator to enhance the transient response with a small on-chip output capac-

itor (50 pF). Since the small on-chip capacitor does not have the ESR, the location of the poles and RHP zero should be placed adequately to make the LDO have a good phase margin. In this paper, the load is modeled as an ideal current source instead of a resistor because the resistor load will affect the output impedance of the LDO. With a resistive load at the output, the output pole frequency will be pushed to a higher frequency especially at no load condition. Since this work focuses on low power design, the bias current of the error amplifier is limited so that the slew rate is constrained. Under this condition, the transient response without any compensation is really bad because the small biasing current of the error amplifier and the large parasitic gate capacitance slows the voltage change at the gate which means the output changes slowly with a large undershoot. Therefore, a sensing network should be proposed to compensate the load transient response. The RC diffrentiator yields the best performance to enhance the transient performance of the LDO without changing the operating point of the LDO and much power consumption. With the gain-compensated error amplifier and the differentiator, the open loop gain of the whole LDO improves to 52.5 dB (243% increase) at worst case and the undershoot during fast load transients decreased from 900 mV to 98.6 mV.

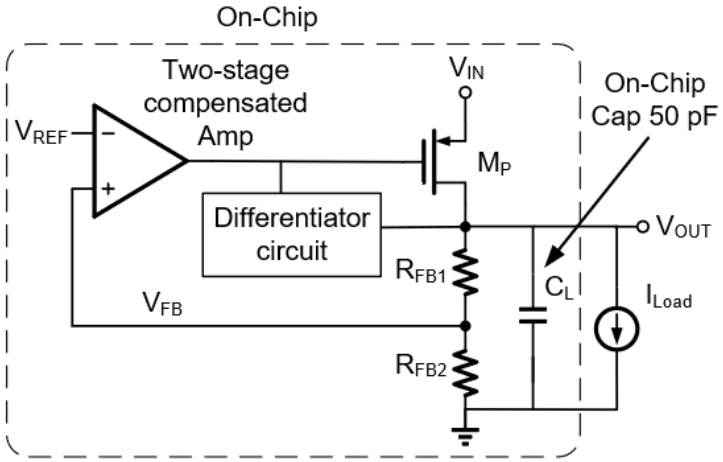

Figure 3.3: Macro model of the compensated LDO

This following sections will introduce the specific design of the pass transistor, feedback network, gain-compensated error amplifier, differentiator. Then stability of the LDO is analyzed.

3.3 Pass Transistor Design

As the largest transistor in an LDO, the pass transistor determines the maximum load current and lowest dropout voltage across it. The gate parasitic capacitor is very large so that approaches are needed to compensate the stability and the transient response of the external capacitor-less LDO.

For the pass element, five basic configurations are showned in Table 3.1. This compare table is from a report of different LDO voltage regulators using different pass elements[9]. These five configurations including NPN Darlington, NPN bipolar, PNP bipolar, NMOS source follower and common source PMOS transistor apply for different technology and specific requirements.

	Darlington	NPN	PNP	NMOS	PMOS
$V_{dropout}$	$V_{dsat} + 2V_{be}$	$V_{dsat} + V_{be}$	V_{ecsat}	V_{dsat}	V_{dsat}
I_{load}	Large	Large	Large	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
Speed	Fast	Fast	Slow	Medium	Medium

Table 3.1: Comparison of pass element configurations

There are many differences between the MOSFET and the bipolar device. Quiescent current is an important difference so that MOSFETs are more popular nowadays with very little quiescent current while the bipolar needs to consume much more quiescent current. It is because the MOSFETs are voltage driven device and the bipolar transistors are current gate driven device with limited forward current gain (β) which means the error amplifier should be able to drive a large sinking or sourcing current to the bipolar pass element. Furthermore, compared with NMOS transistors, PMOS transistors have more benefits such as low dropout voltage and no charge pump

required which is shown in Fig. 3.4. Since the gate source voltage V_{GS} of an NMOS transistor

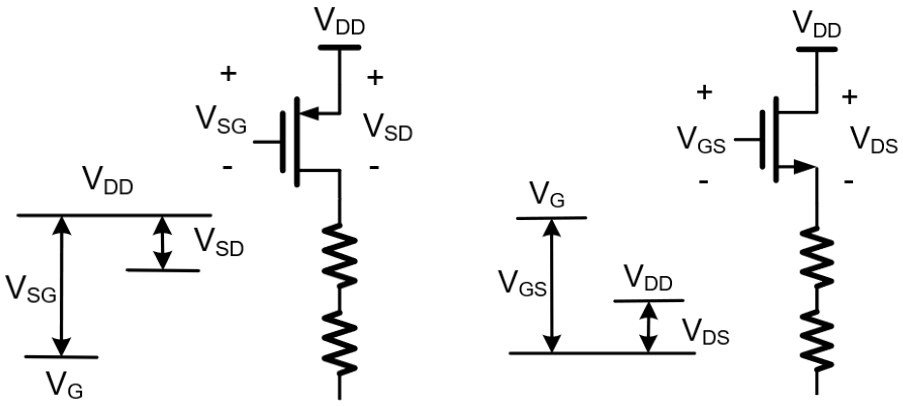

Figure 3.4: Input swing comparison between NMOS and PMOS pass transistors

is usually much larger than the dropout voltage V_{DS} which means the gate voltage of the pass element is larger than the input supply voltage. This requires additional charge pump circuit for the NMOS LDO to boost the gate voltage above the supply voltage which makes the circuit costly and complex. For the PMOS pass transistor, the gate voltage is smaller than the supply voltage by V_{SG} and the gate voltage of the pass transistor is smaller than the supply voltage which eases the requirement for the error amplifier. So for this paper, the PMOS is chose to be the pass element for the LDO. To determine the size of the PMOS transistor, the dropout voltage and the maximum load current should be known first. In this paper, the dropout voltage is 200 mV and the maximum load current is 100 mA. Therefore the width and length ratio can be determined by the square law equation 3.2.

$$\frac{W}{L} = \frac{2I_{o,max}}{\mu_p C_{ox} V_{dsat}^2} = 70941 \tag{3.2}$$

Given that the dimension ratio of the pass transistor, the length of the pass transistor is chose to be 50 nm as a trade-off between the transconductance and the parasitic capacitor at the gate, so the width is calculated as 3.547 mm. The parameter values of the pass transistor are shown in Table 3.2.

Parameter	Value
W	3.547 mm
L	50 nm
V_{ds}	200 mV
I_{MAX}	100 mA

Table 3.2: Pass transistor parameter values

From lots of previous works, the technology is usually 180 nm or more which means the width is too large to make the LDO have a slow transient response with large spikes and small bandwidth. This work is based on TSMC 40 nm technology so that the size of the pass element can be comparatively small which is beneficial to the performance of the LDO. From the simulation, the source gate capacitance C_{sg} is 1.627 pF and the gate drain capacitance C_{gd} is 0.4 pF. It can be seen the parasitic gate capacitance is really small compared with that of most of the previous works. The miller effect is not that obvious when the output load is 100 mA because the gain of the pass element stage decreases with the drain current increase which is about 3.67 at 100 mA so the C_{gd} is small. According to the equation 3.3, gate capacitance C_{gg} is 3.495 pF at 100 mA output load.

$$C_{gg} = C_{sg} + (1 + A)C_{gd} \tag{3.3}$$

Once the size of the pass transistor is determined, the output swing of the error amplifier and the value of the feedback resistors can be decided. To have a 1 uA quiescent current through the pass element when there is no output current, the feedback resistors $R_{FB1} + R_{FB2}$ are calculated as 900 kΩ with an output voltage of 0.9 V. The quiescent current should be designed well to make sure the LDO has enough gain to maintain the accurate output voltage. In this work, the second stage of the error amplifier is connected to the gate of the pass transistor so the V_{sg} of the pass transistor when there is no output current should be larger than V_{dsat} of the PMOS transistor in the second stage. Since the reference voltage is simulated to be 800 mV to yield a proper operation for the error amplifier, the feedback factor β is calculated as 8/9. Then the R_{FB1} is adjusted to 90 kΩ and the R_{FB2} is 720 kΩ to yield a quiescent current through the feedback network about 1.1 uA.

Parameter	Value
R_{FB1}	90 kΩ
R_{FB2}	720 kΩ
β	0.89
I_q	1.1 uA

Table 3.3: Feedback network parameters

Since the pass transistor and the feedback network are predetermined. From simulation, the input swing of the pass transistor under all load conditions are defined. Under different load condition, the source gate voltage Vsg is shown in Table 3.4.

V_{sg}	I_{out}	Region
140.7 mV	0 A	Subthreshold
392.9 mV	1 mA	Subthreshold
564.6 mV	25 mA	Saturation
696.7 mV	100 mA	Saturation

Table 3.4: Operation region under different load conditions

The threshold voltage V_{th} of the pass transistor is 514.9 mV so that the pass transistor under small load which is smaller than 25 mA in this paper is in subthreshold region. Assuming the source bulk voltage V_{sb} is 0 V, the subthreshold current equation is shown in 3.4 where q is the electronic charge, n is the subthreshold swing factor, K is Boltzmann's constant and T is the absolute temperature.

$$I_D \cong I_{D0}\frac{W}{L}e^{qV_{sg}/nKT} \tag{3.4}$$

It should be noticed that under subthreshold region, it shows an exponential relationship between the current of the pass transistor and the souce gate voltage. This relationship degrades the response of the LDO since it needs more current to react when there is a load transient in a short time. After defining the pass transistor and the feedback network, the error amplifier can be designed based on the fixed pass transistor.

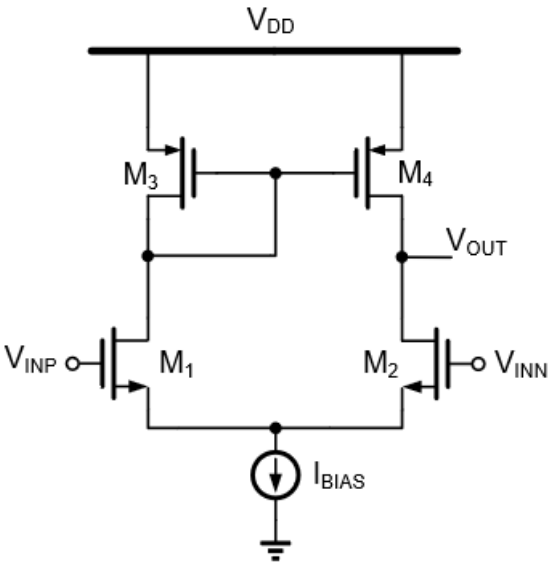

Figure 3.5: Simple OTA

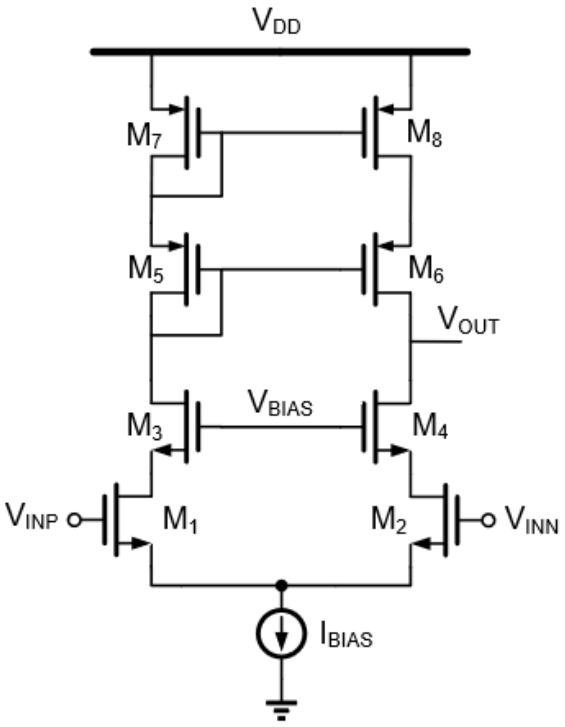

Figure 3.6: Cascode OTA

3.4 Gain-Compensated Error Amplifier

The design of the error amplifier is based on the predetermined pass transistor and the requirement of the open-loop gain under small quiescent current. Since in TSMC 40 nm technology the supply voltage is 1.1 V, the input swing and output swing is really limited so the topologies of the error amplifier are restricted. To make sure the error amplifier can have a larger input and output swing, the transistors in error amplifier should have a low threshold voltage. Then the models for the PMOS and NMOS transistors in the error amplifier are pch_lvt and nch_lvt.

Shown in Fig. 3.5, the simple OTA is composed of an NMOS input pair and an active PMOS load. The gain of the simple OTA is limited by the output resistance $R_{O2} \parallel R_{O4}$. To achieve high gain, the architecture of an OTA is usually cascode or folded-cascode so that the output impedance is boosted to increase the gain of the opamp. See from the Fig. 3.6 and Fig. 3.7, the cascode OTA and low voltage folded-cascode OTA architectures are shown. The output resistance of the cascode

OTA is boosted to $Gm_4R_{O4}R_{O2} \parallel Gm_6R_{O6}R_{O8}$ which is much larger than that of the simple OTA. However, it consumes too much headroom because of the cascoded PMOS current source load and makes it difficult for the next stage to design. The low voltage folded-cascode OTA combine the advantages of the simple OTA and the cascode OTA. It can achieve high output impedance and save more headroom than the cascode OTA. However, this low voltage folded-cascode OTA still consume a lot of headroom and it is not an ideal topology for an LDO in TSMC 40 nm where the typical supply voltage is 1.1 V.

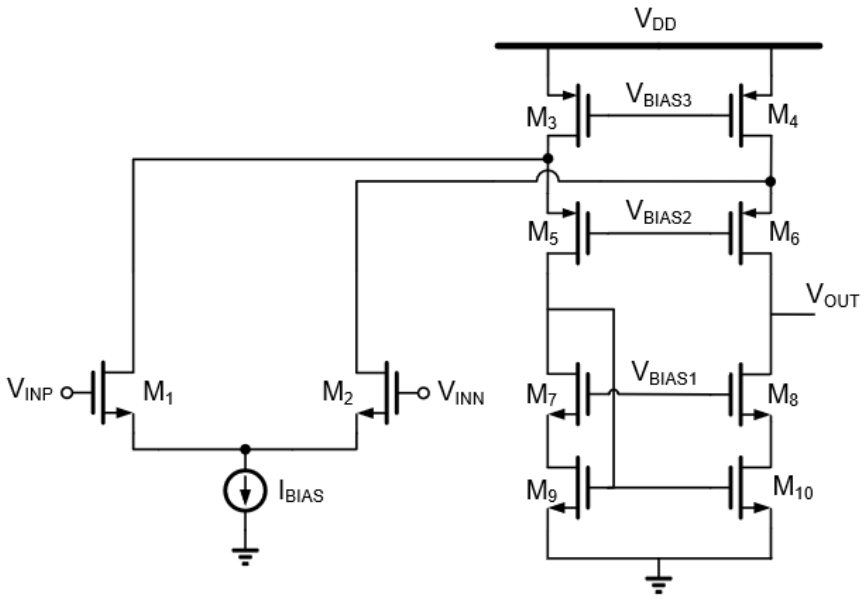

Figure 3.7: Low voltage folded-cascode OTA

Therefore, the low supply voltage limits the topologies for the error amplifier. The simple OTA may have large gain as a result of large output resistance caused by the small bias current. However, the biggest problem of this topology is that any supply variation or noise can be coupled to the gate of the diode-connected transistor M_3 and amplified by M_4 to the output. This effect is worse because it is inside the first stage and will be amplified by the second stage and the pass transistor. Fig. 3.8 shows the single-ended two-stage error amplifier, this topology has multiple advantages over the single-ended simple OTA with a large open loop gain. One advantage is improving the

first stage output impedance because of the common mode feedback resistors R_{CMFB} eliminating the differential voltage at the common gate node at the same time[10]. The first stage output resistance becomes $R_{CMFB}//r_{O1}//r_{O2}$ instead of diode-connected resistance $1/Gm_{02}$. Moreover, the PMOS load transitors define the common mode voltage to the gate of the second stage with locally feedback through the CMFB resistors. This architecture makes the first stage error amplifier have more gain without additional bias circuit for the active load transistors. Furthermore, it consumes little output swing so that the transistors in the error amplifier can maintain saturation region even when the load current is very small causing the gate voltage of the pass element close to supply voltage.

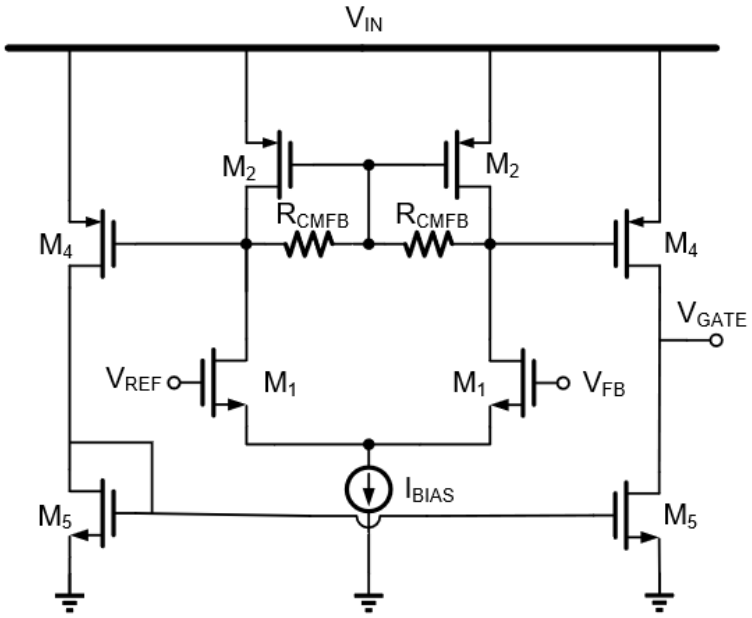

Figure 3.8: Two-stage error amplifier schematic

The transfer function of this architecture is shown in equation 3.5. The error amplifier should be designed to yield a gain around 40 dB to make sure the LDO have a gain larger than 50 dB at all loading conditions since the pass transistor can provide about 10 dB gain from the simulation results. The gate capacitance of the pass transistor is 2.13 pF from the simulation. Assuming the

gain bandwidth product is 5 MHz, the output resistance of the error amplifier should be calculated as 7.47 MΩ to have the dominant pole at around 10 kHz. The gain of the second stage error amplifier determines the transconductance of the second stage amplifier. Assuming the second stage gain is 20 so that gm_2 is calculated as around 3 uA/V. Then the first stage gain is 5 and assuming the transconductance is the same with that of the second stage, the output resistance can be determined. Therefore, the W/L can be decided with the assumption of V_{DS} and I_{DS} from the equation 2.4. Since the quiescent current should be minimized to yield a longer standby mode time, the bias current going through the two stage error amplifier is designed to be 1 uA. The ratio between the first stage and the second stage is 1:1. The width length ratio of the transistors in the error amplifier is less than one so the length cannot be the minimal value which is 40 nm.

$$H = \frac{Gm_1(r_{o1} \parallel r_{o2} \parallel R_{CMFB})}{1 + s(r_{o1} \parallel r_{o2} \parallel R_{CMFB})C_{gg4}} \cdot \frac{Gm_4(r_{o4} \parallel r_{o5})}{1 + s(r_{o4} \parallel r_{o5})C_{ggp}} \tag{3.5}$$

The simulated gain of the two-stage error amplifier is 32.75 dB and the gain of the pass transistor only contributes 9 dB to 18 dB depending on the load condition, so the total gain of the LDO is 41.2 dB at 100 mA and 50.15 dB at 1 mA. In order to achieve more than 50 dB at all load conditions. There should be a method of gain compensation for the error amplifier without consuming too much power.

3.4.1 Gain Compensation with Cross-Coupled Negative Resistor

There are two basic ideas of achieving higher gain. The first one is increasing the bias current so that the transconductance gm is boosted. The other one is increasing the output impedance of the OTA. In this paper, since it is focused on achieving a high gain LDO with low power consumption, the bias current should keep low, then the output impedance should be enlarged to boost the gain. However, methods such as cascading transistors are not suitable for the low power supply technology.

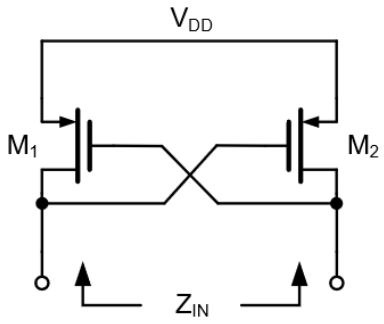

Figure 3.9: Cross-coupled pair

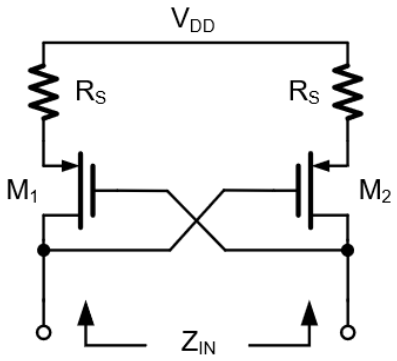

Figure 3.10: Cross-coupled pair with source degeneration resistors

A novel idea is proposed in this subsection. It is paralleling the common mode feedback resistors with a cross-coupled pair negative resistor to have a super large output impedance which is much more effective than the cascading transistors. As it is widely concerned, the cross-coupled pair is a bi-stable element which can amplify the signal very fast so it's widely used in digital circuit such as current-mode logic (CML) latches or sensing amplifiers[11]. This is the large signal characteristics of the cross couple pair. Considering the condition when the drain of the cross couple pair is very close to each other, the cross couple pair behaves as a negative resistor which is shown in Fig. 3.9. See from the drain of the cross couple pair, the equivalent resistance Z_{IN} is equal to$-2/gm$.

While this negative resistor serves many different applications such as LC voltage-controlled oscilator (VCO), this negative resistor can be used to boost the output resistance which can ideally achieve a large gain with very low current. The basic idea behind the resistance boosting is shown in equation 3.6.

$$R_{O1} = \frac{-2/gm \times R_{eq}}{-2/gm + R_{eq}} \tag{3.6}$$

However, the single cross-coupled pair as a negative resistor may cause unstable issue under different severe corners. Therefore, the sensitivity of the cross-coupled pair needs to be decreased to make sure the stability of the LDO. Shown in Fig. 3.10, a cross-coupled pair with source

degeneration resistors is introduced to minimize the sensitivity of the LDO. The equivalent negative resistance Z_{IN} is shown in equation 3.7. If the product of transconductance of the cross-coupled pair and the degeneration resistors is much larger than 1, the equivalent negative resistance is independent of gm of the cross-coupled pair making this approach much more robust.

$$Z_{IN} = -\frac{2(gmR_s + 1)}{gm} \tag{3.7}$$

The gain-enhanced two-stage error amplifier is shown in Fig. 3.12. From the schematic of the two-stage gain compensated error amplifier, the M_3 transistors act as the cross-coupled pair to boost the first stage output resistance with degeneration resistors minimizing the sensitivity. The transfer function of this gain-compensated error amplifier is shown in equation 3.8. The negative resistance of the cross-coupled pair makes the denominator of the equivalent resistor smaller which amplifies the first stage output resistance.

$$H = \frac{Gm_1\big[r_{o1} \parallel r_{o2} \parallel R_{CMFB} \parallel -(1 + Gm_3R_s)/Gm_3\big]}{1 + s\big[r_{o1} \parallel r_{o2} \parallel R_{CMFB} \parallel -(1 + Gm_3R_s)/Gm_3\big]C_{gg4}} \cdot \frac{Gm_4(r_{o4} \parallel r_{o5})}{1 + s(r_{o4} \parallel r_{o5})C_{ggp}} \tag{3.8}$$

The negative resistance can be defined by sizing the finger ratio between M_3 and M_4 transistors to control the current through the cross-coupled pair then control the equivalent negative resistance. If the value of the first stage output resistance is very close to that of the controlled cross-coupled pair, the equivalent resistance of the first stage output can be ideally close to infinity. It should be noticed that the negative resistance should be larger than the output resistance so that the gain of the first stage will not be inverted to make the LDO unstable. Fig. 3.11 shows the relationship between the common mode feedback resistors R_{CMFB} and the open loop gain of the LDO when the output load is 0 A. The maximum gain it can achieve ideally is 75.592 dB when R_{CMFB} is equal to 677 kΩ. The left region is the stable region for an LDO while the right region is the unstable region. From the simulation, the phase is initially 180° less than that in stable region if the value of common feedback resistors excess the critical point. So the design of the common mode feedback resistors is essential to make the LDO have a larger gain and stable. In order to

make sure the stability of the LDO, the common mode feedback expected resistance should be 30% of the critical value so the resistance value is 470 kΩ.

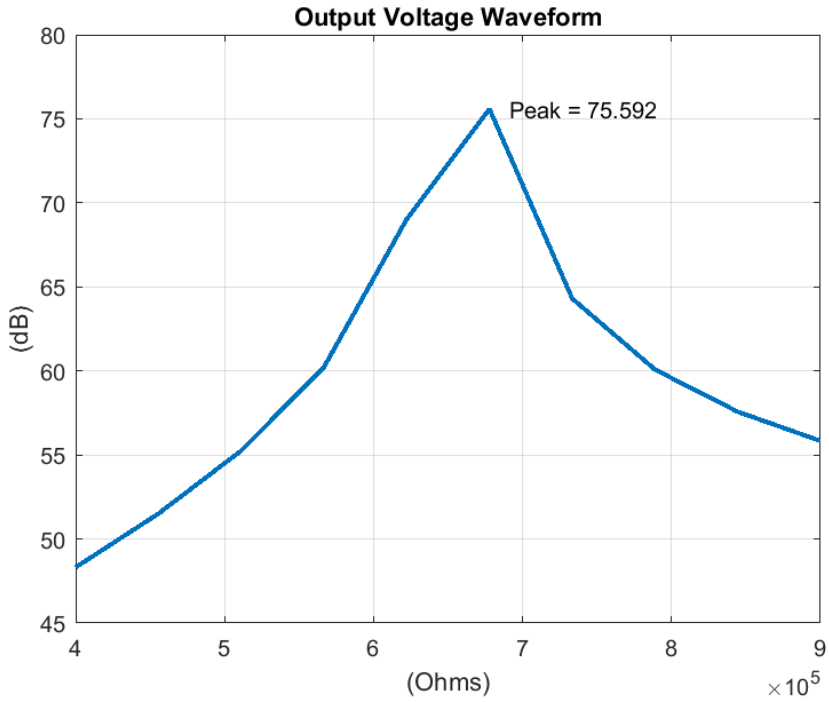

Figure 3.11: Relationship between gain and common mode feedback resistors

Under steady-state conditions, the gate voltage of M_2 transistors is fixed by the current through them and the transconductance of M_3 transistors is also determined by the current through them. Sizing the finger ratio between M_2 and M_3 is able to adjust the negative resistance of the cross-coupled pair. Transistors M_4 and M_5 constitute the second stage of the error amplifier. The quiescent current through the first stage and the second stage are 775 nA and 612 nA. The total quiescent current the error amplifier consumes is only 1.38 uA and the total gain of the two-stage error amplifier is 40.4 dB. Without the cross-coupled pair negative resistor, the two stage error amplifier can only achieve 32.7 dB. Instead of consuming more power, the negative resistor helps the error amplifier to have 10.7 dB (243% increase) more gain. The limitation of this method is area because the common mode feedback resistor need to be large to have a large gain. In the meanwhile, the

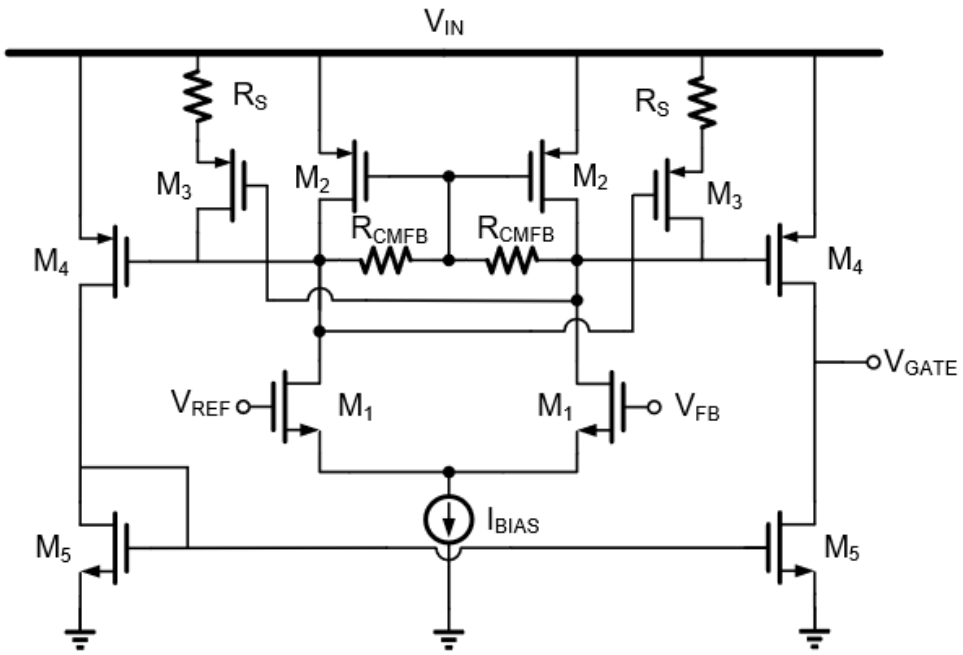

Figure 3.12: Two-stage gain compensated error amplifier

source degeneration resistors also need to be large to minimize the sensitivity of the cross-coupled pair to make the LDO stable even under different corners.

Devices	Size	Devices	Size
M_1	120 nm/480 nm	M_2	120 nm/720 nm
M_3	240 nm/720 nm	M_4	250 nm/720 nm
M_5	120 nm/720 nm		
R_{CMFB}	470 kΩ	R_S	200 kΩ

Table 3.5: Error amplifier parameters

3.5 Transient Response Compensation

Transient response enhancement is really important for an LDO. Without any transient response compensation circuit, the output undershoot is huge which may cause severe effects of the analog

and digital blocks after the LDO. The transient response specification is usually defined as the maximum allowable undershoot for a output current load changing from low load to maximum load. From the equation 2.10, the undershoot of an external capacitor-less LDO during transients is much larger than that of a traditional LDO because there is no large capacitor at the output. Previous work introduced a buffer stage with low output impedance to drive the pass transistor[12]. This buffer stage combined with the large parasitic gate capacitor contributes to a pole at much higher frequency. The most important characteristics is that the buffer stage enhanced the transient response a lot. This buffer stage is not suitable in this work because in 40 nm technology the size of the pass transistor is relatively small which is about 1.1 pF at the gate without miller effect. A buffer stage cannot improve the transient response a lot in this case and it will push the dominant pole at the gate into much higher frequency which deteriorates the phase margin. Milliken in 2007 proposed a current amplifier sensing the output undershoot and transforming the voltage to a large current to escalate discharging the gate capacitor of the pass transistor. However it needs additional large bias current for the current amplifier which increase a lot of power. This paper will introduce a different transient-enhanced circuit with a RC differentiator, an inverter and a discharging NMOS transistor.

An ideal transient-enhanced circuit should include a fast sensing circuit which consumes little power or even no power and a slew rate enhanced circuit to boost the slew rate at the gate of the pass transistor to discharge or charge the large gate capacitor in a very short time. The basic concept is shown in Fig. 3.14. Since the error amplifier consumes only 1.3 uA and the gate parasitic capacitance is about 3.5 pF, the slew rate is calculated as 0.37 V/us which limits the transient response of the LDO. Furthermore, the poles inside the two-stage error amplifier also slow the response during transients. The sensing circuit is needed to sense the output spikes and boost the slew rate to enhance the transient response.

In this paper, two different transient-enhanced topologies are compared. The analog comparator shown in Fig. 3.16 can achieve faster transient response and reduce the undershoot during transients. However, there are two inputs going into the comparator: the output node of the LDO

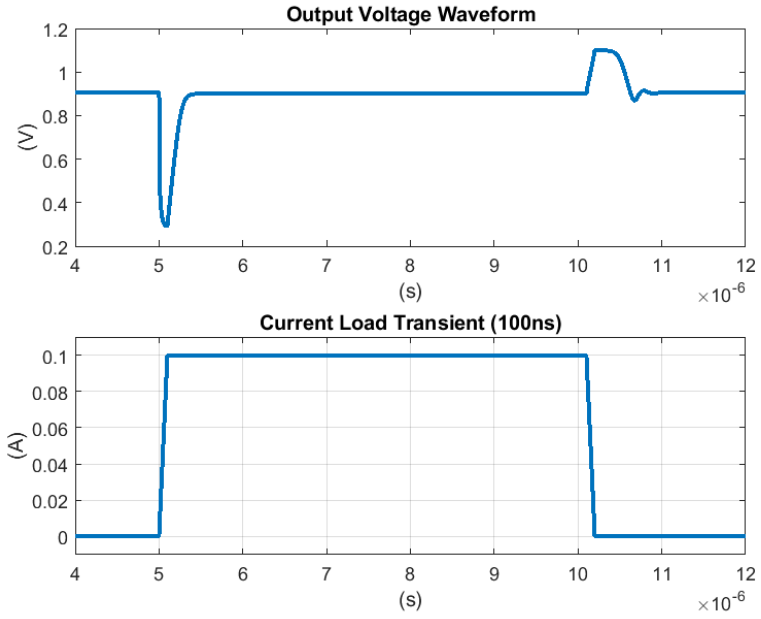

Figure 3.13: Uncompensated transient response

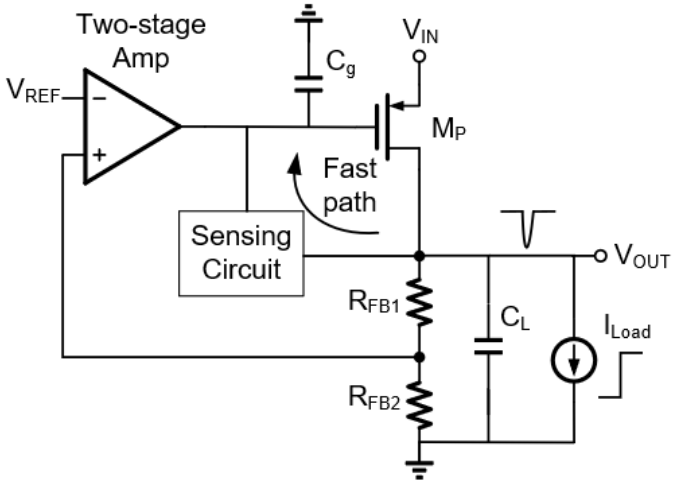

Figure 3.14: Transient-enhanced circuit concept

and a reference voltage. Since the discharging NMOS transistor M_g should be in shut down mode during steady-state condition, the V_{ref} should be smaller than V_{out} to output a high voltage for the inverter to shut down M_g. This makes the comparator's input does not match each other all the time and this also consumes power and suffer the process variation which may cause the inaccuracy of

the comparator. Therefore, the RC differentiator is proposed in this work and it is able to achieve very decent job on sensing the output spikes without consuming too much power.

Shown in Fig. 3.17, the proposed differentiator is composed of a high pass RC filter and an inverter followed by a discharging NMOS transistor connected to the gate of the pass element. In order to make the differentiator only react to the transients, the RC high pass filter which shown in Fig. 3.15 is used to filter out output dc component. For any change at the input of the differentiator, the sensing capacitor C_S converts the voltage difference into current which transformed to voltage change by R_S. The voltage variation can be calculated in equation 3.9.

$$\triangle V_2 = R_S \cdot C_S \frac{\triangle V_1}{dt} \tag{3.9}$$

The RC differentiator is better than an analog comparator because it does not consume power and it is really fast for the load transients. However this differentiator only enhance the slew rate when there is a load changes from 0 A to 100 mA causing the large undershoot. The overshoot is limited by the supply voltage 1.1V so that the maximum overshoot is only 200 mV. In order to reduce the large undershoot and power consumption, the differentiator in this work combined with an inverter and a discharging NMOS transistor is proposed to achieve a better transient response.

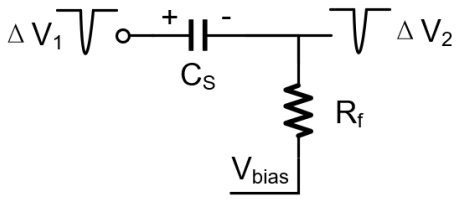

Figure 3.15: RC differentiator

The bias voltage for the inverter input V_{bias} is set to be high so that the inverter output a zero voltage to shut down the NMOS transistor when the circuit is operating in steady-state. However

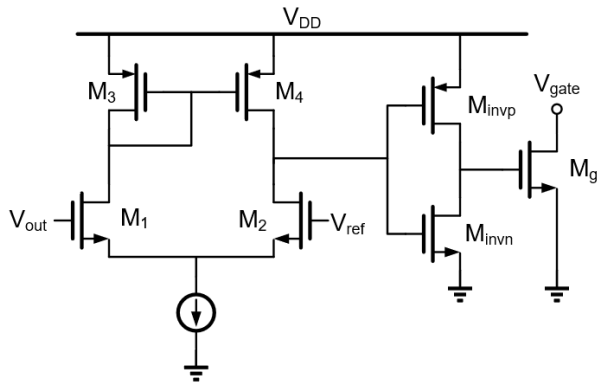

Figure 3.16: Analog comparator

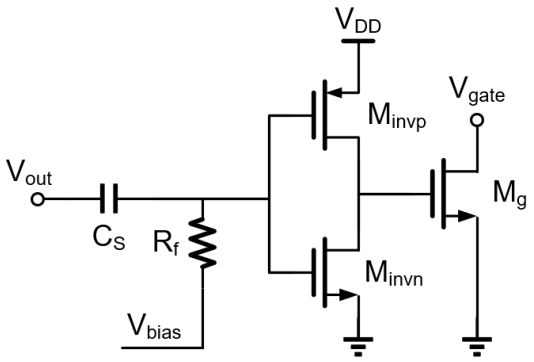

Figure 3.17: Proposed passive differentiator

it cannot be that high because whenever there is a output undershoot the RC differentiator should be able to detect it and reach below the trip point of the inverter immediately. If the bias voltage is set too high, the inverter can only invert the output when the undershoot is very large which is not suitable. Furthermore, the bias voltage can not be too small as well because it is closely related to the leakage current of the discharging NMOS transistor M_g. If the bias voltage is set very low, the leakage current of M_g is large and it will affect the stability of the LDO when it is operating in steady-state condition. As for the NMOS discharging transistor M_g, it should have a threshold voltage as high as possible to minimize the leakage voltage in steady state. The differentiator should not affect the steady state of the LDO otherwise the loop gain and the location of the dominant pole will be changed.

Devices	Size
C_S	1 pF
R_S	10 kΩ
V_{bias}	671.2 mV
M_{invp}	240nm/120nm
M_{invn}	120nm/120nm
M_g	2.4um/40nm

Table 3.6: Feedback network parameters

The size of the inverter should be considered because it affects the trip point and the power consumption. When the load is increasing from a low load condition to a full load condition in a short span of time (100 ns), the output voltage is decreasing dramatically which create a large voltage undershoot. This is detected by the RC differentiator and invert the inverter's output voltage to turn on the M_g and then accelerate discharging the gate and provide enough load current from the pass element. The size of transistors and passive devices in the differentiator to yield a best transient response of the LDO is shown in Table 3.6.

3.6 Stability Analysis

Different from the traditional LDO with a dominant pole at the output, the external capacitor-less LDO has a very small on-chip capacitor which make the dominant pole at the gate of the pass element. Besides, the non-dominant poles at the output and inside the two-stage error amplifier have an important effect on the stability of the LDO. The locations of all poles inside the LDO is shown in Fig. 3.18.

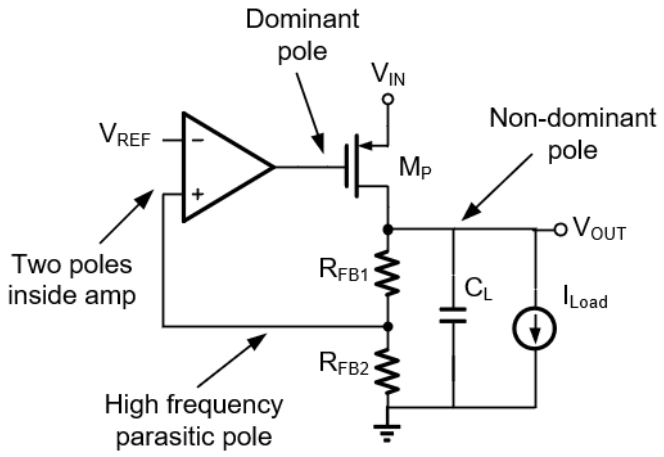

Figure 3.18: Capacitor-less LDO poles location

The stability of an LDO is critical because there are many aspects which may make the LDO

unstable. The first one is the effect of the output load. The impedance of the pass transistor changes with the current through it. When the load current is zero, the impedance is very large which push the output pole to a low frequency and the output pole is at high frequency if the load current is maximum, which makes the compensation for the LDO sophisticated. The second one is the presence of the large parasitic capacitor at the gate. Because of the requirement of low dropout voltage with a large output load current, the size of the pass transistor is very large so that the parasitic capacitor is large as well. This gate parasitic capacitor and the large output resistance of the error amplifier compose the dominant pole for the external capacitor-less LDO. Due to the miller effect of the parasitic gate drain capacitance C_{gd}, the effective gate capacitance is more than the original gate capacitance and partially dependent on the output load. As a result of the gate drain capacitance C_{gd}, a RHP zero at high frequency is embeded in the open loop and it should be placed far above the unity gain frequency to ensure the stability of the LDO. Furthermore, the poles inside the error amplifier also need to be placed beyond the unity gain frequency for LDO to have a good phase margin.

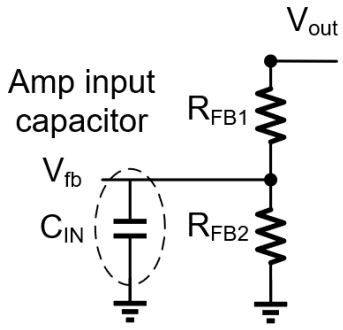

Figure 3.19: Parasitic capacitor in feedback network

It should be noticed that the feedback network also has a parasitic pole at the node between two feedback resistors. Shown in Fig. 3.19, the C_{IN} stands for the input parasitic gate capacitor of the first stage error amplifier. Since the size of the transistors in the error amplifier is small, the input parasitic capacitor is in the range of fF so that the parasitic pole is at high frequency. The transfer

function of the feedback network is shown in equation 3.10. The first part is DC gain and the second part is the AC gain caused by the parasitic pole. Though the parasitic pole in the feedback network is at high frequency, it can affect the frequency response and the transient response to some extent.

$$H_{fb} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{1}{1 + s(R_{FB1} \parallel R_{FB2})C_{IN}} \tag{3.10}$$

The transfer function of the gain-compensated two-stage error amplifier is shown in equation 3.11. Gm_1 is the first stage transconductance, r_{o1} is the first stage output resistance, r_n is the cross-coupled pair negative resistance and C_{o1} is the first stage output capacitance. Similarly, Gm_2, r_{o2} and C_{o2} stands for the second stage transconductance, output resistance and output capacitance. C_{o2} includes not only the output capacitance of the second stage error amplifier but also the parasitic gate capacitance of the pass transistor.

$$H_{amp} = \frac{Gm_1 r_{o1} \parallel r_n}{1 + s(r_{o1} \parallel r_n)C_{o1}} \cdot \frac{Gm_2 r_{o2}}{1 + s r_{o2} C_{o2}} \tag{3.11}$$

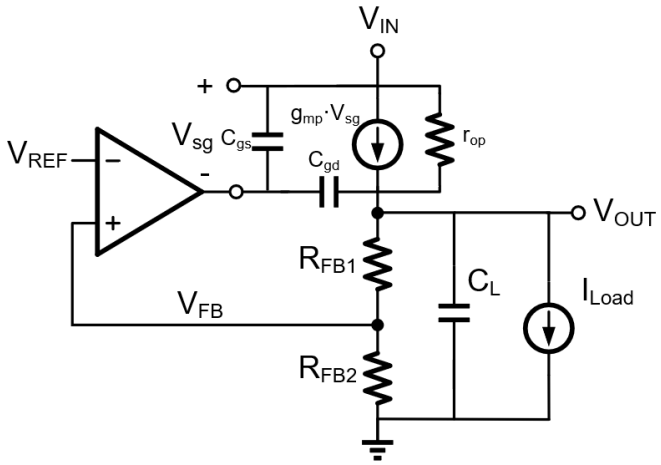

Figure 3.20: PMOS LDO pass element small signal model

The small signal model of the PMOS pass transistor in the LDO is shown in Fig. 3.20. The pass transistor stage is a common source amplifier whose gain is dependent on the load current. The miller capacitor C_{gd} creates one RHP zero for this common source stage. R_{out} is the total equivalent output resistance of the LDO, which includes the feedback resistance, output load resistance and the equivalent resistance of the PMOS pass transistor. As a result of the load changes, the total output resistance varies a lot affecting the output pole greatly. The transfer function of this stage is shown in equation 3.12.

$$H_p = -\frac{g_{mp}R_{out}(1 - s\frac{C_{gd}}{g_{mp}})}{1 + sR_{out}C_{out}} \tag{3.12}$$

The block diagram of the proposed LDO is shown in Fig. 3.21. It can be seen that there are

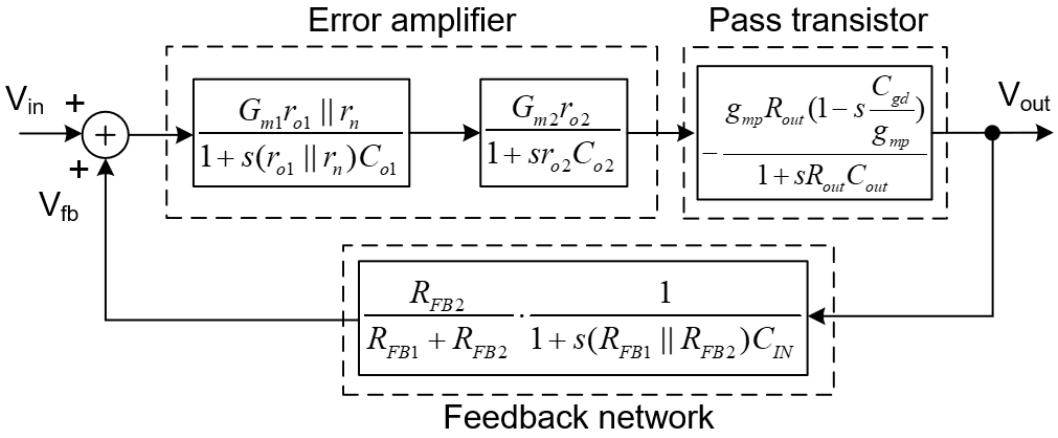

Figure 3.21: Block diagram of the proposed LDO

four poles and one RHP zero in this LDO loop. Due to the cross-coupled negative resistor, the equivalent output resistance of the first stage is boosted which makes the first stage output pole move to a lower frequency. Since the parasitic pole inside the feedback network resides in very high frequency, the effect of this pole is ignored for the following analysis. The complete open

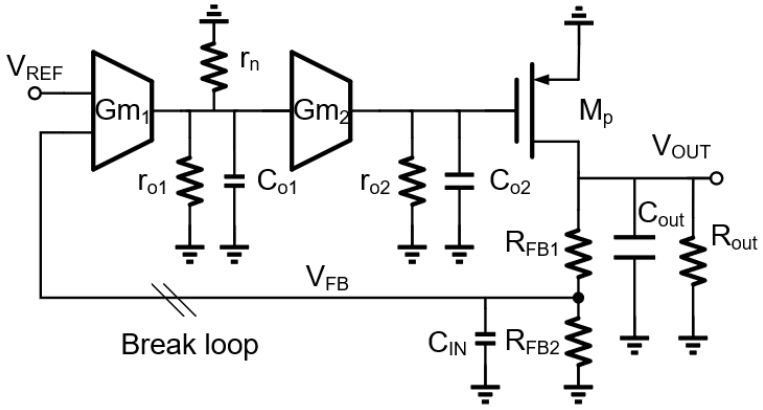

Figure 3.22: AC open-loop simulation circuit

loop transfer function of the LDO is shown in equation 3.13.

$$H = -\frac{R_{FB2} g_{mp} R_{out} Gm_1 (r_{o1} \parallel r_n) Gm_2 r_{o2} (1 - s\frac{C_{gd}}{g_{mp}})}{(R_{FB1} + R_{FB2})(1 + s(r_{o1} \parallel r_n)C_{o1})(1 + sr_{o2}C_{o2})(1 + sR_{out}C_{out})} \tag{3.13}$$

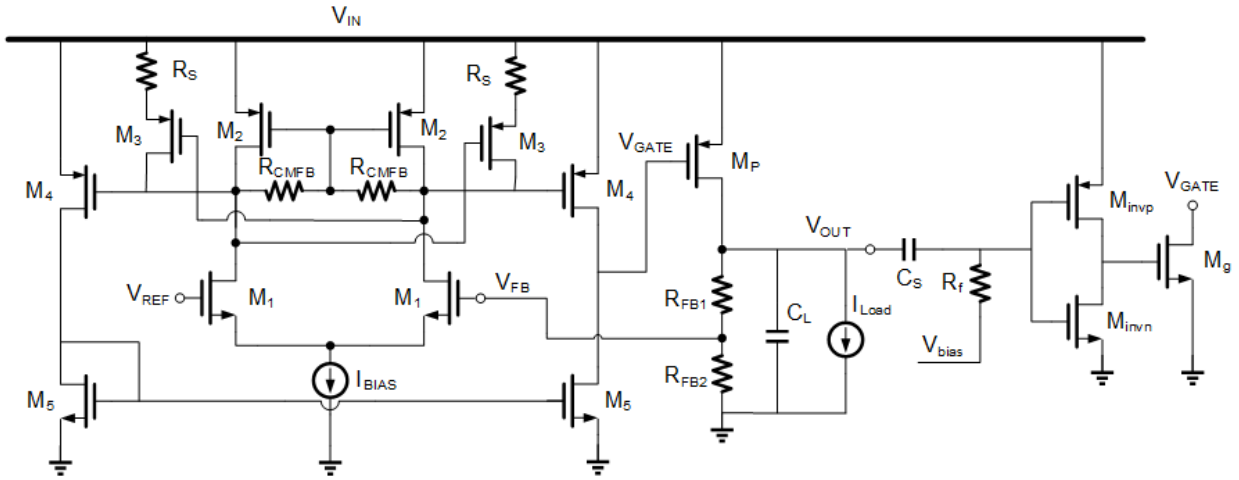

Figure 3.23: Proposed LDO transisitor level design

A widely used method of achieving good stability at all loading conditions is to insert an LHP zero to cancel the second pole which is shown in Fig. 3.25. The miller capacitor in series with a

resistor which contributes to a LHP zero is helpful for stabilizing the LDO. However the zero is fixed and the second non-dominant pole moves more than one decade. This compensation solves the stability issue at 0 A load condition but sacrifices the bandwidth of the system. The phase margin at 0 A load is not critical (more than 45°) because applications such as telephone does not need that accuracy with very good phase margin when it is on stand by mode. As long as the output voltage is close to the target voltage, the transient response is more important. Therefore in this work, there is no compensation for the low load condition. The LDO has 55° phase margin when the output load is 1 mA. As the load current increases, the output pole is pushed to much higher frequency, the phase margin increases to 79.3° when the output load is 100 mA.

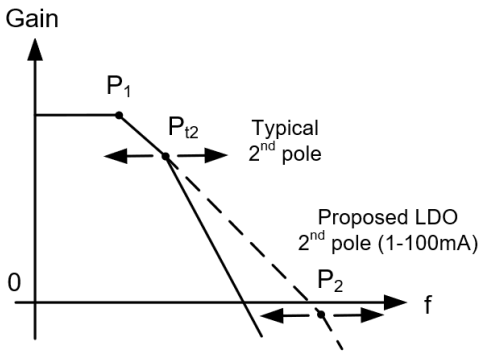

Figure 3.24: Capacitor-less LDO output pole movement

Shown in Fig. 3.25, the capacitor in series with a nulling resistor across the gate and drain of the pass transistor makes the RHP zero changes to LHP. From equation 3.14, the nulling resistor R_{null} pushes the RHP zero to LHP as long as R_{null} is larger than $1/g_{mp}$. Adjust the value of the capacitor and the nulling resistor then the frequency of the LHP zero will be modified to yield a better phase margin of the LDO. The approximation in equation 3.14 is because of the maximum load current condition where the transconductance is really large compared with the nulling resistor so that the

LHP zero moves more than one decade due to the load current.

$$\omega_z = \frac{1}{(1/g_{mp} - R_{null})C_c} \approx \frac{1}{-R_{null}C_c} \tag{3.14}$$

However, the miller compensation with a nulling resistor sacrifices a lot bandwidth which is critical to both transient response and PSRR at higher frequency. For this work, since the output pole is the second pole of the system and it is only at low frequency at less than 200 uA load. A miller compensation with nulling resistor is not suitable for compensating the phase margin of the LDO at very low load.

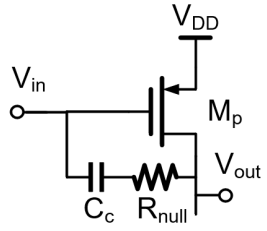

Figure 3.25: Miller compensation with a nulling resistor

The specific simulation results of the location of poles and zeros, UGF, phase margin and open loop gain from 0 A output load current to 100 mA are shown in Table 3.7. From the poles and zero movement as the load changes, the second pole is initially the output pole until the load increases to around 5 mA. The dominant pole is always at the gate of the pass transistor. It can be seen that the worst case happened when there is no output load current. The output pole is at 164.5 kHz and the unity gain frequency is at 727.95 kHz. Therefore the phase margin is only 7.6°. From the root locus for sweeping feedback factor at 0 A load current in Fig. 3.28, with 0.89 feedback factor the poles are in left half plane which means the LDO is stable at that specific feedback factor. The second pole merges with the first pole and goes to the right as a result of the third pole and the RHP zero. Since the RHP zero is proportional to the transconductance of the pass transistor, it resides

at lowest frequency when there is no load at the output. The poles and RHP zero movement as the output load increases from 0 A to 100 mA is shown in Fig. 3.26.

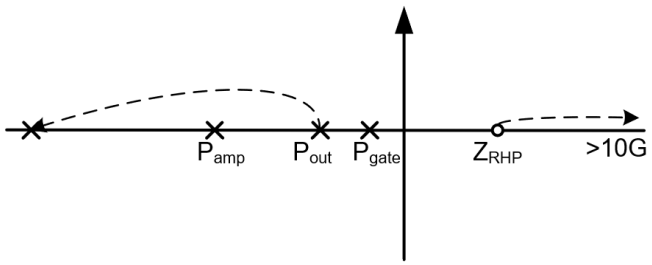

Figure 3.26: Poles and zero movement as load changes from 0 A to 100 mA

I_{out}	P_1	P_2	P_3	Z_{RHP}	UGF	PM	Gain
0 A	8.0k	151.0k	52.0M	8.06M	727.9k	7.6°	52.4 dB
1 mA	7.0k	13.6M	74.4M	>1G	10.3M	55°	64.2 dB
50 mA	9.9k	30.5M	424.6M	>10G	8.1M	75.9°	58.4 dB
100 mA	12.3k	31.8M	658.64M	>10G	6.3M	79.3°	54.3 dB

Table 3.7: AC simulation values

As the output load increases to 1 mA, the frequency response and the root locus are shown in Fig. 3.29 and Fig. 3.30. The frequency of the second pole which is at the output increases to 13.6 MHz while the frequency of the RHP zero increases well above 1 GHz. The effect of the RHP zero can be neglected in this case. As the feedback factor increases, the dominant pole and the second pole merge and split to infinity. The third pole repels the first and the second poles so the root locus is pushed to the right a little bit. However this effect is not that critical compared with that in no load condition. The frequency of the output pole keeps increasing as the output load current goes up to 100 mA. The output pole changes to the third pole and the second pole is inside the error amplifier. As it's shown in the table 3.7, the pole of the error amplifier is around 30 MHz when

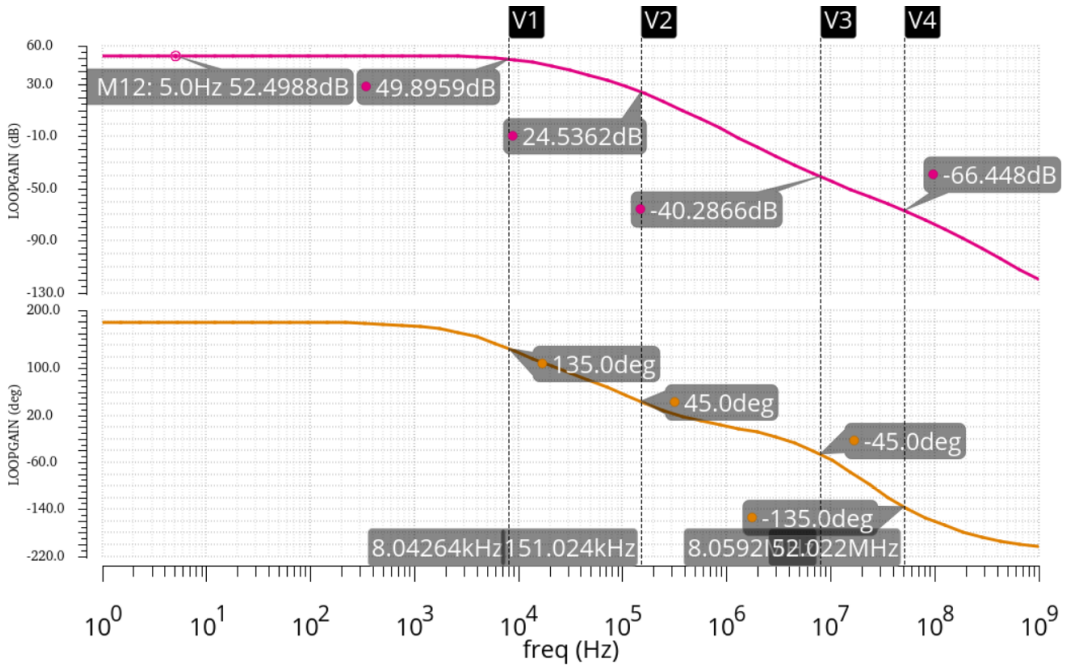

Figure 3.27: Frequency response for 0 A load

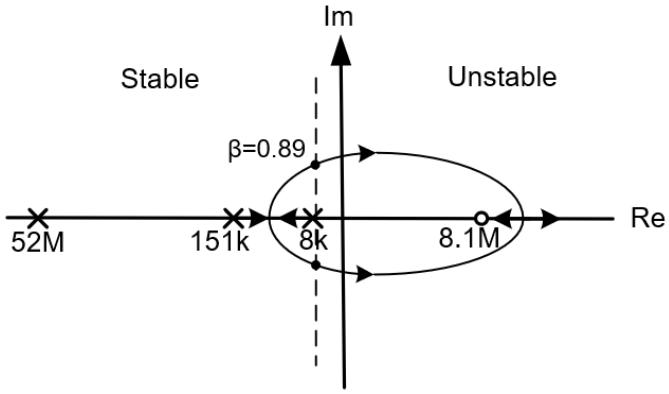

Figure 3.28: Root locus for sweeping feedback factor at no load

there is a high load at the output. Although the output resistance of the error amplifier's first stage is boosted to a large value, the gate capacitance of the error amplifier's second stage is really small (1.34 fF). The 30 MHz pole is around 10 times larger than the UGF so that it can be neglected with respect to the phase margin. The phase margin is increasing from 55.05° to 79.27° when the load is changing from 1 mA to 100 mA. From the Fig. 3.31, the output pole is at 658.64 MHz because

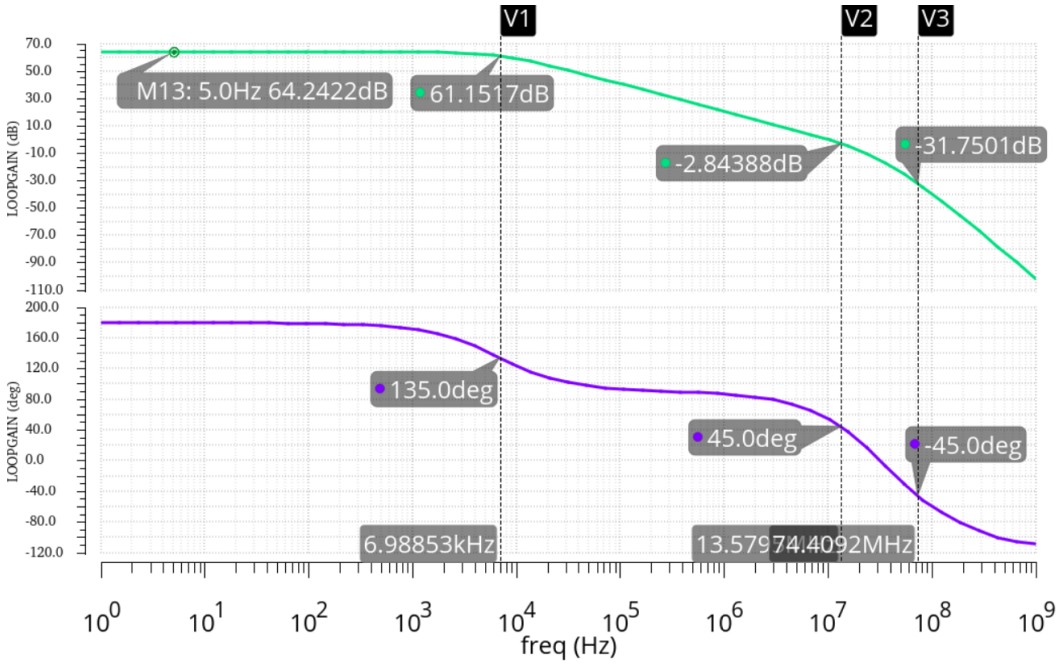

Figure 3.29: Frequency response for sweeping feedback factor at 1 mA load

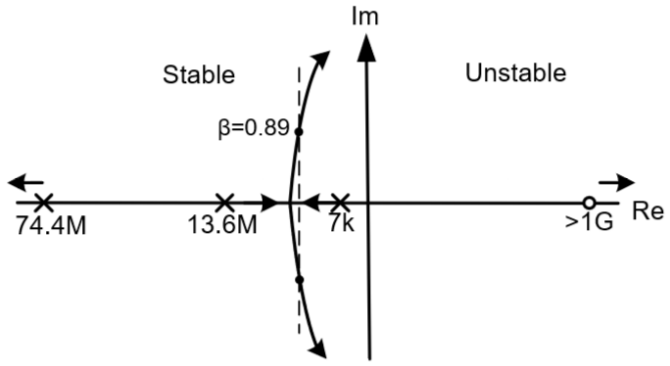

Figure 3.30: Root locus for 1 mA load

of the low impedance at maximum load condition. The root locus is nearly a straight line to the infinity from the merge point. We can conclude that the LDO has good phase margin when the load is above 1 mA. When there is no load at the output, the LDO still have 52.5 dB to regulate the output voltage around the target voltage which is 900 mV. Though the phase margin at no load condition is not that good, it's stable in this work. As long as the LDO can provide an accurate

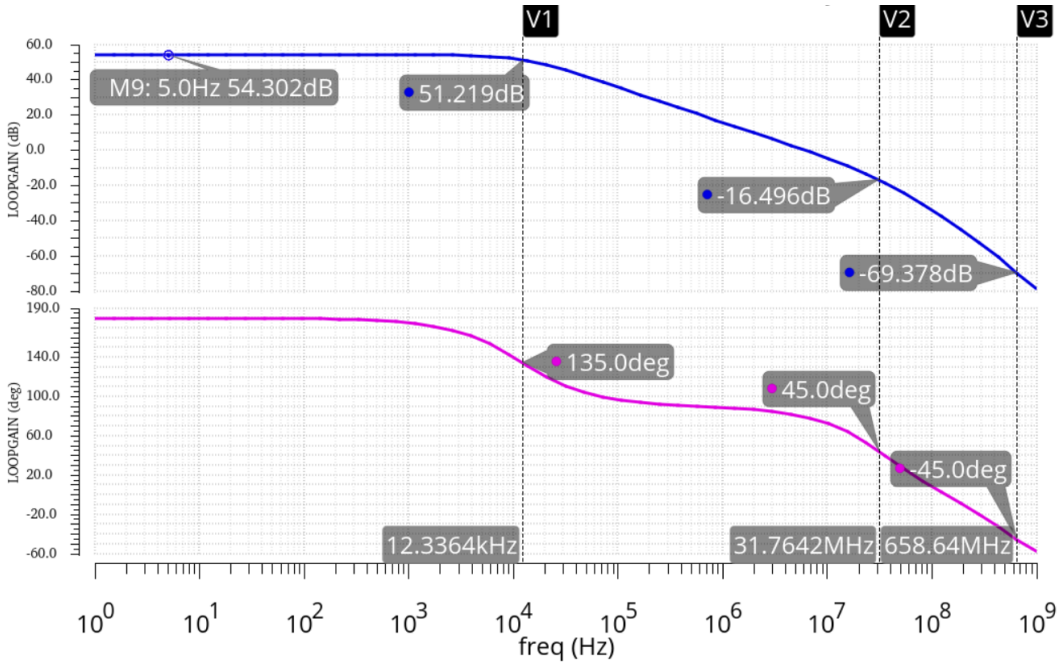

Figure 3.31: Frequency response for 100 mA load

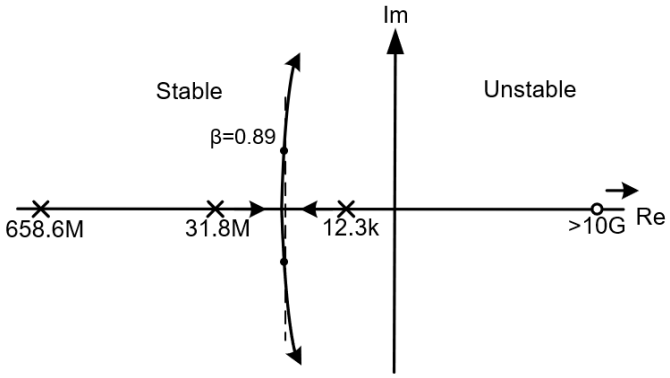

Figure 3.32: Root locus for sweeping feedback factor at 100 mA load

voltage in standby mode and has a fast transient response when there is an instant large output load transient, it's applicable for operation in most applications. For example, when our telephone is in standby mode, the LDO inside should be able to provide accurate voltage for the connected

modules but the phase margin is not that critical as long as it's stable.

$$H = \frac{-g_{mp}R_{out}Gm_1(r_{o1} \parallel r_n)Gm_2r_{o2}(1 - s\frac{C_{gd}}{g_{mp}})}{(1 + s(r_{o1} \parallel r_n)C_{o1})\big[(1 + sr_{o2}C_{o2})(1 + sR_{out}C_{out}) + sR_fC_sg_{mp}R_{out}g_{mg}R_{o2}(1 - s\frac{C_{gd}}{g_{mp}})\big]} \tag{3.15}$$

Since the differentiator is only working when the LDO is in dynamic state, AC response of the differentiator will be analyzed to make sure the stability of the LDO during transients. Fig. 3.33 shows the AC response of the differentiator. The gain increases with 20 dB per decade due to the zero at 0 Hz and stops at the parasitic pole of the differentiator. The speed of the differentiator is related to the parasitic pole so that the choice of the capacitor and the resistor needs careful consideration. The pole need to be beyond the gain-bandwidth product which is 6.4 MHz when the load is 100 mA. The capacitor is designed to be 1 pF and the resistor is 10 kΩ to yield a pole at 15.9 MHz.

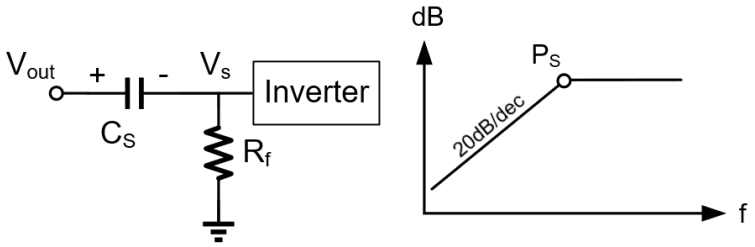

Figure 3.33: Differentiator AC response

From the Fig. 3.34, the differentiator can be modeled as a high pass RC filter with a non-inverting discharging NMOS transistor because of the inverter before the NMOS transistor. Assuming the parasitics of the inverter is ignored then the block diagram of the proposed LDO during transients is shown in Fig. 3.35. The transfer function of this model is shown in equation 3.15 assuming the feedback network is ignored for simplification.

To simplify the equation, some assumptions should be made. Since the analysis is based on the transient response when the output load is just clipping to 100 mA, the RHP zero is pushed to high

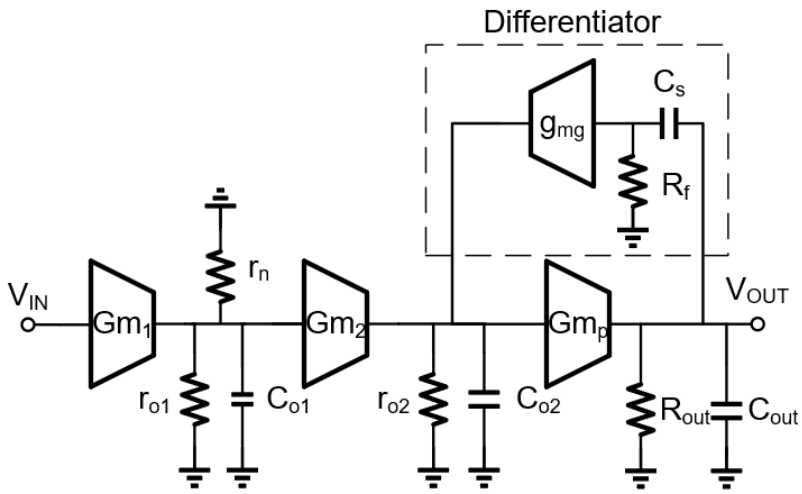

Figure 3.34: Small signal model of the proposed LDO during transients

frequency so that sC_{gd}/g_{mp} is ignored. Furthermore, the output pole is pushed to above 658 MHz when the output load is 100 mA so that $sR_{out}C_{out}$ is much less than 1. The simplified transfer function is shown in equation 3.16 assuming the feedback network is ignored for simplification.

$$H = \frac{-g_{mp}R_{out}Gm_1(r_{o1} \parallel r_n)Gm_2r_{o2}(1 - s\frac{C_{gd}}{g_{mp}})}{\big[1 + s(r_{o1} \parallel r_n)C_{o1})\big]\big[1 + s(r_{o2}C_{o2} + R_fC_sg_{mp}R_{out}g_{mg}R_{o2})\big]} \tag{3.16}$$

It can be seen that the dominant pole of the LDO moves to a lower frequency because of the differentiator. This effect is similar to the miller effect which pushes the dominant pole to a much lowever frequency and stabilize the whole system. When the output load is 100 mA, the second pole is at around 30 MHz which is 10 times more than the unity gain frequency which is around 3MHz. Therefore, the LDO can be seen as a single pole system and the differentiator pushes the dominant pole to a lower frequency, which does not affect the stability of the LDO.

From the block diagram including the differentiator, there are two loops: one is the main loop from the input going through the error amplifier, the pass transistor and the feedback network, the other one is the small loop consisting the pass transistor and the differentiator. At zero frequency, s is equal to zero so that the transfer function of the differentiator is zero. That is to say, at static state the main loop dominates because the differentiator blocks dc component by the high pass

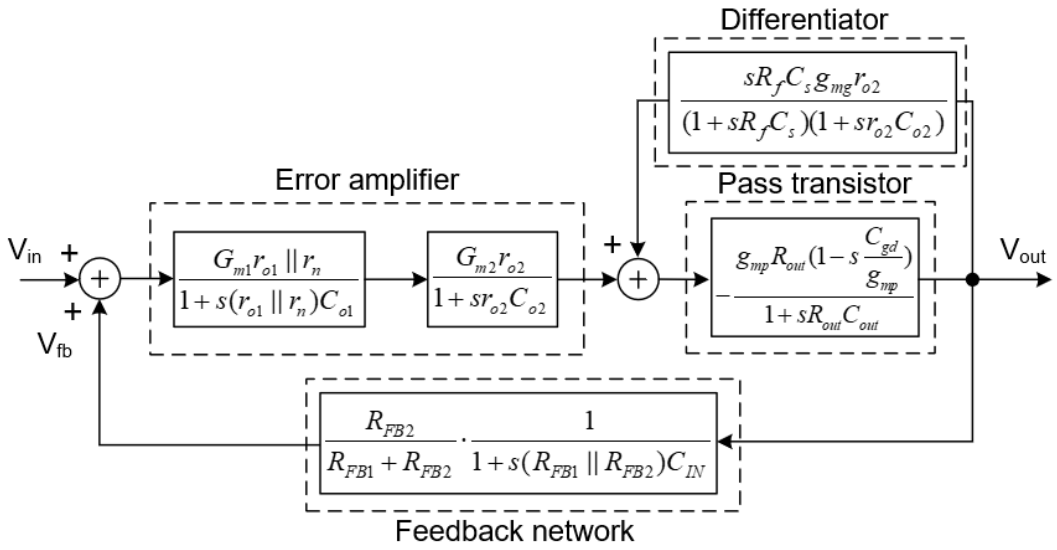

Figure 3.35: Block diagram of the proposed LDO during transients

RC filter. During transients which at high frequency, the small loop dominates because of the differentiator. The main loop is slower during transients because there are 4 poles which slow the transient response. Therefore, the small differentiator loop can react to the output transients and make the transient response faster than the main loop.

From the analysis above, the LDO is able to maintain stability under both the steady state condition and the load transient condition and have a transient response because of the differentiator loop. This is critical for the LDO's operation. The specifications of this LDO is shown in Table 3.8. The dropout voltage of this work is 200 mV and the quiescent current is only about 5.7 uA at all loading conditions. It need to be mentioned that the settling time during load transients is 9 us because of the overshoot. When the output load drops from full load to the no load, the output pole of the LDO moves to a really low frequency which makes the LDO have a small bandwidth. This small bandwidth slows down the settling phase of the LDO. The settling time for the 98.6 mV undershoot is only about 500 ns.

Parameter	Specification	Parameter	Specification
Input Voltage (V_{IN})	1.1 V	Output Voltage (V_O)	0.9 V
Output Current (I_O)	0-100 mA	Output Capacitor (C_O)	50 pF
Quiescent Current (I_Q)	< 5.7 uA	Open Loop Gain	> 50 dB
Line Regulation $(\Delta V_O/\Delta V_{IN})$	0.5%	Load Regulation $(\Delta V_O/\Delta I_O)$	3.89%
Transient $\triangle V_{out}$	98.6 mV	Settling Time (T_S)	< 9 us
PSRR @ 100kHz	-35.2 dB	PSRR @ 1MHz	-16 dB

Table 3.8: Specification of the proposed LDO

4. SIMULATION RESULTS

In this chapter, simulation results including the steady state performance and the dynamic state performance of the LDO are shown. In steady state, the LDO has three important characteristics: line regulation, load regulation and power supply rejection ratio (PSRR). In dynamic state, the bode plot of the LDO shows the stability of the LDO at different output load. The output load transient response and the input line transient response define the LDO's ability to maintain the constant output voltage under transients. Since the precision of the LDO is important to make sure it can function well under different process variation and corners. Monte carlo simulation and corner simulation are also shown in this chapter.

4.1 Steady-state Performance

In this section, the steady-state performance including frequency response, line and load regulation and PSRR are shown in the simulation results.

Frequency response is simulated with three different load conditions: 0 A, 1 mA and 100 mA. Since at 0 A load the requirement for the phase margin is not that mean, the gain is 52.4 dB with phase margin 7.6°. At 1 mA output load condition, the open loop gain is 64.2 dB with phase margin 55°. At 100 mA output load condition, the open loop gain is 54.3 dB with phase margin 79.3°. When the load current is increasing from 1 mA to 100 mA, the loop gain decreases from 64.2 dB to 54.3 dB, this is because the gain of the output transistor stage is inversely proportional to the load current. From 1 mA to 100 mA, the LDO can be seen as a single pole system which has phase margin close to 90°.

From Fig. 4.2, the load regulation of the LDO is simulated with output current from 0 A to 100 mA (full load range). It can be seen that the voltage changes about 3.89 mV from zero output to maximum output load. According to the equation 2.8, the load regulation can be calculated as

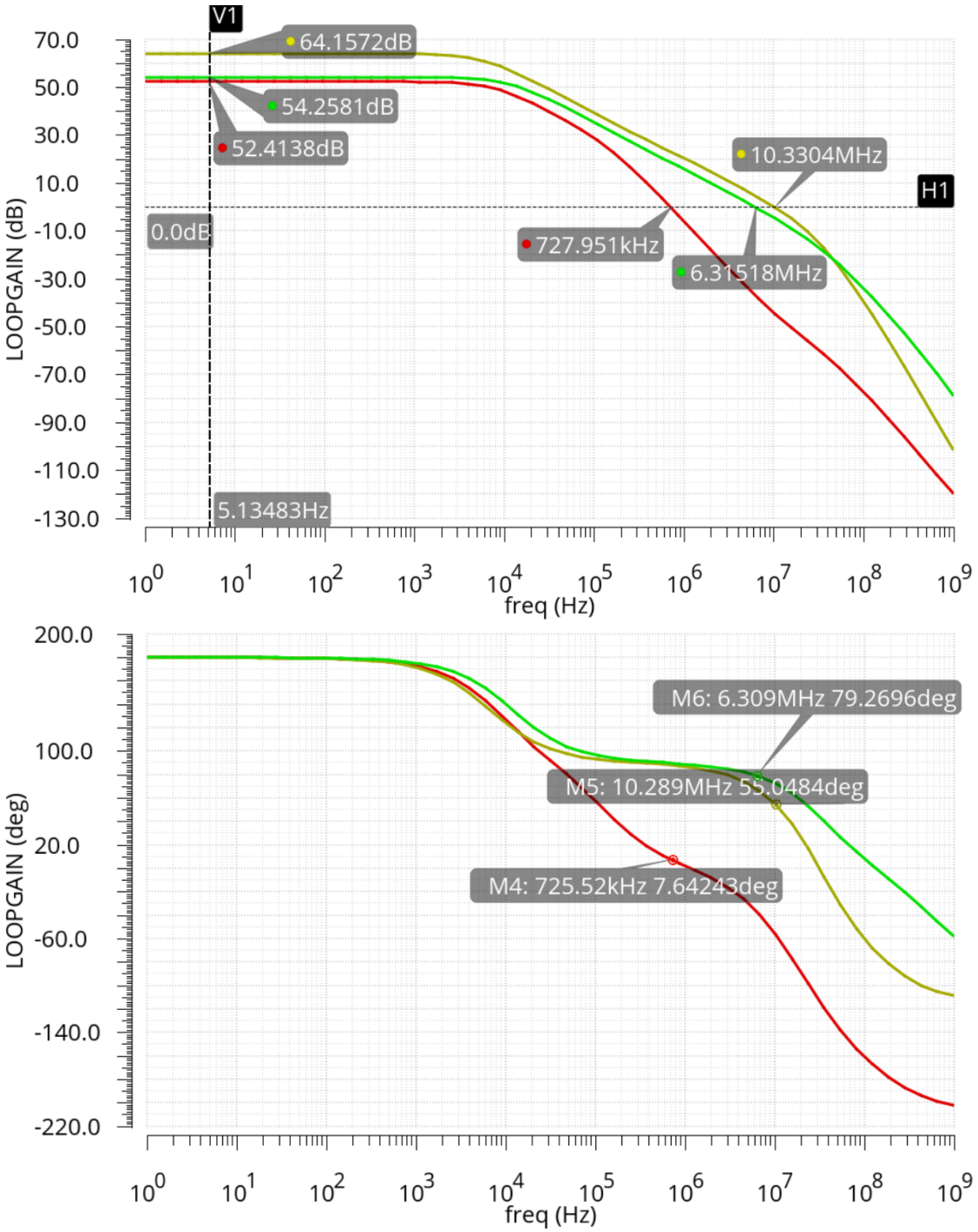

Figure 4.1: Frequency response for output load current at 0 A, 1 mA and 100 mA

3.89%. As for the line regulation testing, the worst case happens when the loop gain is the smallest which is at the zero load condition. The supply voltage of the LDO goes from 1.1 V to 1.5V to test

the line regulation of the LDO, the output voltage changes from 899.99 mV to 902.21 mV which is about 2.21 mV at 100 mA output load condition which is shown in Fig. 4.3.

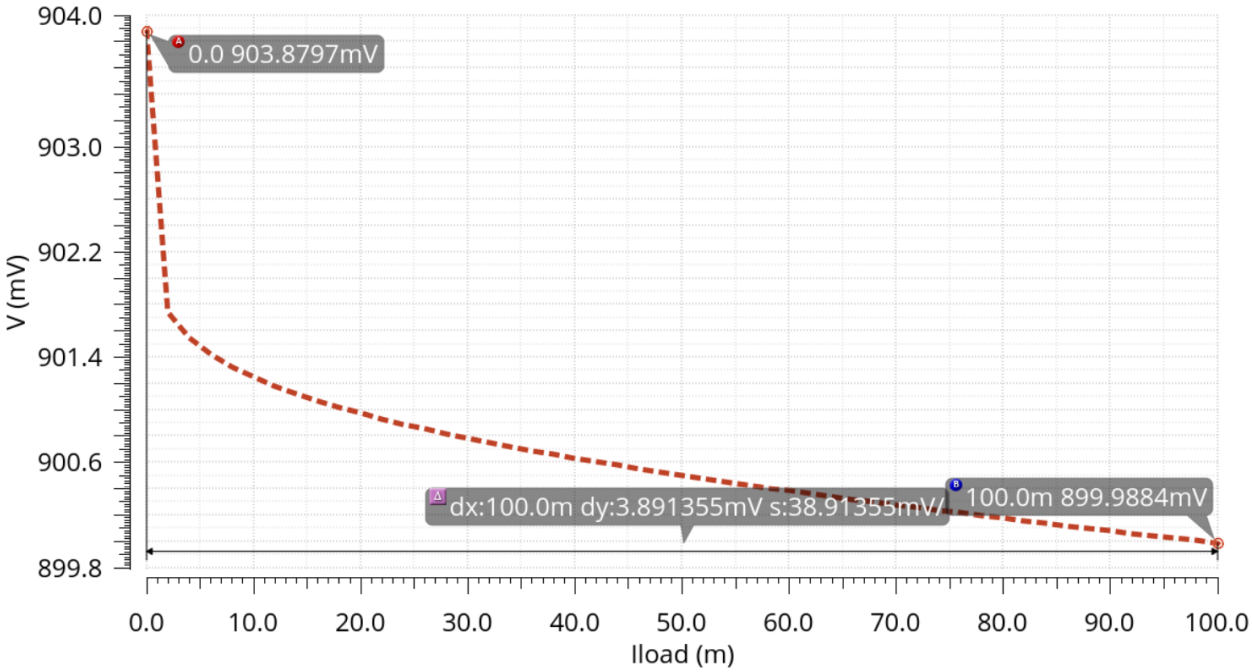

Figure 4.2: Load regulation with load from 0 A to 100 mA

The power supply rejection ratio (PSRR) is defined to stand for the ability for the LDO to reject the supply noise and ripple. Without any compensation circuit for the PSRR, the PSRR can be improved by the open loop gain of the LDO. From Fig. 4.4 shows the PSRR at three loading conditions: 0 A, 1 mA and 100 mA. At 1 mA output current load, the PSRR is the best case because of the large gain. The PSRR starts to decrease at the dominant pole frequency. At high frequency, the PSRR is highly dependent on the output impedance of the LDO.

Since the supply of the LDO is usually from the switching regulator at a certain switching frequency, the PSRR at higher frequency is essential. In this work, at 100 kHz, the PSRR is about -35 dB at worst case.

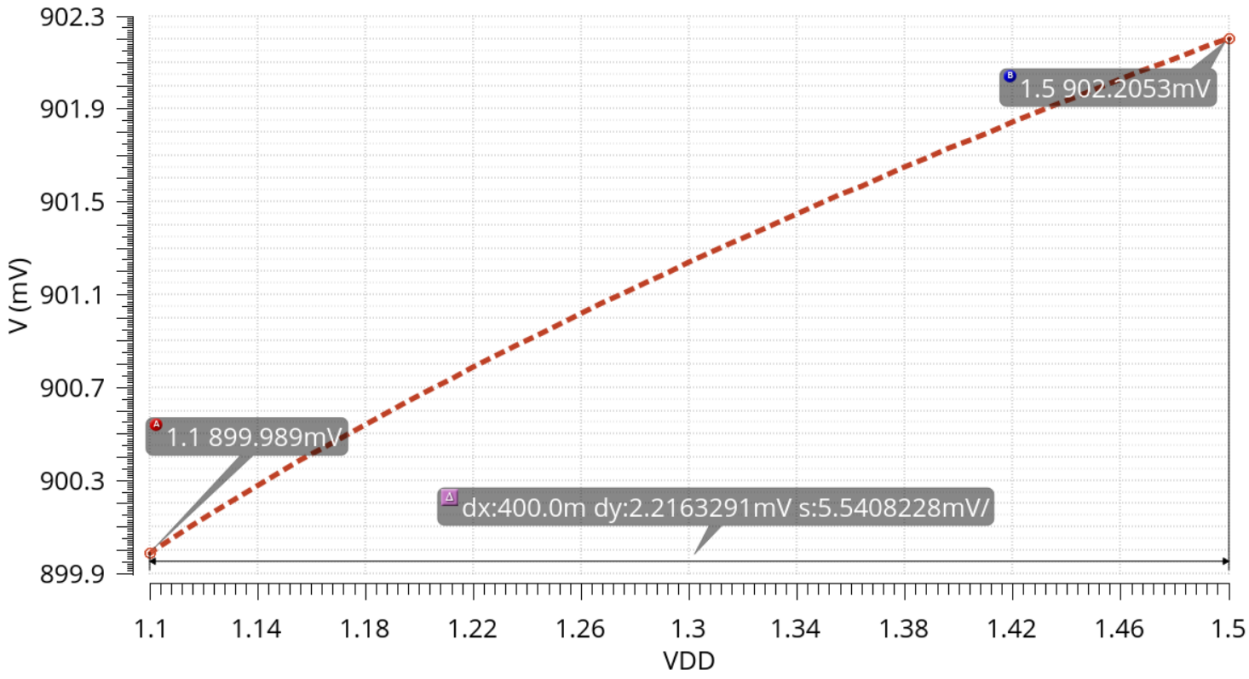

Figure 4.3: Line regulation at 0 A load current

4.2 Dynamic-state Performance

In this section, dynamic-state performance including load transient response, line transient response and the start up condition of the LDO are shown.

Fig. 4.5 shows the uncompensated output voltage transient response when the output load current switches from 0 A to 100 mA with 100 ns rising time and falling time. The output voltage drops to 0 V instantly when the load increases from 0 A to 100 mA causing a more than 900 mV spike. Due to the supply voltage, the overshoot voltage cannot exceed the supply voltage so that the overshoot is restricted to 200 mV but with longer settling time. This longer settling time can be reduced by improving the bandwidth when there is no output load current. The differentiator enhances the transient response a lot which can be seen from the Fig. 4.6. The undershoot voltage becomes 98.6 mV instead of more than 900 mV because of the differentiator. The differentiator senses the output voltage change and turns on the discharging NMOS transistor to boost the slew rate during transients.

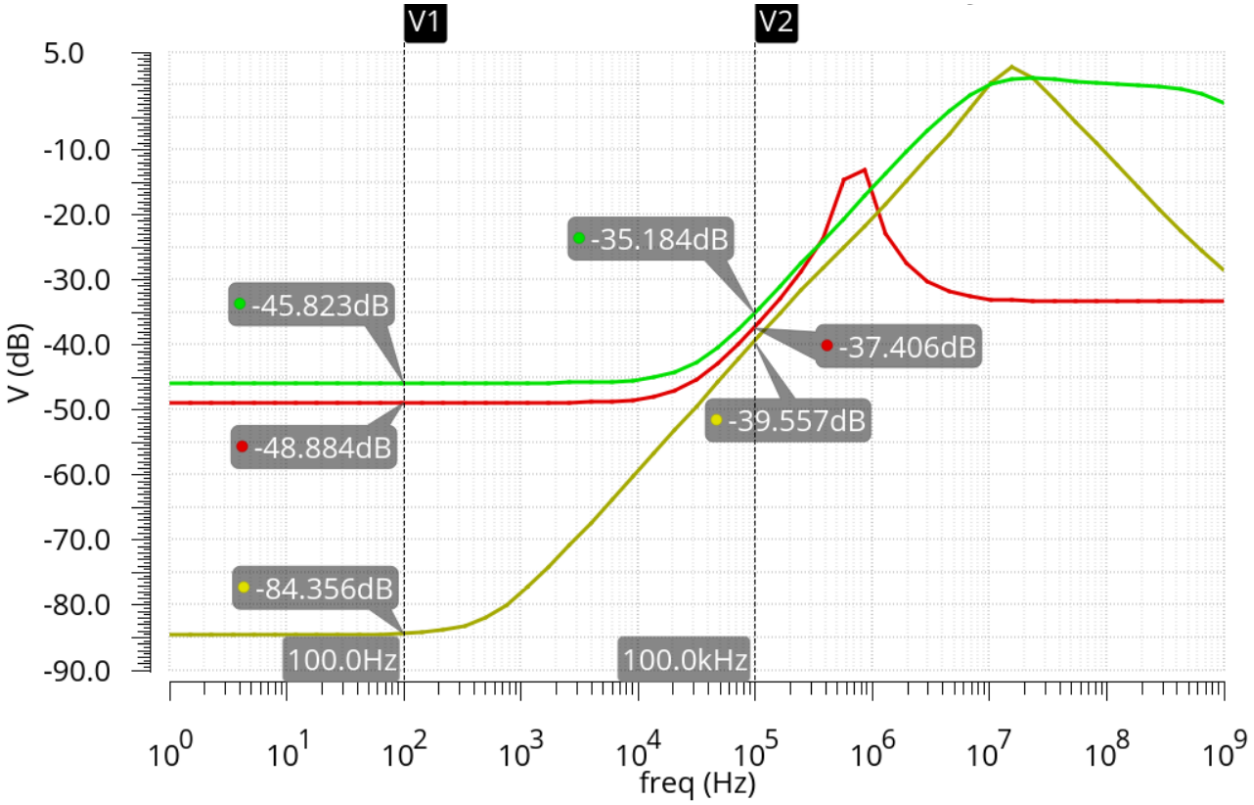

Figure 4.4: PSRR at 0, 1 mA and 100 mA load current

Line transient response is simulated with a supply step from 1.1 V to 1.5V at 1 us rising and falling time. Fig. 4.7 shows the line transient response at 0 A output load current. It shows the output voltage variation is no more than 27.7 mV. At 100 mA output load condition shown in Fig. 4.8, the voltage variation is about 15.45 mV which is less than the case at zero load condition. The small overshoot under line transients at max load means more rejection to the large signal line transients.

Start up condition is critical to the LDO especially in this work. Because of the negative resistance of the cross-coupled pair, there stands some chance that the LDO is not able to start up. From the simulation results, the LDO can start up correctly with 3 us start up time and 27.7 overshoot voltage when there is no load at the output. The worst case happens when the LDO starts up with an output load at 100 mA. Shown in Fig. 4.9 and Fig. 4.10, the LDO is able to start up with a 9.8 us settling time when there is no load at the output. However, the LDO only has

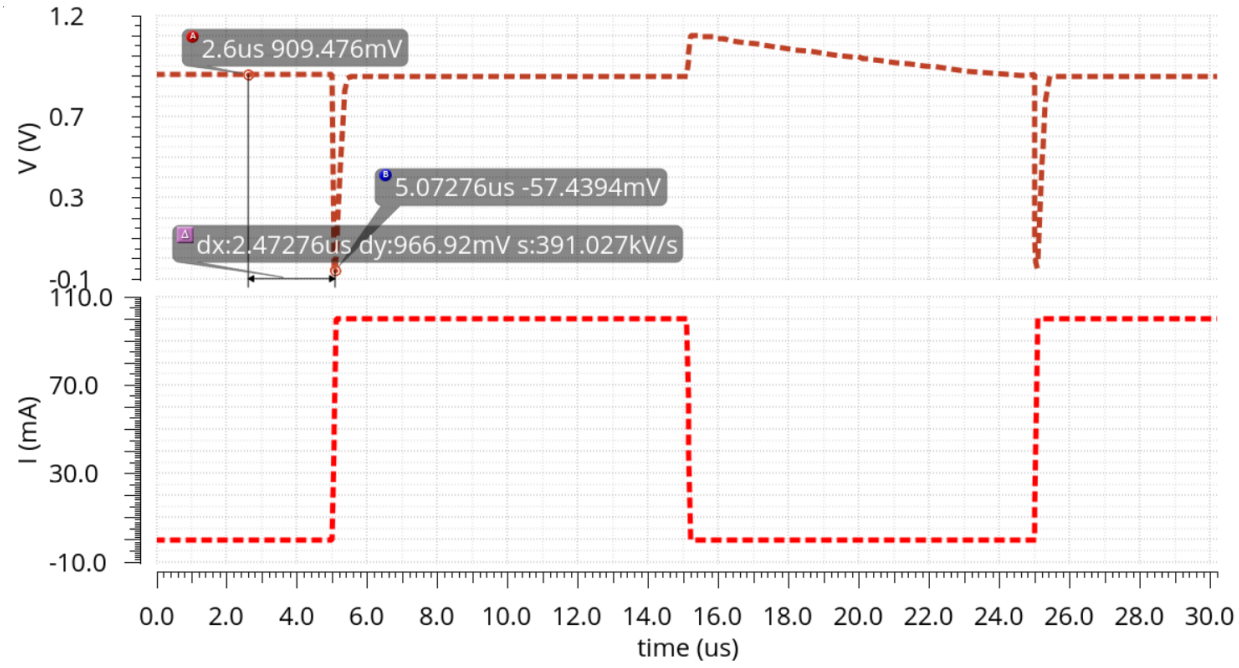

Figure 4.5: Uncompensated load transient response

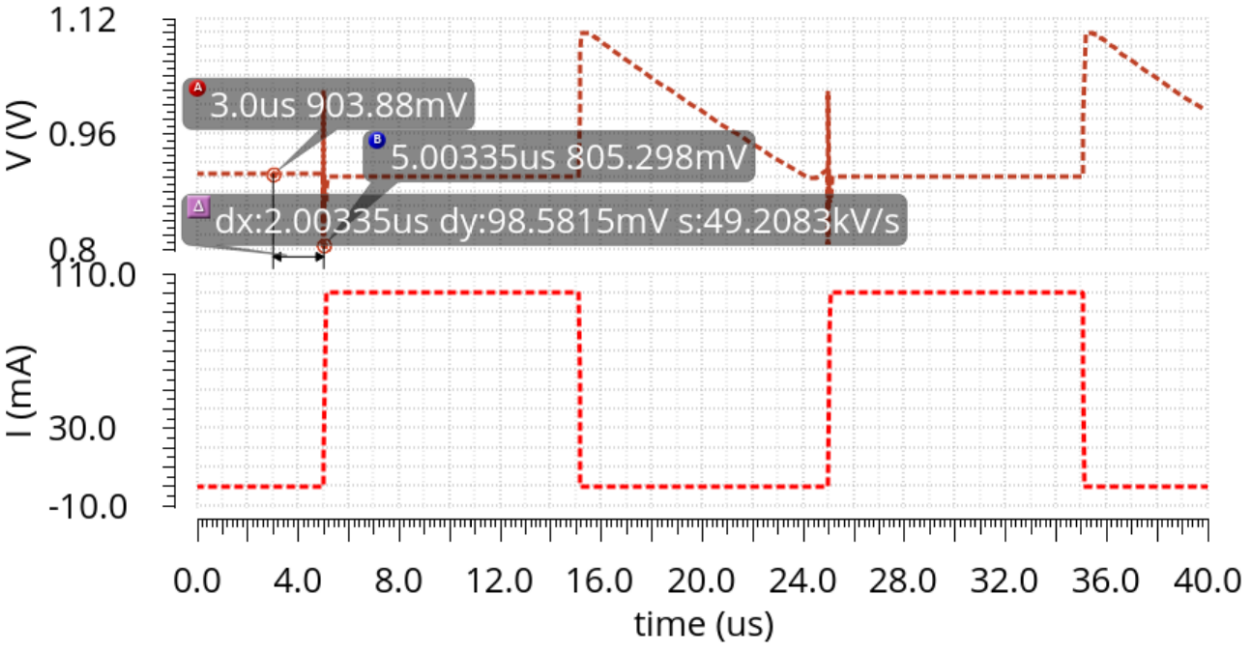

Figure 4.6: Compensated load transient response

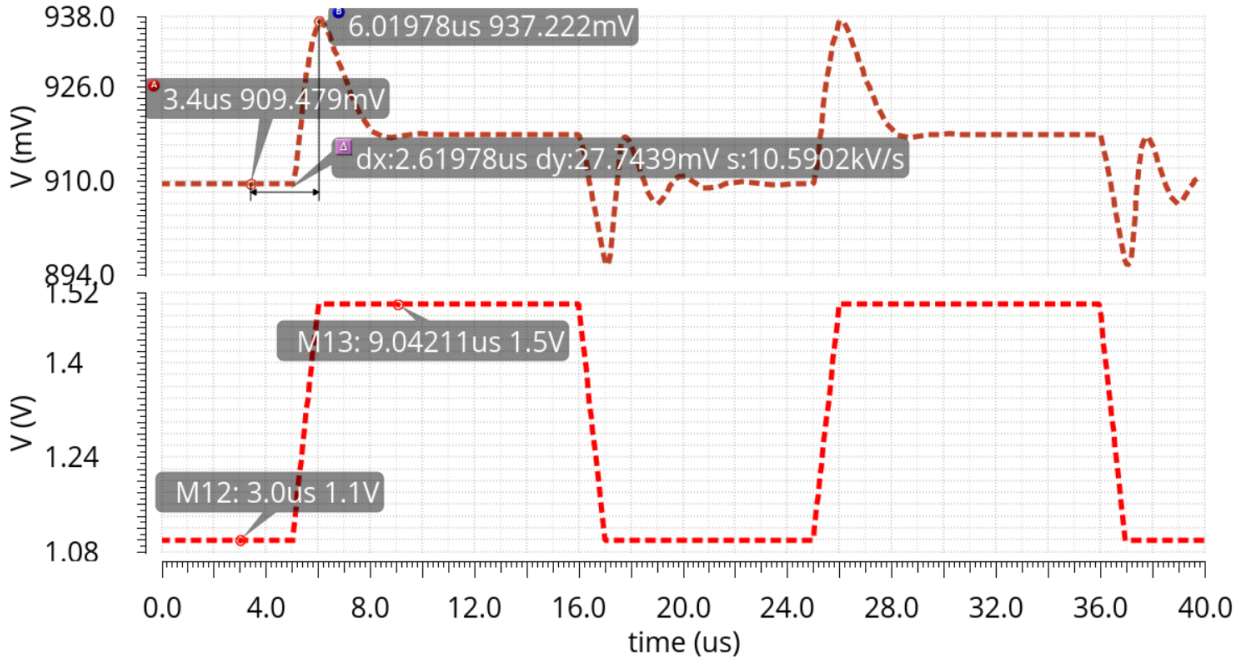

Figure 4.7: Line transient response at no load

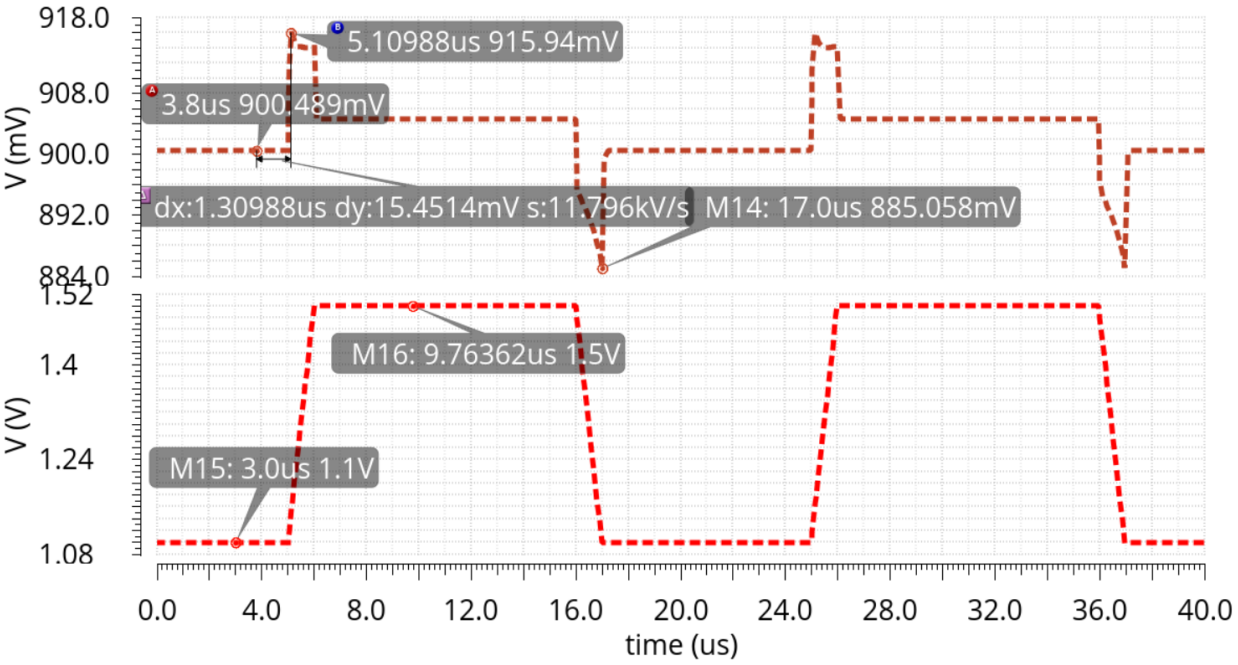

Figure 4.8: Line transient response at 100 mA load

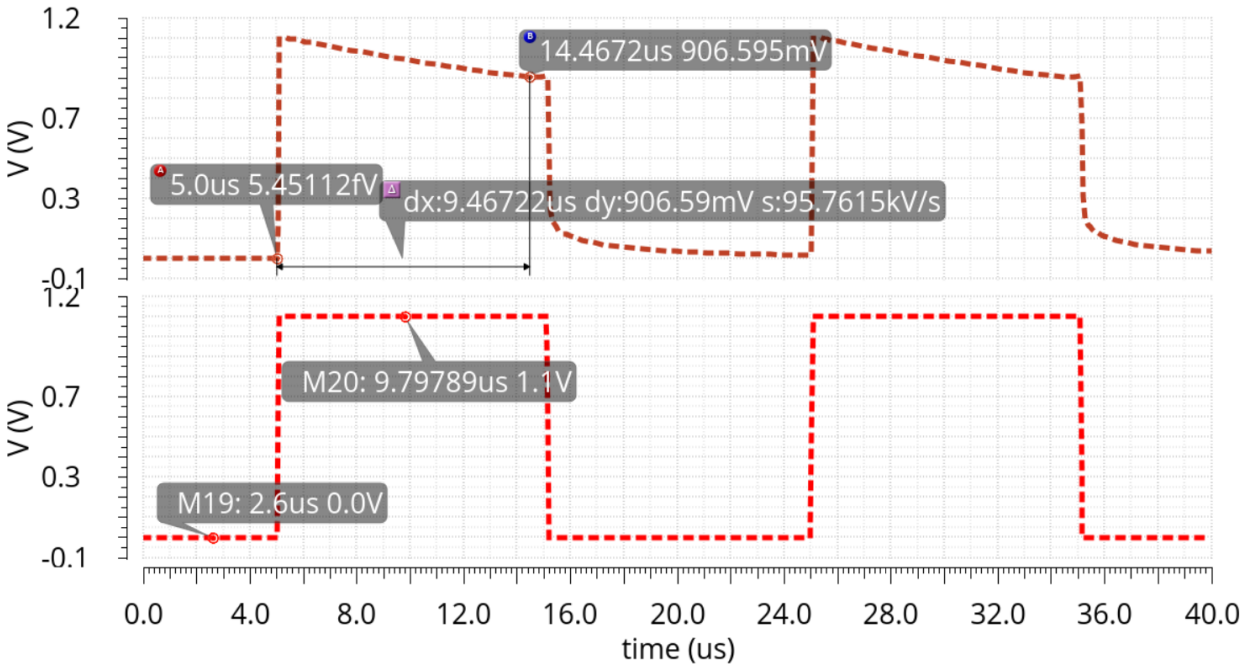

Figure 4.9: Start up condition with 0 A load current

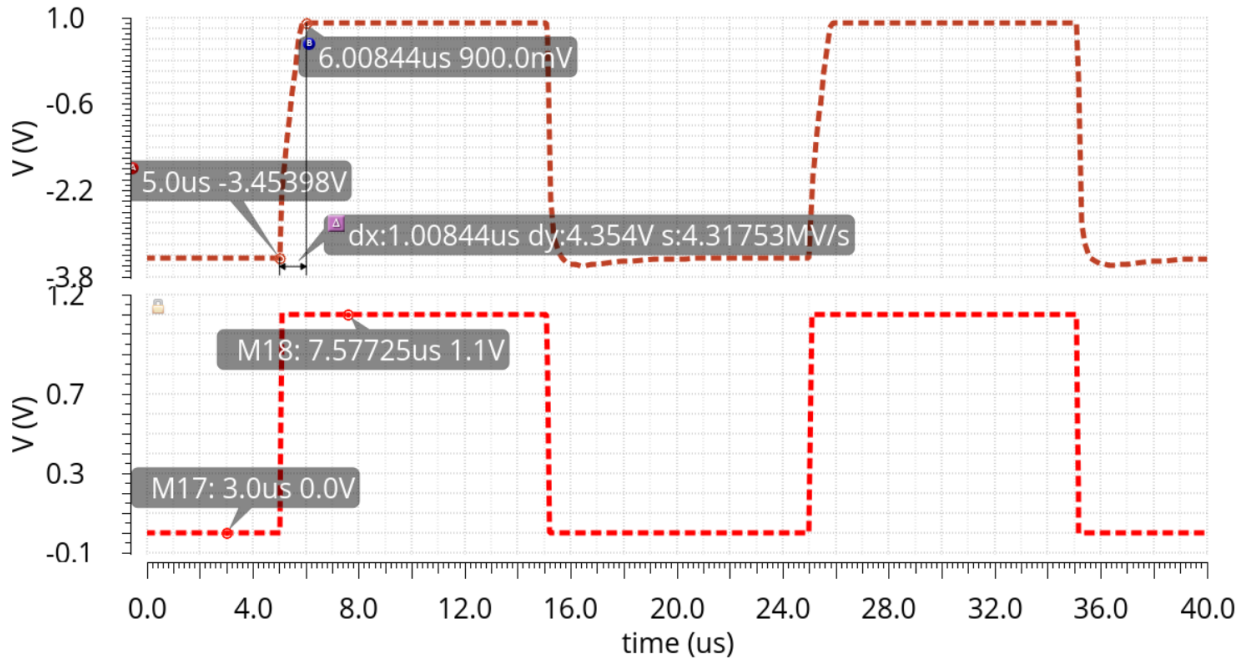

Figure 4.10: Start up condition with 100 mA load current

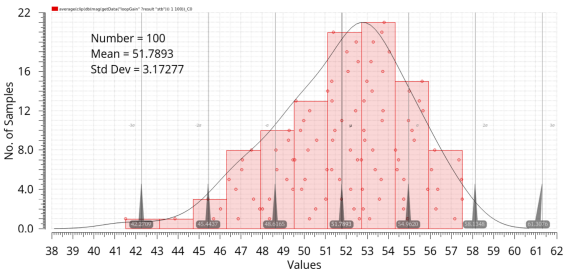

Figure 4.11: Loop gain for no load

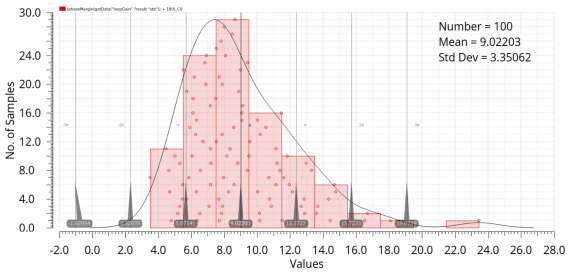

Figure 4.12: Phase margin for no load

1 us start up time when there is full load at the output. This is because the bandwidth under two different loading conditions. The bandwidth at no load is small because the output pole is close to the dominant pole while the output pole is pushed to much higher frequency beyond the UGF causing a good bandwidth.

4.3 Monte Carlo Simulation

Monte carlo simulation is essential for testing the sensitivity of the LDO. The process variation such as threshold voltage variation affects the performance of the LDO a lot. Fig. 4.11 to Fig. 4.16 show the monte carlo simulation results of the loop gain and phase margin of the LDO at 0 A, 1 mA and 100 mA. The minimum loop gain with 0 A output current load is 41.5 dB and the minimum phase margin is 3.4°. At 1 mA output load, the minimum loop gain is 53 dB and the minimum phase margin is 25°. When the output current is 100 mA, the minimum loop gain is 43 dB with phase margin 61°.

Loop gain and phase margin under five different corners are simulated which shown in Fig. 4.17. The worst case happens when the output load is zero. The minimum loop gain is 35.5 dB and the minimum phase margin is 2.75°. When the load increases to 1 mA, the minimum loop gain is 58.2 dB and the minimum phase margin is 63.6°. As for 100 mA output load, the minimum loop gain is 52.1 dB with a minimum phase margin 76.3°. Therefore, the LDO can maintain a good loop gain and phase margin when there is a full load at the output. At no load conditions, the

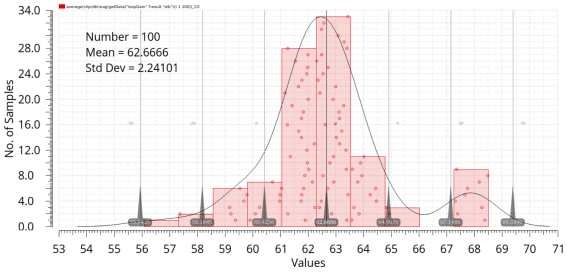

Figure 4.13: Loop gain for 1 mA load

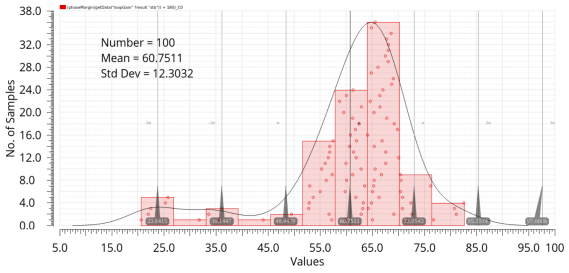

Figure 4.14: Phase margin for 1 mA load

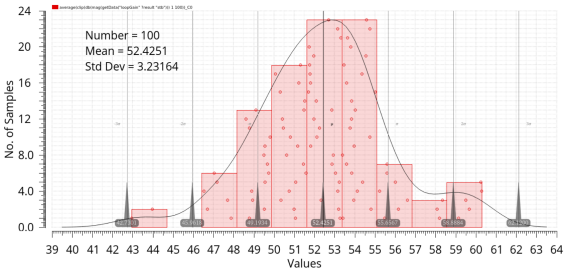

Figure 4.15: Loop gain for 100 mA load

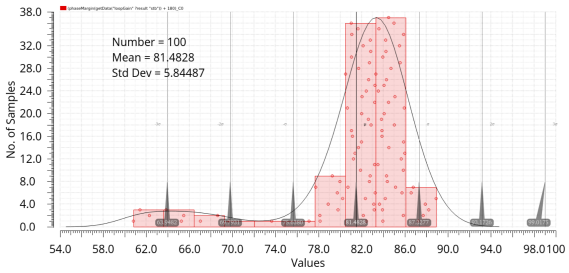

Figure 4.16: Phase margin for 100 mA load

LDO have enough loop gain to maintain an accurate output voltage with a positive phase margin at worst case to ensure the stability of the LDO.

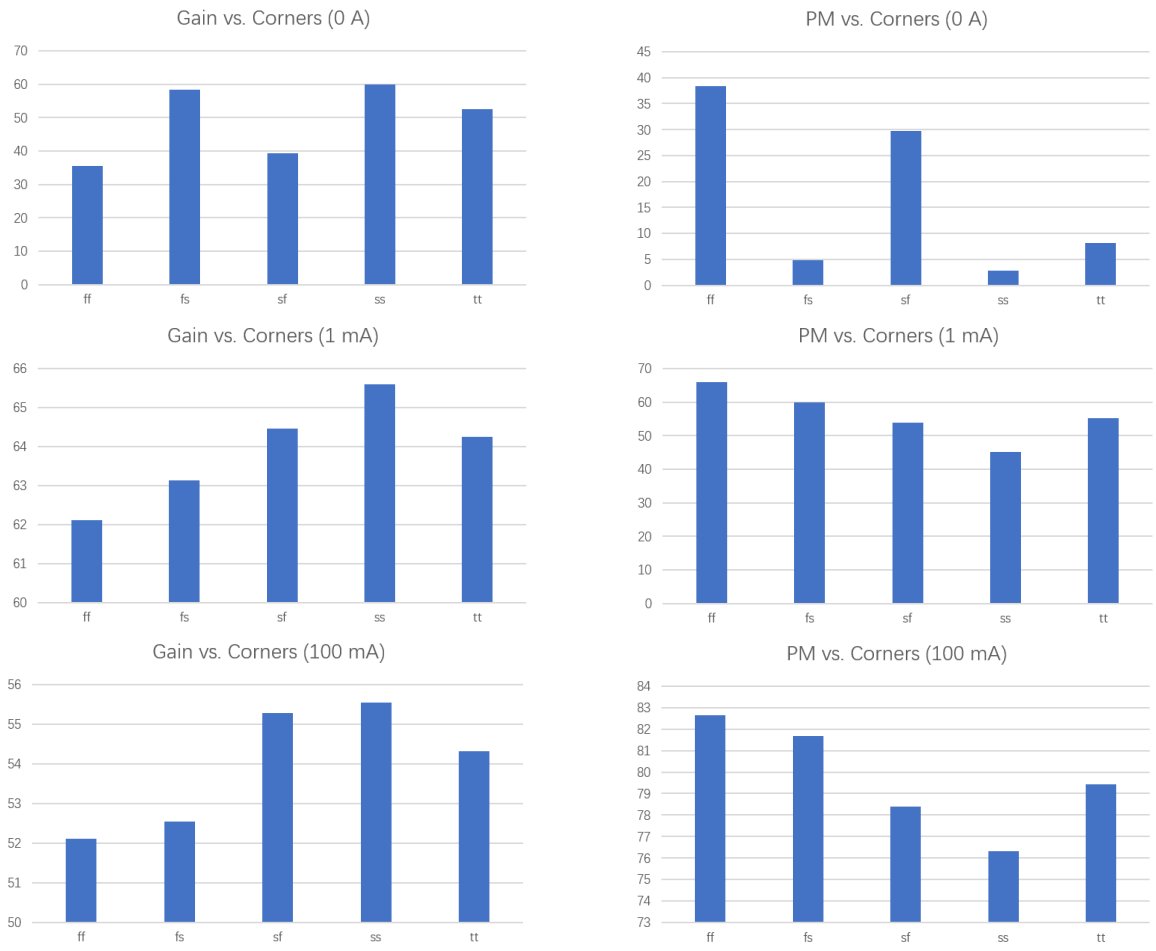

Figure 4.17: Loop gain and phase margin for 5 corners at 0A, 1mA and 100mA

5. CONCLUSIONS AND FUTURE WORK

A novel gain-compensated external capacitor-less LDO is presented to compensate the loop gain to more than 52 dB at all loading conditions with only 5.7 uA quiescent current. A differentiator is used to sense the output load transients to enhance the transient response. The differentiator circuit reduces the uncompensated undershoot from 900 mV to only 98.6 mV. It should be noticed that the LDO is stable (no RHP poles) under all loading conditions but only has good phase margin (> 55°) when the output load current is above 1 mA.

The proposed gain-compensated external capacitor-less LDO is simulated in tsmc 40 nm technology. In this technology the size of the pass element is much smaller which make the gate parasitic capacitor small. This benefits a lot for the size, bandwidth and transient response. In the meanwhile, with the cross-coupled pair negative resistors, the two-stage error amplifier can achieve a 243% higher gain (41.8 dB to 52.5 dB) with very low quiescent current (5.7 uA).

Parameter	[3]	[6]	[10]	This work
Process	CMOS 0.13	CMOS 0.35	CMOS 0.18	CMOS 0.04
I_{max}	50 mA	50 mA	50 mA	100 mA
V_{out}	1 V	2.8 V	1.6 V	0.9 V
V_{drop}	0.2 V	0.2 V	0.2 V	0.2 V
C_{out}	20 pF	100 pF	100 pF	50 pF
Transient$\triangle V_{out}$	56 mV	183 mV	120 mV	98 mV
I_q	37.3 uA	65 uA	55 uA	5.7 uA
Settling	0.4 us	7.8 us	6 us	9 us
Loop gain	75-87	55-62	50-75	52-64
PSRR@100k	-38 dB	-26 dB	-50 dB	-35 dB
FOM[1]	17 fs	476 fs	264 fs	2.79 fs

Table 5.1: Compare table for different LDOs

The proposed LDO specifications are shown in Table 5.1, compared with three different LDOs.

[1] $FOM = C_{out} \cdot \triangle V_{out} \cdot I_q / I_{max}^2$ [4]

The proposed LDO is able to achieve really good static state and dynamic state performance with low power consumption conducting much more loading current at the same time. According to the FOM calculation, a very low FOM 2.87 fs is achieved in this work.

With all these specifications, the proposed external capacitor-less LDO can achieve a decent job for very low voltage, power efficient SOC applications with small on-chip capacitor.

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