An Efficient Test Relaxation Technique For Combinational Circuits Based On Critical Path Tracing

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Summary

Reducing test data size is one of the major challenges in testing systems-on-a-chip. This can be achieved by test compaction and/or compression techniques. Having a partially specified or relaxed test set increases the effectiveness of compaction and compression techniques. In this paper, we propose a novel and efficient test relaxation technique for combinational circuits. It is based on critical path tracing and hence it may result in a reduction in the fault coverage. However, based on experimental results on ISCAS benchmark circuits, the drop in the fault coverage (if any) after relaxation is small for most of the circuits. The technique is faster than the brute-force test relaxation method by several orders of magnitude.