An Efficient Network-On-Chip Architecture Based On The Fat-Tree (FT) Topology

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Summary

A novel approach for an efficient network-on-chip using a modified Fat Tree is presented. Contention is eliminated and latency is reduced through an improved topology and router architecture. The adopted topology increases performance without a substantial increase in the routing cost. This is achieved by using an improved buffer-less, paremeterizable router architecture. The proposed router architecture is simple to implement yet can achieve the required packet collision avoidance. Simulation results that show the level of performance achieved by both the topology and the router architecture are presented. A throughput of more than 90% is achieved way above the 40-50% usually seen in other networks on chips.