CMOS BANDPASS FILTERS FOR LOW-IF BLUETOOTH RECEIVER

BY

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This thesis, written by Mohammad Khalaf Al-Ghamdi under the direction of his thesis advisor and approved by his thesis committee, has been presented to and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL ENGINEERING.

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To

My Parents,

Wife,

Sisters,

&

Professors

For their patience and support

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No one but Allah, the most greatest, deserves all our thanks as he gave us the faith, the patience, and the power to complete this work successfully.

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ABSTRACT

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Bluetooth technology is a small, low-cost, short-range radio link between portable devices and network access point. It is operating in the 2.4 GHz band. Bluetooth receiver performs all the selectivity and blocking by an active on-chip IF filter, requiring a sophisticated high-order IF filter design. The quality of the IF filters dominates the performance of the overall receiver in terms of distortion and adjacent/alternate channel rejection.

The thesis investigates the realization of CMOS bandpass filters for integrated Low-IF Bluetooth receiver. Two different approaches based on voltage-buffer and unity gain cells are investigated. The center frequency and bandwidth of the filter are 3MHz and 1MHz respectively. The proposed designs provide simplified, low power and small area solution.

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تعمل تقنية Bluetooth -وهي تقنية اتصالات لاسلكية قصيرة المدى – على الموجة 2.4 جيجا هرتز و تتميز بأنا متناهية الصغر و رخيصة السعر. مستقبل البلوتوث يتكفل باجراء اختيار الموجة و تصفيتها من الموجات المتداخلة، و تجري الأبحاث لتصنيعه في شريحة الكترونية واحدة. يتضح جليا أن مستقبل البلوتوث يعتمد بشكل أساسي على مدى جودة المرشحات المستخدمة.

في رسالة الماجستير هذه نحاول ان نصنع المرشح الوسطي – وهو المرشح الرئيس في المستقبل – المساهم في جعل المستقبل على شريحة الكترونية واحدة باستخدام تقنية CMOS. سيتم تصميم المرشح بطريقتين بناءاً على نوعية العنصر الأساسي، أولا باستخدام خلية أحادية الربح (unity-gain cell) ثم باستخدام حاجز الجهد (voltage-buffer).المرشح يعمل على تردد 3 ميجا هيرتز و عرض حزمة بمقدار 1 ميجا هيرتز. التصاميم المقترحة تقدم حلولا بسيطة، عالية الأداء و منخفضة الطاقة.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The technology market focuses on improving the use of computing facilities and communication protocols in portable devices or what is called wireless network solutions and applications. The vision of cable-free environment is the driving force behind the booming of wireless or radio-based systems. The goal for such systems is to provide efficient services for mobile users by means of small and short-range radio-based networks. This results in developing several technologies and standards such as WLAN (**W**ireless **L**ocal **A**rea **N**etwork), HomeRF (**Home R**adio **F**requency), IrDA (**I**nfra**r**ed **D**ata **A**ssociation), and Bluetooth. These technologies comprise same objectives of handling voice and data with open standards utilizing low cost, low power, small size and single-chip design solutions. [1]

Bluetooth wireless technology is a short range, point-to-multipoint voice and data communication system. Its potential applications have encouraged leading technology manufacturers in the world - Ericsson, IBM, Intel, Nokia, Toshiba and others to form the Bluetooth Special Interest Group (BSIG) [1]. They developed specifications that

address the requirements for this networking product. The result of this effort is a refined Bluetooth technology. The Bluetooth is characterized by a relaxed dynamic range, noise figure and image rejection specifications to allow the development of fully integrated and inexpensive Bluetooth modules [2]. Bluetooth radio system operates in the unlicensed 2.4-2.5 GHz band. The channel is represented by a pseudo-random hopping sequence hops in the 79 RF channels spaced by 1 MHz. The hopping rate is 1600 hops/s with data transmission rate of 1 Mbps. In point-to-multipoint connection, the channel is shared among several Bluetooth devices. Two or more devices sharing the same channel form a piconet. There is one master device and up to seven active slaves devices in one piconet. [1]

The dominant technologies used in designing devices for mobile radio receivers have been Gallium Arsenide (GaAs), BiCMOS and silicon bipolar. These technologies offer higher breakdown voltage, lower substrate loss and higher quality of monolithic inductors and capacitors compared with the less expensive CMOS technology. CMOS technology was exclusively used in the digital signal-processing units, however, the recent advances in CMOS processes have made it more possible to realize CMOS RF and IF circuits with performance comparable to that of other technologies. Most of the essential building blocks of wireless transceivers such as low noise amplifiers, mixers, frequency synthesizers and intermediate frequency (IF) filters, have been realized by CMOS processes. [3, 4]

1.2 Research Goals

A typical integrated Bluetooth receiver performs all selectivity and blocking by an active on-chip IF filter, requiring a sophisticated high-order IF filter design. The quality of the IF filter dominates the performance of the overall analog receiver in terms of distortion and adjacent/alternate channel rejection. The IF filter must provide enough selectivity and robustness required for channel filtering.

This thesis proposes new designs for implementing fully integrated CMOS IF bandpass filters for Bluetooth receivers. The proposed circuits are optimized to meet the selectivity and dynamic range requirements while consuming relatively small power. Two new filter designs are presented. The first filter is based on unity gain cells (i.e. voltage and current followers) and utilizes linearized MOSFET resistors for tuning. The second design is based on unity gain fully differential voltage buffers providing simplified, low power, and small area design solution.

1.3 Thesis Organization

Chapter 2 provides backgrounds for radio receiver architectures, requirements of Bluetooth IF bandpass filter, and different filtering techniques. A new proposed bandpass filter design based on unity-gain cells with optimized power consumption and dynamic range is presented in chapter 3. Chapter 4 discusses the second design, which utilizes a single voltage-buffer per biquad. Designs of high order-filters based on the proposed techniques are presented in Chapter 5. Comprehensive comparisons between

the proposed designs and other published works, conclusions, and recommendations for further work are given in Chapter 6.

CHAPTER 2

BLUETOOTH RECEIVERS AND LITERATURE REVIEW

2.1 Introduction

The incoming spectrum of signals to a receiver is normally comprised of many different signal bands that could have components from various sources, sometimes very close together [2]. An incoming signal spectrum may look something like that shown in Fig. 2.1.

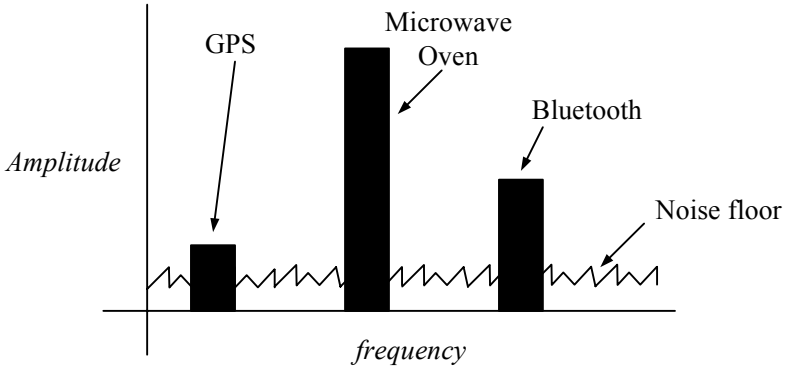


Figure 2.1: Example of Incoming Signal Spectrum

It is important for a given receiver to have enough sensitivity to be able to receive a weak desired signal in the presence of noise and interference. The required sensitivity of a Bluetooth receiver is -70dBm [1]. This means that the receiver must detect signals with as low power as –70dBm (i.e. 70.7 μV assuming a typical load impedance of 50Ω).

Also, the receiver must have a certain minimum selectivity meaning that it must be able to receive a signal in the desired channel in the presents of nearby, unwanted signals or interferers. The following subsection discusses in details different possible Bluetooth receivers.

2.2 Bluetooth Receiver Architectures

A Bluetooth receiver consists mainly of a front-end and a demodulator. The front-end part performing down conversion and channel selection is always analog. The demodulator can be either analog or digital. The relaxed Bluetooth specifications permit the use of the following wireless receiver architectures: High-IF, Low-IF, Very Low IF, and Zero-IF (also called Direct Conversion). [5, 6]

The High-IF receiver performs a single conversion to an IF that is much grater than the channel bandwidth as shown in Fig. 2.2. Since surface acoustic wave (SAW) filters are already available with low cost, the most common choice for the IF frequency is the 110.6 MHz. SAW filters have a very high quality factor (Q), but they are bulky. High quality factor inductors are involved in SAW designs, so they are off-chip filters. [5, 7, 8]. Thus, this architecture does not lend its self to fully integrated applications.

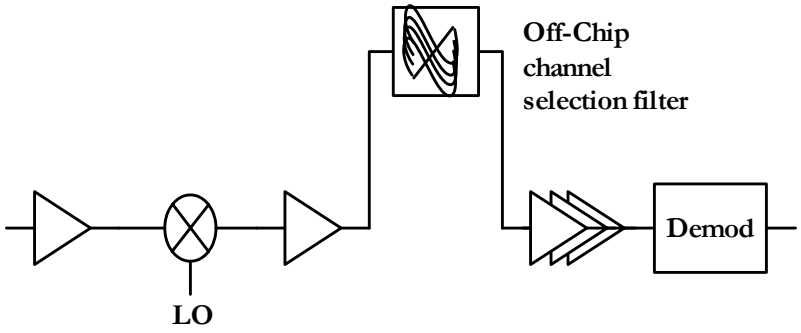


Figure 2.2: High IF

The Low-IF receiver incorporates a single conversion to an IF that is near the channel bandwidth, usually in the 1 MHz - 10 MHz range as shown in Fig. 2.3. High-order filters but with lower quality factors (Q) are required for channel selection. This scheme provides a fully integrable and low power solution. However, it is associated with image problems. Fortunately, Bluetooth specification has relaxed image requirements (40dB) which can be achieved using an image reject mixer. [5, 6, 8]

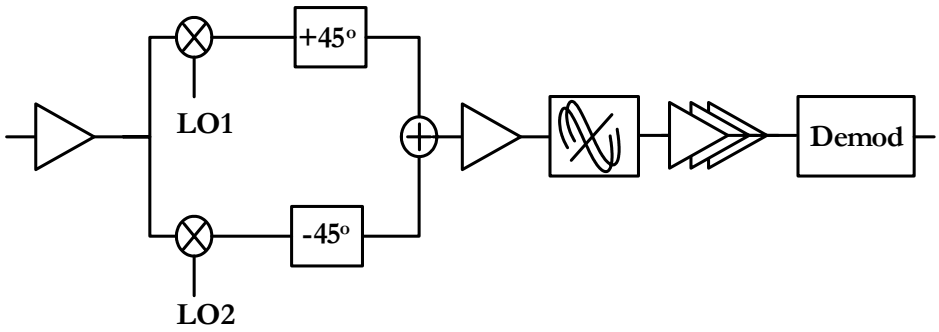


Figure 2.3: Low IF

The Very Low-IF (VLow-IF) receiver uses a single conversion to an IF that is one-half the channel bandwidth as shown in Fig. 2.4. The required low-pass filter must be associated with DC blockers. Typically, the DC notch is implemented using an off chip

large time constant integrator or servo loop [7, 8]. Also, the low-pass filter will suffer from the flicker noise of transistors at such low frequencies [7]. Moreover, the IF chain and the Automatic Gain Control (AGC) must be highly linear to successfully demodulate the signal [5]

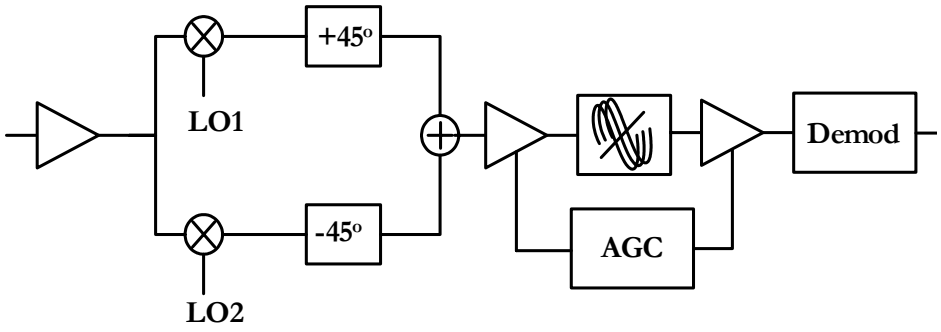


Figure 2.4: Very-Low IF

The Direct Conversion Receiver (DCR) or Zero-IF is a mixed signal front-end receiver. The signal is mixed directly to base-band, requiring an I/Q downmixer and separate base-band path to maintain the negative frequency information. A high selectivity low-pass filter is needed here for channel selection. This architecture suffers from non-linear DC offset problems caused by self mixing since the local oscillator signal is in-band. This DC component must be removed with DC offset correction, usually off chip, to avoid saturating the receiver. [5, 8]

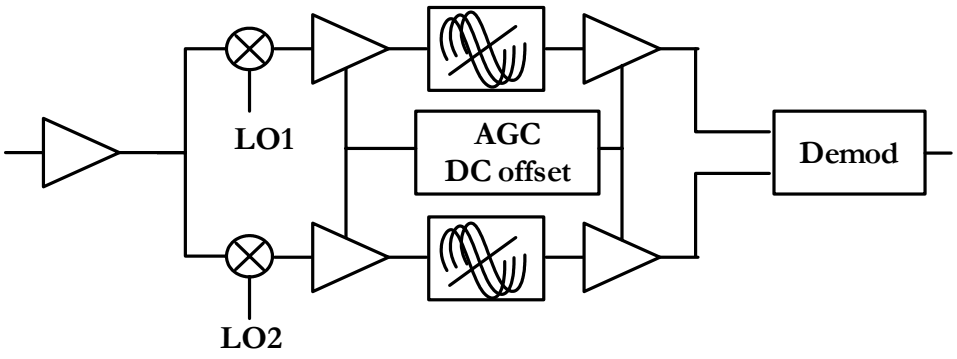


Figure 2.5: Zero IF

In summary, the High-IF architecture is used in the Bluetooth devices available but uses off-chip components. Low-IF, VLow-IF and Zero-IF architectures can be fully integrated in a single chip. However, dynamic ranges of VLow-IF and Zero-IF receivers are significantly degraded by the flicker noise. Hence, the signal-to-noise ratio (SNR) of the receiver will degrade as well. Also, the design of the RF sections for VLow-IF and Zero-IF schemes is more complicated than those of the Low-IF. Moreover, VLow-IF and Zero-IF architectures suffer from folding distortion and DC offset problems, respectively.

On the other hand, the Low-IF architecture circumvents the previously mentioned problems. Also, the relaxed image rejection requirement of the Bluetooth makes the choice of a low-IF architecture attractive [1, 7, 8]. Baseband signal processing in Low-IF can be performed either by analog or mixed signal– filtration and demodulation as demonstrated in Fig. 2.6 [6].

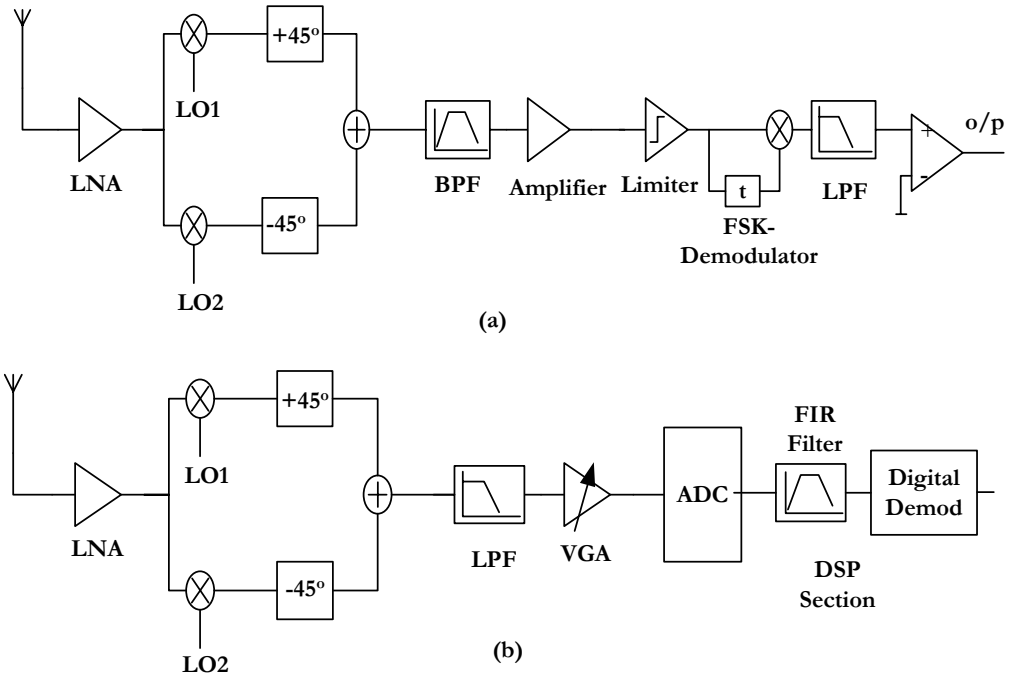


Figure 2.6: Low-IF Bluetooth Receivers: a) Analog Filtering and Demodulation and (b) Mixed Signal Filtering and Demodulation

An analog demodulation scheme does not necessitate analog-to-digital converter (ADC) design. The attenuation of out-of-band blockers in the analog scheme must be fully done in the analog side. A high order bandpass filter with an accurate response is necessary to reject the blocking signals. Also, an amplifier stage is necessary before the limiter. Demodulation of the FSK signal is done after the limiter using a PLL tone detector or any FSK demodulator which is implemented in the analog domain.

On the other hand, a mixed signal scheme requires a relatively high resolution analog-to-digital converter (ADC). A variable gain amplifier (VGA) stage is required to relax the dynamic range of the ADC. The attenuation of the out-of-band blockers in the mixed signal scheme is done partially in the analog section and partially in the digital

section using finite-impulse response (FIR) filter. Therefore, a low-pass analog filter with relaxed selectivity specifications is sufficient. The demodulation of the signal is implemented in the digital domain. Moreover, a mixed signal scheme is incorporated with the following characteristics: the signal after the RF section will be in the baseband, and two paths I/Q are required for image rejection.

Hence, a bandpass filter –in the analog scheme- is responsible for channel selecting in the analog receiver. Whereas, a decimation lowpass filter, analog to digital converter (ADC), and digital bandpass filter –in the mixed signal scheme- are needed to perform the same task in the digital receiver. In practice, the sampling rate is selected as high as ten times of the signal bandwidth requiring high frequency ADC. Therefore, it is expected that the design of bandpass filter would consume less power compared with two lowpass filters, ADC, and the digital filter. [6]

2.3 Bandpass IF Filter Specifications

The analog low-IF Bluetooth receiver performs all selectivity and blocking by an active on-chip IF filter, requiring a sophisticated high-order IF filter. The quality of the IF filter dominates the performance of the overall analog receiver in terms of distortion and adjacent/alternate channel rejection [9]. The analog Low-IF scheme needs high order bandpass filter with accurate frequency response. The choice of the IF involves many design tradeoffs. The filter bandwidth is 1MHz and typically its center frequency is chosen to be around a few MHz [6, 10]. In order to avoid increasing the PLL locking time, phase noise, flicker noise, and folding distortion the IF frequency should be

higher than 2MHz. However, the power consumption of the filter usually increases for higher IF frequency [7, 8]. Hence a 3MHz center frequency is typically selected.

The IF filter must provide enough selectivity and robustness required for channel filtering. A sharp IF filter response is required to be achieved without scarifying the phase response. A nonlinear phase response degrades the performance of the FM demodulator. Hence, it is required to avoid distorting the amplitude and phase of the in-band signal as possible. The in-band group delay of the filter should be less than 1μs to eliminate the inter-symbol distortion. The filter should attenuate blocker one, two, and three or more by at least 0dB, 30dB, and 40dB, respectively. Also, it must exhibit a dynamic range that prevents the interferers from desensitize the receiver. The dynamic range requirements depend on both the linearity and noise performance of the filter. The linearity is measured by 3rd order intercept point IP3 which must be 75dB above the noise floor for this bandpass filter.

Table 2.1: Selectivity Requirements

Requirement	Ratio
Adjacent interference (1 MHz)	0 dB
Second interference (2 MHz)	-30 dB
Third and more interference (≥3 MHz)	-40 dB

The filter must be able to process large signals with little intermodulation distortion. Harmonics of the signal will lie in the filter stopband where they are automatically attenuated. However, it is very possible that 3rd order intermodulation between

particular combinations of two tones in the stopband generates significant products in the passband as shown in Fig. 2.7.

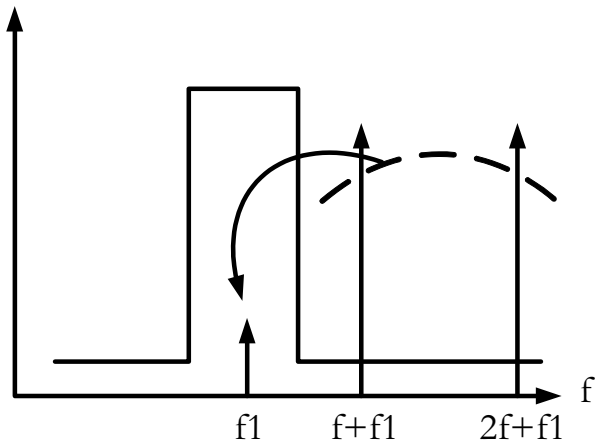


Figure 2.7: Intermodulation between out-of-band signals

Moreover, as the desired signal in an integrated receiver is slightly amplified (20 to 30 dB) before the baseband chain, noises of the baseband circuits dominate the signal-to-noise ratio of the whole receiver. The concept of dynamic range is usually used to describe the performance of filters. Fig. 2.8 shows a filter dynamic range defined as the spurious free dynamic range (SFDR). It can be seen that the usable dynamic range is that the input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. Mathematically, it is given be:

$$DR = \frac{2}{3}\left(IP3 - NF\right) \tag{2.1}$$

where DR is the dynamic range in dB, IP3 is the intermodulation input intercept point in dBm, and NF is the noise floor in dB. The spectral density of noise is defined as the

average normalized noise power (mean-squared value) over 1-Hz bandwidth. The input-refereed-noise (IRN) usually expressed in $V/\sqrt{Hz}$, and,

$$\mathrm{NF} = 20\log\left(IRN \times \sqrt{BW}\right) \tag{2.2}$$

Note that, noise floor and dynamic range are related to the bandwidth of the filter. [7, 8]

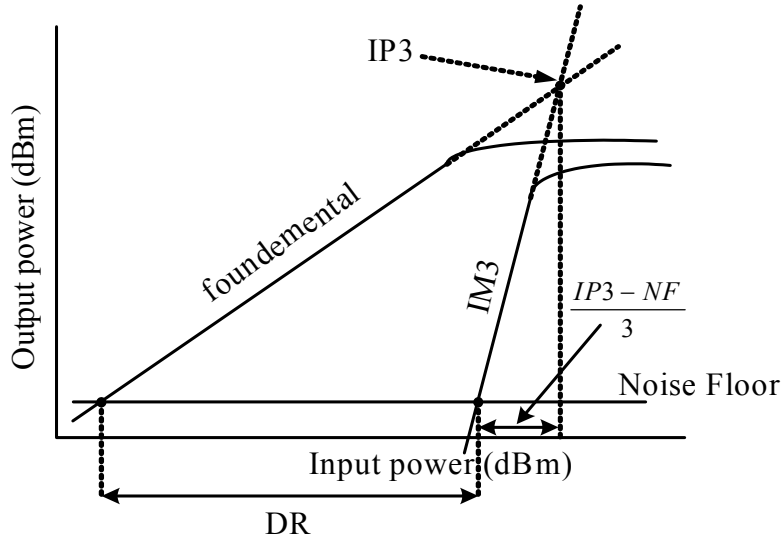


Figure 2.8: Dynamic Range

2.4 Towards Integrated Bluetooth bandpass filter design

Bluetooth open standard encourages researchers to design new solutions for the Bluetooth transceivers. The main targets are simplified, low power, integrated, and low cost designs [1]. Designing highly selective bandpass filter for Bluetooth Low-IF receiver presents a challenging task. The required bandpass filter is realized using

different approaches. The available market receivers use SAW filters, which involving design of an RF mixer with additional power gain to compensate for the filter's insertion loss [4, 8]. Bandpass filter design using stripline or low-temperature co-fired ceramic technology was presented in [11, 12], but this way is not practical. It will add complexity for the circuit design and it will state limitation for mass production.

Several CMOS fully integrated bandpass filters were proposed for Bluetooth receivers [10, 13, 14 and 15]. The presented filters are based on transconductance-C "g_m-C" technique obtained from their passive LC filters counterparts. Filters presented in [10 and 13] utilize an attractive transconductor having no high impedance internal nodes [16]. Circuits based on this g_m-C technique will have no parasitic capacitance resulting in a very wide bandwidth. Thus, they are suitable for very high frequency applications [16].

Design and implementation of an 18^{th} order g_m-C filter in 0.6μm CMOS process were presented in [10]. The filter bandwidth is 1 MHz and its center frequency is 3 MHz. The filter shows very high selectivity of 47dB at 1 MHz offset from the center frequency. The supply voltage used voltage and current are 2.53V and 2.4mA, respectively. The center frequency is tuned by adjusting the supply voltage to change the values of the transconductors. Thus, it would complicate the design of the receiver's power supply. This filter exceeded the selectivity requirements of the Bluetooth in order to avoid the use of automatic tuning circuit. But this is achieved by using excessive number (at least 40) of transconductors. To minimize the number of

required transconductors, different approximations and combinations of filters were tested in [13]. A 4th order Butterworth filter followed by 10th order elliptic filter was chosen. The filter achieves attenuations of 40dB at 2 MHz and 37dB at 4 MHz. Although the number of transconductors is reduced to 34, the presented filter still consumes the same supply current of 2.4mA.

A new transconductance circuit with enhanced output resistance and reduced flicker noise was proposed in [14]. The transconductance value is controlled by a voltage source independent of the supply voltage. A 12-order bandpass filter was built using the proposed g_m-C technique. An additional highpass filter was used at the input of the filter to isolate the common-mode mixer output from the filter common-mode input. Linearity of the filter is degraded as the gain increases and vice versa [14]. The center frequency was selected to be at 2MHz with 1MHz bandwidth. The total noise was $29\mu V_{rms}$ and the IP3 was 37 dBm. The filter uses an automatic tuning circuit and over satisfies the Bluetooth selectivity requirements. A modified version of this filter was used as a part of a low-voltage Bluetooth receiver [15]. A 16th order filter was designed using Butterworth approximation. The filter uses 32 transconductors. The main disadvantage of these filters is their relatively huge supply current of about 0.5mA per filter pole.

In summary, filters implemented in [10, 13, 14 and 15] are based on g_m-C technique. They are obtained from their passive LC counterparts. As shown in table 2.2, these filters exceed the Bluetooth selectivity requirements. But they suffer from relatively

high power consumptions. Also, the filters presented in [10] and [13l require changing the supply voltage to adjust their center frequencies. Moreover, the filters suggested in [14] and [15] exhibit poor dynamic range of about 45dB that is 5dB less than Bluetooth requirements. In this thesis, the proposed filters are optimized to have improved power consumption, efficient tuning methods, and enhanced dynamic ranges.

Table 2.2: Specification of the most recent published Bluetooth BPF

Ref.	Filter-Order	I/Pole (mA) / Power Supply	Center frequency	Attenuation	Gain	Noise $\left(\frac{\mu V}{\sqrt{Hz}}\right)$	Dynamic Range	Group Delay µs	Area mm²
[10]	18th	0.133 / 2.5V	3 MHz	$f_c \pm$ 1MHz> 47 dB	0 dB	250	48.7 dB	1.8	0.55
[13]	14th	0.175 / 2.5V	3 MHz	@2MHz 30dB @4MHz 37dB	0 dB	81	47.5	< 1	0.8
[14]	12th	0.4583 / 2.7V	2 MHz	@ f_c ±1 MHz 29dB @ f_c ±2 MHz 58dB	15dB	29	45.2 dB	0.6	1.68
[15]	16th	0.5 / 1.8V	2 MHz	@ f_c ±1 MHz 29dB @ f_c ±2 MHz 58dB	15dB	32	45 dB	0.6	2

CHAPTER 3

BANDPASS FILTER BASED ON UNITY GAIN CELLS

3.1 Introduction

Recently, analog circuit design using current-mode approach has gained extensive attention. This is driven by the inherent advantages associated with current-mode circuits such as wide bandwidths, large slew rates, low power consumptions, and simple circuitries [7, 8, and 17]. These features are highly understandable in filters based on unity gain cells (i.e. current and voltage followers) as demonstrated in [18-20]. These filter topologies use passive resistors and capacitors. Thus, these filters are not suitable for integrated circuit (IC) applications since their parameters cannot be electronically programmed. Programmability is an essential requirement for integrated filter designs to compensate for inaccurate passive component values and non-ideal characteristics of active elements as well as process variations and temperature effects.

Several MOSFET-C filters based on current mode building blocks were proposed more recently [21-24]. By incorporating the principle of non-linearity cancellation, MOSFET transistors are used as programmable resistors to design filters with tunable characteristics. Therefore, this approach combines the advantages of wide frequency

operation of current mode signal processing and programmability of the conventional MOSFET-C filters.

All the previously published filters based on unity gain cells, without and with MOSFET-C, are single-ended. However, wireless receivers incorporate fully differential (balanced) signal paths. This is because balanced operation improves the performance of analog systems in terms of noise rejection, harmonic distortion and dynamic range. Moreover, fully integrated receivers employ on the same chip both analog and digital parts. Therefore, fully balanced architectures of the analog parts become more essential as they provide immunity to digital noises.

3.2 First Proposed Approach

The first proposed filter is based on unity gain cells. The filter incorporates linearized MOSFET resistors to provide the filter with programmable parameters that can be tuned electronically. This filter design utilizes the low power current follower (CF) and voltage buffer (VB) presented in [25]. New proposed MOSFET non-linearity cancellation methods and fully differential structures are presented.

A unity gain cell is defined in this thesis as a current follower (CF) followed by a voltage buffer (VB) as shown in Fig.3.1. A CF is a two terminal device, which conveys current signals from a low impedance input terminal to a high impedance output terminal. Whereas, a VB transfers a voltage signal from a high impedance input node to

a low impedance output node. The terminal characteristics of current and voltage followers are summarized in Table 3.1.

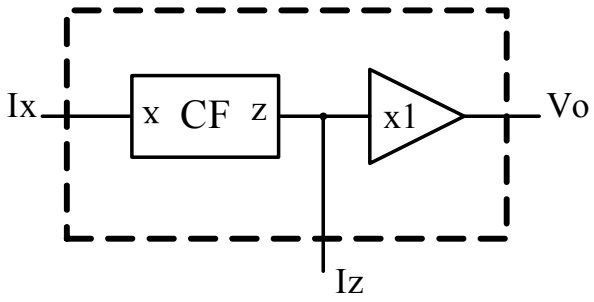


Figure 3.1: Unity Gain Cell

Table 3.1: Unity gain cells terminal characteristics

Characteristics	Current Follower	Voltage Buffer
Relations	$I_{output} = I_{input}$ $V_{input}=0$	$V_{output}=V_{input}$
Input impedance	Very Low Ideally=zero	Very High Ideally =infinity
Output Impedance	Very High Ideally =infinity	Very Low Ideally=zero

Unity gain cells are selected among all other current mode building blocks for the following reasons: first, the input port virtual ground property of the CF facilitates the addition of different signals. In addition, the low output impedance of the VB allows the distribution of output signal to several subcircuits. These features allow for incorporating shunt-shunt negative feedbacks, the most suitable topology for low voltage operation. Moreover, shunt-shunt feedbacks will further reduce input impedances of CFs and the output impedances of VBs improving the accuracy of the filter responses. Second, all internal nodes of filters will be either associated with low

impedances or connected to a capacitor. Hence, all parasitic poles will have almost no effect on the parameters of the filters. This improves the accuracy of the proposed design particularly if the practice capacitors are lumped with the intentional ones. The following subsections describe in details the different basic building blocks of the filter.

3.2.1 Current follower (CF)

A CMOS realization of the current follower (CF) is shown in Fig.3.2 [26]. The X terminal is held at virtual ground, which results in a simple input stage that does not require rail-to-rail operation. The two biasing transistors M9 and M10 force an equal current through transistors M1 and M2. Since the gate voltage of transistors M1 and M2 are equal, the source voltage of transistor M1 equals the source voltage of M2 which results in a virtual ground at the X terminal. The X terminal current is provided by the action of the class-AB negative feedback loop formed by transistors M3- M7. The X terminal input impedance is reduced by amount of feedback. The X terminal current is copied to Z terminal by the current mirrors transistors M6 and M8. Transistors M11 and M12 are used for standby current biasing. The level shifter transistors M3 and M4 are used to adjust the standby current. Assuming all transistors in saturation region and transistors M3 and M4 are matched, the transislinear loop equation will be as follows:

$$\sqrt{\frac{2I_{M7}}{K_P}} + \sqrt{\frac{2I_{M5}}{K_N}} = \sqrt{\frac{2I_{SB}}{K_P}} + \sqrt{\frac{2I_{SB}}{K_N}} \tag{3.1}$$

where $I_{M3}=I_{M4}$ and $I_{M12}=I_{M11}=I_{SB}$. No current is withdrawn from terminal X in standby mode, $I_X=0$, and I_{M1} will be equal to the biasing current I_{bp}. Therefore, from equation (3.1):

$$I_{M7} = I_{M5} = I_{SB} = I_{SB} \tag{3.2}$$

If a current is withdrawn from the X terminal, the gate voltage of M7 is lowered. By the action of the level shift transistors M3 and M4, the gate voltage of transistor M5 is lowered as well. Thus, the current through transistor M7 increases and the current through transistor M5 decreases. The result is that the feedback network provides the necessary extra current flowing out of the X terminal. Similarly, if the X terminal sinks current, the gate voltage of transistors M7 and M5 increases, this decreases the current through transistor M7 and increases the current through transistor M5. [26]

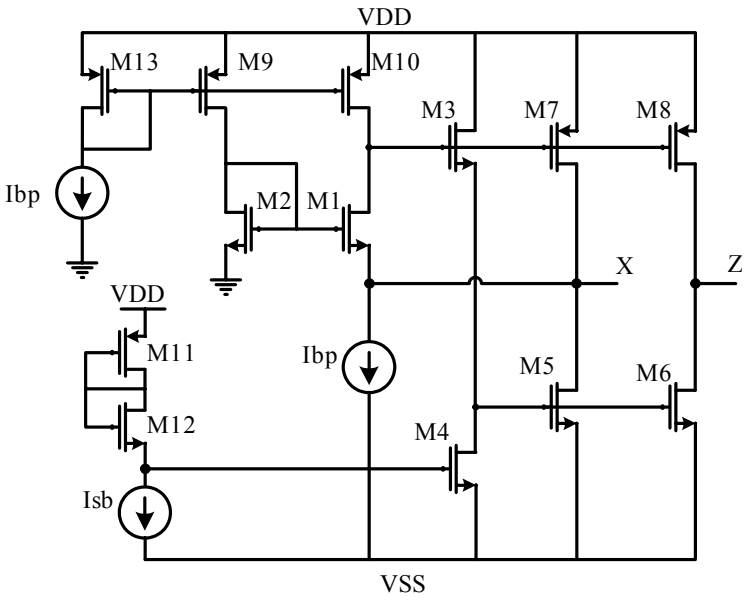


Figure 3.2: CF CMOS realization

3.2.2 Voltage buffer (VB)

A voltage buffer circuit is required to exhibit accurate voltage tracking between the output and input terminals, high input impedance and low output impedance. A CMOS realization of the voltage buffer (VB) is shown in Fig.3.3 [27]. The buffer circuit utilizes a class-AB loop to boost the transconductance of a MOSFET transistor operating in the saturation region. The voltage tracking of the buffer is achieved by forcing a constant biasing current I_B through M1. The source-gate voltage relation of transistor M1 is,

$$V_0 = V_i - V_T - \sqrt{\frac{2I_B}{K}} \tag{3.3}$$

Thus, the source voltage follows the input voltage but with DC shift ($-V_T - \sqrt{2I_B/K}$) that suffers from body effects such as temperature and process dependence. Transistor M2 is used here to cancel the body effect and the DC level shift between *Vi* and *Vo*. Class AB negative feedback operation reduces the output resistance. [27]

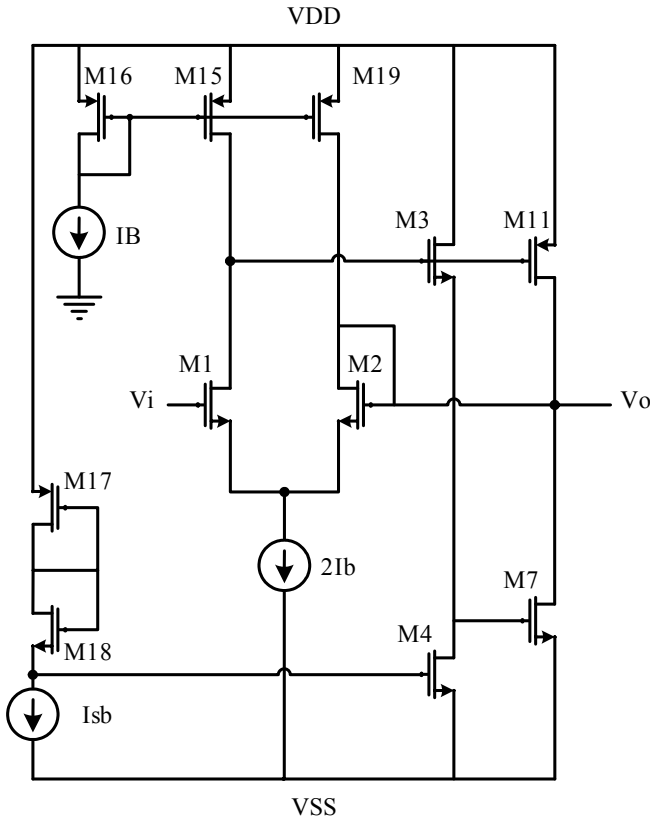


Figure 3.3: VB CMOS realization

3.2.3 Non-Linearity Cancellation

The current of a MOSFET transistor operating in ohmic (triode) region where $V_{DS} << V_{eff}$ can be expressed as:

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_s^2) + a_2(V_D^3 - V_S^3) + \ldots \quad (3.4)$$

where V_G, V_D, V_S, and V_T are the gate, drain, source, and threshold voltages, respectively. K is the transconductance of the transistor. Assuming the two NMOS transistors shown in Fig. 3.4 are identical and operates in the ohmic region [29, 30], it can be shown that the odd and even nonlinearities are cancelled by subtraction as follows:

$$I_1 - I_2 = 2K(V_1 - V_2)(V_A - V_B) \tag{3.5}$$

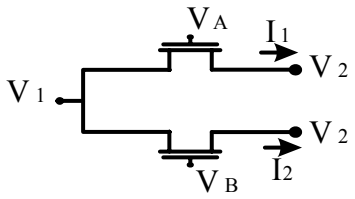


Figure 3.4: A linearized MOSFET resistor

If V_2 is set to zero or virtual ground a linear programmable conductance is obtained whose value is given by:

$$G = \frac{I_1 - I_2}{V_1} = u_n C_{ox} \frac{W}{L}(V_A - V_B) \tag{3.6}$$

The resulting conductance G is independent of the threshold voltage and can be tuned electronically by changing the gate voltages V_A and V_B. Moreover, negative conductance can be obtained by choosing the controlling voltage appropriately. The required virtual grounds and subtraction can be achieved by using two current followers as shown in Fig. 3.5.

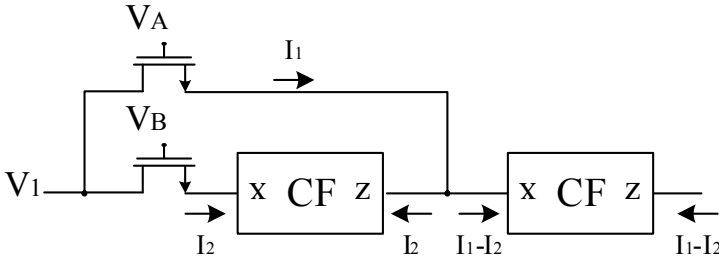
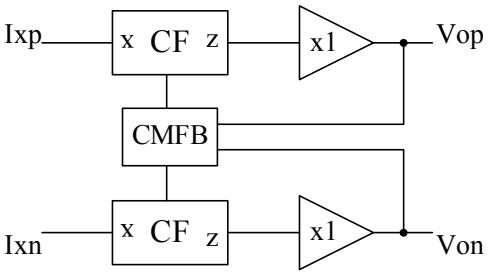


Figure 3.5: Nonlinearity cancellation using CFs

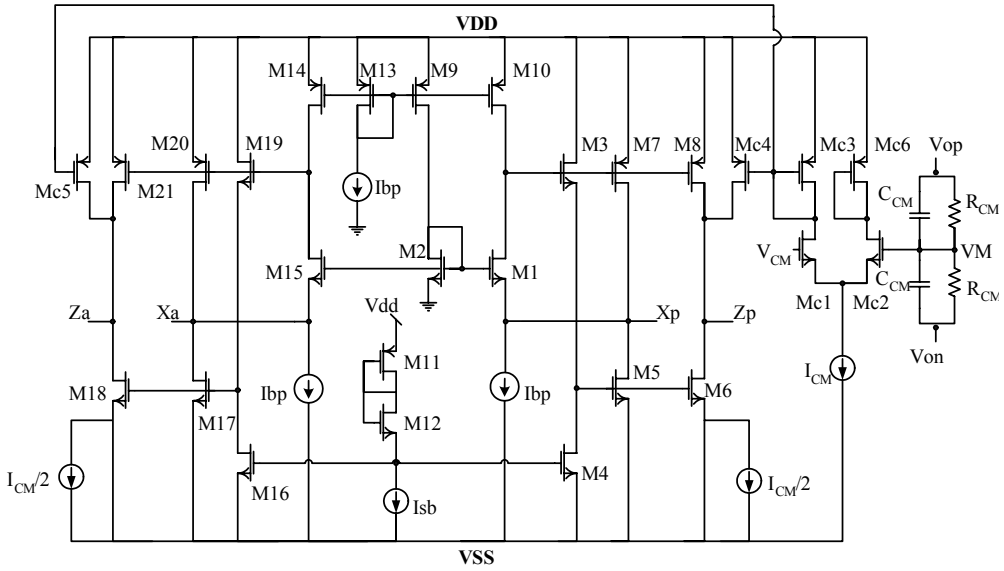
3.2.4 Fully differential realization

There are several approaches to develop the fully differential architectures for CF and VB based circuits. One way is to develop fully differential realizations for both the CF and VB. However, this method would require a separate common-mode feedback (CMFB) circuit for each element. Alternatively, a single CMFB circuit can be employed to establish the common-mode voltage of both the CF and VB, as shown in Fig. 3.6 (a). This method is straightforward, easier to develop, and avoids the use of redundant CMFB circuits.

The fully differential architecture of the CF including the CMFB circuit is shown in Fig. 3.6 (b). The inputs of the CMFB circuit are coming from the low impedance outputs of the voltage buffers. This simplifies the design of the input stage of the CMFB circuit to two resistors (R_{CM}) and two capacitors (C_{CM}). The operation of the CMFB circuit can be explained as follows. The reference common-mode voltage V_{CM} is set mid-rail (V_{CM} = 0) since complementary supplies are used. During the ideal case of zero common-mode voltage where V_{op} and V_{on} are equal in magnitude and opposite in sign, the voltage V_M will be zero. With $V_M = V_{CM} = 0$, half the tail current I_{CM} will pass through MC3-MC5 and the voltage at nodes *Zp* and *Zn* will not change. However, when a positive common mode signal is present (i.e. V_{op} is greater in magnitude than V_{on}), the voltage V_M will be positive. Hence, the currents I_{MC3} and I_{CM4} (I_{CM5}) will decrease reducing the voltage at Z_p (Z_n). This causes the voltage V_{op} and V_{on} to reduce until the common-mode signal is set to zero. The opposite action will be taken in response to a negative common-mode voltage.



(a)



(b)

Figure 3.6: (a) Fully Differential Unity Gain Cell building blocks,

(b) CF-CMFB CMOS realization

3.3 Proposed Filter Based on Unity Gain Cells

The first proposed bandpass IF filter for Bluetooth receivers uses MOSFET-C biquad filter sections based on unity gain cells. The proposed filter achieves independent control of the 3-dB center frequency (ω_o) without disturbing the quality

factor (Q). The proposed biquad is developed from its famous active-RC Tow-Tomas counterpart. The Tow-Thomas opamp based biquad [31]. It consists of lossy integrator followed by lossless integrator and an inverter connected in a loop. The Tow-Thomas Biquad is a flexible circuit structure in which the transfer function properties are easily manipulated by modifying the passive RC elements. It has low sensitivity fixed second order structure. Hence, it is suitable for cascadable high order filters.

Lossless and lossy integrators based on unity gain cells are shown in Fig. 3.7. The transfer function of the ideal integrator of Fig 3.7(a) is given by:

$$\frac{V_o}{V_i} = -\frac{1}{sCR} \tag{3.7}$$

whereas, that of the lossy integrator of Fig 3.7(b) the transfer function is given by:

$$\frac{V_o}{V_i} = -\frac{R_2/R_1}{1+sCR_2} \tag{3.8}$$

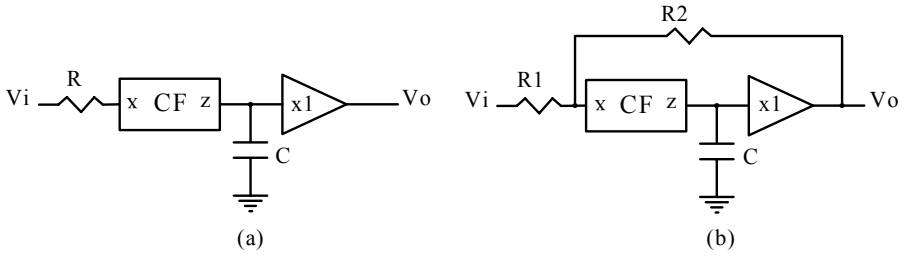


Figure 3.7: Integrators: (a) Lossless (b) Lossy

Tow-Thomas biquad filter, Fig. 3.8(a), can be converted systematically to its unity gain cell counterpart by exchanging their integrator realizations. The inverter is realized in

single-ended structure by a negative CF. The corresponding CF-VB based filter is developed as shown in Fig. 3.8(b).

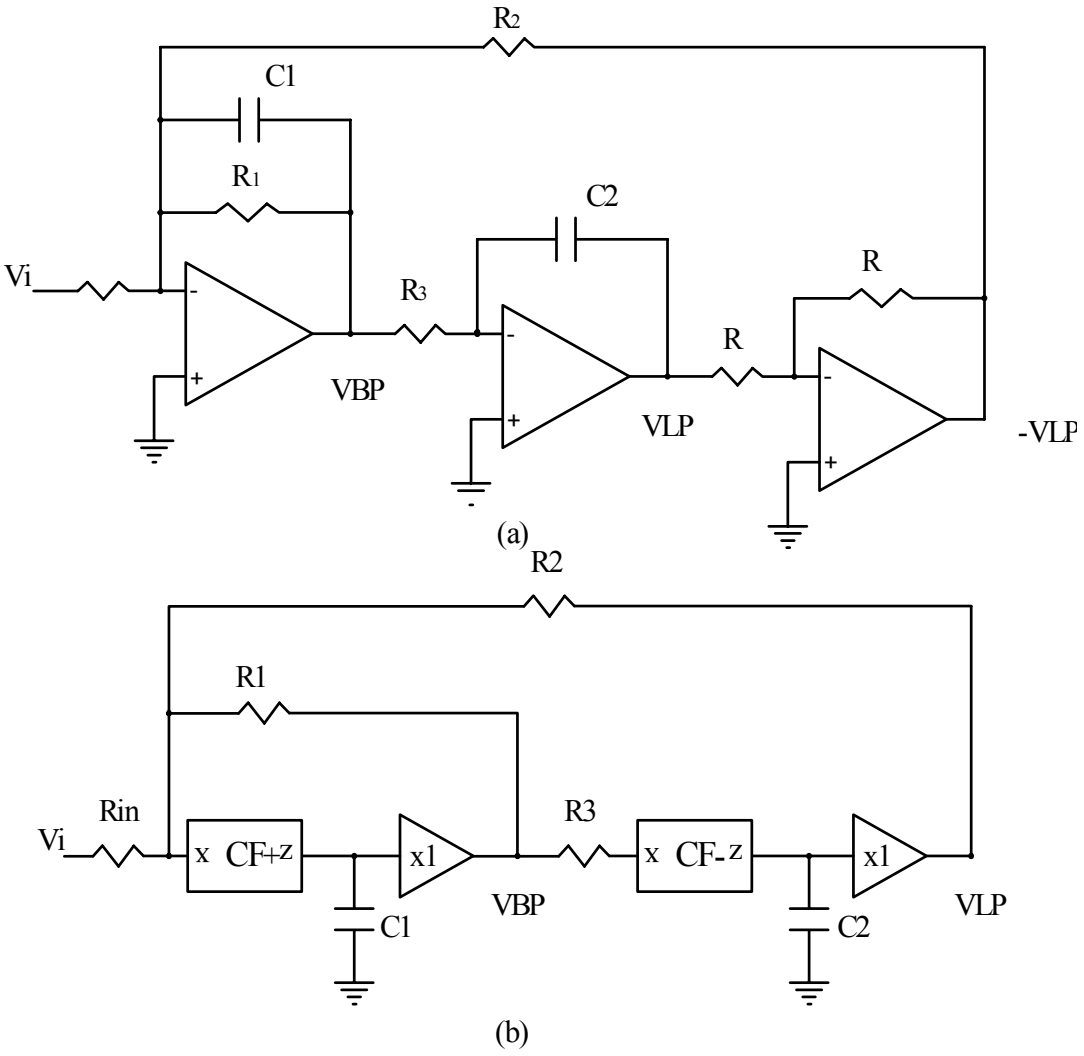


Figure 3.8: Tow-Thomas Biquad Filter (a) Opamps based (b) Unity Gain Cells Based

It can be shown that voltage transfer function of the bandpass filter of Fig. 3.8(b) is given by:

$$\frac{Vo}{Vi} = -\frac{sG_i / C_1}{s^2 + sG_1 / C_1 + G_2G_3 /(C_1C_2)} \tag{3.9}$$

The filter parameters H_o, ω_o, ω_o/Q *(BW)* and Q are given by:

$$H_o = \frac{G_i}{G_1} \tag{3.10}$$

$$\omega_o = \sqrt{\frac{G_2G_3}{C_1C_2}} \tag{3.11}$$

$$BW = \frac{\omega_0}{Q} = \frac{G_1}{C_1} \tag{3.12}$$

$$Q = \sqrt{\frac{G_2G_3C_1}{G_1G_1C_2}} \tag{3.13}$$

where $G=1/R$. The filter gain, H_o, may be changed independently by varying G_i. Q value depends on resistors and capacitors ratios that can be accurately realized in integrated circuits - by variation of 0.1% - . Hence, there may be no need for programming Q. The center frequency, ω_o, can be tuned without disturbing the gain and quality factor by changing G_2 and G_3, simultaneously with keeping the ratio G_2G_3/G_1^2 constant.

The proposed filter uses MOSFET resistor equivalent instead of conventional poly silicon on chip resistors. The simplest method to apply MOSFET technique is to replace every resistor by a triode region transistor. In this case, the equivalent

conductance will be approximately equal to the small-signal drain-source conductance of the transistor [32], which is giving by:

$$r_{ds} \approx 1 \Big/ \left[\frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) \left(V_{gs} - V_t \right) \right] \tag{3.14}$$

The fully differential operation will cancel the even nonlinearity. The nonlinear distortion will be solely due to odd terms (mainly third-order terms). In designing filters for wireless receivers, however, it is crucial to suppress the odd terms to reduce intermodulation nonlinearities. Incorporating, the non-linearity cancellation method presented in Fig. 3.5, each resistor is replaced by a MOSFET transistor pair canceling all MOSFET non-linearity. To keep all MOSFET transistors in the ohmic region, the voltages of the gates are selected as high as possible. Since the linearity condition is $V_{ds} < V_{gs} - V_t$. Thus, the input signal must be smaller than the positive supply voltage by at least V_t.

Fully differential second order filter based on unity gain cells shown in Fig. 3.8(b) can be realized with different circuit topologies that will results in different performances in terms of noise, linearity, power consumption, and common-mode rejection ratio. The following subsections investigate the performance associated with these topologies, compare them, and select the optimum design.

3.3.1 Fully differential BPF using single transistors replacement (Approach-1)

Fig. 3.9 shows a fully differential second order bandpass filter obtained by replacing each resistor with one MOSFET transistor. Although this design uses less number of components – four CFs and four VBs-, its dynamic range is defected by the non-linearity of the MOSFET transistors. The Spice simulation for the second order filter results in input referred noise of $106.2nV/\sqrt{Hz}$ and IP3 of 16dBm at f_c = 3MHz and BW = 1MHz. The IP3 is recorded from simulation results for near blockers (i.e. two different input level signals at 4MHz and 5MHz are applied that results in third order inter-modulation product at 3MHz).

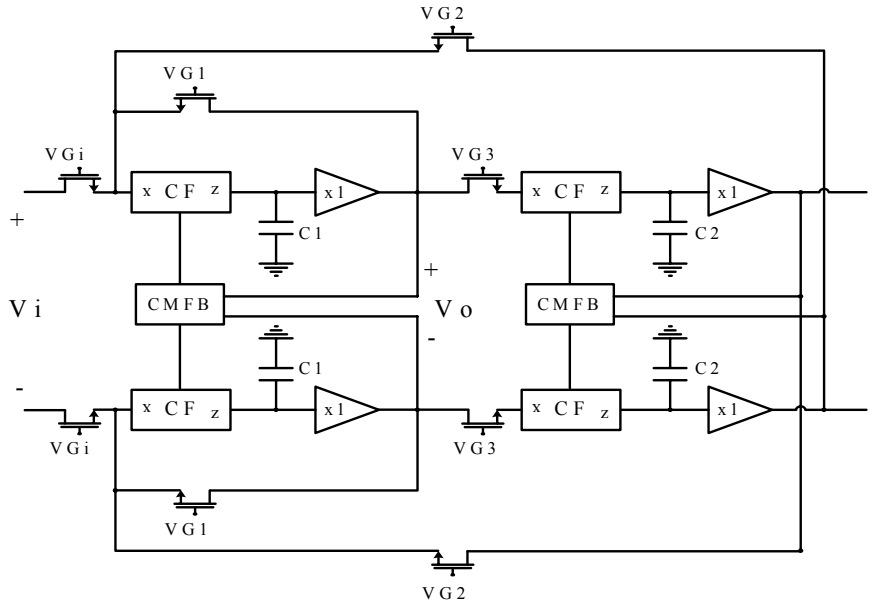


Figure 3.9: Second Order Fully Differential Bandpass Filter (Approach-1)

3.3.2 Fully differential BPF using non-linearity cancellation (Approach-2)

Incorporating the non-linearity cancellation technique proposed in subsection 3.2.4 will result in an enhanced dynamic range in comparison with approach #1. Fig. 3.10

shows a fully differential second order bandpass filter based on unity gain cells with MOSFET non-linearity cancellation. An additional CF is added before every unity gain cell to perform the MOSFET nonlinearity cancellation. This results in an improved IP3 of 22dBm. However, the input referred noise is increased to 133.5 $nV/\sqrt{Hz}$ due to the additional transistors and CFs.

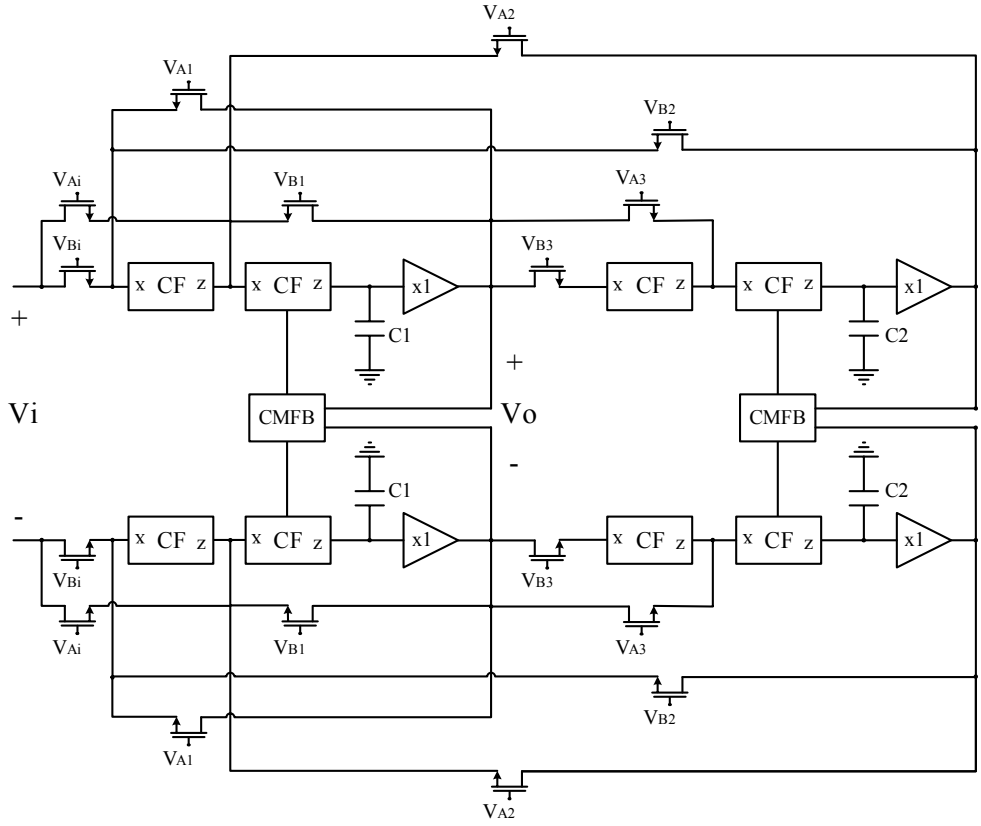


Figure 3.10: Fully Differential Second Order Bandpass Filter Based on Unity Gain Cells with MOSFET non-linearity cancellation (Approach-2)

3.3.3 Fully differential BPF with CFs reduction (Approach-3)

Approach-2 shows 6dB improvement in terms of IP3 value, however, its noise is higher than Approach-1. This sub-section investigates optimization of Approach-2 to

enhance its noise and power consumption performances. It has been found after careful observation that the number of CFs can be reduced by performing MOSFET non-linearity cancellation using a shared CF with two outputs. Additional MOSFETs are added accordingly to perform the necessarily current addition and subtraction. Fig. 3.11 shows the fully differential second order bandpass filter with reduced number of CFs. Compare with approach-2, this significantly reduces noise, power consumption and are of the filter. Also, the linearity is automatically improved as some active elements are removed. The obtained results from Spice show that input the noise is reduced to $126.9\,nV/\sqrt{Hz}$ and IP3 is improved to 27dBm.

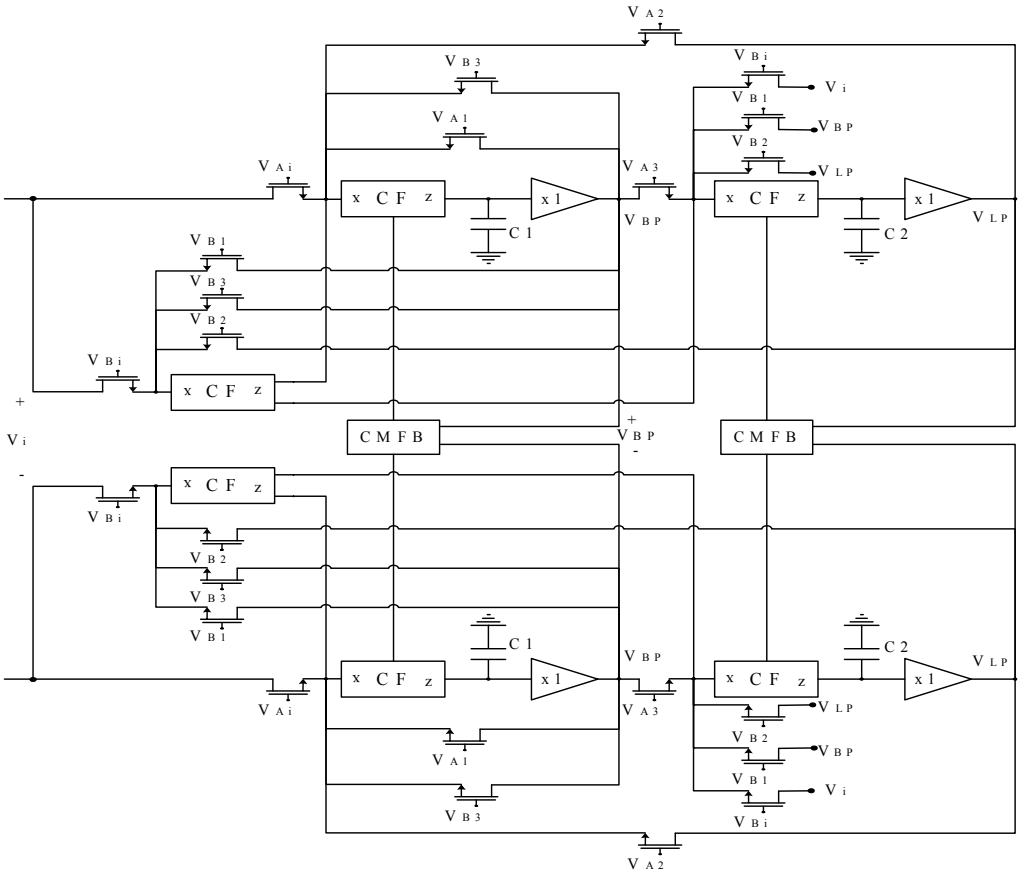


Figure 3.11: Fully Differential Second Order Bandpass Filter with non-linearity cancellation and reduced number of CF (Approach-3)

3.3.4 Comparison

Three approaches have been discussed to construct a CMOS highly linear and low power fully differential bandpass filter. The filter's linearity in approach-1 is dramatically affected by the non-linearity of the MOSFET transistors. Incorporating non-linearity cancellation, in approach-2 enhances the filter's linearity and dynamic range by 6dBm and 2.6dB, respectively. Moreover, active element reduction proposed in approach-3 improves the filter's linearity by 11dBm and 5dBm over approach-1 and approach-2, respectively. Hence, approach-3 dynamic range advances over approach-1 dynamic range by 6.3dB and approach-2 dynamic range by 3.7dB. Table 3.2 summaries the comparison between the discussed approaches.

Table 3.2: Fully Differential Approaches Comparison

Approach #	**Noise** ($nV/\sqrt{Hz}$)	**IP3** **(dBm)**	$DR = \frac{2}{3}(IP3 - NF)$ **(dB)**	**Current Cons.** **(mA)**
1 (4 CFs)	106.2	16	63.7	1.04
2 (8 CFs)	133.5	22	66.3	1.48
3 (6 CFs)	126.9	27	70	1.26

3.3.5 Selection of Common mode feedback (CMFB) topology

The number of CMFB circuit in high order filter can be further reduced as will be shown in the power optimization section. The filter in Fig. 3.11 is a two-integrator loop filter; it is a two stage filtering circuit. The filter design is incorporating two CMFB

circuits. Although CMFB circuitry helps in increasing common-mode rejection ratio - CMRR- and establishing the common-mode output voltage, the CMFB circuitry is often a source of noise injection and more power consumption [10]. Hence, reducing the number of used CMFB circuitry is a goal to minimize the consumed power and the total filter noise without affecting the CMRR.

The proposed bandpass filter in Fig. 3.11 can be restructured in simplified general structure as shown in Fig. 3.12(a). It is clear that every output voltage of the integrators is corrected using independent CMFB circuit. Different topologies for single CMFB may be used instead, Fig.3.12 (b, c, d).

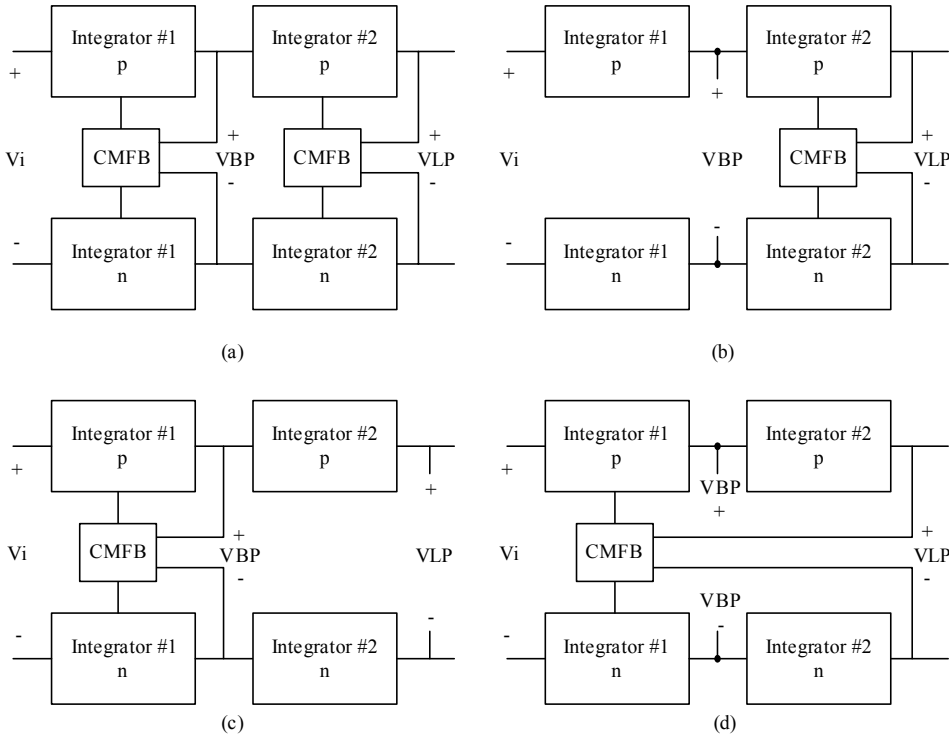


Figure 3.12: Four possible CMFB topologies, simplified filter structure

While the CMRR and the input-referred-noise for the proposed bandpass filter topology (a) is -40dB and 126.9 $nV/\sqrt{Hz}$ respectively, the resulted CMRR and the input-refereed noise for topology (d) are -38dB and 124.2 $nV/\sqrt{Hz}$ with current consumption of 1.18 mA. Comparing topology (a) and (d) shows that the CMRR of topology (d) was degraded by 2dB while the current saving was 6.8%. Table 3.3 summarizes the different topologies characteristics.

Table 3.3: CMFB topologies Comparison

Topology	CMRR (dB)	Noise $(nV/\sqrt{Hz})$	Current Cons. (mA)
(a)	-40	126.9	1.26
(b)	-36	130.1	1.18
(c)	-34	128.2	1.18
(d)	-38	124.2	1.18

3.3.6 Further performance improvements

The second order Opamp based Tow-Thomas biquad, Fig. 3.8(a), consists of three stages. The last stage is an inverter stage to establish the negative feedback. However, the same filter based on unity gain cells, Fig. 3.8(b), incorporates positive and negative type of CF to establish the negative feedback. The terminal currents of the positive CF are both entering or leaving, while the direction of the current is inverted in the negative CF. To avoid design complication, a positive CF may be used instead with

replacing either R_2 or R_3 with a negative resistance. Negative resistance can be implemented by MOSFET resistors easily by applying $V_B > V_A$ in equation (3.6). Moreover, fully differential architecture initiates another technique to replace the inverting stage. This may be achieved by cross-coupling between the output terminals. Table 3.4 illustrates the major variations in the filter's parameters due to different feedback topologies. Although the cross-coupling topology results in improved dynamic range by 1dB over –*R2* topology, it may cause complexity in the IC layouting.

Table 3.4: Negative feedback topologies

	Noise ($nV/\sqrt{Hz}$)	**IP3** **(dBm)**	**DR** **(dB)**
-R2	126.9	27	70
-R3	198.9	26	66
Cross- coupling	122.4	28	71

Furthermore, there is a relation between the proposed filter gain and its input-referred noise. Table 3.5 shows that for a high input resistance the filter's input-referred noise is increased and the gain is decreased and vise versa.

Table 3.5: Gain noise relation

R_i	**Gain** **(dB)**	**Noise** ($nV/\sqrt{Hz}$)	**IP3** **(dBm)**	**DR** **(dB)**
Higher	0	241.2	28	65.6
Lower	15	52.3	26	76

3.3.7 Summary

The proposed cascadable second order bandpass filter supposed to exhibit high dynamic range and minimum power consumption. Introducing MOSFET resistors, for filter programmability, results in adding undesired non-linearity to the filter. The proposed non-linearity cancellation technique adds more circuitry to the filter in the form of active elements providing more noise. Additional active elements reduction was proposed and results in better performance. Furthermore, optimizations of CMFB circuitry shares in reducing power consumption.

CHAPTER 4

BANDPASS FILTER BASED ON VOLTAGE BUFFER

4.1 Introduction

In chapter 3, two methods were proposed to provide programmability features to the two-integrator loops filter based on unity-gain cells. They use either one or two MOSFETs to replace each passive resistor. The later approach results in higher dynamic range particularly after CFs reduction. However, the former approach is simpler and uses less number of MOSFETs and active elements. It is expected that incorporating this approach on other filter topologies, that use less active elements per biquad, would result in improved designs. Sallen-Key (SK) filters are attractive as they utilize a single voltage amplifier to implement cascadable continuous-time biquad filter sections. Buffer based SK filters are characterized by wide bandwidth, low noise, high linearity and low power consumptions [7, 32].

The goal of this chapter is to propose a new filter design based on voltage buffer and investigate its possible performance improvements. It is expected that this technique will exhibit improved power consumption and less area compared with the unity-gain cells approach. To provide programmability to the buffer based proposed filter, single

MOSFET resistor replacement method will be employed. Although the linearity of the filter will be degraded significantly, design techniques are proposed to circumvent this problem and make the eventual design satisfying specifications of the Bluetooth with higher dynamic range and lower power consumption.

4.2 Second Proposed Approach

Ideally, buffer circuits transfer voltage signals between different circuit blocks without loading effects. Basically, voltage buffers are required to exhibit accurate input-to-output voltage tracking, high input impedance, and low output impedance. High performance analog integrated circuits incorporate fully differential signal path. The fully differential operation improves the performance of mixed analog/digital systems in terms of supply noise rejection, dynamic range and harmonics distortion [7, 8, and 34].

Single-ended opamps based circuits can be systematically converted to their fully differential structure counterparts if each opamp has a grounded input terminal. Conversely, SK filter topologies based on voltage buffers do not satisfy the previous condition. As a result, a fully differential buffer based Sallen-Key filters, a fully differential voltage buffer (FDVB) circuit is required to be developed.

4.2.1 Fully differential voltage buffer

A high performance buffer circuit is realized by connecting an opamp in unity gain negative feedback configuration as shown in Fig. 4.1(a). By definition, the fully

balanced version of a voltage buffer is a four terminals device whose symbol is shown in Fig. 4.1(b). It terminal characteristics are given by the following relations:

$$V_{od} \equiv V_{op} - V_{on} = V_{id} \equiv V_{ip} - V_{in} \qquad (4.1)$$

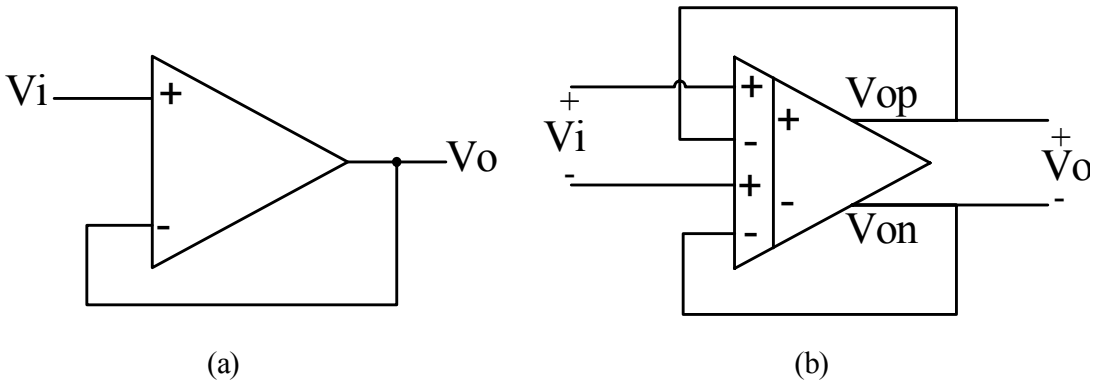


Figure 4.1: Voltage Buffer: (a) single-ended (b) fully differential

Systematically, the single voltage buffer circuit of Fig. 4.1(a), can be extended to fully balanced operation by implementing the following modifications: First, two differential input ports are required rather than two single –ended inputs. Second, two fully balanced outputs of the opamp are needed instead of a single-ended output. Following this procedure results in developing a fully differential voltage buffer (FDVB) based on what is known as fully balanced differential difference amplifier (FBDDA) [30] and symbolically shown in Fig. 4.2(a).

A CMOS circuit realization of a FBDDA is shown in Fig. 4.2(b). It consists of two differential input stages with active loads and common-source amplifiers with active loads as output stages. For lower power operation and high current driving capabilities, a class-AB output stage is employed instead of the conventional class-A counterpart.

The two input stages convert the input voltages into two currents that are subtracted and converted to voltage by the active load and amplified by the output stage. The resulted fully balanced outputs are given by:

$$V_{op} = -V_{on} = A_0 \left[\left(V_{pp} - V_{pn} \right) - \left(V_{np} - V_{nn} \right) \right] \tag{4.2}$$

where A_o is the differential open-loop gain of the FBDDA. Analogues to the traditional op-amp, when a negative feedback is applied the voltages of the two input ports become equal:

$$(V_{pp} - V_{pn}) = (V_{np} - V_{nn}) \qquad as \quad A \to \infty \tag{4.3}$$

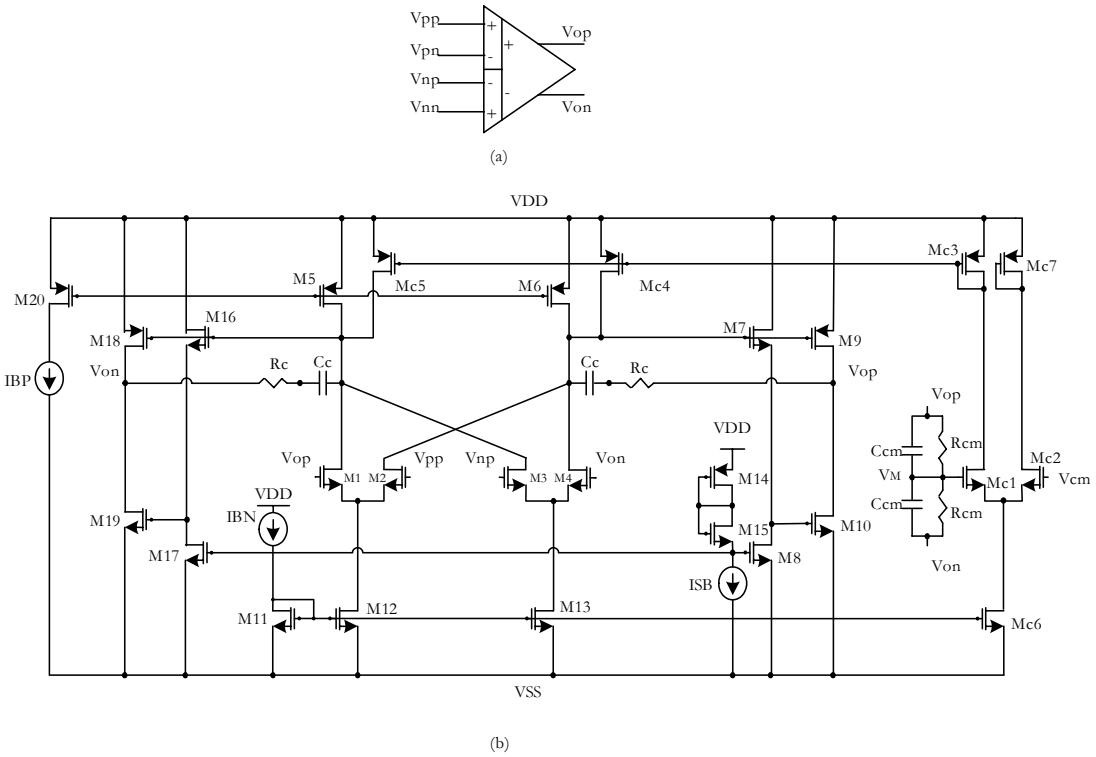


Figure 4.2: FBDDA: (a) symbol (b) CMOS realization

Compensation capacitor (Cc) and resistor (Rc) are employed to ensure the FBDDA stability. The output stages are consisting of transistors M7-M10, and M16-M19 for positive and negative outputs, respectively. Transistors M14-M15 are for class AB biasing. A CMFB establishes the common-mode output voltage level. When dual supply voltages are used, V_{cm} is set to zero. The CMFB circuit is consisting of transistors Mc1-Mc7 in addition to two resistors (R_{cm}) and two capacitors (C_{cm}) used to sense the output voltage (V_{op} and V_{on}) common-mode level.

FBDDA can be configured as a unity gain voltage buffer by connecting it in unity gain negative feedback structure. Unlike the conventional opamp, more than one configuration may be connected to establish the negative feedback. To behave as a conventional opamp, the feedbacks are applied to each of the input pairs locally, i.e. each output is fedback to the corresponding negative input terminal, Fig 4.3. Simulation and experimental results in [33] show that this configuration has much wider linear input differential range.

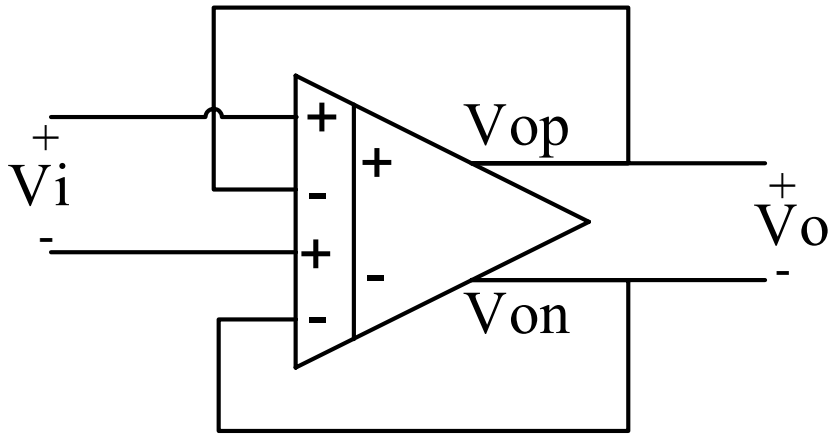


Figure 4.3: Optimum unity negative feedback configuration

4.2.2 Tunable feature implementation

Accurate frequency characteristics are required for successful IF channel select and filtering out the undesired signals. The filter parameters are affected by variations in the time constants of the filter due to changes in the capacitance or the resistance values. This change may reach more than 50% due to process variation [6, 7, and 8]. MOSFET-C technique can be simply used to provide programmability features to their active RC counterparts [36]. The simplest way of applying MOSFET-C technique is to replace all passive resistors in RC active filters by MOSFETs operating in triode region. Hence, MOSFETs provide the filter with programmable parameters that can be tuned electronically by varying their gate voltages.

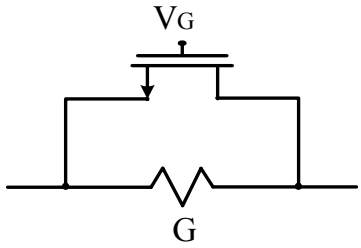


Figure 4.4: Proposed tunable resistor

The even terms are cancelled due to the nature of the fully differential structure. On the other hand, the considerably smaller odd terms are still present. Hence, the filter may not be suitable for rejection of large out-of-band signals. This obstacle can be circumvented by designing a highly linear pre-filter that eliminates the out-of-band blockers [30]. To further absorb this problem, MOSFET-C transistors are placed in parallel as shown in Fig. 4.4 (rather than exchanging them) with the passive resistors trading off some of the tuning range for better linearity performance. The resulting

conductance will be the parallel combination for the silicon conductance (G) and the transistor conductance.

4.3 Proposed Bandpass Filter Based on Voltage Buffer

The equivalent circuit of SK bandpass biquad is shown in Fig. 4.5(a). It uses minimum number of passive elements (i.e. four) and requires an inverting amplifier of gain $= -k$ [33]. Thus, it cannot be implemented using a voltage buffer in single ended topology. The filter of Fig. 4.5(b), overcomes this problem but by using more passive elements [37]. In fully differential architecture, however, the unity gain inverting buffer can be realized by cross-coupling the outputs.

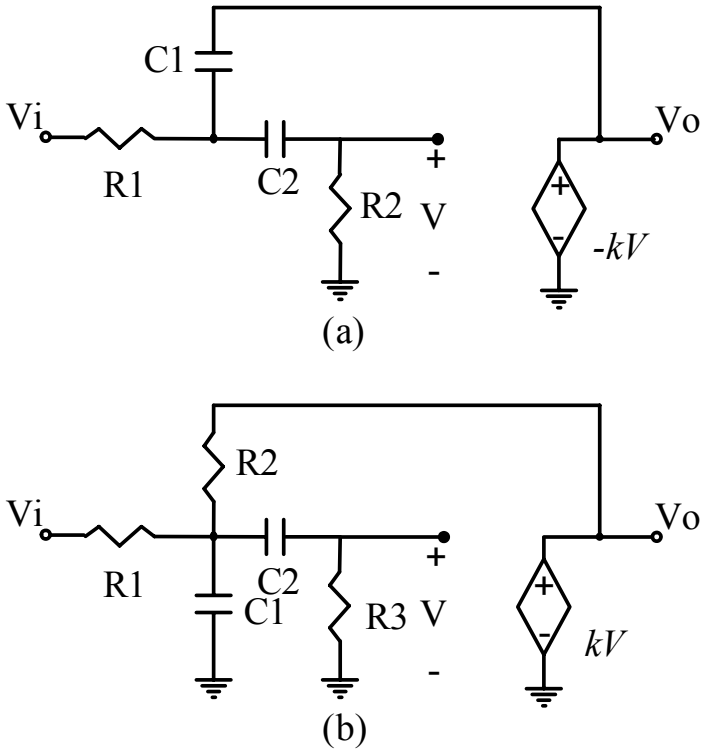


Figure 4.5: Sallen-Key bandpass filters

The transfer functions of these bandpass filters with k=1 are given by:

$$\frac{V_o}{V_i} = \frac{-2C_2R_2}{s^2 + s\left(C_1R_1 + C_2R_2 + C_2R_1\right) + 2C_1C_2R_1R_2} \qquad (4.4.a)$$

$$\frac{V_o}{V_i} = \frac{\dfrac{s}{R_1C_1}}{s^2 + s\left(\dfrac{1}{R_1C_1} + \dfrac{1}{R_3C_1} + \dfrac{1}{R_3C_2}\right) + \dfrac{R_1 + R_2}{R_1R_2R_3C_1C_2}} \qquad (4.4.b)$$

Unluckily, it can be seen that the gains of both filters are less than unity. Hence, cascading biquads based on either topology will result in a bandpass filter with high passband attenuation. On the other hand, the gains of the SK lowpass and highpass filters shown in Fig. 4.6 are ideally equal to unity. Thus, cascading these filter sections provides an alternative approach to construct a high-order bandpass filter without passband attenuation.

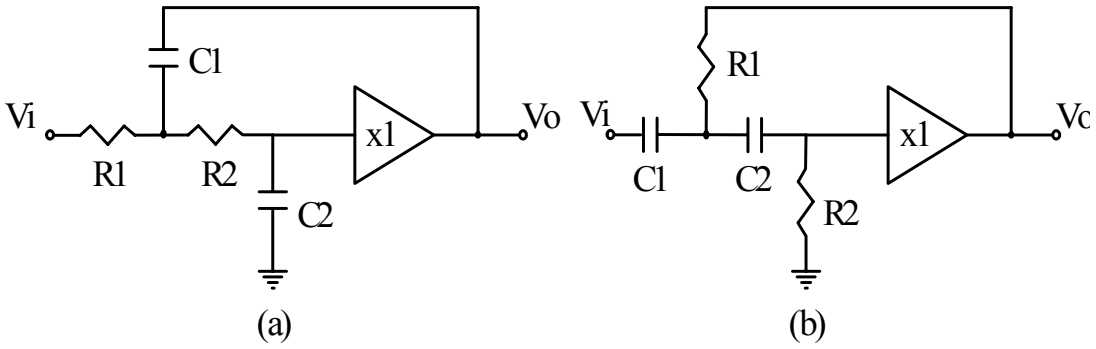


Figure 4.6: SK filters (a) second-order lowpass (b) second-order highpass

A fourth-order SK fully differential bandpass filter using poly-silicon resistors is shown in Fig. 4.7. The Spice simulations show that its input referred noise of

$123\,nV/\sqrt{Hz}$ and IP3 is 31.3dBm when f_c = 3MHz and BW = 1MHz are achieved. The filter exhibits a visibly high linearity posting the dynamic range to approximately 73dB.

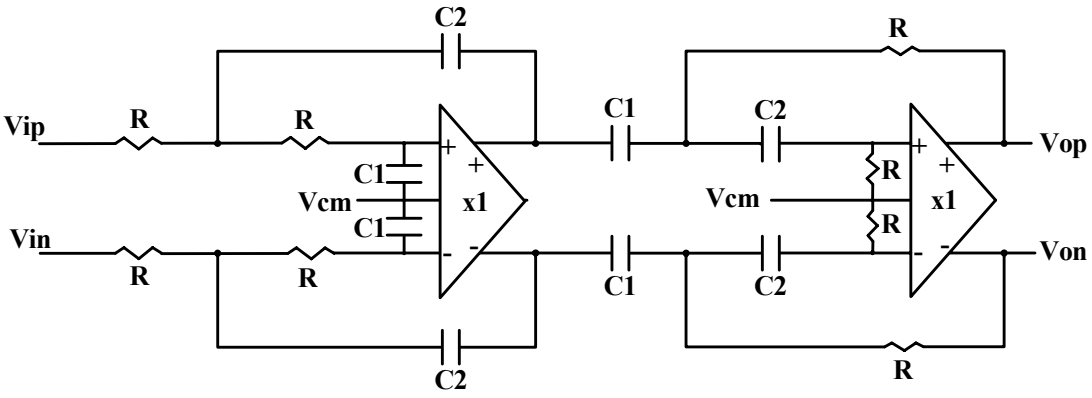


Figure 4.7: SK BPF using poly silicon resistors

Programmability is introduced to the filter by connecting a MOSFET in parallel with each resistor. Simulation results show that the filter exhibits almost the same noise performance. Whereas the recorded IP3 is lower than that of the passive filter by 6.5dB. Thus, its dynamic range is lowered by 4.5dB. Table 4.1 summarizes these characteristics.

Table 4.1: The effect of adding MOSFET tunablity featuer to passive resistors BPF based on voltage buffers

	I. R. Noise ($nV/\sqrt{Hz}$)	IP3 (dBm)	DR (dB)	Current Cons. µA
Passive resistors	123	31.3	73	200
MOSFETs + resistors	126	24.8	68.5	200

4.4 Simple Automatic Frequency Tuning Circuit

Unlike the switched-capacitor filters, all analog filters exhibit inaccurate frequency characteristics. The center frequency f_o, which depends on RC or g_m-C factors, can vary up to 50% due to process variation and parasitics. Therefore automatic tuning of f_o has to be employed. For most of the automatic tuning circuits, the idea of master-slave controlling is used. The master filter refers to the one in the automatic tuning loops while the slave filter refers to the main filter. The idea assumes that both the master and slave filters center frequency are matched. Therefore, by using the same control voltage that controls the master filter, to control the slave filters, both filters should show the same characteristics. [7, 8, 37]

Several automatic frequency tuning circuits were presented, such as in [14, 37, and 38]. Those works were based on delay-looked-loop (DLL) and phase-looked-loop (PLL). They are involving complex circuitry design such as voltage-controlled-oscillator (VCO), phase detector (PD), comparators and other elements. Therefore, automatic tuning circuit consumes extra current, which will increase the filter's power consumption. As an example, in [14] the frequency tuning circuit consists of a relaxation oscillator, two counters, a comparator, an up-down counter and a digital-to-analog converter consuming 0.8 mA which equals to 18% of the filter's current.

Using switched-capacitor circuit and a reference clock frequency, f_{CLK}, a simple frequency tuning circuit can be built, Fig. 4.8 [39]. The equivalent resistance of the precise switched-capacitor resistor is given by $R_{eq} = 1/(f_{CLK}C_m)$. Where V_B is a DC value,

the integrator will result in a steady, V_C, when the transconductance value, G_m, is set to $f_{CLK}C_m$.

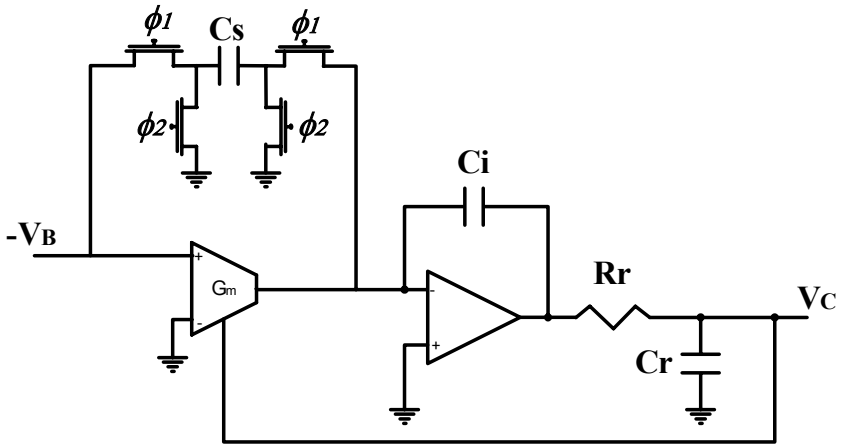


Figure 4.8: Simple automatic frequency tuning circuit

The proposed frequency tuning circuit is obtained by replacing the switched-capacitor resistance with the modified negative resistor, $R_{eq}= -1/(f_{CLK}C_m)$, by exchanging the positions of switches while the positive resistance will consists of the nominal value of the filter resistor and the controlling MOSFET. The integrator output will adjust the gate voltage for the MOSFET until the parallel combination of the positive resistor equal to $f_{CLK}C_m$.

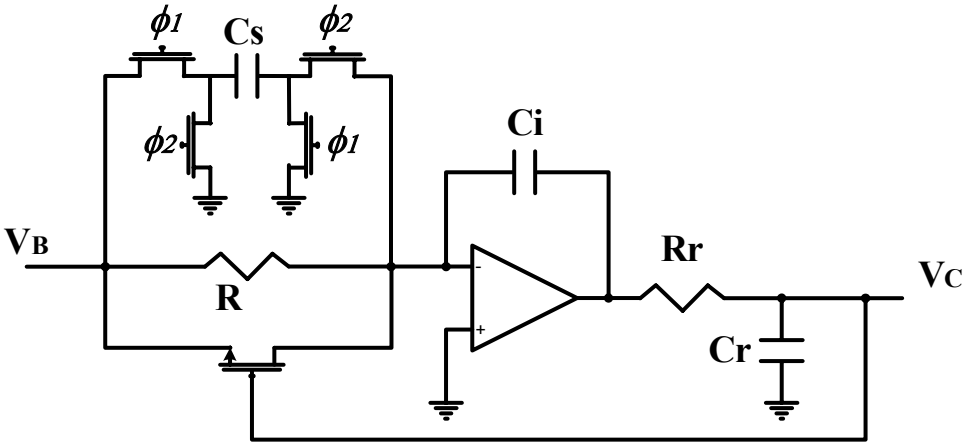


Figure 4.9: Proposed simple automatic frequency circuit

CHAPTER 5

PROPOSED HIGH ORDER FILTER DESIGNS FOR BLUETOOTH

5.1 Introduction

Bluetooth low-IF scheme requires a bandpass filter with high selectivity. The filter is required to provide at least 0dB, 30dB and 40dB attenuations for blockers with offset frequencies of 1MHz, 2MHz and 3MHz, respectively. High order filter designs are required to meet these specifications. Linearity, noise, group delay, area and power consumption are other important design parameters. Filters presented in [10, 13, 14 and 15] oversatisfy the selectivity requirements by designing very sophisticated circuits. Therefore, their circuits turn to be power consumption hungry. This thesis proposes two approaches to implement the IF bandpass filter for Bluetooth. High-order filters achieving the desired selectivity are designed by cascading second-order sections based on unity gain cells or voltage buffers.

5.2 High Order BPF Based on Unity-Gain Cells

The first proposed filter is based on the biquad of Fig. 3.11 that uses unity gain cells as building blocks. The ac responses of the filter for different center frequencies and quality factors were explored using SPICE. The proposed filter was submitted for fabrication in a standard 0.5-μm CMOS technology available through MOSIS. Simulation results using manufacturer BISM3V3 CMOS models (see Appendix A) are obtained. It was found that cascading five of these sections provides the required Bluetooth selectivity as shown in Fig. 5.1. The filter center frequency is 3MHz and its bandwidth is 1MHz. The filter provides attenuations of 14, 34, 48dB for blockers at 4, 5, and 6MHz, respectively. The filter input-refered-noise, IP3 for near blockers and group delay are found to $191.4 nV/\sqrt{Hz}$, 48.7dBm and 0.81μs respectively. These values result in a dynamic range of about 82.1dB. Although the filter exhibits high dynamic range, the over all current consumption is 5.9mA or 0.295mA per pole.

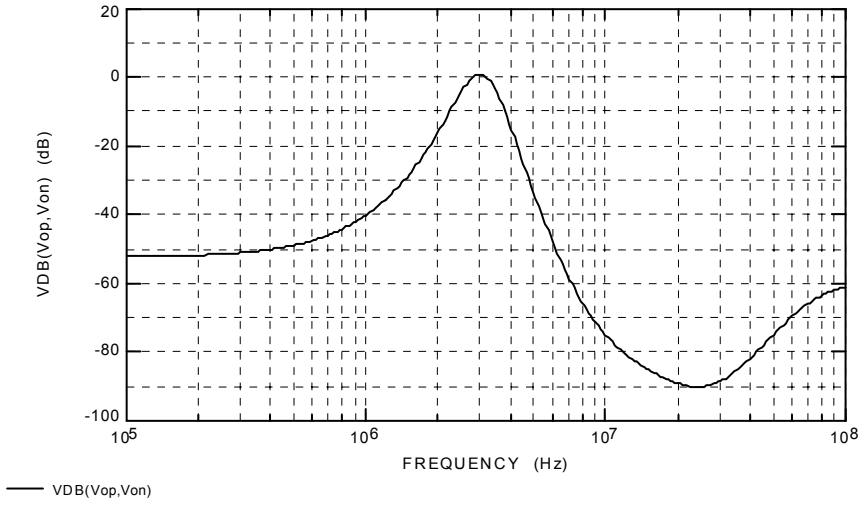


Figure 5.1: The simulated ac response of the first proposed BPF based on unity-gain cells

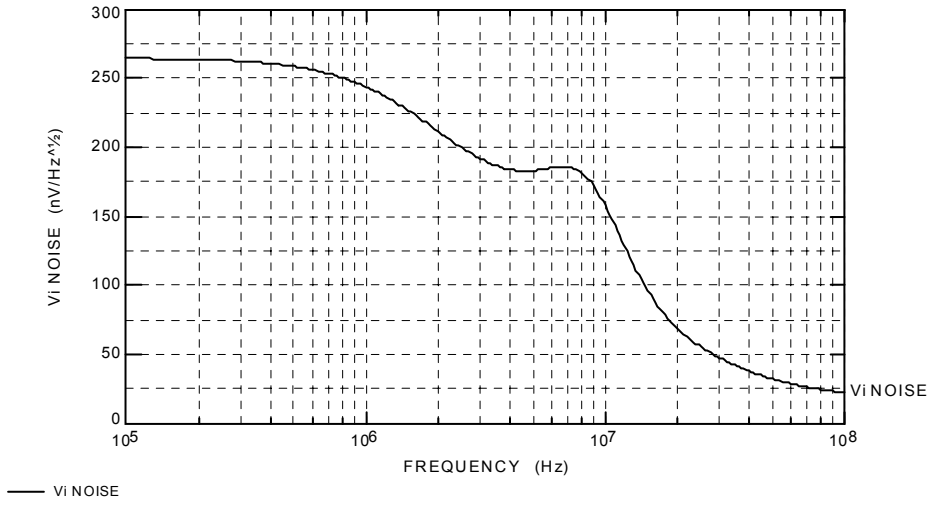


Figure 5.2: The simulated input-refeered-noise of the first proposed BPF based on UGC

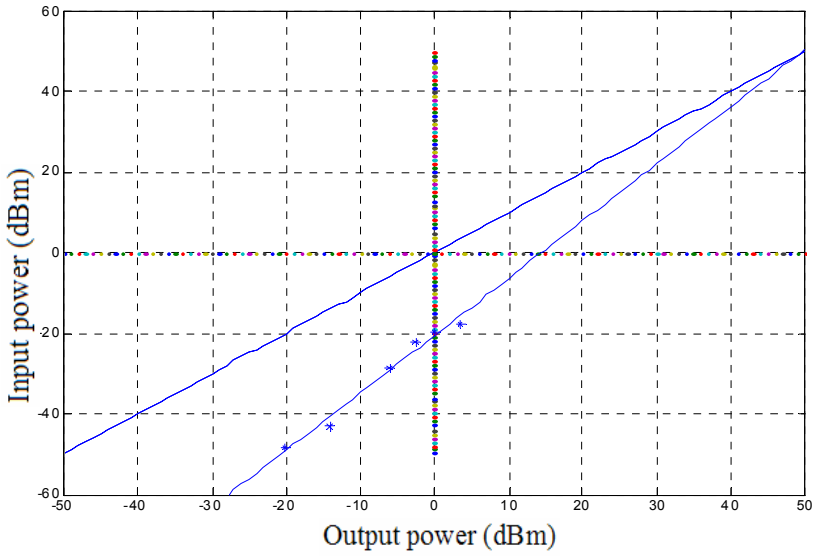


Figure 5.3: The simulated IP3 of first proposed BPF based on unity-gain cells

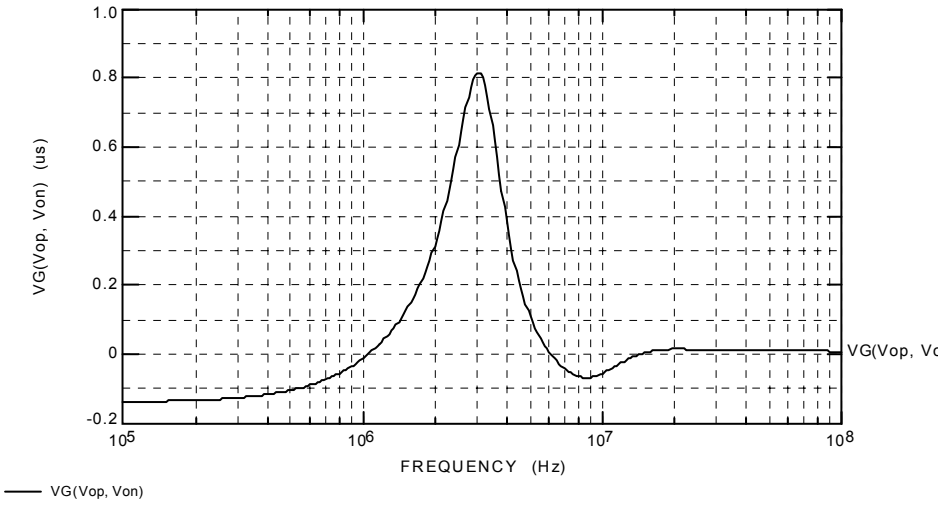


Figure 5.4: the group delay of the first proposed BPF based on unity-gain cells

5.3 High Order BPF Based on Voltage buffers

The second proposed filter is based on Sallen-Key lowpass and highpass biquads, shown in Fig. 4.7. The proposed buffer based filter will satisfy the low-frequency requirements using SK highpass filter biquads, while the high-frequency side will be attenuated by SK lowpass filter biquads. The required Bluetooth selectivity is achieved by cascading two highpass and four lowpass biquads. The highpass filter sections are placed at front and rear ends of the proposed design to prevent any DC offset leakage from the preceding receiver stages or to the subsequent stages. The programmability is introduced to one highpass filter and two lowpass filters at the end of the proposed structure, as shown in Fig. 5.5, to minimize the MOSFET non-linearity effects on the filter's performance.

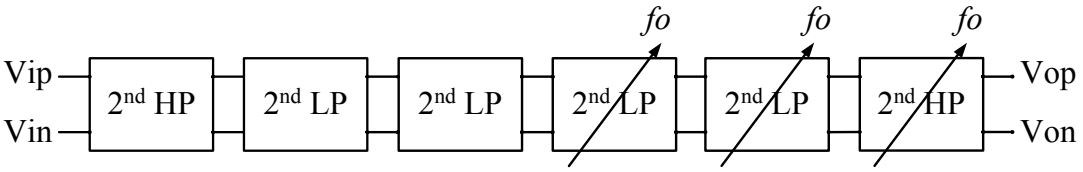


Figure 5.5: Building block for the proposed BPF based on voltage buffers

The proposed filter was submitted for fabrication in a standard 0.5-μm CMOS technology available through MOSIS. The ac response of the proposed 12th-order filter, using manufacturer CMOS transistor models, is shown in Fig. 5.6. The filter center frequency is 3MHz and its bandwidth is 1MHz. The filter provides attenuations of 10, 33, 47dB for blockers at 4, 5, and 6MHz, respectively. The filter input-refereed-noise, IP3 for near blockers and group delay are found to $132.5 nV/\sqrt{Hz}$, 33.6dBm and 0.68μs respectively. These values result in a dynamic range of about 74.1dB. The

filter exhibits high dynamic range, the over all current consumption is 0.648mA or 27µA per pole.

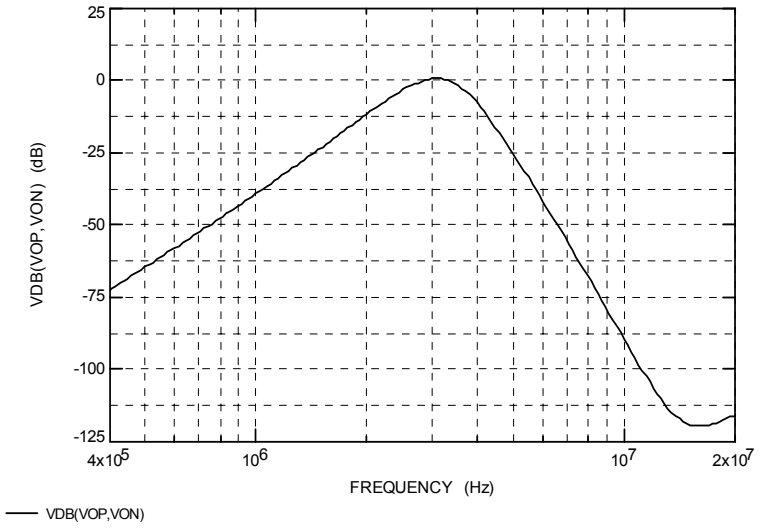


Figure 5.6: The simulated ac response of the proposed BPF based on voltage buffers

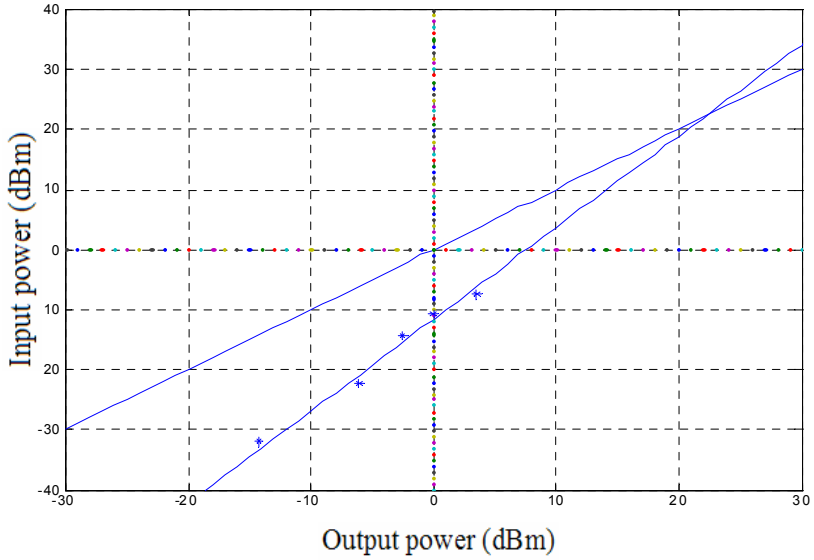


Figure 5.7: The simulated IP3 of the proposed BPF based on VB

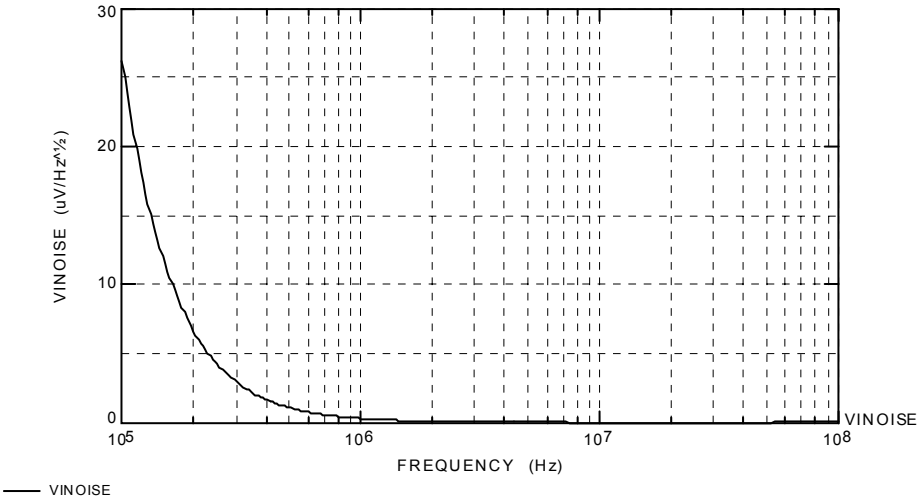


Figure 5.8: The simulated input-refereed-noise of the proposed BPF based on voltage buffers

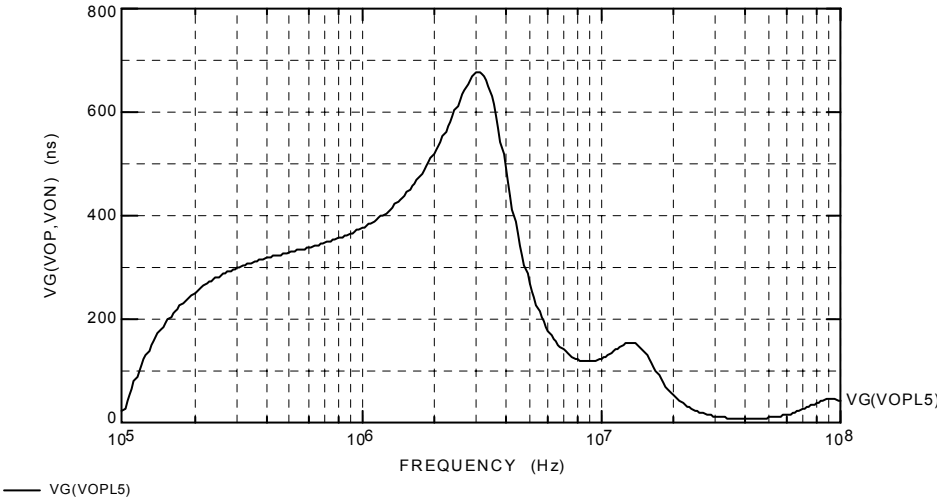


Figure 5.9: The simulated group delay of the proposed BPF based on voltage buffers

CHAPTER 6

CONCLUSION

Fully integrated low-IF Bluetooth receiver requires replacement of the discreet high-Q IF bandpass filter by its integrated counterpart. The RF signal is down-converted without any channel filtering. As a result, strong adjacent interferers can be present along with the desired channel. The main focus is to implement CMOS fully integrated filters meeting selectivity and dynamic range specifications of Bluetooth. Two new CMOS programmable bandpass filters are proposed. The filters are realized with center frequency of 3MHz and bandwidth of 1MHz. The proposed filtering techniques satisfy the required selectivity and dynamic range with improved power consumption and chip area compared with previously published works.

The first proposed filter is based on unity-gain cells. MOSFET linearized resistors are employed to introduce programmability to the filter. A 10th-order bandpass filter is found to meet the selectivity requirements of Bluetooth as stated in table 2.1. The filter considerably over satisfies the required dynamic range by about 32dB due to the utilization of an effective MOSFET non-linearity cancellation method. The proposed filter exhibit a tuning range from 2.5MHz to 3.5MHz for its center frequency.

However, the filter is based on several active elements per biquad which consume a relatively high supply current.

The second proposed filter is based on a single voltage buffer per biquad. Hence, it provides a considerably improved performance in terms of power consumption. A 12^{th}-order filter satisfying Bluetooth selectivity with current consumption of only 0.65mA is presented. Although using non-linear MOSFET resistors for introducing programmability is expected to degrade the filter linearity, special circuit methods are used to releve its effects. As a result, the filter exhibits a dynamic range of approximately 74dB, which is 24dB higher than what is required.

The performance characteristics of the proposed filters are summarized and compared with their counterparts published in [10, 14 and 15] in Table 6.1. Clearly, the simulation results of the proposed filters in this thesis exhibit relatively high dynamic ranges. The filter based on unity-gain cells consumes comparable power consumption while the filter based on voltage buffer is superior in this regard. It exhibits power consumption saving of 73% and 87% compared with filers of [10] and [14], respectively. In addition, if more selectivity is desired, it can be easily achieved by cascading additional biquad sections. Simulation results shows that the proposed filter based on voltage buffer achieves the high selectivity associated with the filters in [14], and [10], using ten-order and twelve-order biquad filter sections, respectively. This would results in significant save of 40% to 50% of the power consumption.

The proposed filters were submitted to fabrication in a standard 0.5-μm CMOS technology available through MOSIS. Fabrication process takes more than fourteen weeks. A network analyzer, a DC analyzer and robust IF signal generators are required to obtain complete and reliable experimental results. Whenever, it is possible the fabricated chips will be tested.

The proposed filter based on voltage buffers exhibits superior performance with very low power consumption. Applying this approach to design filters for other applications such as wireless LAN and WCDMA, **W**ideband **C**ode **D**ivision **M**ultiple **A**ccess, receivers seems to be promising. Further research on utilizing voltage buffer as basic building block in other filtering techniques is under investigation.

Table 6.1: Comparision between the proposed and the previously presinted BPF

Parameters	Specification	Proposed BPF -1*	Proposed BPF -2*	Ericsson-Lund [10]**	Motorola-Texas A&M [14]**
Approach	-------	CFVB	VB	g_m-C	g_m-C
Order	-------	10th	12th	18th	12^{th}
Current	Minimum	5.9mA	0.648mA	2.4mA	4.7mA
I/Pole	Minimum	0.59mA	0.027mA	0.133mA	0.392mA
f_c	IF	3MHz	3MHz	3MHz	3MHz
Pass band gain	----	≈0dB	≈0dB	≈0dB	15dB
Group delay	<1μs	0.76 μs	0.68 μs	1 μs	0.6 μs
1st blocker attenuation	0dB	14dB	10dB	47dB	29dB
2nd blocker attenuation	30dB	34dB	33dB	----	58dB
3rd/more blocker attenuation	40dB	48dB	47dB	----	----
Input referred Noise	----	191.4 nV/$\sqrt{Hz}$	132.5 nV/$\sqrt{Hz}$	250 μV/$\sqrt{Hz}$	29 μV/$\sqrt{Hz}$
IP3		48.7dBm	33.6dBm	74dBm	30dBm
IP3-Noise (referred to 50Ω)	>75dB	123.1dB	111.2dB	87dB	61.1dB

* based on simulation results
** based on experimental results

APPENDIX A

The CMOS transistors model used in the filters simulations:

.MODEL NPN NMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 1.41E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.7086 K1 = 0.8354582 K2 = -0.088431 K3 = 41.4403818 K3B = -14 W0= 6.480766E-7 NLX = 1E-10 DVT0W = 0 DVT1W = 5.3E6 DVT2W = -0.032 DVT0 = 3.6139113 DVT1 = 0.3795745 DVT2 = -0.1399976 U0 = 533.6953445 UA = 7.558023E-10 UB = 1.181167E-18 UC= 2.582756E-11 VSAT = 1.300981E5 A0= 0.5292985 AGS = 0.1463715 B0 = 1.283336E-6 B1 = 1.408099E-6 KETA = -0.0173166 A1 = 0 A2 = 1 RDSW = 2.268366E3 PRWG = -1E-3 PRWB = 6.320549E-5 WR = 1 WINT = 2.043512E-7 LINT= 3.034496E-8 XL = 0 XW = 0 DWG = -1.446149E-8 DWB = 2.077539E-8 VOFF = -0.1137226 NFACTOR = 1.2880596 CIT = 0 CDSC = 1.506004E-4 CDSCD = 0 CDSCB = 0 ETA0 = 3.815372E-4 ETAB= -1.029178E-3 DSUB = 2.173055E-4 PCLM= 0.6171774 PDIBLC1 = 0.185986 PDIBLC2 = 3.473187E-3 PDIBLCB = -1E-3 DROUT = 0.4037723 PSCBE1 = 5.998012E9 PSCBE2 = 3.788068E-8 PVAG = 0.012927 DELTA= 0.01 MOBMOD = 1 PRT= 0 UTE= -1.5 KT1= -0.11 KT1L = 0 KT2= 0.022 UA1= 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT= 3.3E4 WL = 0 WLN= 1 WW = 0 WWN= 1 WWL= 0 LL = 0 LLN = 1 LW= 0 LWN = 1 LWL= 0 CAPMOD = 2 XPART= 0.4 CGDO= 1.99E-10 CGSO= 1.99E-10 CGBO= 0 CJ= 4.233802E-4 PB = 0.9899238 MJ= 0.4495859 CJSW= 3.825632E-10 PBSW= 0.1082556 MJSW=

0.1083618 PVTH0= 0.0212852 PRDSW= -16.1546703 PK2 0.0253069 WKETA = 0.0188633 LKETA= 0.0204965)

.MODEL PNP PMOS (LEVEL = 49 VERSION = 3.1 TNOM = 27 TOX = 1.41E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9179952 K1 = 0.5575604 K2 = 0.010265 K3 = 14.0655075 K3B = -2.3032921 W0 = 1.147829E-6 NLX = 1.114768E-10 DVT0W = 0 DVT1W = 5.3E6 DVT2W = -0.032 DVT0 = 2.2896412 DVT1 = 0.5213085 DVT2 = -0.1337987 U0 = 202.4540953 UA = 2.290194E-9 UB = 9.779742E-19 UC = -3.69771E-11 VSAT = 1.307891E5 A0 = 0.8356881 AGS = 0.1568774 B0 = 2.365956E-6 B1 = 5E-6 KETA = -5.769328E-3 A1 = 0 A2 = 1 RDSW = 2.746814E3 PRWG = 2.34865E-3 PRWB = 0.0172298 WR = 1 WINT = 2.586255E-7 LINT = 7.205014E-8 XL = 0 XW = 0 DWG = -2.133054E-8 DWB = 9.857534E-9 VOFF = -0.0837499 NFACTOR = 1.2415529 CIT = 0 CDSC = 4.363744E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.11276 ETAB = -2.9484E-3 DSUB = 0.3389402 PCLM = 4.9847806 PDIBLC1 = 2.481735E-5 PDIBLC2 = 0.01 PDIBLCB = 0 DROUT = 0.9975107 PSCBE1 = 3.497872E9 PSCBE2 = 4.974352E-9 PVAG = 10.9914549 DELTA = 0.01 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN

= 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.4 CGDO = 2.4E-10 CGSO = 2.4E-10 CGBO = 0 CJ = 7.273568E-4 PB = 0.9665597 MJ = 0.4959837 CJSW = 3.114708E-10 PBSW = 0.99 MJSW = 0.2653654 PVTH0 = 9.420541E-3 PRDSW = -231.2571566 PK2 = 1.396684E-3 WKETA = 1.862966E-3 LKETA = 5.728589E-3)

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