A Programmable Self-Adjusting SCR-Based AC Voltage Regulator

by

Fouad Ali H. Al-Saif

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

June, 1994

Order Number 1360386

A programmable self-adjusting SCR-based AC voltage regulator

Al-Saif, Fouad Ali H., M.S.

King Fahd University of Petroleum and Minerals (Saudi Arabia), 1994

U·M·I
300 N. Zeeb Rd.
Ann Arbor, MI 48106

A PROGRAMMABLE SELF-ADJUSTING SCR-BASED AC VOLTAGE REGULATOR

BY

FOUAD ALI H. AL-SAIF

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE
In

ELECTRICAL ENGINEERING

June, 1994

KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
DAHARAN, 31261, SAUDI ARABIA

COLLEGE OF GRADUATE STUDIES

This thesis, written by Fouad Ali Hasan Al-Saif under the direction of his thesis advisor and approved by his thesis committee, has been presented to and accepted by the dean of the College of Graduate Studies, in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE.

Thesis committee

Thesis Chairman

Thesis Co-Chairman

Member

Member

Department Chairman

Dean, College of Graduate Studies

29. 6. 02

Date

كلية الدراسات العليا
COLLEGE OF GRADUATE STUDIES

To my parents who did it all on their own.

ACKNOWLEDGMENTS

I would like to express my deep appreciation and gratitude to Dr. A. Al-ALi for his generous support and encouragements throughout this thesis.
I also would like to express my gratefulness to Dr. I. El-Amin for his valuable suggestions and helpful remarks.
I also thank Dr. Z. Al-Akhadar and Dr. J. Zrida for their time and kind co-operation.
Finally, I appreciate the help offered by Mr. I. Al-Rashid and Mr. M. Faraht during the development of the practical part of the thesis.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

NAME: FOUAD ALI H. AL-SAIF.

TITLE: A PROGRAMMABLE SELF-ADJUSTING SCR-BASED AC VOLTAGE REGULATOR.

MAJOR: ELECTRICAL ENGINEERING.

DATE: JUNE, 1994.

The objective of the thesis is to simulate, design and implement a smart ac voltage regulator which maintains load voltage of a circuit within a predetermined range. The regulator consists basically of two thyristors, a signal conditioner circuit and an 8-bit microcontroller.

The regulator is designed to continuously monitor the output voltage across a load. If the monitored load voltage deviates from the predetermined range, the regulator will adjust the firing angles of the thyristors to cope with the deviation in the load voltage. The regulator was tested with resistive and inductive loads. During the tests, the regulator was able to regulate the flow of current from the supply to the load by manipulation of the firing angles of the thyristors

in such a way that the predetermined range is never violated. The accuracy provided by the regulator is quite good (≤ 5 %) from the desirable range. In addition, the regulator provides the flexibility of programming. It also ensures voltage stability, because of its automatic nature and fast response time.

MASTER OF SCIENCE DEGREE

KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS

Dhahran, Saudi Arabia

June, 1994

خلاصة

الأسم : فؤاد علي حسن آل سيف.

العنوان : منظم للجهد الكهربائي المتغير قابل للبرمجة ذاتي التكيف.

التخصص : الهندسة الكهربائية.

التاريخ : يونيو 1994.

الهدف من الرسالة هو محاكاة و تصميم و بناء منظم ذكي للجهد الكهربائي المتغير بحيث يقوم بالمحافظة على مستوى الجهد الكهربائي لحمولة دائرة كهربائية. المنظم الكهربائي المقترح يتكون من ثايرستورين، دائرة مكيفة، و جهاز للتحكم. المنظم الكهربائي مصمم بحيث يرصد الجهد الكهربائي لحمولة الدائرة الكهربائية. عندما ينحرف الجهد الكهربائي عن المستوى المحدد له سابقا، فان المنظم يقوم بتعديل زاوية الفتح لكل ثايرستور ليعيد مستوى الجهد الكهربائي الى المستوى المطلوب. المنظم الكهربائي وضع للاختبار مع عدة دوائر كهربائية ذات حمولات مختلفة، خلال الاختبار قام المنظم الكهربائي بتنظيم التيار من المصدر الكهربائي الى حمولة الدائرة الكهربائية وذلك بضبط زاوية الفتح لكل ثايرستور بحيث أن مستوى جهد الخرج يكون دائما عند المستوى المحدد له سابقا. الدقة التي وفرها المنظم الكهربائي المقترح كانت جيدة جدا، بالاضافة الى ذلك المنظم قابل للبرمجة ويحافظ على ثبات الجهد الكهربائي عند مستوى محدد وذلك لسرعة استجابته للتغيرات التي تطرأ على جهد الخرج للدائرة الكهربائية.

درجة الماجستير في العلوم

جامعة الملك فهد للبترول والمعادن

الظهران ، المملكة العربية السعودية

يونيو 1994

CHAPTER I

INTRODUCTION

1.1 GENERAL

The electrical supply voltage in a large industrial manufacturing complex is often subjected to fluctuation of various magnitudes and frequencies. Potential causes of this problem are recognized to be overloads of transmission lines and generators, line and generator outages, and variation of load with voltage. Furthermore, generator excitation limits and load tap changing transformer actions are also possible causes of the problem. [1]

The fluctuation in the supply voltage causes heavy and inconvenient losses in quality and continuity in the power flow. It also shortens machines' lifetime. In addition, it creates instability in electrical systems. Therefore, there is a strong motivation for controlling and maintaining stable voltages at load nodes. Ac voltage regulators act to recover the normal operating voltages and maintain them within a predetermined range.

1.2 VOLTAGE REGULATORS

An ac voltage regulator is a device which regulates flow of current from an ac voltage source to a load. By doing so, the load voltage can be maintained within a predetermined range, if the regulator is smart enough to sense and respond to any variation in the load voltage [2,3,4,5]. Voltage regulators have a great deal of applications in industry. Industrial heating, induction motor speed control for fan and pump drives, transformer tap changers, ac magnet controls, and light controls are just few examples where voltage regulators are utilized [4,5].

1.3 EXISTING REGULATION TECHNIQUES

Currently, tap changers, which are basically voltage regulators, are used as automatic voltage control systems to maintain the consumer's supply voltage within acceptable limits. There are two types of tap changers:

1) Electromechanical Tap Changer

The tap changing mechanism of this kind is based on an electromechanical arrangement which moves a tap selector up or down in a sequential manner. Fig. 1-1 shows an electromechanical tap changer [9]. One major disadvantage of this technique is that the voltage regulation is done in discrete steps. In addition, the maintenance of the electromechanical tap changer is quite costly. Unfortunately, due to the frequent changes of taps, electrical and mechanical wear are inevitable which will create a need for regular maintenance. In addition, this kind of controllers does not have the accuracy or the speed to cope with any sudden change in the conditions of the circuit because of its mechanical nature [9].

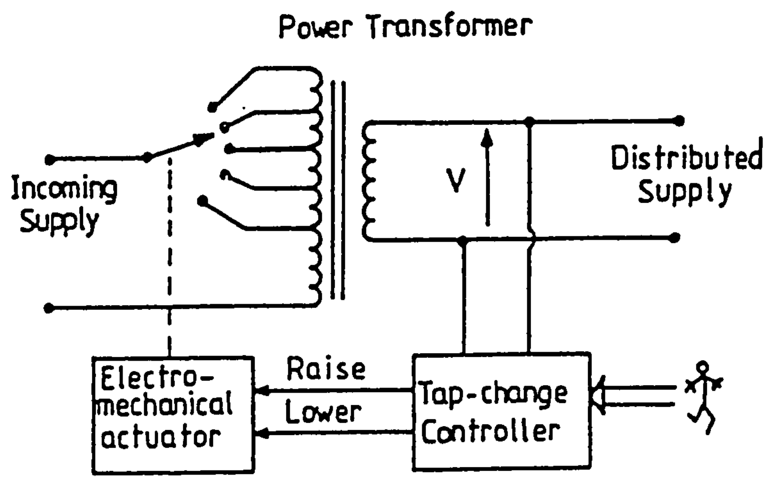


Fig. 1-1 Electromechanical Tap Changer.

2) Thyristor Assisted Tap Changer

Fig. 1-2 shows a thyristor assisted tap changer transformer. This kind of tap changers eliminates the problem of electrical and mechanical wear. It also provides fast switching response because of the utilization of the thyristors. However, it has its own problems. Many of the problems associated with this kind of controllers are due to the method of voltage control in which improper coordination of control signals are employed [9,10]. Another problem is associated with the complexity of controlling the firing angles of the thyristors when a non-resistive load is used. Furthermore, the relatively large number of thyristors needed in the tap changer have so far tended to discourage the wide use of thyristor assisted tap changers.

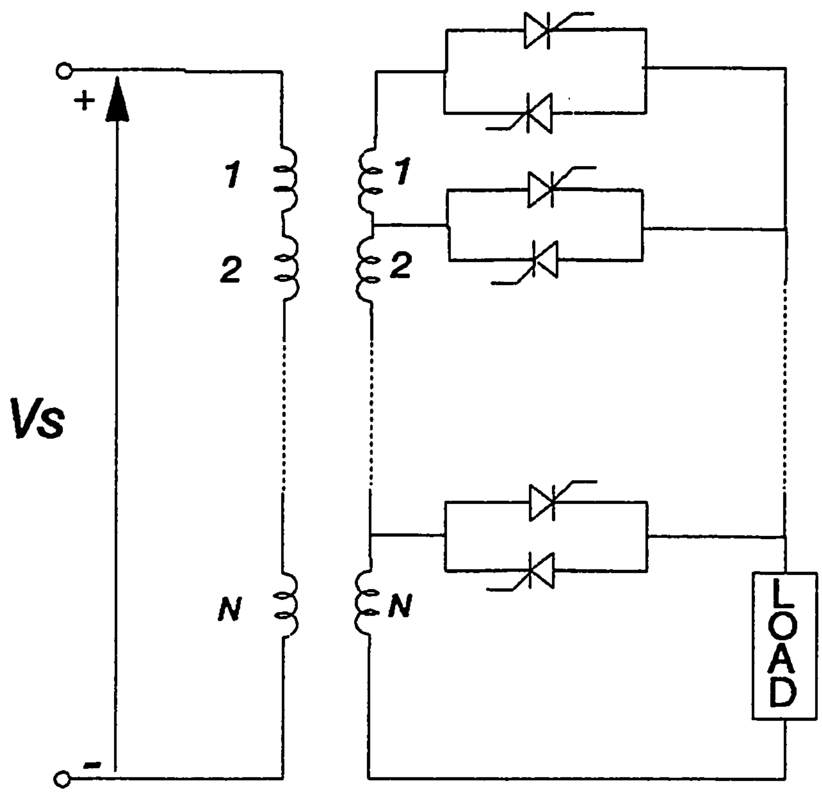


Fig. 1-2 Thyristor Assisted Tap Changer.

1.4 PROBLEM STATEMENT

Voltage stability and continuity of power flow are essential to all consumers of electricity. Unfortunately, the transfer of power from generators to loads might cause the voltage level to drop to an undesirable limit. Therefore, it is vital to control voltages at load nodes. Tap changers act to recover the normal operating voltages and maintain them within a predetermined range. However, the existing tap changers have several problems that might cause them to function improperly. Because of that, there is a pressing need to ensure the smooth operation of voltage controllers by eliminating their problems to guarantee continuity of the power flow. This thesis propose a new microcontroller-based voltage regulator that maintains the output voltage within a predetermined range regardless of the nature and size of the load.

1.5 PROPOSED REGULATOR

The proposed regulator is a new ac voltage regulator based on an 8-bit microcontroller. The proposed regulator automatically monitors, adjusts, and maintains the load voltage within a predetermined range. It consists basically of two units:

1) The Acquisition Unit

   It is responsible for detecting any variation in the load voltage.

2) The Regulating Unit

   It is responsible for taking a corrective action to maintain the load voltage within the predetermined range.

CHAPTER II

LITERATURE REVIEW

2.1 INTRODUCTION

The principles of ac voltage regulation have been known and employed for many years [6,7]. In a power system there might be several circuits serving sensitive loads where voltage reduction would not be acceptable. For these types of loads continuous voltage regulation is indispensable. Because of that, several methods were proposed to eliminate the voltage drop problem. One of the methods used is the electromechanical tap-changing system [8]. This method proved to be successful in regulating the supply voltage against fluctuations. However, the frequent changes of the taps, to maintain a certain degree of regulation, will lead to electrical and mechanical wear [9]. Further enhancements on this type of regulation technique by utilizing thyristors as switching devices were reported [11,12,13,14]. Although the utilization of thyristors eliminated the electrical and mechanical wear, output voltage distortion remains high (>5%). The high distortion means that an ac voltage regulator based on the above methods is unsuitable for sensitive circuits.

Tez proposed a microprocessor-based controller for electromechanical tap-changing transformers [9]. In his design he tried to minimize the electrical and mechanical wear by avoiding the unnecessary and frequent changes of taps while a certain degree of voltage regulation is performed. Servetas and Vlachakis proposed another voltage regulator which employs TRIAC's as switching elements [15]. Their regulator maintains low distortion of harmonics. It also provides good voltage regulation. Servetas and Vlachakis regulator along with Tez regulator are discussed in greater details in the following two sections.

2.2 TEZ PROPOSED CONTROLLER

As mentioned earlier, Tez made use of the basic elements of an automatic tap-changing, shown in Fig. 2-1, to design his controller [9]. He replaced the analog circuitry of the tap-change controller with a digital one by using an 8085 microprocessor.

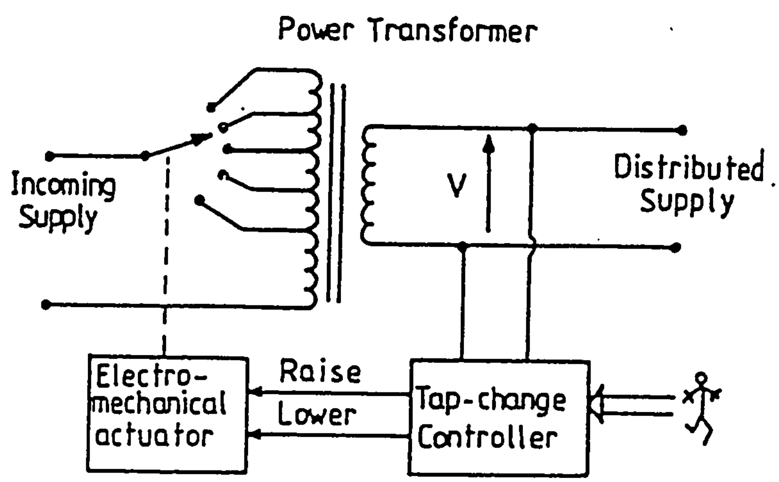


Fig. 2-1 Voltage Regulation by Tap-Changing.

2.2.1 PRINCIPLES OF OPERATION AND SYSTEM INTERFACING

Since the maintenance cost of electromechanical taps is quite high, Tez tried to avoid the unnecessary and too frequent changes of taps. This is achieved by structuring the control strategy to be based on the integral of an error voltage over a period of time rather than its instantaneous value. By doing so, the tap-change controller will not be affected by short term transient or voltage spikes eliminating unnecessarily frequent tap-changing actions. Fig. 2-2 shows a block diagram of the microprocessor-based controller [9].

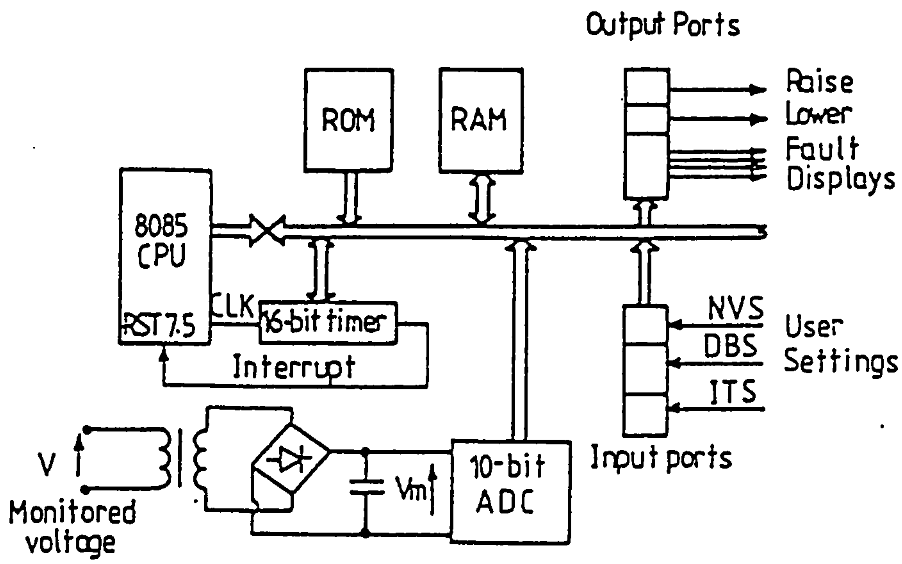


Fig. 2-2 Block Diagram of Tez Microprocessor-Based Controller.

In order for the system to work properly the following inputs should be entered within the given limits:

1) Normal Voltage Setting (NVS)

   The voltage range should be between 80 to 120V with 1V increments.

2) Dead-Band Setting (DBS)

   The dead-band settings defines the acceptable margin of error from the NVS. The allowable settings range from ±0.5% of NVS to ±2.25% of NVS in steps of 0.25%.

3) Integrating Time Setting (ITS)

   The value of ITS defines the minimum time needed before the controller takes any action, if the output voltage lies outside the dead-band of the normal voltage settings.

2.2.2 DRAWBACKS OF THE CONTROLLER

Despite the automatic nature and reprogrammability provided by the controller, the controller has two major disadvantages. The first disadvantage is that electrical and mechanical wear is unavoidable because a totally electronic tap-changing system was not adopted in the design. Therefore, the controller will be in need of costly regular maintenance. The second disadvantage is that the voltage regulation in the system is achieved in a discrete manner which makes the system unsuitable for regulating small voltages. moreover, the controller does not provide on-line correction, because it waits for a period of time (ITS) before taking any corrective action. In addition, the mechanical nature of the electro-mechanical tap changer increases the response time of the system significantly.

2.3 SERVETAS AND VLACHAKIS PROPOSED CONTROLLER

Servetas and Vlachakis adopted a controller that employs TRIAC's as switching elements in the secondary of a power autotransformer, shown in Fig. 2-3 [15].

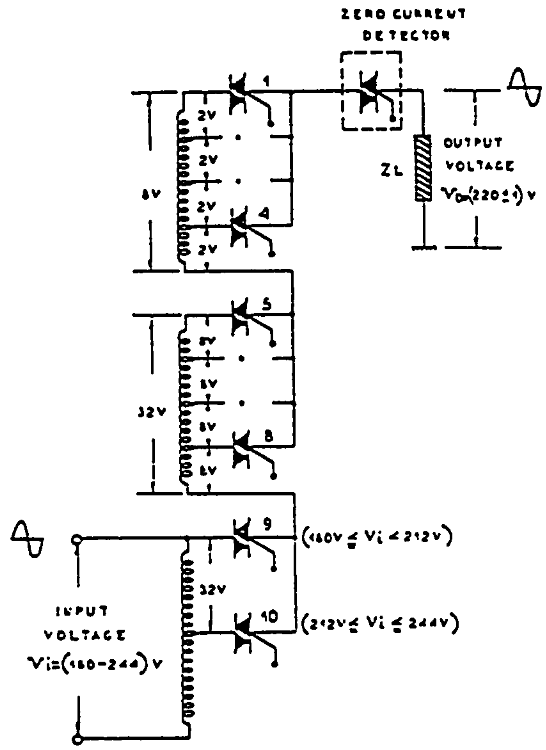


Fig. 2-3 Power Unit Design.

2.3.1 PRINCIPLES OF OPERATION FOR THE CONTROLLER

The block diagram shown in Fig. 2-4 presents the basic structure of Servetas and Vlachakis regulator [15]. The regulator consists basically of the following three sections:

1) Discriminator

   The function of the discriminator is to identifies the root cause of the output-voltage deviation. This cause may be due to the input-voltage variation or the load-current variation or both. After identifying the root cause of the fluctuations, the controlled variable of the regulating system will also be determined in the discriminator section.

2) Central Control Unit

   The primary function of the central control unit is to determine which of the TRIAC's of the power unit should be operated depending on the output-voltage deviation at each instant of time.

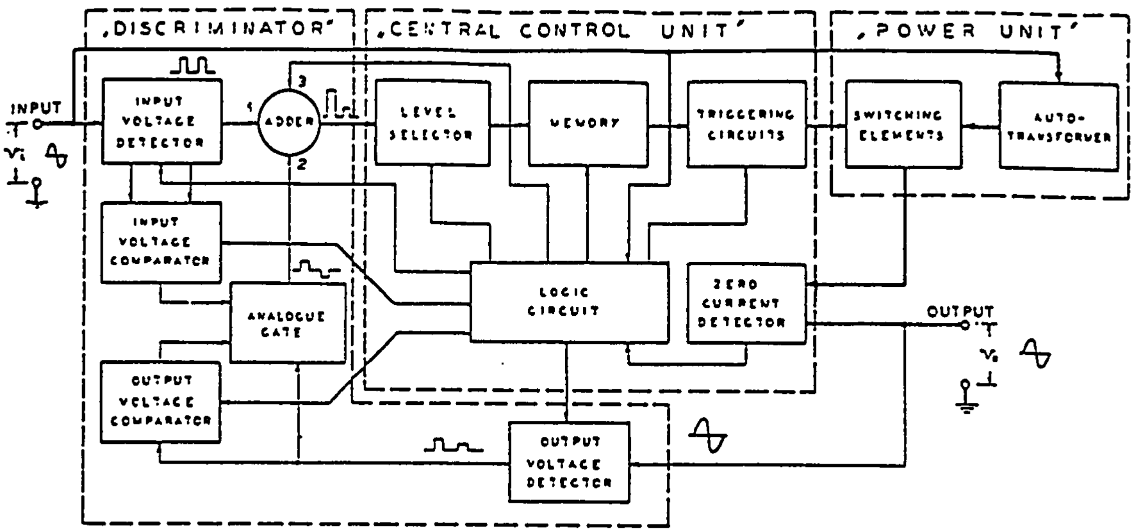


Fig. 2-4 Block Diagram of Servetas & Vlachakis Regulator.

3) <u>Power Unit</u>

The power unit section includes the power auto transformer and the switching elements (TRIAC's). The number of TRIAC's needed depends upon the desired output voltage.

2.3.2 DRAWBACKS OF THE CONTROLLER

Servetas and Vlachakis controller offers good voltage regulation and short time correction. However, one major disadvantage of this controller is the complexity of the power unit. This is because, the number of the TRIAC's needed depends upon the desired voltage. Furthermore, the controller consists of a large number of components which will increase its cost and complexity. Moreover, the regulator is not programmable. In addition, the regulation scheme used by the regulator to adjust the voltage is quite involved because of the interaction of the different components used.

CHAPTER III

AC VOLTAGE REGULATORS ANALYSIS AND SIMULATION

3.1 INTRODUCTION

Controllers and ac switches conduct electrical current in both directions. However, since semiconductor valves only conduct current in one direction, namely the forward direction, two valves always are needed and are connected back-to-back. Fig. 3-1 shows a diagram of a thyristor ac switch circuit. Thyristors (SCR's) proved to be suitable for use as ac switches on account of their extremely high switching capacity and precise set turn-on points [4,5]. Because of that, thyristor switches are being used instead of mechanical switches in alternating current and three-phase circuits [4,5].

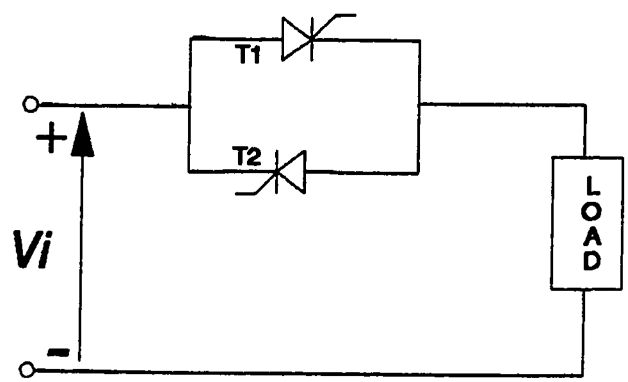


Fig. 3-1 Thyristor AC Switch Circuit.

As a consequence to the growing interest in the thyristors, there has been a pressing need for accurate and simple means to analyze thyristor circuits. Therefore, when the Spice computer program was introduced in the mid-1970s [16], there has been an urgent need for a thyristor (SCR) model that could be used with the program. Recently, several SCR models, based on the two-transistor model for the SCR, have been proposed [17,18,19,20]. While these models accurately reflect the switching dynamics and other parameters of the SCR, they are not functional for simulation purposes without determination of more than 50 model parameters. In addition, they involve a large number of components adding a significant complexity to the SPICE analysis.

In order for the SCR model to be of practical use, it should be as simple as possible to simplify the analysis of thyristor circuits. In 1989 Giacoletto used ideal voltage-controlled and current-controlled switches to propose a model for the SCR [21], shown in Fig. 3-2.

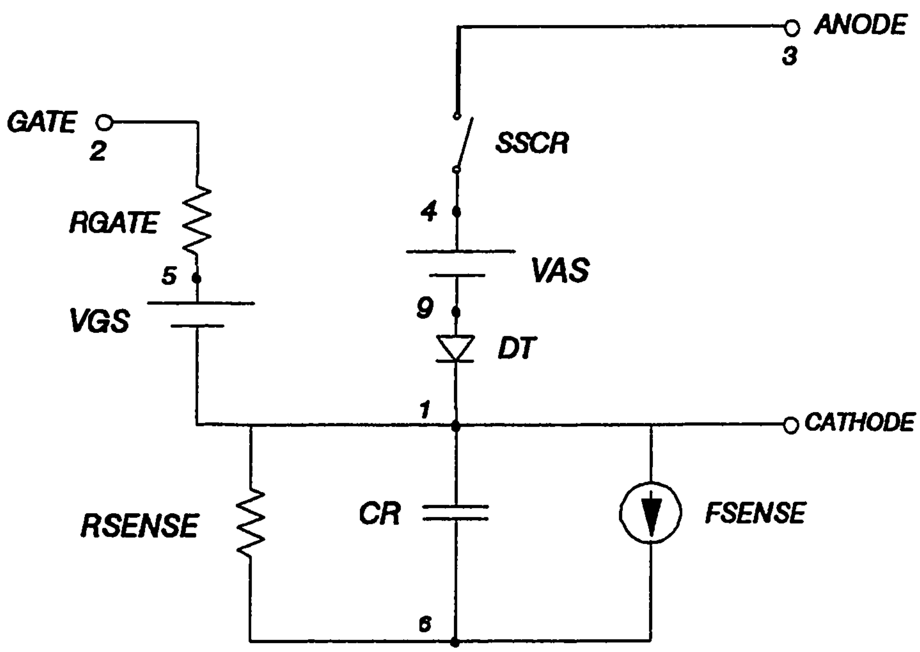


Fig. 3-2 Thyristor Model Circuit.

The PSPICE subcircuit description of the thyristor model is provided below:

```
.SUBCKT  SCR  3  2  1
RGATE    2    5  750
VGS      5    1  0
SSCR     3    4  6  1  SSCR
CSWITCH  3    4  450PF
VAS      4    9  0
DT       9    1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125   ROFF=103000
VON=1 VOFF=0)
.MODEL   DIODE   D
FSENSE   1    6  POLY(2)  VGS  VAS  0  50  11
RSENSE   6    1  1
CR       6    1  0.1UF
.ENDS
```

The model is simple and uses a reasonable number of components which simplifies the analysis of SCR circuits. The model has been found to be computationally efficient and quite adequate for the present study.

3.2 ANALYSIS OF A SINGLE-PHASE AC VOLTAGE REGULATOR

Fig. 3-3(a) shows a single phase ac voltage regulator. It consists of two thyristors connected in an antiparallel fashion. By varying the delay angle of thyristor T1 during the positive half-cycle and the delay angle of thyristor T2 during the negative half-cycle, the power flow is controlled. Fig. 3-3(b) shows the waveforms that illustrate the operation of the circuit [5].

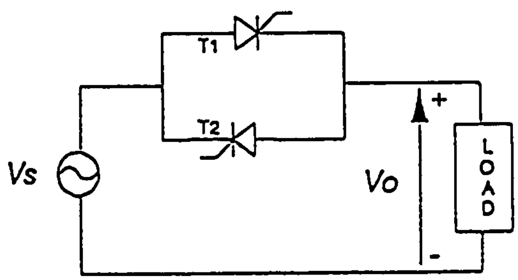
The RMS output voltage can be calculated from the following equation:

$$V_o = \left[(2/2\pi) \int_{\alpha}^{\pi} v^2{}_s \, d(wt) \right]^{\frac{1}{2}} \qquad (3\text{-}1)$$

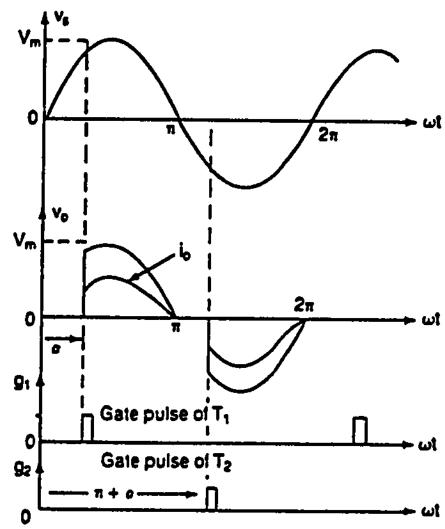
If $v_s = \sqrt{2}\, V_s \sin wt$ then,

$$V_o = V_s \left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2) \right]^{\frac{1}{2}} \qquad (3\text{-}2)$$

the range of delay angle is $0 \le \alpha \le \pi$.



(a) Circuit



(b) Waveforms

Fig. 3-3 Single Phase AC Voltage Regulator.

There are two common loads for such circuits. One is the resistive load and the other is the inductive load. The output waveforms and the position of the firing angle are based on the type of the load the voltage is regulated across. In the next two subsections, both loads will be simulated for the single-phase ac voltage regulator.

3.2.1 ANALYSIS AND SIMULATION OF A SINGLE PHASE AC VOLTAGE REGULATOR WITH RESISTIVE LOAD

Fig. 3-4 shows a circuit diagram of a single-phase regulator with resistive load for PSPICE simulation. By varying the firing angle α from 0 to π, V_O can be varied from VAN to 0. In the simulation The firing angle α was arbitrarily chosen to be equal to 21.61°.
Fig. 3-5 shows the resulted waveforms from simulation.

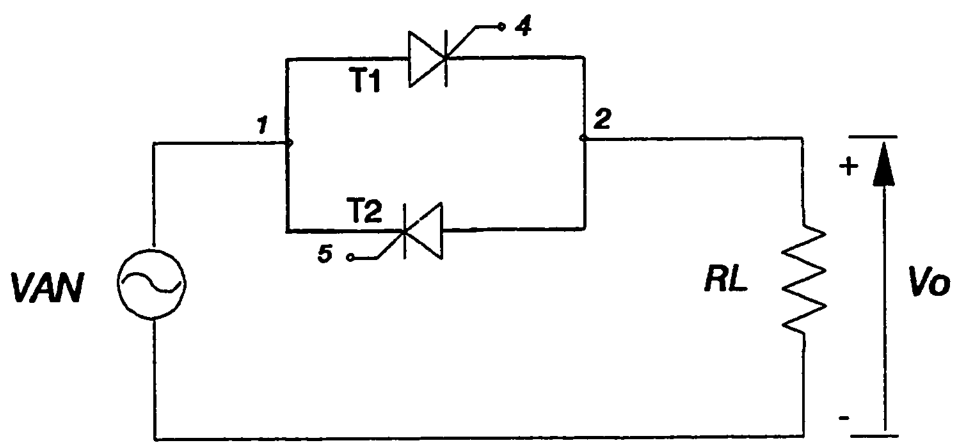


Fig. 3-4 AC Voltage Regulator Circuit with

Resistive Load for PSPICE Simulation.

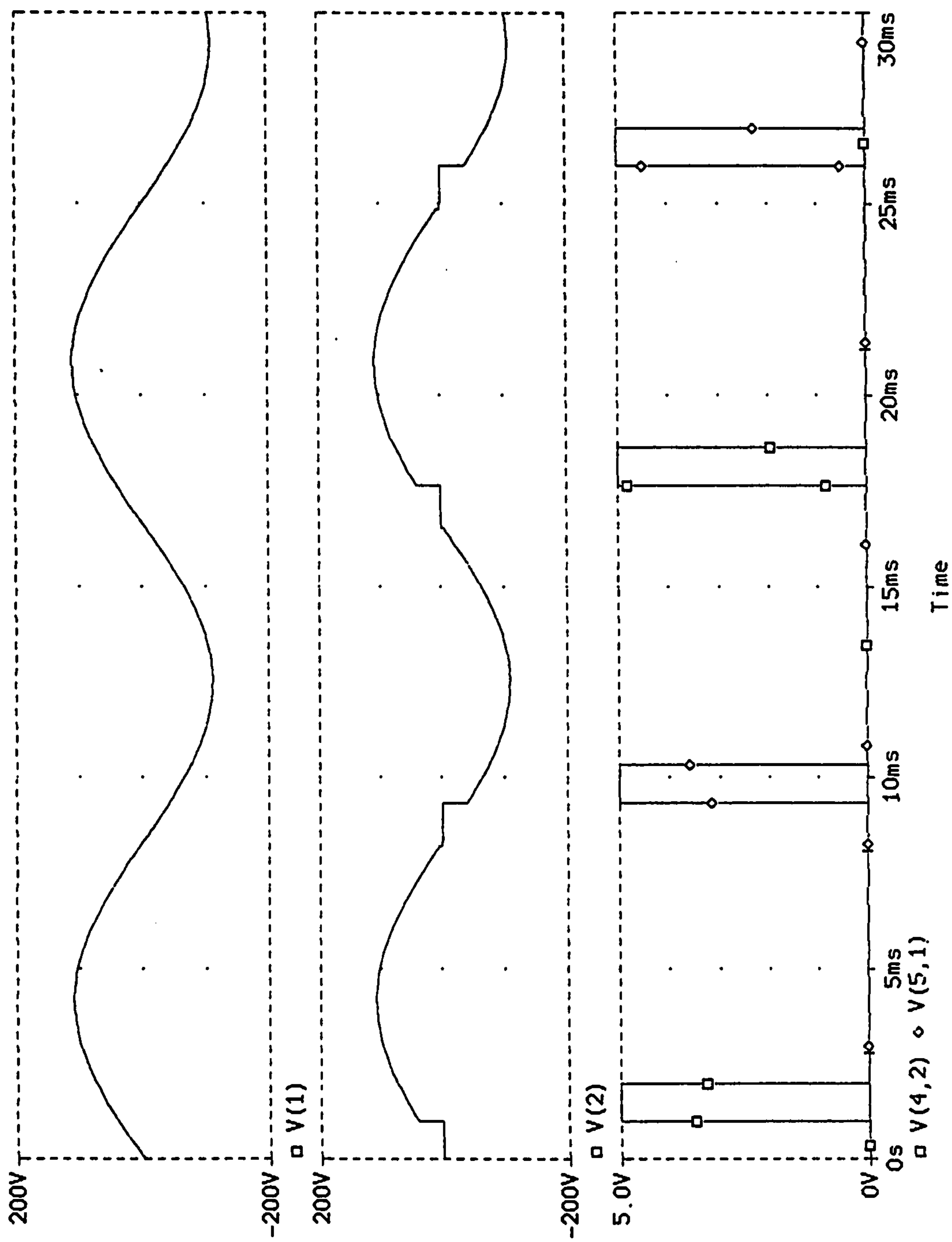
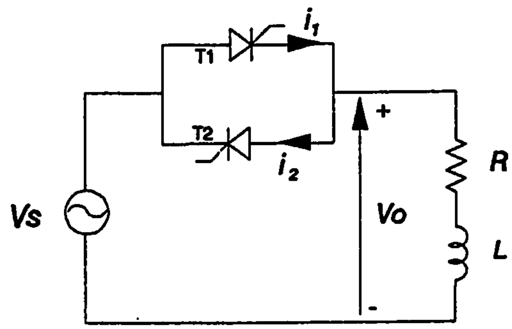


Fig. 3-5 Simulated AC Voltage Regulator Waveforms

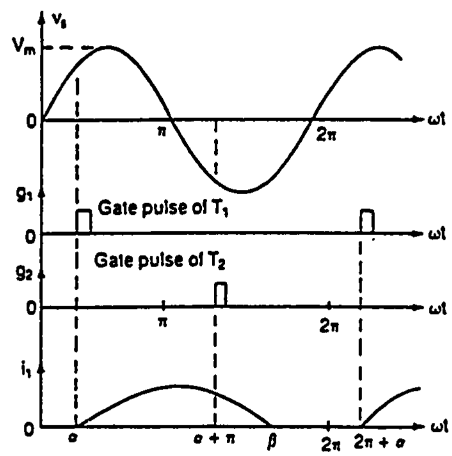
(Resistive Load).

3.2.2 ANALYSIS AND SIMULATION OF A SINGLE PHASE AC VOLTAGE REGULATOR WITH INDUCTIVE LOAD

In reality, most loads are inductive to a certain degree. A full-wave ac voltage regulator with inductive load is shown in Fig. 3-6(a). Due to the presence of the inductive load, the output current lags the voltage by the load phase angle $\phi = \tan^{-1}(wL/R)$. Therefore, the load current would not become zero at $wt = \pi$, but continues to flow until β which is called extinction angle [3,5]. Consequently, only T1 will operate, causing asymmetrical waveforms of output voltage and current, as shown in Fig. 3-6(b) [5]. This obstacle can be overcome by either using a continuous gate pulse with duration $(\pi-\alpha)$ as shown in Fig. 3-6(c), or by using a train of pulses with short durations as shown in Fig. 3-6(d) [2,3,4,5].



(a) Circuit



(b) Waveforms

(c)

(d)

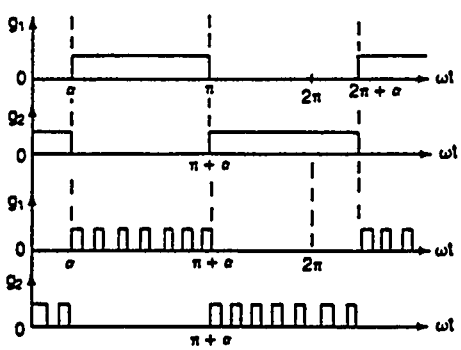


Fig. 3-6 AC Voltage Regulator with Inductive Load.

Fig. 3-6(a) is redrawn in Fig. 3-7 for the purpose of simulation. Note that a free wheeling diode is connected in parallel with the inductive load to provide a path for the inductor current during the discharge process. As a result, the continuous load current profile displays considerably less ripple. The firing angle α was also set to be equal to 21.61° during the simulation of the circuit. The simulated waveforms of the circuit are shown in Fig. 3-8.

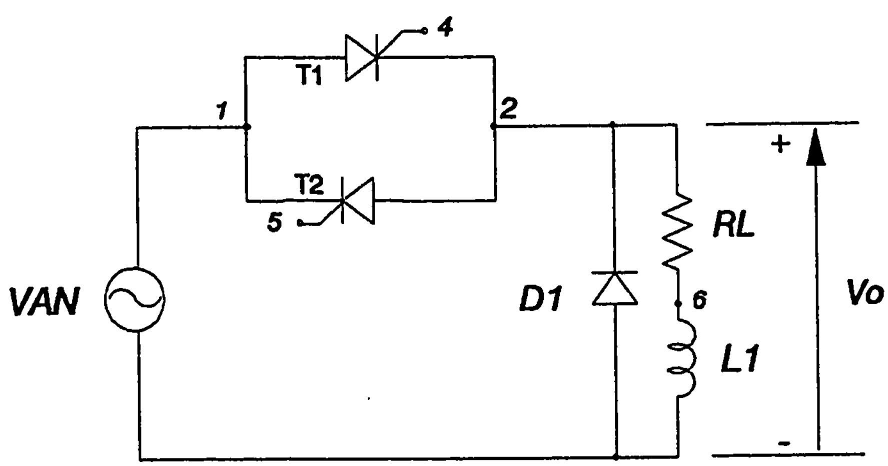


Fig. 3-7 AC Voltage Regulator Circuit with Inductive Load for PSPICE Simulation.

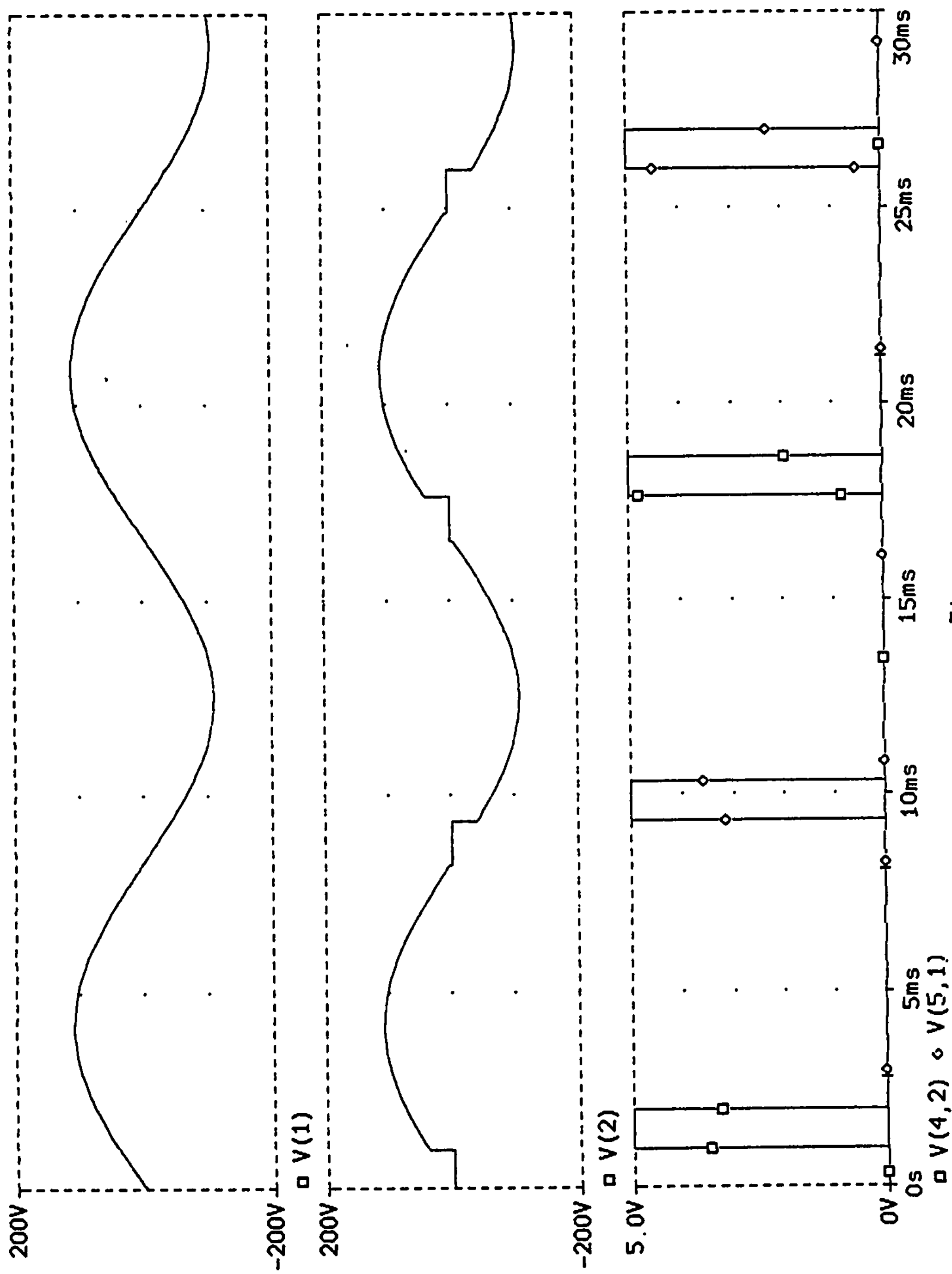


Fig. 3-8 Simulated AC Voltage Regulator Waveforms (Inductive Load).

3.3 ANALYSIS OF A TAP CHANGER TRANSFORMER

For fast switching actions of tap changers, thyristors can be used as ac static switches. Fig. 3-9 shows a circuit diagram of a single-phase tap changer transformer. With this kind of circuit, the load voltage V_o can be varied within three possible ranges. The three ranges are:

1) $0 < V_o < V_1$
2) $0 < V_o < (V_1 + V_2)$
3) $V_1 < V_o < (V_1 + V_2)$

Suppose that v_1 and v_2 are set as follows:

$$v_1 = \sqrt{2}\ V_1 \sin wt$$

$$v_2 = \sqrt{2}\ V_2 \sin wt$$

then, the RMS output voltage for the three ranges can be calculated as follows:

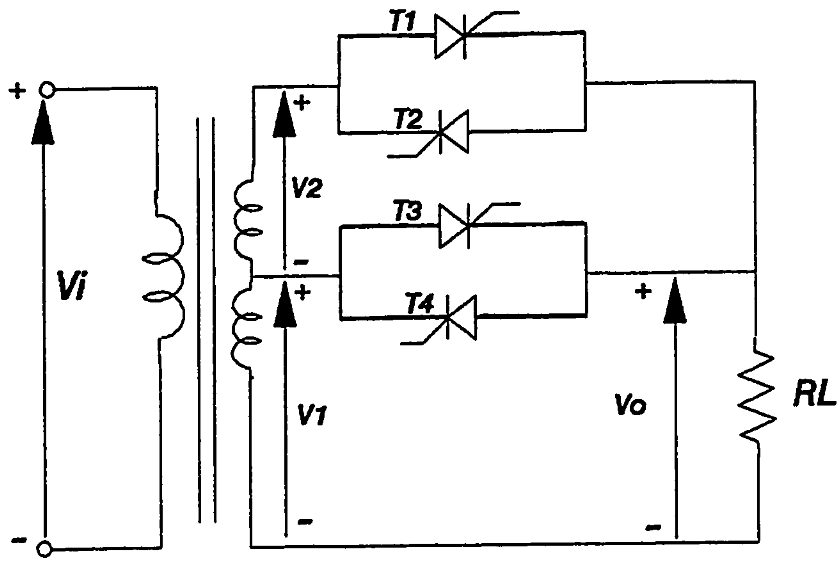


Fig. 3-9 Tap Changer Transformer.

First **Control** **Range:** $0 \le V_o \le V_1$

$$V_o = V_1 \left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2) \right]^{\frac{1}{2}} \qquad (3-3)$$

Fig. 3-10(c) presents the instantaneous load voltage and current for this range [5].

Second **Control** **Range:** $0 \le V_o \le (V_1 + V_2)$

$$V_o = (V_1+V_2) \left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2) \right]^{\frac{1}{2}} \qquad (3-4)$$

Fig. 3-10(d) shows the instantaneous load voltage and current for this range [5].

Third **Control** **Range:** $V_1 \le V_o \le (V_1 + V_2)$

$$V_o = \left[(V^2{}_1/\pi)(\alpha - (\sin 2\alpha)/2) + [(V_1+V_2)^2/\pi][\pi - \alpha + (\sin 2\alpha)/2] \right]^{\frac{1}{2}} \qquad (3-5)$$

Fig. 3-10(e) shows the instantaneous load voltage and current for this range [5].

Note that the range of delay angle is $0 \le \alpha \le \pi$ for the above three equations.

In the subsequent two subsections the tap changer will be simulated for resistive and inductive loads.

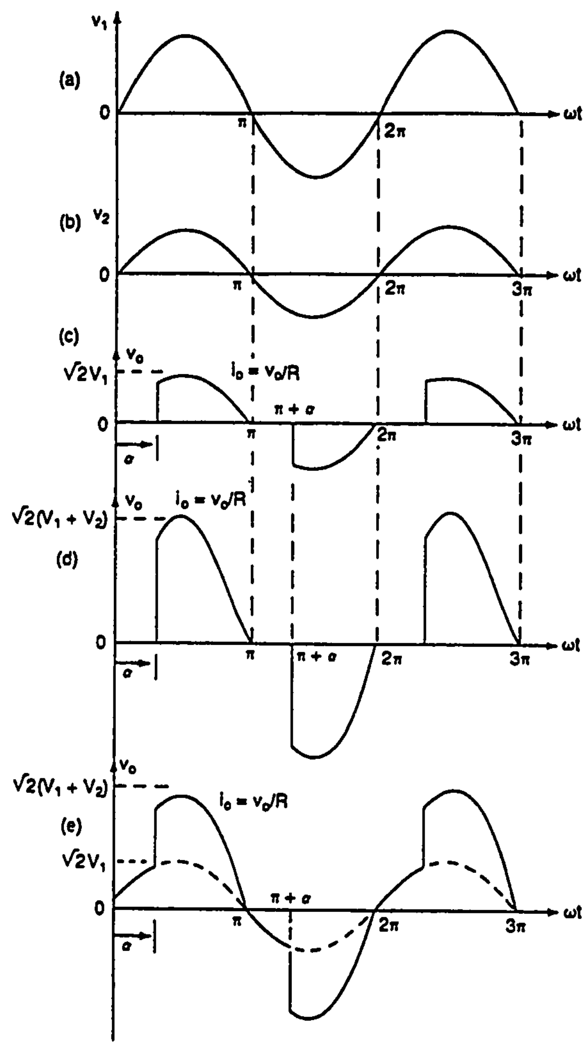


Fig. 3-10 Waveforms for Transformer Tap Changer.

3.3.1 ANALYSIS AND SIMULATION OF A TAP CHANGER TRANSFORMER WITH RESISTIVE LOAD

The operation of a tap changer is simple for a purely resistive load. On the positive half cycle, thyristor T3 is gated on at the zero crossing of the voltage ($wt=0$). The voltage appearing across the load is V1. Thyristor T1 may be gated on at any later time in the positive half cycle. If T1 is turned on (e.g. at $wt=\alpha$), T3 is reverse biased due to secondary voltage V2, and T3 is turned off. The voltage appearing across the load is (V1+V2). T1 is self-commutated at $wt=\pi$ and T4 is turned on. The voltage across the load at that time will be equal to V1. Thyristor T2 may be gated at any later time in the negative half cycle. If T2 is fired (e.g. at $wt=\pi+\alpha$), T4 is turned off due to the reverse voltage V2 and the load voltage is (V1+V2). At $wt=2\pi$, T2 is self-commutated, T3 is fired again and the cycle is repeated. Fig 3-11 shows a circuit diagram of a single phase tap changer with resistive load for PSPICE simulation. The simulated waveforms of the circuit are shown in Fig. 3-12. The firing angle α was set to be equal to 60° during the simulation of the circuit.

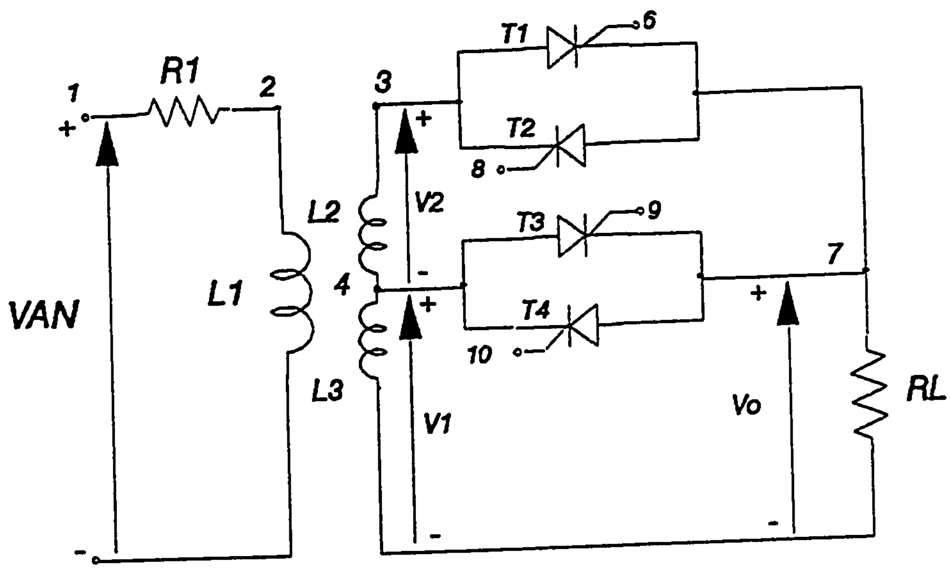


Fig. 3-11 Tap Changer Circuit with Resistive Load for PSPICE Simulation.

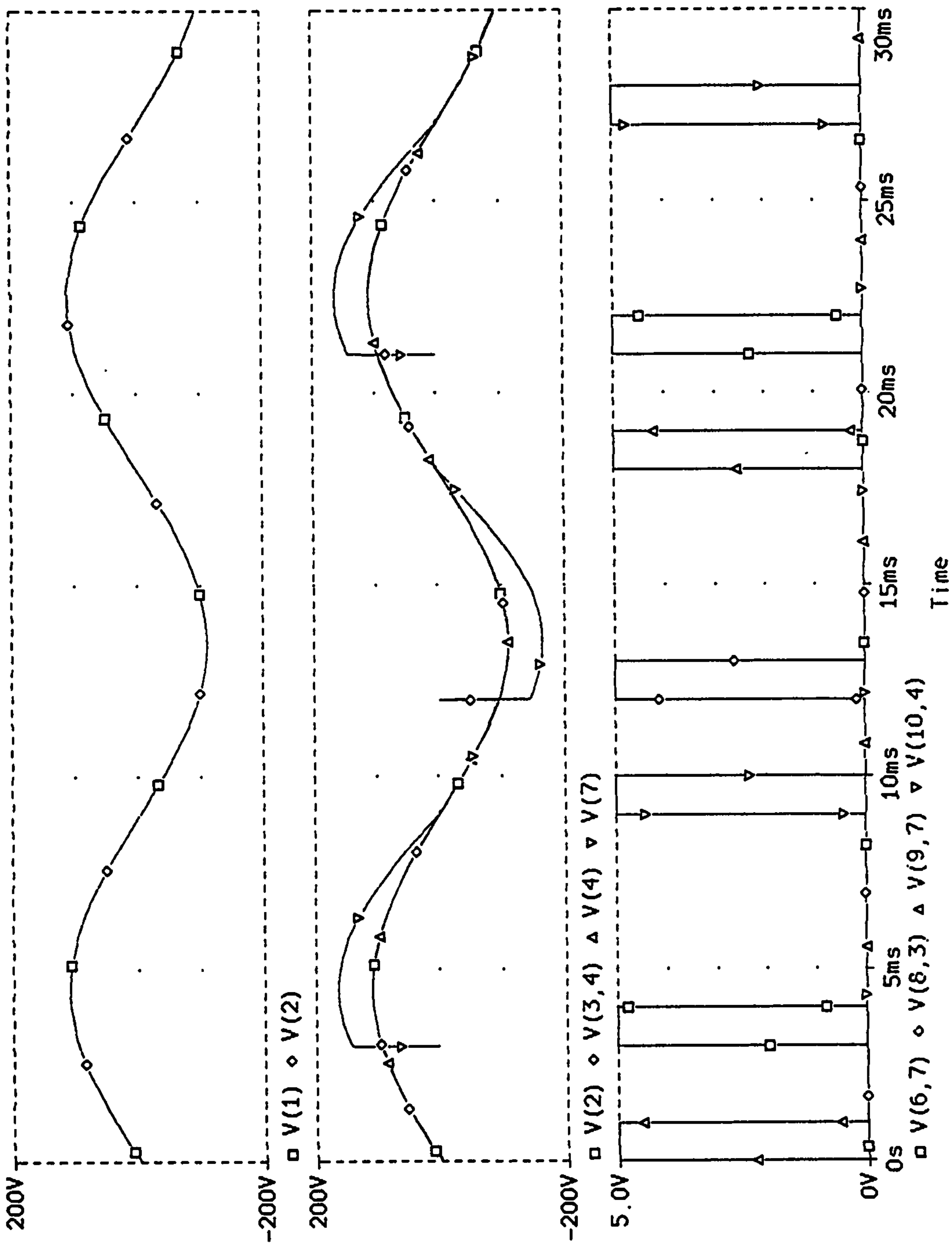


Fig. 3-12 Simulated Tap Changer Waveforms

(Resistive Load).

3.3.2 ANALYSIS AND SIMULATION OF A TAP CHANGER TRANSFORMER WITH INDUCTIVE LOAD

If the load is inductive, T3 cannot turn on at the zero crossing and current will continue to flow in either T2 or T4 depending on which one had control at the end of the previous half cycle. Fig. 3-13 shows the output voltage and current waveforms of an inductive load [2]. Note also if T4 is carrying current at the beginning of the positive half cycle, then gating T1 on while T4 is still conducting will short out V2. Therefore, the control circuit must be designed carefully so that T1 is not turned on until T4 is off and the load current $I_o \geq 0$. Similarly, T2 should not be fired on until T3 is off and the load current $I_o \leq 0$ [3,5].

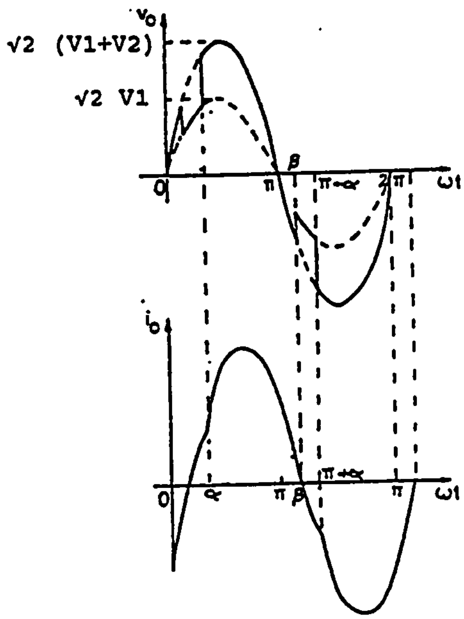


Fig. 3-13 Waveforms of a Transformer tap changer with Inductive Load.

Fig. 3-14 shows a circuit diagram of a single phase tap changer with inductive load for PSPICE simulation. The simulated waveforms of the circuit are shown in Fig. 3-15. The firing angle α was set to be equal to 80° during the simulation of the circuit.

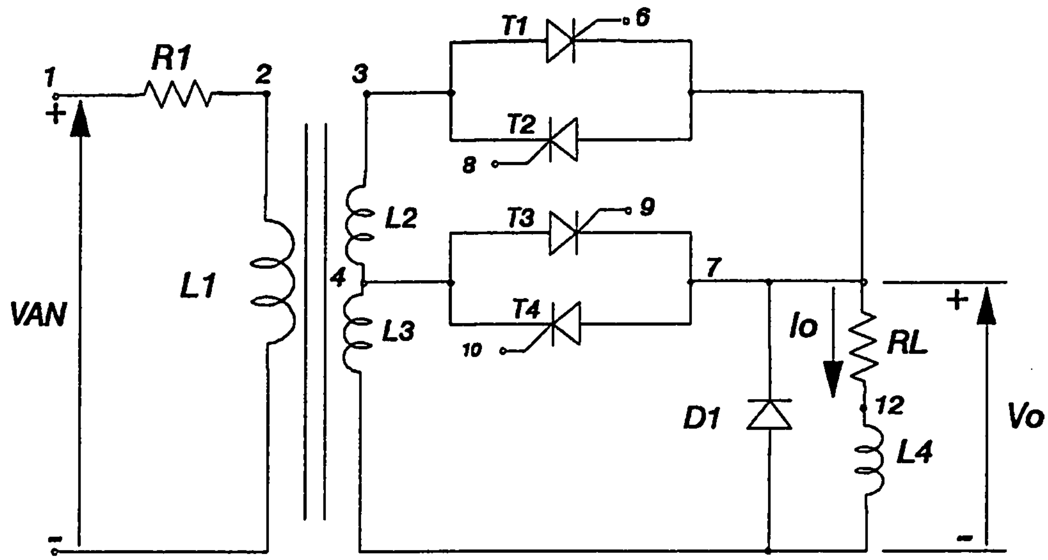


Fig. 3-14 Tap Changer Circuit with Inductive Load for PSPICE Simulation.

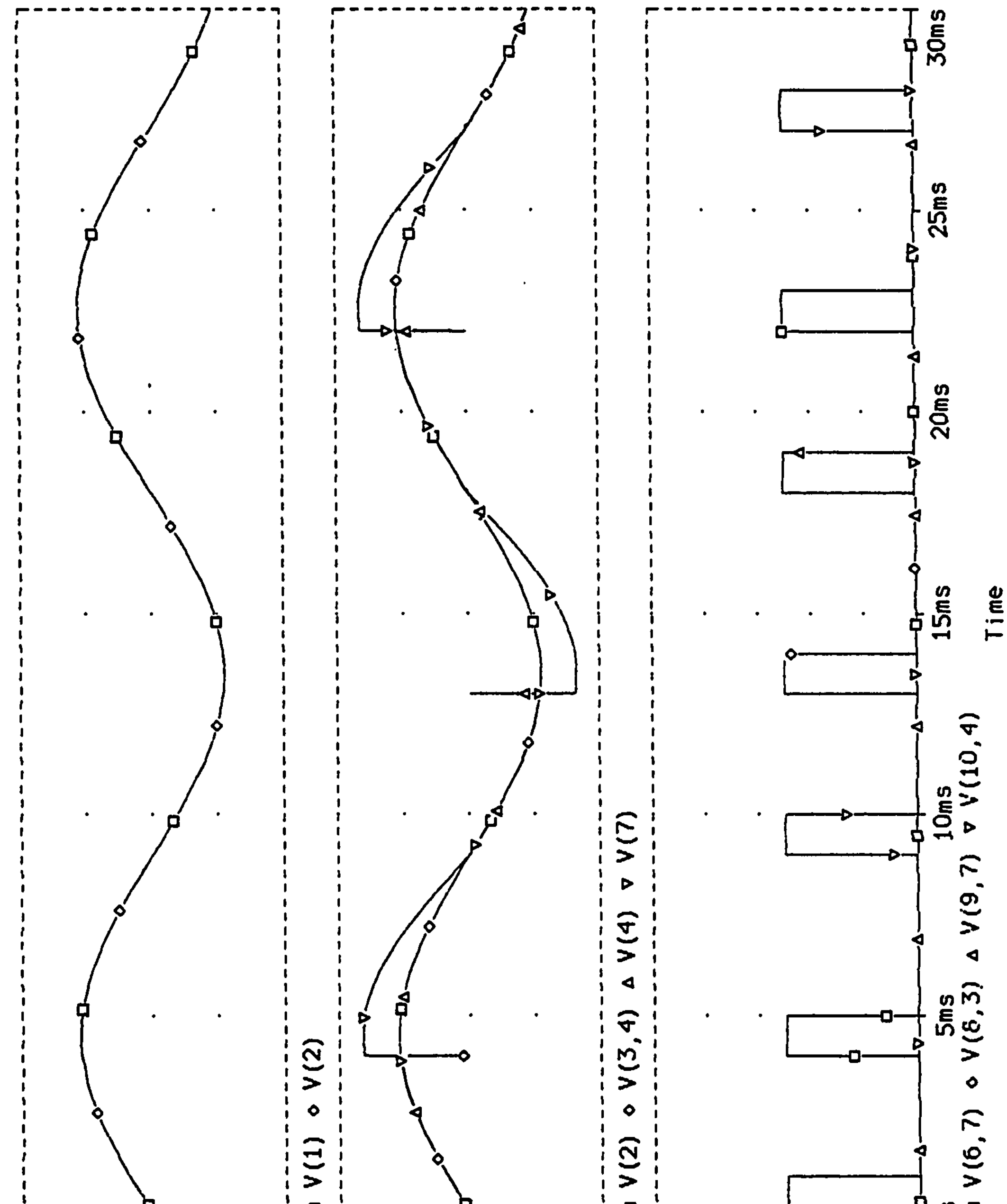


Fig. 3-15 Simulated Tap Changer Waveforms

(Inductive Load).

3.4 ANALYSIS OF A TAP CHANGER TRANSFORMER WITH THREE SECONDARY WINDINGS

If the number of thyristors is increased, a higher and a finer voltage control will be achieved. Fig. 3-16 shows a circuit diagram of a tap changer with three secondary windings. With this kind of circuit, the load voltage V_o can be varied within the following six possible ranges:

1) $0 < V_o < V_1$
2) $0 < V_o < (V_1 + V_2)$
3) $0 < V_o < (V_1 + V_2 + V_3)$
4) $V_1 < V_o < (V_1 + V_2)$
5) $V_1 < V_o < (V_1 + V_2 + V_3)$
6) $(V_1 + V_2) < V_o < (V_1 + V_2 + V_3)$

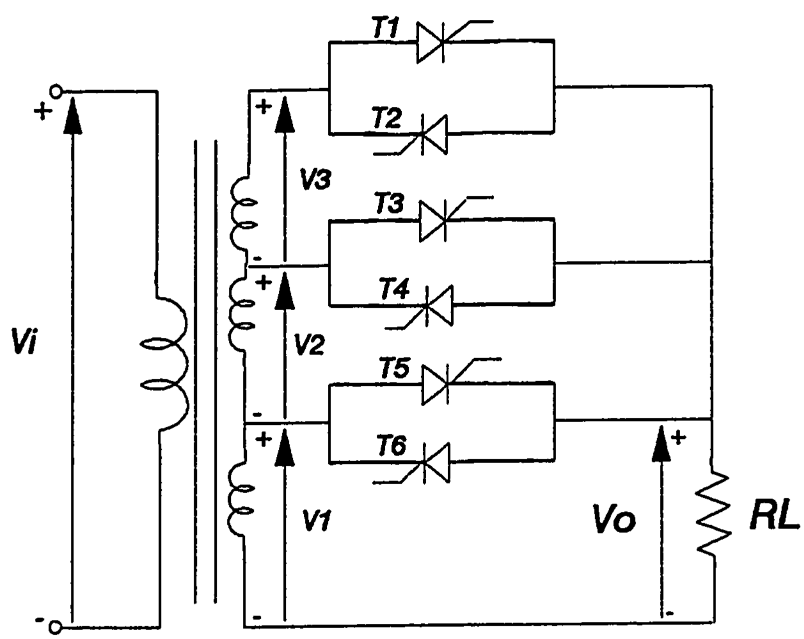


Fig. 3-16 Tap Changer Circuit with Three Secondary Windings.

The RMS output voltage can be calculated from the following equation:

$$V_o = \left[(1/2\pi) \int_0^{2\pi} v^2{}_i \; d(wt) \right]^{1/2} \qquad (3\text{-}6)$$

Suppose that v_1, v_2 and v_3 are set as follows:

$v_1 = \sqrt{2}\ V_1 \sin wt$

$v_2 = \sqrt{2}\ V_2 \sin wt$

$v_3 = \sqrt{2}\ V_3 \sin wt$

then, the RMS output voltage for the six ranges can be calculated as follows:

First Control Range: $0 \le V_o \le V_1$

$$V_o = V_1 \left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2) \right]^{1/2} \qquad (3\text{-}7)$$

Fig. 3-17(d) presents the instantaneous load voltage for this range.

Second Control Range: $0 \le V_o \le (V_1 + V_2)$

$$V_o = (V_1 + V_2) \left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2) \right]^{1/2} \qquad (3\text{-}8)$$

Fig. 3-17(e) shows the instantaneous load voltage for this range.

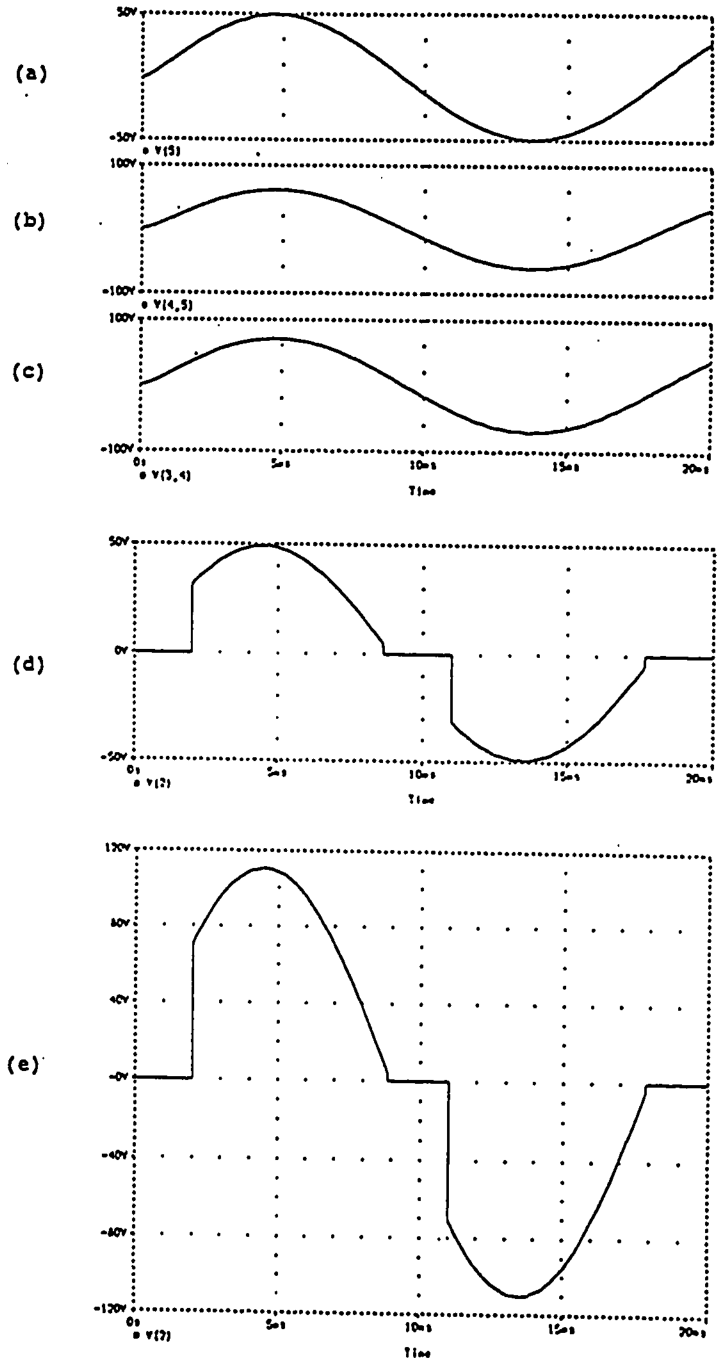


Fig. 3-17 Waveforms for Transformer Tap Changer with Three Secondary Windings.

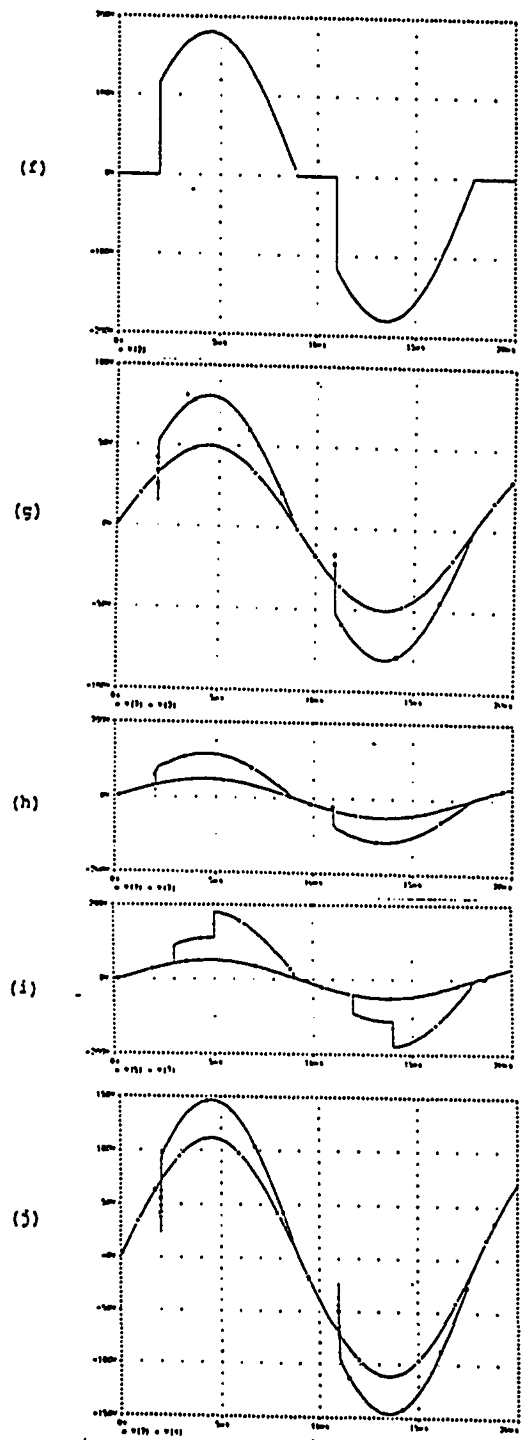


Fig. 3-17 Waveforms for Transformer Tap Changer with Three Secondary Windings (contd.).

Third Control Range: $0 \le V_o \le (V_1 + V_2 + V_3)$

$$V_o = (V_1+V_2+V_3)\left[(1/\pi)(\pi - \alpha + (\sin 2\alpha)/2)\right]^{\frac{1}{2}} \qquad (3\text{-}9)$$

Fig. 3-17(f) shows the instantaneous load voltage for this range.

Fourth Control Range: $V_1 \le V_o \le (V_1 + V_2)$

$$V_o = \left[(V^2{}_1/\pi)(\alpha - (\sin 2\alpha)/2) + [(V_1+V_2)^2/\pi][\pi - \alpha + (\sin 2\alpha)/2]\right]^{\frac{1}{2}} \qquad (3\text{-}10)$$

Fig. 3-17(g) shows the instantaneous load voltage for this range.

Fifth Control Range: $V_1 \le V_o \le (V_1 + V_2 + V_3)$

If Stages one and three are used to satisfy the above range, then the RMS output voltage can be calculated as follows:

$$V_o = \left[(V^2{}_1/\pi)(\alpha - (\sin 2\alpha)/2) + [(V_1+V_2+V_3)^2/\pi][\pi - \alpha + (\sin 2\alpha)/2]\right]^{\frac{1}{2}} \qquad (3\text{-}11)$$

However, if stages one, two and three are used to satisfy the range, then the RMS output voltage is calculated as follows:

$$V_o = \Big[(V^2{}_1/\pi)[\alpha 1 - (\sin 2\alpha 1)/2] + [(V_1+V_2)^2/\pi]\{(\alpha 2-\alpha 1) - (1/2)[\sin(2\alpha 2) - \sin(2\alpha 1)]\} + [(V_1+V_2+V_3)^2/\pi]\{\pi - \alpha 2 + (\sin 2\alpha 2)/2\} \Big]^{\frac{1}{2}} \quad (3\text{-}12)$$

Fig. 3-17(h) and Fig. 3-17(i) shows the instantaneous load voltages for this range. Note that the range of delay angle are

$0 \leq \alpha 1 \leq \pi$

and

$\alpha 1 \leq \alpha 2 \leq \pi$

for the previous equation.

Sixth Control Range: $(V_1 + V_2) \leq V_o \leq (V_1 + V_2 + V_3)$

$$V_o = \Big[[(V_1+V_2)^2/\pi][\alpha - (\sin 2\alpha)/2] + [(V_1+V_2+V_3)^2/\pi]\{\pi - \alpha + (\sin 2\alpha)/2]\} \Big]^{\frac{1}{2}} \quad (3\text{-}13)$$

Fig. 3-17(j) shows the instantaneous load voltage for this range.

Note that the range of delay angle is $0 \leq \alpha \leq \pi$ for all of the above equations. In the subsequent two subsections the three-secondary tap changer will be simulated for resistive and inductive loads.

3.4.1 ANALYSIS AND SIMULATION OF A TAP CHANGER TRANSFORMER WITH THREE SECONDARY WINDINGS (RESISTIVE LOAD)

The operation of the circuit is quite simple for a purely resistive load. On the positive half cycle, thyristor T5 is gated on at wt=0. The output voltage across the load at that time is V1. Thyristor T3 may be gated on at any later time in the positive half cycle (e.g. at $wt=\alpha_1$), T5 is reverse biased due to secondary voltage V2, and (V1+V2) is the output voltage appearing across the load at that moment. Now, if T1 is fired at $wt=\alpha_2$, T3 is reverse biased due to secondary voltage V3, and the load voltage is (V1+V2+V3) at that time. T1 is self-commutated at $wt=\pi$ and T6 is gated on. The voltage across the load at that time will be equal to V1. After that, T4 is fired at $wt=\pi+\alpha_1$, and the load voltage at that moment is (V1+V2). Then, T2 is turned on at $wt=\pi+\alpha_2$, and the load voltage at that instance is (V1+V2+V3). At $wt=2\pi$, T2 is self-commutated, and T5 is fired again and the cycle is repeated. Fig. 3-18 shows a circuit diagram of a three-secondary-winding tap changer with resistive load for PSPICE simulation.

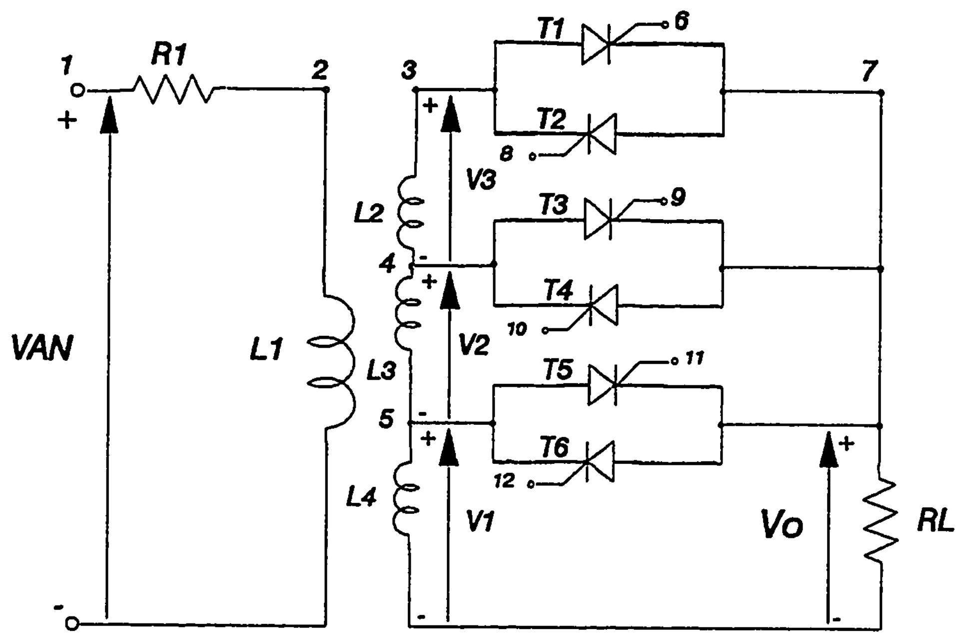


Fig. 3-18 Tap Changer Circuit with Three Secondary Windings with Resistive Load for PSPICE Simulation.

The simulated waveforms of the circuit are shown in Fig. 3-19. The firing angle $\alpha 1$ was set to be equal to 60° and $\alpha 2$ was set to be equal to 100° during the simulation of the circuit.

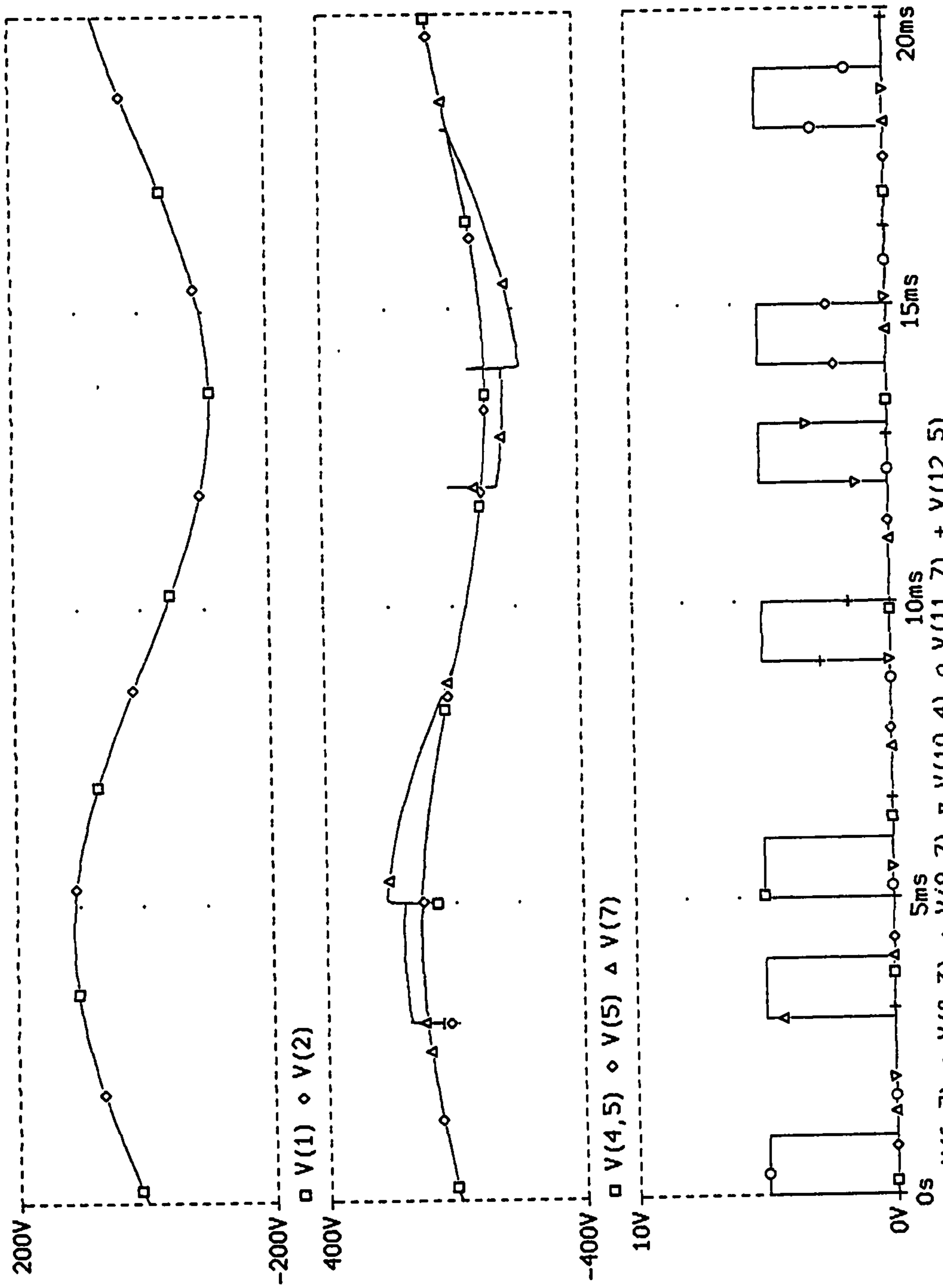


Fig. 3-19 Simulated Tap Changer with Three Secondary Windings Waveforms (Resistive Load).

3.4.2 ANALYSIS AND SIMULATION OF A TAP CHANGER TRANSFORMER WITH THREE SECONDARY WINDINGS (INDUCTIVE LOAD)

Fig. 3-20 shows a circuit diagram of a tap changer with three secondary windings. The load of the circuit is inductive. Care must be taken in designing the control circuit of the system to avoid shorting any of the secondary windings of the transformer. Therefore, T3 is not turned on until T6 is off and the load current $I_o \geq 0$, and T1 is not gated on until T4 is off and the load current $I_o \geq 0$. Similarly, T4 should not be turned on until T5 is off and the load current $I_o \leq 0$, and T2 should not be gated on until T3 is off and the load current $I_o \leq 0$. The simulated waveforms of the circuit are shown in Fig. 3-21. The firing angle $\alpha 1$ was set to be equal to 60° and $\alpha 2$ was set to be equal to 120° during the simulation of the circuit.

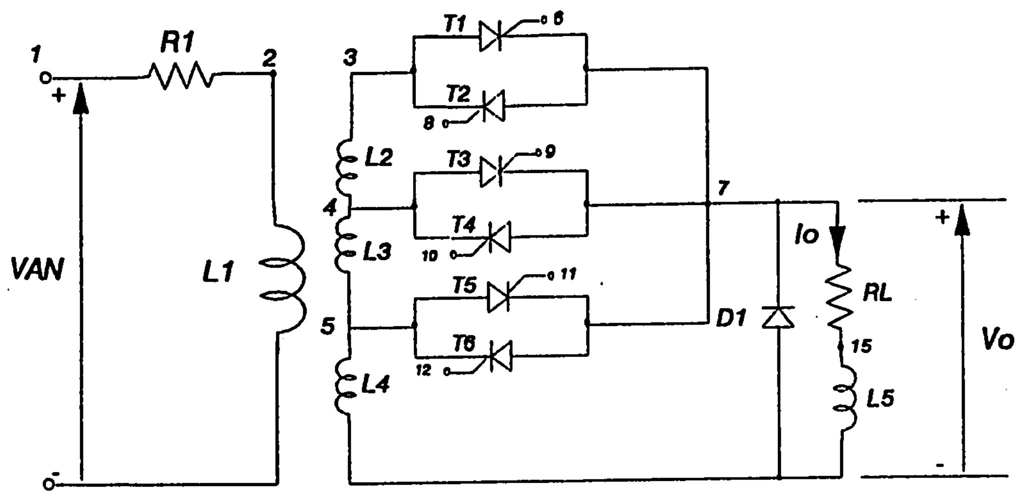


Fig. 3-20 Tap Changer Circuit with Three Secondary Windings with Inductive Load for PSPICE Simulation.

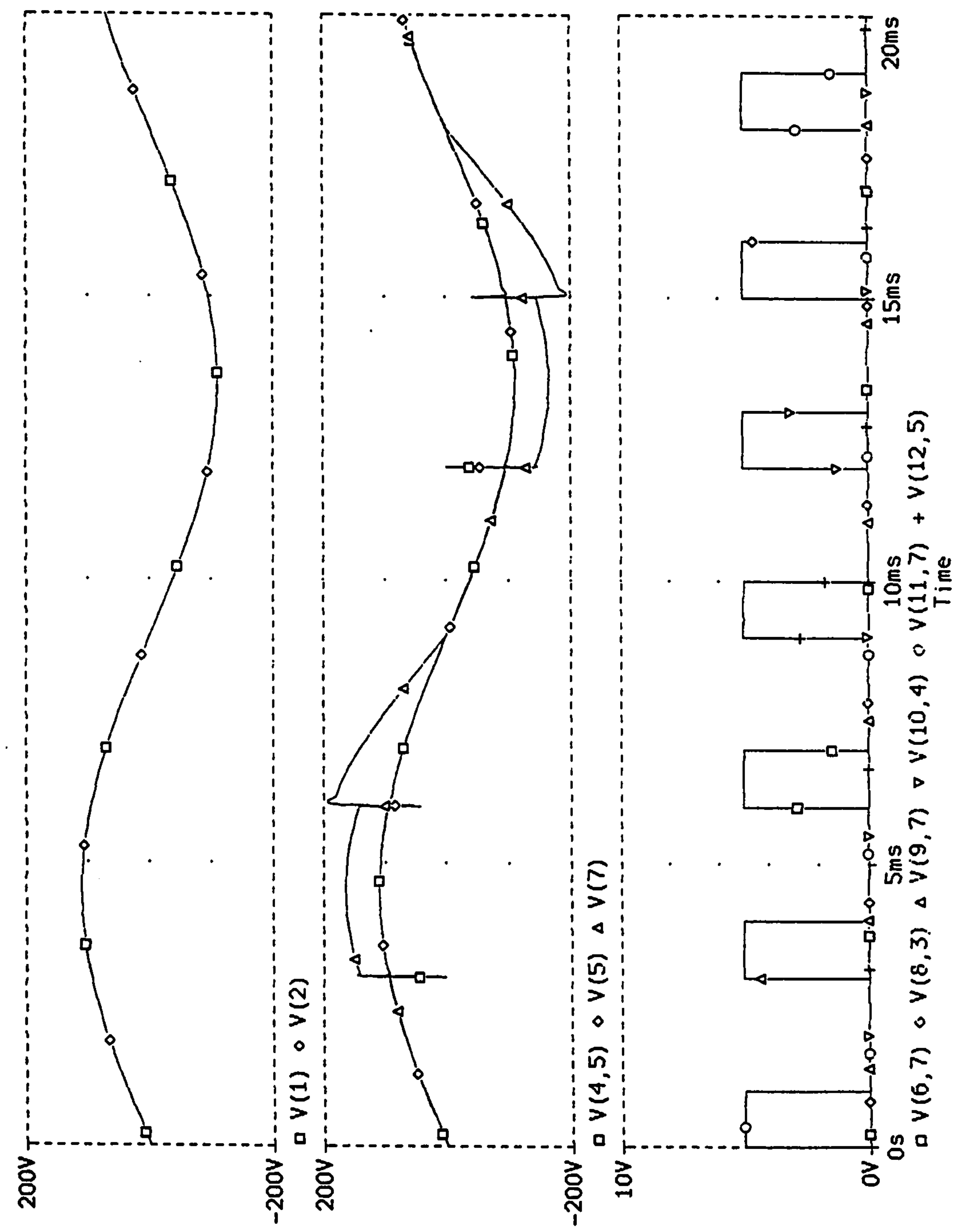


Fig. 3-21 Simulated Tap Changer with Three Secondary Windings Waveforms (Inductive Load).

3.5 DISCUSSION AND ANALYSIS OF THE SIMULATION RESULTS FOR THE SINGLE-PHASE AC VOLTAGE REGULATORS

In the previous sections, a single-phase ac voltage regulator, a two-secondary tap changer and a three-secondary tap changer were simulated. It was shown that, the output voltage can be controlled by just manipulating the firing angles of the thyristors. In this section, the simulation results of the same circuits for resistive and inductive loads are tabulated. Several different firing angles were used in the simulation. Tables 3-1 and 3-2 display the simulation results of the different Regulators.

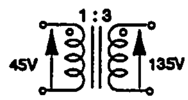
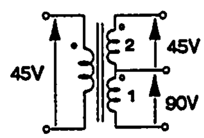
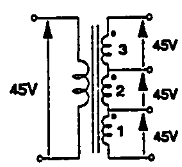
# of Stages used	Vin (RMS)	Vout (RMS)	Firing Angles	Stage used
One-stage		135V	α=0°	1
		120V	α=38°	1
		90V	α=100°	1
		45V	α=164°	1
Two-stage		135V	α=0°	2
		120V	α=68°	1,2
		90V	α=0°	1
		45V	α=164°	1
Three-Stage		135V	α=0°	3
		120V	α=68°	2,3
		120V	α1=30, α2=55	1,2&3
		120V	α1=10, α2=63	1,2&3
		90V	α=0°	2
		45V	α=0°	1

Table 3-1 Simulation Results of the Different Regulators with Resistive Load.

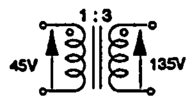
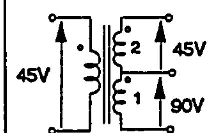
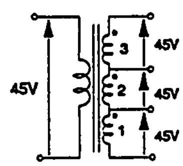
# of Stages used	Vin (RMS)	Vout (RMS)	Firing Angles	Stage used
One-stage		135V	α=0°	1
		120V	α=38°	1
		90V	α=100°	1
		45V	α=164°	1
Two-stage		135V	α=0°	2
		120V	α=68°	1,2
		90V	α=0°	1
		45V	α=164°	1
Three-Stage		135V	α=0°	3
		120V	α=68°	2,3
		120V	α1=30, α2=55	1,2&3
		120V	α1=10, α2=63	1,2&3
		90V	α=0°	2
		45V	α=0°	1

Table 3-2 Simulation Results of the Different Regulators with Inductive Load.

Tables 3-1 and 3-2 reveal that the same output voltage might be achieved with a single-stage, two-stage, and three-stage by just manipulating the firing angles of the circuit used and by using the right transformer that will deliver the necessary input voltage. Therefore, there is no need to use more than one stage to achieve a certain voltage if sufficient input voltage source is provided. By doing that, components will be saved and cost will be cut. Moreover, the strategy needed to control the system will be considerably simpler. It is worth noting that the combinations used to achieve the required voltages are not unique, different combinations might be used to obtain the same output voltages.

3.6 THREE PHASE TAP CHANGER TRANSFORMER

A three-phase tap changer transformer provides a simple and economic method for speed and crane drives control [22]. These type of controllers are also gaining importance as power factor controller in energy savings schemes where the motors are lightly loaded [23,24]. Applications of these controllers also include industrial heating, lighting control, reactive power compensation, and electrochemical processes [25]. Despite the simplicity of such controllers, the analysis of such systems, especially with induction motor loads, is quite complex because of the interaction between the different phases of the system. In the next two subsections the three-phase tap changer will be simulated for resistive and inductive loads.

3.6.1 SIMULATION OF A THREE-PHASE TAP CHANGER TRANSFORMER WITH RESISTIVE LOAD

The three-phase tap changer transformer with resistive load possesses many of the properties of the single-phase tap changer with resistive load. The operation of the circuit is the same as in the single-phase. However, three firing angles are required. One for each phase. Fig. 3-22 shows a three-phase Tap changer transformer with resistive load. During the simulation of the circuit the following firing angles were chosen:

$\alpha_{AN} = 60°$

$\alpha_{BN} = 180°$

$\alpha_{CN} = 300°$

The different simulated waveforms of the controller are shown in Fig. 3-23, 3-24, 3-25 and 3-26.

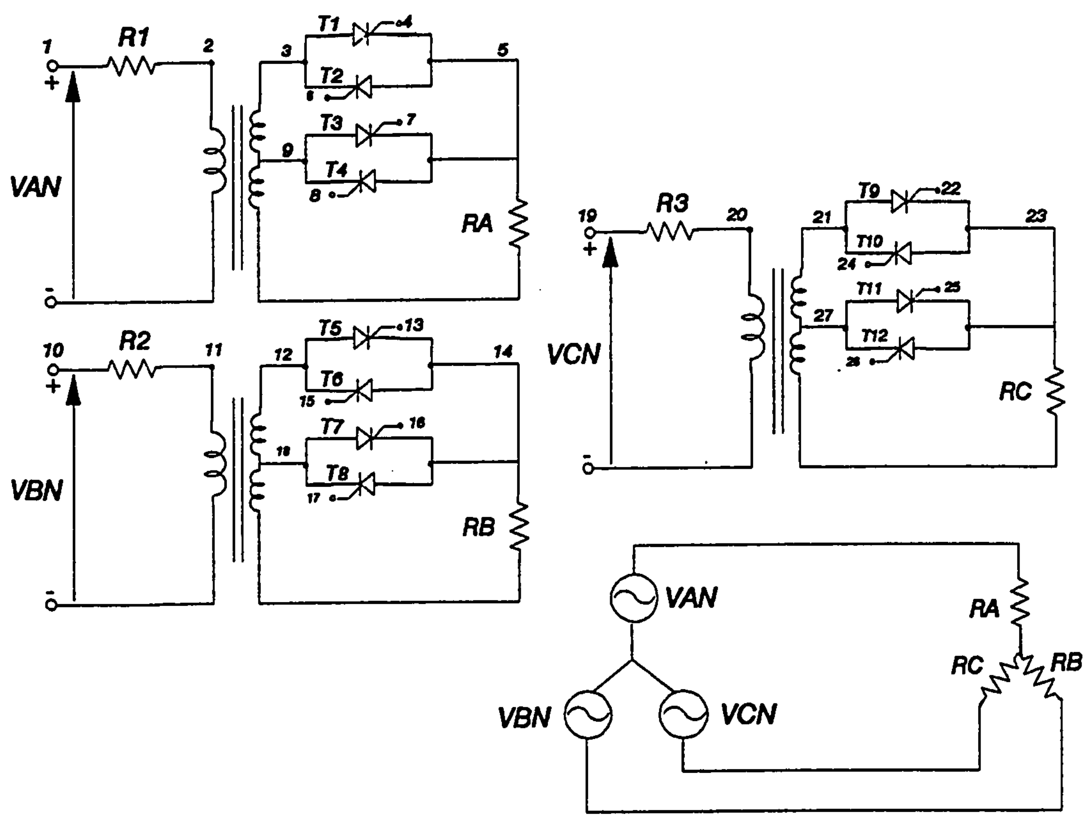


Fig. 3-22 Three-Phase Tap Changer Circuit

with Resistive Load.

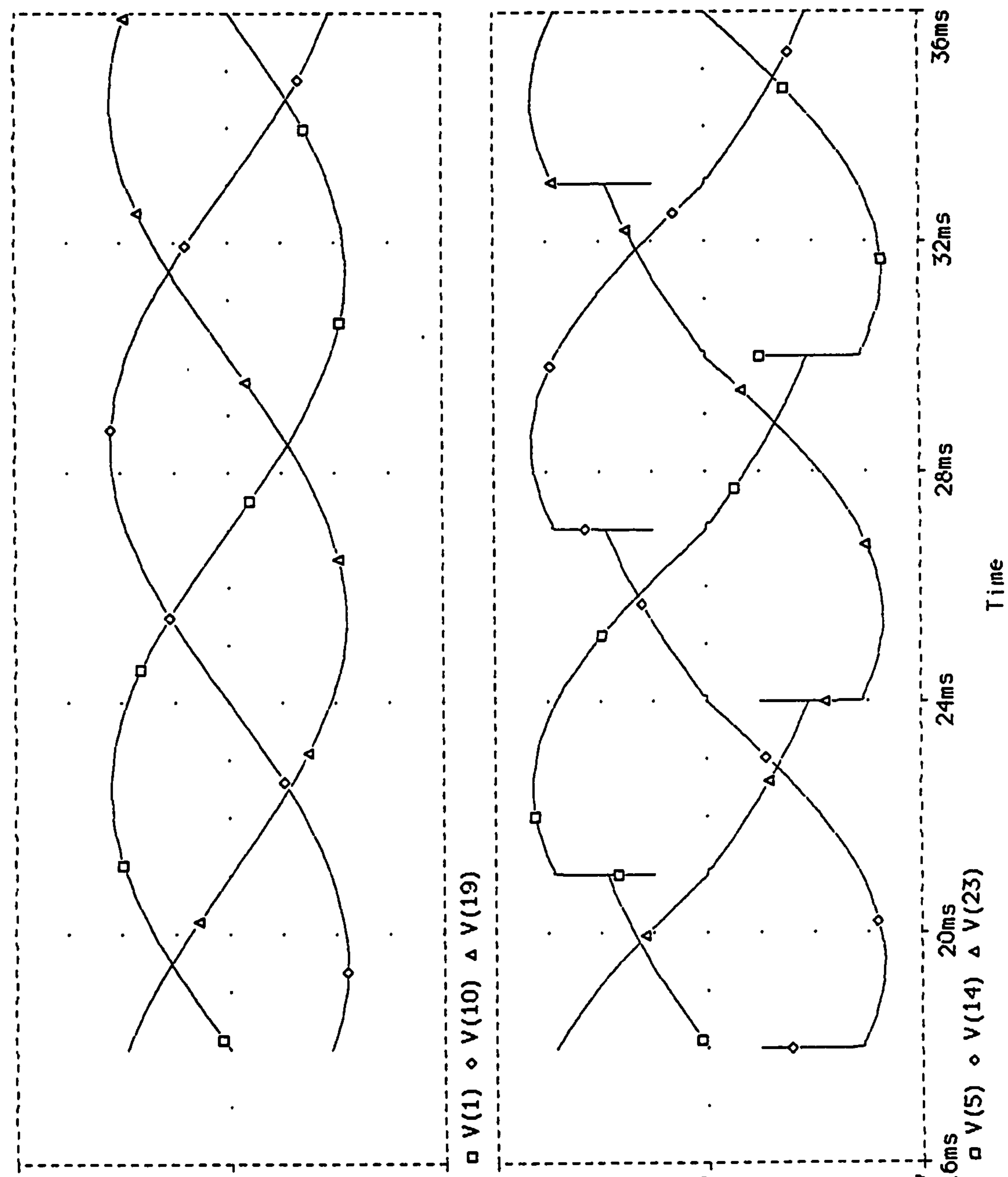


Fig. 3-23 Simulated Waveforms of a Three-Phase Tap Changer with Resistive load.

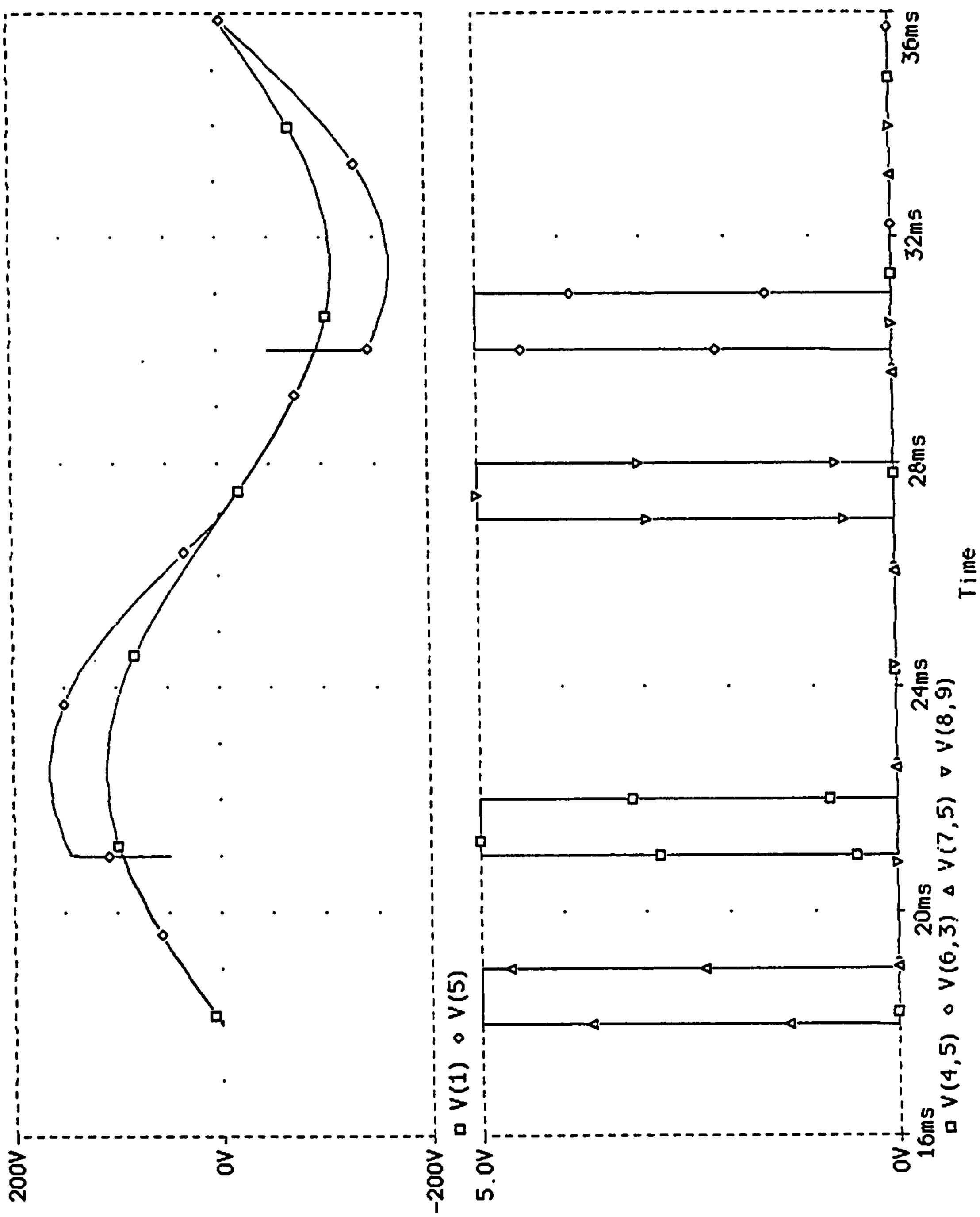


Fig. 3-24 Simulated Waveforms of a Three-Phase Tap Changer with Resistive load for Phase Voltage VAN.

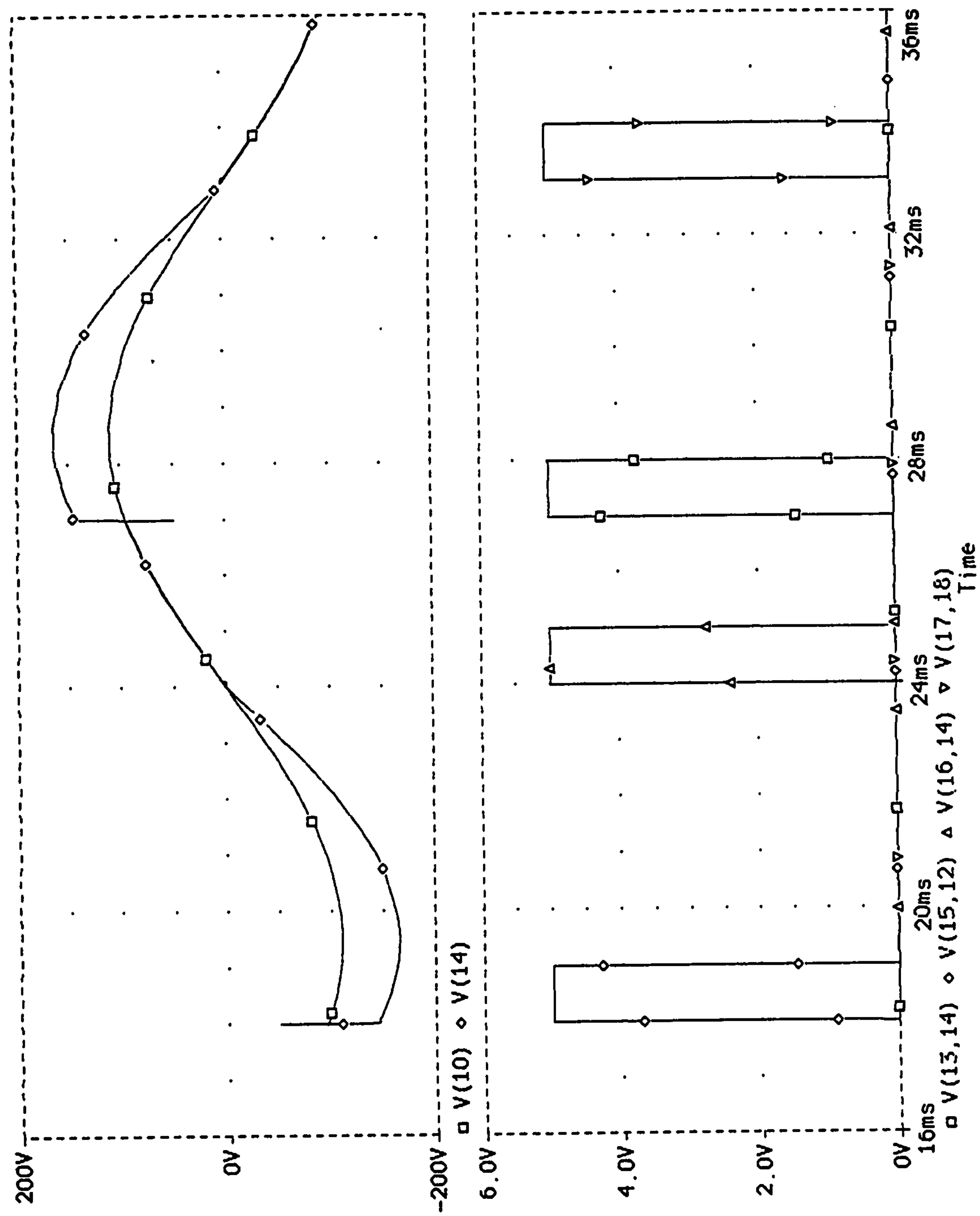


Fig. 3-25 Simulated Waveforms of a Three-Phase Tap Changer with Resistive load for Phase Voltage VBN.

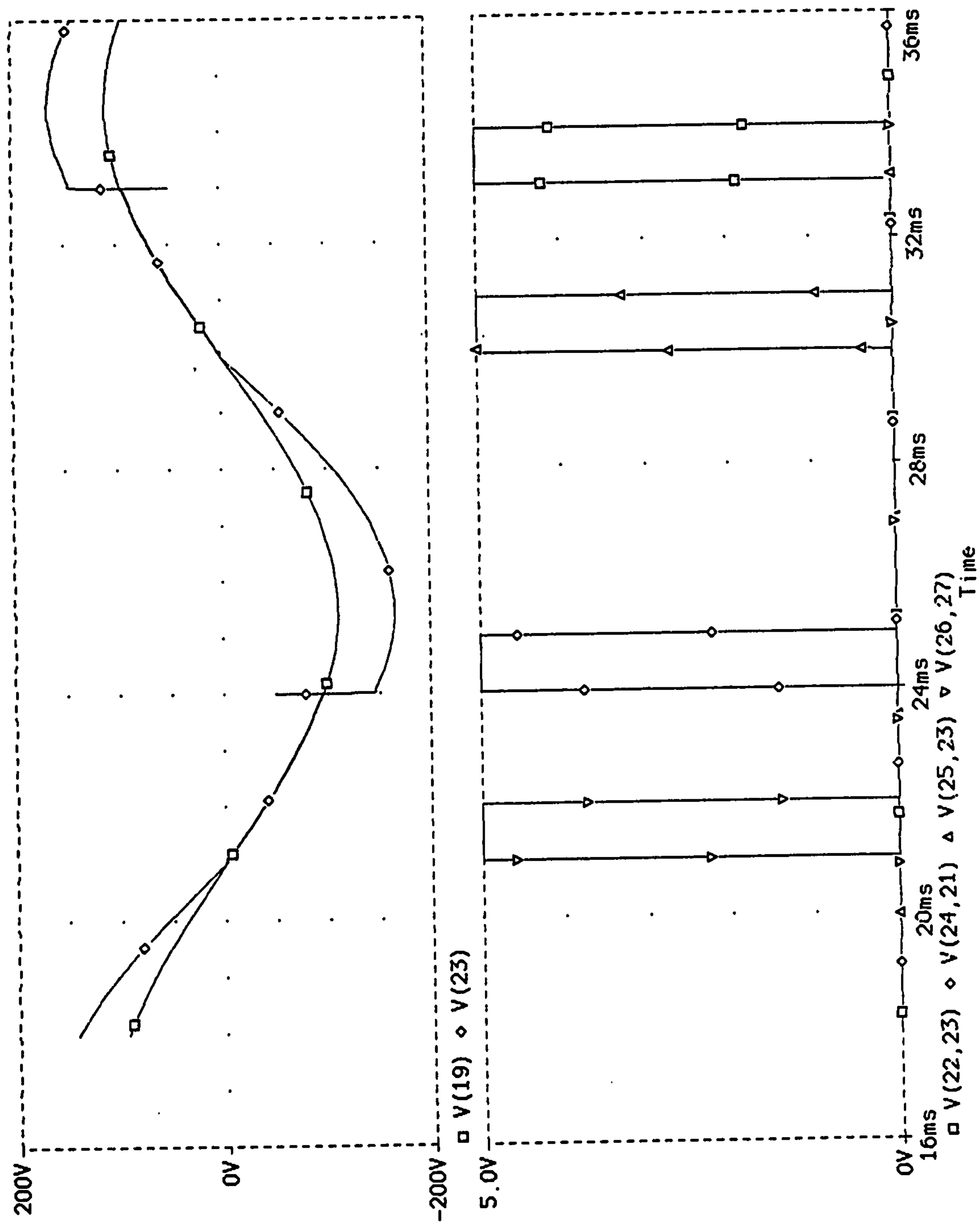


Fig. 3-26 Simulated Waveforms of a Three-Phase Tap Changer with Resistive load for Phase Voltage VCN.

3.6.2 SIMULATION OF A THREE-PHASE TAP CHANGER TRANSFORMER WITH INDUCTIVE LOAD

Fig. 3-27 shows a three-phase Tap changer transformer with inductive load. The three-phase tap changer transformer with inductive load possesses many of the properties and problem of its single-phase counterpart with more complexity. The operation of the circuit is the same as in the single-phase. Of course, care must be taken in designing the control circuit of the system to avoid shorting any of the secondary windings of the transformers. Since the system is three-phase, three firing angles are required. One for each phase. During the simulation of the circuit the following firing angles were chosen:

$\alpha_{AN} = 60°$

$\alpha_{BN} = 180°$

$\alpha_{CN} = 300°$

The different simulated waveforms of the controller are shown in Fig. 3-28, 3-29, 3-30 and 3-31.

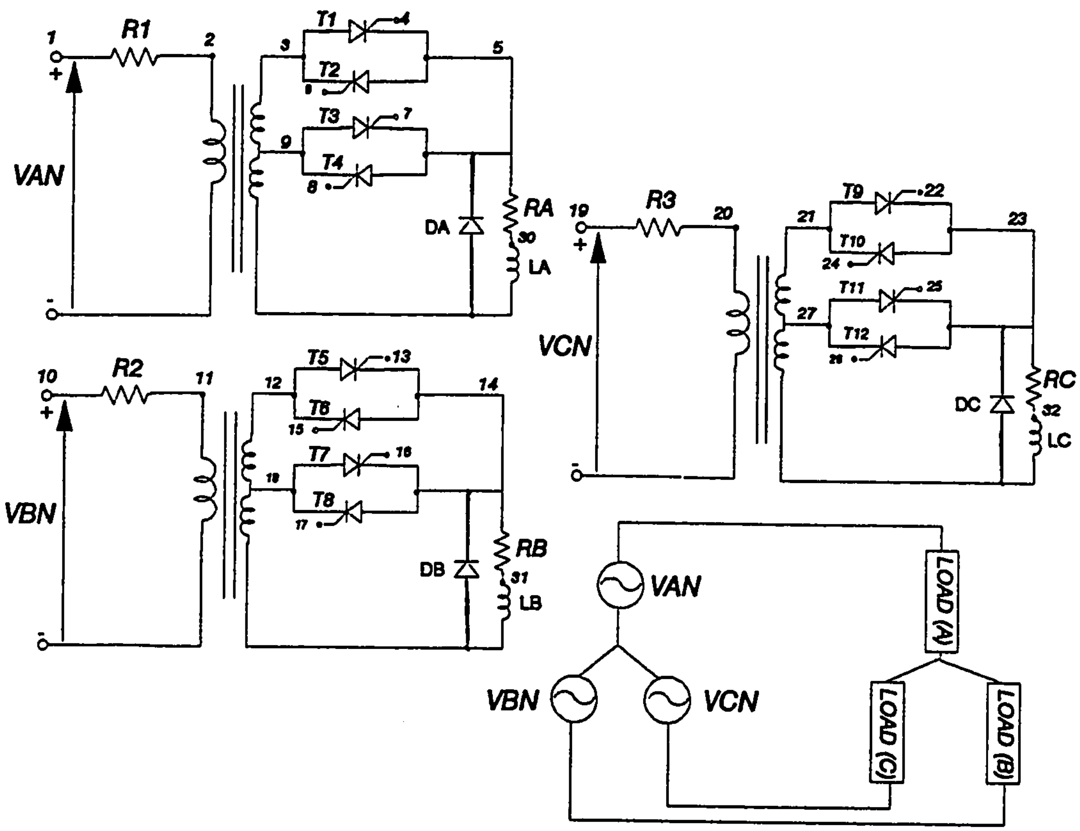


Fig. 3-27 Three-Phase Tap Changer Circuit.

with Inductive Load

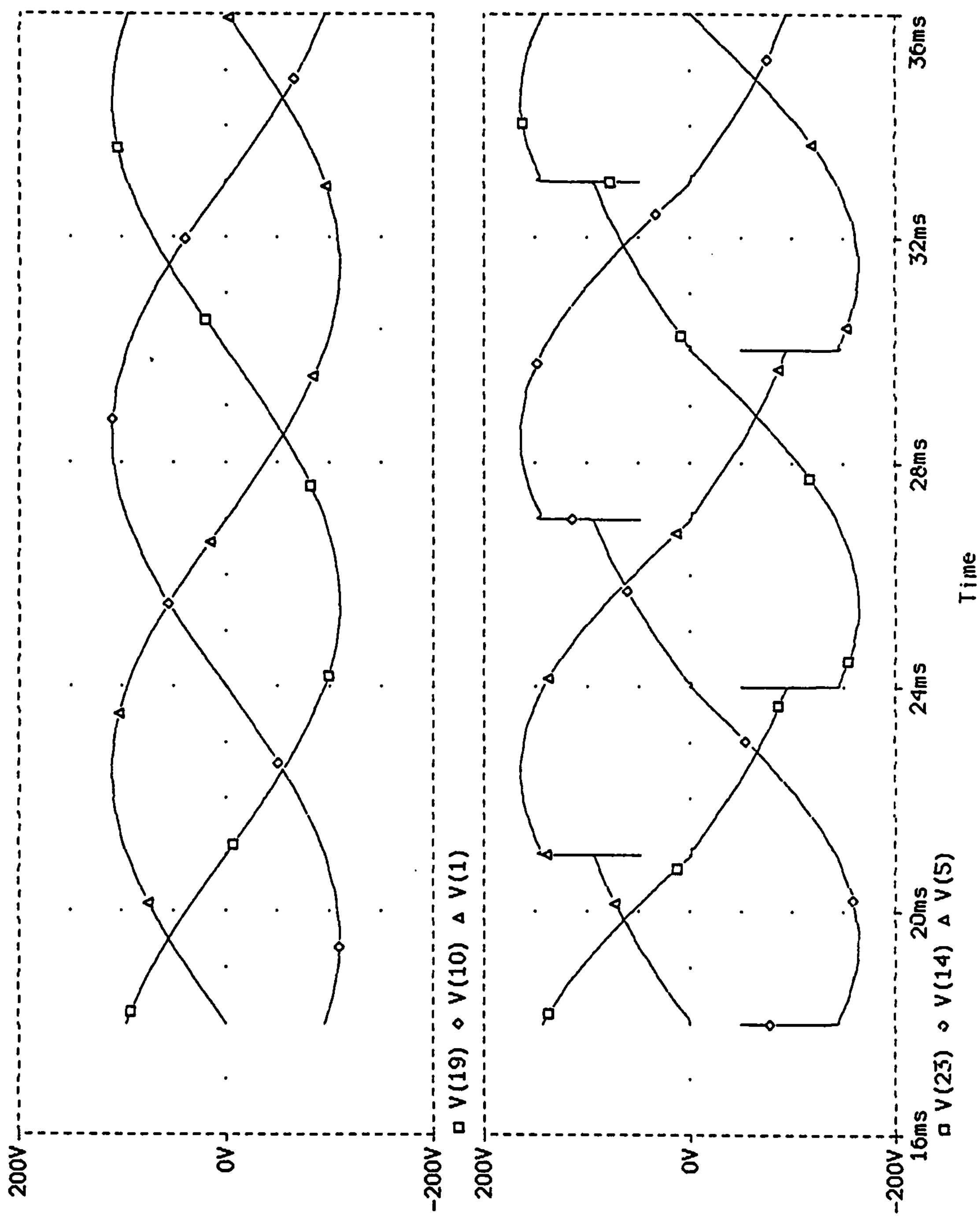


Fig. 3-28 Simulated Waveforms of a Three-Phase Tap Changer with Inductive load.

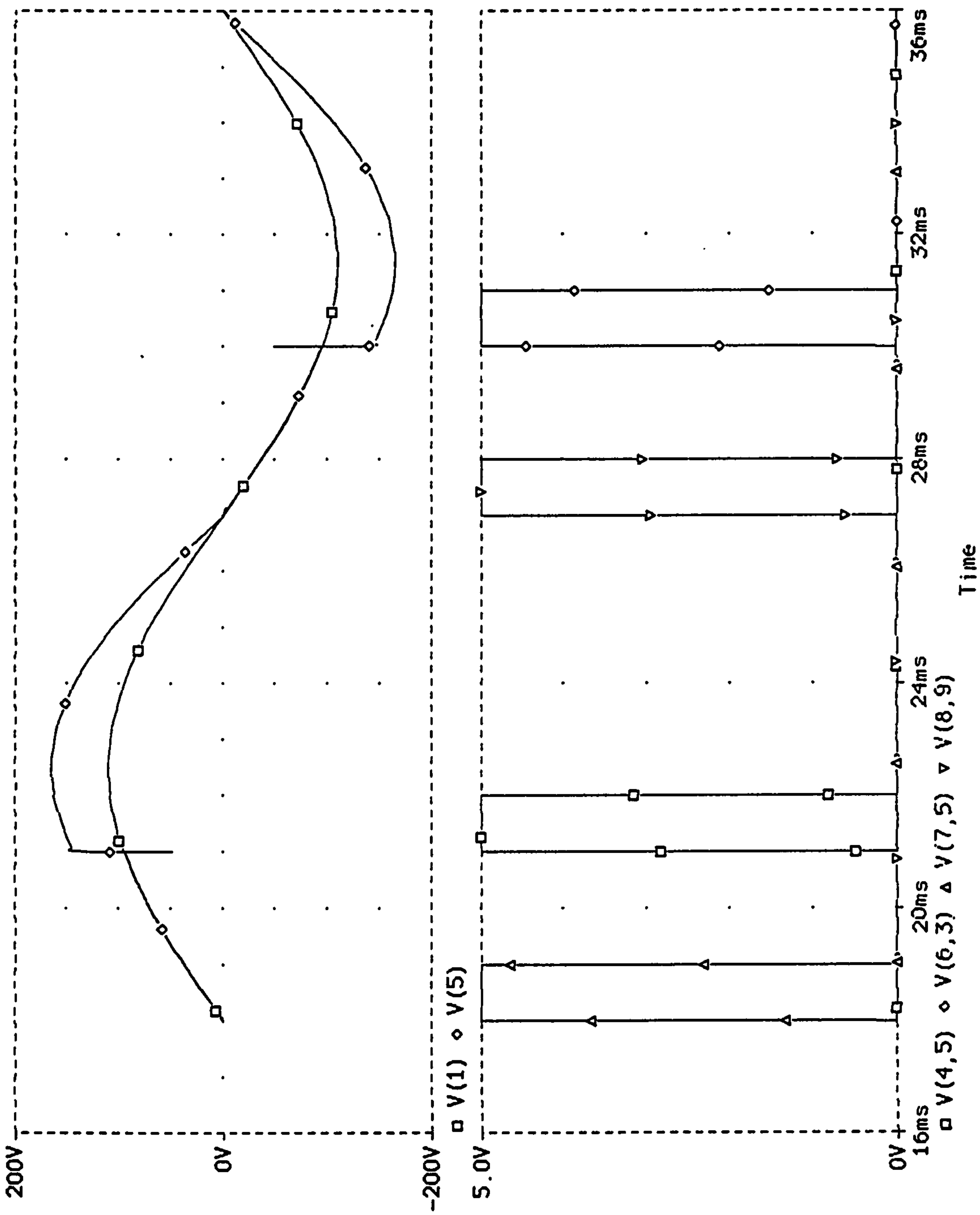


Fig. 3-29 Simulated Waveforms of a Three-Phase Tap Changer with Inductive load for Phase Voltage VAN.

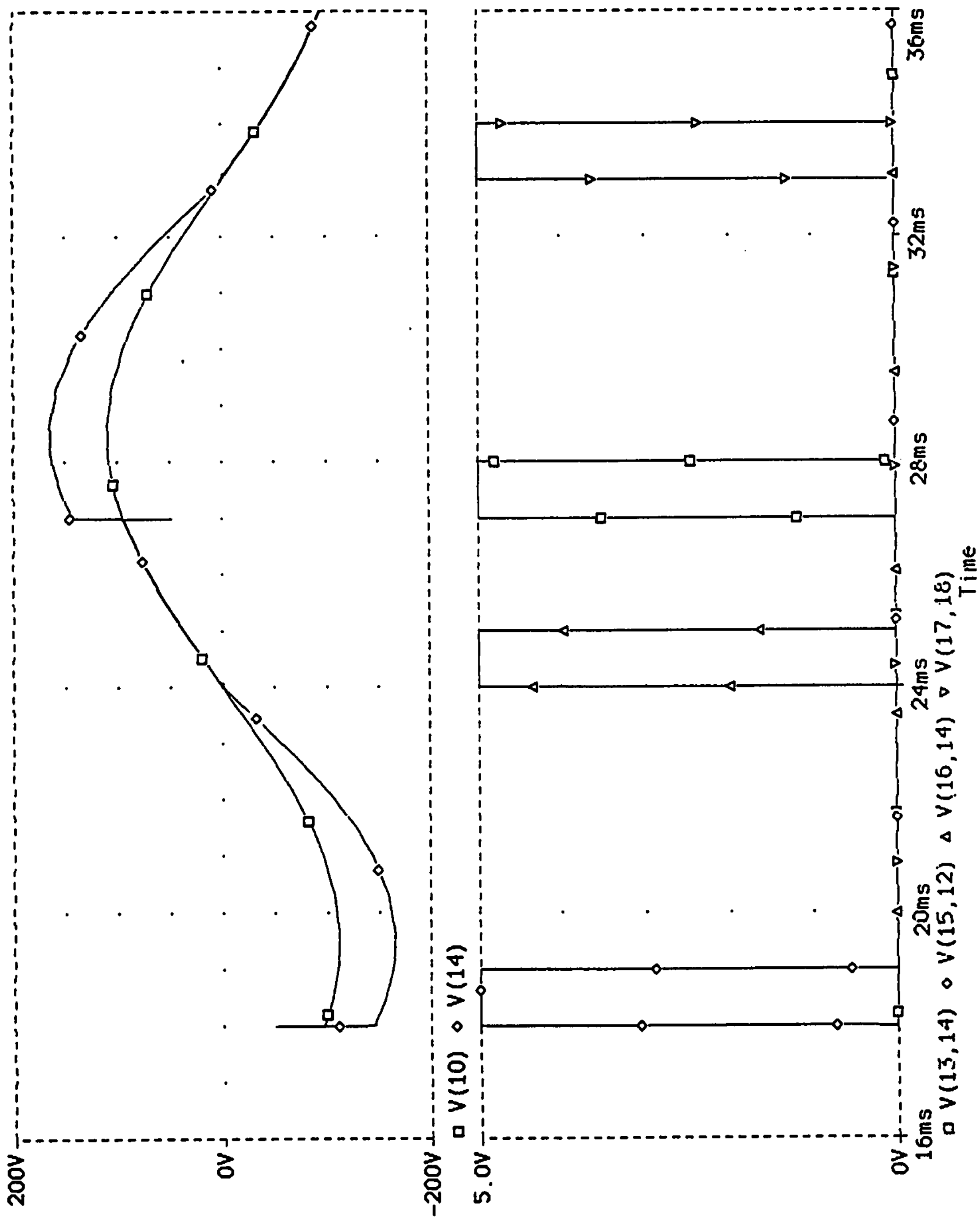


Fig. 3-30 Simulated Waveforms of a Three-Phase Tap Changer with Inductive load for Phase Voltage VBN.

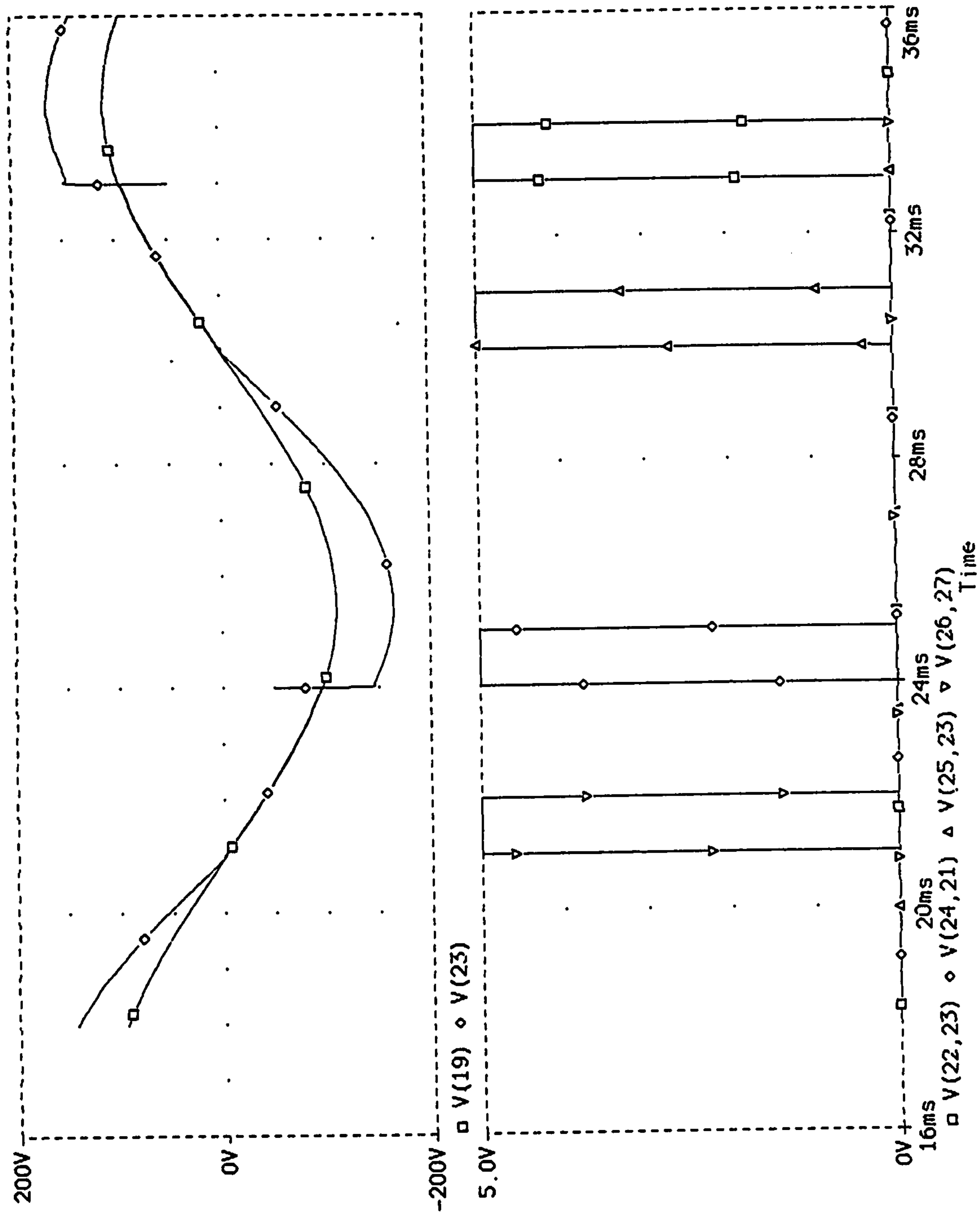


Fig. 3-31 Simulated Waveforms of a Three-Phase Tap Changer with Inductive load for Phase Voltage VCN.

CHAPTER IV

HARDWARE AND SOFTWARE IMPLEMENTATION OF THE PROPOSED AC VOLTAGE REGULATOR

4.1 INTRODUCTION

The proposed regulator is based on an 8-bit MOTOROLA MC68HC11A8 microcontroller. The regulator automatically monitors, adjusts, and maintains the output load voltage within a predetermined range. Fig. 4-1 shows a block diagram of the proposed system. The controller was designed in a single-phase due to the following reasons. The single-phase is in use in many applications, such as lighting control and small motor control. Moreover, the single-phase controller possesses many of the properties and problems of the three-phase controller with less complexity.

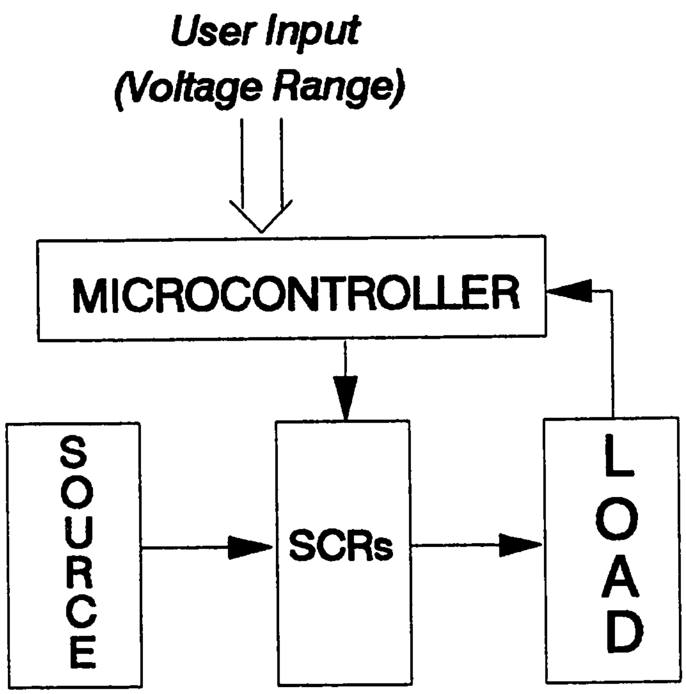


Fig. 4-1 Block Diagram of the Proposed Regulator.

4.2 SYSTEM HARDWARE ARCHITECTURE

Fig. 4-2 shows the overall hardware architecture of the proposed regulator. The proposed regulator consists of two thyristors connected in an antiparallel fashion along with an 8-bit MOTOROLA MC68HC11A8 microcontroller. In addition, an 8-bit digital-to-analog (D/A), a signal conditioner circuit and a control unit to trigger the thyristors are all utilized by the system to perform its functions.

Thyristor switches were used in the proposed regulator instead of mechanical switches because of their high switching frequencies and precise set turn-on points. Only two thyristors are used in implementing the proposed system because, as explained in the previous chapter, there is no need to use more than two thyristors to achieve a specific voltage if sufficient input voltage source is provided.

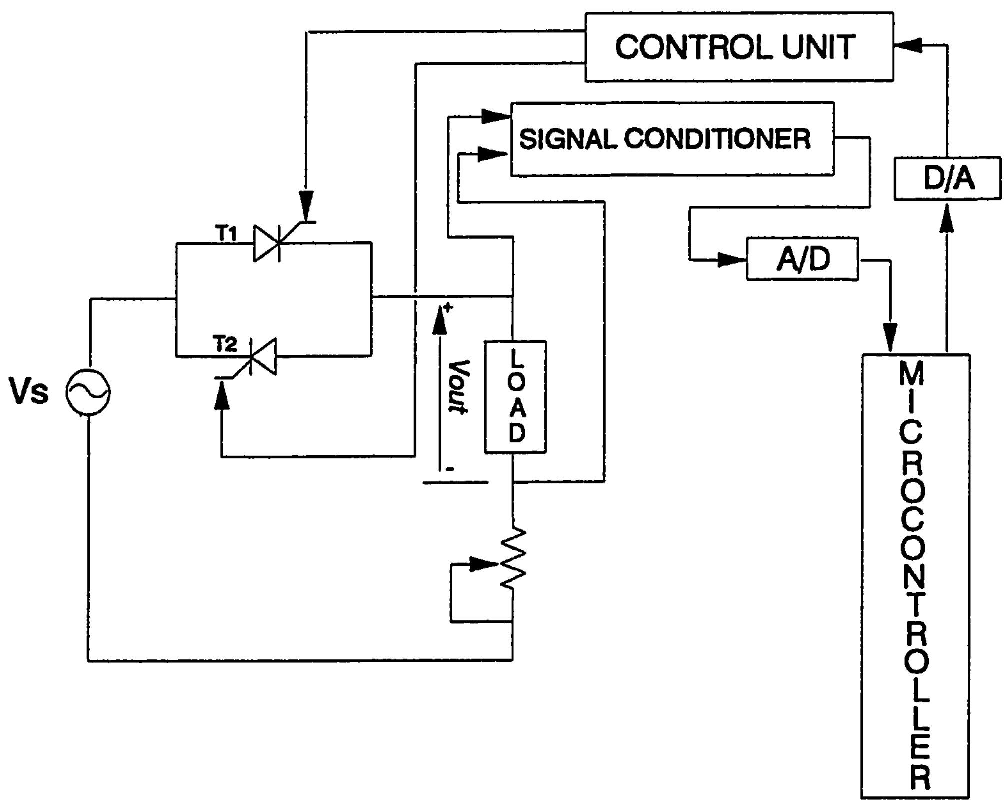


Fig. 4-2 Hardware Architecture.

4.2.1 MC68HC11A8 MICROCONTROLLER

The microcontroller unit in the MC68HC11A8 is equipped with a processing unit, a 2 MHZ clock, interval timer, serial port, and several parallel ports. It is also equipped with 8K bytes of ROM, 512 bytes of EEPROM, and 256 bytes of RAM. Moreover, one of the major peripheral functions provided on-chip is the eight-channel analog-to-digital (A/D) converters with eight bits of resolution [26]. Fig. 4-3 shows a block diagram of the microcontroller [26].

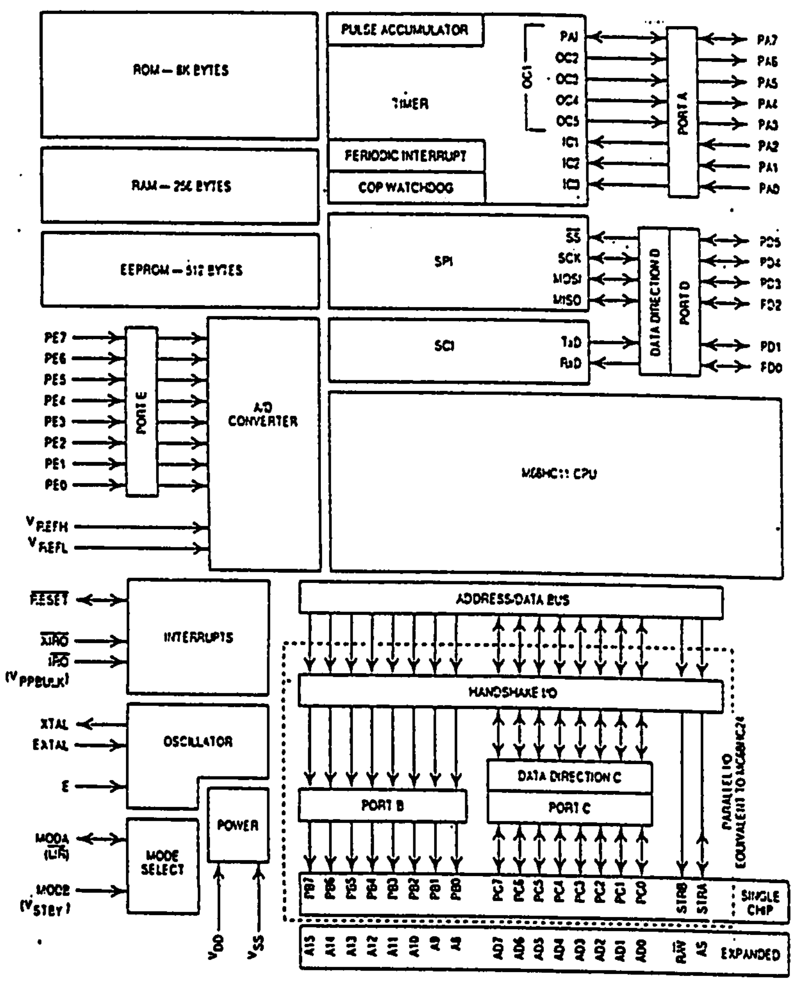


Fig. 4-3 Block Diagram of the MC68HC11A8.

4.2.2 SIGNAL CONDITIONER CIRCUIT

The function of the signal conditioner circuit, shown in Fig. 4-4, is to subdue The monitored load voltage to safeguard the microcontroller from any damage. The output voltage of the signal conditioner circuit should lie between 0 and 5.12 Volts to comply with the requirements of the on-chip 8-bit A/D converter.

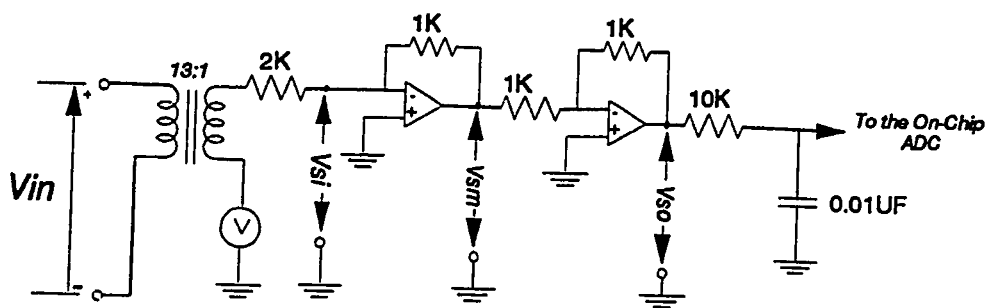


Fig. 4-4 Signal Conditioner Circuit.

Suppose that Vin is as shown in Fig. 4-5, then the resulted Vsi, Vsm and Vso are shown in Fig. 4-6(a), Fig. 4-6(b) and Fig. 4-6(c) respectively.

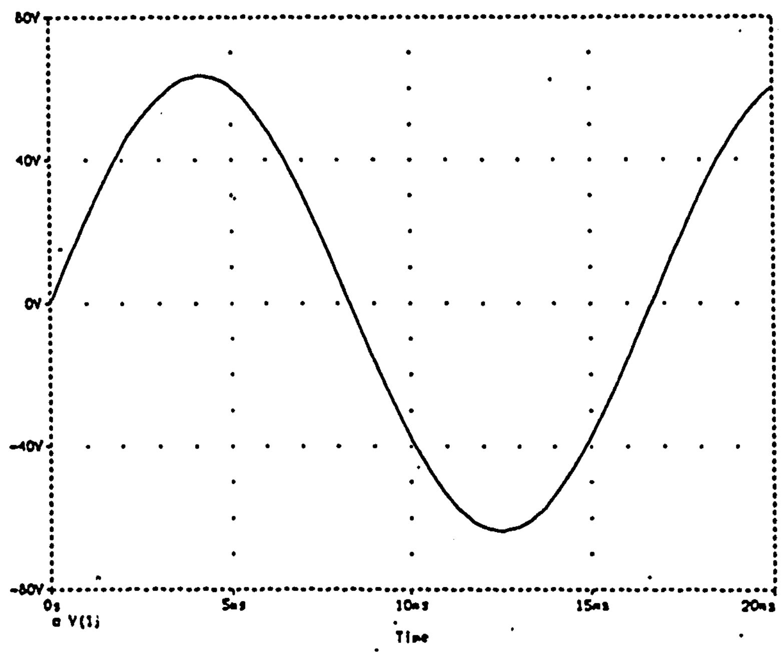
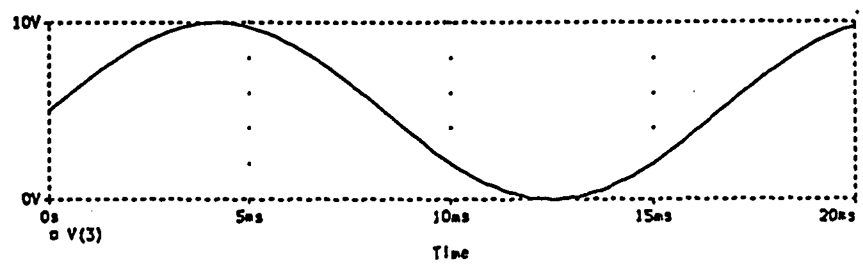
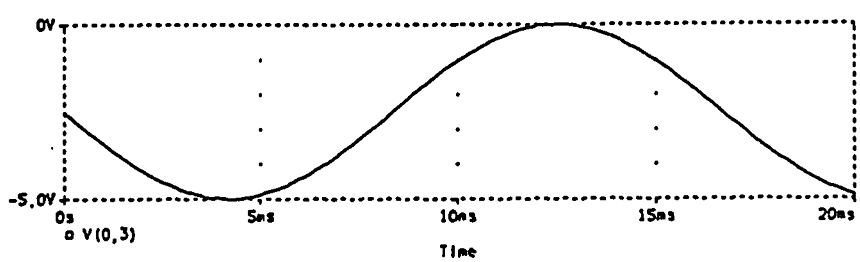


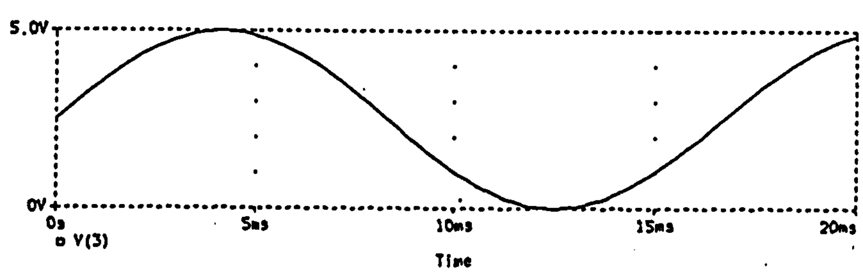
Fig. 4-5 Input Voltage to the Signal Conditioner



(a) Vsi Voltage Waveform.



(b) Vsm Voltage Waveform.



(c) Vso Voltage Waveform.

Fig. 4-6 Signal Conditioner Intermediate Voltages.

4.2.3 THE TWO-PULSE CONTROL UNIT

Fig. 4-7 shows the two-pulse control unit used in the thesis to trigger the thyristors [29]. It is manufactured by LEYBOLD DIDACTIC GMBH (LH) [29]. It supplies trigger pulses at four pulse outputs. The pulse output (5) and (6) supply train of pulses during the positive half-cycle of the mains voltage supply and the pulse outputs (7) and (8) during the negative half-cycle.
The phase of these trigger pulses can be set, dependent on the control voltage U_{ST} = 0...10V, from α = 180° to 0° [29].

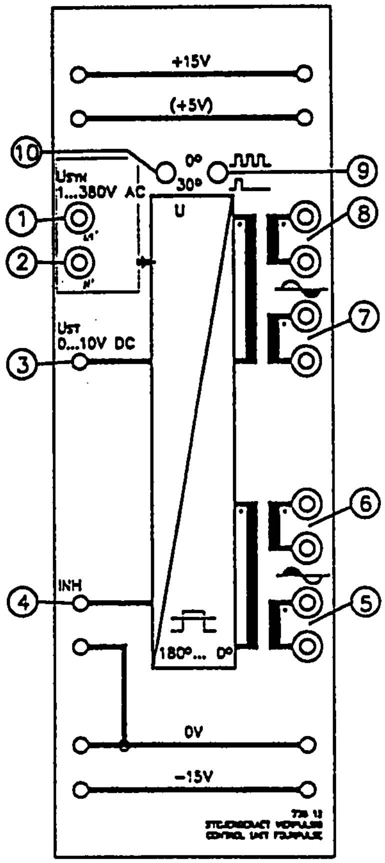


Fig. 4-7 Two-Pulse Control Unit.

4.2.4 THE 8-BIT DIGITAL-TO-ANALOG CONVERTER

The 8-bit D/A converter, shown in Fig. 4-8, gets its input from the 8-bit port (B) of the microcontroller, and its output will set the DC control voltage of the two pulse control unit. The firing angle α can be varied from 0 to π by varying the DC control voltage of the two pulse control unit from 0 to 10 volts. Table 4-1 shows how the D/A converter output and the load voltage varies by just changing Port (B) settings. Therefore by just varying port B settings, manipulation of the output current can be achieved and the output voltage can be maintained within the desirable limit.

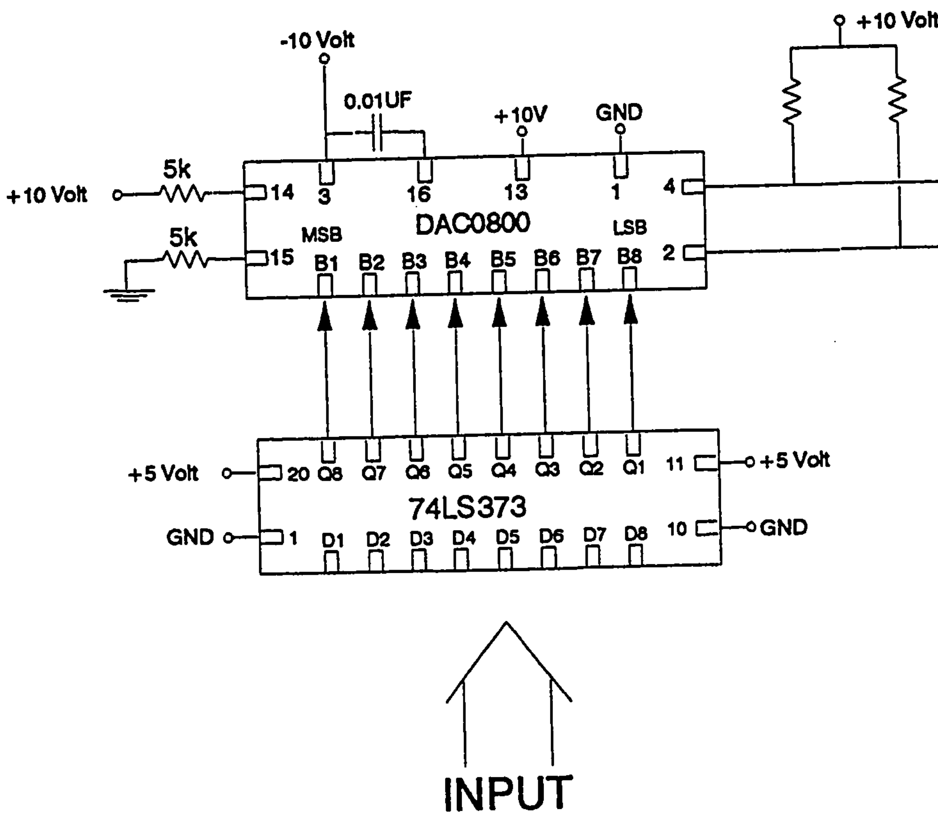


Fig. 4-8 The 8-Bit D/A Converter.

port B	DAC output	Firing angle	Load Voltage
80	00 V	180°	00.0 V
8C	01 V	160°	0.03 V
98	02 V	140°	4.15 V
A4	03 V	120°	13.5 V
B0	04 V	100°	23.4 V
BC	05 V	80°	32.5 V
C8	06 V	60°	39.25 V
D4	07 V	40°	42.00 V
E0	08 V	20°	43.74 V
EC	09 V	00°	45.00 V
F8	10 V	00°	45.00 V
FF	10.6 V	00°	45.00 V

Table 4-1 Port B settings vs. (DAC output, Firing angle & Load Voltage)

Fig. 4-9 shows a plot of the D/A converter output versus the load voltage. Fig. 4-10 shows a plot of the firing angle versus the load voltage.

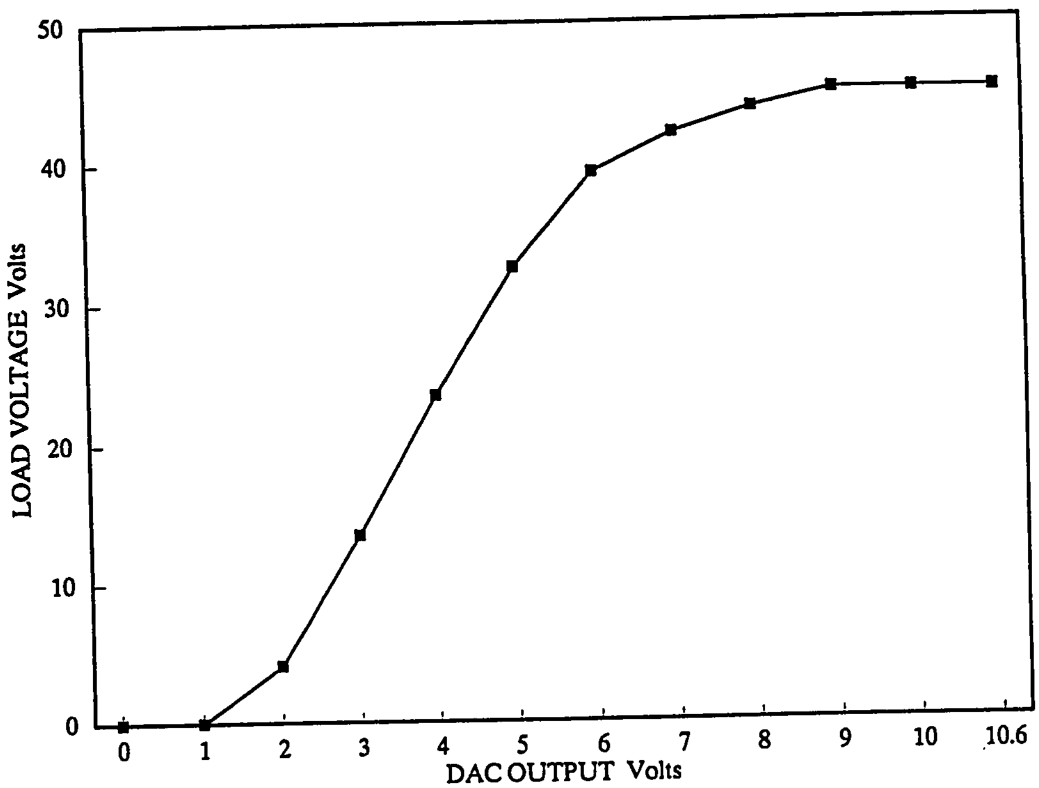


Fig. 4-9 D/A Converter Output vs. Load Voltage.

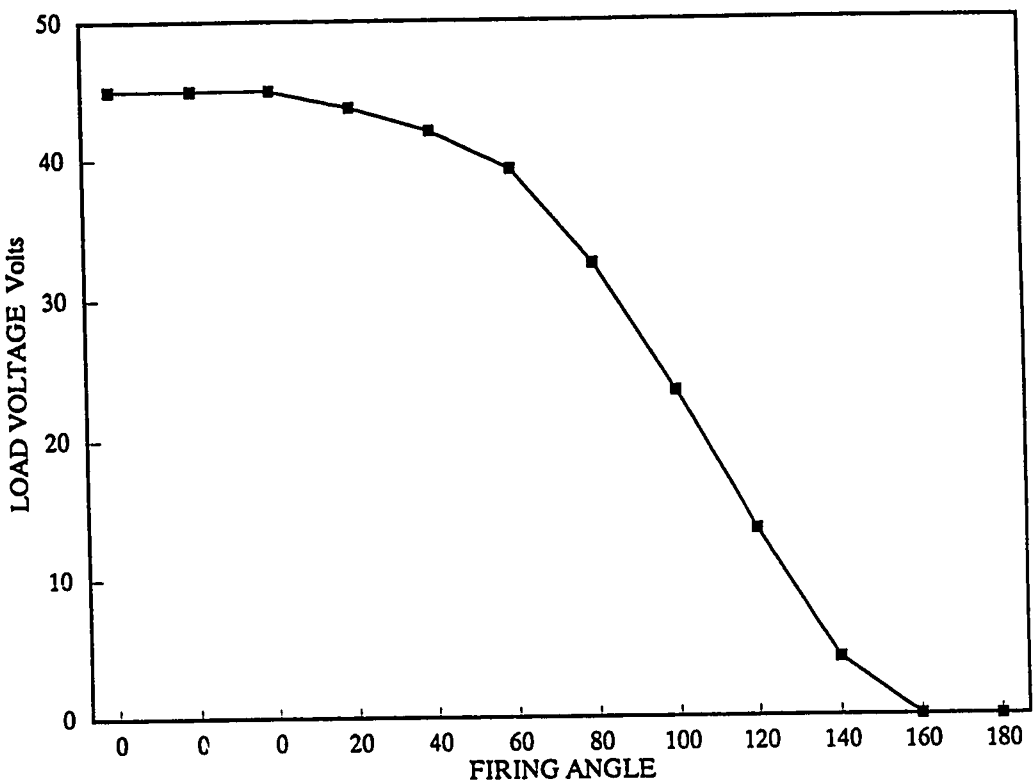


Fig. 4-10 Firing Angle vs. Load Voltage.

4.3 PRINCIPLES OF OPERATION FOR THE PROPOSED REGULATOR

The operation of the proposed regulator is based on a microcontroller software program which initiates a sequence of commands that reads and processes the voltage across the load. Then, a decision based on the value of the load voltage is made. If the load voltage lies within the predetermined range, then no changes is needed and a new reading will be taken. However, if the load voltage is outside the desired range, the microcontroller will increase or decrease the input voltage to the control unit, by changing port B settings, which will update the firing angles of the two thyristors. Having done that, a new reading of the load voltage will be carried out and a new signal will be processed and analyzed to check if the output voltage has reached an acceptable value. Otherwise, a new signal will be issued to the control unit to make up for the error. The above mentioned procedures are repeatedly performed until the desired output voltage is reached.

4.4 REGULATION ALGORITHM AND SOFTWARE IMPLEMENTATION

The regulation program is written in the MC68HC11A8 assembly language rather than a high-level language to minimize the execution time of the program. Thus, a short time will be needed to correct the load voltage if the predetermined range is exceeded. The flowchart of the program is shown in Fig. 4-11. The program consists of four subroutines:

1) Initialization routine

   It sets the program variables.

2) A/D converter programing routine

   It is responsible for programing the on-chip A/D converter and for getting the number of samples required to calculate the V_{rms} across the monitored load.

3) Measurement routine

   It is responsible for calculation of the monitored output voltage. Since the RMS voltage is given by

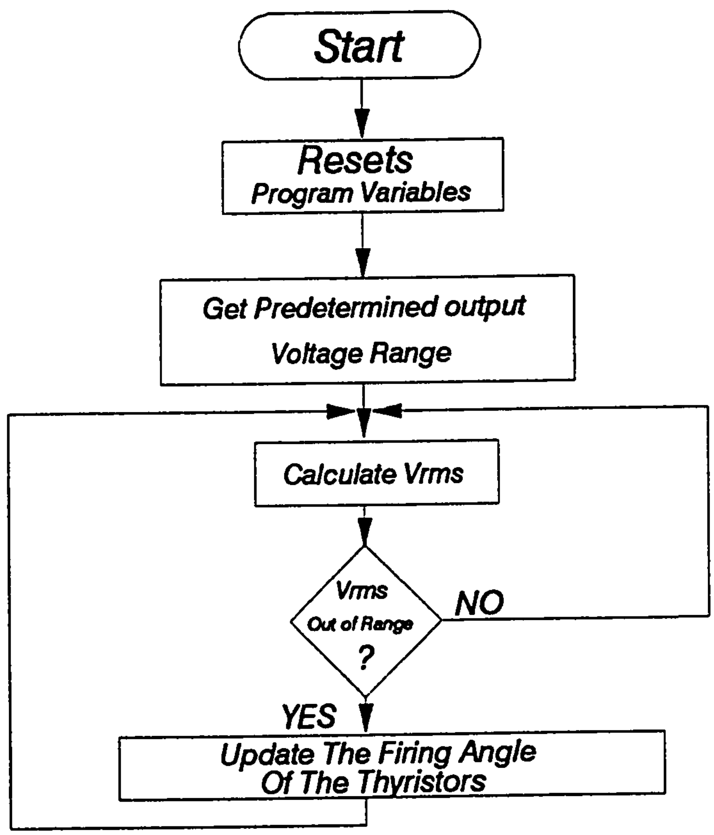


Fig. 4-11 Program Flow Chart.

$$V_{rms} = SQRT\ (1/T \int_0^T v^2(t)dt) \qquad (4\text{-}1)$$

where v(t) is the instantaneous voltage, and T is the period of the voltage waveform [27]. The load voltage is regularly sampled at a rate of 62.5 KHZ and the integration of (4-1) is evaluated numerically by summing the square of the discrete samples over the period. The summation equation used to calculate the output voltage in the program is:

$$V_{out} = SQRT\ (\ 1/N\ (\ \sum_{k=1}^{N} V^2{}_k\ )\ ) \qquad (4\text{-}2)$$

where N represents the number of samples taken over one period [27].

4) <u>Regulation</u> <u>routine</u>

It is responsible for detecting any change in the output voltage. Moreover, it will take a corrective action if the output voltage is found to be outside the predetermined range to ensure the smooth operation of the controller at all times.

4.5 SYSTEM TESTING AND ANALYSIS

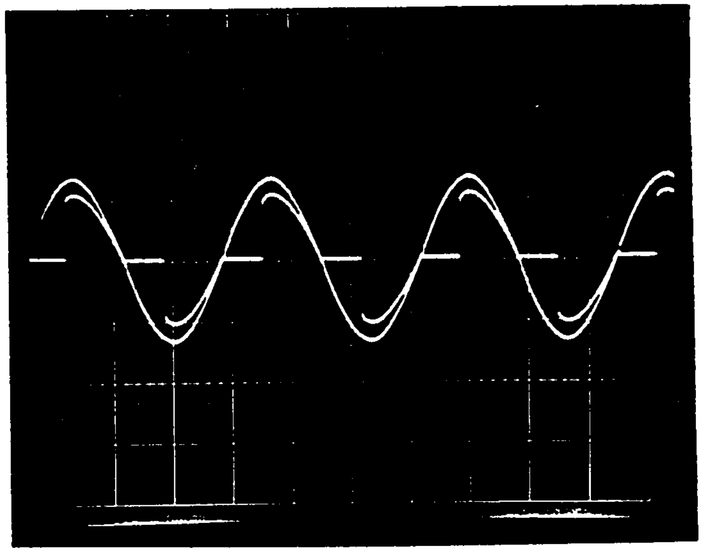
The proposed regulator was tested with resistive and inductive loads. Several ranges were set and the potentiometer, included to simulate a change in the circuit conditions, was taken to both limits (MIN and MAX). Fortunately, the controller was able to cope with the changes in the circuit's load and to maintain the monitored voltage within the predetermined range, with acceptable accuracy ($\leq 5\%$). The experimental results of the test are presented in tables 4-2 and 4-3.

set-range volts	range W/O control	rang with control	% error between set&achvd	
14 - 16	11.7-17.8	14.3-16.2	1.25 %	
19 - 22	17.2-23.9	19.2-21.9	0.00 %	
26 - 28	21.7-30.2	25.9-28.2	0.71 %	Fig 4-12
29 - 30	26.1-37.3	29.3-30.8	2.67 %	
32 - 34	26.8-36.7	32.5-34.2	0.59 %	Fig 4-13
35 - 35	30.1-41.6	35.1-36.3	3.71 %	
33 - 37	30.7-42.1	33.3-37.5	1.35 %	

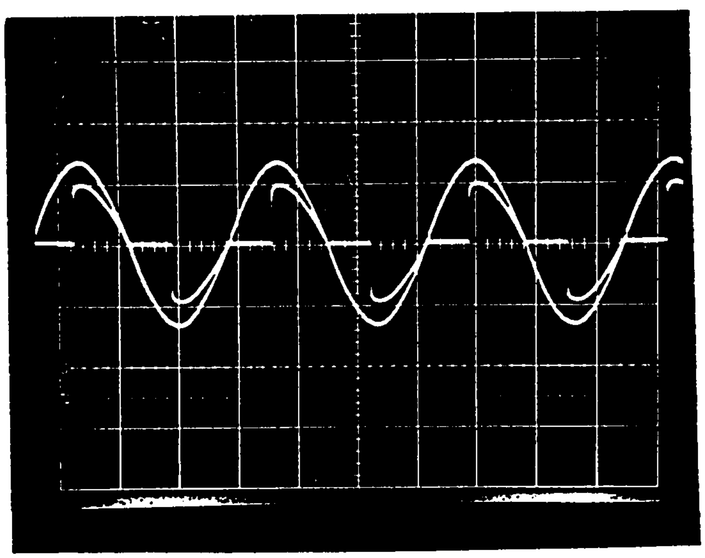
Table 4-2 Experimental Results (Resistive load).

set-range volts	range W/O control	rang with control	% error between set&achvd	
14 - 16	12.2-17.4	13.8-15.7	0.00 %	
19 - 22	17.9-23.5	19.4-22.2	0.90 %	Fig 4-14
26 - 28	22.4-29.8	26.1-28.4	1.42 %	
29 - 30	26.5-36.4	29.3-31.1	3.67 %	
32 - 34	27.1-35.9	32.2-34.5	1.45 %	
35 - 35	30.3-41.3	34.8-36.5	4.29 %	
33 - 37	31.2-41.7	33.7-37.6	1.62 %	Fig 4-15

Table 4-3 Experimental Results (Inductive load).

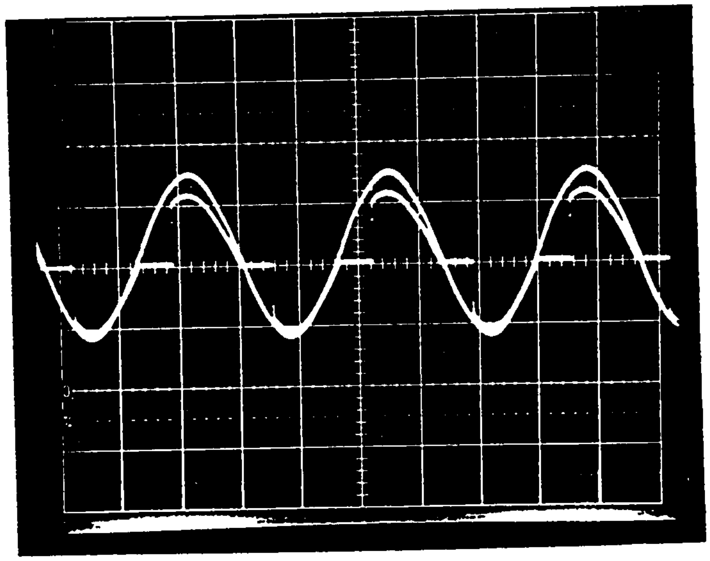


(a) Waveform of the Output Voltage (Vout=28.2 V) and Input Voltage.



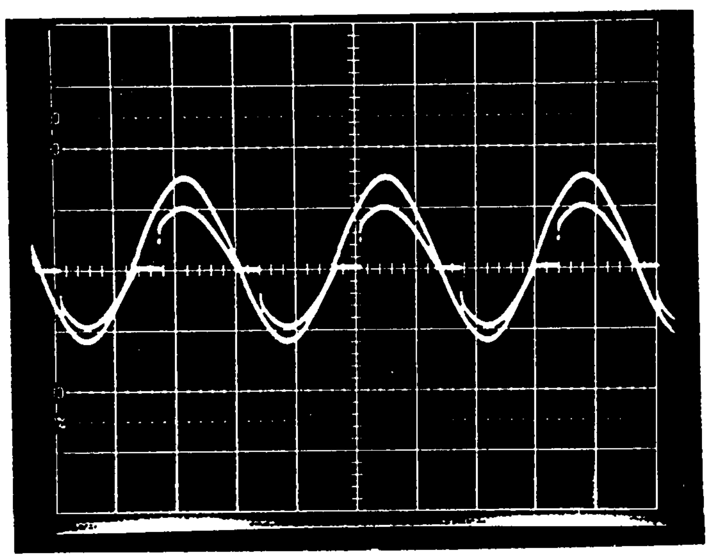
(b) Waveform of the Output Voltage (Vout=25.9 V) and Input Voltage.

Fig. 4-12 Experimental Waveforms



(a) Waveform of the Output Voltage (Vout=34.2 V)

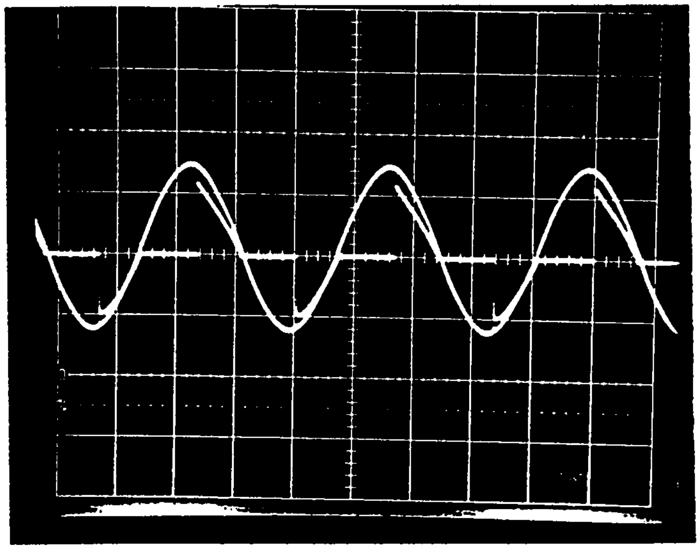
and Input Voltage.



(b) Waveform of the Output Voltage (Vout=32.5 V)

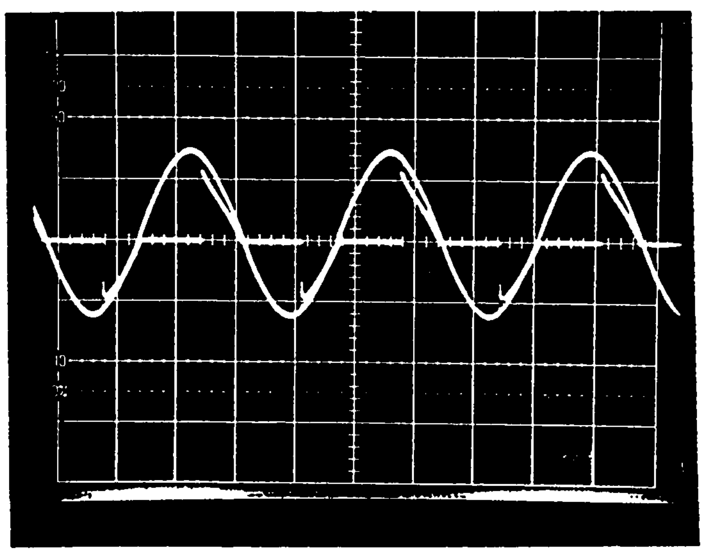
and Input Voltage.

Fig. 4-13 Experimental Waveforms



(a) Waveform of the Output Voltage (Vout=22.2 V)

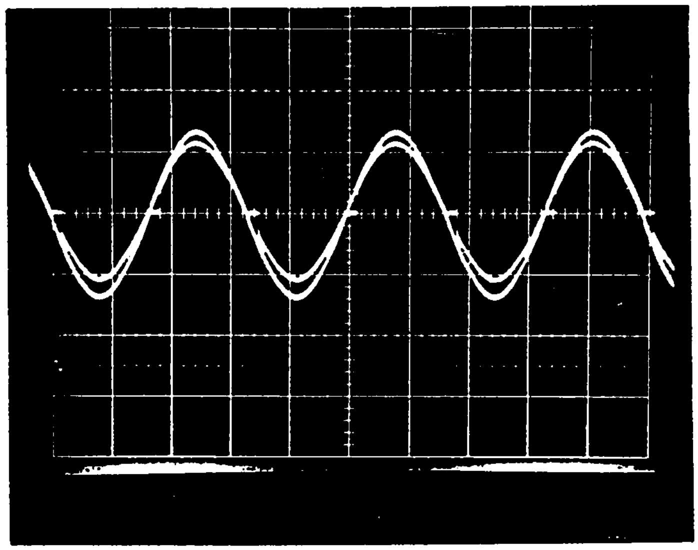
and Input Voltage.



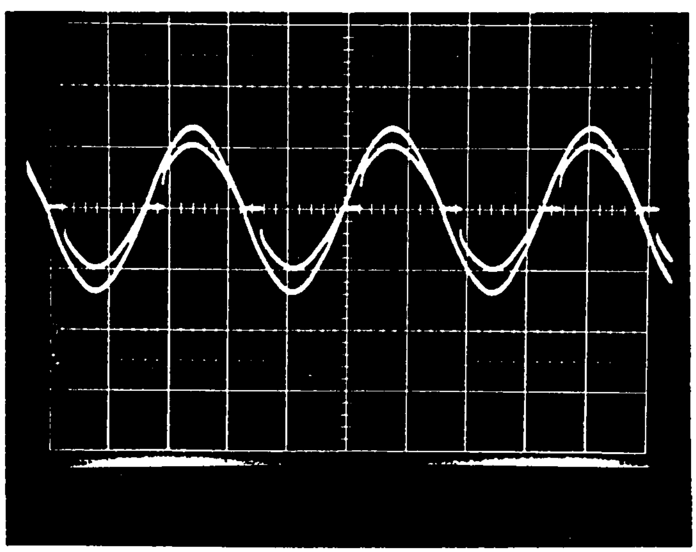
(b) Waveform of the Output Voltage (Vout=19.4 V)

and Input Voltage.

Fig. 4-14 Experimental Waveforms



(a) Waveform of the Output Voltage (Vout=37.6 V) and Input Voltage.



(b) Waveform of the Output Voltage (Vout=33.7 V) and Input Voltage.

Fig. 4-15 Experimental Waveforms

The experimental results shown in table 4-2 and table 4-3 show that the proposed regulator is capable of maintaining the load voltage within (± 5 %) from the predetermined range at all times without any restrictions on the input range. In addition, from the resulted waveforms it is clear that, the method used by the controller leads to a low distortion output voltage. This is because, the correction of the output voltage takes place only once and is not repeated unless the output voltage lies outside the predetermined range. Moreover, the time required to adjust the output voltage is short, because the execution time needed by the program that was developed to carry out the regulation is 0.2495 ms which is extremely short.

The higher values of errors in the previous tables are due to the resolution accuracy of the 8-bit DAC used in the thesis which is:

$$(180° / 256) = 0.703 \text{ Deg.}$$

However if a 10-bit DAC was used, a better resolution would be achieved (0.1758 Deg.). Utilization of a 16-bit DAC would be even better, because its resolution accuracy is (0.00275 Deg.) which is quite good. Therefore, to achieve better results a 10-bit or 16-bit DAC should be used instead of the 8-bit DAC.

CHAPTER V

CONCLUSION AND FUTURE WORK

5.1 DISCUSSION AND CONCLUSION

A new microcontroller-based ac voltage regulator was proposed in this thesis. The regulator is based on an 8-bit MOTOROLA MC68HC11A8 microcontroller. From the simulation results presented in the third chapter, it was found that only two thyristors are necessary to attain a certain voltage. Because of that, the proposed regulator utilizes only two thyristors to regulate the flow of current from the source to the load which reduces the number of components used in its design. As a consequence, the cost of the regulator will be low and the regulation algorithm will be simple. Moreover, the regulator eliminates entirely the problem of electrical and mechanical wear because totally electronic power switches devices were used in its design.

The experimental results shown in chapter four, demonstrate that the proposed regulator is capable of sustaining the load voltage within (± 5 %) from the predetermined range at all times without any restrictions on the input range. The regulator also achieves this with a short correction time because the regulation algorithm is written in the MC68HC11A8 assembly language. Stable voltage and lower distortion are provided by the regulator, since the correction of the output voltage takes place only once and is not repeated unless the output voltage has not reached the predetermined range.

In addition to the above advantages, the proposed regulator offers flexible and low-cost approach to voltage regulation, because of its programmability nature. It is also easily serviced and fully automatic. Because of its fast dynamic response, significant energy savings are made and good quality service is provided.

5.2 FUTURE WORK

Further work can be pursuit in the following areas:

1) A 10-bit or 12-bit A/D converters might be used instead of the 8-bit A/D used in the proposed regulator to achieve better regulation accuracy.

2) The regulator can be implemented for a three-phase instead of a single-phase.

APPENDIX A

```
*    ... PSPICE Source File for a Single Phase AC Voltage
*             Regulator with Resistive Load ...
* ................................................
*    ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  20
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0) .MODEL  DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  10UF
.ENDS
*.......................................................
X1  1  4  2  SCRM
X2  2  5  1  SCRM
RL  2  0  100
VG1  4  2  PULSE(0  5  1MS    .5US  .5US  1MS  16.66MS)
```

```
VG2  5  1  PULSE(0  5  9.33MS  .5US  .5US  1MS  16.66MS)
VAN  1  0  SIN(0  110  60  0  0)
.TRAN  .4MS  30MS
.PROBE
.END
```

```
*    .... PSPICE Source File for a Single Phase Voltage
*                 Regulator with Inductive Load ....
*.................................................
* ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  20
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0) .MODEL  DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  10UF
.ENDS
*     ........  END OF SCR SUBCKT  ..........
X1 1    4 2 SCRM
X2  2  5  1  SCRM
RL  2  6  100
L1  6  0  50mH
D1  0  6  DIODE
VG1  4  2  PULSE(0  5  1MS     .5US  .5US  1MS  16.66MS)
```

```
VG2  5  1  PULSE(0  5  9.33MS  .5US  .5US  1MS  16.66MS)
VAN  1  0  SIN(0  110  60  0  0)
.MODEL  DIODE  D
.TRAN  .4MS  30MS
.PROBE
.END
```

```
*    ... PSPICE SOURCE File for a Tab Changer Transformer
*                  with Resistive Load ....
* .................................................
* ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  750
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  0.2UF
.ENDS
*     ......... END OF SCR SUBCKT .......
X1   3   6   7   SCRM
X2   7   8   3   SCRM
X3   4   9   7   SCRM
X4   7   10  4   SCRM
* ......................................................
```

```
* ... The magnetic specification of the transformer ...
*         ......   PRIMARY   ......
L1  2  0  0.5MH
*          .....   SECONDARY  .......
L2  3  4  0.5MH
L3  4  0  0.5MH
*  .............  MAGNETIC COUPLING  ................
KALL   L1  L2  L3  0.9999
* ..................................................
R1   1  2  1U
RL   7  0  100
VG1  6  7  PULSE(0  5  3MS    .5US  .5US  1MS  18MS)
VG2  8  3  PULSE(0  5  12MS   .5US  .5US  1MS  18MS)
VG3  9  7  PULSE(0  5  0MS    .5US  .5US  1MS  18MS)
VG4  10 4  PULSE(0  5  9MS    .5US  .5US  1MS  18MS)
VAN  1  0  SIN(0  110  55.555  0  0)
.TRAN  .4MS  30MS
.OPTIONS NOMOD NOPAGE RELTOL=0.03 ABSTOL=1UA VNTOL=1MV
 ITL4=40 ITL5=0
.PROBE
.END
```

```
*   ... PSPICE Source File for a Tab Changer Transformer
*                  with Inductive Load ...
* ..............................................
*   ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  750
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  0.5UF
.ENDS
*    ....... END OF SCR SUBCKT ..........
X1   3   6   7   SCRM
X2   7   8   3   SCRM
X3   4   9   7   SCRM
X4   7   10  4   SCRM
* .....................................................
```

```
*  ... The magnetic specification of the transformer ...
*          ......   PRIMARY   ......
L1  2  0  0.5MH
*            .....   SECONDARY  .......
L2  3  4  0.5MH
L3  4  0  0.5MH
*  .............  MAGNETIC COUPLING  ................
KALL   L1  L2  L3  0.9999
* ..................................................
R1   1  2  1UOHM
RL   7  12  100
L4   12  0  100mH
D1   0   12  DIODE
VG1  6  7  PULSE(0  5  4MS     .5US  .5US  1MS  18MS)
VG2  8  3  PULSE(0  5  13MS    .5US  .5US  1MS  18MS)
VG3  9  7  PULSE(0  5  0MS     .5US  .5US  1MS  18MS)
VG4  10 4  PULSE(0  5  9MS     .5US  .5US  1MS  18MS)
VAN  1  0  SIN(0  110  55.555  0  0)
.MODEL DIODE  D
.TRAN  .4MS  30MS
.OPTIONS NOMOD NOPAGE RELTOL=0.02  ABSTOL=1UA  VNTOL=1MV
 ITL4=40  ITL5=0 .PROBE
.END
```

```
*  .... PSPICE Source File for a Tap Changer Transformer
*                with Three Secondary Windings ....
*                  .... Resistive Load ....
* ................................................
*      ........ SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  500
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  0.5UF
.ENDS
*  ............ END OF SCR SUBCKT ............
X1   3   6   7   SCRM
X2   7   8   3   SCRM
X3   4   9   7   SCRM
```

```
X4   7   10  4   SCRM
X5   5   11  7   SCRM
X6   7   12  5   SCRM
* ......................................................
* ... The magnetic specification of the transformer ...
*          ......   PRIMARY   ......
L1  2  0  0.5MH
*           .....   SECONDARY  .......
L2  3  4  0.5MH
L3  4  5  0.5MH
L4  5  0  0.5MH
*  .............  MAGNETIC COUPLING  ................
KALL   L1  L2  L3  L4  0.9999
* ..................................................
R1   1  2  1UOHM
RL   7  0  100
* ......................................................
VG1  6  7  PULSE(0  5  5MS   .5US  .5US  1MS  18MS)
VG2  8  3  PULSE(0  5  14MS  .5US  .5US  1MS  18MS)
VG3  9  7  PULSE(0  5  3MS   .5US  .5US  1MS  18MS)
VG4  10 4  PULSE(0  5  12MS  .5US  .5US  1MS  18MS)
VG5  11 7  PULSE(0  5  0MS   .5US  .5US  1MS  18MS)
VG6  12 5  PULSE(0  5  9MS   .5US  .5US  1MS  18MS)
* ......................................................
```

```
VAN  1  0  SIN(0  110  55.555  0  0)
.OPTIONS NOMOD NOPAGE RELTOL=0.7 ABSTOL=8UA VNTOL=8MV
 ITL4=40 ITL5=0 .TRAN  5MS  20MS
.PROBE
.END
```

```
*  ....  PSPICE Source File for a Tap Changer Transformer
*               with Three Secondary Windings ....
*              .....  Inductive Load   .....
* ................................................
*     .......  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  700OHM
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL  DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  0.5UF
.ENDS
*     ......... END OF SCR SUBCKT ..........
*  .....................................................
X1   3   6   7   SCRM
X2   7   8   3   SCRM
```

```
X3    4    9    7    SCRM
X4    7    10   4    SCRM
X5    5    11   7    SCRM
X6    7    12   5    SCRM
* .......................................................
* The magnetic specification of the transformer.
*          ......   PRIMARY   ......
L1   2   0   0.5MH
*           .....   SECONDARY  .......
L2   3   4   0.5MH
L3   4   5   0.5MH
L4   5   0   0.5MH
*  .............  MAGNETIC COUPLING  ................
*
KALL   L1  L2  L3  L4  0.9999
*
* ...................................................
R1    1  2    1UOHM
RL    7  15   100
L5    15  0   100mH
D1    0    15  DIODE
* .......................................................
VG1  6  7  PULSE(0  5  6MS    .5US  .5US  1MS  18MS)
VG2  8  3  PULSE(0  5  15MS   .5US  .5US  1MS  18MS)
```

```
VG3   9   7   PULSE(0   5   3MS    .5US   .5US   1MS   18MS)
VG4   10  4   PULSE(0   5   12MS   .5US   .5US   1MS   18MS)
VG5   11  7   PULSE(0   5   0MS    .5US   .5US   1MS   18MS)
VG6   12  5   PULSE(0   5   9MS    .5US   .5US   1MS   18MS)
* ....................................................
VAN  1  0  SIN(0  110  55.555  0  0)
.MODEL DIODE D
.OPTIONS NOMOD NOPAGE RELTOL=0.7 ABSTOL=8UA VNTOL=8MV
 ITL5=0 ITL4=40
.TRAN  5MS  20MS
.PROBE
.END
```

```
* .... PSPICE Source File for a Three-Phase Tab Changer
*        Transformer Circuit with Resistive Load ....
* .....................................................
*       ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  750
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  .1UF
.ENDS
*          .......  END OF SCR SUBCKT .......
*......................................................
*          .......  Phase Voltage VAN  .......
VAN  1  0  SIN(0  110  55.555 )
R1   1  2  1UOhm
*   ... The magnetic specification of the transformer ...
```

```
*          ......  PRIMARY  ......
L1  2  0  0.5MH
*           .....  SECONDARY  .......
L2  3  9  0.5MH
L3  9  0  0.5MH
*          .....  MAGNETIC COUPLING  .....
KALLA   L1  L2  L3  0.9999
* ..................................................
X1   3   4   5   SCRM
X2   5   6   3   SCRM
X3   9   7   5   SCRM
X4   5   8   9   SCRM
* ......................................................
RA   5   0   100Ohm
VG1  4   5   PULSE(0  5  21MS   .5US .5US  1MS  18MS)
VG2  6   3   PULSE(0  5  30MS   .5US .5US  1MS  18MS)
VG3  7   5   PULSE(0  5  18MS   .5US .5US  1MS  18MS)
VG4  8   9   PULSE(0  5  27MS   .5US .5US  1MS  18MS)
*.......................................................
*          .......  Phase Voltage VBN  .......
VBN  10  0  SIN(0  110  55.555   0.006)
R2   10  11  1UOhm
*   ... The magnetic specification of the transformer ...
*          ......  PRIMARY  ......
```

```
L4  11  0  0.5MH
*          .....  SECONDARY  .......
L5  12  18  0.5MH
L6  18  0   0.5MH
*        .....  MAGNETIC COUPLING  .....
KALLB   L4  L5  L6  0.9999
* .................................................
X5   12   13   14   SCRM
X6   14   15   12   SCRM
X7   18   16   14   SCRM
X8   14   17   18   SCRM
* .....................................................
RB   14  0  100Ohm
VG5  13  14  PULSE(0  5  9MS   .5US .5US 1MS  18MS)
VG6  15  12  PULSE(0  5  18MS  .5US .5US 1MS  18MS)
VG7  16  14  PULSE(0  5  6MS   .5US .5US 1MS  18MS)
VG8  17  18  PULSE(0  5  15MS  .5US .5US 1MS  18MS)
*.......................................................
*        .......  Phase Voltage VCN  .......
VCN  19  0  SIN(0  110  55.555   0.012)
R3   19  20  1UOhm
*   ... The magnetic specification of the transformer ...
*        ......  PRIMARY  ......
L7  20  0  0.5MH
```

```
*          .....  SECONDARY  .......
L8  21  27  0.5MH
L9  27  0   0.5MH
*         .....  MAGNETIC COUPLING  .....
KALLC   L7  L8  L9  0.9999
* ...................................................
X9     21    22    23    SCRM
X10    23    24    21    SCRM
X11    27    25    23    SCRM
X12    23    26    27    SCRM
* .......................................................
RC    23   0   100Ohm
VG9    22   23   PULSE(0   5   15MS    .5US   .5US   1MS   18MS)
VG10   24   21   PULSE(0   5   24MS    .5US   .5US   1MS   18MS)
VG11   25   23   PULSE(0   5   12MS    .5US   .5US   1MS   18MS)
VG12   26   27   PULSE(0   5   21MS    .5US   .5US   1MS   18MS)
*.........................................................
.TRAN  0.1MS  36MS 18MS 1MS
.OP
.OPTIONS  NOMOD NOPAGE RELTOL=0.2 VNTOL=5MV ITL4=100
 ITL5=20000
.PROBE
.END
```

```
* .... PSPICE Source File for a Three-Phase Tab Changer
*        Transformer Circuit with Inductive Load ....
* .....................................................
*       ........  SCR SUBCIRCUIT   ........
.SUBCKT  SCRM  3  2  1
RGATE  2  5  750
VGS  5  1  0
SSCR  3  4  6  1  SSCR
CSWITCH  3  4  450PF
VAS  4  9  0
DT   9  1  DIODE
.MODEL  SSCR  VSWITCH(RON=0.0125  ROFF=103000  VON=1
VOFF=0)
.MODEL DIODE  D
FSENSE  1  6  POLY(2)  VGS  VAS  0  50  11
RSENSE  6  1  1
CR  6  1  .1UF
.ENDS
*         .......  END OF SCR SUBCKT .......
*........................................................
*         .......  Phase Voltage VAN  .......
VAN  1  0  SIN(0  110  55.555 )
R1   1  2  1UOhm
*   ... The magnetic specification of the transformer ...
```

```
*          ......  PRIMARY  ......
L1  2  0  0.5MH
*           .....  SECONDARY  .......
L2  3  9  0.5MH
L3  9  0  0.5MH
*          .....  MAGNETIC COUPLING  .....
KALLA   L1  L2  L3  0.9999
* ..................................................
X1   3   4   5   SCRM
X2   5   6   3   SCRM
X3   9   7   5   SCRM
X4   5   8   9   SCRM
* ......................................................
RA   5   30  100Ohm
LA   30  0   50mH
DA   0   30  DIODE
VG1  4  5  PULSE(0  5  21MS   .5US .5US  1MS  18MS)
VG2  6  3  PULSE(0  5  30MS   .5US .5US  1MS  18MS)
VG3  7  5  PULSE(0  5  18MS   .5US .5US  1MS  18MS)
VG4  8  9  PULSE(0  5  27MS   .5US .5US  1MS  18MS)
*.......................................................
*          .......  Phase Voltage VBN  .......
VBN  10  0  SIN(0  110  55.555   0.006)
R2   10  11  1UOhm
```

```
*   ... The magnetic specification of the transformer ...
*          ......   PRIMARY   ......
L4  11  0  0.5MH
*           .....   SECONDARY  .......
L5  12  18  0.5MH
L6  18  0   0.5MH
*         .....  MAGNETIC COUPLING  .....
KALLB   L4  L5  L6  0.9999
* ..................................................
X5   12   13   14   SCRM
X6   14   15   12   SCRM
X7   18   16   14   SCRM
X8   14   17   18   SCRM
* ......................................................
RB   14  31  100Ohm
LB   31  0   50mH
DA   0   31  DIODE
VG5  13  14  PULSE(0  5  9MS   .5US .5US 1MS  18MS)
VG6  15  12  PULSE(0  5  18MS  .5US .5US 1MS  18MS)
VG7  16  14  PULSE(0  5  6MS   .5US .5US 1MS  18MS)
VG8  17  18  PULSE(0  5  15MS  .5US .5US 1MS  18MS)
*.......................................................
*          .......  Phase Voltage VCN  .......
VCN  19  0  SIN(0  110  55.555   0.012)
```

```
R3    19  20  1UOhm
*   ... The magnetic specification of the transformer ...
*          ......   PRIMARY   ......
L7   20  0  0.5MH
*            .....   SECONDARY  .......
L8   21  27  0.5MH
L9   27  0   0.5MH
*         .....  MAGNETIC COUPLING  .....
KALLC   L7  L8  L9  0.9999
* ...................................................
X9     21    22    23    SCRM
X10    23    24    21    SCRM
X11    27    25    23    SCRM
X12    23    26    27    SCRM
* ..........................................................
RC    23   32   100Ohm
LC    32   0    50mH
DC    0    32   DIODE
VG9    22   23   PULSE(0   5   15MS   .5US   .5US   1MS   18MS)
VG10   24   21   PULSE(0   5   24MS   .5US   .5US   1MS   18MS)
VG11   25   23   PULSE(0   5   12MS   .5US   .5US   1MS   18MS)
VG12   26   27   PULSE(0   5   21MS   .5US   .5US   1MS   18MS)
*..........................................................
.MODEL DIODE D
```

```
.TRAN  0.1MS  36MS 18MS 1MS
.OP
.OPTIONS  NOMOD NOPAGE RELTOL=0.2 VNTOL=5MV ITL4=100
 ITL5=20000
.PROBE
.END
```

APPENDIX B

AC VOLTAGE CONTROLLER CIRCUIT BY (LH)

Fig. B-1 shows the circuit diagram of the ac voltage controller utilized in the thesis as shown in LEYBOLD DIDACTIC GMBH (LH) manual [28].

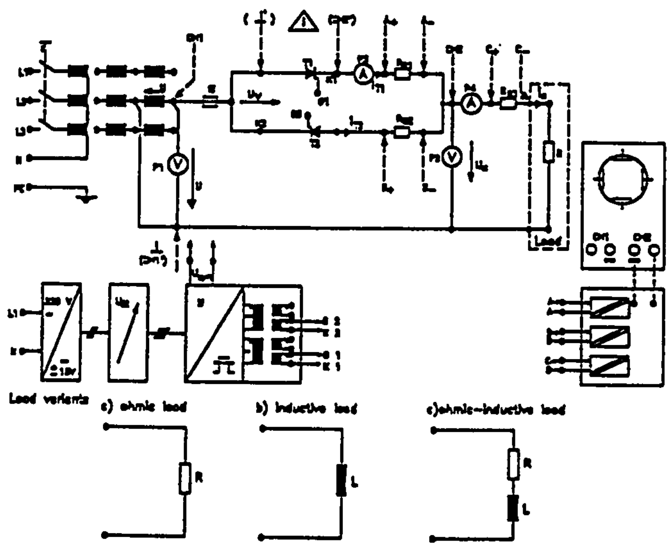


Fig. B-1 Circuit Diagram of the AC Controller

Fig. B-2 shows the waveform of the input source and Fig. B-3 shows the train of pulses provided by the Two-Pulse control unit

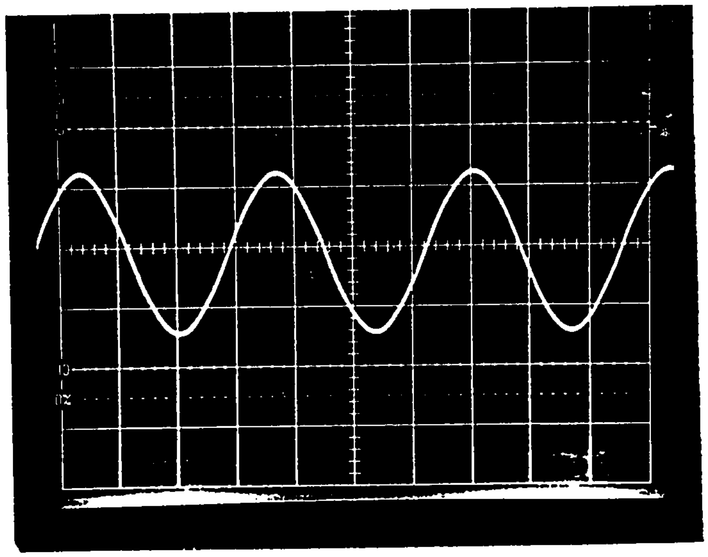


Fig. B-2 Input Source

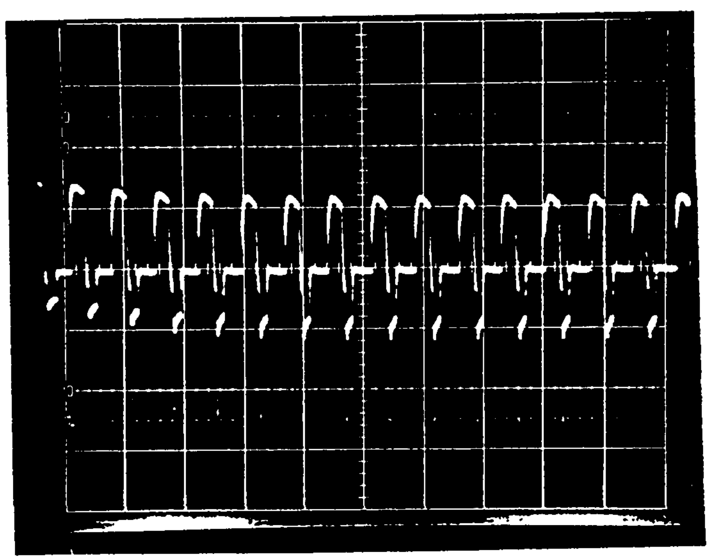


Fig. B-3 Train of Pulses from Control Unit

APPENDIX C

SOURCE CODE OF THE PROGRAM DEVELOPED TO CARRY OUT THE DIGITAL CONTROL FUNCTIONS OF THE PROPOSED CONTROLLER

The following is the source code of the assembly program developed to test the operation of the proposed controller.

```
ADR2    EQU     $1032           ..Setup Portion..
ADCTL   EQU     $1030           Declaration of variables
OPTION  EQU     $1039           used in the program.
        ORG     $C000
        LDAA    #$80
        STAA    OPTION
        LDAA    #$FF
DELAY   DECA
        BNE     DELAY
START   LDAA    #$00            Initialization of the
        STAA    $C400           memory locations where
        STAA    $C760           the calculated output
```

```
        LDD     #$0000          voltage will be stored
        STD     $C401           ($C400-$C402)
        LDX     #$C200
        LDY     #$C200

RET1    LDAA    #$11              ..A/D Programming..
        STAA    ADCTL           The A/D programming is
LOOP1   LDAA    ADCTL           done in such away that,
        ROLA                    a half period will be
        BCC     LOOP1           captured. A zero ($80)
        LDAA    ADR2            will be searched for,
        CMPA    #$80            initially. Then, after a
        BHS     RET1            zero is found the results
RET2    INY                     of the ADC will be stored
        CPY     #$C3ff          starting from $C200 until
        BNE     RIGHT           the next zero ($80) is
        BRA     CHECK           found which indicates the
RIGHT   LDAA    #$11            end of the half cycle.
        STAA    ADCTL
LOOP2   LDAA    ADCTL
        ROLA
        BCC     LOOP2
        LDAA    ADR2
```

```
        CMPA    #$80
        BLS     RET2
        BRA     JMP1
RET3    INX
JMP1    STAA    $0,X
        LDAA    #$11
        STAA    ADCTL
LOOP3   LDAA    ADCTL
        ROLA
        BCC     LOOP3
        LDAA    ADR2
        CMPA    #$80
        BHS     RET3

        LDD     #$0,X       #$C200 is subtracted from
        SUBD    #$C200      The contents of register X,
        STD     $C700       to get the number of
        LDAA    #$00        samples stored. The number
        STAA    $0,X        of samples is stored in
        JSR     Vrms        ($C700-$C701).
CHECK   JSR     COMPAR
        BRA     START
```

```
Vrms    LDX   $C700
        LDY   #$C200
        LDAA  $0,Y
RETURN  LDAB  $0,Y
        MUL
        JSR   DIVID1
        ADDD  $C401
        BCC   JMP2
        STD   $C401
        LDAA  $C400
        INCA
        STAA  $C400
        BRA   JMP3
JMP2    STD   $C401
JMP3    INY
        LDAA  $0,Y
        CMPA  #$00
        BNE   RETURN
        JSR   DIVID2
        RTS
```

..Vrms Subroutine..

The calculation of the output voltage is done according to the following equation:

$$V_{out} = SQRT(1/N (\sum_{K=1}^{N} V^2_k))$$

where V_k is output of ADC and N is the number of samples.

```
DIVID1  IDIV                  In this subroutine the
        STX     $C750         division will be carried
        ADDD    $C760         out.
        STD     $C760
        LDD     $C750
        LDX     $C700
        RTS
DIVID2  LDD     $C760         In this subroutine the
        LDX     $C700         sum of the remainders of
        IDIV                  DIVID1 division will be
        STX     $C750         divided by the number of
        LDD     $C750         samples and added to output
        ADDD    $C401         voltage.
        BCC     JMP4
        STD     $C401
        LDAA    $C400
        INCA
        STAA    $C400
        BRA     JMP5
JMP4    STD     $C401
JMP5    RTS
```

```
COMPAR  LDAA   $C400      ..Comparison Subroutine..
        CMPA   $C500      The upper side of the range
        BHI    CHKUP      is stored in ($C600-$C602)
        BLO    MODAD      and the lower is stored in
        LDD    $C401      ($C500-$C502). The actual
        CPD    $C501      output voltage is stored in
        BEQ    CONTIN     ($c400-$C402). The output
        BLO    MODAD      should lie within the
        BHI    CHKUP      range. Therefore, if the
                          output voltage is lower,
CHKUP   LDAA   $C400      one will be added to port
        CMPA   $C600      B ($1004), which is the
        BLO    CONTIN     input to the DAC, and the
        BHI    MODSB      output voltage will be
        LDD    $C401      calculated once more.
        CPD    $C601      Otherwise, if the output
        BLS    CONTIN     voltage is higher, a one
        BHI    MODSB      will be subtracted from
                          port B ($1004) and the
MODAD   LDAA   $1004      output voltage will be
        CMPA   #$FF       calculated once more.
        BEQ    CONTIN     However, if the output
```

```
        ADDA    #$01        voltage lies within the
        STAA    $1004       range, port B ($1004) will
        BRA     CONTIN      not be updated and the
                            output voltage will be
MODSB   LDAA    $1004       calculated once more.
        CMPA    #$80
        BEQ     CONTIN
        SUBA    #$01
        STAA    $1004
CONTIN  RTS

        SWI
        END
```

REFERENCES

1. Canepa, A., Delfino, B., Invernizzi, M., and Pinceti, P., " Voltage Regulation Via Automatic Load Tap Changing Transformers: Evaluation Of Voltage Stability Conditions," Electric Power Systems Research, Volume B, No. 2, pp. 99-107, October 1987.

2. Bird, B. M. and King, K. G., An Introduction To Power Electronics, John Wiley & Sons Ltd 1983.

3. Heck, F. M., "Direct AC Voltage Control," IEEE Tutorial Course, Power Electronics Applications in Power Systems, pp. 16-26, 1978.

4. Dubey, G., Doralda, S., Joshi, A., and Sinba, R. M., Thyristorised Power Controllers, Wiley Eastern Limited, New Delhi, India, 1986.

5. Rashid, Muhammad Harunur, Power Electronics Circuits, Devices, and Applicaations, Prentice-Hall Inc, Englewood Cliff, New Jersy, 1988.

6. Patchett, G. N., Automatic Voltage Regulator and Stabilizers, London, England, Issac Pitman, 1964.

7. Selvakumar, C. R., "Negative-Feedback High-Efficiency AC Voltage Regulator," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-28, NO. 1, pp. 24-27, Feb 1981.

8. Tez, E. S., Clarke, J. and Smith, I. R., "Inverter Regulation by Transformer Tap Changing," IEE Proc., 129, Pt.B, 315-322, 1982.

9. Tez, E. S., "Microprocessor-Based Controller For Tap-Changing Transformers," Control 85,Inter-national Conference, IEE Conference Pub-lication, NO. 252, V. 2, pp. 609-613, 1985.

10. Medanic, Juraj, Ilic-Spong, M., and Christensen, J., "Discrete Models Of Slow Voltage Dyna-mics For Under Load Tap-Changing Trans-former Coordination," IEEE Transactions On Power Systems, Volume PWRS-2, NO. 4, pp. 873-882, November 1987.

11. Hulley, L. N. and Schofield, G. L., "Varying Power Input by Integral Cycle of Thyristors," Contr. Instrum. (UK), Mar 1971.

12. Lingard, B. W., Johnson, E. W., and Shepherd, W., "Analysis of Thyristor-Controlled Single-Phase Loads with Integral Cycle Triggering," Proc. Inst. Elec. Eng. (Corresp.), Vol. 117, NO. 3, Mar 1970.

13. McVey, E. S. and Veber, R. E., "Design Information for a Switched AC Regulator," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-14, NO. 2, pp. 51-56, Dec 1967.

14. Thomson, R., "A Thyristor Alternating-Voltage Regulator," IEEE Trans. Ind. Gen. Appl., Vol.IGA-4, NO. 2, pp. 162-166, Mar/Apr 1968.

15. Servetas, E. C. and Vlachakis A. V., "A New AC Voltage Regulator Using Thyristors," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-28, NO. 2, pp. 140-145, May 1981.

16. Nagle, W. W., "SPICE2: A Computer Program To Simulate Semiconductor Circuits," Electronic Research Laboratory, College of Engineering, University of California, Berkley, CA, Memo NO. ERL-M520, May 1975.

17. Giacoletto, L. J., "SCR Modeling for the SPICE Computer Program," Dept. of Elec. Eng. Internal Memo, Michigan State Univrsity, Jan 1978.

18. Waiman, F. Ki., "A SPICE Model for the SCR," Dept. of Elec. and Computer Science, M.S. Thesis, University of California, Berkley, CA, Dec. 1979.

19. Avant, R. L., Lee, F. C., and Chen D. T., "A Practical SCR Model for Computer Aided Analysis of AC Resonant Charging Circuit," IEEE Transactions on Industrial Electronics, Vol. IE-29, NO. 4, pp. 319-329, Aug 1982.

20. Avant, R. L., Lee, F. C., "A Unified SCR Model for Continuous Tobology CADA," IEEE Transactions on Industrial Electronics, Vol. IE-31, pp.257-268, Nov 1984.

21. Giacoletto, Lawrence J., "Simple SCR and TRIAC PSPICE Computer Models," IEEE Transactions on Industrial Electronics, Vol. 36, NO. 3, pp. 451-455, Aug 1989.

22. Paice, D. A., "Induction Motor Speed Control by Stator Voltage Control," IEEE Trans. on Power Appl. and Syst., Vol PAS-87, No. 2, pp 585-590, Feb. 1968.

23. Nola, F. J., "Motor Power Factor Controller with Reduced Voltage Starter," US Patent No. 310714, Oct. 13, 1981.

24. Mohan, N., "Improvement in Energy Efficiency of Induction Motors by Means of Voltage Controller," IEEE Trans. on Power Appl. and Syst., Vol PAS-99, No. 4, pp 1466-1471, Jul/Aug. 1980.

25. Dewan, S. B. and Straughen, A., Power Semiconductor Circuits, John Wiley & Sons., 1975.

26. MOTOROLA M68HC11 REFERENCE MANUAL.

27. Hill, J. J. and Alderson, W. E., "Design of a Microprocessor-Based Digital Wattmeter," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-28, NO. 3, pp. 180-184, Aug 1981.

28. LEYBOLD DIDACTIC GMBH, TBS 12.2.1, Power Electronics and Drive Technology 3, Contolled Converter Circuits.

29. LEYBOLD DIDACTIC GMBH, TBS 12.2.1, Power Electronics and Drive Technology 1, Description of Training panels and Peripheral Equipment, General Information.

30. Cook, G. H. and Williams, K. T., "Thyristor Assisted On-Load Tap Changer For Transformers," Fourth International Conference On Power Electronics And Variable-Speed Drives, IEEE Conference Publication, No. 324, pp. 127-131, 1990.

31. Lilley, R. A. and Baum, M. M., "Automatic Tap Change Control System For Supergrid Transformers," Second International Conference on Power System Monitoring, IEE Conference Publication, NO. 266, pp. 280-285, 1986.

32. Ohtsuki, Hiroshi, Akihiko Yokoyama, and Yasuji Sekine, "Reverse Action Of On-Load Tap changer in Association With Voltage Collapse," IEEE Transactions On Power Systems, V. 6, NO. 2, pp. 300-306, February 1991.

33. Roberts, M. J., Rochelle, R. W., and McDonald D. W., "SCR-Controlled Digitally Programmable AC Power Supply," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol. IECI-25, NO. 1, pp. 59-61, Feb 1978.