A New Transformation and Design Technique for Switched Capacitator High Pass Ladder Filters

by

Kemal Mehmet Fidanboylu

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

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This thesis, written by **Kemal Mehmet Fidanboylu** under the direction of his Thesis Committee, and approved by all its members, has been presented to and accepted by the Dean, College of Graduate Studies, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

Dean of the Graduate School

Date June 9, 1987

Department Chairman

Thesis-Committee

Chairman

Member

Member

This thesis is dedicated to my wife

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ABSTRACT

A new technique for the design of switched capacitor high-pass ladder filters using the MLDD transformation is proposed. It is shown that by realizing the resistive source termination of the high-pass continuous ladder proto-type filter with a special delay free circuit, a much superior response is obtained. A new transormation named the modified bilinear transformation for the design of switched capacitor high-pass ladder filters is also proposed. Using this transformation and the proposed design tecnique, it is shown that the magnitude response of the switched capacitor high-pass ladder filter approximates the response of the continuous high-pass ladder proto-type much better than the MLDD transformation. However, in some of the applications this is achieved at the cost of a higher order filter. Finally, an interactive package for the design of switched capacitor high-pass Butterworth and Chebychev fiters using the MLDD and the modified bilinear transformations is presented as a bonus.

الخلاصـــة

فى هذا البحث نقترح طريقة جديدة لتصميم مرشح المكشف المفشامن السلمي للامرار الترددات العاليه باستعمـــــال تحويل آل م٠ل٠د٠د٠ وعند استبدال عناية حصاد المقاومـــه فى النموذج الاولي لمرشح امرار الترددات العاليه المستمر بدائرة اعاقة حرة حصلنا على نتائج متقدمه ٠

فى هذا البحث أيضا أستعملت طريقة تحويل جديدة سميت طريقة التحويل الثنائية الخطيه المعدله لتصميم مرشـــح المكشف المفتاحي لامرار الترددات العاليه ٠ وقد كانـــت القيمه المطلقه الناتج عن هذا التحويل أفضل بكثير مـــن استعمال تحويل آل م٠ل٠د٠د٠

أخيرا استعمل الحاسب الآلي لتصميم مرشحات المكشـــف المفتاحي الـ بتردد دث د وتشبثت باستعمال تحويل الـ م٠ل٠د٠د٠ وطريقة التحويل الثنائيه الخطيه المعدلة ٠

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Chapter I

INTRODUCTION

1.1 Historical Background

The realization of passive RLC filters started in the 1920s[18]. Since inductors are physically large, electrically lossy and noisy, and unsuitable for miniaturization, their replacement by active-RC filters began in the mid 1960s[5,20]. The evolution of active-RC filters was mainly due to the development of low-cost high-performance monolithic operational amplifiers. The next step in miniaturization was the realization of fully integrated filters which started in the early 1970s. This technique makes use of metal-oxide-semiconductor(MOS) integrated circuit technology which offers high quality capacitors, low-leakage charge storage and offset-free switches[20]. However, direct integration of an active-RC filter leads to difficulties.

Active-RC filters are mainly used in telecommunication applications which require time constants of the order 0.1 milli-seconds. In integrated circuits, MOS capacitors are usually made smaller than 100pF, because for an oxide thickness of 700 Angstroms, a 1pF capacitor requires about 3 mil-square chip area. With a capacitor of 10pF, a time constant

of the order 0.1 milli-seconds can be accomplished with a resistor of the order 10 Mega-Ohms. Such a resistor made by using a poly-silicon line occupies an area of 1600 mil-square, which is approximately 10 percent of the average chip area of an analog MOS integrated circuit[20]. Therefore, the large chip area required for constructing an integrated resistor is a major difficulty in the direct integration of active-RC filters.

The second major difficulty of MOS resistors is their non-linear characteristics. Furthermore, since both capacitors and resistors have absolute accuracies in the range of 5-10 percent, and their errors are uncorrelated, the overall error of the RC time constant can be as high as 20 percent. This error also depends on the temperature and signal level[20].

1.2 Evolution of Switched-Capacitor Filters

The difficulties in the direct integration of active-RC filters can be overcome by simulated resistors which are obtained by periodical switching of capacitors between two circuit nodes at a sufficiently high rate. The type of filters emerging from this theory are called switched-capacitor(SC) filters which are analog sampled data circuits[23]. The periodic sampling of analog signals have been used for many years. The first known record of sampling analog signals is found on pages 420-425 of "Treatise on Elec-

tricity and Magnetism" by James Clerk Maxwell[1]. The theory of sampling analog signals was further developed in the late 1950s and several schemes that used switches and capacitors to simulate filters were proposed in the 1960s[13,16]. However, the practical realization of integrated circuit switched-capacitor filters was possible only in the late 1970s[5,23] when MOS technology provided high-quality capacitors, offset-free switches, and moderate quality op-amps.

To show that a simulated resistor can be constructed from capacitors and switches, consider the circuit given in Fig. 1.1(a). Without any loss of generality, assume that both switches are open and the capacitor C is initially discharged. It is further assumed that the voltage sources V_1 and V_2 are constant during all or most of the phase period. The clock waveforms used for driving the switches are shown in Fig. 1.2. As it can be observed from these waveforms, the phases ϕ_1 and ϕ_2 are non-overlapping. At $t=(n-3/2)T+t_1$, the clock pulse ϕ_1 is applied to switch 1. This pulse closes switch 1 and causes a charge transfer from the voltage source V_1 to the capacitor. In practice, a finite resistance R is associated with the switch. This resistance which is connected in series with the capacitor prevents the instantaneous charging of the capacitor C. Definitely, the RC time constant must be much smaller than T/2 in order to let the capacitor charge completely to V_1

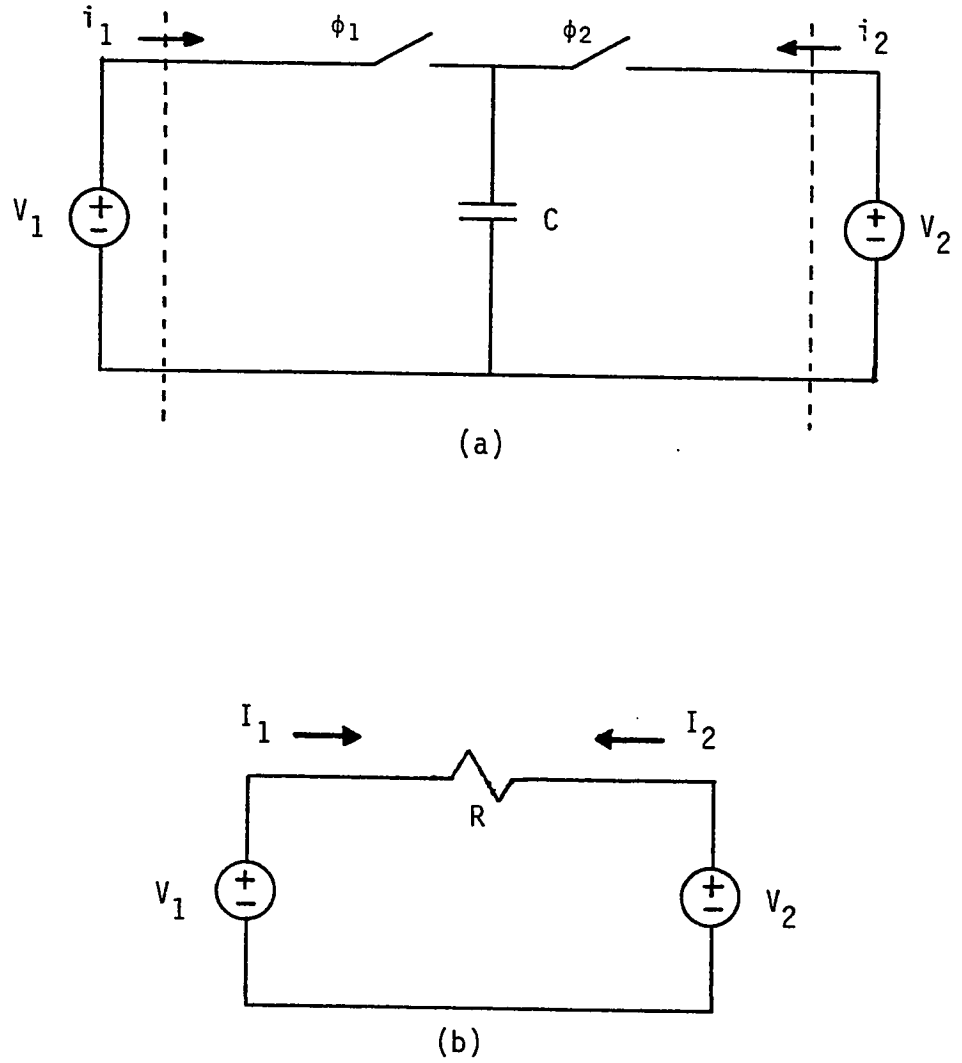


Figure 1.1 (a) Parallel switched capacitor realization of a continuous resistor. (b) Continuous Resistor.

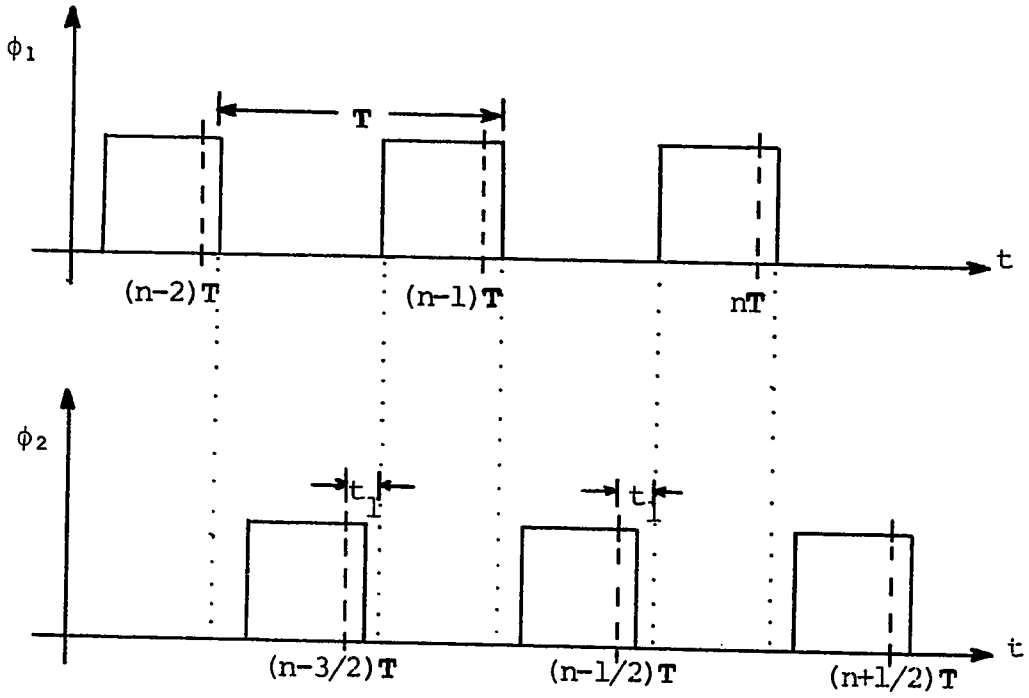


Figure 1.2 Waveform of the two phase non-overlapping clock used in SC filters.

The charge transfered to the capacitor while switch 1 was closed can be written as

$$Q((n-1)T)=CV_1 \tag{1.1}$$

At $t=(n-1)T+t_1$, the clock pulse ϕ_2 is applied to switch 2, while just before this time, due to the non-overlapping characteristics of the clock waveforms, the clock pulse ϕ_1 has already gone to the its low state and switch 1 has opened. During this period, the capacitor is discharged and then charged to V_2, therefore the net charge transfered to the capacitor becomes

$$Q((n-1/2)T)=CV_2-CV_1=C(V_2-V_1) \tag{1.2}$$

At $t=(n-1/2)T+t_1$, the clock pulse ϕ_1 is again applied to switch 1, while just before this time the clock pulse ϕ_2 has gone to its low state. Therefore, the state of the two switches, 1 and 2 in this time interval become closed and open respectively. The capacitor is again discharged and then charged to V_1. The net charge transfered to the capacitor becomes

$$Q(nT)=C(V_1-V_2) \tag{1.3}$$

This sequence of events will continue indefinitely and the net charge transfer for the even and odd phase periods are given by equations (1.2) and (1.3) respectively. To show that the two switches and the capacitor shown in Fig. 1.1(a) simulate the resistor of Fig. 1.1(b), we proceed as follows: First, define the resistance of Fig. 1.1(b) as

$$R = \frac{V_1-V_2}{I_1} = \frac{V_2-V_1}{I_2} \tag{1.4}$$

under the assumption that V_1 and V_2 are constants.

The current flowing in a circuit is defined by

$$i = \frac{dq}{dt} \tag{1.5}$$

Therefore, under the steady state condition, the charge flowing from the left dotted line of Fig. 1.1(a) can be written as

$$Q_1 = \int_{(n-1/2)T+t_1}^{nT+t_1} i_1 \, dt \tag{1.6}$$

But, since switch 1 is open for $(n-1)T+t_1 \leq t < (n-1/2)T+t_1$, then $i_1=0$ during this time interval. Therefore, equation (1.6) can be written as

$$Q_1 = \int_{(n-1)T+t_1}^{nT+t_1} i_1 \, dt \tag{1.7}$$

Since Q_1 given by equation (1.7) is equal to the charge given by Eq. (1.3), we obtain, after equating these two equations and dividing by T

$$\frac{1}{T} Q(nT) = \frac{1}{T} \int_{(n-1)T+t_1}^{nT+t_1} i_1 \, dt = I_1(aver) \tag{1.8}$$

Substituting equation (1.3) into (1.8) gives

$$\frac{V_1-V_2}{I_1(aver)} = \frac{T}{C} \tag{1.9}$$

Comparing Eq. (1.4) and (1.9), the following relationship is obtained

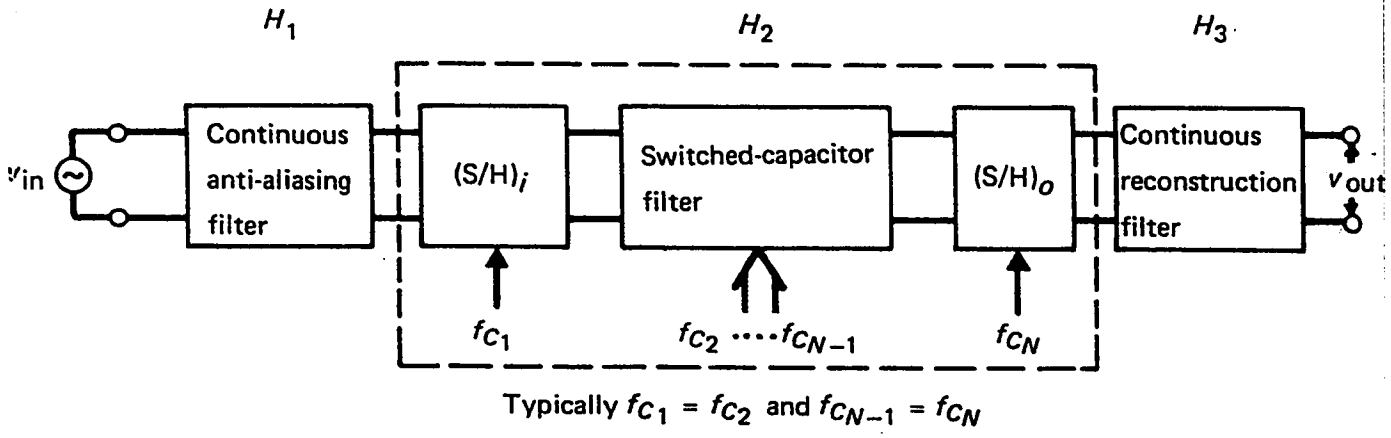
$$R = \frac{T}{C} \tag{1.10}$$

The above relationship is valid when $I_1=I_1(aver)$. This occurs when V_1 and V_2 are constant during the clock period T. Therefore, under the above assumptions, we have shown that a capacitor with two switches driven by two non-overlapping clock pulses simulates a resistor of value T/C[5,23].

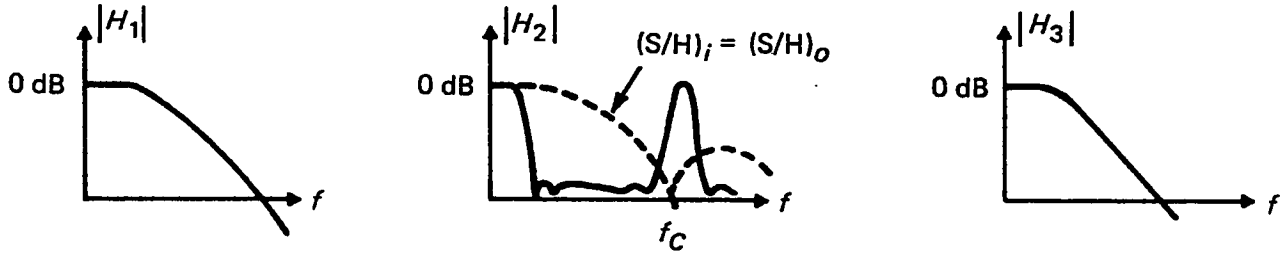
It can be concluded from the above results that an active-RC filter can now be realized by replacing all resistors by equivalent SC branches. A time constant $T_1=R_1C_2$ will be transformed according to equation (1.10) into a new time constant $T_2=TC_2/C_1$. If we let the clock frequency $f_c=1/T$, then this new time constant becomes $T_2=C_2/f_cC_1$, which depends on the ratio of two capacitances and the clock frequency f_c. The clock frequency f_c can be accurately controlled by using a crystal resonator in the clock oscillator and the capacitor ratios can be realized to an accuracy as good as 0.1 percent in MOS technology. Therefore, the new time constant can be made as accurate as 0.1-0.5 percent. Furthermore, the area for resistors is highly reduced by using SC equivalent branches. For a resistor value of R=10 Mega-Ohms, if a 100KHz clock frequency is applied, then equation (1.10) dictates a capacitance value of C=1pF. The new area occupied by this capacitor is about 3 mil-square compared to an area of 1600 mil-square required to construct the above mentioned resistance value. This means that by replacing the above resistance with its equivalent SC branches a reduction in chip area has been accomplished by a factor of 533[20].

1.3 Switched Capacitor Filters as Analog Sampled Data Circuits

As was mentioned earlier, switched capacitor filters are analog sampled data circuits. Due to this property, they are most conveniently analyzed and designed like digital filters, in the z-transform domain. The system given in Fig. 1.3(a) shows the most general form of a switched capacitor network[17]. An analog signal that requires filtering is first passed through a continuous anti-aliasing filter. This is usually a second order low-pass active-RC filter with a sufficiently high cut-off frequency which converts the infinite bandwidth input signal into a band-limited one. The band-limited analog signal is then passed through an input sample-and-hold circuit $(S/H)_i$ and is sampled at intervals of $1/f_{c1}$. The discrete signal coming from the output of the sample-and-hold circuit passes through the desired SC filter. The filtered discrete signal is again passed through an output sample-and-hold circuit $(S/H)_o$ and is resampled at intervals of $1/f_{cN}$. Finally, the desired signal coming from the output of the sample-and-hold circuit passes through a continuous reconstruction filter which converts the sharp transitions in the sampled-data waveform into smooth ones. The typical magnitude responses of the three filters used in an SC network are depicted in Fig. 1.3(b).



(a)



(b)

Figure 1.3 (a)Processing of an analog signal through a switched capacitor filter. (b) Typical magnitude responses

Theoretically, a switched capacitor network can be controlled by multiple clock frequencies. However, usually in practice, two phase clocks are used. In most of the cases, the sample-and-hold operations are inherently performed by the SC filter. When this is so, the SC filter includes the three blocks shown inside the dashed rectangle. Furthermore, if the input or the output of the SC network is interfaced with another digital or sampled-data filter, such as D/A or A/D converters, some of the hardware shown in Fig. 1.3(a) is not necessary. As an example, suppose that the output is interfaced with a digital circuit, then, in such a case, the continuous reconstruction filter is not anymore needed and the sample-and-hold circuit is usually incorporated with the digital circuitry. However, a drawback to this case is the extra requirement of synchronization between the clocks that control the SC filter and those that control the external sampling operations.

Chapter II

SWITCHED CAPACITOR FILTER DESIGN USING RESISTOR SIMULATION

The simplest SC filter design technique is the direct replacement of resistors in an active-RC filter by their SC equivalents. In this technique, the active-RC filter is first designed to meet certain desired specifications. The details of active-RC filter design can be found in references[9,17,24,25,33,38] listed in the bibliography. Once the active-RC filter is designed, each resistor is replaced by an SC equivalent circuit which will be described in the following Sections.

2.1 Parallel SC Resistor Simulation

2.1.1 Operation and Analyses

It has been shown in Chapter 1 that the switched capacitor shown in Fig. 1.1 simulates a resistor of value $R=1/f_cC$. This configuration is called parallel SC realization of a resistance. Before proceeding into further design details, consider the active-RC integrator shown in Fig. 2.1. It is a known fact that the circuit shown in Fig. 2.1 is a basic building block of active-RC filters. The input output relation is given by

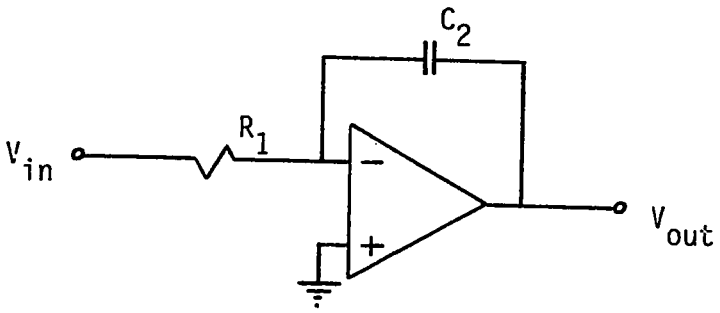


Figure 2.1 Active-RC Integrator.

$$v_{out}(t) = \frac{-1}{R_1 C_2} \int_{-\infty}^{t} v_{in}(\tau)\, d\tau \qquad (2.1)$$

Taking the Laplace transform of both sides of equation (2.1), we obtain

$$V_{out}(s) = \frac{-V_{in}(s)}{sR_1 C_2} \qquad (2.2)$$

The switched capacitor version of the active RC-integrator shown in Fig. 2.1 can be obtained by replacing R_1 by its parallel SC equivalent circuit. The resulting SC integrator circuit is shown in Fig. 2.2. The clock waveforms ϕ_1 and ϕ_2 are shown in Fig. 1.2. The circuits shown in Fig. 2.1 and Fig. 2.2 are equivalent only when the sampling frequency f_c is much higher than the 3-dB frequency of the input signal. Actually, even under these conditions, these two circuits are not exactly equivalent. In order to observe the exact relation between an active-RC integrator and an SC integrator, it is necessary to analyze the SC integrator circuit using sampled data techniques.

Switched capacitor circuits are usually analyzed by making use of the law of conservation of charges rather than Kirchoff's Current Law. This law makes the analysis much easier since charges in an SC network remain finite in contrast to currents which can sometimes be impulses. Furthermore, the charges in an SC network are stored charges and

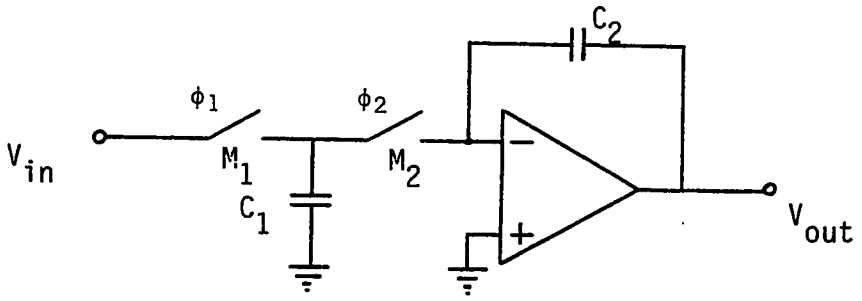


Figure 2.2 Switched Capacitor version of an active-RC integrator using a parallel equivalent branch for resistor simulation.

the storage devices are the plates of a capacitor[36].

The operation of the SC circuit shown in Fig. 2.2 at different clock phases is depicted in Fig. 2.3(a) and Fig. 2.3(b). The description of this operation is given below.
At t=(n-1)T, switch 2 has been closed long enough to charge the capacitor C_1 to a voltage $V_{in}(n-1)$, while switch 2 was open. During this time, the input was isolated from the output and the capacitor C_2 maintains its previous charge.
At $t=(n-1)T+t_1$, the clock pulse ϕ_2 goes to its high state and switch 2 becomes closed while switch 1 has already opened. Therefore, the capacitor C_1 becomes isolated from the input voltage and the charge stored during the previous state is transfered to the capacitor C_2 in the direction as shown in Fig. 2.3(b).
At t=(n-1/2)T, the charge distribution due to one full period is complete and the charge transfer is repeated again for all the other clock periods. To distinguish the charge transfer which takes place when the clock waveform ϕ_1 is high, from the one when the clock waveform ϕ_2 is high, let the clock phase ϕ_1 represent the odd phase and the clock waveform ϕ_2 represent the even phase. Then, the charge associated with the odd phase will be represented by the superscript "o" and the charge associated with the even phase will be represented by the superscript "e" on the voltages

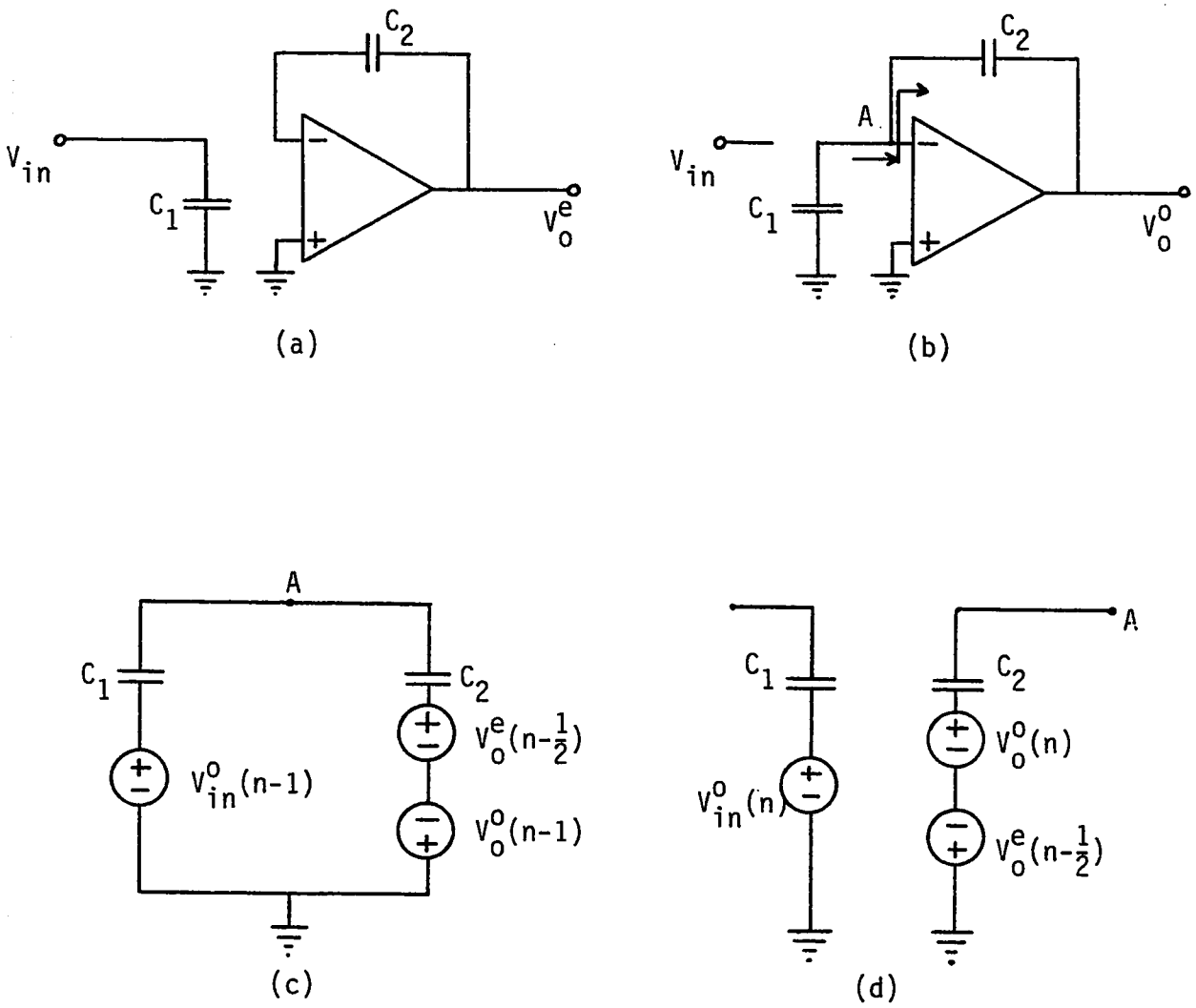


Figure 2.3 Operation of the switched capacitor integrator of Fig. 2.2; (a) during odd phase (b) during even phase (c) Equivalent circuit for the capacitors showing the charge storage at t=(n-1/2)T and (d) at t=nT

characterizing these charges.

The charge stored on a capacitor at any phase can be represented by a voltage source in series with that capacitor, where the polarity of the voltage source represents the polarity of the stored charge. Using this representation, the charge storage on the two capacitors C_1 and C_2 is depicted in Fig. 2.3(c), where the op-amp has been omitted for clarity.

To obtain the difference equation characterizing the operation of the circuit, the conservation of charge law is applied at node A of Fig. 2.3(c). The resulting difference equation is given by

$$C_1 V_{in}^{o}(n-1) + C_2 V_o^{e}(n-1/2) - C_2 V_o^{o}(n-1) = 0 \qquad (2.3)$$

Taking the z-transform of both sides of equation (2.3), we obtain

$$C_1 z^{-1} V_{in}^{o}(z) + C_2 z^{-1/2} V_o^{e}(z) - C_2 z^{-1} V_o^{o}(z) = 0 \qquad (2.4)$$

As was mentioned earlier, during the odd phases, the capacitor C_2 maintains the charge acquired from the previous even phase. Therefore at t=nT, the equivalent circuit showing the charge storage on capacitor C_2 is as shown in Fig. 2.3(d). The conservation of charge law at node A gives

$$C_2 V_o^o(n) - C_2 V_o^e(n-1/2) = 0 \qquad (2.5)$$

taking the z-transform of both sides of equation (2.5) and simplifying, we obtain

$$V_o^o(z) = z^{-1/2} V_o^e(z) \qquad (2.6)$$

Substituting (2.6) into Eq. (2.4) gives

$$C_1 z^{-1} V_{in}^o(z) + C_2 z^{-1/2} V_o^e(z) - C_2 z^{-3/2} V_o^e(z) = 0 \qquad (2.7)$$

The transfer function of the SC circuit shown in Fig. 2.2 is obtained from Eq. (2.7) as

$$H^{oe}(z) = \frac{V_o^e(z)}{V_{in}^o(z)} = -\frac{C_1}{C_2} \frac{z^{-1/2}}{1-z^{-1}} \qquad (2.8)$$

Using (2.6), Eq. (2.8) can also be expressed as

$$H^{oo}(z) = \frac{V_o^o(z)}{V_{in}^o(z)} = -\frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}} \qquad (2.9)$$

The integrator defined by the transfer function given by equation (2.8) has a half delay in the forward path. This transfer function is obtained if the output of the SC cir-

cuit shown in Fig. 2.2 is sampled at the even clock phases. Such an integrator is known as Type I Lossles Discrete Integrator(LDI)[5,6]. The reason that this integrator is called the LDI integrator can be seen as follows:

From Eq. (2.2), the transfer function of the analog integrator can be written as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sR_1C_2} \tag{2.10}$$

For sinusoidal signals, substituting s=jw into the transfer function of the analog integrator, we obtain

$$H(jw) = \frac{V_{out}(jw)}{V_{in}(jw)} = -\frac{1}{jwR_1C_2} \tag{2.11}$$

On the other hand, for discrete frequencies, substituting z=exp(jwT) into Eq. (2.8) gives

$$H^{oe}(e^{jwT}) = -\frac{C_1}{C_2}\left(\frac{e^{-jwT/2}}{1-e^{-jwT}}\right) \tag{2.12}$$

Multiplying the numerator and denominator by exp(jwT) gives

$$H^{oe}(e^{jwT}) = -\frac{C_1}{C_2}\frac{1}{(e^{jwT/2}-e^{-jwT/2})} \tag{2.13}$$

Using Euler's formula in (2.13), the transfer function of the SC integrator becomes

$$H^{oe}(e^{jwT}) = -\frac{C_1}{jwTC_2}\left[\frac{\frac{wT}{2}}{\sin(\frac{wT}{2})}\right] \qquad (2.14)$$

Equation (2.14) gives the exact transfer function of the SC integrator when its output is sampled at the end of even clock phases. For $wT<<1$, $\sin(wT/2)\simeq wT/2$ and Eq. (2.14) can be written as

$$H^{oe}(e^{jwT}) \simeq \frac{-C_1}{jwTC_2} \qquad (2.15)$$

Comparing (2.15) with Eq. (2.11), it can be observed that $R_1=T/C_1=1/f_cC_1$. Therefore, when the sampling frequency is much higher than the frequency of the input signal, the analog integrator is equivalent to a switched capacitor integrator. The error in the magnitude of the SC integrator, which is given by the factor $(wT/2)/\sin(wT/2)$ becomes appreciable when the signal frequency $f>f_c/100$ [20].

Assuming that the signal frequency $f<f_c/100$, then, replacing R_1 by T/C_1 in the transfer function of the analog integrator gives

$$H(s) = -\frac{C_1}{sTC_2} \qquad (2.16)$$

A direct comparison of (2.16) and (2.8) indicates that replacement of all RC integrators by the SC circuit of Fig. 2.2, is equivalent to replacing s by $(1-z^{-1}/Tz^{-1/2})$ provided that the output of the SC circuit is sampled at the end of even phases. This is the well known lossless discrete integrator(LDI)[6] transformation which has found wide application in the design of switched capacitor filters[5,8,12,26,27].

The LDI transformation can also be written as

$$S = \frac{1}{T}(z^{1/2} - z^{-1/2}) \qquad (2.17)$$

The mapping properties and its use in the design of SC filters will be discussed in detail in the next Chapter.

The integrator defined by the transfer function given by Eq. (2.9) has a full delay unit in the forward path. This transfer function is obtained if the output of the SC circuit shown in Fig. 2.2 is sampled at the end of odd clock phases. Such an integrator is known as a Type I Direct Discrete Integrator(DDI)[6]. Following an analysis similar to that for the LDI integrator, the discrete frequency response of Eq. (2.9) can be written as

$$H^{oo}(e^{jwT}) = -\frac{C_1}{C_2}\left[\frac{e^{-jwT}}{1-e^{-jwT}}\right] \qquad (2.18)$$

Using Euler's formula in (2.18), we obtain

$$H^{oo}(e^{jwT}) = \frac{-C_1}{jwTC_2}\left[\frac{\frac{wT}{2}}{\sin(\frac{wT}{2})}\right]\exp(\frac{-jwT}{2}) \qquad (2.19)$$

Equation (2.19) gives the exact transfer function of the SC integrator when its output is sampled at the end of the odd clock phase. The magnitude of Eq. (2.19) can be written as

$$|H^{oo}(e^{jwT})| = \frac{C_1}{wTC_2}\left[\frac{\frac{wT}{2}}{\sin(\frac{wT}{2})}\right] \qquad (2.20)$$

By the same argument given previously, if wT<<1, then the error in the magnitude of the SC integrator is negligible. In order to observe the frequency transformation characterizing the Type I DDI integrator, we proceed as follows: Multiplying the numerator and denominator of Eq. (2.18) by exp(jwT) gives

$$H^{oo}(e^{jwT}) = \frac{-C_1}{C_2}\frac{1}{(e^{jwT}-1)} \qquad (2.21)$$

Since $\exp(jwT)=1+jwT-(wT)^2/2-....$, then, for wT<<1, the terms with second or higher degree can be neglected and Eq. (2.21) becomes

$$H^{oo}(e^{jwT}) \simeq \frac{-C_1}{jwT\,C_2} \qquad (2.22)$$

Comparing (2.22) and (2.11), it can be observed that $R_1=T/C_1=1/f_cC_1$ and the Type I DDI integrator becomes equivalent to the analog integrator. Furthermore, a direct comparison of (2.16) and (2.9) indicates that replacement of all RC integrators by the SC circuit of Fig. 2.2 is equivalent to replacing s by $(1-z^{-1}/Tz^{-1})$ provided that the output is sampled at the end of the odd clock phase. This is the well known forward-difference(or forward Euler) mapping[1,3] used in the design of digital filters from an analog prototype. The phase shift of the LDI integrator discussed previously is $\pi/2$ which is exactly the same as the phase shift of the analog integrator. However, the phase shift of the Type I DDI integrator is given by

$$\text{Arg}\, H^{oo}(e^{jwT}) = \frac{\pi}{2} - \frac{wT}{2} \qquad (2.23)$$

This shows that the Type I DDI integrator has an additional phase lag term of wT/2 radians. This is the major difference between the two SC integrators discussed so far.

2.1.2 Effects of Stray Capacitances

The switched capacitor integrator shown in Fig. 2.2, unfortunately, suffers from a very serious shortcoming, which is the existence of several stray capacitances between various nodes(and lines) and ground. This makes the integrated circuit implementation impractical. The parasitic capacitances due to the switches M_1 and M_2 of the SC integrator shown in Fig. 2.2 is depicted in Fig. 2.4. The most serious problem caused by switches is the clock feed-through, where a portion of the control voltage appears at the Source and Drain terminals of the switch. Since the clock signal is making very large transitions, it can easily couple from the Gate to Source or Drain through C_{GS} or C_{GD}, respectively. The values of C_{GS1}, C_{GD1}, C_{GS2} and C_{GD2} are usually in the range of 0.02pF. Therefore, if the effect of feed-through is not minimized, these capacitances can effect the performance of the SC circuit[7,14]. In general, the clock feed-through is dependent upon the switch configuration and the size of the capacitors in the circuit. The best technique to reduce its effect is to use the largest possible capacitors and to keep the clock swings as small as possible[1,7,14].

A second important non-ideal characteristics of the MOS switches are the parasitic capacitances from the Source to Bulk(substrate) and from the Drain to Bulk, denoted as C_{BS} and C_{BD} respectively. If the parasitic capacitors are

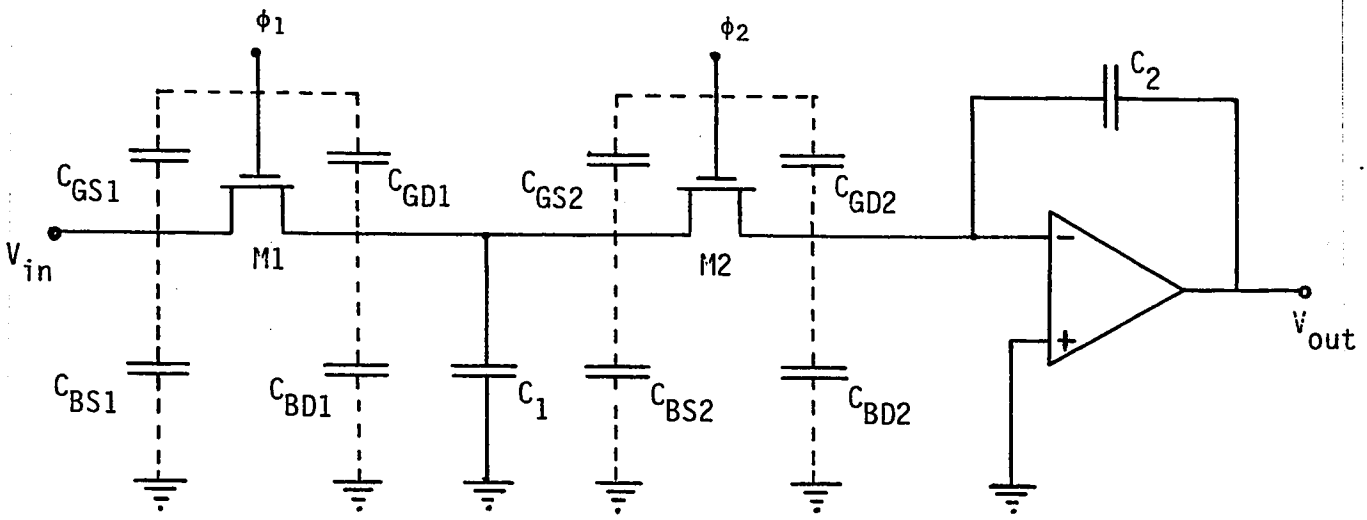


Figure 2.4 Illustration of the parasitic capacitances due to the switches M_1 and M_2 of the SC integrator shown in Fig. 2.2.

connected to a voltage source or to a virtual ground of an op-amp, then they do not affect the performance of the SC circuit[5]. Therefore, the effects of C_{BS1} and C_{BD2}, as shown in Fig. 2.4 are negligible and the only two parasitic capacitances that affect the performance of the SC circuit are C_{BD1} and C_{BS2}. Furthermore, there exist parasitic capacitances from the top and bottom plates of C_1 to the Bulk. However, since the bottom plate of C_1 is connected to the ground, its effect can be eliminated[1]. The parasitic capacitance from the top plate of C_1 to the substrate is in parallel with C_{BD1} and C_{BS2}. These capacitances are combined into a single parasitic capacitance C_p as shown in Fig. 2.5. They can cause serious error, because C_1 is usually small. In addition to this, C_p can sometimes be voltage dependent which can result into non-linear distortion. Suppose that the top plate parasitic is $0.1C_1$ and $C_{BD1}=C_{BS2}=0.1pF$, then an error of 30 percent may be realized if C_1 is designed to be 1pF[1]. Therefore, if a high accuracy is desired for C_1, it must be chosen such that $C_1>5pF$. In general, since $C_2>>C_1$, a large area is required for this SC integrator[20].

The existence of the above parasitic capacitances has caused the development of switched capacitor integrators which are insensitive to parasitic effects[5,23]. The SC

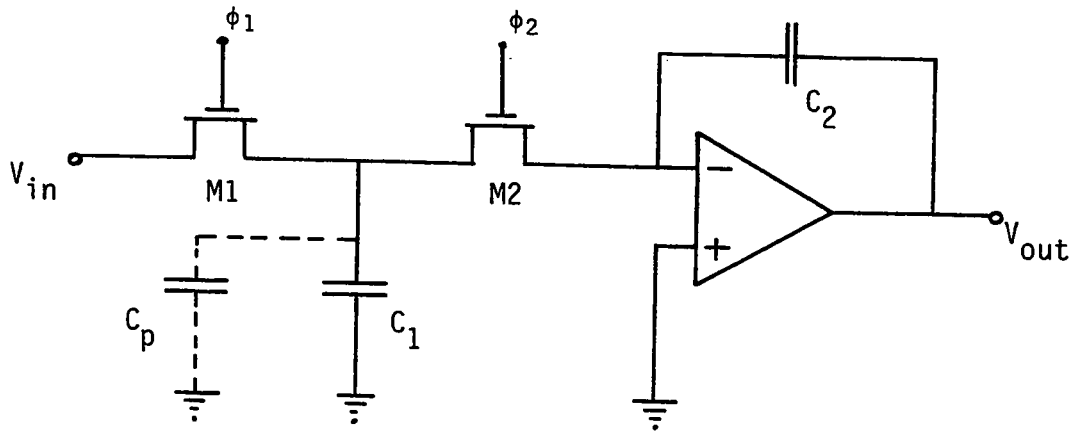


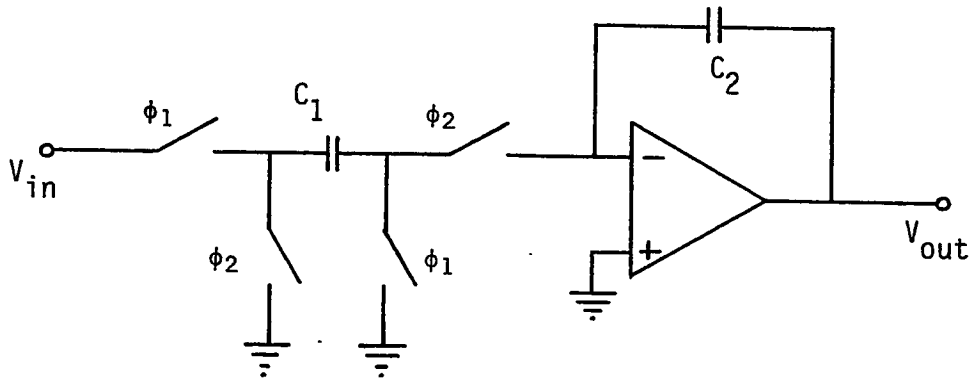
Figure 2.5 Switched Capacitor integrator of Fig. 2.2, showing the combined effect of the parasitic capacitances.

integrator shown in Fig. 2.6(a) is a stray insensitive version of the SC integrator shown in Fig. 2.2. The operation of this stray-free SC integrator is similar to the operation of its stray sensitive version, except for the non-inverting property. Hence the two transfer functions for the stray insensitive integrator can be written as

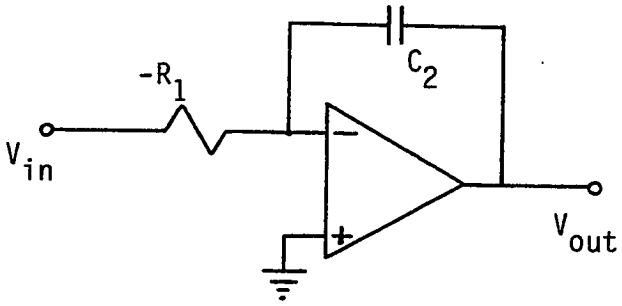
$$H^{oe}(z) = \frac{C_1}{C_2} \frac{z^{-1/2}}{1-z^{-1}} \tag{2.24}$$

$$H^{oo}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}} \tag{2.25}$$

By a similar argument used to derive the relationship between the analog integrator and the stray-sensitive SC integrator, it can be shown that the non-inverting parallel SC branch is equivalent to a negative resistance. Hence, under the assumption that $wT<<1$, the stray-insensitive SC integrator is equivalent to the analog integrator shown in Fig. 2.6(b). Due to this property, the non-inverting parallel SC branch can not be directly used in replacing the resistors in an active-RC filter. However, as it will be shown in the next Chapter, the circuit shown in Fig. 2.6(a) is a very useful building block in the design of SC ladder filters.



(a)



(b)

Figure 2.6 (a) Stray-insensitive SC integrator (b) Analog integrator with negative resistance.

The stray-free property was achieved at the cost of two extra switches. The reason for this insensitivity is due to the following factors:
Every capacitor terminal is either switched between ground and voltage source, which are low impedance nodes or between ground and a virtual ground which are both at the same potential. Hence, they do not affect the performance of the SC integrator[20].

Furthermore, in the case of stray-insensitive SC integrator, the capacitors C_1 and C_2 need not be much larger than the parasitic capacitances. However, they should still be much larger than the capacitance between the lines leading to their electrodes which varies between 1-5 fF (1 fF=10^{-15}F). This allows C_1 to be chosen as small as 0.1pF which leads to a reduction of 10-50 in size with comparison to the stray-sensitive integrators. In addition to this, the accuracy is highly improved and the errors can be reduced to 0.1-0.5 percent[20].

2.1.3 Design Example

The concept of parallel SC resistor simulation to design SC filters from active-RC prototypes will be demonstrated by an example. The interested reader may refer to reference [1] for further details.

Example 2.1

Consider the Tow-Thomas three op-amp biquad shown in Fig. 2.7.

This circuit has both low-pass and band-pass transfer functions simultaneously available at V_1 and V_2, respectively. The transfer functions in the continuous domain are given by[17]

$$H_{LP}(s) = \frac{V_1}{V_{in}} = \frac{-(r_2/r_1)\dfrac{1}{R_4 R_2 C_5 C_6}}{s^2 + \dfrac{1}{R_1 C_5}s + \dfrac{r_2}{r_1}\dfrac{1}{R_2 R_3 C_5 C_6}} \tag{2.26}$$

and

$$H_{BP}(s) = \frac{V_2}{V_{in}} = \frac{-\dfrac{1}{R_4 C_5}s}{s^2 + \dfrac{1}{R_1 C_5}s + \dfrac{r_2}{r_1}\dfrac{1}{R_2 R_3 C_5 C_6}} \tag{2.27}$$

The ideal design equations for this network are

$$R_2 = \frac{r_2}{r_1}\frac{1}{w_o^2 R_3 C_5 C_6} \tag{2.28}$$

$$R_1 = \frac{Q}{w_o C_5} \tag{2.29}$$

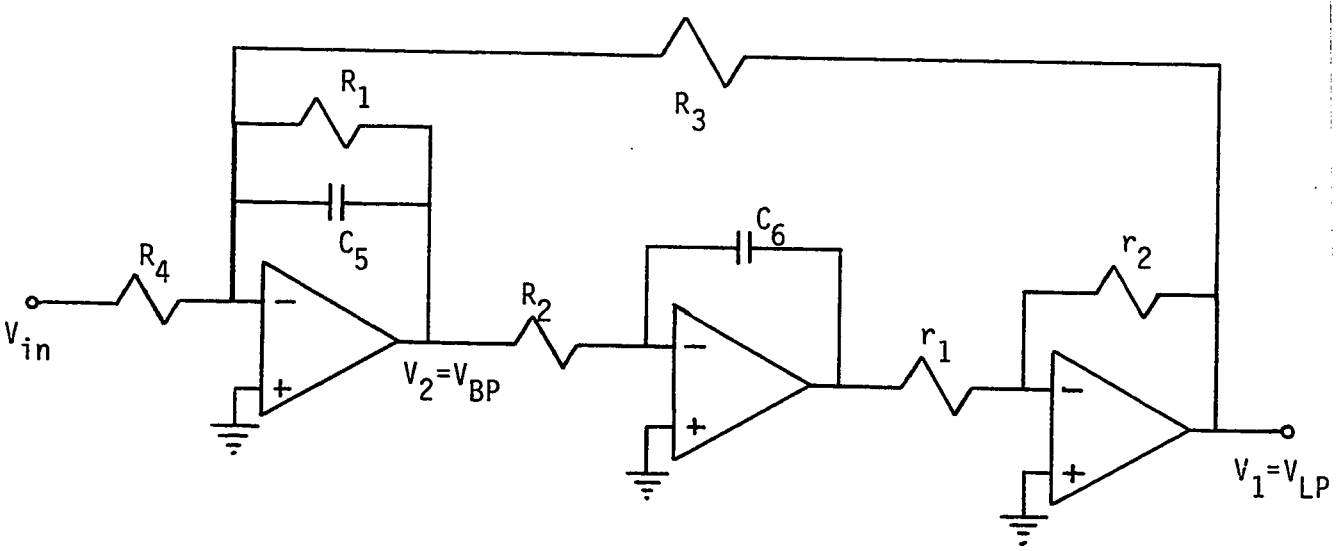


Figure 2.7 The Tow-Thomas circuit.

$$R_4 = \frac{r_1}{r_2}\frac{w_o^2 R_3}{b_o} \quad \text{for } H_{LP} \tag{2.30}$$

or

$$R_4 = \frac{1}{b_1 C_5} \quad \text{for } H_{BP} \tag{2.31}$$

where b_o and b_1 are the gain constants of the low-pass and band-pass filters respectively.

Suppose that we wish to design a switched capacitor low-pass filter using the Tow-Thomas circuit for a given filter specifications. First, we design the normalized filter and then perform the necessary magnitude and frequency scaling to meet the required specifications. This makes the design more general.

For a normalized low-pass filter with w_o=1 rad/sec, assume that r_2=r_1=1 Ohm, C_5=C_6=1 F and R_3=1 Ohm. Computing R_2 and R_1 using equations (2.28) and (2.29), we obtain; R_2=1 Ohm and R_1=Q Ohms. Furthermore, assuming a maximum gain of 1, then, b_o=w_o^2 and R_4 is computed from Eq. (2.30) as 1 Ohm.

Now, suppose that the given specifications require a low-pass SC filter with w_o=1000 rad/sec, Q=5 and a maximum gain of 1.

In this design technique of SC filters, it is not necessary to perform magnitude scaling since all the resistors are replaced by SC equivalent branches and all the capacitances are usually normalized with respect to the smallest capacitance of the circuit. This smallest capacitance is usually named as the unit capacitance C_u which ranges between 0.5pF and 2pF, depending on the technology used. To replace the resistors by their equivalent branches, we have to calculate the capacitance associated with each branch using Eq. (1.10). Furthermore, we have to choose the sampling frequency such that wT<<1.

Choice of f_c=100 KHz guarantees that wT<<1. Next, applying a frequency scaling of k_f=1000 to the capacitances C_5 and C_6 gives

$$C_5=C_6=1/1000 \text{ F}$$

The capacitances associated with each SC equivalent branch are calculated as

$$C_1=(1/R_1 f_c)=1/500{,}000 \text{ F}$$

$$C_2=(1/R_2 f_c)=1/100{,}000 \text{ F}$$

$$C_3=(1/R_3 f_c)=1/100{,}000 \text{ F}$$

$$C_4=(1/R_4 f_c)=1/100{,}000 \text{ F}$$

Since the minimum capacitance is C_1, then all the capacitance values are normalized with respect to C_1. This gives the following normalized capacitance values

$C_1=C_u$

$C_2=5C_u$

$C_3=5C_u$

$C_4=5C_u$

$C_5=500C_u$

$C_6=500C_u$

The switched capacitor realization of the Tow-Thomas circuit is shown in Fig. 2.8. It should be noted that the last op-amp section of the Tow-Thomas circuit behaves as an inverting amplifier. One of the advantages of SC filters in comparison to active-RC filters is the ability to invert a signal without requiring additional amplifiers. For the Tow-Thomas circuit, this inversion was accomplished simply by replacing the summing resistor with a non-inverting parallel SC equivalent branch. The exact transfer functions of this SC filter are found by applying the law of conservation of charges as[1]

$$H(z)=\frac{V_{LP}}{V_{in}}=\frac{-A_1A_2z^{-2}}{1-(2-A_3)z^{-1}+(1+A_1A_2-A_3)z^{-2}} \qquad (2.32)$$

$$H(z)=\frac{V_{BP}}{V_{in}}=\frac{-A_2z^{-1}(1-z^{-1})}{1-(2-A_3)z^{-1}+(1+A_1A_2-A_3)z^{-2}} \qquad (2.33)$$

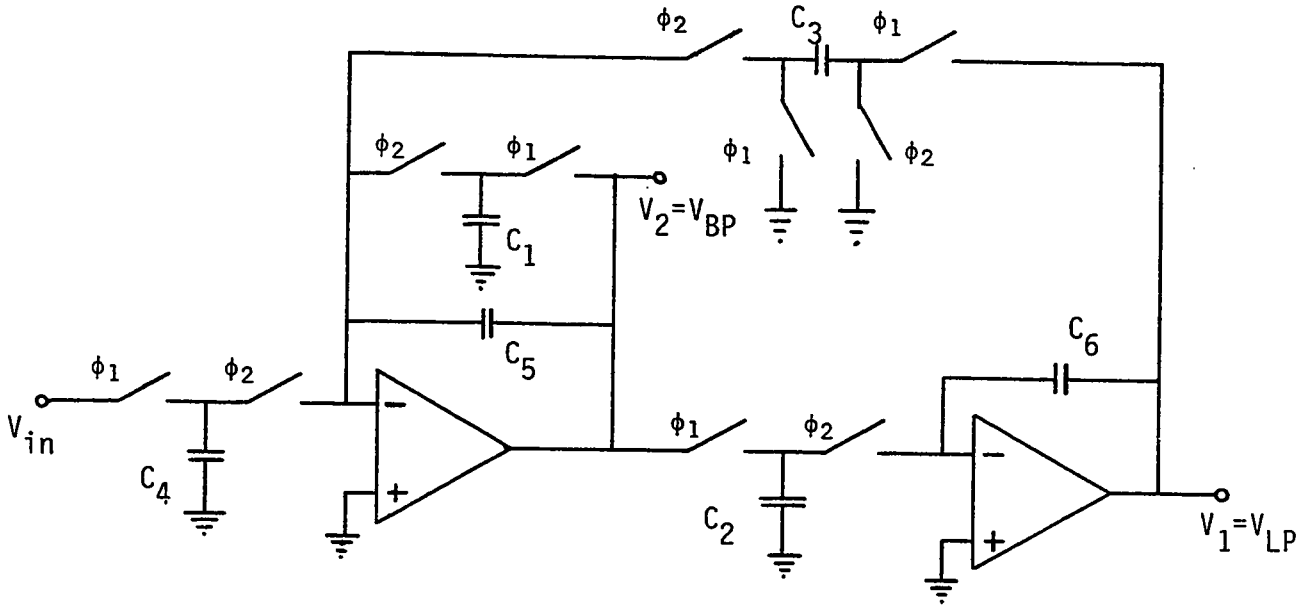


Figure 2.8 Switched Capacitor realization of the Tow-Thomas circuit using parallel SC equivalent branches.

where $A=C_4/C_5, A_1=C_4/C_3, A_2=C_2/C_6$ and $A_3=C_4/C_1$

2.2 Series SC Resistor Simulation

2.2.1 Operation and Analyses

A second type of SC integrator which is commonly used as a building block in the design of SC filters makes use of a series SC equivalent branch to simulate a resistor. This circuit is shown in Fig. 2.9. The clock waveforms used for driving the switches are shown in Fig. 1.2. Using the conservation of charge analysis as explained in Section 2.1.1, the operation of this circuit is analyzed as follows:

At $t=(n-3/2)T+t_1$, ϕ_1 goes high and switch S1 is closed, while just before this time, switch S2 has already opened. During this time, C_1 charges to the instantaneous value of $V_{in}(n-1)$. A current flows through C_2 in the direction as indicated in Fig. 2.10(a). This implies that the charge on C_2 changes by an amount equal to the charge deposited on C_1.

At $t=(n-1)T+t_1$, ϕ_2 goes high. This makes a short circuit across the terminals of C_1 which will be discharged completely. Since switch S1 is closed during this time, C_2 maintains the charge acquired from the previous state.

At $t=(n-1/2)T$, the charge distribution due to one full period is complete and the charge transfer repeats in a similar fashion for all the other periods.

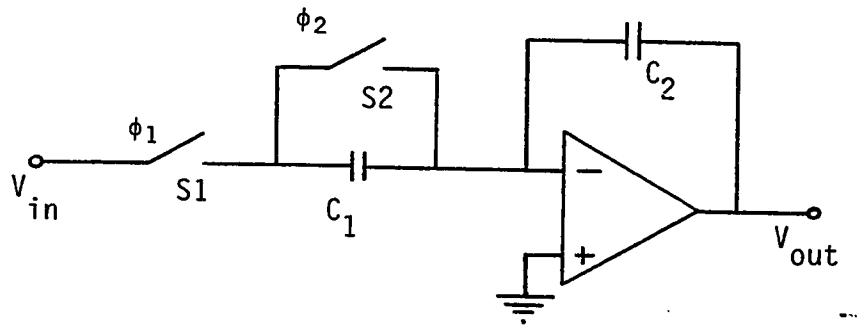


Figure 2.9 Switched Capacitor Integrator using a series equivalent branch for resistor simulation.

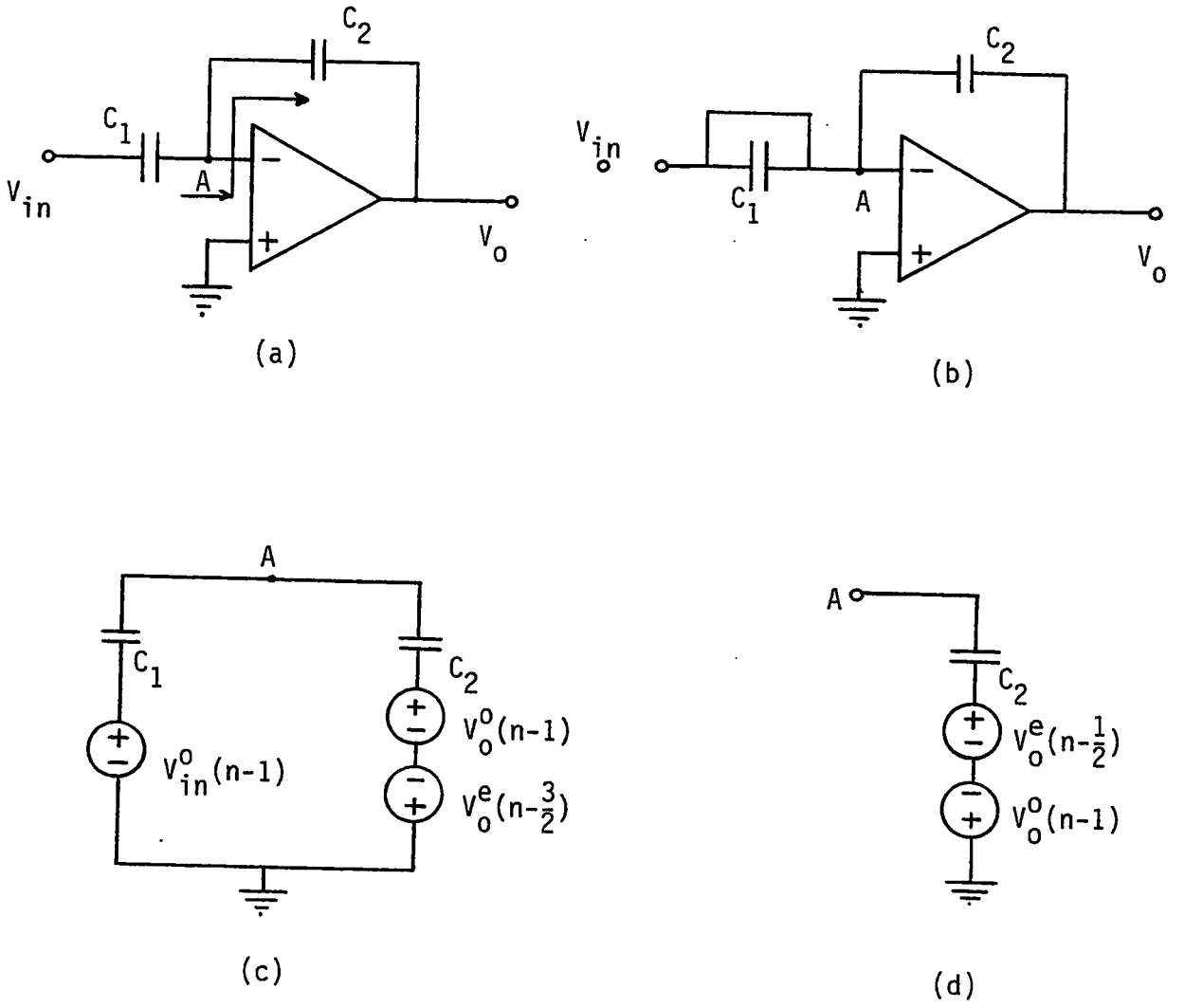


Figure 2.10 Operation of the switched capacitor integrator of Fig. 2.9; (a) during odd phase (b) during even phase (c) Equivalent circuit for the capacitors showing the charge storage at t=(n-1)T and (d) at t=(n-1/2)T

To obtain the difference equation characterizing the performance of this circuit, the conservation of charge law is applied at node A. The equivalent circuit showing the distribution of charges is shown in Fig. 2.10(c) for t=(n-1)T. This difference equation is given by

$$C_1 V_{in}^{o}(n-1) + C_2 V_o^{o}(n-1) - C_2 V_o^{e}(n-3/2) = 0 \qquad (2.34)$$

At t=(n-1/2)T, the conservation of charge law at node A gives

$$C_2 V_o^{e}(n-1/2) - C_2 V_o^{o}(n-1) = 0 \qquad (2.35)$$

The equivalent circuit showing the charge distribution at this instant is shown in Fig. 2.10(d). Taking the z-transform of both sides of equation (2.34), we obtain

$$C_1 z^{-1} V_{in}^{o}(z) + C_2 z^{-1} V_o^{o}(z) - C_2 z^{-3/2} V_o^{e}(z) = 0 \qquad (2.36)$$

Multiplying both sides of equation (2.36) by z gives

$$C_1 V_{in}^{o}(z) + C_2 V_o^{o}(z) - C_2 z^{-1/2} V_o^{e}(z) = 0 \qquad (2.37)$$

Next, taking the z-transform of both sides of Eq. (2.35) and multiplying by $z^{1/2}$, we obtain

$$V_o^e(z) = z^{-1/2} V_o^o(z) \tag{2.38}$$

Using Eq. (2.38) to eliminate $V_o^o(z)$ in Eq. (2.37) gives the following transfer function

$$H^{oe}(z) = \frac{V_o^e(z)}{V_{in}^o(z)} = -\frac{C_1}{C_2} \frac{z^{-1/2}}{1-z^{-1}} \tag{2.39}$$

Moreover, if we use Eq. (2.38) to eliminate $V_o^e(z)$ in Eq. (2.37), the following transfer function is obtained

$$H^{oo}(z) = \frac{V_o^o(z)}{V_{in}^o(z)} = -\frac{C_1}{C_2} \frac{1}{1-z^{-1}} \tag{2.40}$$

The transfer function given by Eq. (2.39) is identical to the one given by Eq. (2.8). Therefore, by the same argument presented in Section 2.1.1, sampling the output of the SC integrator at the end of even clock phases realizes the LDI transformation. This shows that the SC integrator shown in Fig. 2.9 is equivalent, in operation, to the SC integrator shown in Fig. 2.2, provided that their outputs are sampled at the end of even clock phase.

On the other hand, if the output of the SC integrator shown in Fig. 2.9 is sampled at the end of odd clock phase, the transfer function given by Eq. (2.40) is obtained. Com-

paring this transfer function with the one given by Eq. (2.9), it can be observed that no delay exists in the forward path. This type of integrator is called Type II Direct Transform Discrete Integrator(DDI). To observe the characteristics of this integrator, we proceed as follows:
Substituting z=exp(jwT) into Eq. (2.40) gives

$$H^{oo}(e^{jwT}) = -\frac{C_1}{C_2}\,\frac{1}{1-e^{jwT}} \tag{2.41}$$

After multiplying the numerator and denominator by exp(jwT) and simplifying, Eq. (2.41) becomes

$$H^{oo}(e^{jwT}) = \frac{-C_1}{jwT\,C_2}\left[\frac{\frac{wT}{2}}{\sin(\frac{wT}{2})}\right]\exp(jwT/2) \tag{2.42}$$

The phase shift of Type II DDI integrator is given by the following equation

$$\text{Arg}\,H^{oo}(e^{jwT}) = \frac{\pi}{2} + \frac{wT}{2} \tag{2.43}$$

A comparison of (2.42) and (2.19) shows that the magnitude of Type II DDI integrator is the same as the magnitude of Type I DDI integrator. The only difference is the leading phase shift instead of a lagging one.

By Euler's formula, $\exp(-jwT)=1-jwt-(wT)^2/2+\ldots$. For $wT<<1$, the second and higher order terms can be neglected, therefore Eq. (2.41) can be written as

$$H^{oo}(e^{jwT}) \simeq \frac{-C_1}{C_2}\,\frac{1}{jwT} \qquad (2.44)$$

Comparing (2.44) with Eq. (2.11), it is easily observed that $R_1=(T/C_1)=1/f_cC_1$ and the Type II DDI integrator becomes equivalent to the analog integrator as shown in Fig. 2.1. Furthermore, if we compare Eq. (2.44) with Eq. (2.16), we can conclude that, replacement of all RC integrators by the circuit of Fig. 2.9 is equivalent to replace s by $(1-z^{-1}/T)$, provided that the output is sampled at the end of odd clock phase. This is recognized as the backward-difference (backward-Euler) mapping[1,31] used in the design of digital filters from an analog prototype.

Unfortunately, the series equivalent branch used in the SC integrator shown in Fig. 2.9 is stray sensitive due to the reasons explained in Section 2.1.2. The stray insensitive version of this integrator which has been extensively used in the design of SC filters[3,8,12,26,27] is shown in Fig. 2.11. The transfer functions of this integrator are also given by equations (2.39) and (2.40).

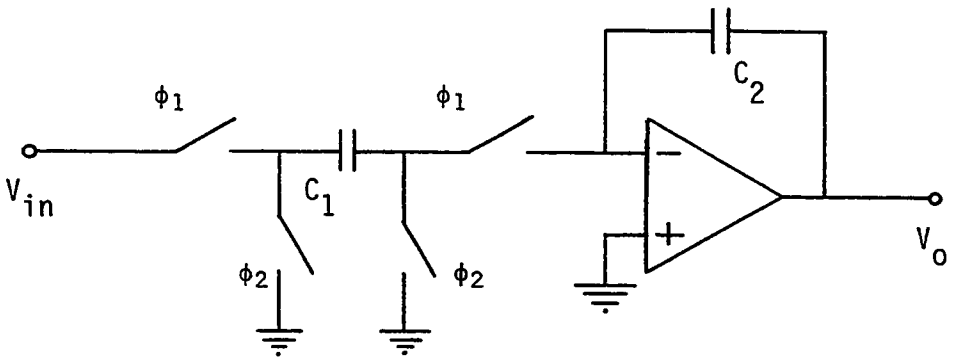


Figure 2.11 Stray-insensitive version of the switched capacitor Integrator shown in Fig. 2.9

2.2.2 Switched Capacitor Filter Design Using Series SC Resistor Simulation

As was mentioned in the previous Section, replacement of resistors in an active-RC filter by series equivalent branches is equivalent to applying the backward-difference mapping to the transfer function of an active-RC filter. This mapping, unlike the forward-difference mapping, transforms a stable RC active filter into a stable SC filter. Assuming that a sample-and-hold circuit $(S/H)_i$ is cascaded with an SC filter as shown in Fig. 1.3, the resulting transfer function denoted by $H_{RE}(w)$ becomes[1]

$$H_{RE}(w) = H(w)\frac{\sin wT}{wT} \tag{2.45}$$

where H(w) is the transfer function of the SC filter obtained from the transfer function of the active RC-prototype by the direct application of the backward transformation and sin(wT)/wT is the spectrum for a zero order sample-and-hold circuit as shown in Fig. 2.12. The design procedure is similar to the one presented in Section 2.1.3. However, as was mentioned earlier, this design is accurate only when wT<<1. When the signal frequency is not much smaller than the sampling frequency, a set of prewarping equations based on a prewarping algorithm can be used to obtain more accurate results. The interested reader is referred to pages 193-194 of reference [1] for further

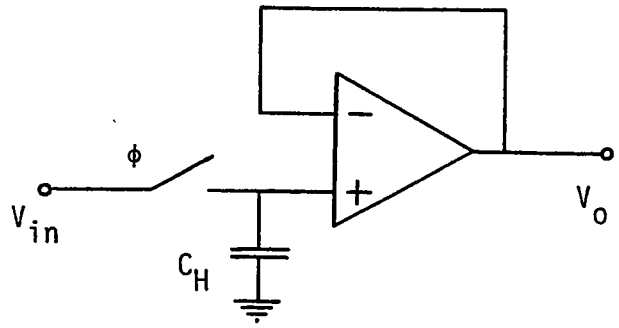


Figure 2.12 A zero-order sample-and-hold circuit.

details. The design of SC filters based on series SC resistor simulation will be demonstrated by an example.

Example 2.2

Consider the Delyiannis-Friend bandpass circuit [38] shown in Fig. 2.13

The continuous domain transfer function of this circuit is given by

$$H(s) = \frac{\frac{-1}{R_1 C_4} s}{s^2 + s\left(\frac{1}{R_2 C_3} + \frac{1}{R_2 C_4}\right) + \frac{1}{R_1 R_2 C_3 C_4}} \qquad (2.46)$$

Assuming that $C_3=C_4=C$ the center frequency w_o and the selectivity Q are given by

$$w_o = \frac{1}{C\sqrt{R_1 R_2}} \qquad (2.47)$$

$$Q = \frac{1}{2}\sqrt{\frac{R_2}{R_1}} \qquad (2.48)$$

choosing $R_1=1$ gives the following design equations

$$R_2=4Q^2 \quad , \quad C=\frac{1}{2w_oQ} \qquad (2.49)$$

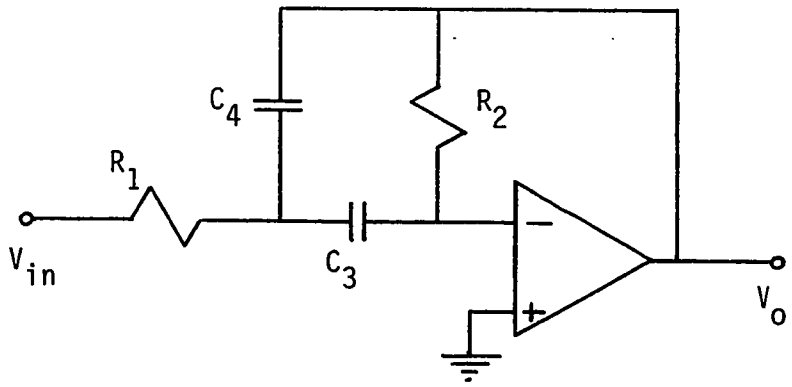


Figure 2.13 Delyiannis-Friend band-pass filter.

Suppose that we are asked to design a bandpass SC filter using series SC equivalent branches with w_o=1000 rad/sec, Q=4 and a sampling frequency of 100 KHz. Using the Delyiannis-Friend circuit as the active RC-prototype, the component values are calculated using equation (2.49) and (1.9) as

$$R_2=4Q^2=64 \text{ Ohms}$$

$$C=C_3=C_4=(1/2w_oQ)=1/8000 \text{ F}$$

By Eq. (1.9), the capacitances associated with each resistor branch are calculated as

$$C_1=(1/R_1f_c)=1/100,000 \text{ F}$$

$$C_2=(1/R_2f_c)=1/64x10^5 \text{ F}$$

Normalizing all capacitances with respect to C_2, we obtain

$$C_1=64C_u$$

$$C_2=C_u$$

$$C=C_3=C_4=800C_u$$

The desired SC filter which is shown in Fig. 2.14 is obtained by replacing R_1 and R_2 with the stray-insensitive series equivalent branches. The transfer function of this SC filter is obtained by using the backward transformation, $s=(1-z^{-1}/T)$ in Eq. (2.46). After simplification, we obtain

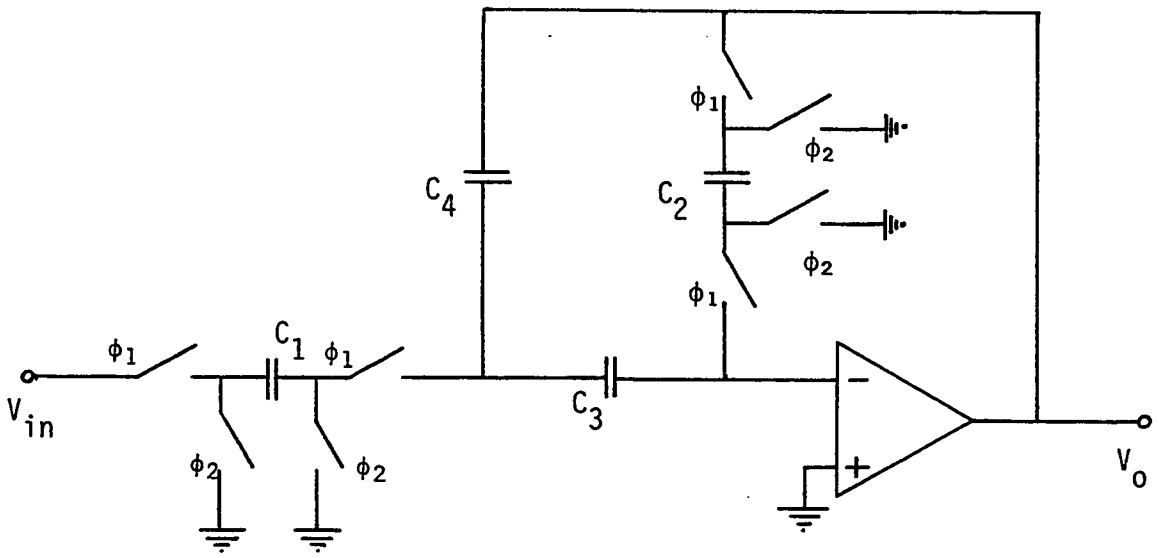


Figure 2.14 Switched capacitor implementation of Fig. 2.13

$$H(z) = \frac{\frac{-T^2}{C_1 C}(1-z^{-1})}{z^{-2} - 2z^{-1}(1+\frac{T^2}{C_2 C}) + (1+\frac{2T^2}{C_2 C} + \frac{T^4}{C_1 C_2 C^2})} \quad (2.50)$$

where $T=1/f_c$. The exact transfer function can be obtained by applying the law of conservation of charges.

2.3 Bilinear SC Resistor simulation

2.3.1 Operation and Analyses

Consider the SC integrator shown in Fig. 2.15(a). With a similar discussion presented in the previous Sections, the circuit is analyzed using the law of conservation of charges. At t=(n-1)T, the conservation of charge law at node A gives

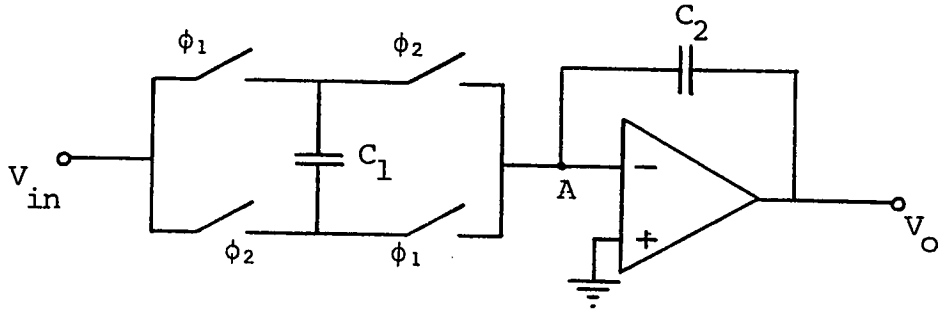
$$C_1 V_{in}^o(n-1) - C_1 V_{in}^e(n-3/2) + C_2 V_o^o(n-1) - C_2 V_o^e(n-3/2) = 0 \quad (2.51)$$

Taking the z-transform of both sides of Eq. (2.51), we obtain

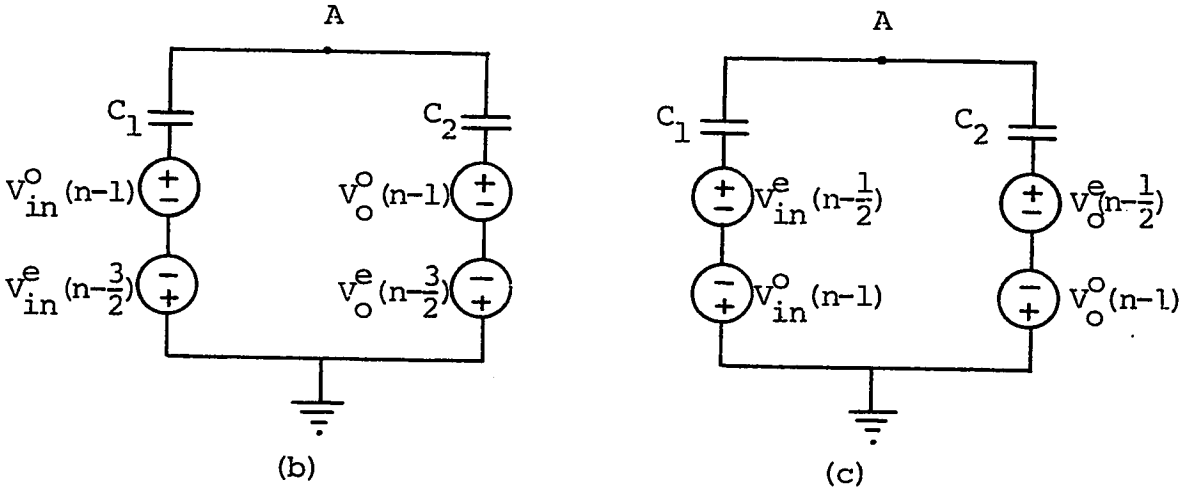
$$C_1 z^{-1} V_{in}^o(z) - C_1 z^{-3/2} V_{in}^e(z) + C_2 z^{-1} V_o^o(z) - C_2 z^{-3/2} V_o^e(z) = 0 \quad (2.52)$$

Multiplying both sides by z gives

$$C_1 V_{in}^o(z) - C_1 z^{-1/2} V_{in}^e(z) + C_2 V_o^o(z) - C_2 z^{-1/2} V_o^e(z) = 0 \quad (2.53)$$



(a)



(b) (c)

Figure 2.15 (a) Bilinear SC integrator (b) Equivalent circuit for the charge distribution at t=(n-1)T (c) Equivalent circuit for the charge distribution at t=(n-1/2)T

At t=(n-1/2)T, the law of conservation of charges at node A yields

$$C_1 V_{in}^e(n-1/2) - C_1 V_{in}^o(n-1) + C_2 V_o^e(n-1/2) - C_2 V_o^o(n-1) = 0 \qquad (2.54)$$

Taking the z-transform of both sides, we obtain

$$C_1 z^{-1/2} V_{in}^e(z) - C_1 z^{-1} V_{in}^o(z) + C_2 z^{-1/2} V_o^e(z) - C_2 z^{-1} V_o^o(z) = 0 \qquad (2.55)$$

Multiplying both sides by $z^{1/2}$ yields

$$C_1 V_{in}^e(z) - C_1 z^{-1/2} V_{in}^o(z) + C_2 V_o^e(z) - C_2 z^{-1/2} V_o^o(z) = 0 \qquad (2.56)$$

The equivalent circuit for the charge distribution at these two phases are shown in Fig. 2.15(b) and 2.15(c) respectively. If the output is sampled at both the even and odd phases, the transfer function of the SC circuit can be obtained by summing equations (2.53) and (2.54) and can be written as

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{V_o^o + V_o^e}{V_{in}^o + V_{in}^e} = -\frac{C_1}{C_2}\,\frac{1+z^{-1/2}}{1-z^{-1/2}} \qquad (2.57)$$

This SC integrator operates somehow different than the SC integrators presented in the previous Sections. The first obvious difference is in the charge transfer of the SC equivalent branch. The capacitor C_1 is discharged and

charged twice at every clock period T. The second obvious difference is in the definition of the transfer function of the circuit. Unlike the previous integrators, the transfer function of this circuit is obtained by sampling the output at both phases. This doubles the effective period. Therefore, in order to establish a basis of comparison, a new period is defined as

$$T_1=\frac{T}{2} \tag{2.58}$$

Defining a new discrete frequency as $z_1=\exp(jwT_1)$, then, from equation (2.58), this new discrete frequency can be written as

$$z_1=z^{1/2} \tag{2.59}$$

Substituting (2.59) into (2.57) gives the following transfer function

$$H(z_1) = \frac{-C_1}{C_2}\,\frac{1+z_1^{-1}}{1-z_1^{-1}} \tag{2.60}$$

Substituting $z_1=\exp(jwT_1)$ into Eq. (2.60), we obtain

$$H(e^{jwT_1}) = \frac{-C_1}{C_2}\left(\frac{1+e^{-jwT_1}}{1-e^{-jwT_1}}\right) \qquad (2.61)$$

Multiplying both sides of Eq. (2.61) by $\exp(jwT_1/2)$ gives

$$H(e^{jwT_1}) = \frac{-C_1}{C_2}\left(\frac{e^{jwT_1/2}+e^{-jwT_1/2}}{e^{jwT_1/2}-e^{-jwT_1/2}}\right) \qquad (2.62)$$

Equation (2.62) can be written as

$$H(e^{jwT_1}) = \frac{-C_1}{jC_2}\,\frac{\cos(wT_1/2)}{\sin(wT_1/2)} \qquad (2.63)$$

For $wT<<1$, $\sin(wT_1/2)\approx wT_1/2$ and $\cos(wT_1/2)\approx 1$. Therefore, Eq. (2.63) becomes

$$H(e^{jwT_1}) \approx \frac{-2C_1}{jwT_1C_2} \qquad (2.64)$$

A direct comparison of Eq. (2.64) and (2.11) shows that the SC integrator shown in Fig. 2.15(a) is approximately equivalent to the active-RC integrator of Fig. 2.1 when $R_1=T_1/2C_1$. Substituting this value of R_1 into Eq. (2.10) gives

$$H(s) = \frac{-2C_1}{sT_1C_2} \qquad (2.65)$$

Comparing Eq. (2.65) with (2.60) shows that replacement of all RC integrators by the SC circuit of Fig. 2.15(a) is equivalent to repalacing s by $2(1-z_1^{-1})/T_1(1+z_1^{-1})$. This is the well known Bilinear Transformation which is very widely used in the design of digital filters from an analog model.

With the information given in Section 2.1.2, it can be shown that the Bilinear SC equivalent branch shown in Fig. 2.15(a) is stray-sensitive to parasitic effects.

2.3.2 Switched Capacitor Filter Design Using Bilinear Resistor Simulation

The design of SC filters based on the Bilinear SC resistor simulation is similar to the previous design techniques except for a few differences. The Bilinear Transformation transforms stable active-RC filters into stable SC filters. This property is shared with the backward difference transformation. In discrete filter design it is preferable that the transformation used maps the imaginary jw-axis of the s-plane onto the unit circle of the z-plane. This makes sure that the shape of the gain response can be preserved[17,31]. The Bilinear Transformation, unlike the backward difference mapping, satisfies the above property. However, due to the non-linear relationship between the discrete and continuous filter frequencies introduced by the Bilinear transformation, the SC filter specifications has to be prewarped. For the backward difference transformation, this was not neces-

sary when wT<<1. Details of prewarping for different transformations will be studied in detail in Chapter 3.

A general procedure for the design of SC filters based on an element by element resistor simulation in analog RC filters using the Bilinear transformation is presented below[1].

1. The desired passband and stopband limit frequencies, w_d's of the SC filter are prewarped to obtain the corresponding Ω_a's of the active-RC prototype filter, using the relation

$$\Omega_a = \frac{2}{T} \tan\left(\frac{w_d T}{2}\right) \qquad (2.66)$$

2. The active-RC prototype is designed from the prewarped specifications using Ω_a's.

3. Each resistor R_m in the active RC circuit is replaced by the Bilinear SC equivalent branches, where R_m is given by

$$R_m = \frac{T_1}{2C_m} \qquad (2.67)$$

Since T_1=T/2, where T is the sampling period, R_m becomes

$$R_m = \frac{T}{4C_m} \tag{2.68}$$

For design examples and further details, the reader is referred to reference [1].

Chapter III

SWITCHED CAPACITOR LADDER FILTER DESIGN

In the previous Chapter, we have presented the conceptually simplest design technique of SC filters. Unfortunately, for higher order and more complicated filters, some of the required pole-Q's are usually very high and the element value sensitivities of the corresponding section become too high for reliable fabrication. This leads to a very low yield and the circuit becomes uneconomical for fabrication[20].

The most widely used SC filter design is based on the signal-flow-graph(SFG) representation of the current-voltage relations of a passive ladder prototype filter. The prototype filter used is usually a doubly-terminated LC ladder network that is designed to effect maximum power transfer from source to load over the filter passband. These filters have very low sensitivities to variations in their component values. It has been shown [5,23] that this low sensitivity is preserved in the switched capacitor filters whose design are based on the SFG representation of these ladder prototype filters.

In this design technique, the SC filter is obtained by replacing each reactive component of the SFG by SC building blocks. For the low-pass and band-pass SC ladder filters, the building blocks used are either LDI or Bilinear SC integrators which have been presented in Chapter 2. Replacing the reactive components by the SC integrator building blocks, actually corresponds to applying the LDI or Bilinear transformation(depending on the type of SC integrator used) to the transfer function of the passive prototype ladder filter[1,5,8,11,12,26,27,28]. Unfortunately, these two transformations can not be directly used to design SC high pass ladder filters[4,21,22,29,34,35]. In the following Sections, we shall present the use of different transformations in the design of SC ladder filters.

3.1 Use of LDI Transformation in the Design of SC Ladder Filters

3.1.1 Properties of LDI transformation

The LDI transformation was introduced in Chapter 2 and is repeated here for convenience

$$s = \frac{1}{T}(z^{1/2} - z^{-1/2}) \tag{3.1}$$

where 1/T is the sampling frequency. This transformation maps part of the imaginary axis ($-2/T<\Omega<2/T$) in the s-plane onto the unit circle in the z-plane. The relationship between the continuous-time frequency Ω and the discrete-

time frequency w can be found by letting $s=\sigma+j\Omega$ and $z=\exp(jwT)$ in Eq. (3.1). This gives

$$\sigma + j\Omega = j\frac{2}{T}\sin\left(\frac{wT}{2}\right) \tag{3.2}$$

Equating the real and imaginary parts yields

$$\sigma = 0 \text{ and } \Omega = \frac{2}{T}\sin\left(\frac{wT}{2}\right) \tag{3.3}$$

Equation (3.3) shows that the continuous time frequencies are not linearly related with discrete frequencies. This property of the LDI transformation requires the SC filter specifications to be "prewarped" according to Eq. (3.3). The warping effect of Eq. (3.3) is shown in Fig. 3.1. On the same graph, the Ω=w curve has been also plotted for comparison. From Fig. 3.1, it can be observed that the effect of warping increases as wT approaches π, because the nonlinearity of the curve increases in this region.

The Lossless Discrete Integrator transfer function is given by[6]

$$H_{LDI}(z) = P\frac{z^{1/2}}{z-1} = P\frac{z^{-1/2}}{1-z^{-1}} \tag{3.4}$$

where P is a constant. It has been shown in Section 2.1.1 that, if the output of the SC integrator shown in Fig. 2.2 is sampled at the end of even clock phase, the transfer

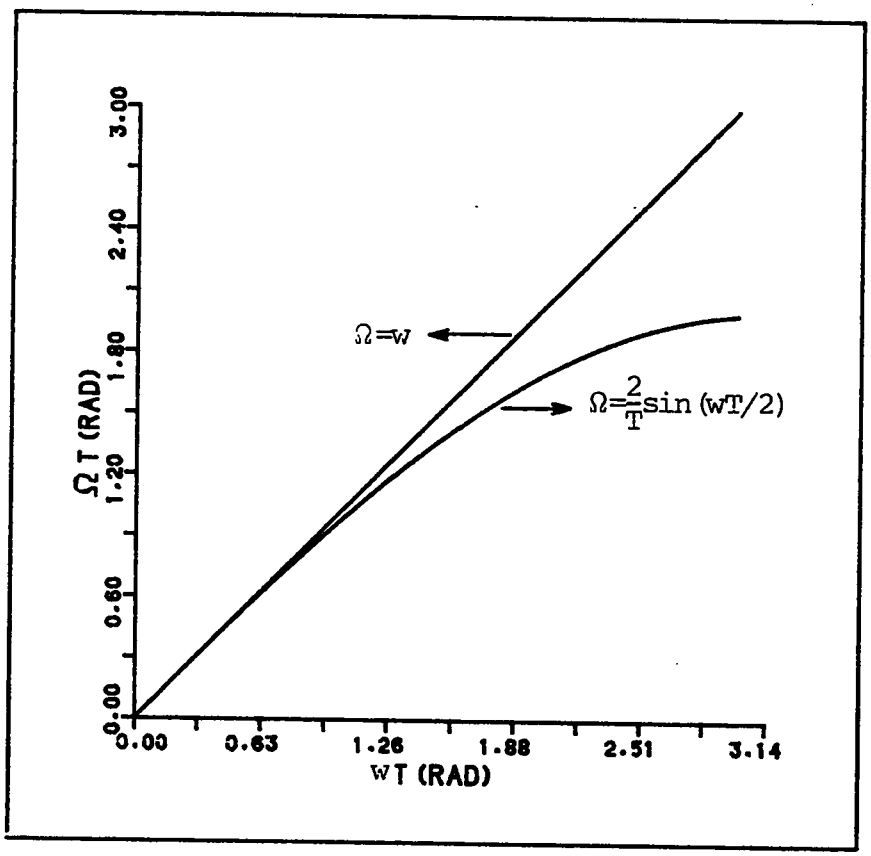


Figure 3.1 Warping effect of the LDI transformation

function becomes identical to the LDI transfer function. However, it has been shown in Section 2.1.2 that this SC integrator is sensitive to parasitic effects. In the same Section a stray-insensitive version of this integrator was also presented. The transfer function of the stray-insensitive integrator which is shown in Fig. 2.6(a) is repeated here for convenience.

$$H^{oe}(z) = \frac{V_o^e(z)}{V_o^o(z)} = \frac{C_1}{C_2}\,\frac{z^{-1/2}}{1-z^{-1}} \tag{3.5}$$

Comparing Eq. (3.4) and (3.5) shows that the two transfer functions become equivalent by choosing P equal to the capacitor ratio C_1/C_2. Therefore, the stray-insensitive SC integrator shown in Fig. 2.6(a) actually realizes the LDI transfer function. The general design of SC ladder filters based on the LDI transformation is studied in the following Section.

3.1.2 Design of SC Ladder Filters Based on the LDI Transformation

3.1.2.1 Low-Pass SC Ladder Filters

The following design procedure for the design of low-pass SC ladder filters has been compiled from various references [1,5,8,11,12,26,27,28] and put into a compact form. Suppose the following SC low-pass filter specifications:

A_{max}: maximum attenuation in the passband region

A_{min}: minimum attenuation in the stopband region

w_p : passband edge frequency

w_s : stopband edge frequency

Step 1

Obtain the low-pass continuous filter specifications Ω_p and Ω_s by prewarping w_p and w_s according to Eq. (3.3).

Step 2

Transform the low-pass continuous filter specifications into the normalized low-pass continuous filter specifications by using $s=S/\Omega_p$ transformation.

Step 3

Design the low-pass continuous filter by using the transformed specifications in step 2.

Step 4

Apply $S=s/\Omega_p$ transformation to the low-pass continuous filter of step 3 to obtain the denormalized low-pass continuous ladder prototype.

Step 5

Obtain the SFG of the low-pass continuous ladder filter obtained in step 4.

Step 6

Realize the resistive source termination and the reactive components of the SFG using the method explained below.

To demonstrate the above design procedure, suppose that for a given SC low-pass filter specifications, the application of steps 1 through 4 has resulted in a 4'th order all-pole low-pass ladder prototype as shown in Fig. 3.2(a). The reactive components are the shunt capacitors and series inductors. The source termination is the resistive component which is connected at the input port. The load termination is the resistive component located at the output port. There are several techniques to obtain the signal-flow-graph(SFG) of a ladder structure. The interested reader may refer to the references[17,25,33,38] listed in the bibliography. In this thesis, we have used the technique presented in references [17,18], where all series elements or combination of elements are represented by their admittances and all shunt elements or combination of elements are represented by their impedances. The SFG of the 4'th order low-pass doubly terminated ladder filter shown in Fig. 3.2(a) is obtained as follows:

First, the voltage and current relations for the circuit are obtained such that loop and node equations involve only integrations. These relations are shown below.

$$V_s = V_{in} - V_1 \qquad (3.6a)$$

$$I_s = \frac{V_s}{R_s} \tag{3.6b}$$

$$I_1 = I_s - I_2 \tag{3.6c}$$

$$V_1 = \frac{I_1}{sC_{1L}} \tag{3.6d}$$

$$I_2 = \frac{V_2}{sL_{2L}} \tag{3.6e}$$

$$V_2 = V_1 - V_3 \tag{3.6f}$$

$$I_3 = I_2 - I_4 \tag{3.6g}$$

$$V_3 = \frac{I_3}{sC_{3L}} \tag{3.6h}$$

$$I_4 = \frac{V_4}{sL_{4L}} \tag{3.6i}$$

$$V_4 = V_3 - V_5 \tag{3.6j}$$

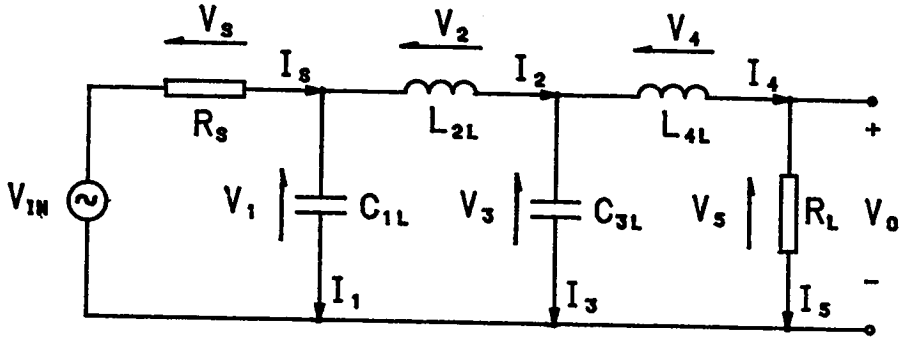
$$V_5 = I_5 R_L \tag{3.6k}$$

$$V_o = V_5 \tag{3.6l}$$

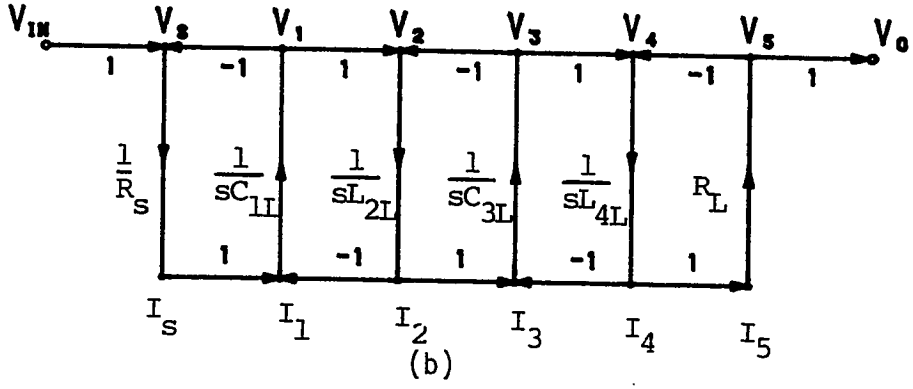
Using the above voltage current relations, the signal-flow-graph is obtained as shown in Fig. 3.2(b). Each node (voltage or current) is defined by the signal paths flowing into it. The factor written next to each arrow is the gain of the path. Each reactive component corresponds to an analog integration. Since the actual implementation will use voltage controlled voltage sources (operational amplifiers) as integrators, it is necessary to transform the current nodes to voltage nodes. This is accomplished by multiplying all cur-

rent nodes by a scaling resistance R so that the currents I_i are now represented as voltages $V_i'=RI_i$. In order to maintain the proper relationships between the voltage and current nodes, the gain factors must also be scaled by a factor of R. The final form of the SFG which is used in the design of SC low-pass ladder filters is shown in Fig. 3.2(c).

The next step in the design is to replace the reactive components of the SFG shown in Fig. 3.2(c) by differential input switched capacitor LDI integrators as shown in Fig. 3.3(a). The realization of the source and load terminations is one of the major difficulties in the design of SC ladder filters. One realization technique is to use series or parallel SC equivalent branches across the feedback of the first and the last SC LDI integrator building blocks[8,12]. Such a building block is shown in Fig. 3.3(b). However, when this is done, the overall transfer function of the SC network becomes different from the transfer function of the low-pass SC ladder filter, which is obtained from a continuous filter prototype by the direct application of the LDI transformation. This variation in the transfer function causes a distortion in the magnitude response of the SC filter. Davis et. al.[12] proposed a solution to the above problem by solving a set of non-linear equations using numerical techniques. However, discussion of these features is beyond the scope of this thesis.



(a)



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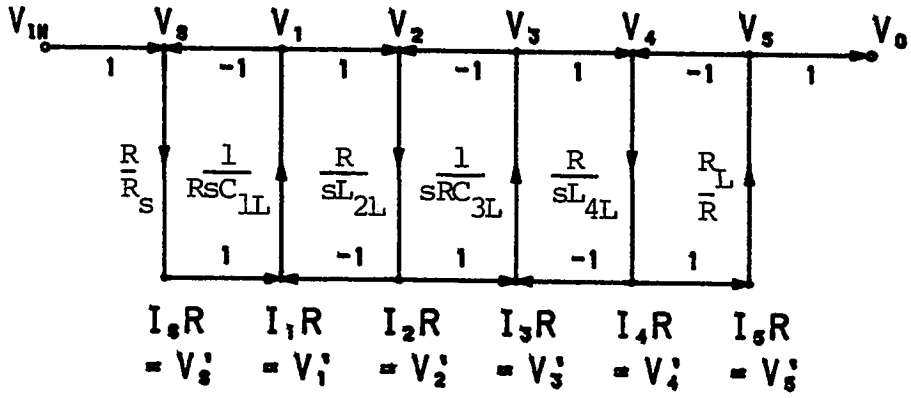


(c)

Figure 3.2 (a) Fourth order doubly terminated all pole low-pass filter. (b),(c) Signal-Flow-Graph of (a).

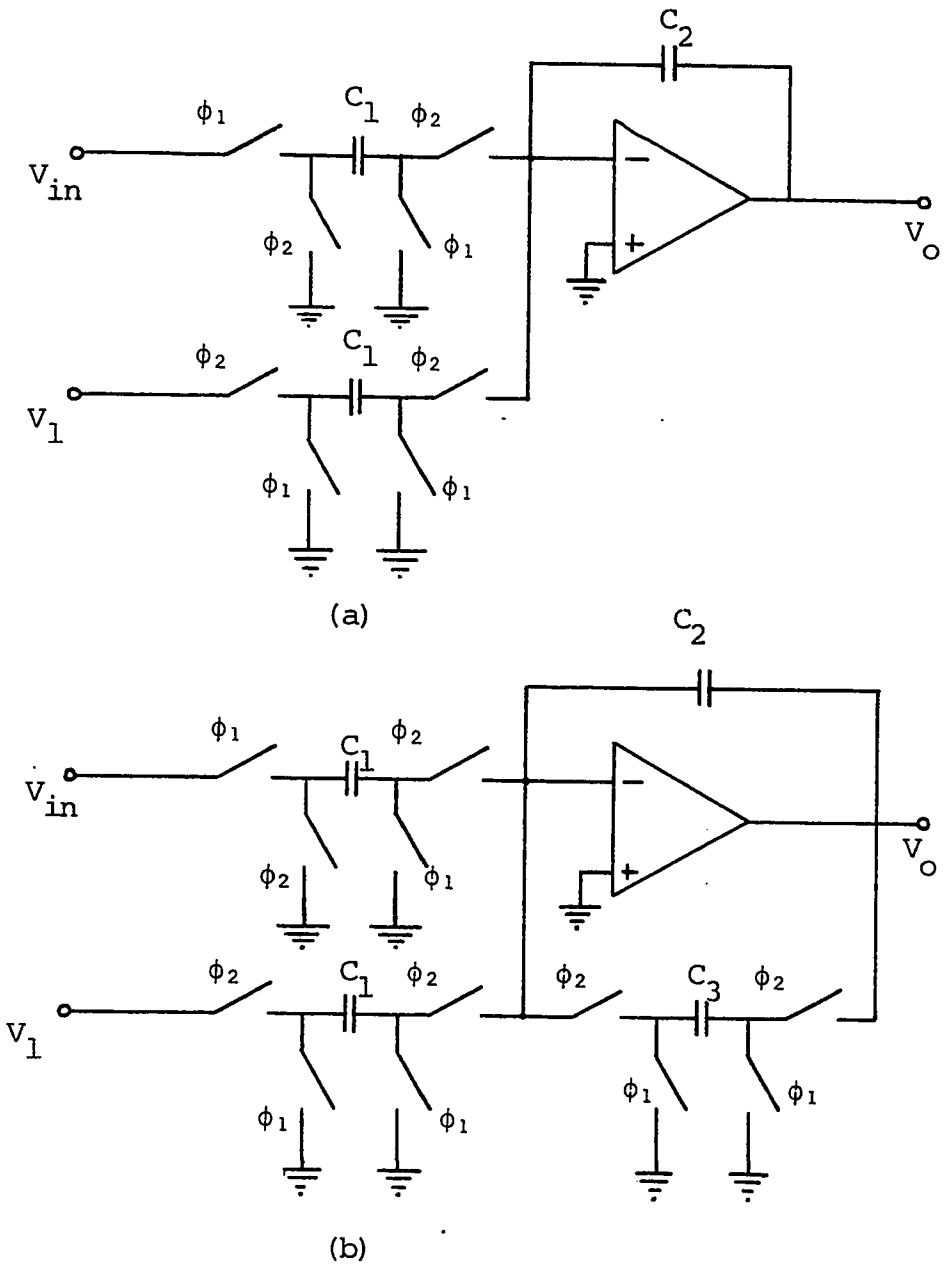


Figure 3.3 (a) A differential input SC LDI building block. (b) Modified LDI building block to realize the resistive source termination.

3.1.2.2 Band-Pass SC Ladder Filters

The design of SC band-pass ladder filters based on the LDI transformation is similar to the design of SC low-pass LDI ladder filters. The design procedure for geometrically symmetric band-pass ladder filters is shown below.

Suppose the following SC low-pass filter specifications:

A_{max} : maximum attenuation in the passband region

A_{min} : minimum attenuation in the stopband region

w_{p1}, w_{p2}: passband filter frequency

w_{s1}, w_{s2}: stopband filter frequency

Step 1

Obtain the band-pass continuous filter specifications Ω_{p1}, Ω_{p2}, Ω_{s1} and Ω_{s2} by prewarping w_{p1}, w_{p2}, w_{s1} and w_{s2} according to Eq. (3.3).

Step 2

Make the prewarped specifications geometrically symmetric, such that

$$\Omega_{p1}\Omega_{p2}=\Omega_{s1}\Omega_{s2}=\Omega_o^2$$

Hence obtain the normalized low-pass continuous filter specifications.

Step 3

Design the low-pass continuous filter by using the transformed specifications in step 2.

Step 4

Apply $S=(s^2+\Omega_o^2)/sB$ transformation to the low-pass continuous filter of step 3 to obtain the band-pass continuous ladder prototype, where

$$B=\Omega_{p2}-\Omega_{p1}$$

Step 5

Obtain the SFG of the band-pass continuous ladder filter obtained in step 4.

Step 6

Realize the resistive source termination and the reactive components of the SFG using the method explained for the design of SC low-pass ladder filters.

For further details, the reader is referred to Chapter 4 of reference [1].

3.1.2.3 High-Pass SC Ladder Filters

The design of high-pass LDI ladder filters have been studied by Taylor et. al.[34,35] and Baher[4]. Baher[4] has shown mathematically that the basic LDI building blocks are capable of providing high-pass filters with amplitude selectivity. However, these filters cannot be obtained from a lumped prototype. Beside this, the design technique requires the use of damped building blocks for the realization of resistive source and load terminations. These are conventional SC blocks with series or parallel SC branches on the feed-

back path. As was mentioned in the previous Sections, the use of damped building blocks for realizing resistive source and load terminations results in distortion of the magnitude response of the SC filter. Such a distortion is completely undesirable.

The design procedure of Taylor et. al.[34,35] makes use of unit element prototypes. To obtain SC high-pass LDI ladder filters, Taylor et. al. cascades each unit element in the low-pass prototype with a gyrator of the same impedance. However, with this design technique, the selectivity of the high-pass filter will in general be poorer that the desired one. Furthermore, their method is not applicable to the design of elliptic SC ladder filters[35].

3.2 Use of Bilinear Transformation in the Design of SC Ladder Filters

3.2.1 Properties of Bilinear Transformation

The bilinear transformation given by Eq. (3.7), unlike the LDI transformation, maps the entire imaginary axis of the s-plane onto the unit circle of the z-plane. Hence, the frequency warping effects are different.

$$s = \frac{2}{T}\,\frac{1-z^{-1}}{1+z^{-1}} \tag{3.7}$$

The relationship between the continuous-time frequency Ω and the discrete frequency w can be found by letting $s=\sigma+j\Omega$ and $z=\exp(jwT)$ in Eq. (3.7). This gives

$$\sigma+j\Omega = j\frac{2}{T}\tan\left(\frac{wT}{2}\right) \tag{3.8}$$

Equating the real and imaginary parts yields

$$\sigma = 0 \quad \text{and} \quad \Omega = \frac{2}{T}\tan\left(\frac{wT}{2}\right) \tag{3.9}$$

Since the continuous-time and discrete-time frequencies are not linearly related, the SC filter specifications have to be "prewarped" according to Eq. (3.9). The warping effect of Eq. (3.9) is depicted in Fig. 3.4. In the same figure, the curve showing the warping effect of the LDI transformation has also been plotted for comparison. It can be observed that the warping introduced by the bilinear transformation is greater than that of LDI transformation.

The bilinear discrete integrator transfer function is given by[6]

$$H_{\text{Bilinear}}(z) = P\,\frac{1+z^{-1}}{1-z^{-1}} \tag{3.10}$$

where P is a constant. It has been shown in Section 2.3 that, if the output of the bilinear integrator shown in Fig. 2.15(a) is sampled at both phases, then the transfer function becomes identical to the bilinear discrete integrator transfer function. However, this circuit is sensitive to parasitic effects. Many stray insensitive building blocks

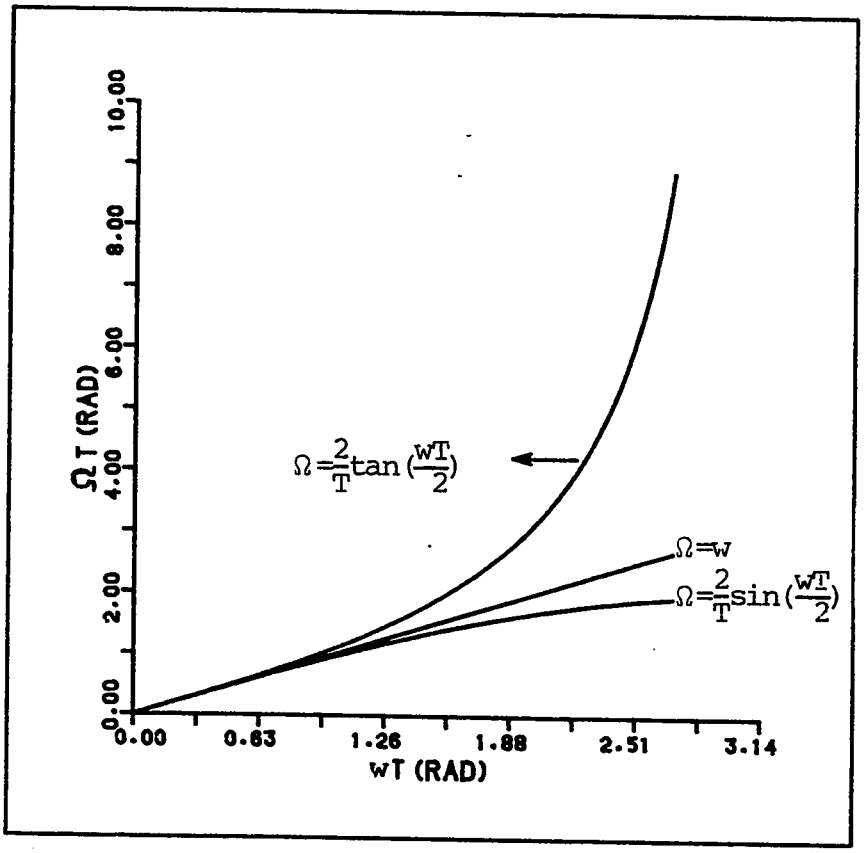


Figure 3.4 Warping effect of the Bilinear transformation

that realize the bilinear transfer function is available in the literature[21,27,28,29]. One such building block proposed by Lee et. al.[28] is shown in Fig. 3.5.

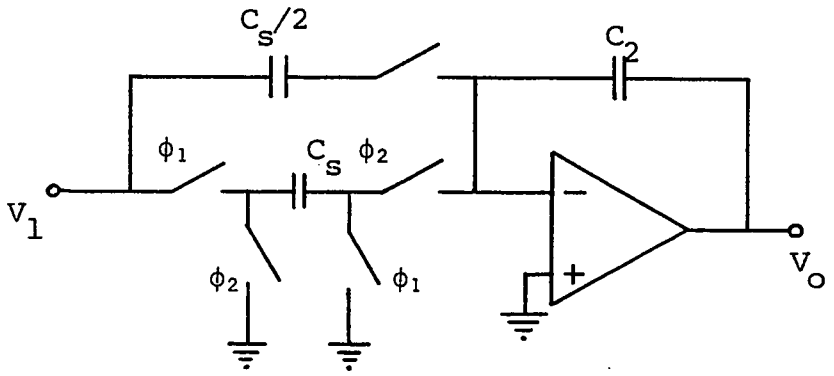


Figure 3.5 First order low-pass SC building block realizing the bilinear transfer function.

3.2.2 Design of SC Ladder Filters Based on the Bilinear Transformation

Several design techniques have been proposed for the design of SC ladder filters using the bilinear z-transformation. However, the discussion of these methods is far beyond the scope of this thesis. One of the methods utilize the same procedure given in Section 3.1 for the design of SC low-pass and band-pass ladder filters using the LDI and Bilinear transformations. The building block shown in Fig. 2.15(a), though stray-sensitive, can be used for realizing the reactive components of the prototype SFG.

A unique problem exists in the design of bilinear high-pass (and band-stop) filters[20]. Gregorian et. al.[20] say that, for an input sample-and-hold signal of discrete frequency $f=f_c/2$, the input branch does not transmit any charge to the first op-amp for $z=-1$. Therefore, for a high-pass response, which requires $V_{out}(z)$ to be non-zero at $z=-1$, the transfer impedance of the rest of the circuit must be infinite. This causes instability if the high-pass ladder filter is designed using the design procedure presented in Section 3.1. This problem has been overcome by using impedance scaling[21,28].

In the design method proposed by Lee et. al.[28] for the high-pass SC ladder filters, some of the branches used were stray-sensitive. This is definitely undesirable. Lin et.

al.[29] have proposed a circuit technique to transform the high-pass filter proposed by Lee et. al.[28], into a stray-insensitive one. However, no details are given.

On the other hand, the method proposed by Hokenek et.al.[21], uses stray-insensitive SC branches, however, the design procedure is not as direct as the one that we shall propose in Chapter 4.

3.3 Use of MLDD Transformation in the Design of SC High-Pass Ladder Filters

3.3.1 Properties of the MLDD Transformation

The modified lossless discrete differentiator(MLDD) transformation given by Eq. 3.11, was originally proposed by Bruton[6] for the purpose of realizing low-sensitivity high-pass leapfrog digital ladder filters.

$$s = \frac{2}{T}\,\frac{z^{-1/2} - z^{-3/2}}{1+z^{-2}} \tag{3.11}$$

where 1/T is the sampling frequency. To see the effect of this transformation on the design of SC high-pass ladder filters, we let $s=\sigma+j\Omega$ and $z=\exp(jwT)$. Hence Eq. (3.11) becomes

$$\sigma+j\Omega = j\,\frac{2}{T}\,\frac{\sin(wT/2)}{\cos(wT)} \tag{3.12}$$

where Ω and w are the continuous and discrete angular frequencies respectively. Equating the real and imaginary parts of Eq. (3.12) gives

$$\sigma = 0 \quad \text{and} \quad \Omega = \frac{2}{T}\,\frac{\sin(wT/2)}{\cos(wT)} \tag{3.13}$$

The plot of Eq. (3.12) in Fig. 3.6 shows the warping effect of the MLDD transformation. Note that this curve is completely different from the warping curves for bilinear and LDI transformations in the sense that MLDD transformation exhibits non-linearity when wt approaches π/2, whereas the LDI and bilinear transformations exhibit non-linearity when wT approaches π.

The MLDD transfer function[6] is given by

$$H_{mldd}(z) = P\,\frac{z^{-1/2} - z^{-3/2}}{1+z^{-3/2}} \tag{3.14}$$

where P is a constant. The switched capacitor realization of the MLDD transfer function was originally realized by Horio et. al.[22]. Switched capacitor, MLDD building blocks proposed by Horio et. al.[22] is shown in Fig. 3.7. If the output of this SC building block is sampled at the end of clock phase 2, then, its transfer function can be written as[22]

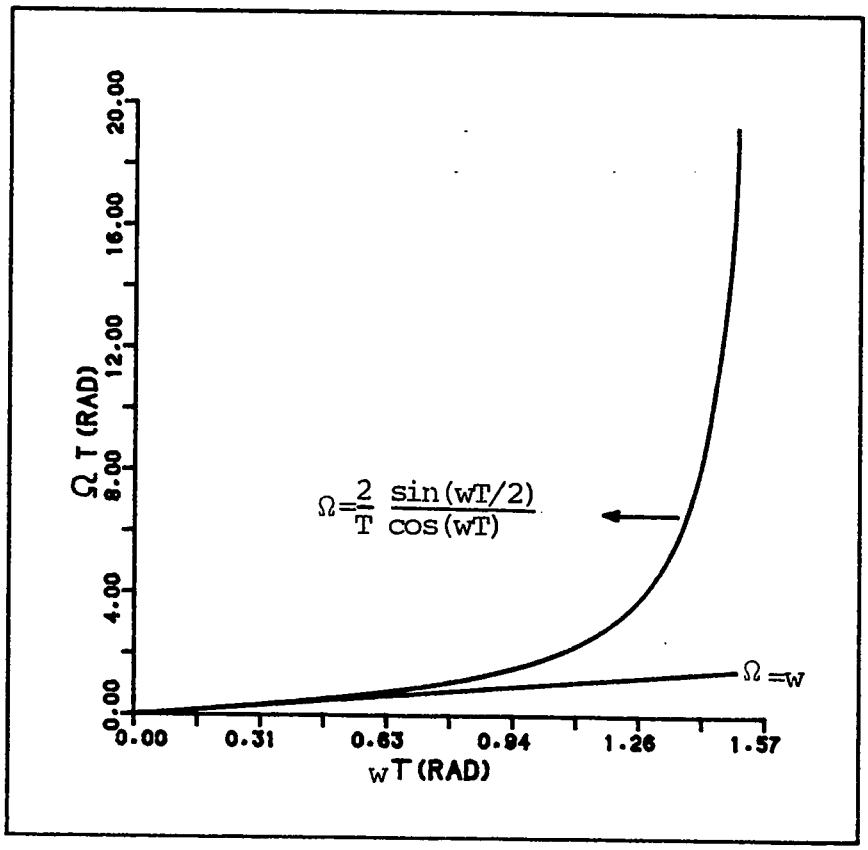


Figure 3.6 Warping effect of the MLDD transformation

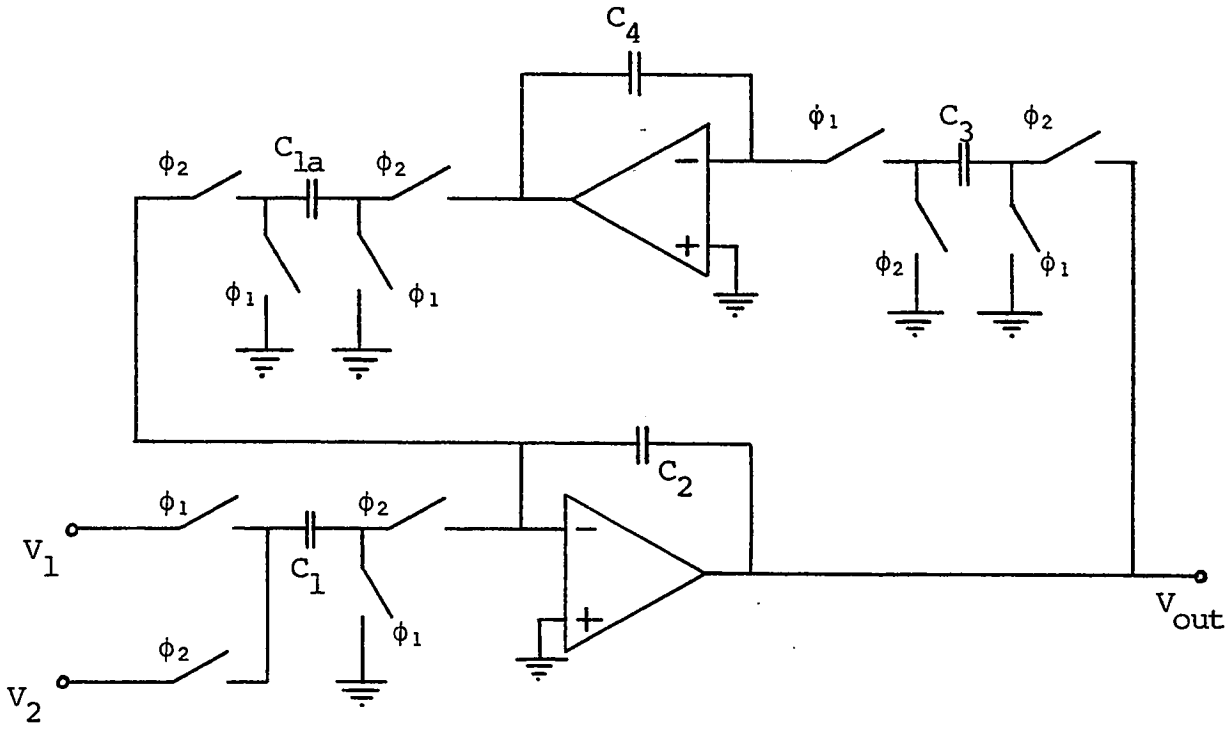


Figure 3.7 Stray-insensitive MLDD building block of Horio et.al. with two op-amps.

$$H^{oe}(z) = \frac{V^{e}_{out}(z)}{(V^{o}_{1}(z) - V^{o}_{2}(z))} = \frac{C_1}{C_2} \frac{z^{-1/2} - z^{-3/2}}{1 + z^{-2}} \qquad (3.15)$$

where $C_1/C_2=2C_4/C_3$, $C_1=C_{1a}$ and inputs are sampled-and-held signals. In addition to the two op-amp MLDD building block, Horio et. al. have also proposed a single op-amp MLDD building block as shown in Fig. 3.8. However, it can easily be observed that the top plates of the capacitors used in this single op-amp configuration are stray-sensitive. Furthermore, two of the feedback capacitors have floating nodes and the op-amp has an open feedback path between switching intervals. These factors make such a configuration physically unrealizable.

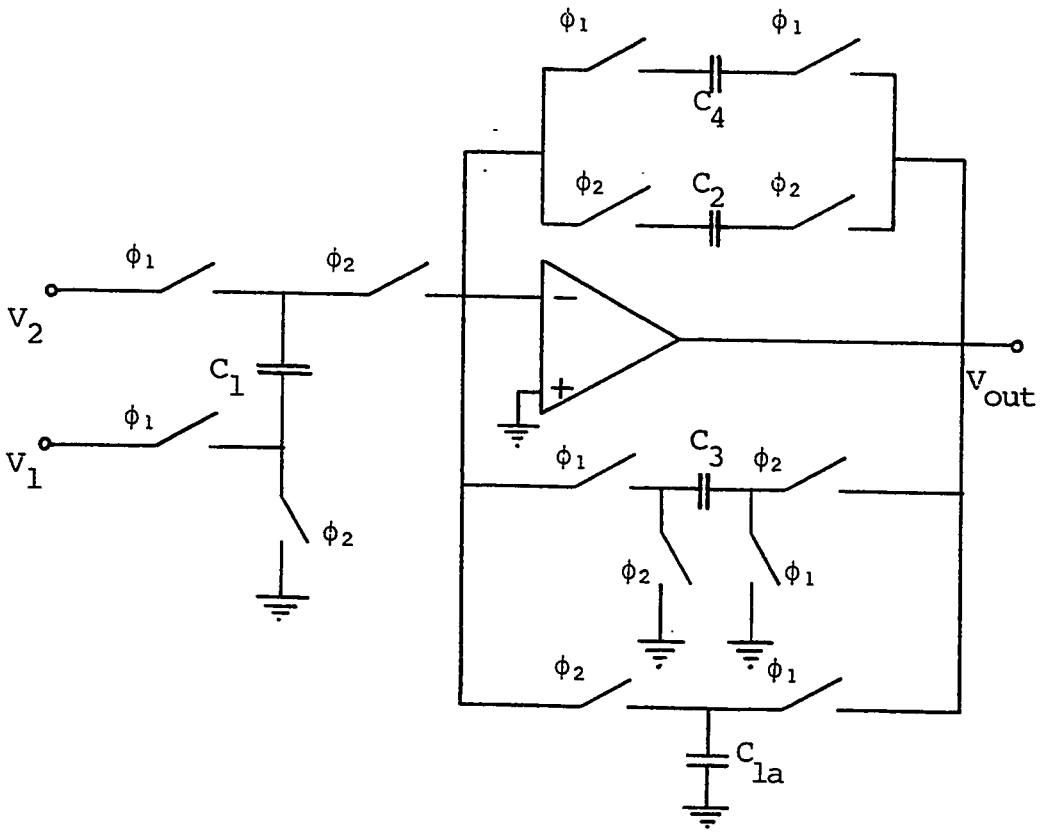


Figure 3.8 Single op-amp MLDD building block of Horio et. al..

3.3.2 Design of High-Pass Ladder Filters based on the MLDD Transformation

First of all, it should be pointed out that the design procedure proposed by Horio et. al. for the design of SC high-pass ladder filters using the MLDD transformation is very loosely stated. In the next Chapter, we shall propose a new and more concrete design procedure for the design of high-pass ladder filters based on the MLDD transformation.

In the realization by Horio et. al., the resistive source termination of the analog ladder filter is realized using a stray-insensitive parallel feedback path across the first building block. As was mentioned earlier and as it will be shown in the next Chapter, such a realization results in a very large distortion in the magnitude response of the SC filter. This distortion can be completely removed by a new realization technique that will be proposed in the next Chapter.

Chapter IV

A NEW SWITCHED CAPACITOR HIGH-PASS FILTER REALIZATION USING THE MLDD TRANSFORMATION

The properties and application of the MLDD transformation to the design of SC high-pass ladder filters have already been discussed in Section 3.3. In this chapter, a new switched capacitor realization for the design of SC ladder filters using the MLDD transformation is proposed. By realizing the resistive source termination of the continuous filter prototype with a special delay-free circuit, a much superior magnitude response is obtained[32].

4.1 Design Procedure

Suppose the following SC high-pass filter specifications

A_{max}: maximum attenuation in the passband region

A_{min}: minimum attenuation in the stopband region

w_p : passband edge frequency

w_s : stopband edge frequency

With the above specifications, a switched capacitor high-pass ladder filter is designed using the following steps:

Step 1

Obtain the high-pass continuous filter specifications Ω_p and Ω_s by prewarping w_p and w_s according to:

$$\Omega=\frac{2}{T}\frac{\sin(wT/2)}{\cos(wT)}$$

Step 2

Transform the high-pass continuous filter specifications into the low-pass continuous filter specifications using $s=\Omega_p/S$ transformation.

Step 3

Design the low-pass continuous filter by using the transformed specifications in step 2.

Step 4

Apply $S=\Omega_p/s$ transformation to the low-pass continuous filter of step 3 to obtain the high-pass continuous ladder prototype.

Step 5

Obtain the SFG of the high-pass continuous ladder filter obtained in Step 4.

Step 6

Realize the resistive source termination and the reactive components of the SFG using the method explained in the following Sections.

4.2 SFG Synthesis of High-Pass SC Ladder Filters

Consider the signal flow graph of an even, n'th order high-pass continuous Chebychev filter as shown in Fig. 4.1. The resistive source termination is the leftmost vertical component of the SFG with gain R/R_S. The reactive components are those sections containing the reactive term, and the load termination is the rightmost vertical component with gain R_L/R. From this signal flow graph, it can be observed that each component except the load termination has a differential input. Furthermore, each reactive component represents a differentiator in contrast to the low-pass case, where each reactive component corresponds to an integrator.

In the design of high-pass SC ladder filters using the MLDD transformation, each reactive component in the SFG is replaced by a building block realizing the MLDD transfer function. As was mentioned earlier, the resistive source termination can be realized by a series or parallel type SC feedback path across the first MLDD building block[8,12]. However, the overall transfer function of the SC network becomes different from the transfer function of high-pass SC ladder filter, which is obtained from a continuous filter prototype by the MLDD transformation. This variation in the transfer function causes a distortion in the magnitude response of the SC filter. We propose that realizing the resistive source terminations separately by a delay free,

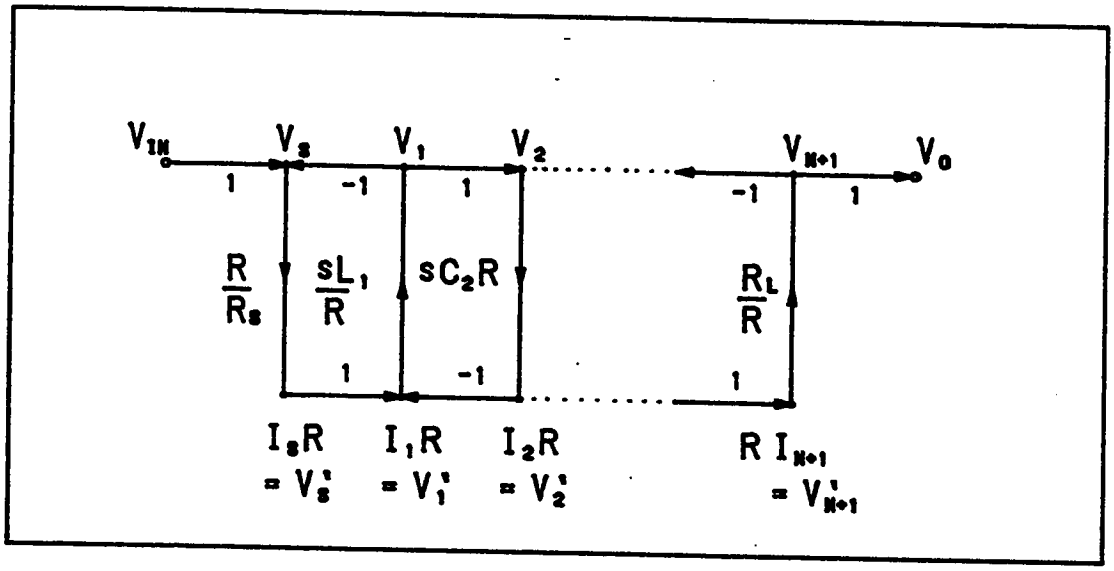


Figure 4.1 SFG for an n'th order high-pass continuous Chebychev filter(n even).

differential input SC amplifier of constant gain R/R_s will give a much better magnitude response. This is because for the proposed configuration, the overall transfer function of the high-pass SC ladder filter will be exactly the same as the transfer function obtained from the high-pass continuous ladder filter by the direct application of the MLDD transformation. The resistive load termination corresponds to a feedback from the output to the input of the final reactive component of the SFG. By setting R_L equal to R, this feedback becomes unity and can be realized by a direct connection.

4.3 A New MLDD Building Block for the Design of High-Pass SC Ladder Filters

The MLDD transfer function[6] was introduced in Section 3.3 and is repeated here for convenience.

$$H_{mldd} = P \frac{z^{-1/2} - z^{-3/2}}{1 + z^{-2}} \qquad (4.1)$$

where P is a constant.

We have realized the MLDD transfer function by a fully differential op-amp as shown in Fig. 4.2. The analysis and derivation of the transfer function of this circuit is shown below.

The clock waveforms driving the two switches are shown in Fig. 1.2. For the analysis, we have assumed ideal switches and ideal fully-differential op-amps.

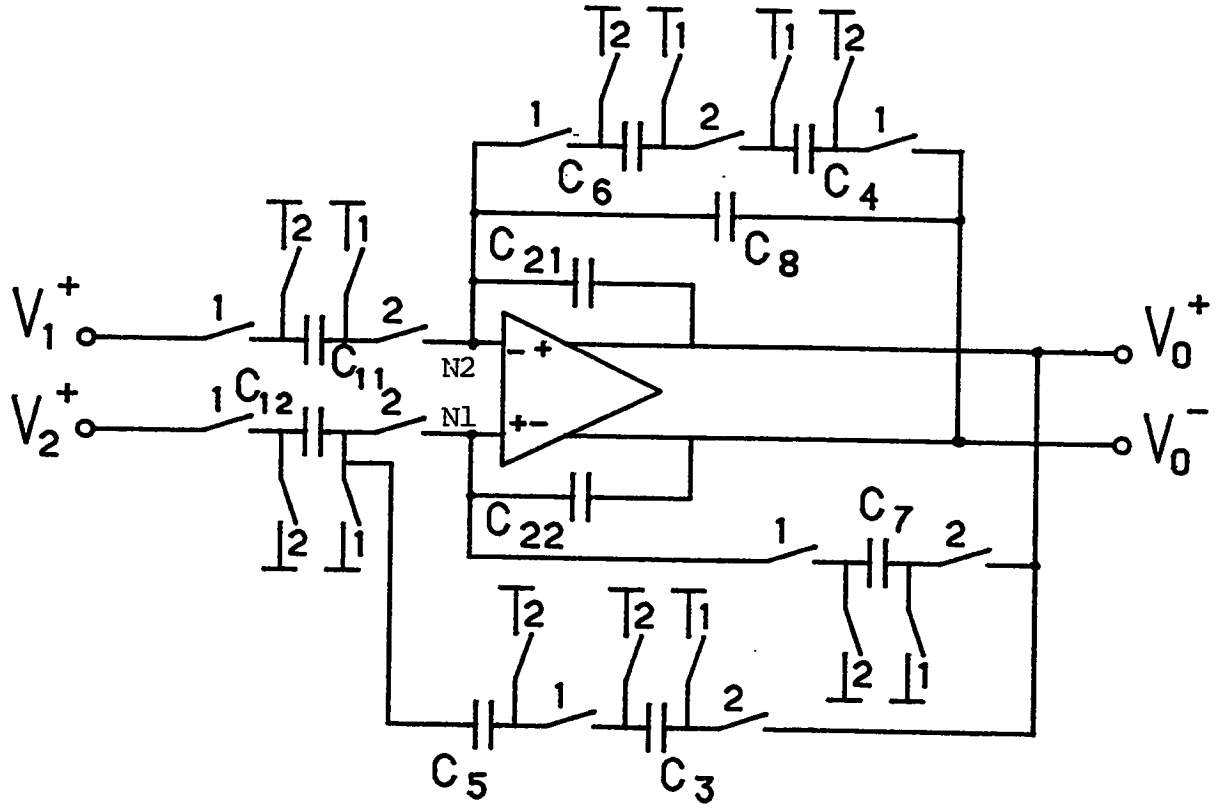


Figure 4.2 Stray-insensitive, fully differential MLDD building Block

At t=(n-1/2)T, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 4.3(a). The application of the conservation of charge law at node N1 gives

$$[V_{N1}^{e}(n-1/2)-V_{N1}^{o}(n-1)] = \frac{-C_{12}}{(C_{12}+C_{22}+C_5)} V_2^{+o}(n-1) + \frac{C_{22}}{(C_{12}+C_{22}+C_5)}[V_o^{-e}(n-1/2)-V_o^{-o}(n-1)]$$

$$+ \frac{C_3 C_5}{(C_3+C_5)(C_{12}+C_{22}+C_5)} V_o^{+e}(n-3/2) \qquad (4.2)$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 is shown in Fig. 4.3(b). The application of the conservation of charge law at node N2 yields

$$[V_{N2}^{e}(n-1/2) - V_{N2}^{o}(n-1)] = \frac{C_8}{(C_{11}+C_{21}+C_8)}[V_o^{-e}(n-1/2)-V_o^{-o}(n-1)] - \frac{C_{11}}{(C_{11}+C_{21}+C_8)} V_1^{+o}(n-1)$$

$$+ \frac{C_{21}}{(C_{11}+C_{21}+C_8)} [V_o^{+e}(n-1/2) - V_o^{+o}(n-1)] \qquad (4.3)$$

For an ideal differential op-amp, the voltage at the inverting input terminal equals the voltage at the non-inverting input terminal. Hence we can write

$$V_{N1}^{e}(n-1/2)-V_{N1}^{o}(n-1)=V_{N2}^{e}(n-1/2)-V_{N2}^{o}(n-1)$$

Therefore, equating Eq. (4.2) to Eq. (4.3), we obtain

$$\frac{-C_{12}}{(C_{12}+C_{22}+C_5)} V_2^{+o}(n-1) + \frac{C_{22}}{(C_{12}+C_{22}+C_5)}[V_o^{-e}(n-1/2)-V_o^{-o}(n-1)] + \frac{C_3 C_5}{(C_3+C_5)(C_{12}+C_{22}+C_5)} V_o^{+e}(n-3/2)$$

$$= \frac{-C_{11}}{(C_{11}+C_{21}+C_8)} V_1^{+o}(n-1) + \frac{C_{21}}{(C_{11}+C_{21}+C_8)}[V_o^{+e}(n-1/2)-V_o^{+o}(n-1)]$$

$$+ \frac{C_8}{(C_{11}+C_{21}+C_8)}[V_o^{-e}(n-1/2) - V_o^{-o}(n-1)] \qquad (4.4)$$

Substituting $V_i^+=-V_i^-=V_i$ for i=0,1,2 and taking the z-transform of both sides of equation (4.4) gives

$$\frac{-C_{12}}{(C_{12}+C_{22}+C_5)} z^{-1} V_2^o(z) + \frac{C_{22}}{(C_{12}+C_{22}+C_5)}[z^{-1} V_o^o(z) - z^{-1/2} V_o^e(z)] + \frac{C_3 C_5}{(C_3+C_5)(C_{12}+C_{22}+C_5)} z^{-3/2} V_o^e(z)$$

$$= \frac{-C_{11}}{(C_{11}+C_{21}+C_8)} z^{-1} V_1^o(z) + \frac{C_{21}}{(C_{11}+C_{21}+C_8)}[z^{-1/2} V_o^e(z) - z^{-1} V_o^o(z)]$$

$$- \frac{C_8}{(C_{11}+C_{21}+C_8)}[z^{-1/2} V_o^e(z) - z^{-1} V_o^o(z)] \qquad (4.5)$$

Letting

$$A = \frac{C_{11}}{(C_8+C_{11}+C_{21})} = \frac{C_{12}}{(C_{12}+C_{22}+C_5)} \qquad (4.6)$$

and

$$B = \frac{C_8}{3(C_8+C_{11}+C_{21})} = \frac{C_{21}}{2(C_8+C_{11}+C_{21})} \qquad 95$$

$$= \frac{C_{22}}{2(C_{12}+C_{22}+C_5)} = \frac{C_3C_5}{(C_3+C_5)(C_{12}+C_{22}+C_5)} \qquad (4.7)$$

Substituting A and B into equation (4.5), we obtain

$$Az^{-1}(V_1^o(z)-V_2^o(z)) = B[z^{-1/2}V_o^e(z)-z^{-3/2}V_o^e(z)-z^{-1}V_o^o(z)] \qquad (4.8)$$

At t=nT, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 4.3(c). The application of the conservation of charge law at node N1 gives

$$V_{N1}^o(n)-V_{N1}^e(n-1/2) = \frac{-C_7}{(C_7+C_{22})}V_o^{+e}(n-1/2) + \frac{C_{22}}{(C_7+C_{22})}[V_o^{-o}(n)-V_o^{-e}(n-1/2)] \qquad (4.9)$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 becomes as shown in Fig. 4.3(d). Applying the conservation of charge law at node N2 yields

$$V_{N2}^o(n)-V_{N2}^e(n-1/2) = \frac{C_8}{(C_8+C_6+C_{21})}[V_o^{-o}(n)-V_o^{-e}(n-1/2)] + \frac{C_6C_4}{(C_4+C_6)(C_6+C_{21}+C_8)}V_o^{-o}(n-1)$$

$$+ \frac{C_{21}}{(C_6+C_{21}+C_8)}[V_o^{+o}(n)-V_o^{+e}(n-1/2)] \qquad (4.10)$$

Equating (4.9) to (4.10) under the ideal op-amp assumption, we obtain

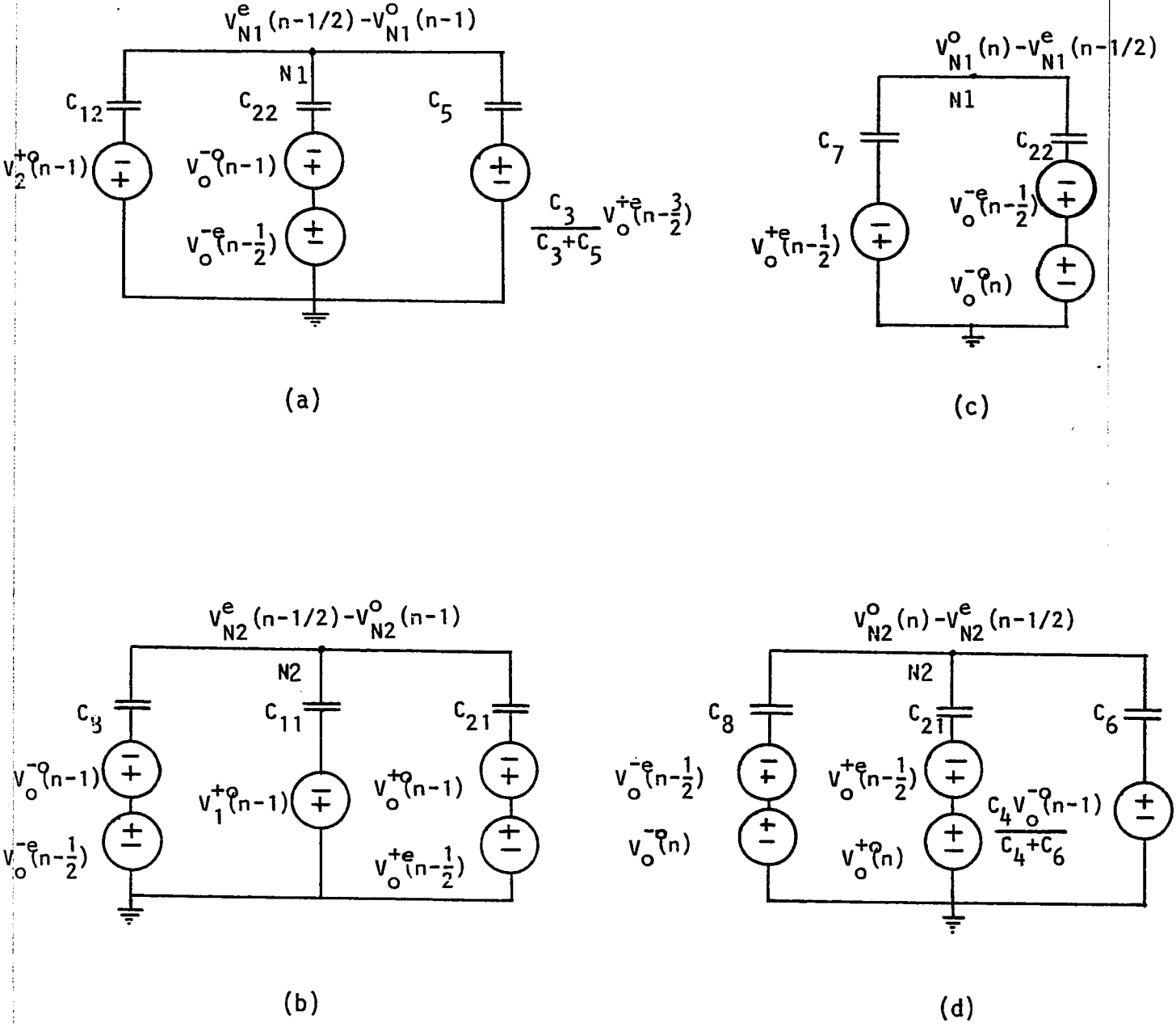


Figure 4.3 Equivalent circuit for the charge distribution: (a) at node N1 when t=(n-1/2)T (b) at node N2 when t=(n-1/2)T (c) at node N1 when t=nT (d) at node N2 when t=nT

$$\frac{-C_7}{(C_7+C_{22})} V_o^{+e}(n-1/2) + \frac{C_{22}}{(C_7+C_{22})}[V_o^{-o}(n)-V_o^{-e}(n-1/2)] = \frac{C_8}{(C_8+C_6+C_{21})}[V_o^{-o}(n)-V_o^{-e}(n-1/2)]$$

$$+ \frac{C_6 C_4}{(C_4+C_6)(C_6+C_{21}+C_8)} V_o^{-o}(n-1) + \frac{C_{21}}{(C_6+C_{21}+C_8)}[V_o^{+o}(n)-V_o^{+e}(n-1/2)] \qquad (4.11)$$

Substituting $V_i^+=-V_i^-=V_i$ for i=0,1,2 and taking the z-transform of both sides of equation (4.11) gives

$$\frac{-C_7}{(C_7+C_{22})} z^{-1/2} V_o^e(z) + \frac{C_{22}}{(C_7+C_{22})}[z^{-1/2} V_o^e(z) - V_o^o(z)] = \frac{-C_4 C_6}{(C_4+C_6)(C_6+C_{21}+C_8)} z^{-1} V_o^o(z)$$

$$+ \frac{C_{21}}{(C_6+C_{21}+C_8)}[V_o^o(z)-z^{-1/2} V_o^e(z)] - \frac{C_8}{(C_6+C_{21}+C_8)}[V_o^o(z)-z^{-1/2} V_o^e(z)] \qquad (4.12)$$

Letting

$$E = \frac{C_{21}}{(C_6+C_8+C_{21})} = \frac{2C_{22}}{3(C_7+C_{22})} = \frac{C_7}{3(C_7+C_{22})}$$

$$= \frac{C_4 C_6}{(C_4+C_6)(C_6+C_8+C_{21})} \qquad (4.13)$$

Substituting equation (4.13) into equation (4.12) and simplifying gives

$$V_o^o(z) = \frac{-2z^{-1/2} V_o^e(z)}{(1-z^{-1})} \qquad (4.14)$$

Next substituting Eq. (4.14) into Eq. (4.8) and simplifying yields

$$V_o^e(z) = \frac{A}{B}\left(\frac{z^{-1} - z^{-2}}{z^{-1/2} + z^{-5/2}}\right)[V_1^o(z) - V_2^o(z)] \tag{4.15}$$

After multiplying both the numerator and the denominator of Eq. (4.15) by $z^{1/2}$, the transfer function of the circuit can be written as follows,

$$\frac{V_o^e(z)}{[V_1^o(z)-V_2^o(z)]} = \frac{A}{B}\left(\frac{z^{-1/2} - z^{-3/2}}{1+z^{-2}}\right) \tag{4.16}$$

To reduce the complexity of equations (4.6), (4.7) and (4.13), without any loss of generality, let

$$C_{11}=C_{12}=C_1 \text{ and } C_{21}=C_{22}=C_2$$

Solving for C_3 through C_8, we obtain

$$C_3 = (3/4)C_2 \tag{4.17a}$$

$$C_4 = 2C_2 \tag{4.17b}$$

$$C_5 = (3/2)C_2 \tag{4.17c}$$

$$C_6 = 2C_2 \tag{4.17d}$$

$$C_7 = 2C_2 \tag{4.17e}$$

$$C_8 = (3/2)C_2 \tag{4.17f}$$

Under these conditions, the transfer function given by Eq. (4.16) will be reduced to

$$\frac{V_o^e(z)}{[V_1^o(z)-V_2^o(z)]} = \frac{2C_1}{C_2}\left(\frac{z^{-1/2}-z^{-3/2}}{1+z^{-2}}\right) \qquad (4.18)$$

Equation (4.18)is similar to Eq. (4.1) with $P=2C_1/C_2$, which shows that the SC circuit shown in Fig. 4.2, realizes the MLDD transfer function.

4.4 Building Block For Realizing the Resistive Source Termination of the Continuous Ladder Filter Prototype

Consider the SC circuit shown in Fig. 4.4(a), which is proposed for the realization of the resistive source termination.

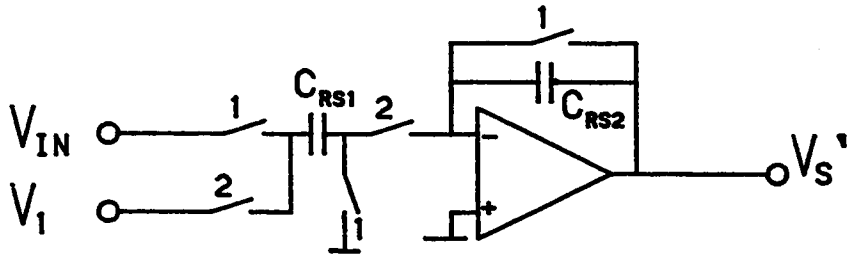
At t=(n-1/2)T, the equivalent circuit for the charge distribution at the inverting input is shown in Fig. 4.4(b). The application of the conservation of charge law at the inverting input results in the following difference equation:

$$C_{RS1}(V_1^e(n-1/2) - V_{in}^o(n-1)) + C_{RS2}V_s'^e(n-1/2) = 0 \qquad (4.19)$$

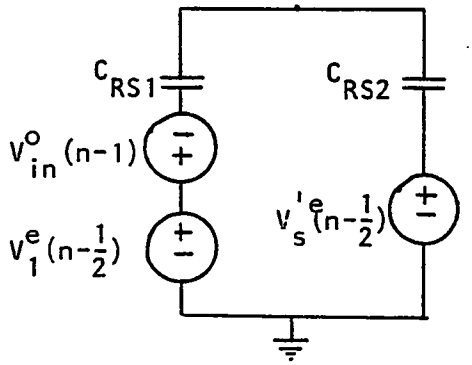
Taking the z-transform of both sides of Eq. (4.19) gives

$$C_{RS1}z^{-1/2}V_1^e(z) - C_{RS1}z^{-1}V_{in}^o(z) + C_{RS2}z^{-1/2}V_s'^e(z) = 0 \qquad (4.20)$$

Assuming the input signal V_{in} is sampled-and-held such that



(a)



(b)

Figure 4.4 (a) Stray-insensitive op-amp for realizing the resistive source termination (b) Equivalent circuit for the charge distribution at the inverting input for t=(n-1/2)T.

$$V_{in}^{e}(z) = z^{-1/2} V_{in}^{o}(z) \tag{4.21}$$

Substituting Eq. (4.21) into Eq. (4.20), we obtain

$$V_{s}^{'e}(z) = (C_{RS1}/C_{RS2})\,[V_{in}^{e}(z) - V_{1}^{e}(z)] \tag{4.22}$$

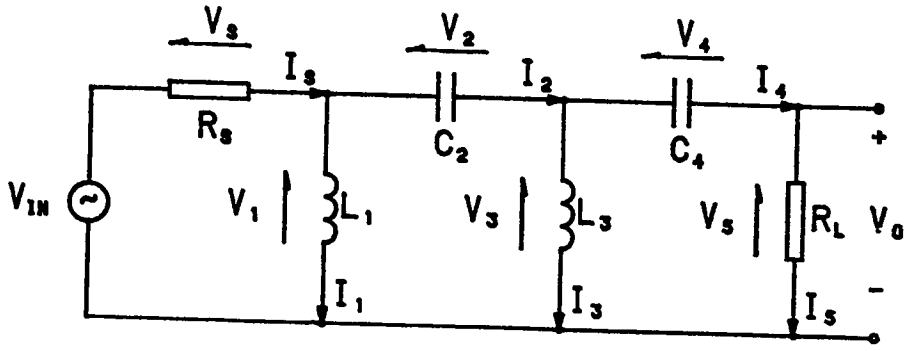
Eq. (4.22) shows that the circuit proposed in Fig. 4.4(a) realizes a differential amplifier of constant gain C_{RS1}/C_{RS2}, which makes it a suitable building block for realizing the resistive source termination of the continuous ladder filter prototype.

4.5 Design Example

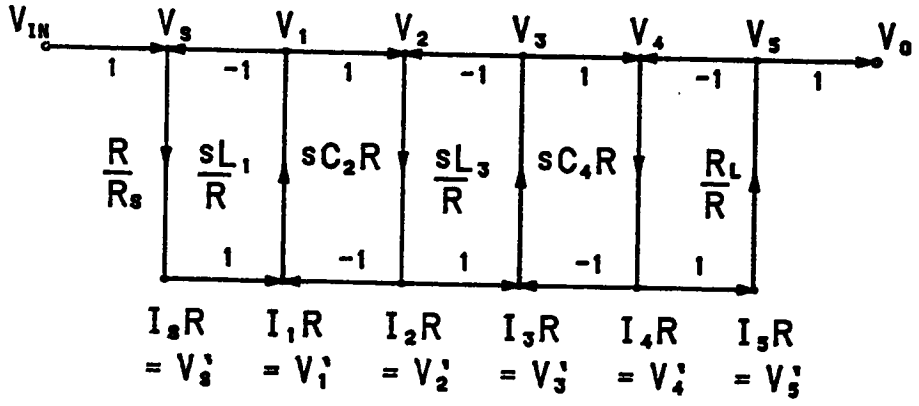
Consider the design of a high-pass SC Chebychev filter using the following specifications:

A_{max}=1 dB, A_{min}=25 dB, f_p=10 kHz (or w_p=62.83 kad/sec), f_s=6.5 kHz (or w_s=40.84 krad/sec), 1/T=80 kHz.

Using the design procedure described in Section 4.1, the order of the filter is found to be 4. The circuit for the prewarped continuous high-pass ladder filter and its corresponding SFG are shown in Fig. 4.5(a) and 4.5(b), respectively. Realizing the source termination with the building block circuit shown in Fig. 4.4(a) and the reactive components with the circuit shown in Fig. 4.2, the SC filter



(a)



(b)

Figure 4.5 (a) Fourth order continuous high-pass Chebychev ladder filter. (b) SFG of 4.5(a).

required to meet the given specifications is obtained as shown in Fig. 4.6.

For an even order high-pass Chebychev filter, load resistance R_L is usually calculated to give the value for maximum power transfer. For the above example, R_L is calculated to be 0.376 Ohms. As was mentioned in Section 4.2, this has to be equated to R in order to accomplish unity feedback for the realization of the resistive load termination. Source resistance R_s is usually taken as 1 Ohm. For the source termination, the gain of the SFG has to equated to C_{RS1}/C_{RS2}. This gives the capacitor ratio for the first section as

$$\frac{C_{RS1}}{C_{RS2}} = \frac{R}{R_s} = 0.376 \qquad (4.23)$$

The capacitance ratios of the reactive components can be calculated by equating the gain of each reactive component of the SFG to the gain of the MLDD transfer function as given in Eq. (4.18). This results in the following capacitance ratios for the reactive sections:

$$\frac{C_{11}}{C_{12}} = \frac{L_1}{RT} = 1.170 \qquad (4.24)$$

$$\frac{C_{21}}{C_{22}} = \frac{RC_2}{T} = 0.326 \qquad (4.25)$$

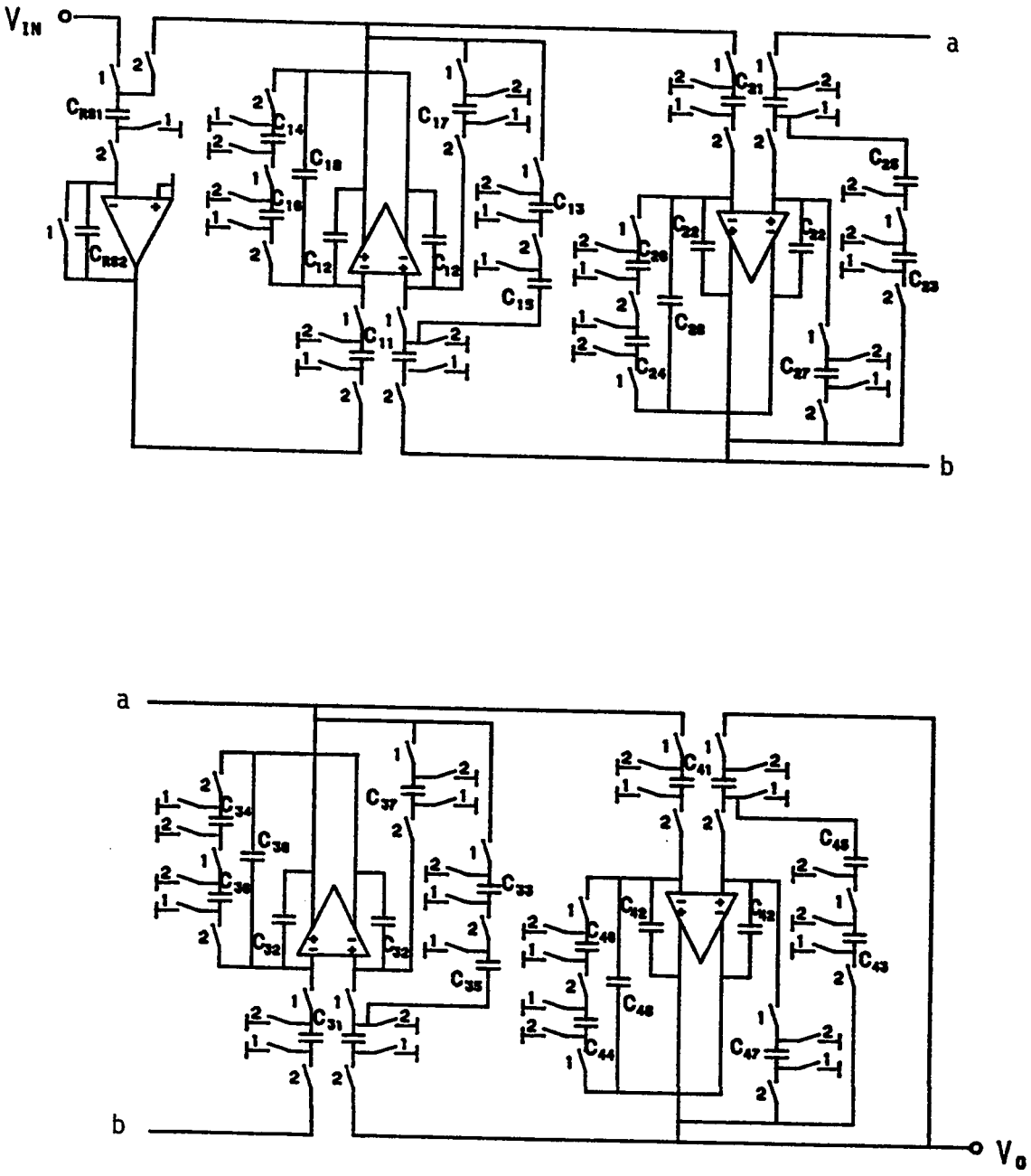


Figure 4.6 Fourth order SC high-pass Chebychev ladder filter based on the MLDD transformation.

$$\frac{C_{31}}{C_{32}} = \frac{L_3}{RT} = 0.868 \qquad (4.26)$$

$$\frac{C_{41}}{C_{42}} = \frac{RC_4}{T} = 0.440 \qquad (4.27)$$

Capacitance values C_{13} through C_{18}, C_{23} through C_{28}, C_{33} through C_{38}, C_{43} through C_{48} can be calculated using Equations (4.23) through (4.27) and Eq. (4.17) respectively. As was mentioned earlier, in SC filter design, the capacitance values are normalized with respect to the smallest capacitance in the circuit. For SC ladder filters, the normalized capacitances are calculated for each section separately. For the above design example the normalized capacitances have been calculated to be as follows:

Normalized Capacitances for the source termination

$C_{RS1} = C_u$

$C_{RS2} = 2.659C_u$

Normalized Capacitances for the Section No: 1

$C_{11} = 1.561C_u$

$C_{12} = 1.333C_u$

$C_{13} = C_u$

$C_{14} = 2.667C_u$

$C_{15} = 2.000C_u$

$C_{16} = 2.667C_u$

$C_{17} = 2.667C_u$

$C_{18} = 2.000C_u$

Normalized Capacitances for the Section No: 2

$C_{21} = C_u$

$C_{22} = 3.064C_u$

$C_{23} = 2.298C_u$

$C_{24} = 6.128C_u$

$C_{25} = 4.596C_u$

$C_{26} = 6.128C_u$

$C_{27} = 6.128C_u$

$C_{28} = 4.596C_u$

Normalized Capacitances for the Section No: 3

$C_{31} = 1.567C_u$

$C_{32} = 1.333C_u$

$C_{33} = C_u$

$C_{34} = 2.667C_u$

$C_{35} = 2.000C_u$

$C_{36} = 2.667C_u$

$C_{37} = 2.667C_u$

$C_{38} = 2.000C_u$

Normalized Capacitances for the Section No: 4

$C_{41} = C_u$

$C_{42} = 2.272C_u$

$C_{43} = 1.704C_u$

$C_{44} = 4.544C_u$

$C_{45} = 3.408C_u$

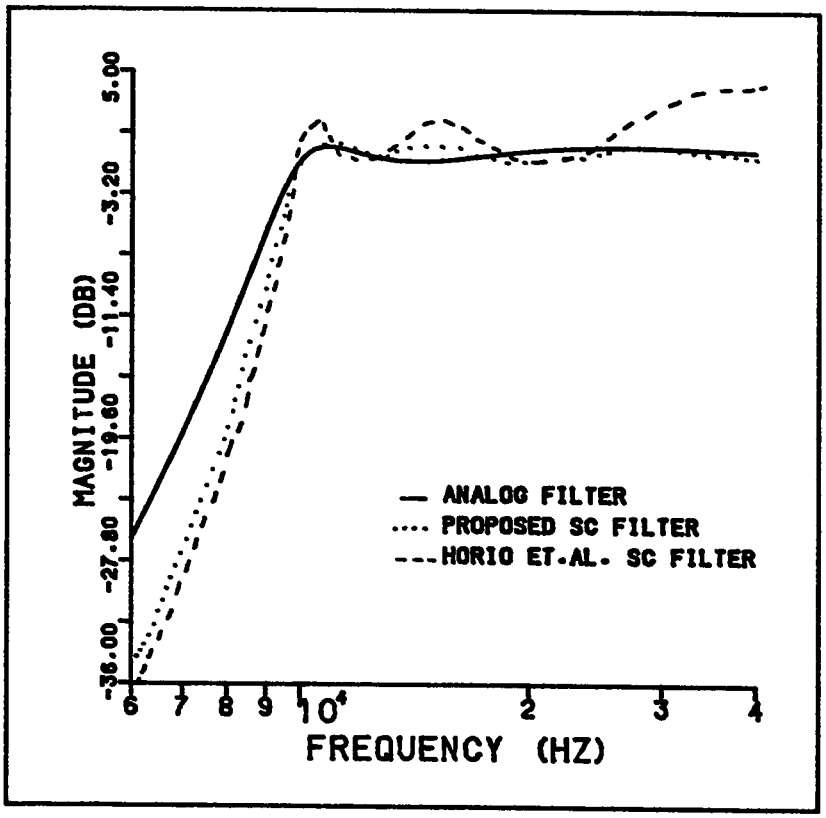
$C_{46} = 4.544C_u$

$C_{47} = 4.544C_u$

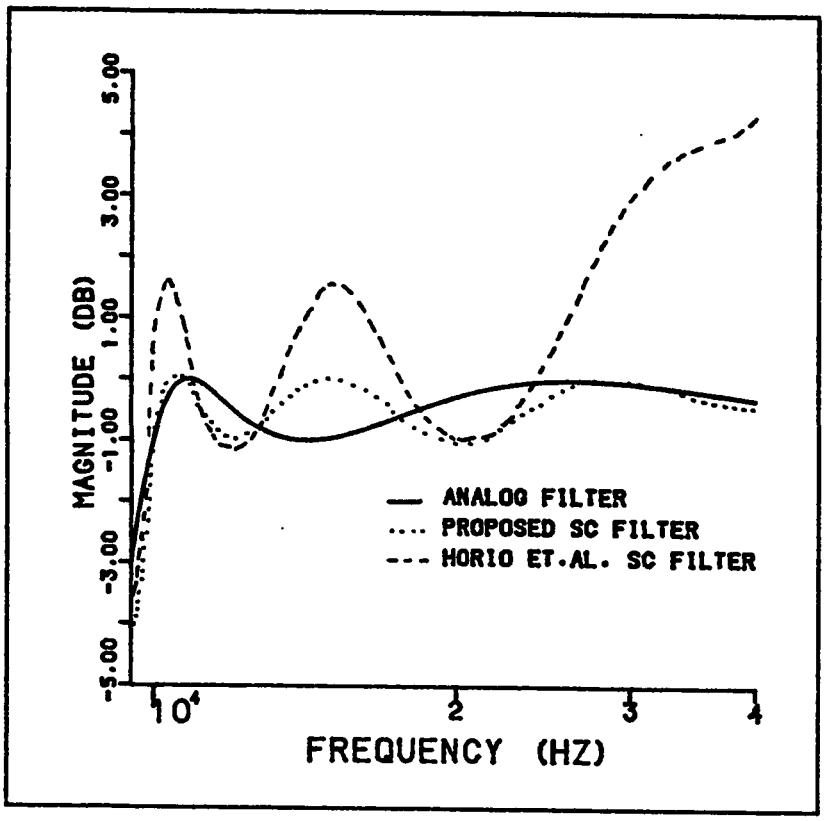
$C_{48} = 3.408C_u$

From the above normalized capacitance values, the total capacitance for the integrated circuit realization of the SC high-pass filter is calculated to be $107.13C_u$.

The simulated magnitude responses of the high-pass SC ladder filter using the proposed design and of that using Horio et. al.'s design are shown in Fig. 4.7. The magnitude response of the high-pass continuous ladder filter is plotted on the same graph for comparison. It can be observed that the proposed technique approximate the high-pass continuous ladder filter response much better than Horio et. al.'s realization, which used a parallel stray-sensitive SC feedback path for the resistive source termination. Furthermore, the reactive components have been realized by a differential op-amp which has a better performance at high frequencies[19] than a single output op-amp.



(a)



(b)

Figure 4.7 Simulated responses of design example.

Chapter V

A NEW TRANSFORMATION FOR THE DESIGN OF SWITCHED CAPACITOR HIGH-PASS LADDER FILTERS

In this chapter, a new transformation for the design of switched capacitor high-pass ladder filters is proposed. It will be shown that, by realizing the resistive source termination with a differential, delay-free op-amp, the magnitude response of the SC high-pass ladder filter will closely approximate its continuous counterpart. This new transformation has been named the modified bilinear transformation due to its resemblance to the well known bilinear transformation.

5.1 The Modified Bilinear Transformation

5.1.1 Definition and Mapping Properties

Consider the following transformation from the z-plane to the s-plane

$$s = \frac{2}{T} \cdot \frac{1-z^{-1/2}}{1+z^{-1/2}} = \frac{2}{T} \frac{z^{1/2}-1}{z^{1/2}+1} \qquad (5.1)$$

where 1/T is the sampling frequency. From the theory of complex variables, it is a known fact that the function $z^{1/2}$

is a double valued function. Therefore, every point on the z-plane, except the origin, is mapped onto two distinct points on the s-plane. This is obviously undesirable, because, if the discrete-time filters are to be derived from continuous-time filters, then a one-to-one correspondence should exist between poles(zeros) on the s-plane and poles(zeros) on the z-plane[31]. This means that the transformation given by Eq. (5.1) has to be defined such that a one-to-one mapping is accomplished from the s-plane to the z-plane. A second requirement is that Eq. (5.1) maps the interior of the unit circle on the z-plane onto the left half of the s-plane, so that stable analog filters results into stable discrete-time filters[31]. To satisfy the above requirements, we define the following mapping.

Let $w=z^{1/2}$ and $z=re^{j\theta}$. Then, there are exactly two different values of w corresponding to any choice of r, θ, given by

$$w_1 = r^{1/2} e^{j(\Theta/2)}, \qquad \text{for } -\pi < \Theta \leq \pi \tag{5.2a}$$

and

$$w_2 = r^{1/2} e^{j(\Theta/2+\pi)} = -w_1, \qquad \text{for } -\pi < \Theta \leq \pi \tag{5.2b}$$

where, for definiteness, $r^{1/2}$ is taken to be the positive

square root of r. The two functions, w_1 and w_2 are called the branches of w. By choosing a branch cut extending from 0 to $-\infty$, the two branches can be made analytic everywhere on the z-plane, except at the two points z=0 and $z=\infty$ If w_1 is taken as the desired branch, then a one-to-one mapping G(z) is established from the z-plane to the s-plane. The inverse mapping $G^{-1}(s)=z$ can be easily computed to be as follows:

$$z = \left[\frac{1+(T/2)s}{1-(T/2)s}\right]^2 \tag{5.3}$$

The mapping properties from the z-plane to the s-plane of this new transformation can best be described by first mapping the unit circle on the z-plane, corresponding to branch w_1, onto the w-plane. Since $w=z^{1/2}$, then the unit circle on the z-plane defined by the branch w_1, is mapped onto a semi-circle on the right hand side of the w-plane as shown in Fig. 5.1(a). The inner part of the unit circle on the z-plane is mapped into the inner part of this semi-circle. With the above definition of w, the transformation from the w-plane onto the s-plane is given by

$$s = \frac{2}{T}\frac{w-1}{w+1} \tag{5.4}$$

This is the well known bilinear transformation from the w-plane onto the s-plane whose mapping properties are described in detail in Fig. 5.1(b). It can be observed that the semi-circle located on the right hand side of the w-plane is mapped onto a semi-circle of radius 2/T located on the left hand side of the s-plane. The mapping from the z-plane to the s-plane can now be established by combining the two mappings shown in Fig. 5.1(a) and 5.1(b). This result is shown in Fig. 5.1(c). Therefore, the modified bilinear transformation maps the unit circle of the z-plane onto a part of the Ω-axis of the s-plane, namely $-2/T<\Omega<2/T$. This property of the modified bilinear transformation is similar to that of the LDI transformation. Furthermore, the inside of the unit circle on the z-plane is not completely mapped onto the left hand side of the s-plane, but into a semi-circle of radius 2/T. This implies, when defining the modified bilinear transformation in the above manner, that it is necessary to impose a constraint on the analog prototype of the SC high-pass ladder filter. Since the mapping of any stable pole in the s-plane outside the semi-circle of radius 2/T is not defined, the constraint should make sure that the poles and zeros of the continuous high-pass filter are inside this semi-circle.

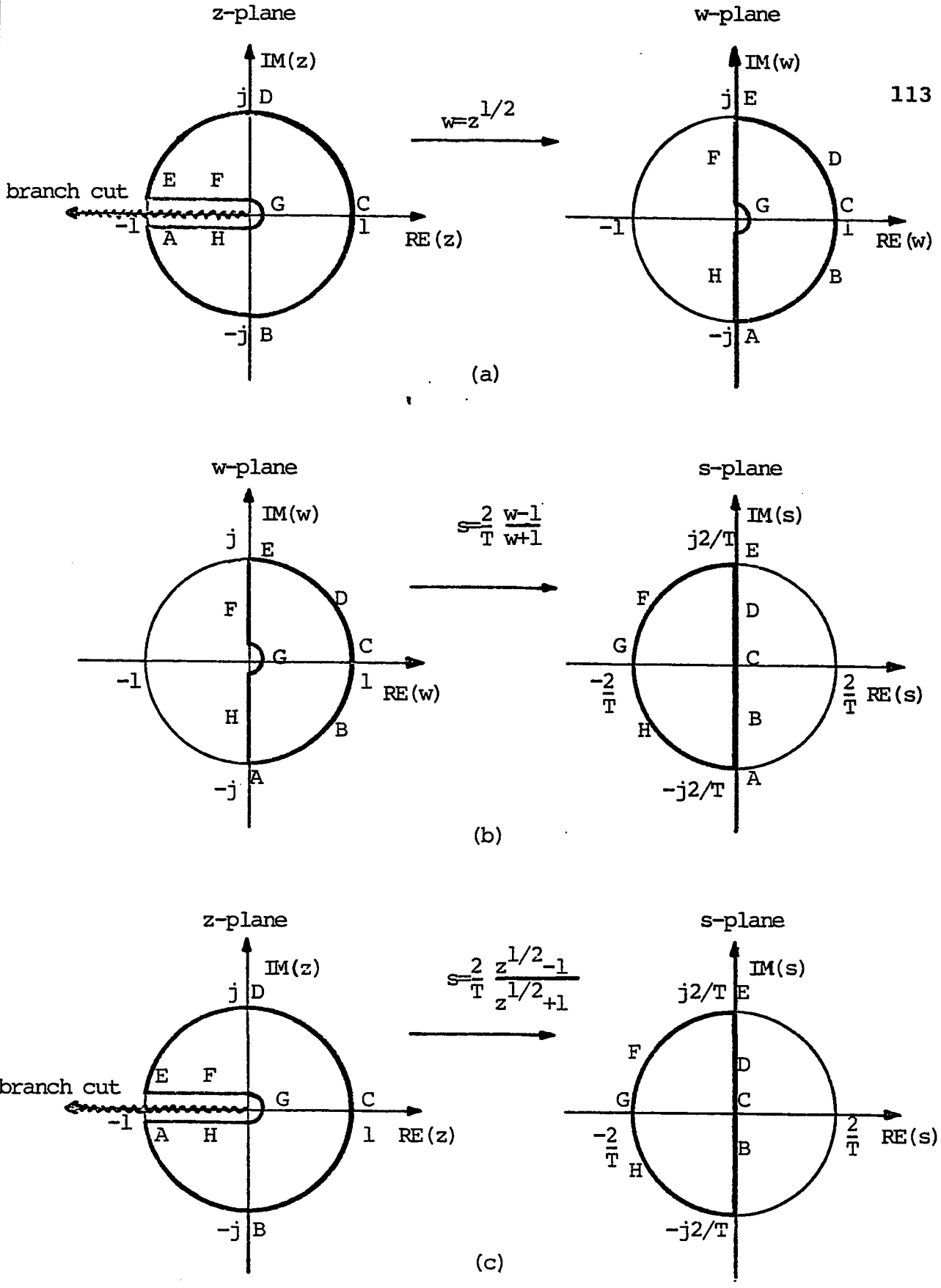


Figure 5.1 Mapping properties of the modified bilinear transformation.

5.1.2 Warping Effects

To see the effect of the modified bilinear transformation on the design of SC high-pass ladder filters, we let $s=\sigma+j\Omega$ and $z=\exp(jwT)$. Hence Eq. (5.1) becomes

$$\sigma + j\Omega = \frac{2}{T}\tan\left(\frac{wT}{4}\right) \tag{5.5}$$

where Ω and w are the continuous and discrete angular frequencies, respectively. Equating the real and imaginary parts of Eq. (5.5) gives

$$\sigma = 0 \text{ and } \Omega = \frac{2}{T}\tan\left(\frac{wT}{4}\right) \tag{5.6}$$

The plot of Eq. (5.6) in Fig. 5.2 shows the warping effect of the modified bilinear transformation. Note that, this curve is different from the curves showing the warping effect of the LDI, Bilinear and MLDD transformations in the sense that the continuous and discrete angular frequencies are almost linearly related between $wT=0$ and $wT=\pi$ with a slope of 0.542.

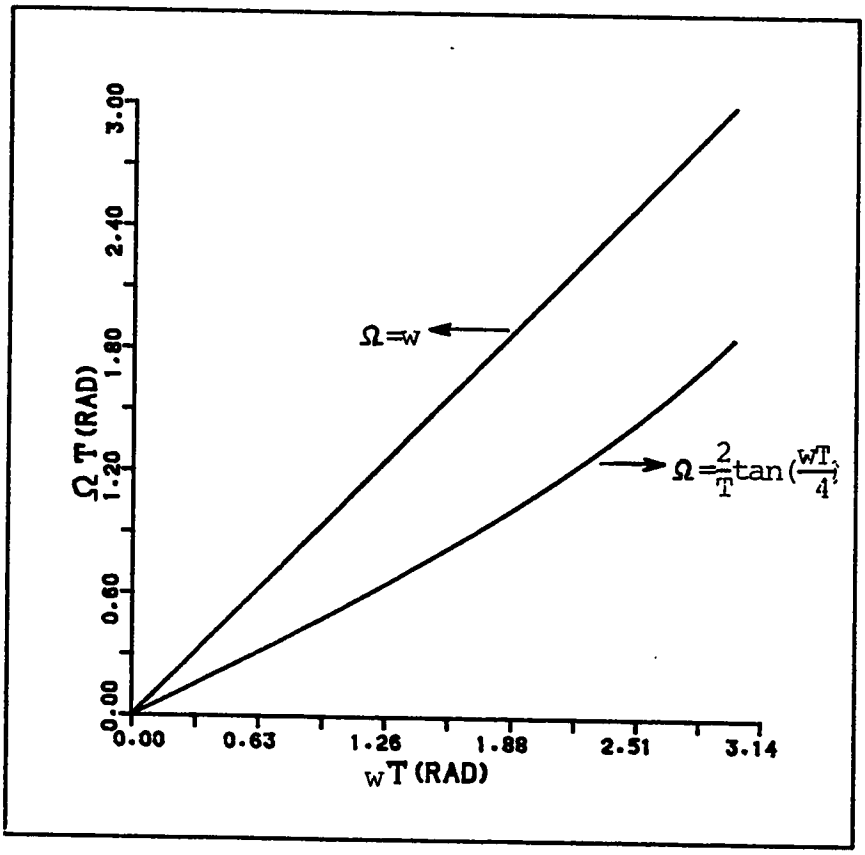


Figure 5.2 Warping effect of the modified bilinear transformation.

5.2 *Design Procedure*

The design procedure for switched capacitor high-pass ladder filters using the modified bilinear transformation is similar to the design procedure proposed in chapter 4, except for an extra condition in step 4 to make sure that the poles of the continuous high-pass filter are inside the semi-circle of radius 2/T.

We have investigated the use of the modified bilinear transformation in the design of SC high-pass ladder filters from analog proto-types for two classes of analog filters: Chebychev and Butterworth. From this investigation, the following observations can be made:

Since the poles of a continuous Butterworth high-pass filter lie on a circle of radius Ω_p [33], as long as the sampling frequency is chosen higher than the Nyquist rate, Eq. (5.6) guarantees that Ω_p will be less than 2/T. Therefore, for the design of SC high-pass Butterworth ladder filters, it is not necessary to compute the poles of the high-pass continuous ladder proto-type and the design procedure follows the same steps as proposed in chapter 4 without any constraint. On the other hand, the poles of a continuous low-pass Chebychev filter lie on an ellipse of minor axis sinh(a) and major axis cosh(a), where a is given by[38]

$$a = \left(\frac{1}{N}\right) \sinh^{-1}\left[\left(10^{0.1\,Amax}-1\right)^{-1/2}\right] \qquad (5.7)$$

In Eq. (5.7), N is the order of the filter and A_{max} is the maximum attenuation in the passband region. By the pole-reciprocity theorem[38], the poles of the high-pass continuous Chebychev filter are the reciprocal of the poles of the normalized low-pass continuous Chebychev filter multiplied by the factor Ω_p. Since sinh(a)<cosh(a), the reciprocal of these two functions become (1/sinh(a))>(1/cosh(a)). This implies that Ω_p/sinh(a)>Ω_p/cosh(a).

From the above discussion, we can conclude that, the worst case takes place when a pole of the high-pass continuous Chebychev filter is located at Ω_p/sinh(a). Therefore, this pole location can be taken as an upper-bound for 2/T. If the sampling frequency is chosen such that 2/T>Ω_p/sinh(a), then all the poles of the high-pass continuous Chebychev ladder filter will lie inside the semi-circle of radius 2/T. The above inequality can be utilized efficiently for hand-held calculations. However, if the designer has computer facilities available, he can do a better design by computing the location of the pole which is farthest from the origin and choosing 2/T larger than its magnitude. This computation is performed only for even order high-pass Chebychev filters, because for odd order filters, there is always a pole located at Ω_p/sinh(a).

5.3 *Building Block For Realizing the Modified Bilinear Transfer Function*

The modified bilinear transfer function can be defined as

$$H(z) = P \frac{1-z^{-1/2}}{1+z^{-1/2}} \tag{5.8}$$

where P is a constant.

We have realized this new transfer function by a fully differential op-amp as shown in Fig. 5.3. The analysis and derivation of the transfer function of this circuit is shown below.

The clock waveforms driving the two switches are shown in Fig. 1.2. For the analysis, we have assumed ideal switches and ideal fully-differential op-amps.

At t=(n-1/2)T, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 5.4(a). The application of the conservation of charge law at node N1 gives

$$V_{N1}^{e}(n-1/2) - V_{N1}^{o}(n-1) = \frac{C_1}{C_1+C_2+C_3}[V_1^{+e}(n-1/2) - V_1^{+o}(n-1)]$$

$$+ \frac{C_2}{C_1+C_2+C_3}[V_o^{-e}(n-1/2) - V_o^{-o}(n-1)] - \frac{C_3}{C_1+C_2+C_3} V_o^{+o}(n-1) \tag{5.9}$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 is shown in Fig. 5.4(b). The

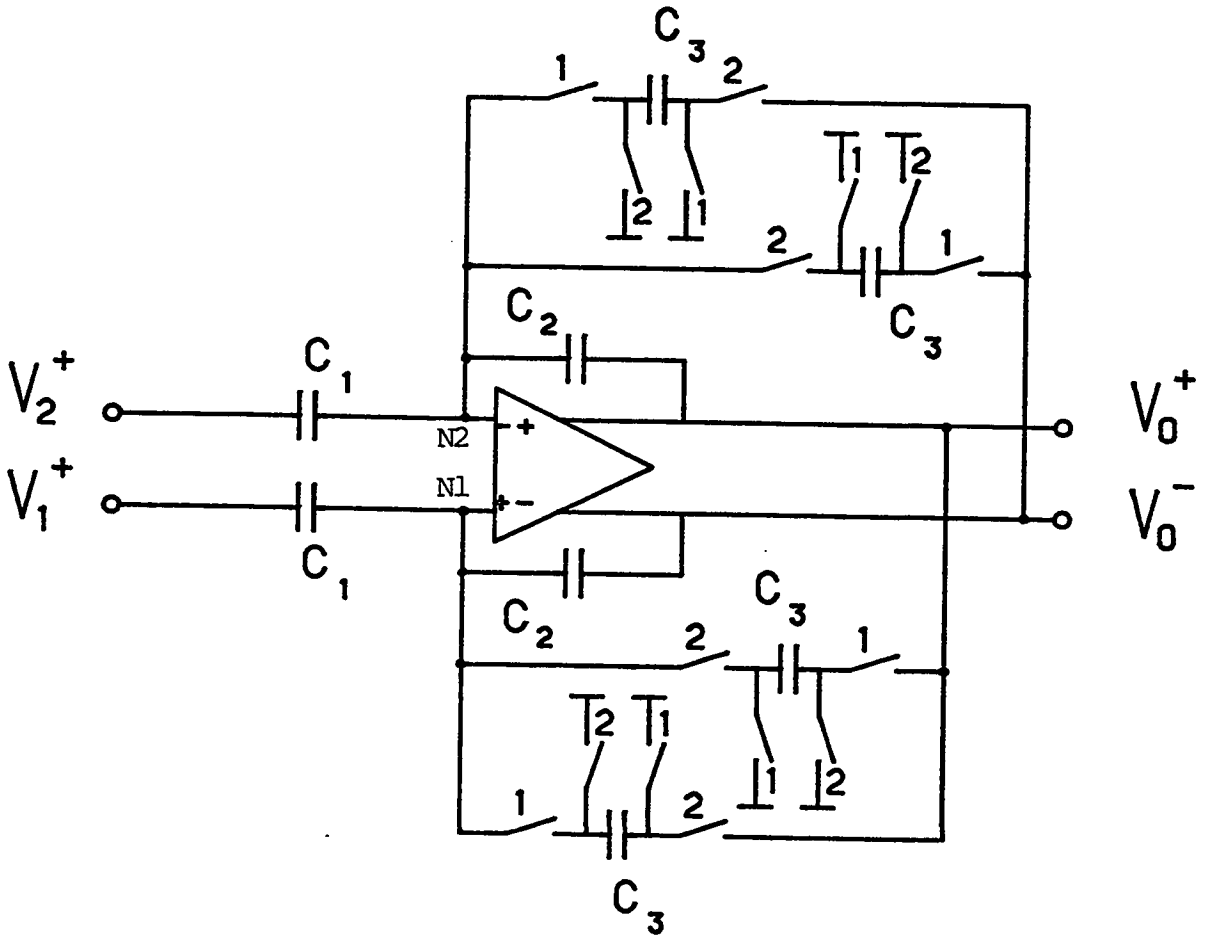


Figure 5.3 Stray-insensitive, fully differential building block for realizing the modified bilinear transfer function.

application of the conservation of charge law at node N2 yields

$$V_{N2}^{e}(n-1/2) - V_{N2}^{o}(n-1) = \frac{C_1}{(C_1+C_2+C_3)}[V_2^{+e}(n-1/2) - V_2^{+o}(n-1)]$$

$$+ \frac{C_2}{(C_1+C_2+C_3)}[V_o^{+e}(n-1/2) - V_o^{+o}(n-1)] - \frac{C_3}{(C_1+C_2+C_3)} V_o^{-o}(n-1) \qquad (5.10)$$

For an ideal differential op-amp, the voltage at the inverting input terminal, equals the voltage at the non-inverting input terminal. Hence, we can write

$$V_{N1}^{e}(n-1/2)-V_{N1}^{o}(n-1)=V_{N2}^{e}(n-1/2)-V_{N2}^{o}(n-1)$$

Therefore, equating Eq. (5.9) to Eq. (5.10) and simplifying, we obtain

$$C_1[V_1^{+e}(n-1/2) - V_1^{+o}(n-1)] + C_2[V_o^{-e}(n-1/2) - V_o^{-o}(n-1)] - C_3 V_o^{+o}(n-1)$$

$$= C_1[V_2^{+e}(n-1/2) - V_2^{+o}(n-1)] + C_2[V_c^{+e}(n-1/2) - V_o^{+o}(n-1)] - C_3 V_o^{-o}(n-1) \qquad (5.11)$$

Substituting $V_i^{+}=-V_i^{-}=V_i$ for i=0,1,2 and taking the z-transform of both sides of equation (5.11) gives

$$C_1\{[z^{-1/2}V_1^e(z) - z^{-1}V_1^o(z)] - [z^{-1/2}V_2^e(z) - z^{-1}V_2^o(z)] \quad (5.12)$$

$$= 2C_2[z^{-1/2}V_o^e(z) - z^{-1}V_o^o(z)] + 2C_3z^{-1}V_o^o(z)$$

Choosing $C_3=2C_2$ and substituting in Eq. (5.12), after simplification, we obtain

$$C_1\{[(V_1^e(z) - z^{-1/2}V_1^o(z)] - [V_2^e(z) - z^{-1/2}V_2^o(z)]\} = 2C_2[V_o^e(z) + z^{-1/2}V_o^o(z)] \quad (5.13)$$

At t=nT, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 5.4(c). The application of the conservation of charge law at node N1 gives

$$V_{N1}^o(n-1) - V_{N1}^e(n-1/2) = \frac{C_1}{(C_1+C_2+C_3)}[V_1^{+o}(n) - V_1^{+e}(n-1/2)]$$

$$+ \frac{C_2}{(C_1+C_2+C_3)}[V_o^{-o}(n) - V_o^{-e}(n-1/2)] - \frac{C_3}{(C_1+C_2+C_3)}V_o^{+e}(n-1/2) \quad (5.14)$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 becomes as shown in Fig. 5.4(d). Applying the conservation of charge law at node N2 yields

$$V_{N2}^{o}(n) - V_{N2}^{e}(n-1/2) = \frac{C_1}{(C_1+C_2+C_3)}[V_2^{+o}(n) - V_2^{+e}(n-1/2)$$

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$$+ \frac{C_2}{(C_1+C_2+C_3}\,[V_o^{+o}(n) - V_o^{+e}(n-1/2)] - \frac{C_3}{(C_1+C_2+C_3)}\,V_o^{-e}(n-1/2) \qquad (5.15)$$

Equating (5.14) to (5.15) under an ideal op-amp assumption and simplifying, we obtain

$$C_1[V_1^{+o}(n) - V_1^{+e}(n-1/2)] + C_2[V_o^{-o}(n) - V_o^{-e}(n-1/2)] - C_3\,V_o^{e+}(n-1/2)$$

$$= C_1[V_2^{+o}(n) - V_2^{+e}(n-1/2)] + C_2[V_o^{+o}(n) - V_o^{+e}(n-1/2)] - C_3\,V_o^{-e}(n-1/2) \qquad (5.16)$$

Substituting $V_i^{+}=-V_i^{-}=V_i$ for i=0,1,2 and taking the z-transform of both sides of equation (5.16) gives

$$C_1\{[V_1^{o}(z) - z^{-1/2}V_1^{e}(z)] - [V_2^{o}(z) - z^{-1/2}V_2^{e}(z)]\}$$

$$= 2C_2[V_o^{o}(z) + z^{-1/2}V_o^{e}(z)] \qquad (5.17)$$

Adding equation (5.13) to (5.17) and simplifying, we obtain

$$C_1\{[V_1^{o}(z) + V_1^{e}(z)] - [V_2^{o}(z) + V_2^{e}(z)]\}(1-z^{-1/2})$$

$$= 2C_2\{(V_o^{o}(z) + V_o^{e}(z))(1+z^{-1/2}) \qquad (5.18)$$

Defining

$$H(z) = \frac{V_o^{o}(z) + V_o^{e}(z)}{[(V_1^{o}(z)+V_1^{e}(z)) - (V_2^{o}(z)+V_2^{e}(z))]} \qquad (5.19)$$

and using Eq. (5.18) we obtain

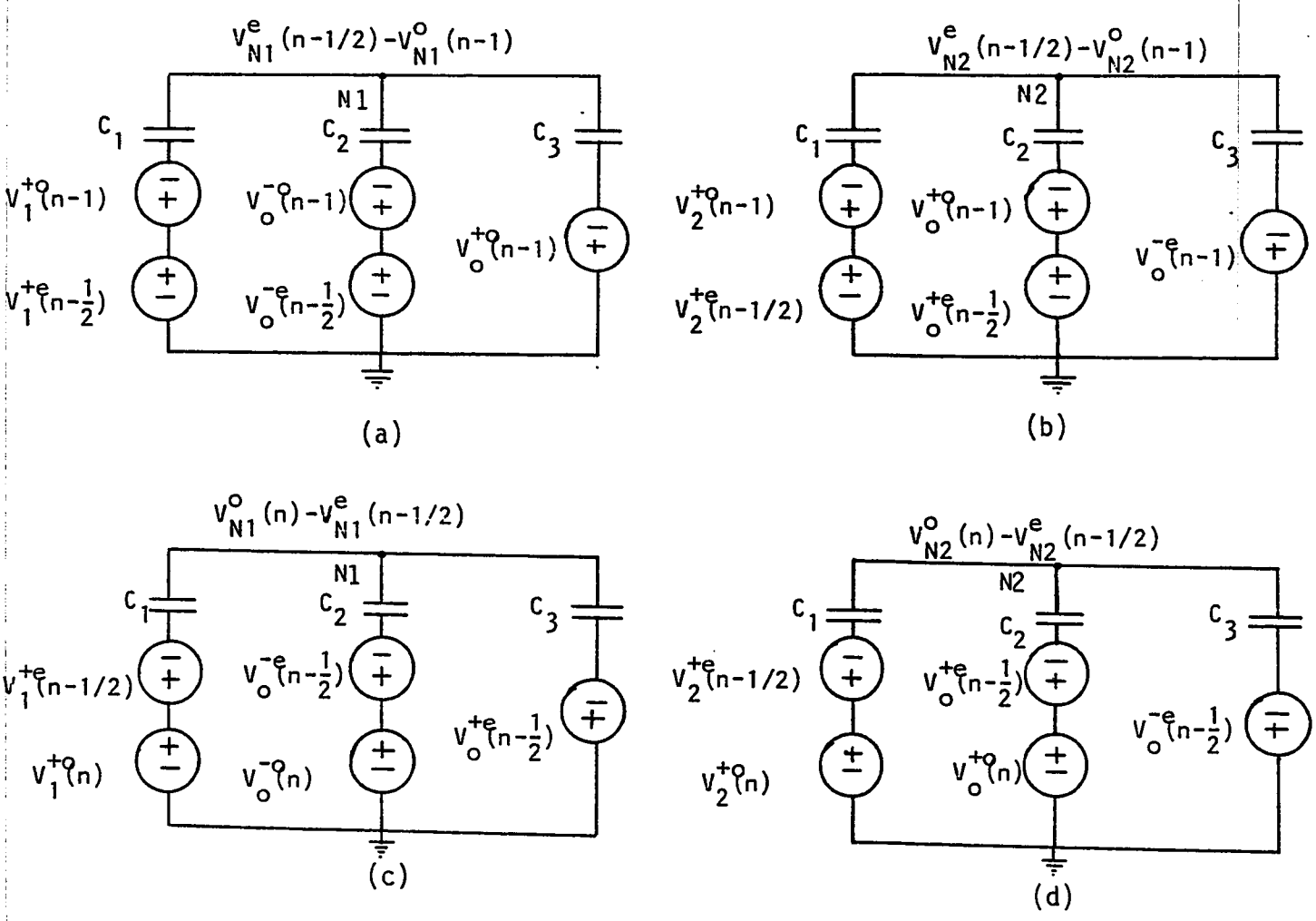


Figure 5.4 Equivalent circuit for the charge distribution of Fig. 5.3: (a) at node N1 when t=(n-1/2)T (b) at node N2 when t=(n-1/2)T (c) at node N1 when t=nT (d) at node N2 when t=nT

$$H(z) = \frac{V_o(z)}{V_1(z) - V_2(z)} = \frac{C_1}{2C_2} \frac{(1-z^{-1/2})}{(1+z^{-1/2})} \qquad (5.20)$$

which becomes the modified bilinear transfer function with $P=C_1/2C_2$. This implies that sampling the output of the SC circuit shown in Fig. 5.3 both at the even and the odd clock phases realizes the modified bilinear transfer function.

5.4 Building Block For Realizing the Resistive Source Termination

Consider the SC circuit shown in Fig. 5.5, which is proposed for the realization of the resistive source termination in the design of SC high-pass ladder filters using the modified bilinear transformation.

At t=(n-1/2)T, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 5.6(a). The application of the conservation of charge law at node N1 gives

$$C_1[V_1^{+e}(n-1/2) - V_1^{+o}(n-1)] + C_2[V_o^{-e}(n-1/2) - V_o^{-o}(n-1)]$$

$$-C_2V_o^{-o}(n-1) = (C_1+C_2+C_2)[V_{N1}^{e}(n-1/2) - V_{N1}^{o}(n-1)] \qquad (5.21)$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 is shown in Fig. 5.6(b). The application of the conservation of charge law at node N2

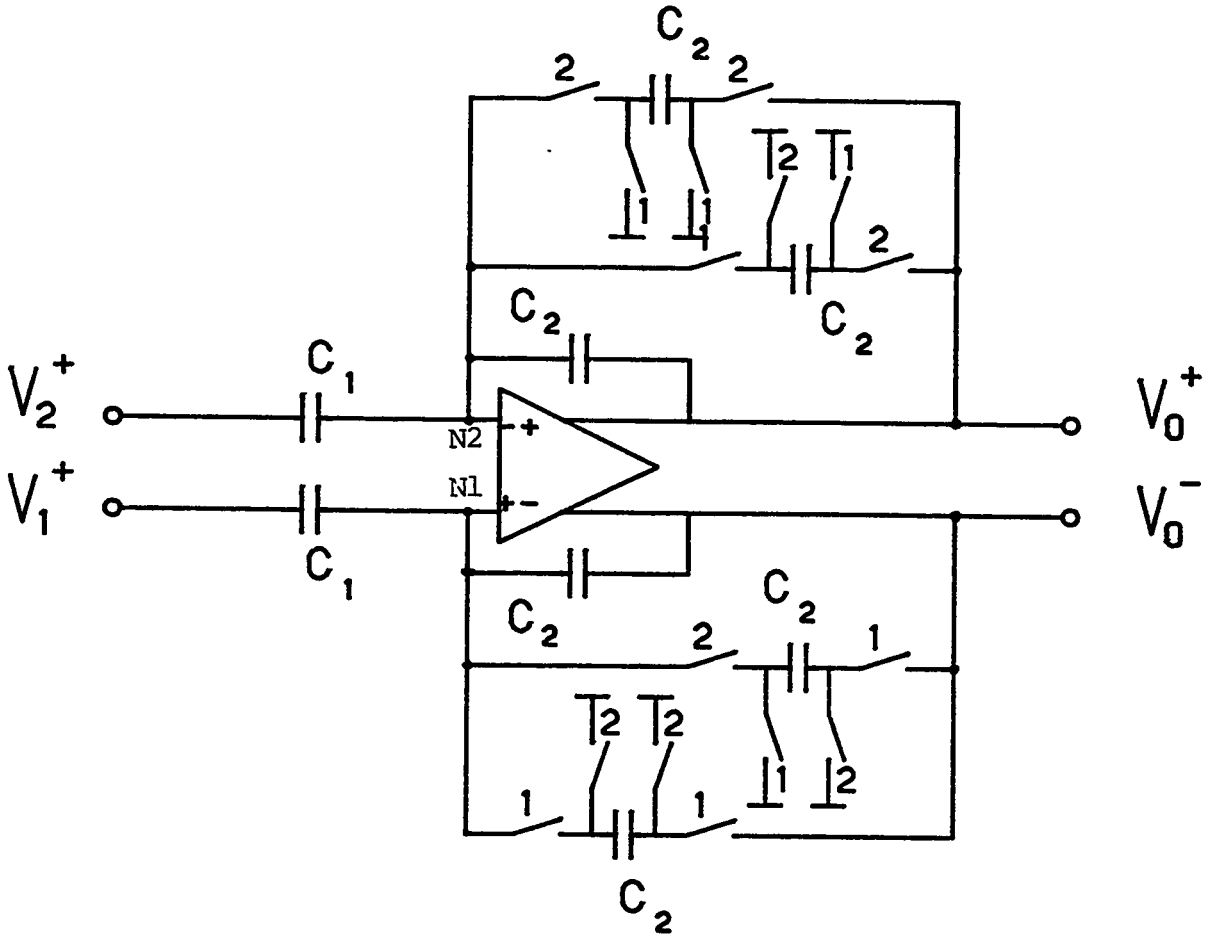


Figure 5.5 Stray-insensitive op-amp for realizing the resistive source termination to be used in the design of SC high-pass ladder filters using the modified bilinear transformation.

yields

$$C_1[V_2^{+e}(n-1/2) - V_2^{+e}(n-1)] + C_2[V_o^{+e}(n-1/2) - V_o^{+o}(n-1)$$

$$+C_2V_o^{+e}(n-1/2) = (C_1+C_2+C_2)[V_{N2}^{e}(n-1/2) - V_{N2}^{o}(n-1)] \qquad (5.22)$$

For an ideal differential op-amp, the voltage at the inverting input terminal equals the voltage at the non-inverting input terminal. Hence, we can write

$$V_{N1}^{e}(n-1/2)-V_{N1}^{o}(n-1)=V_{N2}^{e}(n-1/2)-V_{N2}^{o}(n-1)$$

Therefore, equating Eq. (5.21) to Eq. (5.22), we obtain

$$C_1[V_1^{+e}(n-1/2) - V_1^{+o}(n-1)] + C_2[V_o^{-e}(n-1/2) - V_o^{-o}(n-1)] - C_2V_o^{-o}(n-1)$$

$$= C_1[V_2^{+e}(n-1/2) - V_2^{+o}(n-1)] + C_2V_o^{+e}(n-1/2) + C_2[V_o^{+e}(n-1/2) - V_o^{+o}(n-1) \qquad (5.23)$$

Substituting $V_i^{+}=-V_i^{-}=V_i$ for i=0,1,2 and taking the z-transform of both sides of equation (5.23) gives

$$C_1\{[V_1^{e}(z)z^{-1/2} - z^{-1}V_1^{o}(z)] - [z^{-1/2}V_2^{e}(z) - z^{-1}V_2^{o}(z)]\}$$

$$= 3C_2[z^{-1/2}V_o^{e}(z) - z^{-1}V_o^{o}(z)] \qquad (5.24)$$

At t=nT, the equivalent circuit for the charge distribution at node N1 becomes as shown in Fig. 5.6(c). The application of the conservation of charge law at node N1 gives

$$C_1[V_1^{+o}(n) - V_1^{+e}(n-1/2)] + C_2[V_o^{-o}(n) - V_o^{-e}(n-1/2)] + C_2V_o^{-o}(n)$$

$$= (C_1+C_2+C_2)[V_{N1}^{o}(n) - V_{N1}^{e}(n-1/2)] \qquad (5.25)$$

For the inverting input, the equivalent circuit for the charge distribution at node N2 becomes as shown in Fig. 5.6(d). Applying the conservation of charge law at node N2 yields

$$C_1[V_2^{+o}(n) - V_2^{+e}(n-1/2) - C_2V_o^{e+}(n-1/2) + C_2[V_o^{+o}(n) - V_o^{+e}(n-1/2)]$$

$$= (C_1+C_2+C_2)[V_{N2}^{o}(n) - V_{N2}^{e}(n-1/2)] \qquad (5.26)$$

Equating (5.25) to (5.26) under an ideal op-amp assumption, we obtain

$$C_1[V_1^{+o}(n) - V_1^{+e}(n-1/2)] + C_2V_o^{-o}(n) + C_2[V_o^{-o}(n) - V_o^{-e}(n-1/2)]$$

$$= C_1[V_2^{+o}(n) - V_2^{+e}(n-1/2)] - C_2V_o^{+e}(n-1/2) + C_2[V_o^{+o}(n) - V_o^{+e}(n-1/2)] \qquad (5.27)$$

Substituting $V_i^{+}=-V_i^{-}=V_i$ for i=0,1,2, and taking the z-transform of both sides of equation (5.27) gives

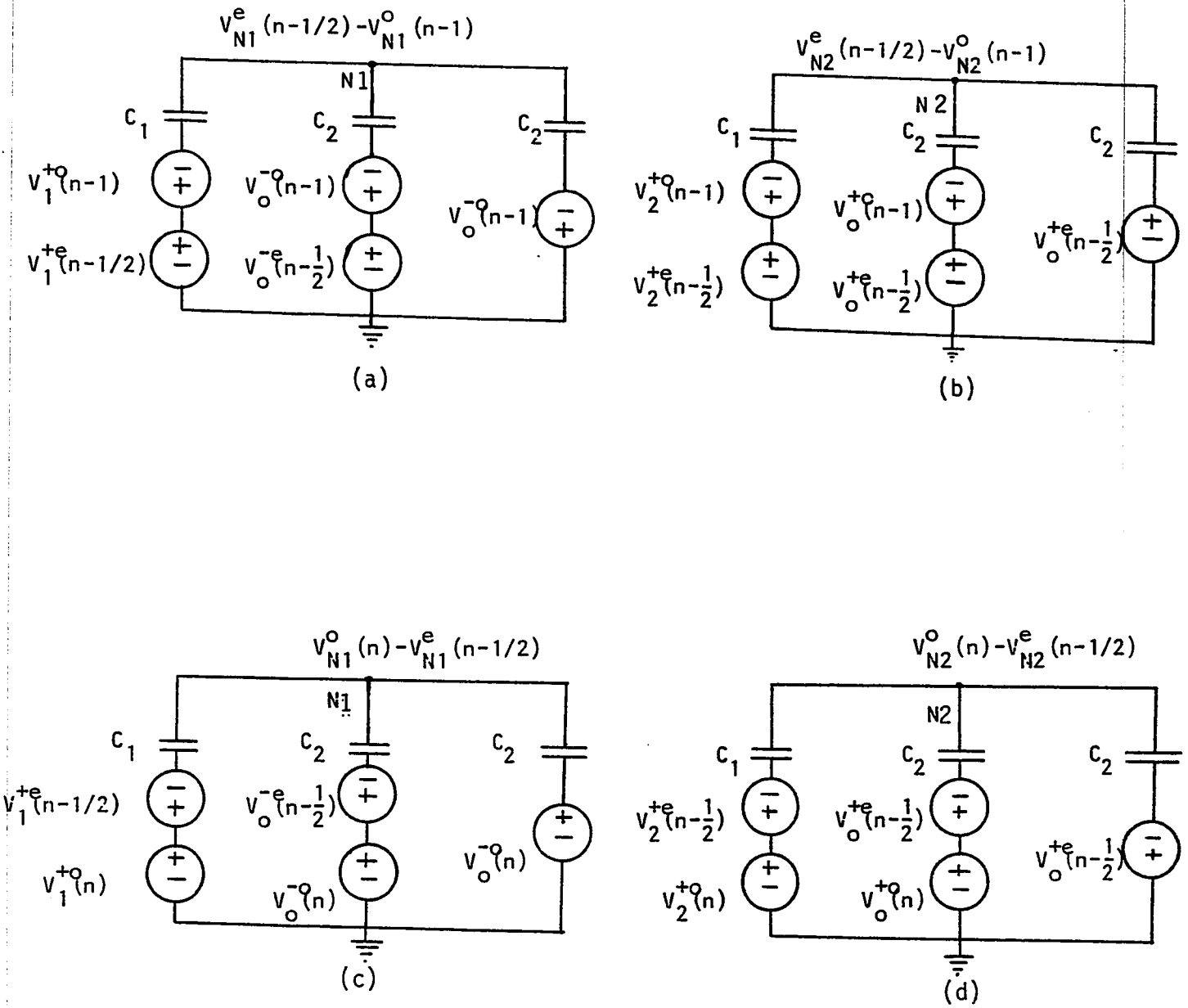


Figure 5.6 Equivalent circuit for the charge distribution of Fig. 5.5: (a) at node N1 when t=(n-1/2)T (b) at node N2 when t=(n-1/2)T (c) at node N1 when t=nT (d) at node N2 when t=nT

$$C_1\{[V_1^o(z) - z^{-1/2}V_1^e(z)] - [V_2^o(z) - z^{-1/2}V_2^e(z)]\} = 3C_2[V_o^o(z) - z^{-1/2}V_o^e(z)] \quad (5.28)$$

Adding equation (5.24) to (5.28) and simplifying, we obtain

$$C_1\{[V_1^o(z) + V_1^e(z)] - [V_2^o(z) + V_2^e(z)]\}(1-z^{-1/2})$$

$$= 3C_2[V_o^o(z) + V_o^e(z)](1-z^{-1/2}) \quad (5.29)$$

Therefore, the transfer function of this circuit can be written as

$$H(z) = \frac{C_1}{3C_2} = \frac{V_o^e(z) + V_o^o(z)}{\{[V_1^e(z)+V_1^o(z)] - [V_2^e(z)+V_2^o(z)]\}} = \frac{V_o(z)}{V_1(z) - V_2(z)} \quad (5.30)$$

Equation (5.30) is similar to the transfer function of a differential amplifier of constant gain $C_1/3C_2$. This makes it suitable for the realization of the source termination in the design of SC high-pass ladder filters using the modified bilinear transformation. To distinguish the capacitance ratios of the building block for the resistive source termination from those of the reactive components, we shall use C_{RS1} and C_{RS2} instead of C_1 and C_2 respectively, as the capacitances of the resistive source termination.

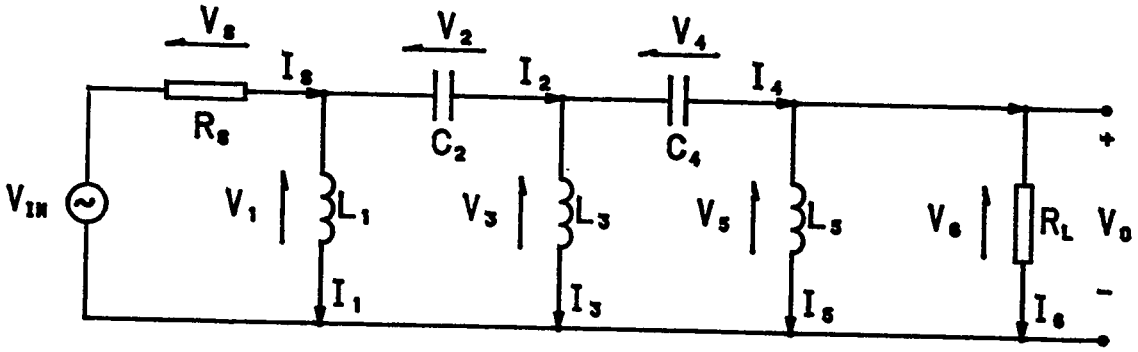
5.5 *Design Example*

Consider the design of a high-pass SC Chebychev filter using the folowing specifications:

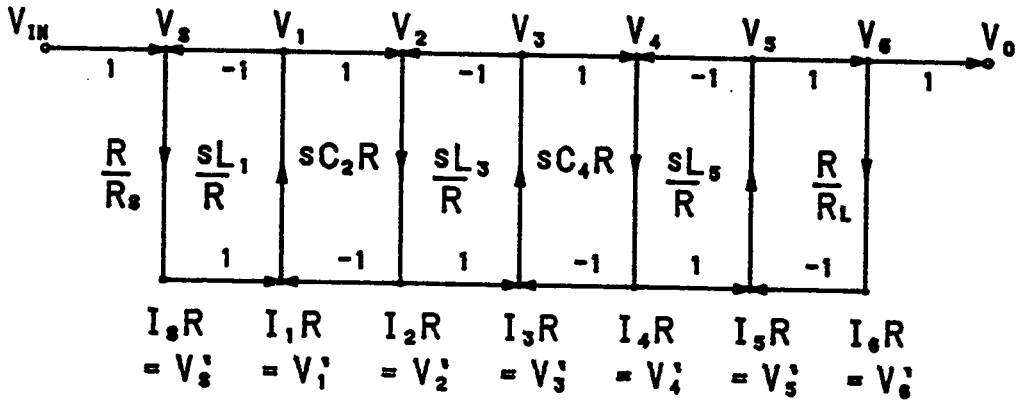
A_{max}=1 dB, A_{min}=25 dB, f_p=10 kHz (or w_p=62.83 krad/sec), f_s=6.5 kHz (or w_s=40.84 krad/sec), 1/T=80 kHz.

Using the design procedure described in section 4.1, the order of the filter is found to be 5. For the above value of sampling frequency all the poles of the high-pass continuous ladder filter lie inside the semi-circle of radius 2/T. The circuit for the prewarped continuous high-pass ladder filter and its corresponding SFG are shown in Fig. 5.7(a) and 5.7(b), respectively. Realizing the source termination with the building block circuit shown in Fig. 5.5 and the reactive components with the circuit shown in Fig. 5.3, the SC filter required to meet the given specifications is obtained and shown in Fig. 5.8.

By the same argument applied in the design example in chapter 4, the gain of the transfer function of the SC building block realizing the resistive source termination, given by Eq. (5.31), is equated to R/R_s. For an odd order continuous Chebychev high-pass filter, the load resistance R_L is 1 Ohm. Hence, the capacitance ratio becomes



(a)



(b)

Figure 5.7 (a) Fifth order high-pass continuous Chebychev ladder filter. (b) SFG of 5.7(a).

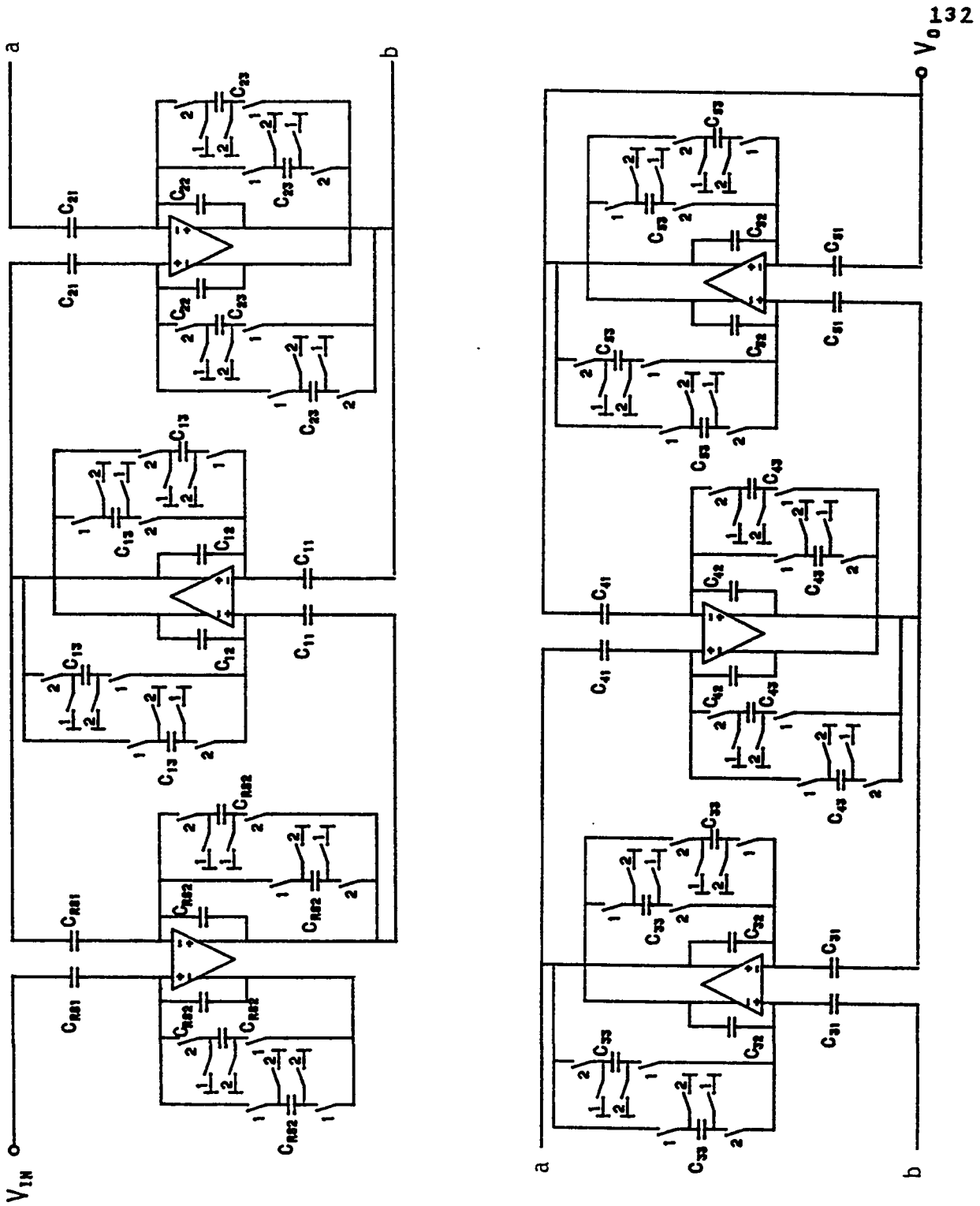


Figure 5.8 Fifth order SC high-pass Chebychev ladder filter based on the modified bilinear transformation.

$$\frac{C_{RS1}}{C_{RS2}} = \frac{3R}{R_s} = 3.00 \tag{5.31}$$

The capacitance ratios of the reactive components can be calculated by equating the gain of each reactive component of the SFG to the gain of the modified bilinear transfer function as given in Eq. (5.20). This results in the following capacitance ratios for the reactive sections:

$$\frac{C_{11}}{C_{12}} = \frac{4L_1}{RT} = 4.709 \tag{5.32}$$

$$\frac{C_{21}}{C_{22}} = \frac{4RC_2}{T} = 9.215 \tag{5.33}$$

$$\frac{C_{31}}{C_{32}} = \frac{4L_3}{RT} = 3.35 \tag{5.34}$$

$$\frac{C_{41}}{C_{42}} = \frac{4RC_4}{T} = 9.215 \tag{5.35}$$

$$\frac{C_{51}}{C_{52}} = \frac{4L_5}{RT} = 4.709 \tag{5.36}$$

Capacitance values C_{13}, C_{23}, C_{33}, C_{43} and C_{53} can be calculated using the relation $C_{i3}=2C_{i2}$. As was mentioned earlier, in SC filter design, the capacitance values are normalized with respect to the smallest capacitance in the circuit. For SC ladder filters, the normalized capacitances are cal-

culated for each section separately. For the above design example the normalized capacitances have been calculated to be as follows:

Normalized Capacitances for the source termination

$$C_{RS1} = 3.0C_u$$

$$C_{RS2} = C_u$$

Normalized Capacitances for the Section No: 1

$$C_{11} = 4.709C_u$$

$$C_{12} = C_u$$

$$C_{13} = 2.00C_u$$

Normalized Capacitances for the Section No: 2

$$C_{21} = 9.215C_u$$

$$C_{22} = C_u$$

$$C_{23} = 2.00C_u$$

Normalized Capacitances for the Section No: 3

$$C_{31} = 3.350C_u$$

$$C_{32} = C_u$$

$$C_{33} = 2.00C_u$$

Normalized Capacitances for the Section No: 4

$$C_{41} = 9.215C_u$$

$$C_{42} = C_u$$

$$C_{43} = 2.00C_u$$

Normalized Capacitances for the Section No: 5

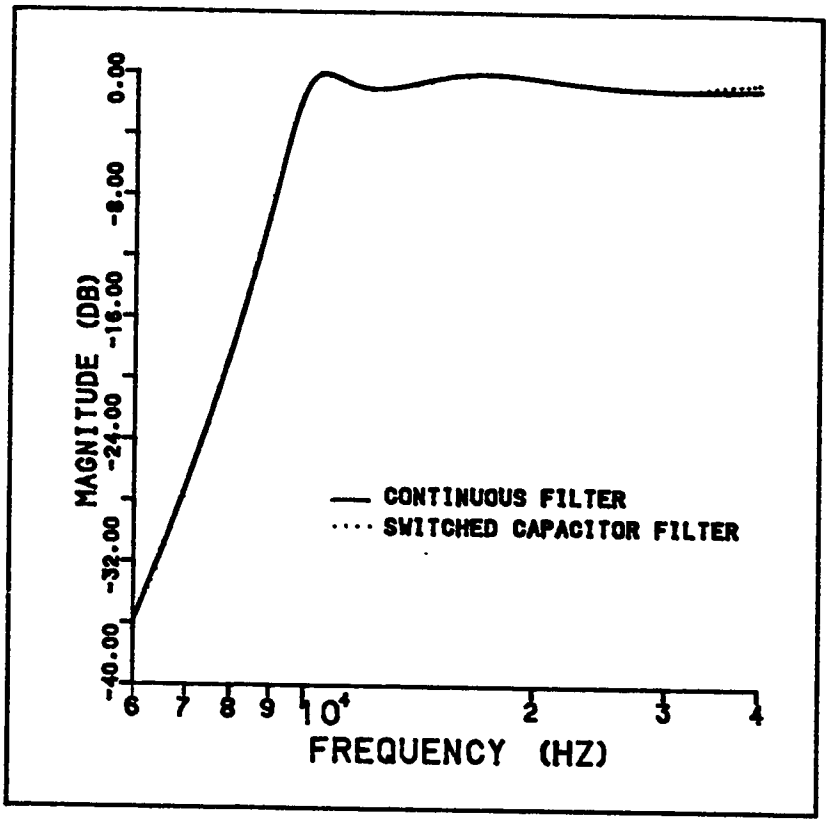
$$C_{51} = 4.709C_u$$

$$C_{52} = C_u$$

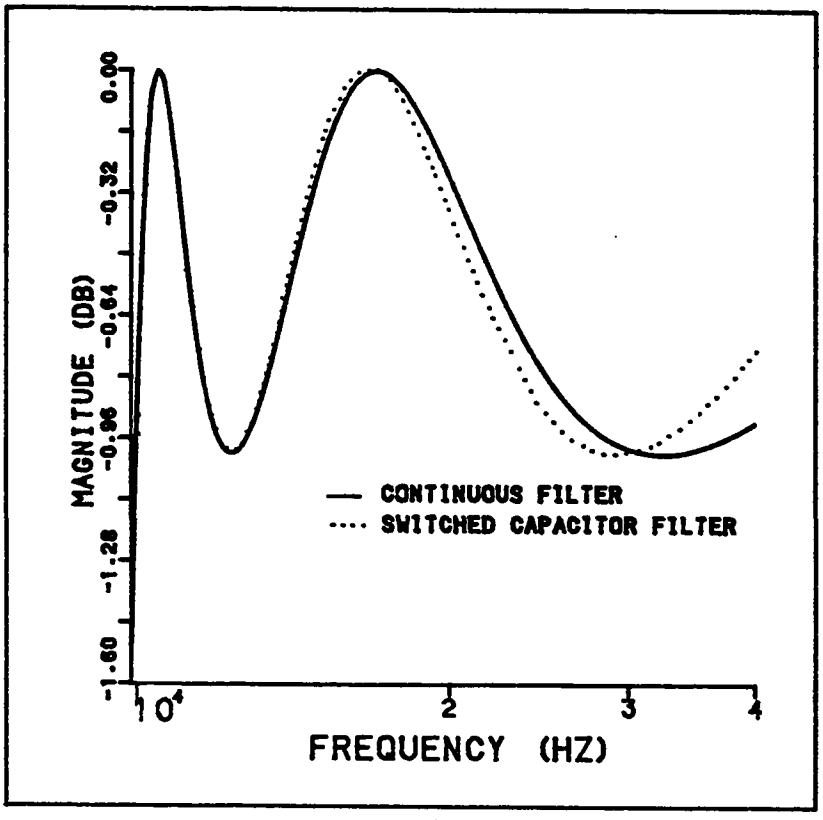
$$C_{53} = 2.00C_u$$

From the above normalized capacitance values, the total capacitance for the integrated circuit realization of the SC high-pass filter is calculated to be $124.4C_u$.

The simulated magnitude responses of the high-pass SC ladder filter using the proposed design technique is shown in Fig. 5.9. The magnitude response of the high-pass continuous ladder filter is plotted on the same graph for comparison. It can be observed that with the proposed technique the new transformation gives very accurate results and the response of the high-pass SC filter becomes almost the same as the continuous ladder filter response.



(a)



(b)

Figure 5.9 (a),(b) Simulated responses of design example.

Chapter VI

AN INTERACTIVE PACKAGE FOR DESIGNING SWITCHED CAPACITOR HIGH-PASS LADDER FILTERS

6.1 Description of Package

In this chapter we shall demonstrate the use of the interactive package that we have prepared for the design of switched capacitors high-pass ladder filters using the MLDD and the modified bilinear transformations. The package is based on the procedure proposed in chapters 4 and 5. Two classes of filters are handled in this package: Butterworth and Chebychev. The program requests for the high-pass filter parameters and it provides all the necessary design information for the user. In addition to this, the program gives the magnitude and phase responses of the switched capacitor and continuous filter prototype and it draws the circuit of the resulting SC high-pass filter.

The package which performs the main design, has been named as HPSC1. The compilation and running of the program should be done under the PLOTSYS system. In order to observe the magnitude and phase response, the computer terminal used must have a color display capability. A second program named as HPSC2 provides the user with the magnitude and

phase response of the filter whose design parameters were provided via the program HPSC1. This program was written to avoid the user from entering the same data to the package HPSC1 in order to observe the responses in detail. Therefore, once the desired parameters are provided to the package HPSC1, the user can observe the magnitude and phase response to any extent by adjusting the window data of the PLOTSYS menu and using the program HPSC2. Furthermore, the program writes all the necessary information in an output file which has also been named as HPSC1. Some of this information is also shown on the screen interactively.

In chapter 5, we have mentioned that, in the design of SC high-pass ladder filters using the modified bilinear transformation, the sampling frequency should be chosen such that the poles of the high-pass continuous filter lie inside the semi-circle of radius 2/T. This package takes care of this constraint and gives a warning message whenever the above condition is not satisfied. The next section describes the interactive use of the package.

6.2 Using the Package

Suppose that we have been asked to design a switched capacitor high-pass Chebychev ladder filter using the modified bilinear transformation using the following specifications: A_{min}=20 dB, A_{max}=0.5 dB, f_p=5 KHz, f_s=2 KHz, 1/T=100 KHz.

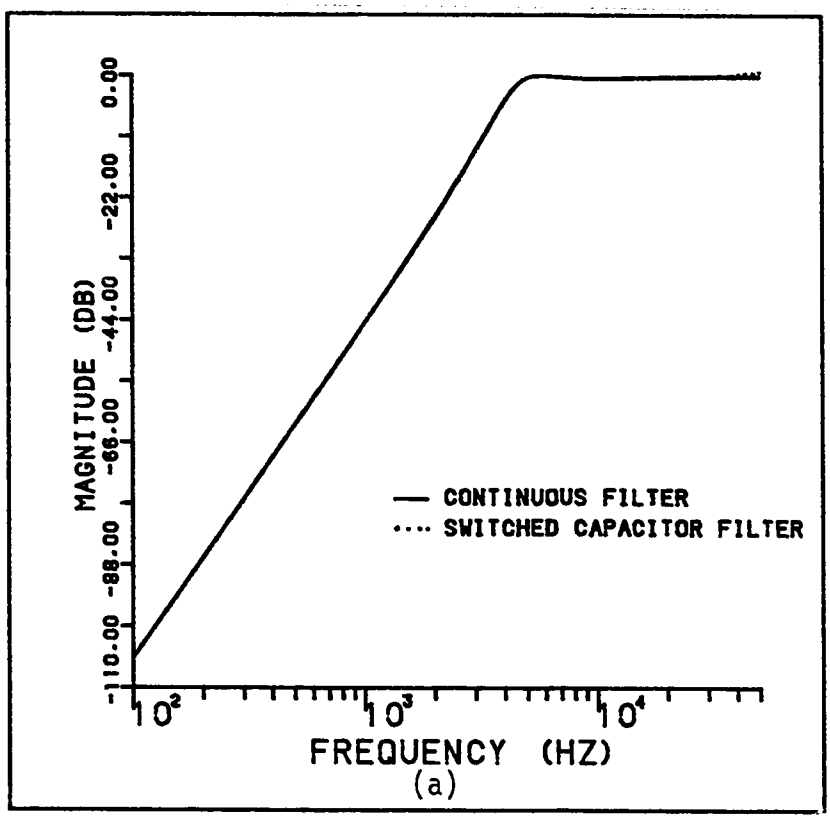
Furthermore, suppose that we would like to observe the magnitude and phase response from 4800 Hz to 50 KHz in increments of 200 Hz. Once we run the HPSC1 program on the PLOTSYS menu, the package will request for the above parameters in the following manner:

```
    HELLO.  WELCOME TO FIDANBOYLU'S PACKAGE
    FOR DESIGNING HIGH PASS SWITCHED CAPACITOR
              LADDER FILTERS.
    PLEASE ENTER THE FOLLOWING PARAMETERS
    AMIN = MINIMUM STOPBAND ATTENUATION IN DB.
?
  20.0
    AMAX = MAXIMUM PASSBAND ATTENUATION IN DB.
?
  0.5
    FP   = PASSBAND EDGE FREQUENCY IN HERTZ.
?
  5000.0
    FS   = STOPBAND EDGE FREQUENCY IN HERTZ.
?
  2000.0
    FSAMP= SAMPLING FREQUENCY IN HERTZ.
?
  100.E3
    WHAT TYPE OF FILTER DESIGN DO YOU NEED?
    TYPE 1 FOR BUTTERWORTH AND 2 FOR CHEBYCHEV.
?
```

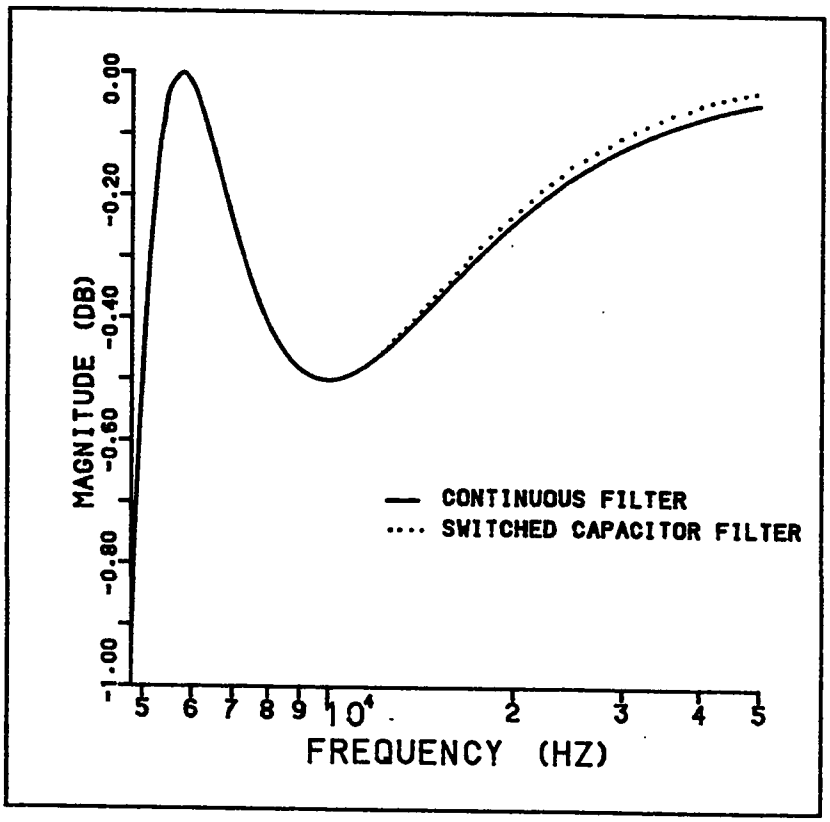
```
 2

   WHAT TYPE OF TRANSFORMATION DO YOU WANT?
   TYPE 1 FOR MLDD AND 2 FOR MBIL.

?

 2

   ORDER OF THE FILTER = 3
   THE HALF POWER FREQ. OF THE HP CONT. FILTER IS =
   0.1348E+05 RAD/SEC

   NORMALIZED CAPACITANCES FOR THE SOURCE TERMINATION
   CRS1 =    3.000000 CU
   CRS2 =    1.000000 CU
   NORMALIZED CAPACITANCES FOR SECTION NO:  1
   C(11) =   15.919755 CU
   C(12) =    1.000000 CU
   C(13) =    2.000000 CU

   NORMALIZED CAPACITANCES FOR SECTION NO:  2
   C(21) =   23.171890 CU
   C(22) =    1.000000 CU
   C(23) =    2.000000 CU

   NORMALIZED CAPACITANCES FOR SECTION NO:  3
   C(31) =   15.919755 CU
   C(32) =    1.000000 CU
   C(33) =    2.000000 CU

   THE TOTAL CAPACITANCE FOR THE SC FILTER =  152.022799 CU

   DO YOU WANT TO SEE THE MAGNITUDE AND PHASE RESPONSE?
```

```
    IF YES TYPE 1 OTHERWISE TYPE 0
?    1
     PLEASE ENTER THE FOLLOWING PARAMETERS.
     FINT = INITIAL FREQUENCY FOR PLOTTING(IN HERTZ)
?
  4800.0
     FEND = FINAL FREQUENCY FOR PLOTTING(IN HERTZ)
?
  50.E3
     FINC = INCREMENT FREQUENCY FOR PLOTTING(IN HERTZ)
?
  200.0
```

The magnitude and phase responses obtained from this program are shown in Figures 6.1 and 6.2 respectively. Furthermore, the circuit of the desired SC high-pass ladder filter which was also drawn by this package is shown in Fig. 6.3.

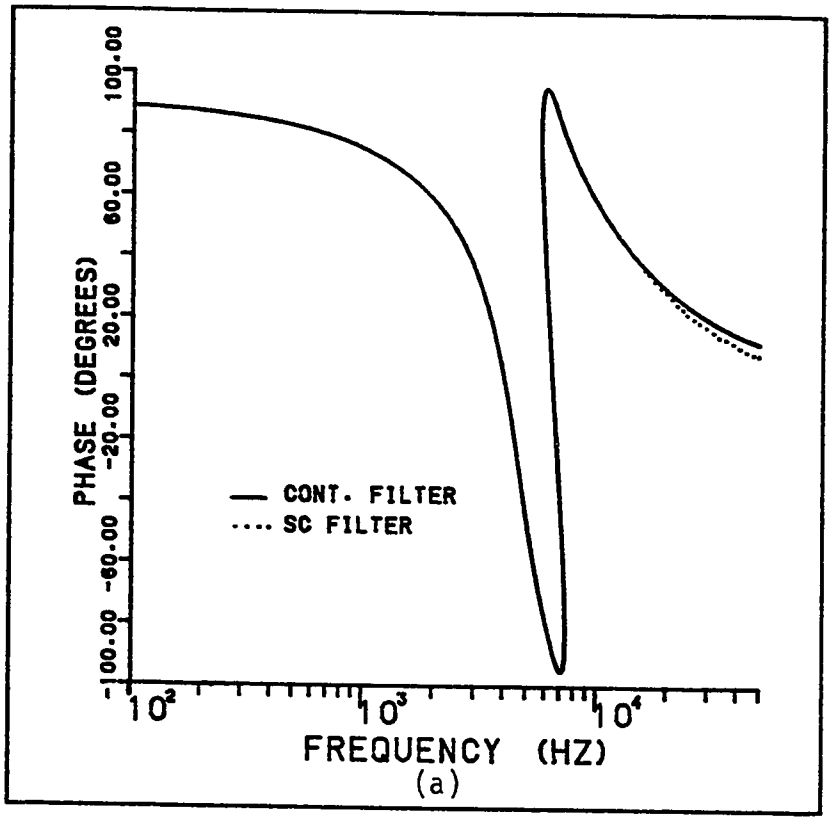


(a)



(b)

Figure 6.1 (a),(b) Magnitude response of a third order SC high-pass Chebychev ladder filter.



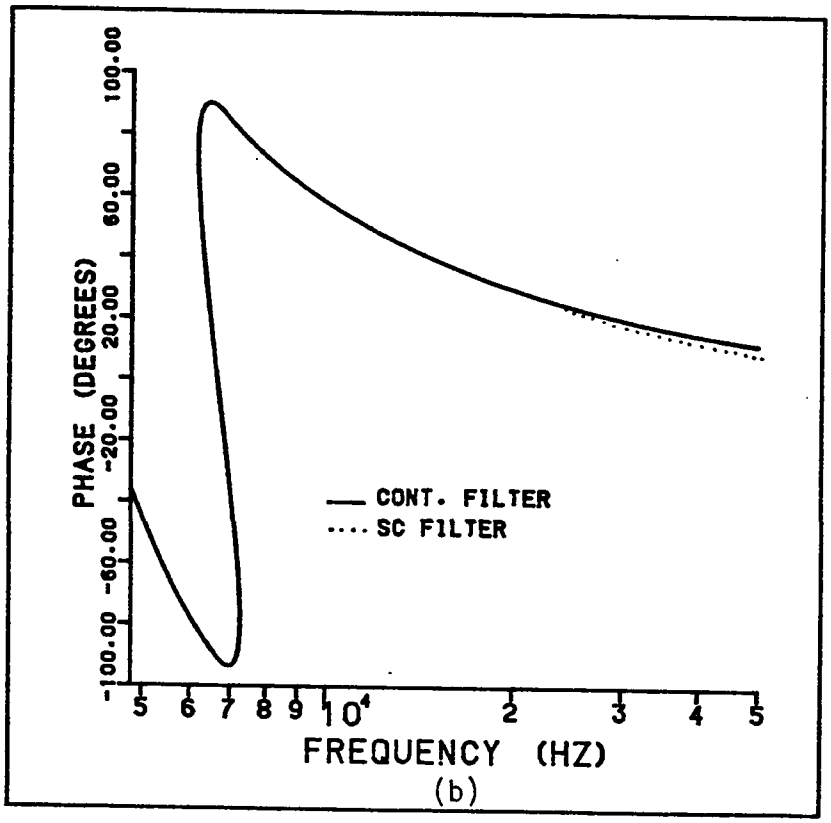


Figure 6.2 (a),(b) Phase response of a third order SC high-pass Chebychev ladder filter.

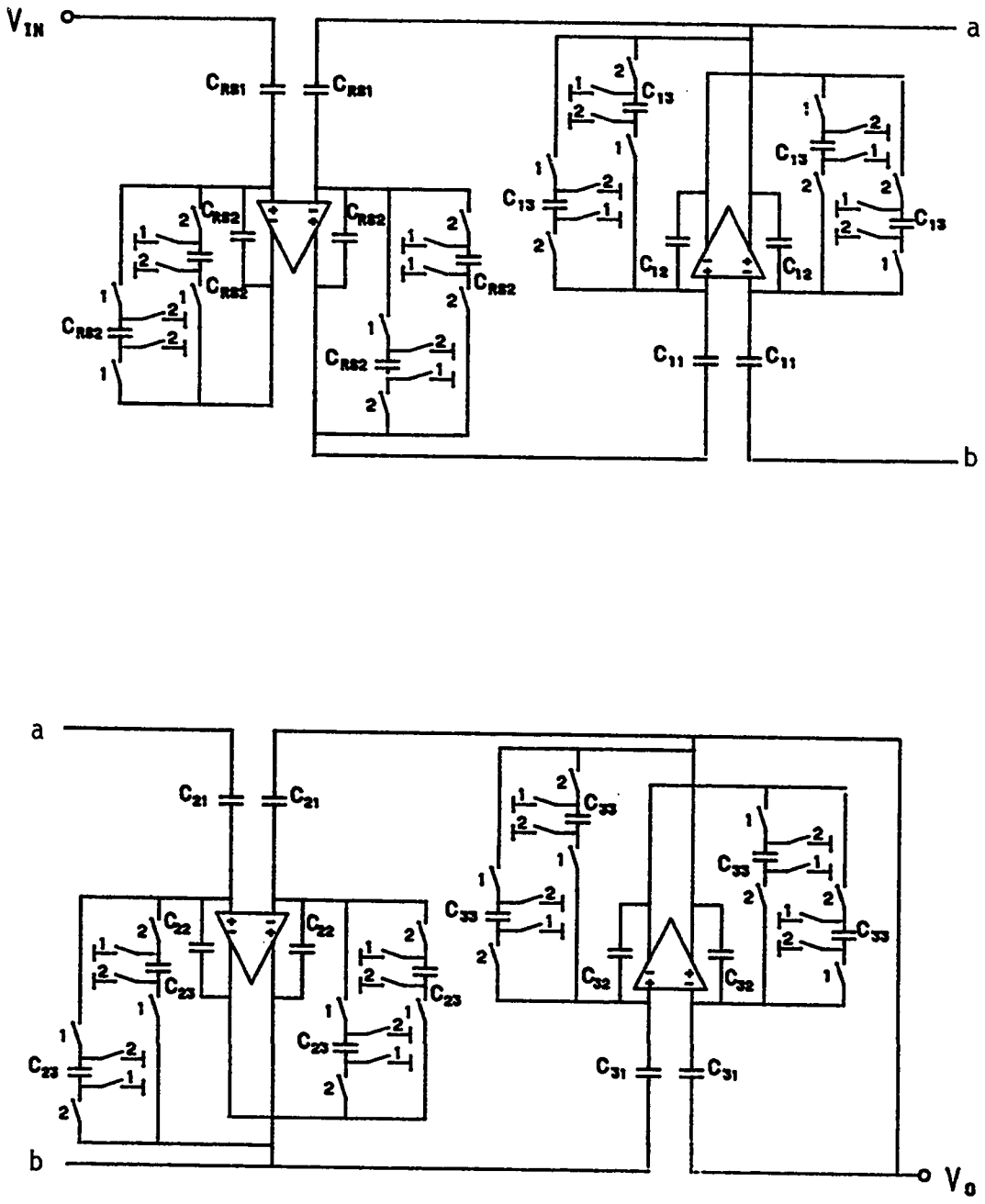


Figure 6.3 Third order SC high-pass Chebychev ladder filter.

Chapter VII

CONCLUSIONS

In this Chapter, we shall give a critical comparison of our findings with the results obtained by others. This will follow with a summary and suggestions for future work.

7.1 Comparison of Results

In Chapter 4, we have proposed a new technique for the design of switched capacitor high-pass ladder filters using the MLDD transformation. By realizing the resistive source termination with a special delay free building block, we have shown that the magnitude response of the SC high-pass ladder filter designed using this technique approximated the magnitude response of the high-pass continuous filter much closer than that of Horio et. al.. The reactive components are realized by a differential op-amp which has a much better performance than the single output op-amp at high frequencies. The proposed technique is much simpler than those presented by others. Beside this, the proposed design technique preserves completely the sensitivity properties of the SC high-pass ladder filters. This is not the case in the techniques proposed by others for the design of SC high-pass filters.

In Chapter 5, we have proposed a new transformation for the design of switched capacitor high-pass ladder filters. The SC high-pass ladder filters designed using this transformation give a magnitude response which is almost the same as the response of the high-pass continuous ladder filter. The only problem in the use of this transformation is in the design of SC high-pass Chebychev ladder filters which require the sampling frequency to be chosen large enough to assure that the poles of the high-pass continuous filter are located inside a semi-circle of radius 2/T. The modified bilinear transfer function is also realized by a differential op-amp. Since this transformation is based on the same design technique proposed in chapter 4, sensitivity properties of the SC high-pass ladder filters are completely preserved. The results obtained from the use of this transformation are better than those obtained from the use of the MLDD transformation. However, in some of the applications this has been achieved at the cost of a higher order SC high-pass filter.

7.2 Summary

The most widely used SC filter design is based on the SFG representation of the current-voltage relations of a passive ladder prototype filter. Switched-capacitor low-pass and band-pass ladder filters have been successfully designed by using the LDI and bilinear transformations. A number of

techniques have been previously reported for the design of switched capacitor high-pass ladder filters based on the LDI and bilinear transformations. However, these techniques have certain limitations and are not as direct as those techniques used for the design of SC low-pas and band-pass filters.

Horio et. al. have proposed a switched capacitor high-pass filter design technique based on the MLDD transformation. However, in their design technique, the resistive source termination is realized by a parallel SC feedback path across the first building block. It has been shown that realizing the resistive source termination by a parallel SC feedback path across the first building block, changes the overall transfer function of the SC filter. This variation in the transfer function causes a distortion in the magnitude response of the SC filter. We have shown that realizing the resistive source termination separately by a delay free differential input SC amplifier of constant gain R/R_s, gives a much better magnitude response. This is because, with the proposed configuration, the overall transfer function of the high-pass SC ladder filter will be exactly the same as the transfer function obtained from the high-pass continuous ladder filter by the direct application of the MLDD transformation. We have realized the MLDD transfer function with a differential op-amp which has a much better performance at higher frequencies. With the design procedure that we have

proposed, the design of SC high-pass ladder filters will be as direct as in the low-pass and band-pass case. With our technique, the magnitude and phase responses of the high-pass SC ladder filters have turned out to be much closer to the ideal responses of the high-pass continuous ladder filters.

We have proposed a new transformation for the design of SC high-pass ladder filters which has been named the modified bilinear transformation. We have used the technique that we have proposed for the design of SC high-pass ladder filters using the MLDD transformation. The magnitude and phase responses of the SC high-pass ladder filters obtained from the use of this transformation are almost the same as those of the high-pass continuous ladder prototype filter. For the design of SC high-pass Chebychev filters using the new transformation, the sampling frequency has to be chosen such that, all the poles of the high-pass continuous filter lie inside a semi-circle of radius 2/T.

As a bonus, we have prepared an interactive package for designing SC high-pass Butterworth and Chebychev filters based on the MLDD and modified bilinear transformations. The package gives all the necessary information to the designer, it provides with the magnitude and phase response of the resulting filter and it draws the complete circuit.

7.3 Suggestions for Future Work

The work presented in this thesis can be extended in the following directions:

1. The design of switched capacitor high-pass elliptic ladder filters based on the new modified bilinear transformation has not been investigated in this thesis, therefore, it stays as an open problem.
2. The use of the new modified bilinear transformation for the design of switched capacitor low-pass and band-pass filters should be investigated.
3. The use of the MLDD transformation for the design of switched capacitor low-pass and band-pass filters needs also investigation.
4. A sensitivity analysis of the proposed SC high-pass ladder filters to the variation of capacitance values should be performed.
5. The proposed package can be easily extended to be used for the design of SC low-pass and band-pass ladder filters using the LDI and bilinear transformations.

APPENDIX A

HPSC1 FORTRAN FILE

```
      REAL FNTL(900),DBHS(900),DBHZ(900),PHAHS(900),PHAHZ(900)
      REAL*8 OMGP,OMGS,FP,FS,T,PI,FSAMP
      REAL*8 FINT,FR,FEND,FINC,WP,WS
      REAL*8  LLP(50),CLP(50),LHP(50),CHP(50),C(600)
      REAL*8  RL,CLMIN,CCMIN,TOTCAP,TOTC
      REAL*8  ALPHA(50),BETA(50)
      REAL*8 ROOT(50),ROOTM
      COMPLEX*16  S,Z1,Z2,Z3,Z,HS,HZ,TR,CJ
      COMPLEX*8  HS1,HZ1
C******
C*   THIS PACKAGE WAS WRITTEN BY KEMAL MEHMET FIDANBOYLU AS A PARTIAL
C*   FULLFILLMENT FOR THE DEGREE OF MASTER OF SCIENCE IN ELECTRICAL
C*   ENGINEERING (JUNE 1987).
C******
        CALL PLOTS(0,0,1)
C**
C**                          DESIGN OF
C**
C**   N'TH ORDER BUTTERWORTH AND CHEBYCHEV SWITCHED CAPACITOR
C**                  HIGH PASS LADDER FILTERS
C**
C**                            USING
C**
C****              **** MLDD TRANSFORMATION  ****
C****
C****      WITH   S=(2/T)*(Z**-1/2 - Z**-3/2)/(1+Z**-2)
C****
C****
C**** ** OR ***** NEW MODIFIED BILINEAR TRANFORMATION  ****
C****
C****      WITH   S=(2/T)*(1-Z**-1/2)/(1+Z**-1/2)
C****
C****
C****
       WRITE(6,100)
 100  FORMAT(//,4X,'HELLO! WELCOME TO  FIDANBOYLU"S PACKAGE')
      WRITE(6,101)
 101  FORMAT(//,4X,'FOR DESIGNING HIGH PASS SWITCHED CAPACITOR')
      WRITE(6,110)
 110  FORMAT(//,4X,'          LADDER  FILTERS.              ')
      WRITE(6,120)
```

```
 120  FORMAT(///,4X,'PLEASE ENTER THE FOLLOWING PARAMETERS.')
        WRITE(6,130)
 130  FORMAT(//,4X,'AMIN = MINIMUM STOPBAND ATTENUATION IN DB.')
        READ(5,*) AMIN
        WRITE(7,131) AMIN
 131  FORMAT(//,4X,'AMIN=MINIMUM STOPBAND ATTENUATION IN DB.=',F10.3)
        WRITE(6,140)
 140  FORMAT(//,4X,'AMAX = MAXIMUM PASSBAND ATTENUATION IN DB.')
        READ(5,*) AMAX
        WRITE(7,141) AMAX
 141  FORMAT(//,4X,'AMAX=MAXIMUM PASSBAND ATTENUATION IN DB.=',F10.3)
        WRITE(6,150)
 150  FORMAT(//,4X,'FP = PASSBAND EDGE FREQUENCY IN HERTZ.')
        READ(5,*) FP
        WRITE(7,151) FP
 151  FORMAT(//,4X,'FP = PASSBAND EDGE FREQUENCY IN HERTZ.=',E11.4)
        WRITE(6,160)
 160  FORMAT(//,4X,'FS = STOPBAND EDGE FREQUENCY IN HERTZ.')
        READ(5,*) FS
        WRITE(7,161) FS
 161  FORMAT(//,4X,'FS = STOPBAND EDGE FREQUENCY IN HERTZ.=',E11.4)
        WRITE(6,170)
 170  FORMAT(//,4X,'FSAMP= SAMPLING  FREQUENCY IN HERTZ.')
        READ(5,*) FSAMP
        WRITE(7,171) FSAMP
 171  FORMAT(//,4X,'FSAMP= SAMPLING  FREQUENCY IN HERTZ.=',E11.4)
C****
        WRITE(6,180)
 180  FORMAT(//,4X,'WHAT TYPE OF FILTER DESIGN DO YOU NEED?')
        WRITE(6,181)
 181  FORMAT(//,4X,'TYPE 1 FOR BUTTERWORTH AND 2 FOR CHEBYCHEV')
        READ(5,*) ITYP
          IF(ITYP.EQ.1)THEN
        WRITE(7,182)
 182  FORMAT(//,4X,'HIGH PASS SC BUTTERWORTH FILTER DESIGN.')
          ELSE
        WRITE(7,183)
 183  FORMAT(//,4X,'HIGH PASS SC CHEBYCHEV FILTER DESIGN.')
          ENDIF
C****
        WRITE(6,190)
 190  FORMAT(//,4X,'WHAT TYPE OF TRANFORMATION DO YOU WANT?')
        WRITE(6,191)
 191  FORMAT(//,4X,'TYPE 1 FOR MLDD AND 2 FOR MBIL')
        READ(5,*) ITRAN
          IF(ITRAN.EQ.1)THEN
        WRITE(7,192)
 192  FORMAT(//,4X,'WITH MODIFIED LOSSLESS DISCRETE DIFFERENTIATOR
```

```
     *TRANSFORMATION')
           ELSE
          WRITE(7,193)
 193     FORMAT(//,4X,'WITH MODIFIED BILINEAR TRANFORMATION.')
           ENDIF
C****
C****
               T  = 1./FSAMP
               PI = 4.DO*DATAN(1.DO)
               CJ = DCMPLX(0.DO,1.DO)
               WP = 2.DO*PI*FP
               WS = 2.DO*PI*FS
C****
C****
          IF(ITRAN.EQ.1)THEN
C** OMGP = PREWARPED PASSBAND FREQUENCY OF THE FILTER IN RADIANS.
C** OMGS = PREWARPED STOPBAND FREQUENCY OF THE FILTER IN RADIANS.
             OMGP = OMGPR1(FP,T)
             OMGS = OMGPR1(FS,T)
          ELSE
             OMGP = OMGPR2(FP,T)
             OMGS = OMGPR2(FS,T)
          ENDIF
C
C**** WARNING
C
        IF(OMGP.LE.0.DO.OR.OMGS.LE.0.DO)THEN
           WRITE(6,194)
 194     FORMAT(//,4X,'YOU ARE EITHER GIVING WRONG PARAMETERS')
           WRITE(6,195)
 195     FORMAT(//,4X,'OR CHOOSING A LOW SAMPLING FREQUENCY')
           WRITE(6,196)
 196     FORMAT(//,4X,'TYPE A NUMBER TO RETURN BACK')
           READ(5,*) WNG
           STOP
        ELSE
           CONTINUE
        ENDIF
C
C**** END WARNING
C
C****
          IF(ITYP.EQ.1)THEN
             CALL ORDERB(N,AMAX,AMIN,OMGP,OMGS)
C*
C****  WARNING
C*
        IF(N.LE.1)THEN
```

```
          WRITE(6,197)
 197      FORMAT(//,4X,'YOU ARE EITHER GIVING WRONG PARAMETERS')
          WRITE(6,198)
 198      FORMAT(//,4X,'OR CHOOSING A LOW SAMPLING FREQUENCY')
          WRITE(6,199)
 199      FORMAT(//,4X,'TYPE A NUMBER TO RETURN BACK')
          READ(5,*) WNG
          STOP
        ELSE
           CONTINUE
        ENDIF
C*
C****   END WARNING
C*
            CALL OMGZRB(N,AMAX,OMGZLP)
          ELSE
            CALL ORDERC(N,AMAX,AMIN,OMGP,OMGS)
C*
C****   WARNING
C*
        IF(N.LE.1)THEN
          WRITE(6,1197)
 1197     FORMAT(//,4X,'YOU ARE EITHER GIVING WRONG PARAMETERS')
          WRITE(6,1198)
 1198     FORMAT(//,4X,'OR CHOOSING A LOW SAMPLING FREQUENCY')
          WRITE(6,1199)
 1199     FORMAT(//,4X,'TYPE A NUMBER TO RETURN BACK')
          READ(5,*) WNG
          STOP
       ELSE
          CONTINUE
       ENDIF
C*
C****   END WARNING
C*
C*
            CALL OMGZRC(N,AMAX,OMGZLP)
           N2=N/2
           S = CMPLX(1.0,0.0)
         CALL TRFNC(TR,OMGP,S,ALPHA,BETA,N,AMAX,ROOT)
            ROOTM = 1.D-20
          DO 201 KE=1,N2
            IF(ROOT(KE).GT.ROOTM)THEN
              ROOTM = ROOT(KE)
            ELSE
              CONTINUE
            ENDIF
 201      CONTINUE
```

```
                EPS = SQRT(10.**(.1*AMAX)-1.)
                AC = ARSINH(1./EPS)/FLOAT(N)
                AW = OMGP/SINH(AC)
                IF((2*N2).LT.N)THEN
                  AW=AW
                 ELSE
                  AW=ROOTM
                ENDIF
C*
          IF((2./T).LE.AW.AND.ITRAN.NE.1)THEN
               WRITE(6,200)
 200         FORMAT(//,4X,' THE TRANSFORMATION IS NOT VALID.')
               WRITE(6,202) AW/2.0
 202         FORMAT(//,4X,'YOU SHOULD MAKE THE SAMPLING FREQUENCY
     *MORE THAN',E12.4,' HZ')
               WRITE(6,203)
 203         FORMAT(//,4X,'TYPE A NUMBER TO RETURN BACK')
               READ(5,*) DELAY
                STOP
          ELSE
               CONTINUE
          ENDIF
C*
        ENDIF
C****
                WRITE(6,300) N
                WRITE(7,300) N
 300            FORMAT(//,4X,'ORDER OF THE FILTER = ',I2)
               OMGZHP = OMGP/OMGZLP
            WRITE(6,310) OMGZHP
            WRITE(7,310) OMGZHP
 310  FORMAT(//,4X,'THE HALF POWER FREQ. OF THE HP CONT. FILTER IS
     * =',E11.4,' RAD/SEC')
C**
C**  CALCULATION OF CAPACITANCE VALUES.
C**
          IF(ITYP.EQ.1)THEN
              CALL  LPBUTW(N,LLP,CLP,RL)
          ELSE
              CALL  LPCHEB(N,AMAX,RL,LLP,CLP)
          ENDIF
C**
          IF(ITRAN.EQ.1)THEN
C*
C* CALCULATION OF CAPACITANCE VALUES FOR THE MLDD SC FILTER
C*
       WRITE(6,702)
       WRITE(7,702)
```

```
 702  FORMAT(/,'NORMALIZED CAPACITANCES FOR THE SOURCE TERMINATION')
             CRS1 = 1.0
             CRS2 = 1.D0/RL
               TOTCAP = CRS1+CRS2
              WRITE(6,700) CRS1
              WRITE(7,700) CRS1
 700         FORMAT(/,4X,'CRS1 =',F12.6,' CU')
              WRITE(6,701) CRS2
              WRITE(7,701) CRS2
 701         FORMAT(/,4X,'CRS2 =',F12.6,' CU')
           DO 710 I10= 1,N,2
             I11= I10 + 1
             I12= I10*10
             LHP(I10)  = 1.D0/(CLP(I10)*OMGP)
             C(I12+2)  = RL*T/LHP(I10)
             C(I12+3)  = 0.75D0*C(I12+2)
             C(I12+4)  = 2.D0*C(I12+2)
             C(I12+5)  = 1.5D0*C(I12+2)
             C(I12+6)  = 2.D0*C(I12+2)
             C(I12+7)  = 2.D0*C(I12+2)
             C(I12+8)  = 1.5D0*C(I12+2)
C*
          WRITE(6,712) I10
          WRITE(7,712) I10
 712  FORMAT(//,4X,'NORMALIZED CAPACITANCES FOR SECTION NO:',I2)
              CLMIN = 1.0D30
             DO 720 J1=I12+2,I12+8
                IF(C(J1).LT.CLMIN)THEN
                  CLMIN = C(J1)
                ELSE
                  CONTINUE
                ENDIF
 720         CONTINUE
                IF(CLMIN.GE.1.0D0) CLMIN=1.D0
                 C(I12+1) = 1.D0
             DO 721 J11=I12+1,I12+8
                   IF(J11.LE.(I12+2))THEN
                    TOTC = 2.D0*C(J11)/CLMIN
                   ELSE
                    TOTC = C(J11)/CLMIN
                   ENDIF
                 TOTCAP = TOTCAP+TOTC
                WRITE(6,722) J11,C(J11)/CLMIN
                WRITE(7,722) J11,C(J11)/CLMIN
 722           FORMAT(/,4X,'C(',I3,') =',F20.6,' CU')
 721         CONTINUE
C*
                IF(I11.GT.N) GO TO 402
```

```
C*
                  I13= I11*10
                  CHP(I11) = 1.D0/(LLP(I11)*OMGP)
            C(I13+2)  = T/(RL*CHP(I11))
            C(I13+3)  = 0.75D0*C(I13+2)
            C(I13+4)  = 2.D0*C(I13+2)
            C(I13+5)  = 1.5D0*C(I13+2)
            C(I13+6)  = 2.D0*C(I13+2)
            C(I13+7)  = 2.D0*C(I13+2)
            C(I13+8)  = 1.5D0*C(I13+2)
C*
        WRITE(6,714) I11
        WRITE(7,714) I11
 714  FORMAT(//,4X,'NORMALIZED CAPACITANCES FOR SECTION NO:',I2)
             CCMIN = 1.0D30
            DO 730 J2=I13+2,I13+8
               IF(C(J2).LT.CCMIN)THEN
                 CCMIN = C(J2)
               ELSE
                 CONTINUE
               ENDIF
  730       CONTINUE
               IF(CCMIN.GE.1.0D0) CCMIN=1.D0
               C(I13+1) = 1.D0
            DO 731 J21=I13+1,I13+8
                  IF(J21.LE.(I13+2))THEN
                   TOTC = 2.D0*C(J21)/CCMIN
                  ELSE
                   TOTC = C(J21)/CCMIN
                  ENDIF
                TOTCAP = TOTCAP+TOTC
              WRITE(6,732) J21,C(J21)/CCMIN
              WRITE(7,732) J21,C(J21)/CCMIN
  732         FORMAT(/,4X,'C(',I3,') =',F20.6,' CU')
  731       CONTINUE
  710     CONTINUE
  402   CONTINUE
        WRITE(6,740) TOTCAP
        WRITE(7,740) TOTCAP
 740   FORMAT(//,4X,'THE TOTAL CAPACITANCE FOR THE SC FILTER =',
     *F20.6,' CU')
C*
              ELSE
C*
C* CALCULATION OF CAPACITANCE VALUES FOR THE MBIL SC FILTER
C*
      WRITE(6,750)
      WRITE(7,750)
```

```
 750  FORMAT(/,'NORMALIZED CAPACITANCES FOR THE SOURCE TERMINATION')
            CRS1 = 3.D0*RL
           IF(CRS1.GE.1.D0)THEN
            CRS2 = 1.D0
           ELSE
            CRS2 = 1.D0/(3.D0*RL)
            CRS1 = 1.D0
           ENDIF
             TOTCAP = 2.D0*CRS1+6.D0*CRS2
            WRITE(6,760) CRS1
            WRITE(7,760) CRS1
 760        FORMAT(/,4X,'CRS1 =',F12.6,' CU')
            WRITE(6,761) CRS2
            WRITE(7,761) CRS2
 761        FORMAT(/,4X,'CRS2 =',F12.6,' CU')
          DO 770 I70= 1,N,2
             I71= I70 + 1
             I72= I70*10
               LHP(I70)  = 1.D0/(CLP(I70)*OMGP)
               C(I72+1)  = 4.D0*LHP(I70)/(RL*T)
          IF(C(I72+1).GE.1.D0)THEN
             C(I72+2) = 1.D0
          ELSE
             C(I72+2) = 1.D0/C(I72+1)
             C(I72+1) = 1.D0
          ENDIF
             C(I72+3) = 2.D0*C(I72+2)
C*
        WRITE(6,772) I70
          WRITE(7,772) I70
 772    FORMAT(//,4X,'NORMALIZED CAPACITANCES FOR SECTION NO: ',I2)
             DO 781 J71=I72+1,I72+3
                   IF(J71.LE.(I72+2))THEN
                    TOTC = 2.D0*C(J71)
                   ELSE
                    TOTC = 4.D0*C(J71)
                   ENDIF
                 TOTCAP = TOTCAP+TOTC
               WRITE(6,782) J71,C(J71)
               WRITE(7,782) J71,C(J71)
  782          FORMAT(/,4X,'C(',I3,') =',F20.6,' CU')
  781        CONTINUE
C*
              IF(I71.GT.N) GO TO 403
C*
                I73= I71*10
                CHP(I71) = 1.D0/(LLP(I71)*OMGP)
                C(I73+1)  = 4.D0*RL*CHP(I71)/T
```

```
          IF(C(I73+1).GE.1.D0)THEN
               C(I73+2) = 1.D0
          ELSE
               C(I73+2) = 1.D0/C(I73+1)
               C(I73+1) = 1.D0
          ENDIF
               C(I73+3)  = 2.D0*C(I73+2)
C*
       WRITE(6,784) I71
       WRITE(7,784) I71
 784   FORMAT(//,4X,'NORMALIZED CAPACITANCES FOR SECTION NO:',I2)
             DO 791 J81=I73+1,I73+3
                   IF(J81.LE.(I73+2))THEN
                    TOTC = 2.D0*C(J81)
                   ELSE
                    TOTC = 4.D0*C(J81)
                   ENDIF
                 TOTCAP = TOTCAP+TOTC
               WRITE(6,792) J81,C(J81)
               WRITE(7,792) J81,C(J81)
  792          FORMAT(/,4X,'C(',I3,') =',F20.6,' CU')
  791       CONTINUE
  770     CONTINUE
  403    CONTINUE
       WRITE(6,799) TOTCAP
       WRITE(7,799) TOTCAP
 799  FORMAT(//,4X,'THE TOTAL CAPACITANCE FOR THE SC FILTER =',
     *F20.6,' CU')
C**
C** END OF CALCULATION OF CAPACITANCE VALUES
C**
         ENDIF
C**
              WRITE(6,311)
 311  FORMAT(/,'DO YOU WANT TO SEE THE MAGNITUDE AND PHASE RESPONSE')
              WRITE(6,312)
 312   FORMAT(//,4X,'IF YES TYPE 1 OTHERWISE TYPE 0')
         READ(5,*) STP
C*
            IF(STP.EQ.0)THEN
             STOP
            ELSE
             CONTINUE
            ENDIF
C*
         WRITE(7,320)
 320  FORMAT(//,2X,'FREQUENCY(HZ)',6X,'MAGNITUDE(DB)',14X,
     *'PHASE (DEGREES)')
```

```
        WRITE(7,321)
 321  FORMAT(/,14X,'CONT. FILTER',4X,'SC FILTER',6X,'CONT.FILTER',
     *5X,'SC FILTER')
        WRITE(6,330)
 330  FORMAT(//,4X,'PLEASE ENTER THE FOLLOWING PARAMETERS.')
        WRITE(6,340)
 340  FORMAT(//,4X,'FINT = INITIAL FREQUENCY FOR PLOTTING(IN HERTZ)')
        READ(5,*) FINT
        WRITE(6,350)
 350  FORMAT(//,4X,'FEND = FINAL FREQUENCY FOR PLOTTING(IN HERTZ)')
        READ(5,*) FEND
        WRITE(6,360)
 360  FORMAT(//,4X,'FINC=INCREMENT FREQUENCY FOR PLOTTING(IN HERTZ)')
        READ(5,*) FINC
C****
C****   FOLLOWING PROGRAM SEGMENT GENERATES DATA FOR PLOTTING THE
C****              MAGNITUDE AND PHASE RESPONSE FOR
C****              CHEBYCHEV AND BUTTERWORTH FILTER
C****
          I1=0
          FR = FINT
        DO 500 I=1,895
           I1=I1+1
C** I1 IS FOR COUNTING
            W    = FR*2.D0*PI
            S    = CMPLX(0.0,W)
            Z1   = CDEXP(-W*T*CJ/2.)
            Z2   = CDEXP(-3.*W*T*CJ/2.)
            Z3   = CDEXP(-2.*W*T*CJ)
         IF(ITRAN.EQ.1)THEN
            Z  = (2.D0/T)*(Z1-Z2)/(1.D0+Z3)
         ELSE
            Z  = (2.D0/T)*(1.D0-Z1)/(1.D0+Z1)
         ENDIF
C*
        IF(ITYP.EQ.1)THEN
           CALL  TRFNB(TR,WP,S,N)
             HS   = TR
             HS1  = HS
           CALL  TRFNB(TR,OMGP,Z,N)
             HZ   = TR
             HZ1  = HZ
        ELSE
          CALL TRFNC(TR,WP,S,ALPHA,BETA,N,AMAX,ROOT)
             HS   = TR
             HS1  = HS
          CALL TRFNC(TR,OMGP,Z,ALPHA,BETA,N,AMAX,ROOT)
             HZ   = TR
```

```
            HZ1  = HZ
          ENDIF
C*
C*
          IF(REAL(HS1).EQ.0.0)THEN
             APHS=AIMAG(HS1)/ABS(AIMAG(HS1))
             PHAHS(I)=APHS*90.0
          ELSE IF(REAL(HS1).GT.0.0.AND.AIMAG(HS1).LT.0.0)THEN
             THETAS = ATAN(ABS(AIMAG(HS1))/ABS(REAL(HS1)))
             PHAHS(I) = -180.0*THETAS/PI
          ELSE IF(REAL(HS1).LT.0.0.AND.AIMAG(HS1).GT.0.0)THEN
             THETAS = ATAN(ABS(AIMAG(HS1))/ABS(REAL(HS1)))
             PHAHS(I) = 180.0-180.0*THETAS/PI
          ELSE IF(REAL(HS1).LT.0.0.AND.AIMAG(HS1).LT.0.0)THEN
             THETAS = ATAN(ABS(AIMAG(HS1))/ABS(REAL(HS1)))
             PHAHS(I) =-180.0+180.0*THETAS/PI
          ELSE
             PHAHS(I) = (180.0/PI)*ATAN(AIMAG(HS1)/REAL(HS1))
           ENDIF
C*
C*
          IF(REAL(HZ1).EQ.0.0)THEN
             APHZ = AIMAG(HZ1)/ABS(AIMAG(HZ1))
             PHAHZ(I) = APHZ*90.0
          ELSE IF(REAL(HZ1).GT.0.0.AND.AIMAG(HZ1).LT.0.0)THEN
             THETAZ = ATAN(ABS(AIMAG(HZ1))/ABS(REAL(HZ1)))
             PHAHZ(I) = -180.0*THETAZ/PI
          ELSE IF(REAL(HZ1).LT.0.0.AND.AIMAG(HZ1).GT.0.0)THEN
             THETAZ = ATAN(ABS(AIMAG(HZ1))/ABS(REAL(HZ1)))
             PHAHZ(I) = 180.0-180.0*THETAZ/PI
          ELSE IF(REAL(HZ1).LT.0.0.AND.AIMAG(HZ1).LT.0.0)THEN
             THETAZ = ATAN(ABS(AIMAG(HZ1))/ABS(REAL(HZ1)))
             PHAHZ(I) =-180.0+180.0*THETAZ/PI
          ELSE
             PHAHZ(I) = (180.0/PI)*ATAN(AIMAG(HZ1)/REAL(HZ1))
           ENDIF
C*
         RMGHS = CDABS(HS)
         RMGHZ = CDABS(HZ)
         DBHS(I) = 20.0*ALOG10(RMGHS)
         DBHZ(I) = 20.0*ALOG10(RMGHZ)
          WRITE(7,88) FR,DBHS(I),DBHZ(I),PHAHS(I),PHAHZ(I)
 88         FORMAT(2X,F10.2,2X,E12.4,2X,E12.4,2X,F12.3,2X,F12.3)
            FNTL(I)=ALOG10(SNGL(FR))
          WRITE(8,90) FNTL(I),DBHS(I),DBHZ(I),PHAHS(I),PHAHZ(I)
 90           FORMAT(2X,F10.4,F12.4,F12.4,F12.3,F12.3)
          FR = FR + FINC
          IF(FR.GT.FEND)GO TO 600
```

```
 500      CONTINUE
C****
C****    FOLLOWING PROGRAM SEGMENT OBTAINS THE PLOTS FOR THE
C****    MAGNITUDE AND PHASE RESPONSE
C****
 600           CONTINUE
               CALL PLOT(4.0,4.0,-3)
               CALL NEWPEN(1)
               CALL FACTOR(1.0)
C**
C** AXL IS THE AXIS LENGTH
C**
               AXL = 10.
C**            WRITE(7,*) I1
               IF(I1.EQ.895)THEN
                FEND=FR-FINC
               WRITE(7,*) FEND
               ELSE
                FEND=FEND
               ENDIF

C***
C***  PROGRAM SEGMENT FOR ADJUSTING SCALING
C***
        FSINT=SNGL(FINT)
        FNTL(I1+1) = ALOG10(FSINT)
        FNTL(I1+2) = (ALOG10(SNGL(FEND))-FNTL(I1+1))/AXL
C***
            PMIN1= 1.E30
            PMAX1= 1.E-30
            PMIN2= 1.E30
            PMAX2= 1.E-30
            PMIN3= 1.E30
           DO 50 IP2=1,I1
              IF(DBHS(IP2).LE.PMIN1) THEN
                PMIN1 = DBHS(IP2)
              ELSE IF(DBHS(IP2).GE.PMAX1) THEN
                PMAX1 = DBHS(IP2)
              ENDIF
C***
              IF(DBHZ(IP2).LE.PMIN2) THEN
                PMIN2 = DBHZ(IP2)
              ELSE IF(DBHZ(IP2).GE.PMAX2) THEN
                PMAX2 = DBHZ(IP2)
              ENDIF
C***
              IF(PHAHZ(IP2).LE.PMIN3) THEN
                PMIN3 = PHAHZ(IP2)
```

```
            ENDIF
 50        CONTINUE
C***
            DBHS(I1+1) =IFIX(PMIN1 - 4.)
            DBHS(I1+2) =IFIX(1.+(PMAX1-DBHS(I1+1))/AXL)
C***
            DBHZ(I1+1) =IFIX(PMIN2- 4.)
            DBHZ(I1+2) =IFIX(1.+(PMAX2-DBHZ(I1+1))/AXL)
C***
C***
              IF(DBHS(I1+1).LT.DBHZ(I1+1)) THEN
                DBHZ(I1+1) = DBHS(I1+1)
              ELSE
                DBHS(I1+1) = DBHZ(I1+1)
              ENDIF
C***
              IF(DBHS(I1+2).GT.DBHZ(I1+2)) THEN
                DBHZ(I1+2) = DBHS(I1+2)
              ELSE
                DBHS(I1+2) = DBHZ(I1+2)
              ENDIF
C***
                PHAHS(I1+1) = -200.0
                PHAHZ(I1+1) = -200.0
                PHAHS(I1+2) = 400./AXL
                PHAHZ(I1+2) = 400./AXL
C***
C***
C***
      CALL LGAXS(0.0,0.0,21HFREQUENCY (HZ)        ,
     * -21,AXL,0.0,FSINT,FNTL(I1+2))
      CALL AXIS(0.0,0.0,21HMAGNITUDE (DB)        ,
     * 21,AXL,90.0,DBHZ(I1+1),DBHZ(I1+2))
         CALL NEWPEN(2)
      CALL FLINE(FNTL,DBHS,-I1,1,0,2)
         CALL NEWPEN(3)
      CALL FLINE(FNTL,DBHZ,-I1,1,0,2)
         CALL NEWPEN(2)
      CALL SYMBOL(0.5,11.1,0.4,22H__ CONTINUOUS FILTER  ,0.0,22)
         CALL NEWPEN(3)
      CALL SYMBOL(0.5,10.5,0.4,25H__ SWITCHED CAPACITOR F. ,0.0,25)
         CALL NEWPEN(1)
      CALL RECT(-2.5,-2.0,14.0,14.,0.,3)
          CALL PLOT(17.0,0.0,-3)
          CALL NEWPEN(1)
      CALL LGAXS(0.0,0.0,21HFREQUENCY (HZ)        ,
     * -21,AXL,0.0,FSINT,FNTL(I1+2))
      CALL AXIS(0.0,0.0,21HPHASE (DEGREES)       ,
```

```
     *  21,AXL,90.0,PHAHZ(I1+1),PHAHZ(I1+2))
           CALL NEWPEN(2)
         CALL FLINE(FNTL,PHAHS,-I1,1,0,2)
           CALL NEWPEN(3)
         CALL FLINE(FNTL,PHAHZ,-I1,1,0,2)
           CALL NEWPEN(2)
       CALL SYMBOL(0.5,11.1,0.4,22H__ CONTINUOUS FILTER  ,0.0,22)
           CALL NEWPEN(3)
       CALL SYMBOL(0.5,10.5,0.4,25H__ SWITCHED CAPACITOR F. ,0.0,25)
           CALL NEWPEN(1)
         CALL RECT(-2.5,-2.0,14.0,14.,0.,3)
C ***********************************************
C FOLLOWING PROGRAM SEGMENT DRAWS THE CIRCUIT
C      OF THE SC HIGH PASS LADDER FILTER
C ***********************************************
       CALL PLOT(-20.,16.,-3)
       CALL FACTOR (1.5)
       CALL NEWPEN(1)
            IP=3
            ID=2
             A =0.28
             A1=0.18
             B=-0.068
       IF(ITRAN.EQ.1)THEN
C ***********************************************
C PROGRAM FOR DRAWING SC LADDER FILTER RESULTING
C          FROM THE MLDD TRANFORMATION.
C ***********************************************
        CALL  RSMLDD(0.0,0.0)
          X=1.0
          Y=0.6
        DO 10 I= 1 ,N2
            F1=(2*I-1.)*10.
         CALL BMLDD1(X,Y,F1)
            X=X+5.2
            Y=Y
            F2=I*2.*10.
         CALL BMLDD2(X,Y,F2)
            X=X+5.2
            Y=Y
  10    CONTINUE
C*
C*
           IF((2*N2).LT.N)THEN
             F1=N*10.
             CALL BMLDD1(X,Y,F1)
            X=X+9.2
            Y=Y
```

```
            V1=1.0
            X12=X+3.4*V1
          ELSE
            V1=2
            X12=X+4.0*V1
          ENDIF
       ELSE
C ************************************************
C PROGRAM FOR DRAWING SC LADDER FILTER RESULTING
C    FROM THE MODIFIED BILINEAR  TRANFORMATION.
C ************************************************
       CALL RSMBIL(-5.0,0.6)
          X=1.0
          Y=0.6
        DO 20 I= 1 ,N2
           F1=(2*I-1.)*10.
         CALL BMBIL1(X,Y,F1)
           X=X+5.8
           Y=Y
           F2=I*2.*10.
         CALL BMBIL2(X,Y,F2)
           X=X+5.8
           Y=Y
  20    CONTINUE
C*
          IF((2*N2).LT.N)THEN
            F1=N*10.
            CALL BMBIL1(X,Y,F1)
           X=X+9.35
           Y=Y
             V1=1.0
             X12=X+3.4*V1
          ELSE
           X=X-0.5
           Y=Y
             V1=2.0
             X12=X+4.0*V1
          ENDIF
C*
       ENDIF
C*
               X11=X+4.3*V1
               X13=X+4.6*V1
               X14=X13 + 0.15
               X15=X+4.*V1-.6
               X16=X13+.4
             CALL PLOT(X15,Y+.6,IP)
             CALL PLOT(X13,Y+.6,ID)
```

```
              CALL PLOT(X14,Y+.6,IP)
              CALL CIRCLE(X14,Y+.6,0.,360.,.075,5)
              CALL PLOT(X11,Y+.6,IP)
              CALL PLOT(X11,Y+6.8,ID)
              CALL PLOT(X12,Y+6.8,ID)
             CALL SYMBOL(X16,Y+.4,0.3,5HV    ,0.0,5)
             CALL SYMBOL(X16+A,Y+.4+B,0.15,5HO    ,0.0,5)
       CALL PLOT (80.,80.,999)
       STOP
       END
C*********************************************
C**
        FUNCTION OMGPR1(F,T)
C**
C*  FUNCTION SUBPROGRAM FOR PREWARPING MLDD
C*
C*  **OMGPR1 IS THE PREWARPING EQUATION FOR MLDD TRANFORMATION.**
C**
          REAL*8  F,T,PI,W
          PI    = 4.D0*DATAN(1.D0)
          W=2.D0*PI*F
           OMGPR1= (2.D0/T)*DSIN(W*T/2.D0)/DCOS(W*T)
       RETURN
       END
C*********************************************
C**
C**
       FUNCTION OMGPR2(F,T)
C**
C*        FUNCTION SUBPROGRAM FOR PREWARPING MBIL
C*
C* OMGPR2 IS THE PREWARPING EQUATION FOR MODIFIED BILINEAR TRANSF.
C**
          REAL*8  F,T,PI,W
          PI    = 4.D0*DATAN(1.D0)
          W=2.D0*PI*F
           OMGPR2= (2.D0/T)*DTAN(W*T/4.D0)
       RETURN
       END
C*********************************************
C**
C**
       FUNCTION ARCOSH(X)
C**
C*  FUNCTION SUBPROGRAM FOR INVERSE HYPERBOLIC COSINE
C**
       REAL*8 X
          ARCOSH = DLOG(X+DSQRT(X**2-1.D0))
```

```
      RETURN
      END
C*********************************************
C*
C*
      FUNCTION ARSINH(X)
C**
C*  FUNCTION SUBPROGRAM FOR INVERSE HYPERBOLIC SINE
C**
         ARSINH = ALOG(X+SQRT(X**2+1.))
      RETURN
      END
C*********************************************
C**
C**
      SUBROUTINE ORDERB(N,AMAX,AMIN,OMGP,OMGS)
C**
C*  SUBROUTINE FOR CALCULATING THE ORDER OF BUTTERWORTH FILTER
C*  THE ORDER OF THE FILTER IS CALCULATED AS "N"
C**
      REAL*8 OMGP,OMGS,A3
       A1 = 10.**(AMIN/10.)-1.
        A2 = 10.**(AMAX/10.)-1.
       A3 = 2.*DLOG10(OMGP/OMGS)
          OR = ALOG10(A1/A2)/A3
          N = IFIX(OR+1.)
      RETURN
      END
C*********************************************
C**
C**
      SUBROUTINE ORDERC(N,AMAX,AMIN,OMGP,OMGS)
C**
C*  SUBROUTINE FOR CALCULATING THE ORDER OF CHEBYCHEV FILTER
C*  THE ORDER OF THE FILTER IS CALCULATED AS "N"
C**
      REAL*8 OMGP,OMGS,A4,A3
       A1 = 10.**(AMIN/10.)-1.
        A2 = 10.**(AMAX/10.)-1.
         A3 = SQRT(A1/A2)
       A4 = ARCOSH(OMGP/OMGS)
          OR = ARCOSH(A3)/A4
          N = IFIX(OR+1.)
      RETURN
      END
C*********************************************
C**
C**
```

```
        SUBROUTINE OMGZRB(N,AMAX,OMGZLP)
C**
C*   SUBROUTINE FOR CALCULATING THE HALF POWER FREQUENCY
C*    OF THE BUTTERWORTH FILTER.
C**
         A1 = 10.**(.1*AMAX)-1.
         P2 = 1./FLOAT(2*N)
         OMGZLP= 1./A1**P2
        RETURN
        END
C***********************************************
C**
C**
        SUBROUTINE OMGZRC(N,AMAX,OMGZLP)
C**
C*   SUBROUTINE FOR CALCULATING THE HALF POWER FREQUENCY
C*    OF THE CHEBYCHEV FILTER.
C**
         EPS = SQRT(10.**(.1*AMAX)-1.)
         P2 = 1./FLOAT(N)
         OMGZLP= COSH(P2*ARCOSH(1./EPS))
        RETURN
        END
C***********************************************
C**
C**
        SUBROUTINE TRFNB(TR,W,S,N)
C**
C*   SUBROUTINE FOR OBTAINING THE TRANSFER FUNCTION
C*              OF THE BUTTERWORTH FILTER
C**
          COMPLEX*16 TR,S,HBN
          REAL*8 PSI(50),W
          PI    = 4.D0*DATAN(1.D0)
            N1 = (N-1)/2
            N2 = N/2
         IF((2*N2).LT.N)THEN
C* POLES FOR ODD ORDER
             HBN=DCMPLX(1.D0,0.D0)
         DO 10 K=1,N1
            PSI(K)= PI*K/FLOAT(N)
             HBN =(W**2+2.D0*DCOS(PSI(K))*W*S+S**2)*HBN/S**2
 10     CONTINUE
              HBN = HBN*(W + S)
                TR = S/HBN
         ELSE
C* POLES FOR EVEN ORDER
             HBN=DCMPLX(1.D0,0.D0)
```

```
          DO 20 I=1,N2
             PSI(I)= PI*(2.D0*I-1.D0)/(2.D0*N)
              HBN =(W**2+2.D0*DCOS(PSI(I))*W*S+S**2)*HBN/S**2
 20     CONTINUE
                TR = 1.D0/HBN
          ENDIF
          RETURN
          END
C*********************************************
C**
          SUBROUTINE TRFNC(TR,W,S,ALPHA,BETA,N,AMAX,ROOT)
C**
C*   SUBROUTINE FOR OBTAINING THE TRANSFER FUNCTION
C*         OF THE CHEBYCHEV FILTER
C**
           COMPLEX*16 TR,S,HBN
           REAL*8 ALPHA1,W,B,B1,RIPL
           REAL*8 ALPHA(1),BETA(1),DN1,DN2
           REAL*8 ROOT(1),ROOTA,ROOTB,ROOTC,ROOTA1,ROOTA2
           PI    = 4.D0*DATAN(1.D0)
            EPS = SQRT(10.**(.1*AMAX)-1.)
            RIPL= 1.D0/DSQRT(1.D0 + EPS**2)
             A  = ARSINH(1./EPS)/FLOAT(N)
             N1 = (N-1)/2
             N2 = N/2
          IF((2*N2).LT.N)THEN
C* POLES FOR ODD ORDER
              HBN=DCMPLX(1.D0,0.D0)
              DN1=1.D0
          DO 10 K=1,N1
             B = (2.D0*K-1.D0)*PI/(2.D0*N)
           ALPHA(K) = SINH(A)*DSIN(B)
           BETA(K)  = COSH(A)*DCOS(B)
      HBN =(W**2+2.D0*ALPHA(K)*W*S+(ALPHA(K)**2+BETA(K)**2)*S**2)*
     *HBN/S**2
              DN1 =(ALPHA(K)**2 + BETA(K)**2)*DN1
 10     CONTINUE
              N3= N1+1
              B1= (2.D0*N3-1.D0)*PI/(2.D0*N)
              ALPHA1 = SINH(A)*DSIN(B1)
              DN2 = DN1*ALPHA1
               HBN = HBN*(W + ALPHA1*S)
                 TR = DN2*S/HBN
          ELSE
C* POLES FOR EVEN ORDER
              HBN=DCMPLX(1.D0,0.D0)
              DN1=1.D0
          DO 20 I=1,N2
```

```
            B = (2.D0*I-1.D0)*PI/(2.D0*N)
           ALPHA(I) = SINH(A)*DSIN(B)
           BETA(I)  = COSH(A)*DCOS(B)
         ROOTA  = ALPHA(I)**2 + BETA(I)**2
         ROOTB  = 2.D0*ALPHA(I)*W
         ROOTC  = W**2
         ROOTA1 = (ROOTB/(2.D0*ROOTA))**2
         ROOTA2 = DABS(ROOTB**2-4.D0*ROOTA*ROOTC)/((2.D0*ROOTA)**2)
         ROOT(I)= DSQRT(ROOTA1+ROOTA2)
      HBN =(W**2+2.D0*ALPHA(I)*W*S+(ALPHA(I)**2+BETA(I)**2)*S**2)*
     *HBN/S**2
           DN1 =(ALPHA(I)**2 + BETA(I)**2)*DN1
 20     CONTINUE
           DN2 = DN1*RIPL
              TR = DN2/HBN
        ENDIF
        RETURN
        END
C*********************************************
C***
        SUBROUTINE  LPCHEB(N,AMAX,RL,LLP,CLP)
C***
C*** SUBROUTINE WHICH COMPUTES THE VALUES OF CIRCUIT
C*** ELEMENTS IN THE LOW PASS CHEBYCHEV LADDER FILTER.
C***
        REAL*8    LLP(1),CLP(1),A1,A2,A3,A4
        REAL*8    PI,H1,H,RL,ZETA
        PI    = 4.D0*DATAN(1.D0)
         EPS = SQRT(10.0**(.1*AMAX)-1.0)
        H1  = DSQRT(1.D0+(1.D0/EPS**2))
         H   = (H1 + (1.D0/EPS))**(1./FLOAT(N))
        ZETA= (H-(1.D0/H))
                N2 = N/2
                ID = 2*N2
        DO 10 M=1,N2
             M2   = 2*M
             M3   = 4*M-3
             M4   = 4*M-1
             M5   = 2*M-1
             M6   = 2*M+1
             M7   = 4*M+1
           CLP(1)   = 4.D0*DSIN(PI/(2.D0*N))/ZETA
           A1= 16.D0*DSIN(M3*PI/(2.D0*N))*DSIN(M4*PI/(2.D0*N))
           A2= ZETA**2+4.D0*(DSIN(M5*PI/(1.D0*N)))**2
           LLP(M2)  = A1/(A2*CLP(M5))
           A3= 16.D0*DSIN(M4*PI/(2.D0*N))*DSIN(M7*PI/(2.D0*N))
           A4= ZETA**2+4.D0*(DSIN(M2*PI/(1.D0*N)))**2
           CLP(M6)  = A3/(A4*LLP(M2))
```

```
  10          CONTINUE
               IF(ID.LT.N)THEN
C* FOR ODD N RL=1
                   RL=1.DO
                   CLP(N) = 4.DO*DSIN(PI/(2.DO*N))/(ZETA*RL)
                ELSE
C* FOR EVEN N RL=VALUE FOR MAXIMUM POWER TRANSFER
                  RL = 1.DO+2.DO*EPS**2-2.DO*EPS*SQRT(1.0+EPS**2)
                  LLP(N) = 4.DO*RL*DSIN(PI/(2.DO*N))/ZETA
                ENDIF
              RETURN
              END
C*************************************************
C***
          SUBROUTINE  LPBUTW(N,LLP,CLP,RL)
          REAL*8   LLP(1),CLP(1),PI,RL
C***
C*** THE FOLLOWING PROGRAM COMPUTES THE VALUES OF CIRCUIT
C*** ELEMENTS IN THE LOW PASS LADDER BUTTERWORTH FILTERS.
C***
            PI = 4.DO*DATAN(1.DO)
            RL = 1.DO
          DO 30 K = 1,N,2
             K1  = K + 1
             K2  = 2*K-1
             K21 = 2*K1-1
             N2  = 2*N
             CLP(K) = 2.DO*DSIN(K2*PI/N2)
               IF(K1.GT.N)RETURN
                 LLP(K1) = 2.DO*DSIN(K21*PI/N2)
  30         CONTINUE
             RETURN
             END
C*************************************************
C*  SUBROUTINE FOR DRAWING THE FIRST BUILDING
C*  BLOCK OF THE MLDD TRANSFORMATION
C***
       SUBROUTINE BMLDD1(X,Y,F1)
       IP=3
       ID=2
         G1=1.0
         G2=2.0
          A1=0.20
          A2=0.20
          B=-0.068
           X1=X+2.2
           X2=X1+.3
           X3=X+2.4
```

```
            X5=X-.5
            X6=X-.05
            Y1=Y+.5
            Y2=Y1+1.4
C
C SEGMENT FOR DRAWING CONNECTIONS
C
C DRAW TO CONNECT F-DOPAMP  LEFT TOP
          CALL PLOT(10.8+X,6.1+Y,IP)
          CALL PLOT(8.9+X,6.1+Y,ID)
C DRAW TO CONNECT F-DOPAMP  LEFT BOTTOM
          CALL PLOT(8.9+X,3.+Y,IP)
          CALL PLOT(10.+X,3.+Y,ID)
C DRAW TO CONNECT S-OPAMP  BOTTOM
          CALL PLOT(10.2+X,.6+Y,IP)
          CALL PLOT(10.2+X,1.+Y,ID)
          CALL PLOT(7.0+X,.6+Y,IP)
          CALL PLOT(10.2+X,.6+Y,ID)
C DRAW TO CONNECT S-OPAMP TOP
          CALL PLOT(10.2+X,6.8+Y,IP)
          CALL PLOT(7.2+X,6.8+Y,ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT TOP
          CALL PLOT(10.2+X,6.8+Y,IP)
          CALL PLOT(10.2+X3,6.8+Y,ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.8+X,1.+Y,IP)
          CALL PLOT(10.8+X,.6+Y,ID)
          CALL PLOT(10.8+X3,.6+Y,ID)
C
C
C
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP
          CALL PLOT(10.2+X,6.1+Y1,IP)
          CALL PLOT(10.2+X2,6.1+Y1,ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.2+X,6.1+Y1,IP)
          CALL PLOT(10.2+X3,6.1+Y1,ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
          CALL PLOT(9.4+X1,3.+Y,IP)
          CALL PLOT(8.8+X1,3.+Y,ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM LINE
          CALL PLOT(9.4+X1,4.1+Y1,IP)
          CALL PLOT(9.4+X1,2.5+Y1,ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP  LINE LAST ONE
          CALL PLOT(10.2+X2,6.1+Y1,IP)
          CALL PLOT(10.2+X2,4.7+Y1,ID)
          CALL PLOT(10.2+X2,2.5+Y1,IP)
          CALL PLOT(10.2+X2,2.0+Y1,ID)
```

```
          CALL PLOT(8.5+X2,2.0+Y1,ID)
          CALL PLOT(8.5+X2,1.7+Y1,ID)
C
C CALL FOR DRAWING INPUT SWITCHES
C
          CALL VSW(10.2+X,3.+Y,G1)
          CALL HSWL(10.2+X,2.2+Y,G2)
          CALL CP(10.2+X,2.1+Y)
            CALL SYMBOL(10.25+X,2.2+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(10.25+X+A1,2.2+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(10.25+X+A2,2.2+Y+B,0.12,F1+1.,0.0,-1)
          CALL HSWL(10.2+X,1.8+Y,G1)
          CALL VSW(10.2+X,1.9+Y,G2)
          CALL DPUMLD(10.2+X,3.+Y)
          CALL VSW(10.8+X,3.+Y,G1)
          CALL HSWR(10.8+X,2.2+Y,G2)
          CALL CP(10.8+X,2.1+Y)
          CALL HSWR(10.8+X,1.8+Y,G1)
          CALL VSW(10.8+X,1.9+Y,G2)
          CALL FBCPL(10.2+X,4.4+Y)
            CALL SYMBOL(9.39+X,3.28+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.34+X+A1,3.27+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.34+X+A2,3.27+Y+B,0.12,F1+2.,0.0,-1)
          CALL FBCPR(10.8+X,4.4+Y)
            CALL SYMBOL(11.21+X,3.28+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(11.16+X+A1,3.27+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(11.16+X+A2,3.27+Y+B,0.12,F1+2.,0.0,-1)
C
C  CALL FOR DRAWING THE EXTRA CAPACITOR(C8)
C
          CALL PLOT(9.4+X6,6.1+Y,IP)
          CALL PLOT(9.4+X6,4.7+Y,ID)
          CALL CP(9.4+X6,4.7+Y)
            CALL SYMBOL(9.5+X6,4.75+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.5+X6+A1,4.75+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.5+X6+A2,4.75+Y+B,0.12,F1+8.,0.0,-1)
          CALL PLOT(9.4+X6,4.5+Y,IP)
          CALL PLOT(9.4+X6,3.0+Y,ID)
C
C  CALL FOR DRAWING THE NEGATIVE FEEDBACK SWITCHES
C
          CALL VSW(9.4+X5,6.1+Y,G2)
          CALL HSWL(9.4+X5,5.3+Y,G1)
          CALL CP(9.4+X5,5.2+Y)
            CALL SYMBOL(9.415+X5,5.25+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.415+X5+A1,5.25+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.415+X5+A2,5.25+Y+B,0.12,F1+4.,0.0,-1)
          CALL VSW(9.4+X5,5.0+Y,G1)
```

```
          CALL HSWL(9.4+X5,4.9+Y,G2)
          CALL CP(9.4+X5,4.1+Y)
            CALL SYMBOL(9.415+X5,4.15+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.415+X5+A1,4.15+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.415+X5+A2,4.15+Y+B,0.12,F1+6.,0.0,-1)
          CALL HSWL(9.4+X5,4.2+Y,G2)
          CALL HSWL(9.4+X5,3.8+Y,G1)
          CALL VSW(9.4+X5,3.9+Y,G2)
C
C   CALL FOR DRAWING THE POSITIVE FEEDBACK SWITCHES
C
          CALL VSW(9.4+X1,6.1+Y1,G1)
          CALL HSWR(9.4+X1,5.3+Y1,G2)
          CALL CP(9.4+X1,5.2+Y1)
            CALL SYMBOL(8.77+X1,4.9+Y1,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(8.77+X1+A1,4.9+Y1+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(8.77+X1+A2,4.9+Y1+B,0.12,F1+7.,0.0,-1)
          CALL VSW(9.4+X1,5.0+Y1,G2)
          CALL HSWR(9.4+X1,4.9+Y1,G1)
CCC   SECOND STAGE
          CALL VSW(10.2+X2,4.7+Y1,G1)
          CALL HSWL(10.2+X2,3.9+Y1,G2)
          CALL CP(10.2+X2,3.8+Y1)
            CALL SYMBOL(10.4+X2,3.7+Y1,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(10.4+X2+A1,3.7+Y1+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(10.4+X2+A2,3.7+Y1+B,0.12,F1+3.,0.0,-1)
          CALL HSWL(10.2+X2,3.5+Y1,G1)
          CALL VSW(10.2+X2,3.6+Y1,G2)
          CALL CP(10.2+X2,2.7+Y1)
            CALL SYMBOL(9.7+X2,2.3+Y1,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.7+X2+A1,2.3+Y1+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.7+X2+A2,2.3+Y1+B,0.12,F1+5.,0.0,-1)
          CALL HSWL(10.2+X2,2.8+Y1,G1)
        RETURN
        END
C*********************************************
C*  SUBROUTINE FOR DRAWING THE SECOND BUILDING
C*  BLOCK OF THE MLDD TRANSFORMATION
C***
        SUBROUTINE BMLDD2(X,Y,F2)
        IP=3
        ID=2
           A1=0.20
           A2=0.18
           B=-0.068
          G1=1.0
          G2=2.0
          X1=X+2.2
```

```
          X2=X1+.3
          X3=X+2.4
          Y1=Y+.5
C DRAW TO CONNECT F-DOPAMP  LEFT TOP
          CALL PLOT(10.8+X,(1.3+Y),IP)
          CALL PLOT(8.9+X,(1.3+Y),ID)
C DRAW TO CONNECT F-DOPAMP  LEFT BOTTOM
          CALL PLOT(8.9+X,4.4+Y,IP)
          CALL PLOT(10.+X,4.4+Y,ID)
C DRAW TO CONNECT D-OPAMP  BOTTOM
          CALL PLOT(7.8+X,(.6+Y),IP)
          CALL PLOT(10.2+X,(.6+Y),ID)
C DRAW TO CONNECT D-OPAMP TOP
          CALL PLOT(10.2+X,(6.8+Y),IP)
          CALL PLOT(7.4+X,(6.8+Y),ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT TOP
          CALL PLOT(10.8+X,(6.8+Y),IP)
          CALL PLOT(10.8+X3,(6.8+Y),ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.2+X,(.6+Y),IP)
          CALL PLOT(10.2+X3,(.6+Y),ID)
C
C
C
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP
          CALL PLOT(10.2+X,(.4+Y1),IP)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
C         CALL PLOT(10.2+X,(6.1+Y1),IP)
C         CALL PLOT(10.2+X3,(6.1+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
          CALL PLOT(9.4+X1,(4.4+Y),IP)
          CALL PLOT(8.9+X1,(4.4+Y),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM LINE
          CALL PLOT(9.4+X1,(3.9+Y1),IP)
          CALL PLOT(9.4+X1,(2.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP  LINE (LAST ONE)
          CALL PLOT(10.2+X2,(2.1+Y1),IP)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
          CALL PLOT(10.2+X2,(4.3+Y1),IP)
          CALL PLOT(10.2+X2,(4.8+Y1),ID)
          CALL PLOT(8.5+X2,(4.8+Y1),ID)
          CALL PLOT(8.5+X2,(5.1+Y1),ID)
C
C  CALL FOR DRAWING THE EXTRA CAPACITOR(C8)
C
            X6=X-.05
            YT=Y-1.7
```

```
      CALL PLOT(9.4+X6,6.1+YT,IP)
      CALL PLOT(9.4+X6,4.7+YT,ID)
      CALL CP(9.4+X6,4.7+YT)
        CALL SYMBOL(9.5+X6,4.20+YT,0.2,5HC     ,0.0,5)
C       CALL SYMBOL(9.5+X6+A1,4.20+YT+B,0.075,5HC     ,0.0,5)
        CALL NUMBER(9.5+X6+A2,4.20+YT+B,0.12,F2+8.,0.0,-1)
      CALL PLOT(9.4+X6,4.5+YT,IP)
      CALL PLOT(9.4+X6,3.0+YT,ID)
C
C CALL FOR DRAWING INPUT SWITCHES
C
        YS=Y+3.8
      CALL VSW(10.2+X,3.+YS,G1)
      CALL HSWL(10.2+X,2.2+YS,G2)
      CALL CP(10.2+X,2.1+YS)
        CALL SYMBOL(10.25+X,2.2+YS,0.2,5HC     ,0.0,5)
C       CALL SYMBOL(10.25+X+A1,2.2+YS+B,0.075,5HC     ,0.0,5)
        CALL NUMBER(10.25+X+A2,2.2+YS+B,0.12,F2+1.,0.0,-1)
      CALL HSWL(10.2+X,1.8+YS,G1)
      CALL VSW(10.2+X,1.9+YS,G2)
      CALL DPDMLD(10.2+X,3.+Y)
      CALL VSW(10.8+X,3.+YS,G1)
      CALL HSWR(10.8+X,2.2+YS,G2)
      CALL CP(10.8+X,2.1+YS)
      CALL HSWR(10.8+X,1.8+YS,G1)
      CALL VSW(10.8+X,1.9+YS,G2)
      CALL FBCPL(10.2+X,4.4+Y)
        CALL SYMBOL(9.39+X,3.92+Y,0.2,5HC     ,0.0,5)
C       CALL SYMBOL(9.34+X+A1,3.91+Y+B,0.075,5HC     ,0.0,5)
        CALL NUMBER(9.34+X+A2,3.91+Y+B,0.12,F2+2.,0.0,-1)
      CALL FBCPR(10.8+X,4.4+Y)
        CALL SYMBOL(11.21+X,3.92+Y,0.2,5HC     ,0.0,5)
C       CALL SYMBOL(11.16+X+A1,3.91+Y+B,0.075,5HC     ,0.0,5)
        CALL NUMBER(11.16+X+A2,3.91+Y+B,0.12,F2+2.,0.0,-1)
C
C  CALL FOR DRAWING THE NEGATIVE FEEDBACK SWITCHES
C
          X5=X-.5
          YT=Y-1.7
      CALL VSW(9.4+X5,6.1+YT,G1)
      CALL HSWL(9.4+X5,5.3+YT,G2)
      CALL CP(9.4+X5,5.2+YT)
        CALL SYMBOL(9.415+X5,5.25+YT,0.2,5HC     ,0.0,5)
C       CALL SYMBOL(9.415+X5+A1,5.25+YT+B,0.075,5HC     ,0.0,5)
        CALL NUMBER(9.415+X5+A2,5.25+YT+B,0.12,F2+6.,0.0,-1)
      CALL VSW(9.4+X5,5.0+YT,G2)
      CALL HSWL(9.4+X5,4.9+YT,G1)
      CALL CP(9.4+X5,4.1+YT)
```

```
            CALL SYMBOL(9.415+X5,3.55+YT,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.415+X5+A1,3.55+YT+B,0.075,5HC     ,0.0,5)
            CALL NUMBER(9.415+X5+A2,3.55+YT+B,0.12,F2+4.,0.0,-1)
          CALL HSWL(9.4+X5,4.2+YT,G1)
          CALL HSWL(9.4+X5,3.8+YT,G2)
          CALL VSW(9.4+X5,3.9+YT,G1)
C
C  CALL FOR DRAWING THE POSITIVE FEEDBACK SWITCHES
C
          YU=Y-3.7
          Y3=YU+.5
C         Y4=Y3+1.4
          CALL VSW(9.4+X1,6.1+Y3,G1)
          CALL HSWR(9.4+X1,5.3+Y3,G2)
          CALL CP(9.4+X1,5.2+Y3)
            CALL SYMBOL(8.77+X1,5.1+Y3,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(8.77+X1+A1,5.1+Y3+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(8.77+X1+A2,5.1+Y3+B,0.12,F2+7.,0.0,-1)
          CALL VSW(9.4+X1,5.0+Y3,G2)
          CALL HSWR(9.4+X1,4.9+Y3,G1)
CCC   SECOND STAGE
          Y8=Y+.1
          CALL CP(10.2+X2,4.7+Y8)
            CALL SYMBOL(9.7+X2,4.85+Y8,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.7+X2+A1,4.85+Y8+B,0.12,5HC     ,0.0,5)
            CALL NUMBER(9.7+X2+A2,4.85+Y8+B,0.12,F2+5.,0.0,-1)
          CALL HSWL(10.2+X2,4.4+Y8,G2)
          CALL VSW(10.2+X2,4.5+Y8,G1)
          CALL HSWL(10.2+X2,3.7+Y8,G2)
          CALL CP(10.2+X2,3.6+Y8)
            CALL SYMBOL(10.3+X2,3.1+Y8,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(10.3+X2+A1,3.1+Y8+B,0.075,5HC     ,0.0,5)
            CALL NUMBER(10.3+X2+A2,3.1+Y8+B,0.12,F2+3.,0.0,-1)
          CALL HSWL(10.2+X2,3.3+Y8,G1)
          CALL VSW(10.2+X2,3.4+Y8,G2)
        RETURN
        END
C*********************************************
C*  SUBROUTINE FOR DRAWING THE RESISTIVE SOURCE
C*  TERMINATION OF THE MLDD BUILDING BLOCKS.
C***
         SUBROUTINE RSMLDD(X,Y)
          IP=3
          ID=2
          G1=1.0
          G2=2.0
           A =0.28
           A1=0.18
```

```
      B=-0.068
       CALL SYMBOL(6.1+X,7.2+Y,0.3,5HV     ,0.0,5)
       CALL SYMBOL(6.1+X+A-.05,7.2+B+Y,0.15,5HIN    ,0.0,5)
      CALL PLOT(7.+X,7.4+Y,IP)
      CALL CIRCLE(7.+X,7.4+Y,0.,360.,.075,5)
      CALL PLOT(7.+X,7.4+Y,IP)
      CALL PLOT(7.7+X,7.4+Y,ID)
      CALL PLOT(7.7+X,7.+Y,ID)
      CALL VSW(7.7+X,7.+Y,G1)
      CALL PLOT(7.7+X,6.3+Y,IP)
      CALL PLOT(8.2+X,6.3+Y,ID)
      CALL PLOT(8.2+X,7.4+Y,IP)
      CALL PLOT(8.2+X,7.2+Y,ID)
      CALL VSW(8.2+X,7.2+Y,G2)
      CALL CP(7.7+X,6.1+Y)
       CALL SYMBOL(7.0+X,6.0+Y,0.2,5HC     ,0.0,5)
       CALL SYMBOL(7.0+A1+X,6.0+B+Y,0.12,5HRS1   ,0.0,5)
      CALL VSW(7.7+X,5.9,G2+Y)
      CALL HSWR(7.7+X,5.8,G1+Y)
      CALL SAMPD(7.7+X,5.0+Y)
      CALL FBCPL(7.7+X,5.0+Y)
      CALL PLOT(7.+X,5.0+Y,ID)
      CALL PLOT(7.+X,4.75+Y,ID)
      CALL VSW(7.+X,4.75+Y,G1)
       CALL SYMBOL(7.36+X,3.88+Y,0.2,5HC     ,0.0,5)
       CALL SYMBOL(7.36+A1+X,3.88+B+Y,0.12,5HRS2   ,0.0,5)
      CALL PLOT(7.+X,3.85+Y,IP)
      CALL PLOT(7.+X,3.6+Y,ID)
      CALL PLOT(8.+X,3.6+Y,ID)
      CALL PLOT(8.+X,3.8+Y,ID)
      CALL PLOT(8.+X,1.2+Y,ID)
      RETURN
      END
C*****************************************************
C  SUBROUTINE FOR DRAWING VERTICAL SWITCH
C  STARTING POINT : TOP OF SWITCH
C  MOVEMENT       : IN DECREASING VERTICAL DIRECTION
C  LENGTH         : 0.9 CM
C***
      SUBROUTINE VSW(X,Y,G)
        IP=3
        ID=2
        X1=X-.1
        X2=X-.27
        Y1=Y-.3
        Y2=Y1-.3
        Y3=Y2-.3
        Y4=Y1-.25
```

```
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,IP)
          CALL PLOT(X,Y2,ID)
          CALL PLOT(X,Y3,ID)
          CALL PLOT(X,Y,IP)
            CALL NUMBER(X2,Y4,.15,G,0.0,-1)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING FEEDBACK CAPACITOR LEFT
C  STARTING POINT : TOP OF FEEDBACK CAPACITOR
C  MOVEMENT       : IN DECREASING VERTICAL DIRECTION
C  LENGTH         : 1.4 CM
C  LOCATION       : MIDDLE OF OP-AMP,LEFT SIDE
C***
        SUBROUTINE FBCPL(X,Y)
          IP=3
          ID=2
          X1=X-.4
          Y1=Y-.6
          Y2=Y1-.2
          Y3=Y2-.6
          CALL PLOT(X,Y,IP)
          CALL PLOT(X1,Y,ID)
          CALL PLOT(X1,Y1,ID)
          CALL CP(X1,Y1)
          CALL PLOT(X1,Y2,IP)
          CALL PLOT(X1,Y3,ID)
          CALL PLOT(X,Y3,ID)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING FEEDBACK CAPACITOR RIGHT
C  STARTING POINT : TOP OF FEEDBACK CAPACITOR
C  MOVEMENT       : IN DECREASING VERTICAL DIRECTION
C  LENGTH         : 1.4 CM
C  LOCATION       : MIDDLE OF OP-AMP,RIGHT SIDE
C***
        SUBROUTINE FBCPR(X,Y)
          IP=3
          ID=2
          X1=X+.4
          Y1=Y-.6
          Y2=Y1-.2
          Y3=Y2-.6
          CALL PLOT(X,Y,IP)
```

```
          CALL PLOT(X1,Y,ID)
          CALL PLOT(X1,Y1,ID)
          CALL CP(X1,Y1)
          CALL PLOT(X1,Y2,IP)
          CALL PLOT(X1,Y3,ID)
          CALL PLOT(X,Y3,ID)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING CAPACITOR
C  STARTING POINT : TOP OF CAPACITOR
C  MOVEMENT       : IN DECREASING VERTICAL DIRECTION
C  LENGTH         : 0.2 CM
C***
        SUBROUTINE CP(X,Y)
          IP=3
          ID=2
          Y1=Y-.05
          Y2=Y1-.1
          Y3=Y2-.05
          X1=X-.15
          X2=X+.15
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,IP)
          CALL PLOT(X2,Y1,ID)
          CALL PLOT(X1,Y2,IP)
          CALL PLOT(X2,Y2,ID)
          CALL PLOT(X,Y2,IP)
          CALL PLOT(X,Y3,ID)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROUTINE FOR DRAWING HORIZONTAL SWITCH  TO THE RIGHT
C  STARTING POINT : LEFT SIDE  OF SWITCH
C  MOVEMENT       : IN INCREASING HORIZANTAL DIRECTION
C  LENGTH         : 0.9 CM
C***
        SUBROUTINE HSWR(X,Y,G)
          IP=3
          ID=2
          G1=1.0
          G2=2.0
          Y1=Y+.1
          Y2=Y-.1
          Y3=Y+.1
```

```
          Y4=Y+.07
          X1=X+.3
          X2=X1+.3
          X3=X2+.3
          X4=X2+.08
          CALL PLOT(X,Y,IP)
          CALL PLOT(X1,Y,ID)
          CALL PLOT(X2,Y1,ID)
          CALL PLOT(X2,Y,IP)
          CALL PLOT(X3,Y,ID)
          CALL PLOT(X3,Y2,IP)
          CALL PLOT(X3,Y3,ID)
            CALL NUMBER(X4,Y4,.15,G,0.0,-1)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING HORIZONTAL SWITCH TO THE LEFT
C  STARTING POINT : RIGHT SIDE  OF SWITCH
C  MOVEMENT       : IN DECREASING HORIZANTAL DIRECTION
C  LENGTH         : 0.9 CM
C***
        SUBROUTINE HSWL(X,Y,G)
          IP=3
          ID=2
          G1=1.0
          G2=2.0
          Y1=Y+.1
          Y2=Y-.1
          Y3=Y+.1
          Y4=Y+.07
          X1=X-.3
          X2=X1-.3
          X3=X2-.3
          X4=X2-.22
          CALL PLOT(X,Y,IP)
          CALL PLOT(X1,Y,ID)
          CALL PLOT(X2,Y1,ID)
          CALL PLOT(X2,Y,IP)
          CALL PLOT(X3,Y,ID)
          CALL PLOT(X3,Y2,IP)
          CALL PLOT(X3,Y3,ID)
            CALL NUMBER(X4,Y4,.15,G,0.0,-1)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING SINGLE OUTPUT OPAMP  DOWN
```

```
C  AREA             : 1.0 CM  SQUARE
C  STARTING POINT   : INVERTING INPUT
C  MOVEMENT         : IN DECREASING VERTICAL DIRECTION
C  WITH INPUT AND OUTPUT CONNECTIONS
       SUBROUTINE SAMPD(X,Y)
         IP=3
         ID=2
         Y1=Y-.2
         Y2=Y1-1.
         Y3=Y-.15
         Y4=Y3+.3
         Y5=Y1-.2
         Y6=Y5
         X1=X-.2
         X2=X1+.5
         X3=X1+1.
         X4=X3-.2
         X5=X-.075
         X6=X5+.6
         CALL PLOT(X,Y,IP)
         CALL PLOT(X,Y1,ID)
         CALL PLOT(X1,Y1,ID)
         CALL PLOT(X2,Y2,ID)
         CALL PLOT(X3,Y1,ID)
         CALL PLOT(X4,Y1,ID)
         CALL PLOT(X4,Y,ID)
         CALL PLOT(X3,Y,ID)
         CALL PLOT(X3,Y3,IP)
         CALL PLOT(X3,Y4,ID)
         CALL PLOT(X4,Y1,IP)
         CALL PLOT(X,Y1,ID)
         CALL SYMBOL(X5,Y5,.15,2H- ,0.0,2)
         CALL SYMBOL(X6,Y6,.15,2H+ ,0.0,2)
         CALL PLOT(X,Y,IP)
       RETURN
       END
C*********************************************
C  SUBROTINE FOR DRAWING DOUBLE OUTPUT OPAMP UP
C  AREA             : 1.0 CM  SQUARE
C  STARTING POINT   : INVERTING INPUT
C  MOVEMENT         : IN INCREASING VERTICAL DIRECTION
C  WITH INPUT AND OUTPUT CONNECTIONS
       SUBROUTINE DPUMLD(X,Y)
         IP=3
         ID=2
         Y1=Y+.2
         Y2=Y1+1.
         Y3=Y+.6
```

```
          Y4=Y3+3.2
C Y9 FOR -VE OUTPUT
          Y9=Y3+2.5
          Y5=Y+.2
          Y6=Y1+.15
          X1=X-.2
          X2=X1+.5
          X3=X1+1.
          X4=X3-.2
          X5=X-.075+.05
          X51=X-.075
          X6=X51+.6
          X7=X+.6
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,ID)
          CALL PLOT(X2,Y2,ID)
          CALL PLOT(X3,Y1,ID)
          CALL PLOT(X4,Y1,ID)
          CALL PLOT(X4,Y,ID)
          CALL PLOT(X4,Y1,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X,Y3,IP)
          CALL PLOT(X,Y4,ID)
          CALL PLOT(X7,Y3,IP)
          CALL PLOT(X7,Y9,ID)
          CALL PLOT(X,Y,IP)
          CALL SYMBOL(X5,Y5,.15,2H- ,0.0,2)
          CALL SYMBOL(X6,Y5,.15,2H+ ,0.0,2)
          CALL SYMBOL(X5,Y6,.15,2H+ ,0.0,2)
          CALL SYMBOL(X6,Y6,.15,2H- ,0.0,2)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING DOUBLE OUTPUT OPAMP DOWN
C  AREA            : 1.0 CM  SQUARE
C  STARTING POINT  : INVERTING INPUT
C  MOVEMENT        : IN DECREASING VERTICAL DIRECTION
C  WITH INPUT AND OUTPUT CONNECTIONS
        SUBROUTINE DPDMLD(X,Y)
          IP=3
          ID=2
          Y =Y+1.4
          Y1=Y-.2
          Y2=Y1-1.
          Y3=Y-.6
          Y4=Y3-3.2
```

```
C Y9 FOR +VE OUTPUT
          Y9=Y3-2.5
          Y5=Y-.4
          Y6=Y1-.35
          X1=X-.2
          X2=X1+.5
          X3=X1+1.
          X4=X3-.2
          X5=X-.075+.05
          X51=X-.075
          X6=X51+.6
          X7=X+.6
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,ID)
          CALL PLOT(X2,Y2,ID)
          CALL PLOT(X3,Y1,ID)
          CALL PLOT(X4,Y1,ID)
          CALL PLOT(X4,Y,ID)
          CALL PLOT(X4,Y1,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X,Y3,IP)
          CALL PLOT(X,Y4,ID)
          CALL PLOT(X7,Y3,IP)
          CALL PLOT(X7,Y9,ID)
          Y10=Y+.4
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y10,ID)
          CALL PLOT(X7,Y,IP)
          CALL PLOT(X7,Y10,ID)
          CALL SYMBOL(X5,Y5,.15,2H- ,0.0,2)
          CALL SYMBOL(X6,Y5,.15,2H+ ,0.0,2)
          CALL SYMBOL(X5,Y6,.15,2H+ ,0.0,2)
          CALL SYMBOL(X6,Y6,.15,2H- ,0.0,2)
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*************************************************
C*
C* BUILDING BLOCK 1 FOR MODIFIED BILINEAR
C*              TRANFORMATION
C*
        SUBROUTINE BMBIL1(X,Y,F1)
        IP=3
        ID=2
          G1=1.0
          G2=2.0
           A1=0.20
```

```
          A2=0.20
          B=-0.068
           X1=X+2.4
           X2=X1+.3
           X3=X+2.4+.6
           XC3=X+2.4
           X5=X-.1
           X6=X5-2.0
           X7=X-.05
           Y1=Y+.5
           Y2=Y1+1.4
           Y3=Y+0.3
C
C SEGMENT FOR DRAWING CONNECTIONS
C
C DRAW TO CONNECT F-DOPAMP  LEFT TOP
         CALL PLOT(10.8+X,6.1+Y1,IP)
         CALL PLOT(8.1+X,6.1+Y1,ID)
         CALL PLOT(8.1+X,4.7+Y1,ID)
C DRAW TO CONNECT F-DOPAMP  LEFT BOTTOM
         CALL PLOT(9.0+X,3.+Y,IP)
         CALL PLOT(10.+X,3.+Y,ID)
C DRAW TO CONNECT D-OPAMP  BOTTOM
         CALL PLOT(10.2+X,.6+Y,IP)
         CALL PLOT(10.2+X,1.+Y,ID)
         CALL PLOT(7.0+X,.6+Y,IP)
         CALL PLOT(10.2+X,.6+Y,ID)
C DRAW TO CONNECT D-OPAMP TOP
         CALL PLOT(10.2+X,6.8+Y,IP)
         CALL PLOT(7.2+X,6.8+Y,ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT TOP
         CALL PLOT(10.2+X,6.8+Y,IP)
         CALL PLOT(10.2+X3,6.8+Y,ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT BOTTOM
         CALL PLOT(10.8+X,1.+Y,IP)
         CALL PLOT(10.8+X,.6+Y,ID)
         CALL PLOT(10.8+X,.6+Y,IP)
         CALL PLOT(10.8+X3,.6+Y,ID)
C
C
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP
         CALL PLOT(10.2+X,6.1+Y,IP)
         CALL PLOT(10.2+X2,6.1+Y,ID)
         CALL PLOT(10.2+X2,6.1+Y,IP)
         CALL PLOT(10.2+X2,4.7+Y,ID)
C
C CALL FOR DRAWING INPUT CAPACITORS
C
```

```
          CALL PLOT(10.2+X,1.0+Y,IP)
          CALL PLOT(10.2+X,1.9+Y,ID)
          CALL PLOT(10.2+X,2.1+Y,IP)
          CALL PLOT(10.2+X,3.0+Y,ID)
          CALL CP(10.2+X,2.1+Y)
            CALL SYMBOL(9.50+X,2.0+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.50+X+A1,2.0+Y+B,0.125,5HL     ,0.0,5)
            CALL NUMBER(9.50+X+A2,2.0+Y+B,0.12,F1+1.,0.0,-1)
          CALL CP(10.8+X,2.1+Y)
            CALL SYMBOL(11.05+X,2.0+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(11.05+X+A1,2.0+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(11.05+X+A2,2.0+Y+B,0.12,F1+1.,0.0,-1)
          CALL PLOT(10.8+X,1.0+Y,IP)
          CALL PLOT(10.8+X,1.9+Y,ID)
          CALL PLOT(10.8+X,2.1+Y,IP)
          CALL PLOT(10.8+X,3.0+Y,ID)
C
          CALL DPUMBL(10.2+X,3.+Y)
          CALL FBCPL(10.2+X,4.4+Y)
            CALL SYMBOL(9.30+X,3.28+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.25+X+A1,3.27+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.25+X+A2,3.27+Y+B,0.12,F1+2.,0.0,-1)
          CALL FBCPR(10.8+X,4.4+Y)
            CALL SYMBOL(11.28+X,3.28+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(11.24+X+A1,3.27+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(11.24+X+A2,3.27+Y+B,0.12,F1+2.,0.0,-1)
C
C   CALL FOR DRAWING THE +VE FEEDBACK SWITCHES
C
          CALL VSW(9.3+X5,6.1+Y1,G2)
          CALL HSWL(9.3+X5,5.3+Y1,G1)
          CALL CP(9.3+X5,5.2+Y1)
            CALL SYMBOL(9.415+X5,5.25+Y1,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.415+X5+A1,5.25+Y1+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.415+X5+A2,5.25+Y1+B,0.12,F1+3.,0.0,-1)
          CALL VSW(9.3+X5,5.0+Y1,G1)
          CALL HSWL(9.3+X5,4.9+Y1,G2)
          CALL PLOT(9.3+X5,4.1+Y1,IP)
          CALL PLOT(9.3+X5,2.5+Y1,ID)
CCC   SECOND STAGE
          CALL VSW(10.2+X6,4.7+Y1,G1)
          CALL HSWR(10.2+X6,3.9+Y1,G2)
          CALL CP(10.2+X6,3.8+Y1)
            CALL SYMBOL(9.5+X6,3.7+Y1,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(9.5+X6+A1,3.7+Y1+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(9.5+X6+A2,3.7+Y1+B,0.12,F1+3.,0.0,-1)
          CALL HSWR(10.2+X6,3.5+Y1,G1)
          CALL VSW(10.2+X6,3.6+Y1,G2)
```

```
          CALL PLOT(10.2+X6,2.7+Y1,IP)
          CALL PLOT(10.2+X6,2.5+Y1,ID)
          CALL PLOT(11.2+X6,2.5+Y1,ID)
C
C  CALL FOR DRAWING THE -VE FEEDBACK SWITCHES
C
          CALL VSW(9.4+X1,6.1+Y,G1)
          CALL HSWR(9.4+X1,5.3+Y,G2)
          CALL CP(9.4+X1,5.2+Y)
            CALL SYMBOL(8.77+X1,4.9+Y,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(8.77+X1+A1,4.9+Y+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(8.77+X1+A2,4.9+Y+B,0.12,F1+3.,0.0,-1)
          CALL VSW(9.4+X1,5.0+Y,G2)
          CALL HSWR(9.4+X1,4.9+Y,G1)
          CALL PLOT(9.4+X1,4.1+Y,IP)
          CALL PLOT(9.4+X1,2.7+Y3,ID)
CCC   SECOND STAGE
          CALL VSW(10.2+X2,4.7+Y3,G2)
          CALL HSWL(10.2+X2,3.9+Y3,G1)
          CALL CP(10.2+X2,3.8+Y3)
            CALL SYMBOL(10.4+X2,3.7+Y3,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(10.4+X2+A1,3.7+Y3+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(10.4+X2+A2,3.7+Y3+B,0.12,F1+3.,0.0,-1)
          CALL HSWL(10.2+X2,3.5+Y3,G2)
          CALL VSW(10.2+X2,3.6+Y3,G1)
          CALL PLOT(10.2+X2,2.7+Y3,IP)
          CALL PLOT(8.4+X2,2.7+Y3,ID)
        RETURN
        END
C*********************************************
C*
C* BUILDING BLOCK 2 FOR MODIFIED BILINEAR
C*              TRANFORMATION
C*
C*
        SUBROUTINE BMBIL2(X,Y,F2)
        IP=3
        ID=2
           A1=0.20
           A2=0.18
           B=-0.068
          G1=1.0
          G2=2.0
            X1=X+2.4
          X2=X1+.3
          X3=X+2.4+.6
          XC3=X+2.4
          X5=X-.1
```

```
          X6=X5-2.0
          YT=Y-1.7
          YT1=Y-1.7-0.4
          YT3=YT1+0.3
          Y8=Y-.1
          Y1=Y+.5+0.4
          YU=Y-3.7
          Y3=YU+.5+0.4
          YS=Y+3.8
C DRAW TO CONNECT F-DOPAMP  LEFT TOP
          CALL PLOT(10.+X,4.4+Y,IP)
          CALL PLOT(8.1+X,4.4+Y,ID)
          CALL PLOT(8.1+X,4.7+YT3,ID)
C DRAW TO CONNECT D-OPAMP  BOTTOM
          CALL PLOT(7.8+X,(.6+Y),IP)
          CALL PLOT(10.2+X,(.6+Y),ID)
C DRAW TO CONNECT D-OPAMP TOP
          CALL PLOT(10.2+X,(6.8+Y),IP)
          CALL PLOT(7.4+X,(6.8+Y),ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT TOP
          CALL PLOT(10.8+X,(6.8+Y),IP)
          CALL PLOT(10.8+X3,(6.8+Y),ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.2+X,(.6+Y),IP)
          CALL PLOT(10.2+X3,(.6+Y),ID)
C
C
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.2+X,(.4+Y1),IP)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT VERTICAL LINE
          CALL PLOT(9.4+X1,(3.5+Y1),IP)
          CALL PLOT(9.4+X1,(2.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM LINE
          CALL PLOT(10.2+X2,(1.5+Y1),IP)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
          CALL PLOT(10.2+X2,(.4+Y1),IP)
          CALL PLOT(10.2+XC3,(.4+Y1),ID)
C
C CALL FOR DRAWING INPUT CAPACITORS
C
          CALL PLOT(10.2+X,1.0+YS,IP)
          CALL PLOT(10.2+X,1.9+YS,ID)
          CALL PLOT(10.2+X,2.1+YS,IP)
          CALL PLOT(10.2+X,3.0+YS,ID)
          CALL CP(10.2+X,2.1+YS)
            CALL SYMBOL(9.50+X,2.0+YS,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(9.50+X+A1,2.0+YS+B,0.075,5HL    ,0.0,5)
```

```
            CALL NUMBER(9.50+X+A2,2.0+YS+B,0.12,F2+1.,0.0,-1)
          CALL CP(10.8+X,2.1+YS)
            CALL SYMBOL(11.05+X,2.0+YS,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(11.05+X+A1,2.0+YS+B,0.075,5HL    ,0.0,5)
            CALL NUMBER(11.05+X+A2,2.0+YS+B,0.12,F2+1.,0.0,-1)
          CALL PLOT(10.8+X,1.0+YS,IP)
          CALL PLOT(10.8+X,1.9+YS,ID)
          CALL PLOT(10.8+X,2.1+YS,IP)
          CALL PLOT(10.8+X,3.0+YS,ID)
C
          CALL DPDMBL(10.2+X,3.+Y)
          CALL FBCPL(10.2+X,4.4+Y)
            CALL SYMBOL(9.30+X,3.98+Y,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(9.25+X+A1,3.97+Y+B,0.075,5HL    ,0.0,5)
            CALL NUMBER(9.25+X+A2,3.97+Y+B,0.12,F2+2.,0.0,-1)
          CALL FBCPR(10.8+X,4.4+Y)
            CALL SYMBOL(11.28+X,3.98+Y,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(11.24+X+A1,3.97+Y+B,0.075,5HL    ,0.0,5)
            CALL NUMBER(11.24+X+A2,3.97+Y+B,0.12,F2+2.,0.0,-1)
C
C   CALL FOR DRAWING THE +VE FEEDBACK SWITCHES
C
          CALL VSW(9.3+X5,6.1+YT,G2)
          CALL HSWL(9.3+X5,5.3+YT,G1)
          CALL CP(9.3+X5,5.2+YT)
            CALL SYMBOL(9.415+X5,4.75+YT,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(9.415+X5+A1,4.75+YT+B,0.075,5HL    ,0.0,5)
            CALL NUMBER(9.415+X5+A2,4.75+YT+B,0.12,F2+3.,0.0,-1)
          CALL VSW(9.3+X5,5.0+YT,G1)
          CALL HSWL(9.3+X5,4.9+YT,G2)
          CALL PLOT(9.3+X5,4.1+YT,IP)
          CALL PLOT(9.3+X5,2.7+YT3,ID)
C         CALL PLOT(9.7+X5,3.0+YT,ID)
CCC   SECOND STAGE
          CALL VSW(10.2+X6,4.7+YT3,G1)
          CALL HSWR(10.2+X6,3.9+YT3,G2)
          CALL CP(10.2+X6,3.8+YT3)
            CALL SYMBOL(9.5+X6,3.7+YT3,0.2,5HC    ,0.0,5)
C           CALL SYMBOL(9.5+X6+A1,3.7+YT3+B,0.075,5HL    ,0.0,5)
            CALL NUMBER(9.5+X6+A2,3.7+YT3+B,0.12,F2+3.,0.0,-1)
          CALL HSWR(10.2+X6,3.5+YT3,G1)
          CALL VSW(10.2+X6,3.6+YT3,G2)
          CALL PLOT(10.2+X6,2.7+YT3,IP)
          CALL PLOT(12.9+X6,2.7+YT3,ID)
C
C   CALL FOR DRAWING THE -VE FEEDBACK SWITCHES
C
          CALL VSW(9.4+X1,6.1+Y3,G1)
```

```
          CALL HSWR(9.4+X1,5.3+Y3,G2)
          CALL CP(9.4+X1,5.2+Y3)
            CALL SYMBOL(8.77+X1,5.1+Y3,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(8.77+X1+A1,5.1+Y3+B,0.075,5HL     ,0.0,5)
            CALL NUMBER(8.77+X1+A2,5.1+Y3+B,0.12,F2+3.,0.0,-1)
          CALL VSW(9.4+X1,5.0+Y3,G2)
          CALL HSWR(9.4+X1,4.9+Y3,G1)
CCC   SECOND STAGE
          CALL VSW(10.2+X2,4.5+Y8,G2)
          CALL HSWL(10.2+X2,3.7+Y8,G1)
          CALL CP(10.2+X2,3.6+Y8)
            CALL SYMBOL(10.3+X2,3.1+Y8,0.2,5HC     ,0.0,5)
C           CALL SYMBOL(10.3+X2+A1,3.1+Y8+B,0.075,5HC     ,0.0,5)
            CALL NUMBER(10.3+X2+A2,3.1+Y8+B,0.12,F2+3.,0.0,-1)
          CALL HSWL(10.2+X2,3.3+Y8,G2)
          CALL VSW(10.2+X2,3.4+Y8,G1)
          CALL PLOT(8.8+X1,4.4+Y,IP)
          CALL PLOT(10.2+X2,4.4+Y,ID)
        RETURN
        END
C*************************************************
C**
C** SUBROUTINE FOR RESISTIVE SOURCE TERMINATION
C** OF THE MODIFIED BILINEAR TRANSFORMATION.
C**
        SUBROUTINE RSMBIL(X,Y)
        IP=3
        ID=2
           A =0.28
           A1=0.20
           A2=0.18
           B=-0.068
          G1=1.0
          G2=2.0
            X1=X+2.4
          X2=X1+.3
          X3=X+2.4+.6
          XC3=X+2.4
          X5=X-.1
          X6=X5-2.0
          YT=Y-1.7
          YT3=YT+0.3
          Y1=Y+.5
          YU=Y-3.7
          Y3=YU+.5
          YS=Y+3.8
C DRAW TO CONNECT F-DOPAMP  LEFT BOTTOM
          CALL PLOT(10.2+X,1.3+Y,IP)
```

```
          CALL PLOT(8.1+X,1.3+Y,ID)
C DRAW TO CONNECT F-DOPAMP  LEFT TOP
          CALL PLOT(10.+X,4.4+Y,IP)
          CALL PLOT(8.1+X,4.4+Y,ID)
          CALL PLOT(8.1+X,3.3+Y,ID)
C DRAW TO CONNECT D-OPAMP TOP
          CALL PLOT(10.2+X,(6.8+Y),IP)
          CALL PLOT(7.4+X,(6.8+Y),ID)
            CALL SYMBOL(6.5+X,6.6+Y,0.3,5HV     ,0.0,5)
            CALL SYMBOL(6.45+X+A,6.6+Y+B,0.15,5HIN    ,0.0,5)
          CALL PLOT(7.4+X,6.8+Y,IP)
          CALL CIRCLE(7.4+X,6.8+Y,0.,360.,.075,5)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT TOP
          CALL PLOT(10.8+X,(6.8+Y),IP)
          CALL PLOT(10.8+X3,(6.8+Y),ID)
C DRAW TO CONNECT TO THE NEXT -DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.8+X,(.6+Y),IP)
          CALL PLOT(10.2+X3,(.6+Y),ID)
C
C
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM
          CALL PLOT(10.8+X,Y1+1.0,IP)
          CALL PLOT(10.8+X,(.4+Y1),ID)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT BOTTOM LINE
          CALL PLOT(9.4+X1,(3.9+Y1),IP)
          CALL PLOT(9.4+X1,(2.4+Y1),ID)
C DRAW TO CONNECT F-DOPAMP  RIGHT TOP  LINE
          CALL PLOT(10.2+X2,(2.1+Y1),IP)
          CALL PLOT(10.2+X2,(.4+Y1),ID)
          CALL PLOT(10.2+X2,(.4+Y1),IP)
          CALL PLOT(10.2+XC3,(.4+Y1),ID)
C
C CALL FOR DRAWING INPUT CAPACITORS
C
          CALL PLOT(10.2+X,1.0+YS,IP)
          CALL PLOT(10.2+X,1.9+YS,ID)
          CALL PLOT(10.2+X,2.1+YS,IP)
          CALL PLOT(10.2+X,3.0+YS,ID)
          CALL CP(10.2+X,2.1+YS)
            CALL SYMBOL(9.30+X,2.0+YS,0.2,5HC     ,0.0,5)
            CALL SYMBOL(9.30+X+A1,2.0+YS+B,0.125,5HRS1  ,0.0,5)
          CALL CP(10.8+X,2.1+YS)
            CALL SYMBOL(11.05+X,2.0+YS,0.2,5HC     ,0.0,5)
            CALL SYMBOL(11.05+X+A1,2.0+YS+B,0.125,5HRS1  ,0.0,5)
          CALL PLOT(10.8+X,1.0+YS,IP)
          CALL PLOT(10.8+X,1.9+YS,ID)
          CALL PLOT(10.8+X,2.1+YS,IP)
```

```
          CALL PLOT(10.8+X,3.0+YS,ID)
C
          CALL DPDMBL(10.2+X,3.+Y)
          CALL FBCPL(10.2+X,4.4+Y)
            CALL SYMBOL(9.24+X,3.98+Y,0.2,5HC     ,0.0,5)
            CALL SYMBOL(9.19+X+A1,3.97+Y+B,0.125,5HRS2   ,0.0,5)
          CALL FBCPR(10.8+X,4.4+Y)
            CALL SYMBOL(11.24+X,3.98+Y,0.2,5HC     ,0.0,5)
            CALL SYMBOL(11.20+X+A1,3.97+Y+B,0.125,5HRS2   ,0.0,5)
C
C   CALL FOR DRAWING THE +VE FEEDBACK SWITCHES
C
          CALL VSW(9.3+X5,6.1+YT,G2)
          CALL HSWL(9.3+X5,5.3+YT,G1)
          CALL CP(9.3+X5,5.2+YT)
            CALL SYMBOL(9.415+X5,4.60+YT,0.2,5HC     ,0.0,5)
            CALL SYMBOL(9.415+X5+A1,4.60+YT+B,0.125,5HRS2   ,0.0,5)
          CALL VSW(9.3+X5,5.0+YT,G1)
          CALL HSWL(9.3+X5,4.9+YT,G2)
          CALL PLOT(9.3+X5,4.1+YT,IP)
          CALL PLOT(9.3+X5,3.0+YT,ID)
          CALL PLOT(9.7+X5,3.0+YT,ID)
CCC   SECOND STAGE
          CALL VSW(10.2+X6,4.7+YT3,G1)
          CALL HSWR(10.2+X6,3.9+YT3,G2)
          CALL CP(10.2+X6,3.8+YT3)
            CALL SYMBOL(9.4+X6,3.7+YT3,0.2,5HC     ,0.0,5)
            CALL SYMBOL(9.4+X6+A1,3.7+YT3+B,0.125,5HRS2   ,0.0,5)
          CALL HSWR(10.2+X6,3.5+YT3,G2)
          CALL VSW(10.2+X6,3.6+YT3,G1)
          CALL PLOT(10.2+X6,2.7+YT3,IP)
          CALL PLOT(11.3+X6,2.7+YT3,ID)
C
C   CALL FOR DRAWING THE -VE FEEDBACK SWITCHES
C
          CALL VSW(9.4+X1,6.1+Y3,G1)
          CALL HSWR(9.4+X1,5.3+Y3,G2)
          CALL CP(9.4+X1,5.2+Y3)
            CALL SYMBOL(8.57+X1,5.1+Y3,0.2,5HC     ,0.0,5)
            CALL SYMBOL(8.57+X1+A1,5.1+Y3+B,0.125,5HRS2   ,0.0,5)
          CALL VSW(9.4+X1,5.0+Y3,G2)
          CALL HSWR(9.4+X1,4.9+Y3,G1)
CCC   SECOND STAGE
          Y8=Y-.1
          CALL VSW(10.2+X2,4.5+Y8,G2)
          CALL HSWL(10.2+X2,3.7+Y8,G1)
          CALL CP(10.2+X2,3.6+Y8)
            CALL SYMBOL(10.3+X2,3.1+Y8,0.2,5HC     ,0.0,5)
```

```
            CALL SYMBOL(10.3+X2+A1,3.1+Y8+B,0.125,5HRS2   ,0.0,5)
C           CALL NUMBER(10.3+X2+A2,3.1+Y8+B,0.12,2.,0.0,-1)
          CALL HSWL(10.2+X2,3.3+Y8,G1)
          CALL VSW(10.2+X2,3.4+Y8,G2)
          CALL PLOT(8.8+X1,4.4+Y,IP)
          CALL PLOT(10.2+X2,4.4+Y,ID)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING DOUBLE OUTPUT OPAMP UP
C  FOR THE MODIFIED BILINEAR TRANFORMATION
        SUBROUTINE DPUMBL(X,Y)
          IP=3
          ID=2
          Y1=Y+.2
          Y2=Y1+1.
          Y3=Y+.6
          Y4=Y3+3.2
C Y9 FOR -VE OUTPUT
          Y9=Y3+2.5
          Y5=Y+.2
          Y6=Y1+.15
          X1=X-.2
          X2=X1+.5
          X3=X1+1.
          X4=X3-.2
          X5=X-.075+.05
          X51=X-.075
          X6=X51+.6
          X7=X+.6
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,ID)
          CALL PLOT(X2,Y2,ID)
          CALL PLOT(X3,Y1,ID)
          CALL PLOT(X4,Y1,ID)
          CALL PLOT(X4,Y,ID)
          CALL PLOT(X4,Y1,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X,Y3,IP)
          CALL PLOT(X,Y9,ID)
          CALL PLOT(X7,Y3,IP)
          CALL PLOT(X7,Y4,ID)
          CALL PLOT(X,Y,IP)
          CALL SYMBOL(X5,Y5,.15,2H+ ,0.0,2)
          CALL SYMBOL(X6,Y5,.15,2H- ,0.0,2)
          CALL SYMBOL(X5,Y6,.15,2H- ,0.0,2)
          CALL SYMBOL(X6,Y6,.15,2H+ ,0.0,2)
```

```
          CALL PLOT(X,Y,IP)
        RETURN
        END
C*********************************************
C  SUBROTINE FOR DRAWING DOUBLE OUTPUT OPAMP DOWN
C  FOR THE MODIFIED BILINEAR TRANFORMATION
        SUBROUTINE DPDMBL(X,Y)
          IP=3
          ID=2
          Y =Y+1.4
          Y1=Y-.2
          Y2=Y1-1.
          Y3=Y-.6
          Y4=Y3-3.2
C Y9 FOR -VE OUTPUT
          Y9=Y3-2.5
          Y5=Y-.4
          Y6=Y1-.35
          X1=X-.2
          X2=X1+.5
          X3=X1+1.
          X4=X3-.2
          X5=X-.075+.05
          X51=X-.075
          X6=X51+.6
          X7=X+.6
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X1,Y1,ID)
          CALL PLOT(X2,Y2,ID)
          CALL PLOT(X3,Y1,ID)
          CALL PLOT(X4,Y1,ID)
          CALL PLOT(X4,Y,ID)
          CALL PLOT(X4,Y1,IP)
          CALL PLOT(X,Y1,ID)
          CALL PLOT(X,Y3,IP)
          CALL PLOT(X,Y9,ID)
          CALL PLOT(X7,Y3,IP)
          CALL PLOT(X7,Y4,ID)
          Y10=Y+.4
          CALL PLOT(X,Y,IP)
          CALL PLOT(X,Y10,ID)
          CALL PLOT(X7,Y,IP)
          CALL PLOT(X7,Y10,ID)
          CALL SYMBOL(X5,Y5,.15,2H+ ,0.0,2)
          CALL SYMBOL(X6,Y5,.15,2H- ,0.0,2)
          CALL SYMBOL(X5,Y6,.15,2H- ,0.0,2)
          CALL SYMBOL(X6,Y6,.15,2H+ ,0.0,2)
```

```
  CALL PLOT(X,Y,IP)
RETURN
END
```

APPENDIX B

HPSC1 EXEC FILE

```
FILEDEF FT05F001 TERMINAL (LRECL 80 RECFM V
FILEDEF FT06F001 TERMINAL (LRECL 80 RECFM F
FILEDEF FT07F001 DISK HPSC1 OUTPUT A (LRECL 80 RECFM F
FILEDEF FT08F001 DISK HPSC1 DATA A
```

APPENDIX C

HPSC2 FORTRAN FILE

```
      REAL FNTL(900),DBHS(900),DBHZ(900),PHAHS(900),PHAHZ(900)
        CALL PLOTS(0,0,1)
            CALL PLOT(4.0,4.0,-3)
            CALL NEWPEN(1)
            CALL FACTOR(1.0)
C**
C** AXL IS THE AXIS LENGTH
C**
            AXL = 10.
      I1=0
      DO 20 I=1,896
      I1=I1+1
      READ(5,*,END= 30) FNTL(I),DBHS(I),DBHZ(I),PHAHS(I),PHAHZ(I)
 20   CONTINUE
 30   CONTINUE
      I1 = I1 -1
C***
C***  PROGRAM SEGMENT FOR ADJUSTING SCALING
C***
            FINT= 10.**(FNTL(1))
            FEND= 10.**(FNTL(I1))
        FNTL(I1+1) = FNTL(1)
        FNTL(I1+2) = (FNTL(I1)-FNTL(1))/AXL
C***
           PMIN1= 1.E30
           PMAX1= 1.E-30
           PMIN2= 1.E30
           PMAX2= 1.E-30
           PMIN3= 1.E30
          DO 50 IP2=1,I1
            IF(DBHS(IP2).LE.PMIN1) THEN
              PMIN1 = DBHS(IP2)
            ELSE IF(DBHS(IP2).GE.PMAX1) THEN
              PMAX1 = DBHS(IP2)
            ENDIF
C***
            IF(DBHZ(IP2).LE.PMIN2) THEN
              PMIN2 = DBHZ(IP2)
            ELSE IF(DBHZ(IP2).GE.PMAX2) THEN
              PMAX2 = DBHZ(IP2)
            ENDIF
```

```
C***
               IF(PHAHZ(IP2).LE.PMIN3) THEN
                 PMIN3 = PHAHZ(IP2)
               ENDIF
 50          CONTINUE
C***
             DBHS(I1+1) =IFIX(PMIN1 - 4.)
             DBHS(I1+2) =IFIX(1.+(PMAX1-DBHS(I1+1))/AXL)
C***
             DBHZ(I1+1) =IFIX(PMIN2- 4.)
             DBHZ(I1+2) =IFIX(1.+(PMAX2-DBHZ(I1+1))/AXL)
C***
C***
               IF(DBHS(I1+1).LT.DBHZ(I1+1)) THEN
                 DBHZ(I1+1) = DBHS(I1+1)
               ELSE
                 DBHS(I1+1) = DBHZ(I1+1)
               ENDIF
C***
               IF(DBHS(I1+2).GT.DBHZ(I1+2)) THEN
                 DBHZ(I1+2) = DBHS(I1+2)
               ELSE
                 DBHS(I1+2) = DBHZ(I1+2)
               ENDIF
C***
               IF(PMIN3.LE.-85.0.AND.PMIN3.GE.-91.0)THEN
                 PHAHS(I1+1) = -100.0
                 PHAHZ(I1+1) = -100.0
                 PHAHS(I1+2) = 200./AXL
                 PHAHZ(I1+2) = 200./AXL
               ELSE
                 PHAHS(I1+1) = -200.0
                 PHAHZ(I1+1) = -200.0
                 PHAHS(I1+2) = 400./AXL
                 PHAHZ(I1+2) = 400./AXL
               ENDIF
C***
C***
C***
          CALL LGAXS(0.0,0.0,21HFREQUENCY (HZ)          ,
     * -21,AXL,0.0,FINT,FNTL(I1+2))
          CALL AXIS(0.0,0.0,21HMAGNITUDE (DB)           ,
     * 21,AXL,90.0,DBHZ(I1+1),DBHZ(I1+2))
             CALL NEWPEN(2)
          CALL FLINE(FNTL,DBHS,-I1,1,0,2)
             CALL NEWPEN(3)
          CALL FLINE(FNTL,DBHZ,-I1,1,0,2)
             CALL NEWPEN(2)
```

```
      CALL SYMBOL(0.5,11.1,0.4,22H__ CONTINUOUS FILTER  ,0.0,22)
           CALL NEWPEN(3)
      CALL SYMBOL(0.5,10.5,0.4,25H__ SWITCHED CAPACITOR F. ,0.0,25)
           CALL NEWPEN(1)
         CALL RECT(-2.5,-2.0,14.0,14.,0.,3)
            CALL PLOT(17.0,0.0,-3)
            CALL NEWPEN(1)
         CALL LGAXS(0.0,0.0,21HFREQUENCY (HZ)        ,
     * -21,AXL,0.0,FINT,FNTL(I1+2))
         CALL AXIS(0.0,0.0,21HPHASE (DEGREES)        ,
     *  21,AXL,90.0,PHAHZ(I1+1),PHAHZ(I1+2))
           CALL NEWPEN(2)
         CALL FLINE(FNTL,PHAHS,-I1,1,0,2)
           CALL NEWPEN(3)
         CALL FLINE(FNTL,PHAHZ,-I1,1,0,2)
           CALL NEWPEN(2)
      CALL SYMBOL(0.5,11.1,0.4,22H__ CONTINUOUS FILTER  ,0.0,22)
           CALL NEWPEN(3)
      CALL SYMBOL(0.5,10.5,0.4,25H__ SWITCHED CAPACITOR F. ,0.0,25)
           CALL NEWPEN(1)
           CALL NEWPEN(1)
        CALL RECT(-2.5,-2.0,14.0,14.,0.,3)
C
C
      CALL PLOT(20.0,20.0,999)
      STOP
      END
```

APPENDIX D

HPSC2 EXEC FILE

```
FILEDEF FT05F001 DISK HPSC1 DATA A
```

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