

A Hybrid Modular Multilevel Converter with Reduced Full-Bridge Submodules

Rui Li, Lie Xu, *Senior Member, IEEE*, Lujie Yu, and Liangzhong Yao, *Senior Member, IEEE*

Abstract—A hybrid modular multilevel converter (MMC) with reduced full-bridge (FB) submodules (SMs) is proposed, where a high voltage rating half-bridge (HB) based MMC is connected in series with a low voltage rating FB-MMC in parallel with a fault breaking circuit on its DC side. Unlike conventional hybrid MMCs with mixed HB and FB SMs, the proposed topology uses the DC capacitor in the fault breaking circuit to block DC faults, while the FB-MMC only commutates the fault current from the FB-MMC to the fault breaking circuit. Thus, the proposed converter only requires around 10%-20% FB SMs, leading to reduced capital cost and losses compared to typical hybrid MMC. The optimal ratio of the FB-MMC and HB-MMC is assessed and comparative studies show superiority of the proposed topology over other alternatives. A case study with 10% FB SMs demonstrates the validity of the proposed hybrid MMC for DC fault blocking and post-fault system restart.

Index Terms—DC fault, DC circuit breaker (DCCB), HVDC transmission, hybrid multilevel converter, modular multilevel converter (MMC).

I. INTRODUCTION

High-voltage DC (HVDC) transmission systems based on modular multilevel converters (MMCs) have developed rapidly due to their significant advantages. However, the behaviors and characteristics of half-bridge (HB) submodule (SM) based MMC (HB-MMC) to DC faults are major issues to be considered in applications. In the event of a DC short circuit, high AC currents flow through the freewheeling diodes of HB-MMC from the AC to the DC side, which requires additional measures and could potentially cause serious damage to the converters and associated semiconductor devices [1-3].

Conventional mechanical DC circuit breakers (DCCBs) have low conduction losses. However, their response is too slow and the semiconductors still endure high current stress during the response time. The solid-state DC circuit breaker can achieve fast interruption but at high capital cost and significant on-state operation losses [4]. The hybrid DC circuit breaker combines the advantages of the mechanical and solid-state DCCBs, where a mechanical path serves as main conduction path with minimal losses during normal operation, and a parallel-connected solid-state breaker is used for DC fault isolation [5, 6]. However, it has relatively large footprint and its capital cost is still very high [7, 8].

R. Li and L. Xu are with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, G1 1XW UK (e-mail: rui.li@strath.ac.uk, lie.xu@strath.ac.uk).

L. Yu is with the School of Electrical and Information Engineering, Tianjin University, Tianjin, 300072, China (e-mail: lujie.yu@outlook.com).

L. Yao is with the School of Electrical Engineering and Automation, Wuhan University, Wuhan, 430072, China (yaoliangzhong@whu.edu.cn).

In addition to the use of DCCB for fault isolation, different fault blocking converter topologies have been proposed. In the full-bridge (FB) SM based MMC (FB-MMC), the FB SM capacitors can be inserted into the circuit in either polarity. This feature allows the FB-MMC to block DC faults and offer greater controllability [9]. However, FB-MMC doubles the required semiconductors compared to HB-MMC, leading to additional cost and losses.

In addition to the FB SM, various SM topologies have been proposed, e.g. clamp double (CD) SM [10], cross connected (CC) SM [11, 12], unipolar FB SM [13], unipolar CC SMs [14], etc. These SMs use additional semiconductor switches to change the current path during DC faults and block the fault currents fed from the AC side, while operate in a similar way with HB SM during normal operation. However, the introduction of additional semiconductors leads to higher losses and cost.

The alternate-arm multilevel converter (AAC) presented in [15] can block DC faults with reduced semiconductor losses compared to the FB-MMC. However, the direct switches in the AAC arm require series connection of large numbers of IGBTs [16]. Based on HB-MMC, the hybrid cascaded MMC (HC-MMC) is proposed in [17], where cascaded FB chains are connected on the AC side of HB-MMC to provide reverse blocking voltage after the converter is blocked following the fault. This topology has lower losses and cost than FB-MMCs but the cascaded FB chains need to be coordinately controlled with the HB-MMC part.

Reference [18] proposes a hybrid MMC (H-MMC), which mixes FB and HB SMs in each arm to obtain DC fault blocking capability with lower losses than the FB-MMC. Also, it can generate negative voltage, which enables greater controllability of the converter [18, 19]. The ratio between the FB and HB number is typically fix at one to effectively block DC faults. The ratio greater than one is also discussed in [18] to transfer more power than the conventional MMC by utilizing the negative output voltage capability of the FB SMs. However, with more HB SMs replaced by FB SMs, the power losses are increased.

Another hybrid MMC is proposed in [20], where only one HB SM is replaced by a FB SM in the lower arm. During DC faults, all the HB SMs in the upper arm are commanded to output zero voltage to create an artificial AC short circuit so as to bypass the fault currents fed by the AC grid from DC side. Meanwhile, all the SMs in the lower arm are turned off thus the FB SM provides blocking voltage to rapidly reduce the DC current to zero. As a result, the DC switches can be opened at zero current to isolate the DC fault and then all the HB SMs in

the upper arm can be deactivated. However, before the opening of the DC switches, large fault currents flow through the IGBTs in the upper arm, leading to severe overcurrent.

In order to overcome the above problems, a hybrid MMC with reduced FB SMs (RFB-MMC) is proposed in this paper and its operation including DC fault blocking and restart capabilities is researched. The proposed converter is introduced in section II including the converter topology and typical characteristics. In section III, the operating principle considering DC fault blocking and restart procedure is detailed. Section IV presents the design principles of the proposed topology, considering cost, loss, and control strategy. The performance of the proposed RFB-MMC is assessed in section V using simulations and section VI concludes the paper.

II. PROPOSED HYBRID MMCs WITH REDUCED FB SMs

Fig. 1 shows a generic version of the proposed hybrid MMC with reduced FB SMs. Its main power stage consists of a series connection of HB-MMC and FB-MMC on their DC sides. A fault breaking circuit, composed of an ultra-fast disconnecter (UFD), a residual DC current breaker (RB), and a DC capacitor C_F , is connected in parallel with the FB-MMC on the DC side to provide DC fault blocking and DC circuit breaking capability.

For the conventional hybrid MMC, the negative voltage provided by the FB SMs needs to be greater than the peak AC line-to-line voltage to block DC faults. Thus, typically it requires 50% FB SMs, leading to higher cost and power losses than HB-MMCs [18, 19]. In contrast, in the proposed topology, the FB-MMC only commutates the fault current from the FB-MMC to the fault breaking circuit and does not need to match the AC side voltage to block DC faults. Thus, the ratio k between the FB SM number N_{FB} and the total SM number N in each arm of the FB-MMC can be much less than the typical value of 50%, i.e.:

$$k = \frac{N_{FB}}{N} = \frac{N_{FB}}{N_{FB} + N_{HB}} < 50\% \quad (1)$$

where N_{HB} is the HB SM number per arm for the HB-MMC. As will be discussed in section IV, k can be reduced from the typical value of 50% in H-MMC to 10%, leading to reduced losses and capital cost.

For modular design, the FB and HB SM capacitors have the same voltage V_C :

$$V_C = \frac{V_{dcFB}}{N_{FB}} = \frac{V_{dcHB}}{N_{HB}} = \frac{V_{dc}}{N} = \frac{kV_{dc}}{N_{FB}} \quad (2)$$

where V_{dcFB} , V_{dcHB} and V_{dc} are the DC voltages of the FB-MMC, HB-MMC and RFB-MMC, respectively. Considering unity modulation index, the peak AC line-to-line voltages V_{acFB} and V_{acHB} of the FB-MMC and HB-MMC are assumed as (3) and (4), respectively:

$$V_{acFB} = \frac{\sqrt{3}}{2} k V_{dc} \quad (3)$$

$$V_{acHB} = \frac{\sqrt{3}}{2} (1-k) V_{dc} \quad (4)$$

According to Kirchhoff's current law, the DC currents are governed by (5) from Fig. 1:

$$I_{dcHB} = I_{dcFB} + I_{CF} = I_{RB} \quad (5)$$

where I_{dcHB} and I_{dcFB} are the DC currents of HB-MMC and FB-MMC, respectively, and I_{CF} and I_{RB} are the currents flowing through capacitor C_F and residual breaker RB, respectively.

During normal operation, i.e. non-DC fault conditions, the proposed topology operates in the same way as the conventional HB-MMCs including the same AC fault ride-through capability [21].

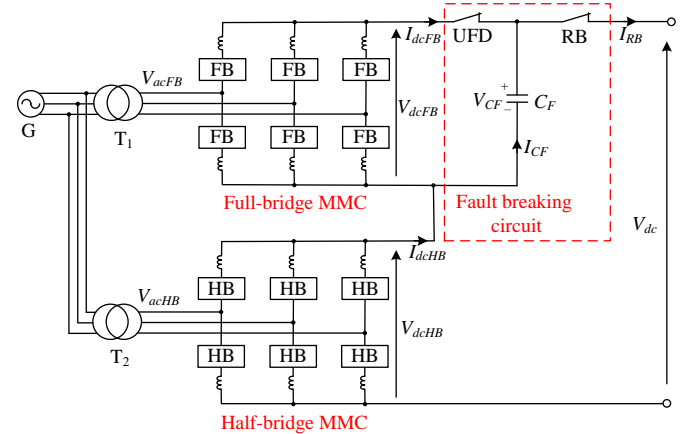


Fig. 1. Proposed hybrid MMC with reduced FB SMs.

III. OPERATING PRINCIPLE OF THE PROPOSED RFB-MMC

The operating principles of the proposed scheme, including DC fault blocking and system restart, are presented in this section.

A. DC Fault Blocking

The principle idea of the proposed topology is to use DC capacitor C_F rather than FB SMs to block DC faults such that k ratio can be significantly reduced. The operation of the circuit can be explained as follows.

- During normal operation (Stage I), UFD and RB are closed and the capacitor voltage V_{CF} equals to the nominal FB-MMC DC voltage while the capacitor current I_{CF} is around zero, as shown in Fig. 2 (a). Both the FB-MMC and HB-MMC transmit power during normal operation.
- In the event of DC faults, the HB SM capacitors and the capacitor C_F are initially discharged as illustrated in Stage II shown in Fig. 2 (b). The currents I_{dcHB} and I_{CF} thus increase, which can be used to detect the fault.
- Both the HB-MMC and FB-MMC are then blocked after fault detection and the FB-MMC provides negative blocking voltage to its AC side, while also suppresses its DC current I_{dcFB} to zero. Thus, all the DC fault current from the HB-MMC I_{dcHB} is commutated to the capacitor C_F . As the current flowing through the FB-MMC is zero as expressed by (6), the UFD can be opened under zero current (Stage III, Fig. 2 (c)).

$$I_{CF} = I_{dcHB}, \quad I_{dcFB} = 0 \quad (6)$$

- The DC fault current charges the capacitor C_F , and once the capacitor voltage V_{CF} is greater than the peak AC line-to-line voltage V_{acHB} , as depicted by (7), the uncontrolled fault current from the HB-MMC AC side will be suppressed and

the DC fault blocked (Stage IV, Fig. 2 (d)).

$$|V_{CF}(t)| = \left| V_{dcFB} - \frac{1}{C_F} \int_{t_0}^t I_{CF} dt \right| \geq V_{acHB} \quad (7)$$

where t_0 is the instant when the DC fault occurs.

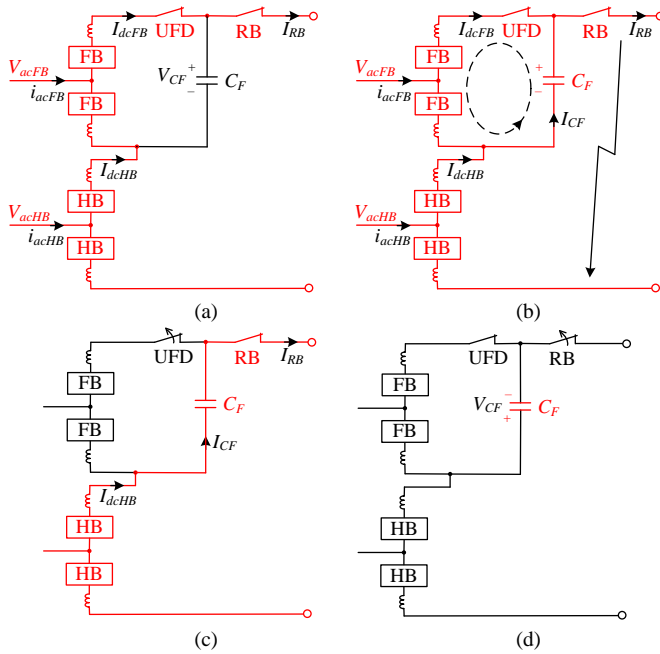


Fig. 2. Single-phase illustration of fault current commutation of the RFB-MMC: (a) Stage I: normal operation, (b) Stage II: fault current commutation, (c) Stage III: capacitor C_F reverse charging, and (d) Stage IV: fault blocking.

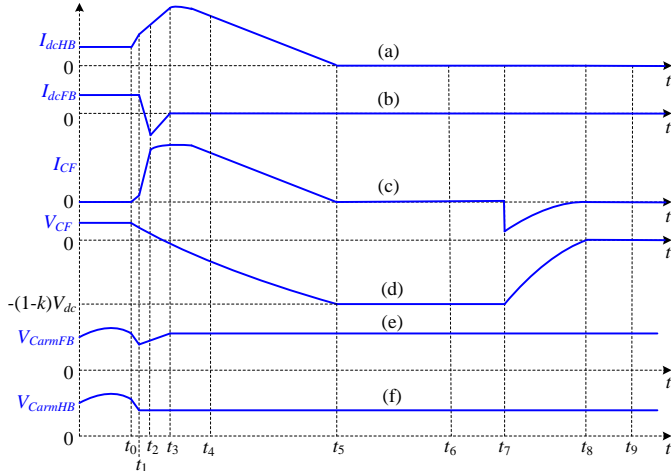


Fig. 3. Illustration of the typical waveforms of the RFB-MMC during faults: (a) HB-MMC DC current, (b) FB-MMC DC current, (c) capacitor C_F current, (d) capacitor C_F voltage, (e) sum of SM capacitor voltages of FB-MMC, and (f) sum of SM capacitor voltages of HB-MMC.

The typical waveforms of the proposed converter during DC faults are illustrated in Fig. 3, which are described as follows.

- When a DC fault occurs at $t=t_0$, capacitor C_F discharges and its current I_{CF} increases. Meanwhile, SM capacitors of HB-MMC are also discharged, leading to the increase of the DC current I_{dcHB} .
- Once the DC fault is detected at $t=t_1$ by either over current detection or other suitable methods [22], both the FB and HB converters of the RFB-MMC are blocked and the SM

capacitors stop discharging.

- After the converters are blocked at $t=t_1$, the fault currents flow through the antiparallel diodes in the arms and charge the SM capacitors of the FB-MMC, as shown in Fig. 4 (a), which considers one SM per arm for ease of illustration. Fig. 4 (a) can be equivalent as Fig. 4 (b) and as seen, depending on the arm current directions, the upper and lower arms of the FB-MMC provide positive and negative voltages. Thus, the sum of the upper and lower arm voltages of the FB-MMC is zero ($V_{dcFB}-V_{dcFB}$) during $t_1\sim t_2$. Due to the capacitor voltage V_{CF} , the DC current I_{dcFB} decreases to zero and reverses until $t=t_2$ when one of the upper and lower arm currents in a phase becomes zero. At this instant, the blocking voltage provided by the FB-MMC is increased from zero to $2V_{dcFB}$ (i.e. $V_{dcFB}+V_{dcFB}$), as seen from Fig. 4 (c). The DC current I_{dcFB} then starts to decrease and is suppressed to zero at $t=t_3$. The fault current is thus commutated to the capacitor C_F and the FB-MMC is bypassed, as illustrated in Fig. 2 (c). Therefore, UFD is opened at zero current at $t=t_4$ after certain delays. Typical UFD opening time is 2 ms, and thus, it takes around 2 ms from fault detection at $t=t_1$ to the opening of the UFD at $t=t_4$.

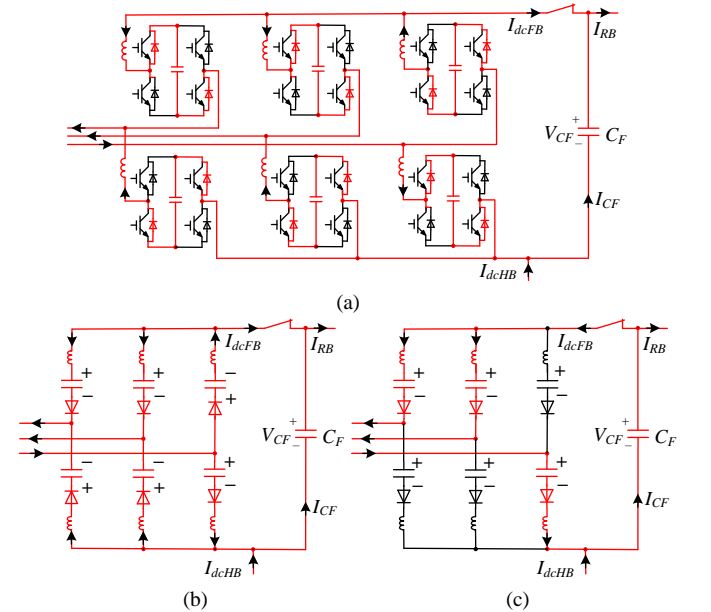


Fig. 4. Current path illustration during FB-MMC DC current reversal: (a) detailed current path during $t_1\sim t_2$, (b) equivalent current path during $t_1\sim t_2$ and (c) equivalent current path during $t_2\sim t_3$.

- Following the blocking of the RFB-MMC at $t=t_1$, the sum of SM capacitor voltages of HB-MMC V_{CarmHB} remains unchanged seen in Fig. 3 (f), as the fault currents only flow through the antiparallel diodes of the HB SMs and do not charge the HB SM capacitors. In contrast, the FB SMs provide negative voltages to suppress the fault currents, which charge the FB SM capacitors, leading to slight increase of the FB capacitor voltage V_{CarmFB} from $t=t_1$ to $t=t_3$ as illustrated in Fig. 3 (e). After the suppression of the FB-MMC DC current I_{dcFB} to zero at $t=t_3$, V_{CarmFB} remains unchanged.
- From fault initiation, fault currents continue being fed to the DC side by the AC grid voltage V_{acHB} through the

antiparallel diodes of the HB-MMC. The fault current I_{dcHB} flows through C_F and its voltage V_{CF} decreases to zero and then reverses. When V_{CF} increases to around $-(1-k)V_{dc}$, the fault current I_{dcHB} reduces to zero at $t=t_5$ and the DC fault is thus blocked, as illustrated in Fig. 2 (d), and Fig. 3 (a) and (d). If the residual breaker RB is connected with the faulty DC line, it can be opened at $t=t_6$ to physically isolate the RFB-MMC from the faulty DC network. On the other hand, if the DC fault is in other part of the DC network in a multi-terminal DC system, i.e. the DC fault is not at the DC line connected to the RFB-MMC, the RB can remain closed.

B. System Restart

After fault isolation, the RFB-MMCs connected to the healthy part of the DC network need to recover and restart power transmission. This requires C_F to be discharged first. In the proposed scheme, a fast discharging resistor R_{dis} is switched in using a mechanical switch S_{dis} with the closing time of 20 ms as shown in Fig. 5. The sequence during restart is detailed as follows.

- After fault isolation (at other part of the DC network so RB remains closed), the mechanical switch S_{dis} is closed at $t=t_7$ and the capacitor C_F is discharged as seen in Fig. 3. When the capacitor voltage V_{CF} drops below the peak of the HB-MMC AC voltage V_{acHB} at $t=t_8$, AC currents start to flow through the freewheeling diodes and charge the healthy DC cables. Once the DC cables are charged, the charging currents reduce to zero.
- After the capacitor C_F is safely discharged, the discharging switch S_{dis} is opened and the UFD closes at $t=t_9$. The FB-MMC is thus connected in the circuit and normal operation can be resumed.

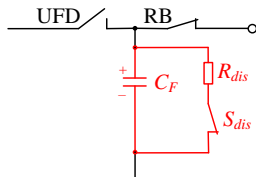


Fig. 5. Discharging circuit for the fault blocking capacitor C_F of the RFB-MMC.

The fast discharging resistor R_{dis} only needs to dissipate the energy stored in the capacitor C_F during system restart and does not introduce power losses during normal operation, as it is disconnected from the circuit by the mechanical switch S_{dis} .

IV. DESIGN OF THE PROPOSED RFB-MMC

The design principles of the proposed RFB-MMC are presented in this section, considering cost, losses, and control structures.

A. Cost Consideration

1) Capacitor C_F requirements

To ensure that UFD is safely opened under zero current at $t=t_4$ in Stage III, the reversed DC capacitor voltage V_{CF} needs to be less than the negative voltage $V_{blockFB}$ provided by the FB-MMC, as expressed by (8). Otherwise, V_{CF} will force I_{dcFB} to increase again.

$$|V_{CF}(t_4)| = \left| V_{dcFB} - \frac{1}{C_F} \int_{t_0}^{t_4} I_{CF} dt \right| < V_{blockFB}. \quad (8)$$

$$V_{blockFB} = 2V_C N_{FB} = 2V_{dcFB} = 2kV_{dc}$$

Typical UFD opening time is around 2 ms. Thus, 2 ms after fault detection and the initiation of the opening of the UFD, the reversed capacitor voltage V_{CF} needs to be less than the blocking voltage $V_{blockFB}$. Considering the integration of the fault current within the first 2ms is largely constant, from (8), the required capacitance C_F is inversely proportional to the blocking voltage of the FB-MMC. In the most severe cases tested while considering possible different power flow directions, operation point, etc., the value of the required capacitance C_F is $0.5C_{SM}/N$ in the specific case with $k=20\%$, where C_{SM} is the SM capacitance. With the variation of k , the required C_F can be considered as inversely proportional to the ratio k as:

$$C_F = \frac{0.2}{k} \frac{C_{SM}}{2N} = \frac{C_{SM}}{10kN}. \quad (9)$$

The total energy stored in the FB and HB SM capacitors of the RFB-MMC is

$$E_{SM} = 6kN \frac{1}{2} C_{SM} \left(\frac{V_{dc}}{N} \right)^2 + 6(1-k)N \frac{1}{2} C_{SM} \left(\frac{V_{dc}}{N} \right)^2. \quad (10)$$

$$= \frac{3C_{SM}}{N} V_{dc}^2$$

From (9) and (10), and assuming the blocking voltage provided by the capacitor C_F during DC faults is $(1-k)V_{dc}$, the energy stored in the capacitor C_F is expressed as

$$E_{CF} = \frac{1}{2} C_F [(1-k)V_{dc}]^2$$

$$= \frac{C_{SM}}{20kN} (1-k)^2 V_{dc}^2 = (1-k)^2 \frac{E_{SM}}{60k}. \quad (11)$$

The FB and HB SMs of the proposed RFB-MMC require the same value of capacitor as that used in the conventional HB-MMC and can be in the range of is 30~40 kJ/MVA [23]. From (11), the total required capacitor volume of the RFB-MMC is thus around $1 + \frac{(1-k)^2}{60k}$ times that of HB-MMC.

2) Cost evaluation

The required IGBT number per arm of the proposed RFB-MMC is the sum of those in the FB-MMC and HB-MMC:

$$4Nk + 2N(1-k) = 2N(1+k). \quad (12)$$

Assuming the SM capacitors and semiconductor devices equally share the total cost CO_{HB-MMC} of the conventional HB-MMC [24], the semiconductor cost CO_{semi} of the proposed RFB-MMC is:

$$CO_{semi} = \frac{2N(1+k)}{2N} \times \frac{CO_{HB-MMC}}{2} = \frac{1+k}{2} CO_{HB-MMC}. \quad (13)$$

The capacitor cost of the FB and HB SMs in the RFB-MMC CO_{CSM} is the same as that of the conventional HB-MMC:

$$CO_{CSM} = 0.5CO_{HB-MMC}. \quad (14)$$

From (11), the cost of the fault blocking capacitor C_F is

$$CO_{CF} = \frac{E_{CF}}{E_{SM}} \frac{CO_{HB-MMC}}{2} = \frac{(1-k)^2}{120k} CO_{HB-MMC}. \quad (15)$$

Similar to the residual breaker of hybrid breakers, the residual breaker RB physically isolates the faulty cables after faults are blocked by the RFB-MMC. Thus, its opening speed is not critical and normal mechanical switches can be used. The cost CO_{else} of the RB, UFD and the discharging circuit is estimated as $0.05CO_{HB-MMC}$ [20]. The total cost of the RFB-MMC is thus calculated as

$$CO_{RFB} = CO_{semi} + CO_{CSM} + CO_{CF} + CO_{SF} + CO_{else} \\ = \frac{61k^2 + 124k + 1}{120k} CO_{HB-MMC} \quad (16)$$

The total cost of the FB-MMC and the conventional hybrid MMC is estimated as (17) and (18), respectively:

$$CO_{FB-MMC} = (1+1) \frac{CO_{HB-MMC}}{2} + \frac{CO_{HB-MMC}}{2} = 1.5CO_{HB-MMC} \quad (17)$$

$$CO_{H-MMC} = (1+0.5) \frac{CO_{HB-MMC}}{2} + \frac{CO_{HB-MMC}}{2} = 1.25CO_{HB-MMC} \quad (18)$$

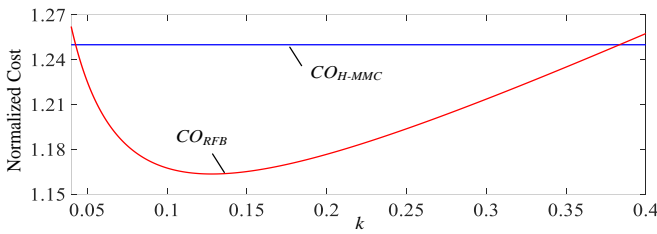


Fig. 6. Comparison of normalized cost between the conventional hybrid MMC and the proposed RFB-MMC with the variation of k .

From (16) and (18), the normalized capital costs of the conventional hybrid MMC and the proposed RFB-MMC are plotted in Fig. 6, where the HB-MMC cost CO_{HB-MMC} is defined as the base value. When k is in the range of (0.04~0.38), the proposed topology is more cost-effective than the conventional H-MMC, and the minimum cost CO_{RFBmin} of the RFB-MMC is around $1.16CO_{HB-MMC}$ from (16), a reduction of 7.2% compared to the H-MMC cost of $1.25CO_{HB-MMC}$.

TABLE I

Comparison of the proposed RFB-MMC ($k=0.1$) with other alternatives.

	HB-MMC	FB-MMC	H-MMC	RFB-MMC
Capacitor stored energy (kJ/MVA)	30~40	30~40	30~40	35~47
No. of semiconductors per arm	$2N$	$4N$	$3N$	$2.2N$
No. of semiconductors in current path per arm	N	$2N$	$1.5N$	$1.1N$
Cost (pu)	1	1.5	1.25	1.16
Losses	1%	1.7%	1.35%	1.07%
DC fault blocking	No	Yes	Yes	Yes

According to (12), the required IGBT number per arm of the proposed RFB-MMC with $k=0.1$ is $2.2N$, a reduction of 26.7% compared to that of the conventional hybrid MMC ($3N$). From (11), when $k=0.1$, the capacitance requirement of the RFB-MMC is in the range of 35~47 kJ/MVA. The comparison of the proposed RFB-MMC with other alternative MMC configurations is summarized in Table I.

B. Loss Consideration

The proposed fault breaking circuit is inactive during normal operation. Currents only flow through the mechanical devices UFD and RB, and thus the loss of the fault breaking circuit is negligible.

The conduction loss of the RFB-MMC is proportional to the semiconductor number in the current path per arm, which is expressed as (19) for the proposed RFB-MMC:

$$2N_{FB} + N_{HB} = 2kN + (1-k)N = (1+k)N \quad (19)$$

Thus, with $k=0.1$, the per arm semiconductor number in the current path of the proposed RFB-MMC is $1.1N$, lower than that of the conventional hybrid MMC ($1.5N$), as listed in Table I. This significantly reduces conduction losses. The switching loss of the RFB-MMC is similar to that of HB-MMC. Assuming the conduction and switching losses of the conventional HB-MMC are $0.7LO_{HB-MMC}$ and $0.3LO_{HB-MMC}$, respectively [25], the total loss of the proposed RFB-MMC is

$$\frac{2N + 2kN}{2N} \times 0.7LO_{HB-MMC} + 0.3LO_{HB-MMC} \\ = (1 + 0.7k) LO_{HB-MMC} \quad (20)$$

The losses of the conventional HB-MMC and hybrid MMC are typically 1% and 1.35%, respectively [18, 25]. From (20), the loss of the proposed RFB-MMC with $k=0.1$ is calculated as 1.07%, a reduction of 20.7% compared to the conventional hybrid MMC as listed in Table I.

The capitalized cost associated with losses is typically 3000€/kW [25] and thus the proposed RFB-MMC further reduces the cost by 10 M€ per converter if the conventional hybrid MMC rated at 1200 MW is replaced by the proposed RFB-MMC.

The proposed RFB-MMC shows superiorities over other alternatives in terms of efficiency and required semiconductor number, which are among the major concerns when constructing HVDC projects. The construction, installation and space requirements of various topologies will incur different costs, which need to be taken into consideration in real applications.

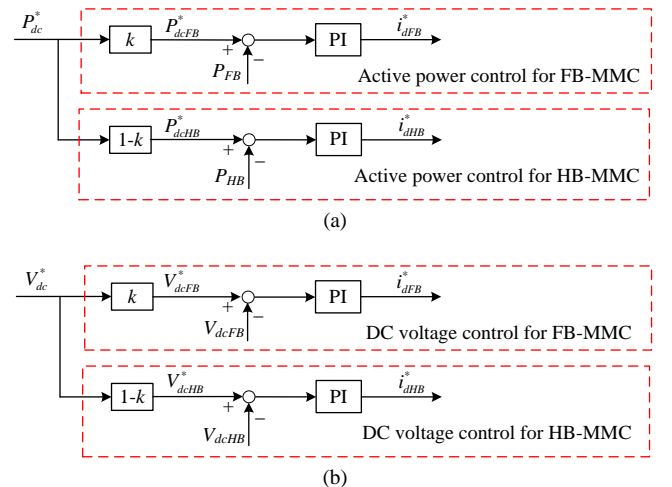


Fig. 7. Control structure of the proposed RFB-MMC: (a) active power control and (b) DC voltage control.

C. Control Strategy

For the proposed topology, the FB-MMC and HB-MMC are connected in series and share the same DC current. To ensure DC voltage sharing according to the ratio k defined by (1), the active power references of the FB-MMC and HB-MMC need to be set as $P_{dcFB}^* = kP_{dc}^*$ and $P_{dcHB}^* = (1-k)P_{dc}^*$, respectively, as

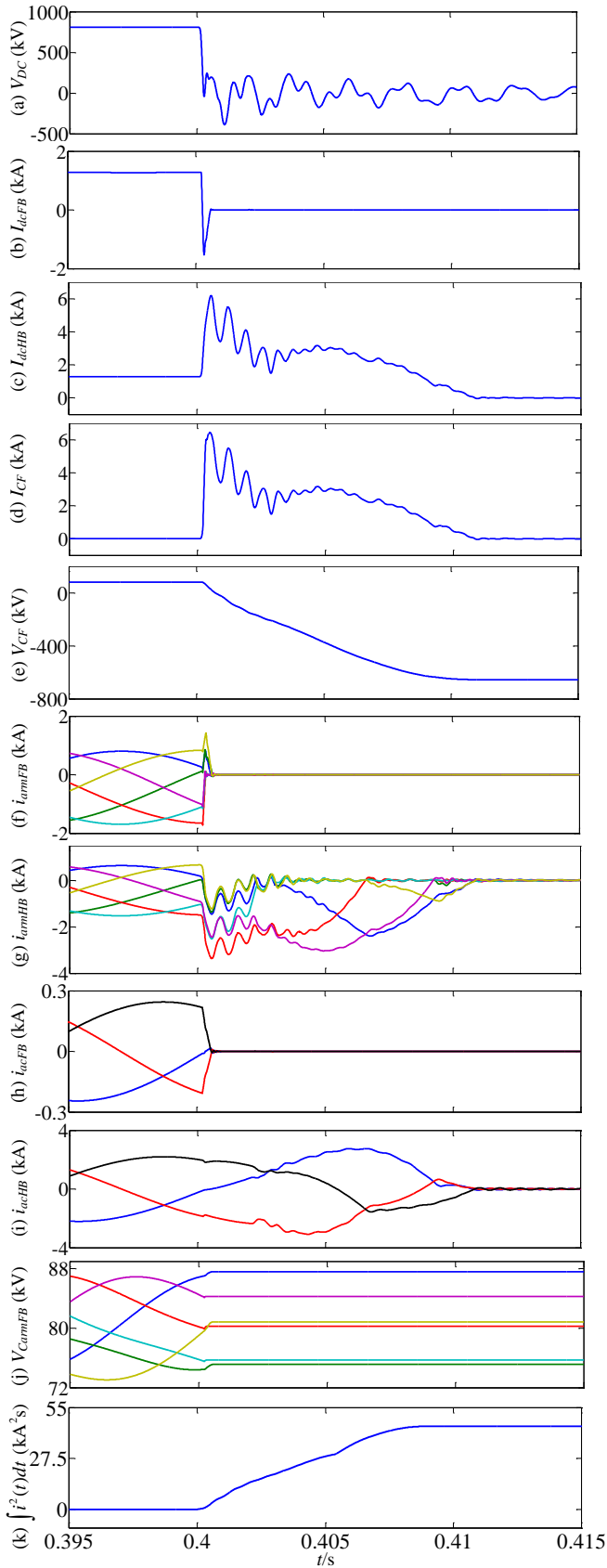


Fig. 9. DC fault blocking waveforms of RFB-MMC₁: (a) RFB-MMC DC voltage, (b) FB-MMC DC current, (c) HB-MMC DC current, (d) capacitor C_F current, (e) capacitor C_F voltage, (f) FB-MMC arm currents, (g) HB-MMC arm currents, (h) FB-MMC grid-side AC currents, (i) HB-MMC grid-side AC currents, (j) sum of SM capacitor voltages of FB-MMC, and (k) maximum diode $\int i^2(t)dt$ of HB-MMC.

voltage of C_F (i.e. V_{CF}) decreases to zero and then reverses, as shown in Fig. 9 (e). However, V_{CF} is still lower than the FB-MMC blocking voltage of 160 kV before $t=0.4022$ s and thus the DC current of the FB-MMC remains at zero, and the UFC is opened under zero current at $t=0.4022$ s. The DC fault current continues charging the capacitor C_F and, with the increase of the capacitor voltage V_{CF} in opposite to the fault current direction, gradually decreases to zero around 11 ms after fault detection when V_{CF} reaches around -720 kV, Fig. 9 (c), (d) and (e). The DC fault blocking time of the proposed topology is thus around 11 ms. Similar behaviors can also be observed from the arm and AC currents of the HB-MMC, as seen from Fig. 9 (g) and (i). The peak fault current flowing through the arms of the HB-MMC reaches 3.4 kA (2.3 pu). However, the fault currents only flow through the antiparallel diodes and drop to zero in around 11 ms. The maximum diode $\int i^2(t)dt$ is 45 kA²s as illustrated in Fig. 9 (k), which is in the safe operation range of the diodes studied [28].

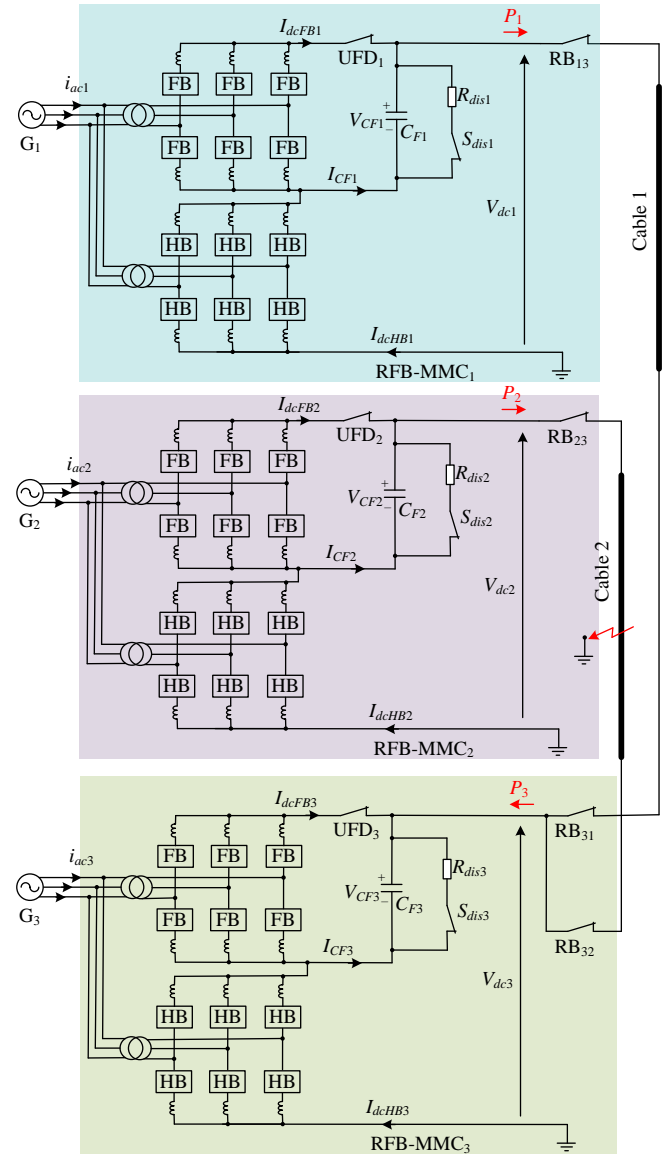


Fig. 10. Three-terminal DC network based on the proposed RFB-MMC.

As shown in Fig. 9 (d), the peak fault current flowing

through the blocking capacitor C_F is around 6.5 kA and is much less than those of the DCCB capacitors proposed by Mitsubishi and SCiBreak AB (16 kA and 10 kA, respectively) [29, 30].

As the FB SMs of the RFB-MMC only block the fault currents fed from the FB-MMC AC side and commutate the DC current to the fault breaking capacitor C_F at the initial stage of the fault, the capacitor voltages of the FB SMs do not have over charging issue, as demonstrated in Fig. 9 (j).

B. DC Fault Ride-through

The proposed RFB-MMC is also tested using a three-terminal DC network as illustrated in Fig. 10. Stations RFB-MMC₁ and RFB-MMC₂ operate on power control mode and are connected to the bus-bar of RFB-MMC₃ through residual breakers RB₃₁ and RB₃₂, respectively. RFB-MMC₁ and RFB-MMC₂ have the same parameters as the aforementioned point-to-point HVDC link, as listed in Table II. RFB-MMC₃ controls the DC voltage of the DC network and also has the same parameters as those in Table II except its power rating, SM capacitance C_{SM} and blocking capacitance C_F are doubled. A solid pole-to-pole DC fault occurs at the middle of the 75 km Cable 2 at $t=0.4$ s.

After the occurrence of the DC fault, the DC voltage of the network drops to around zero and the three respective stations are blocked 0.3 ms, 0.5 ms, and 1 ms after fault initiation, following the same procedure as detailed in section V Subsection A. The power transmission is thus interrupted, as shown in Fig. 11 (b) and (c). As observed in Fig. 11 (d) and (e), fault currents flow into the RFB-MMCs at the initial stage of fault occurrence but are quickly suppressed at zero. After fault isolation by opening RB₂₃ and RB₃₂ (fault location is not in the scope of this paper so it considers the fault is located by other methods) at $t=0.421$ s, RFB-MMC₁ and RFB-MMC₃ can be restarted to restore power transmission between them, as detailed as follows.

At $t=0.435$ s, the mechanical switch of the discharging circuit S_{dis} is activated to quickly discharge the capacitor C_F , as shown in Fig. 11 (i). With the decrease of its voltage V_{CF} , currents flow through the HB-MMC and capacitor C_F from AC grid to charge the DC cables, which leads to the increase of the DC voltage and enables soft-restart of the proposed converters, as displayed in Fig. 11 (a), (e), (f), and (h). As shown in Fig. 11 (i), the capacitor voltage V_{CF} decreases to around zero at $t=0.45$ s, and switch S_{dis} is then opened. UFD is closed at $t=0.452$ s and then the system is now ready to restart.

Station RFB-MMC₃ is firstly enabled $t=0.455$ s to restore the DC voltage as shown in Fig. 11 (a) and RFB-MMC₁ is activated at $t=0.565$ s and gradually ramps up the active power to the rated value in 50 ms, Fig. 11 (b) and (d). The power transmission between the two healthy stations is thus resumed, Fig. 11 (c) and (e).

With the FB SMs reduced from 50% to 10%, the proposed RFB-MMCs are still capable of blocking DC faults, avoiding overcurrent of HVDC stations. In a multi-terminal configuration, the healthy parts of the DC network can quickly resume normal operation after fault isolation.

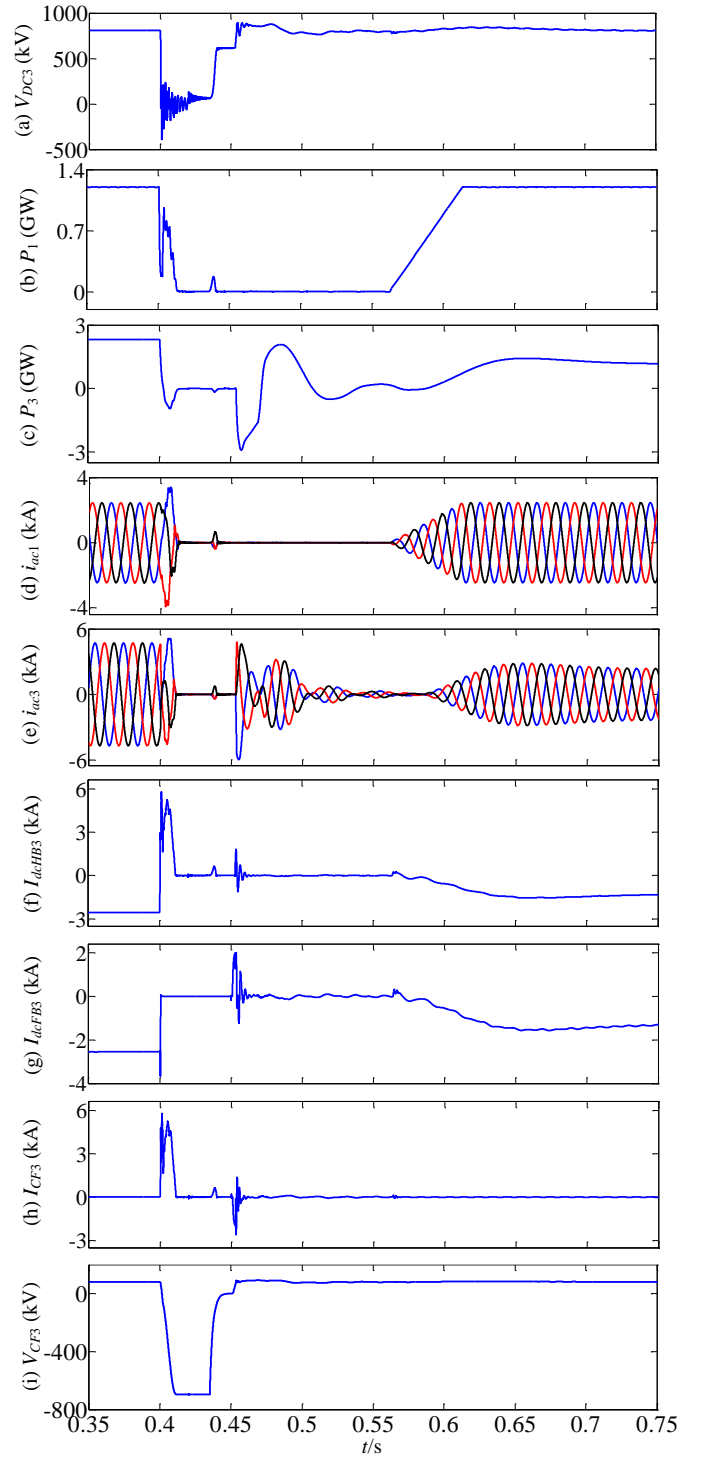


Fig. 11. System restart waveforms during DC faults: (a) RFB-MMC₃ DC voltage, (b) RFB-MMC₁ active power, (c) RFB-MMC₃ active power, (d) RFB-MMC₁ grid-side AC currents, (e) RFB-MMC₃ grid-side AC currents, (f) HB-MMC₃ DC current, (g) FB-MMC₃ DC current, (h) capacitor C_{F3} current, and (i) capacitor C_{F3} voltage.

VI. CONCLUSION

This paper proposes a novel hybrid MMC, where a high voltage rating HB-MMC is connected in series with a circuit formed by parallel-connected low voltage rating FB-MMC and a fault breaking circuit on DC side. During normal operation, both the FB-MMC and HB-MMC transmit power with the fault

breaking circuit bypassed. During DC faults, the DC capacitor of the fault breaking circuit is charged by the fault currents and provides negative voltage to block faults. The proposed topology significantly reduces the required FB SM number from 50% for a typical hybrid MMC to 10%, leading lower capital cost and power loss compared to hybrid MMC with 50% of FB SMs. The DC fault blocking and restart capability, high efficiency, and low capital cost of the proposed RFB-MMC make it attractive for application in HVDC systems.

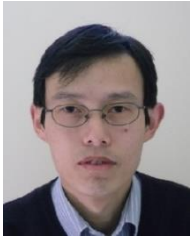
VII. REFERENCES

- [1] M. B. Ghat and A. Shukla, "A New H-Bridge Hybrid Modular Converter (HBHMC) for HVDC Application: Operating Modes, Control, and Voltage Balancing," *IEEE Transactions on Power Electronics*, vol. 33, pp. 6537-6554, 2018.
- [2] T. H. Nguyen, K. H. A. Hosani, and M. E. Moursi, "Alternating Submodule Configuration Based MMCs with Carrier-Phase-Shift Modulation in HVDC Systems for DC-Fault Ride-Through Capability," *IEEE Transactions on Industrial Informatics*, pp. 1-1, 2019.
- [3] X. Chen, L. Wang, H. Sun, and Y. Chen, "Fuzzy Logic Based Adaptive Droop Control in Multiterminal HVDC for Wind Power Integration," *IEEE Transactions on Energy Conversion*, vol. 32, pp. 1200-1208, 2017.
- [4] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of Solid-State Circuit Breaker-Based Protection for DC Shipboard Power Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, pp. 260-268, 2017.
- [5] N. Ahmed, L. Ångquist, S. Mahmood, A. Antonopoulos, L. Harnefors, S. Norrga, *et al.*, "Efficient Modeling of an MMC-Based Multiterminal DC System Employing Hybrid HVDC Breakers," *IEEE Transactions on Power Delivery*, vol. 30, pp. 1792-1801, 2015.
- [6] O. Cwikowski, J. Sau-Bassols, B. Chang, E. Prieto-Araujo, M. Barnes, O. Gomis-Bellmunt, *et al.*, "Integrated HVDC Circuit Breakers With Current Flow Control Capability," *IEEE Transactions on Power Delivery*, vol. 33, pp. 371-380, 2018.
- [7] E. Kontos, T. Schultz, L. Mackay, L. M. Ramirez-Elizondo, C. M. Franck, and P. Bauer, "Multiline Breaker for HVdc Applications," *IEEE Transactions on Power Delivery*, vol. 33, pp. 1469-1478, 2018.
- [8] A. Mokherdorran, O. Gomis-Bellmunt, N. Silva, and A. Carvalho, "Current Flow Controlling Hybrid DC Circuit Breaker," *IEEE Transactions on Power Electronics*, vol. 33, pp. 1323-1334, 2018.
- [9] J. Hu, K. Xu, L. Lin, and R. Zeng, "Analysis and Enhanced Control of Hybrid-MMC-Based HVDC Systems During Asymmetrical DC Voltage Faults," *IEEE Transactions on Power Delivery*, vol. 32, pp. 1394-1403, 2017.
- [10] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, "Assembly HVDC Breaker for HVDC Grids With Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 32, pp. 931-941, 2017.
- [11] S. Debnath, Q. Jiangchao, B. Bahrani, M. Saedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 37-53, 2015.
- [12] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 18-36, 2015.
- [13] R. Li, J. E. Fletcher, L. Xu, D. Holliday, and B. W. Williams, "A Hybrid Modular Multilevel Converter With Novel Three-Level Cells for DC Fault Blocking Capability," *Power Delivery, IEEE Transactions on*, vol. 30, pp. 2017-2026, 2015.
- [14] J. Qin, M. Saedifard, A. Rockhill, and R. Zhou, "Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits," *IEEE Transactions on Power Delivery*, vol. 30, pp. 385-394, 2015.
- [15] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, *et al.*, "The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," *Power Delivery, IEEE Transactions on*, vol. 29, pp. 310-317, 2014.
- [16] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, *et al.*, "The Extended Overlap Alternate Arm Converter: A Voltage-Source Converter With DC Fault Ride-Through Capability and a Compact Design," *IEEE Transactions on Power Electronics*, vol. 33, pp. 3898-3910, 2018.
- [17] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, "Hybrid Cascaded Modular Multilevel Converter With DC Fault Ride-Through Capability for the HVDC Transmission System," *Power Delivery, IEEE Transactions on*, vol. 30, pp. 1853-1862, 2015.
- [18] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and Operation of a Hybrid Modular Multilevel Converter," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 1137-1146, 2015.
- [19] J. Lee, J. Jung, and S. S. AE, "Balancing of Submodule Capacitor Voltage of Hybrid Modular Multilevel Converter (MMC) under DC Bus Voltage Variation of HVDC System," *IEEE Transactions on Power Electronics*, pp. 1-1, 2019.
- [20] X. Huang, L. Qi, and J. Pan, "A New Protection Scheme for MMC-based MVDC Distribution Systems with Complete Converter Fault Current Handling Capability," *IEEE Transactions on Industry Applications*, pp. 1-1, 2019.
- [21] L. Shi, G. P. Adam, R. Li, and L. Xu, "Control of Offshore MMC during Asymmetric Offshore AC Faults for Wind Power Transmission," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1-1, 2019.
- [22] R. Li, L. Xu, and L. Yao, "DC Fault Detection and Location in Meshed Multiterminal HVDC Systems Based on DC Reactor Voltage Change Rate," *IEEE Transactions on Power Delivery*, vol. 32, pp. 1516-1526, 2017.
- [23] J. Hu, M. Xiang, L. Lin, M. Lu, J. Zhu, and Z. He, "Improved Design and Control of FBSM MMC With Boosted AC Voltage and Reduced DC Capacitance," *IEEE Transactions on Industrial Electronics*, vol. 65, pp. 1919-1930, 2018.
- [24] Q. Song, R. Zeng, Z. Yu, W. Liu, Y. Huang, W. Yang, *et al.*, "A Modular Multilevel Converter Integrated With DC Circuit Breaker," *IEEE Transactions on Power Delivery*, vol. 33, pp. 2502-2512, 2018.
- [25] T. Jonsson, P. Lundberg, S. Maiti, and Y. Jiang-Häfner, "Converter technologies and functional requirements for reliable and economical HVDC grid design," *Cigre Canada, Calgary, Canada*, 2013.
- [26] X. Chen, L. Yan, X. Zhou, and H. Sun, "A Novel DVR-ESS-Embedded Wind-Energy Conversion System," *IEEE Transactions on Sustainable Energy*, vol. 9, pp. 1265-1274, 2018.
- [27] R. Li, L. Xu, and D. Guo, "Accelerated switching function model of hybrid MMCs for HVDC system simulation," *IET Power Electronics*, vol. 10, pp. 2199-2207, 2017.
- [28] Infineon Technologies AG, FZ1200R45HL3 datasheet, Feb 2018.
- [29] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, *et al.*, "HVDC circuit breakers for HVDC grid applications," in *Proc. Cigré AORC Technical Meeting, Tokyo, Japan*, 2014.
- [30] L. Ångquist, A. Baudoin, S. Norrga, S. Nee, and T. Modeer, "Low-cost ultra-fast DC circuit-breaker: Power electronics integrated with mechanical switchgear," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, 2018, pp. 1708-1713.



Rui Li received the M.S. and Ph.D degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2008 and 2013, respectively. He is a researcher with University of Strathclyde in Glasgow, UK, since 2013.

His research interests include HVDC transmission system, grid integration of renewable power, power electronic converters, and energy conversion.



Lie Xu (M'03–SM'06) received the B.Sc. degree in Mechatronics from Zhejiang University, Hangzhou, China, in 1993, and the Ph.D. degree in Electrical Engineering from the University of Sheffield, Sheffield, UK, in 2000.

He is currently a Professor at the Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK. He previously worked in Queen's University of Belfast and ALSTOM T&D, Stafford, UK. His research interests include power electronics, wind energy generation and grid integration, and application of power electronics to power systems. He is an Editor of IEEE Transactions on Power Delivery and IEEE Transactions on Energy Conversion.



Lujie Yu received the B.S. degree from North China Electric Power University (NCEPU), Baoding, China, in 2012, M.S. degree from NCEPU, Beijing, China, in 2015, Ph.D degree in Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK in 2019. Currently, he is a lecturer with School of Electrical and Information Engineering, Tianjin University, Tianjin, China.

His research interests include HVDC transmission system and wind power integration.



Liangzhong Yao (SM'12) is the Professor in the School of Electrical Engineering and Automation at Wuhan University, Hubei, China. He received the M.Sc. and Ph.D. degrees in electrical power engineering from Tsinghua University, Beijing, China, in 1989 and 1993, respectively.

He was a Postdoctoral Research Associate at the University of Manchester (formerly the University of Manchester Institute of Science and Technology), Manchester, U.K., from 1995 to 1999; a Senior Power System Analyst in the Network Consulting Department at ABB U.K. Ltd. from 1999 to 2004; the Department Manager for Network Solutions, Renewables and Smart Grids Technologies at ALSTOM Grid Research & Technology Centre, Stafford, U.K., from 2004 to 2011; the Vice President at State Grid Electric Power Research Institute (i.e. NARI Group) in Nanjing from 2011-2012, and the Vice President and Honorary Chief Engineer at China Electric Power Research Institute (CEPRI) in Beijing, from 2011 to 2018.

Dr. Yao is a Chartered Engineer, a Fellow of the IET, and a member of CIGRE.