Advances in Radio Science (2003) 1: 201–205

Advances in Radio Science

A software-radio front-end for microwave applications

M. Streifinger[1], T. Müller[2], J.-F. Luy[2], and E. M. Biebl[1]

[1]Technische Universität München, Fachgebiet Höchstfrequenztechnik, Arcisstr. 21, 80333 München, Germany
[2]DaimlerChrysler Forschungszentrum, Wilhelm-Runge-Str. 11, 89081 Ulm, Germany

Abstract. In modern communication, sensor and signal processing systems digitisation methods are gaining importance. They allow for building software configurable systems and provide better stability and reproducibility. Moreover digital front-ends cover a wider range of applications and have better performance compared with analog ones. The quest for new architectures in radio frequency front-ends is a clear consequence of the ever increasing number of different standards and the resulting task to provide a platform which covers as many standards as possible.

At microwave frequencies, in particular at frequencies beyond 10 GHz, no direct sampling receivers are available yet. A look at the roadmap of the development of commercial analog-to-digital-converters (ADC) shows clearly, that they can neither be expected in near future.

We present a novel architecture, which is capable of direct sampling of band-limited signals at frequencies beyond 10 GHz by means of an over-sampling technique. The well-known Nyquist criterion states that wide-band digitisation of an RF-signal with a maximum frequency f requires a minimum sampling rate of $2 \cdot f$. But for a band-limited signal of bandwidth B the demands for the minimum sampling rate of the ADC relax to the value $2 \cdot B$. Employing a noise-forming sigma-delta ADC architecture even with a 1-bit-ADC a signal-to-noise ratio sufficient for many applications can be achieved. The key component of this architecture is the sample-and-hold switch. The required bandwidth of this switch must be well above $2 \cdot f$.

We designed, fabricated and characterized a preliminary demonstrator for the ISM-band at 2.4 GHz employing silicon Schottky diodes as a switch and SiGe-based MMICs as impedance transformers and comparators. Simulated and measured results will be presented.

Correspondence to: M. Streifinger
(streifinger@ei.tum.de)

1 Introduction

Many applications of communication, sensor and signal processing systems would provide greater performance, if various standards could be handled with only one hardware device. Conceivable applications could be combined GSM / GPS devices (Müller et al., 2000) or a GPS receiver combined with a short-range radar. One first step towards this aim is the realization of a direct sampling receiver. The advantage is, that the input frequency and the channel bandwidth can be chosen in the receiver's digital part, fully independent of the used front-end.

In the following some analogue receiver architectures and the architecture of a direct sampling receiver will be introduced. The validity of the concept given and multiple simulations will be proved by measured results of a scaled demonstrator at 2.4 GHz.

2 Multiband capable receiver architectures

The requirements for multiband receivers lead to two main needs regarding the receiver topology: On the one hand the centre frequency has to be tuned over a large frequency range. On the other hand the bandwidths of the standards can differ by more than two decades.

The limit of heterodyne receivers regarding the tuneable bandwidth is given by the first IF frequency. Because of the non-linear character of the mixer, fourth order harmonics will arise between baseband and the double bandwidth of the input filter. This limits the maximum tuning bandwidth significantly or increases the number of IF stages up to an uneconomical number.

An attractive alternative is the direct conversion receiver. As shown in the block diagram (Fig. 1) the signal is mixed down to the baseband by two orthogonal carriers separately (Jentschel et al., 2000). This receiver can be built up very economically but several drawbacks prevent the usage for multimode receivers. Because of the always existing I-Q

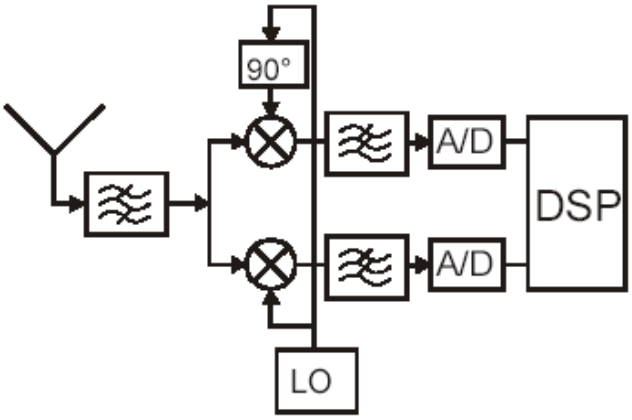

Fig. 1. Block diagram of the direct conversion receiver.

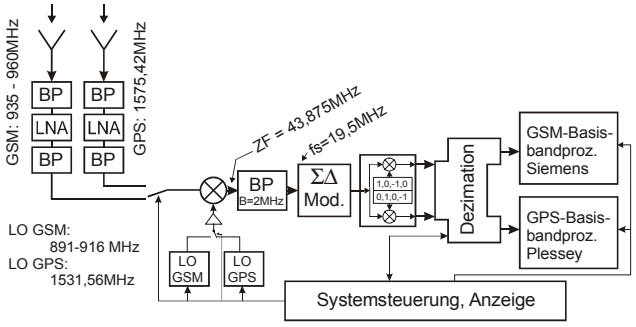

Fig. 2. Block diagram of a GSM – GPS receiver with common IF.

mismatch this topology is not suited for high order modulation schemes. A leakage of the LO leads to partly time variant DC bias after the down converting process which are costly to suppress. Because the bandwidth of the standard is defined by the lowpass filter, it has to be configured for multimode reception (Böhm et al., 1999).

The problem of LO leakage can be partly solved by using a very low IF for this type of receiver and implementing the shift into the baseband in the digital domain (Crols and Steyaert, 1998).

Looking at standards at mm-wave frequencies the Six-Port receiver becomes attractive (Tatu et al., 2001). The six-port can be considered as a black box with two inputs and four outputs. When the six-port itself is linear and the outputs are non-linear the relations between input signals and the output signals can be derived by a calibration procedure. The feasible tuning bandwidth is given by the characteristics of the six-port itself and the subsequent non-linear devices. The channel bandwidth is defined by the lowpass filters behind the non-linear outputs. A straight-forward approach to software configurable receivers is to sample the input signal at an IF or the input frequency itself. Bandpass-limited undersampling can be used to reduce the sampling rate and the effort in processing the digital signals. Unfortunately, the influence of sampling jitter and the requirements on the anti aliasing filter increases when doing this.

A disadvantage of sampling at IF is, that the IF filter defines the maximum channel bandwidth. When choosing a large IF bandwidth to receive any possible standard, the required dynamic range increases and leads to intermodulation specifications comparable to wide band sampling systems.

Figure 2 shows the block diagram of a combined GSM – GPS receiver, where both standards are received in time multiplex (Müller, 2002). The intermediate frequency was chosen in a way that the digital down-conversion can be realized by the multiplication with ones and zeros. The baseband processing is done by standard chipsets (Müller et al., 2000).

When sampling the RF signal directly, the analog-to-digital converter has to cope the high input bandwidth and all interferers after the antenna. The immense advantage is that we obtain full flexibility in choosing the input frequency, channel bandwidth etc. by selecting the proper digital signal processing. The following chapter will present the design of a 24GHz sampling head.

3 Concept of a direct sampling receiver

The concept of the direct sampling receiver is based on a band limited over sampling approach. The Nyquist-criterion is applied to the bandwidth of the signal of interest rather than to the complete incoming spectrum. Sampling of the whole spectrum of the input signal with a maximum frequency f, the minimum sample rate would be $2 \cdot f$. If the bandwidth B of the signal of interest is well known, the demands for the minimum sampling rate relax to the value of $2 \cdot B$ (Vaughan et al., 1991).

In case of oversampling the oversampling ratio (OSR) is defined as ratio of half the sampling rate related to the 3 dB-bandwidth of the filter. For an application in the ISM band (f_0 = 24 GHz) the required bandwidth would be B = 500 MHz. We assume a ratio of

$$\frac{f_0 \cdot 4}{f_s} = n = 9$$

and obtain a sampling frequency of f_s = 10.66 GHz and an OSR = 10.66 in this case. The expected resolution of this ADC is 3 bit (without noise shaping).

Using this concept, a noise shaping Sigma Delta Converter can be realized which will further improve the resolution (Norsworthy et al., 1997). The expected signal to noise ratio is shown in Fig. 3.

The aim is the realisation of the architecture shown in Fig. 4 for an input frequency of 24 GHz. As a first step, a scaled demonstrator was built up and analysed at 2.4 GHz. The following exposition mainly handles this demonstrator. If necessary and sensible, comments regarding the feasibility at 24 GHz will be made.

The key components of the receiver are the anti aliasing filter, the clocked sample & hold circuit (S/H) and the comparator or ADC itself as shown in Fig. 4 (Luy and Müller, 1999).

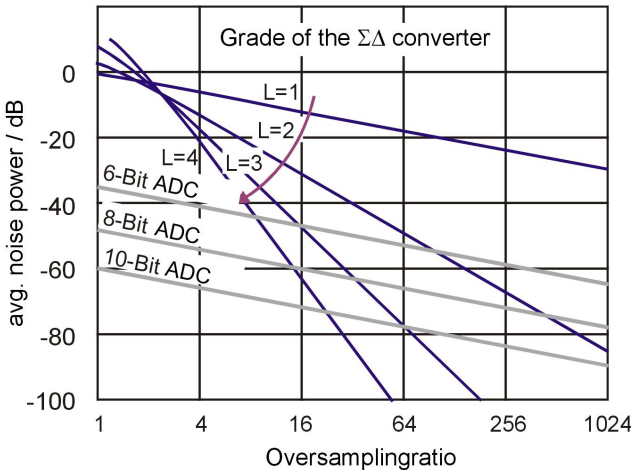

Fig. 3. Reachable signal to noise ratio of a 1-bit sigma delta converter and converters without noise shaping dependant on the OSR.

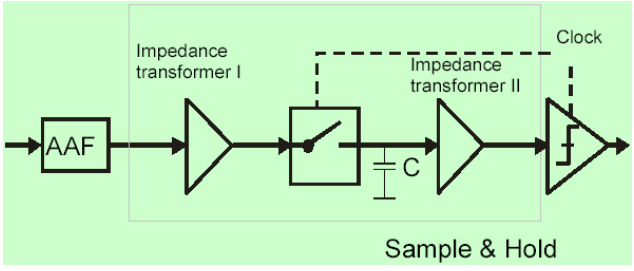

Fig. 4. Digital millimeter wave receiver architecture.

The anti-aliasing-filter (AAF) suppresses all out-of-band interferers in order to fulfil the Nyquist criterion at least regarding the bandwidth of the signal of interest.

The output voltage of the S/H switch must follow the input signal as long as the switch is closed (Fig. 6). Thus, the output impedance of the first amplifier driving the switch bridge has to be rather small. Good results are received by values of less then 10Ω. For this reason an impedance transformer is needed, as we usually have systems with a 50Ω wave impedance. On the other hand, to hold the output voltage of the S/H switch constant as long as the switch is open, the input impedance of the second amplifier should be more than 200Ω. So we need a second impedance transformer, to transform the 200Ω impedance back to a value dependant on the subsequent stage. Moreover both impedance transformers have to amplify the signals according to the dynamic range of the respective stages.

The clocked comparator and further signal processing parts are beyond the scope of this paper.

The key component of the receiver is the S/H circuit as shown in Fig. 5. As sampling switch a SIMMWIC Schottky diode quadruple bridge is used, followed by a shunt lumped holding capacitor (Jensen and Larson, 2001). The diodes are well suited because of their high reverse and their low forward resistance. As the diode switch contains four strong

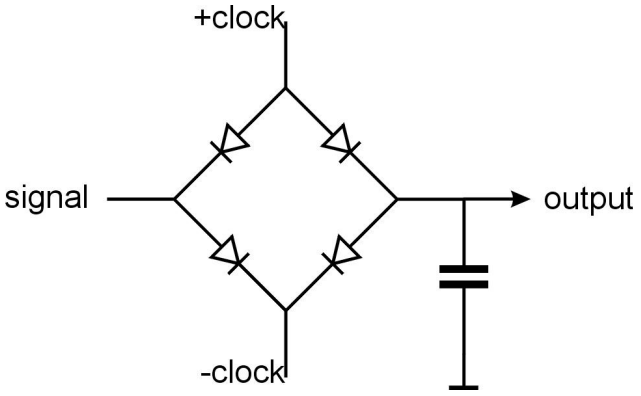

Fig. 5. schematic of the sample and hold circuit.

nonlinearities generating many harmonics and intermodulation products an precise simulation of the circuit is rather difficult but nonetheless absolutely essential. Generally spoken the diode switch is the most broad-banded component of the whole front-end.

To prevent cross talk between the incoming signal and the clock signal, the diode quadruple has to be driven symmetrically. This is achieved by implementing a balun circuit in the clock signal path. Further very critical components are the length of the wave guide between the diode switch and the holding capacitor as well as the capacitor's physical dimensions. If one of them two is too large, oscillations emerge because of the parasitic inductivities and the holding capacitance.

4 Simulation of the sample and hold circuit

Having an exact diode model is crucial for the correct simulation of the sampling circuit. The following parameters where extracted from DC and RF measurements: Saturated reverse current: I_S = 4,3 nA, serial resistance R_S = 8,5Ω, ideality factor N = 1.09 and zero bias junction capacity C_{j0} = 12 fF...14 fF.

Simulations have shown that small changes of I_S, R_S and N do not affect the behaviour of the device much, whereas even small changes in the value of C_{j0} can deteriorate the functionality of the switch: During the hold stage, output voltage shows sinusoidal oscillations. Obviously, the isolation between signal input and the output is not sufficient due to the capacitive coupling by the junction capacity. As a countermeasure one can either apply a reverse DC bias or increase the clock power. Adding reverse DC bias increases the complexity of the circuit significantly, increasing the clock power is limited by the maximum forward current of the diodes. Simulations showed that we could expect sufficient isolation for reasonable clock power without reverse bias for working in the ISM Band at 24 GHz.

Figure 6 shows the voltage measured at the holding capacitor. As input signal an unmodulated carrier of 2.4 GHz was used. The SMA connectors and bonding wires were

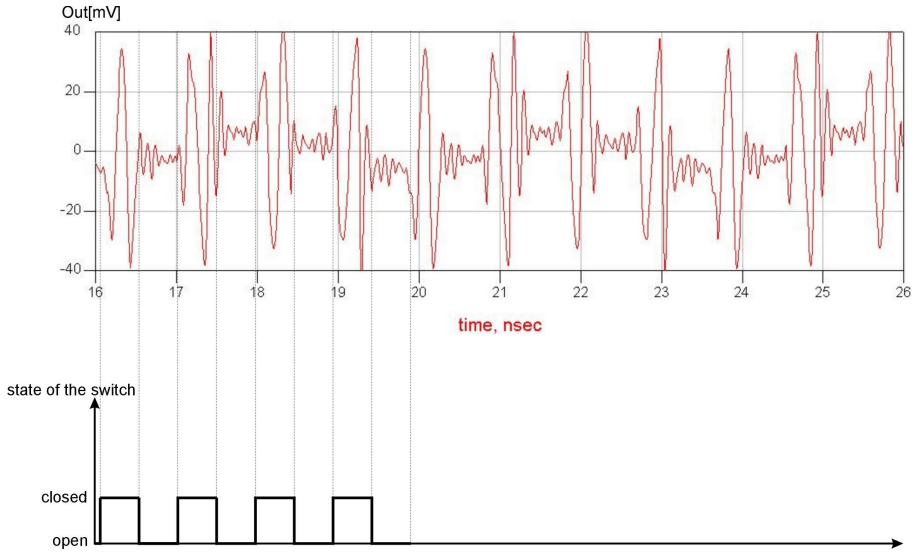

Fig. 6. Simulated voltage time curve at the holding capacitance and state of the diode switch.

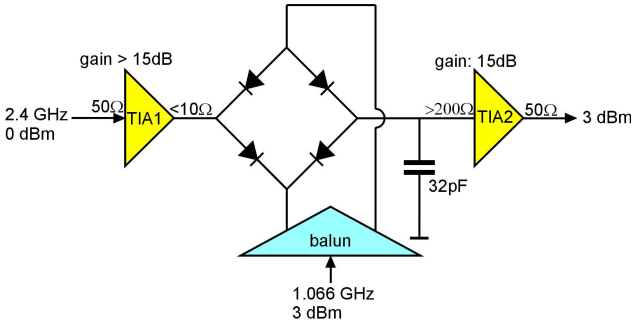

Fig. 7. Specification of the 2.4 GHz demonstrator.

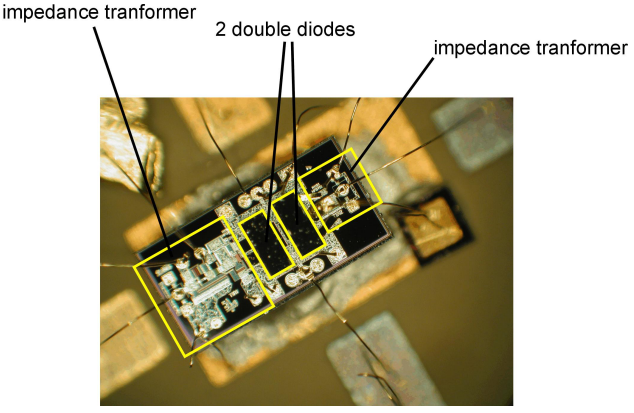

Fig. 8. The chip module with both impedanc tranformers and the diode bridge.

not considered in this simulation. As can be seen, the output voltage follows the input signal as long as the switch is "closed". When the switch is open, the output voltage is not exactly constant. In fact, decaying high-frequency oscillations are observed. A comprehensive examination of this effect shows, that parasitic inductivities of the bonding wires and the via holes are responsible for that behaviour. As shown later (Fig. 9), a simulation including these parasitics predicts very well the measured results. This indicates that proper models are used for the hardware components and layout structure.

5 Demonstrator at 2.4 GHz

For being able to verify the simulated results a scaled demonstrator at 2.4 GHz was built. It was realized without AAF and comparator. Based on the results of the simulations showed, the following specifications (Fig. 7) were chosen.

The demonstrator was built according to the specifications given in Fig. 7 and characterized. Both impedance amplifiers were realized by ATMEL. To work around the problems of the bonding wires and their parasitic influences, both impedance transformers were assembled on one chip where the diodes were also flip chip bonded on. In future, also the holding capacity will be integrated in this chip module.

The chip module was mounted on TMM10i substrate and connected to the balun and the bias circuits. The connections to the sources and to a sampling oscilloscope were done via SMA connectors mounted on the demonstrator's backside.

Figure 9 shows the output voltage, measured at the holding capacitance. This signal corresponds well to the simulated output voltage shown in Fig. 6. A problem; which has still to be solved, are the oscillations created by the parasitics. They are mainly caused by the externally mounted chip capacitor. In future, it will be integrated on the chip module containing the diode bridge and the impedance transformers.

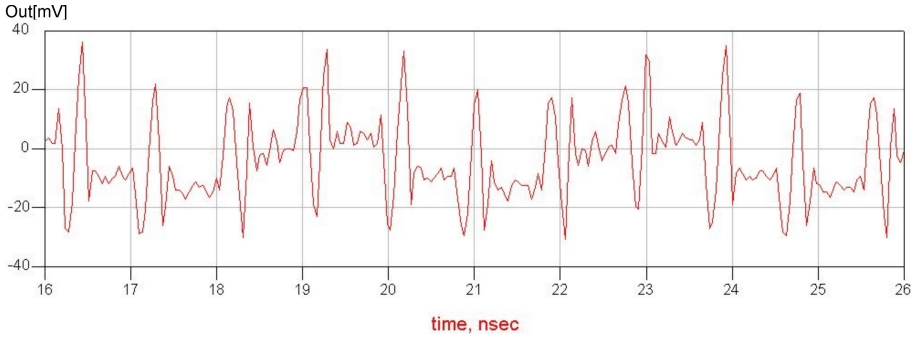

Fig. 9. Measured output voltage.

6 Conclusion

An overview on existing mm-wave receivers was given. The direct sampling receiver based on band-limited oversampling seems to be the best and most flexible solution, but as it is the most ambitious approach, it still needs extensive development. The critical components have been analysed and specified. It appears that a realisation for applications working in the ISM band at 24 GHz seems possible using present technologies.

References

Böhm, K., Pfau, J., Schnepp, H.: A tunable low power BiCMOS continuous-Time Gm-C lowpass filter, IEEE Radio and Wireless Conference, T5.6, Denver, Colorado, USA, August 1999.

Crols, J. and Steyaert, M. S.: Low-IF Topologies for High-Performance Analog Front Ends of Fully Integrated Receivers, IEEE Tr. on Circuits and Systems – II: Analog and Digital Signal Processing, 45, 3, 1998.

Jensen, J. C. and Larson, L. E.: A Broadband 10-GHz Track-and-Hold in Si/SiGe HBT Technology, IEEE Journal of Solid State Circuits, 36, 3, 2001.

Jentschel, H.-J., Berndt, H., and Pursche, U.: Direct Conversion Receivers – Expectations and Experiences, in RF Front End Architectures, IEEE MTT-S 2000, Boston, Workshop, 2000.

Luy, J. F. and Müller, Th.: Front-End Architectures in Millimeter-Wave Systems: From Analogue to Digital Concepts, EuMC 1999, Munich, pp. 309–312, 1999.

Müller, T., Biebl, E. M., Böhm, K., and Luy, J.-F.: Zwischenfrequenz – digitalisierender GPS / GSM Empfänger, Kleinheubacher Berichte 2000, Band 43, pp. 301–307, 2000.

Müller, T.: Direktabtastende Architekturen fr Hochfrequenzempfänger, Dissertation, Fachgebiet Höchstfrequenztechnik, TU München, 2002.

Norsworthy, S., Schreier, R., and Temes, G.: Delta-Sigma Data Converters, Theory, Design and Simulation, IEEE Press 1997, Piscataway, NJ, 1997.

Tatu, S. O., Moldovan, E., Wu, K., and Bosisio, R. G.: A New Direct Millimeter-Wave Six-Port Receiver,IEEE Tr. on Microwave Theory and Techniques, 49, 12, 2001.

Vaughan, R. G., Scott, N. L., and White, D. R.: The Theory of Bandpass Sampling, IEEE Transactions on Signal Processing, 39, 9, 1991.