EUROPEAN MICROWAVE WEEK 2019
SIX DAYS · THREE CONFERENCES · ONE EXHIBITION
PORTE DE VERSAILLES PARIS, FRANCE
29TH SEPTEMBER - 4TH OCTOBER 2019
Exhibition Hours:
Tuesday, 1st October 9.30 - 18.00
Wednesday 2nd October 9.30 - 17.30
Thursday 3rd October 9.30 - 16.30
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WS-01

Recent advances in SiGe BiCMOS: technologies, modelling & circuits for 5G, radar & imaging

TARANTO

http://tima.univ-grenoble-alpes.fr/taranto/

On wafer small signal characterization beyond 100 GHz for compact model assessment

Sebastien Fregonese[#1], Marina Deng[#1], Marco Cabbia[#1], Chandan Yadav[#1], Soumya Ranjan Panda [#1&2], Thomas Zimmer[#1]

[#1]Université Bordeaux / CNRS, laboratoire IMS, FRANCE

[#2]IIT Madras, India

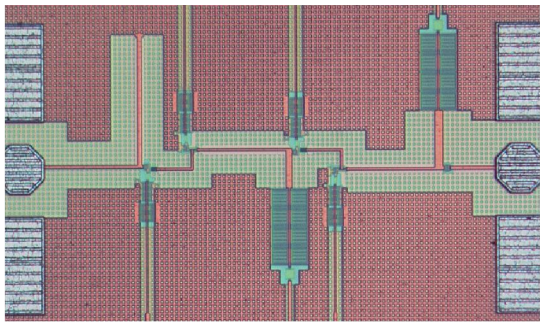
[#1] Sebastien.Fregonese@ims-bordeaux.fr

Outline

- Motivation
- EM simulation vs Measurement up to 500 GHz
- HBT measurement up to 500 GHz
- Conclusion and Outlooks

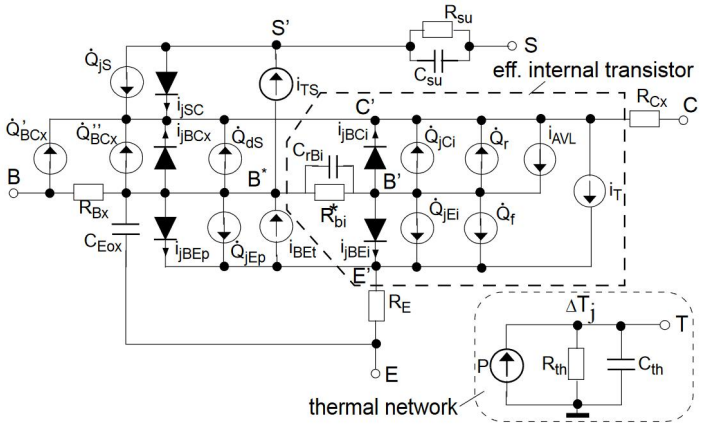
Motivation

Transistor HF Characterization Challenges



RF circuit/system design

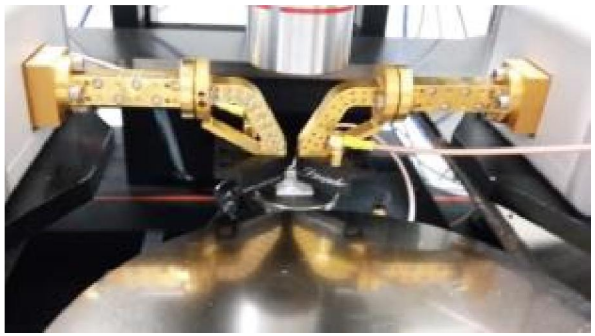
Relies on



Accurate compact models

Extraction of specific parameters
Validation

Accurate S-parameter measurements above 110 GHz = big challenge



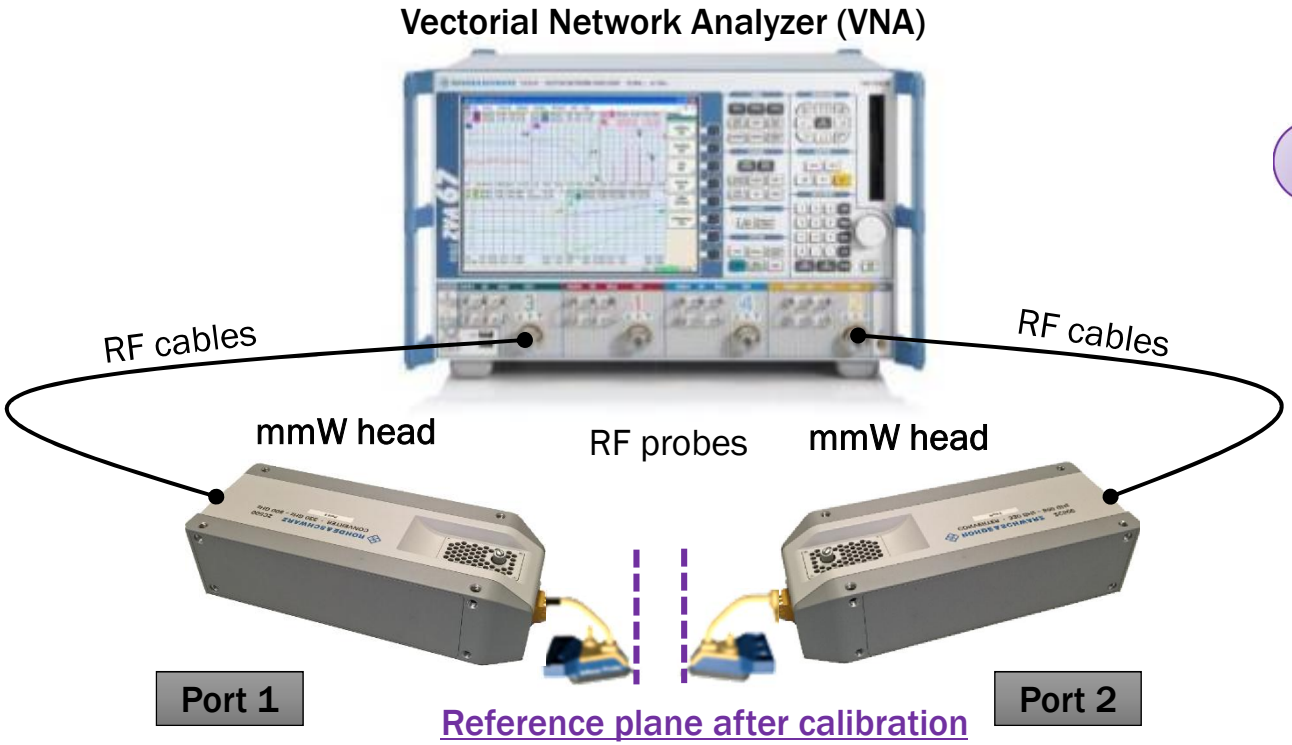
Motivation

- Calibration & De-embedding Issues

Standard procedure (2-step calibration)

1 → Off-wafer calibration on ISS

2 → On-wafer de-embedding

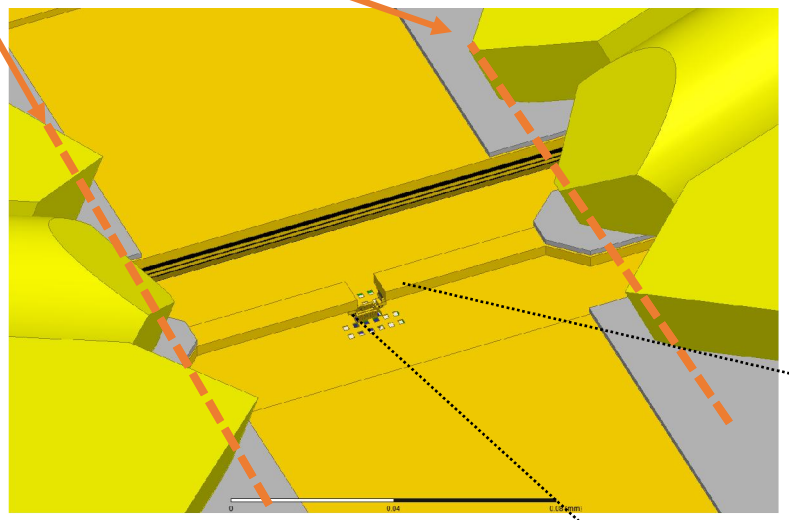


Impedance Standard Substrate
From Cascade Microtech

Motivation

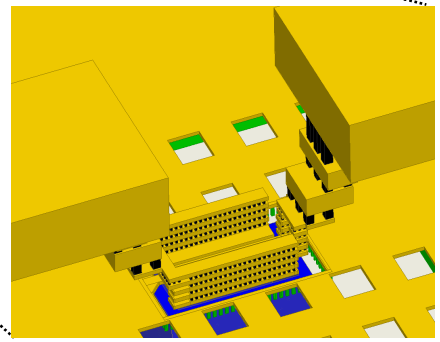
- Calibration & De-embedding Issues

Reference plane after calibration



1 → Off-wafer calibration on ISS

2 → On-wafer de-embedding



Ref. plane after de-embedding (DUT terminals)

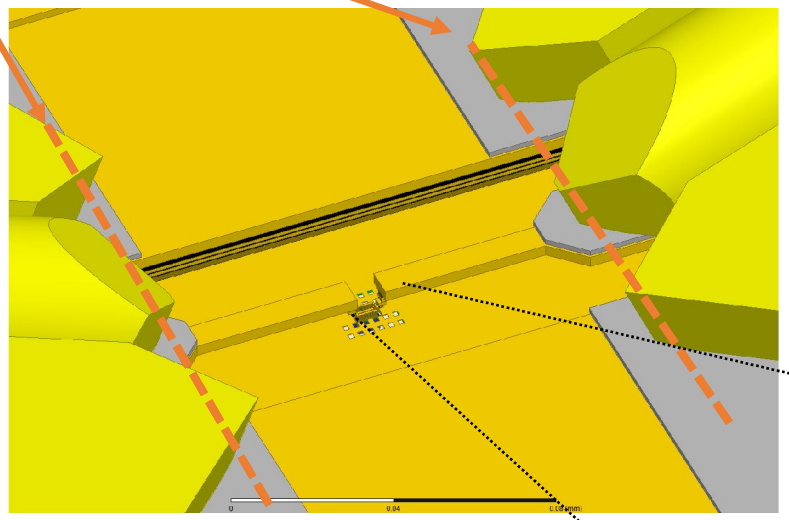
Different electrostatic environment

calibration range of validity ?

Motivation

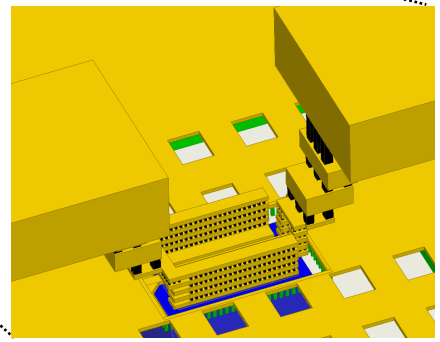
- Calibration & De-embedding Issues

Reference plane after calibration



1 → On-wafer TRL calibration

2 → On-wafer de-embedding



Ref. plane after de-embedding (DUT terminals)

Same electrostatic environment

calibration range of validity ?

Motivation

- S parameters measurement above 110 GHz requires to answer the following questions:

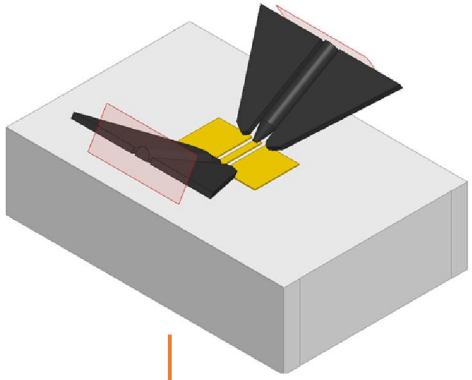
  - Which calibration & de-embedding method should I use ?

  - Do I really measure my DUT ?
    - ⇒ Impact of adjacent structures
    - ⇒ Impact of probes

  => Need for reproducing measurement results with EM simulation tools

EM simulation vs Measurement up to 500 GHz

ISS SOLT

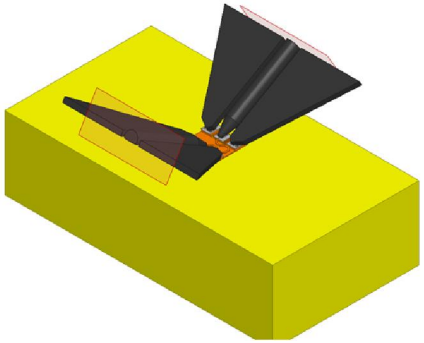


Simulation of :
Thru
Reflect (open, Short)
Lines
Load

Extraction of SOLT parameters using ISS TRL

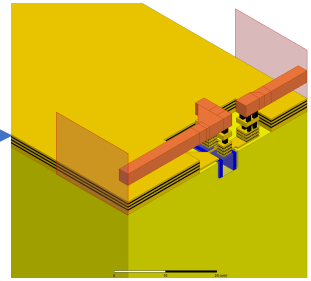
Simulation of :
DUT
Pad open
Pad short

Intrinsic DUT



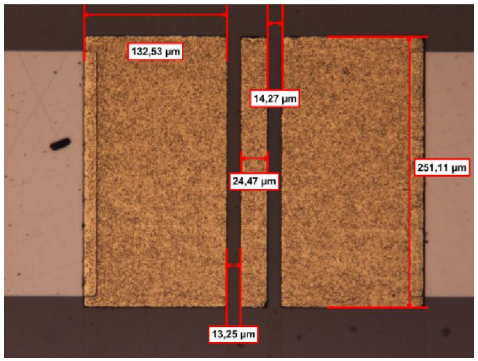
SOLT on ISS

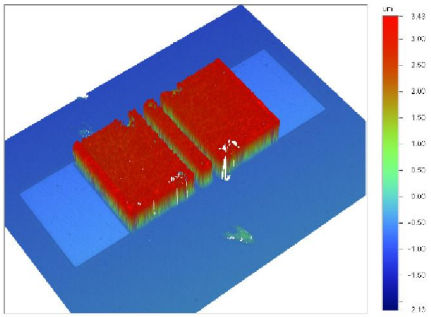
De-embedding



EM simulation vs Measurement up to 500 GHz

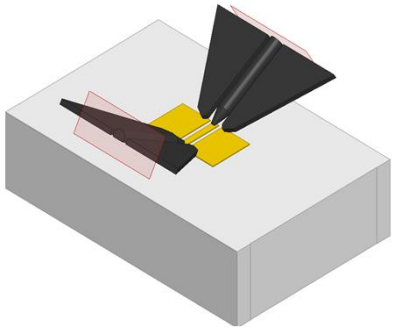
- **Characterisation of the ISS calibration kit for SOLT**





Interferometry image of the through from the ISS (GGB-CS15)

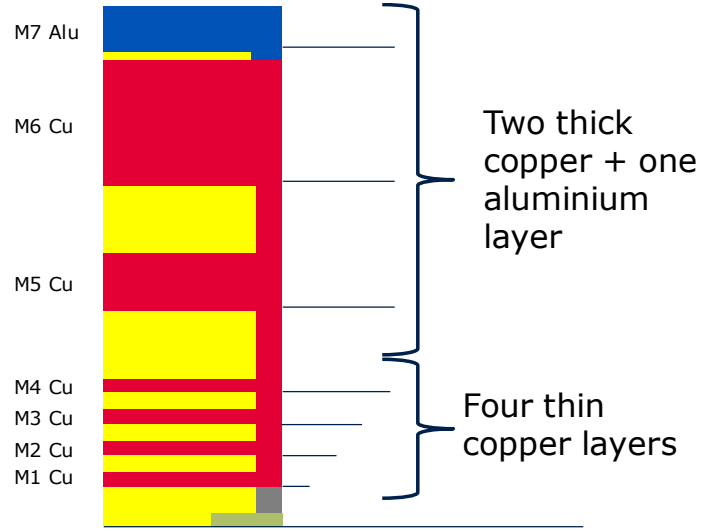
	Data sheet of CS15 delivered by Pico-probe GGB industries used for 50-125 µm probe pitch	EM simulation for 50 µm probe pitch (extracted from TRL at 60 GHz and 250 GHz)
Open	3.25fF	3.2-3.4fF
Short	2pH	1.5 pH-2.5pH
Load	1.5fF	1.4-2.2fF
Through	1.13ps	1.10ps



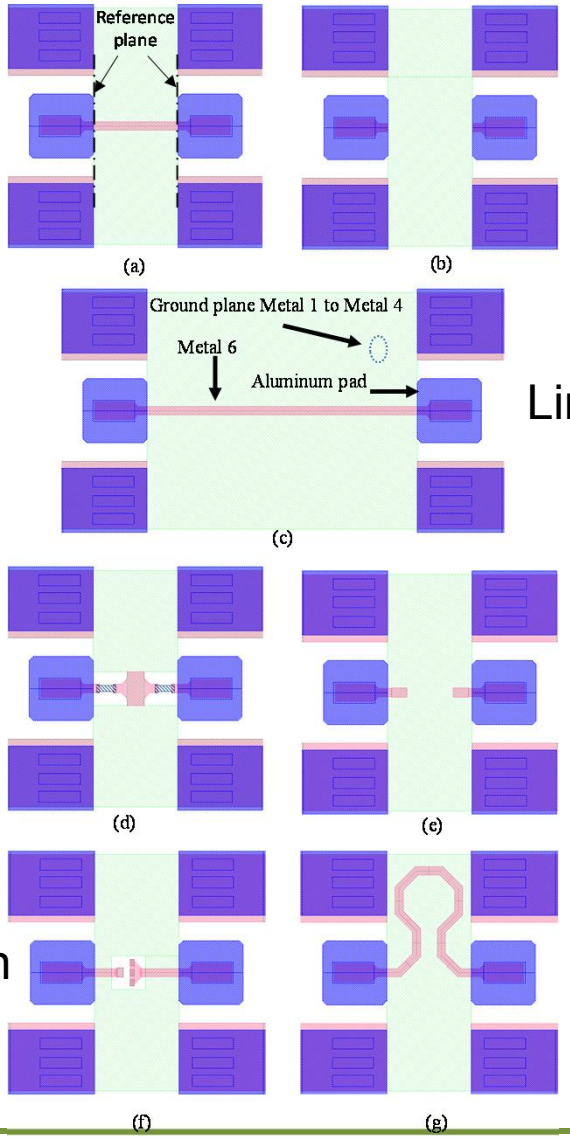
EM simulation vs Measurement up to 500 GHz

- Silicon test structures:

The probe pitch is 50 µm

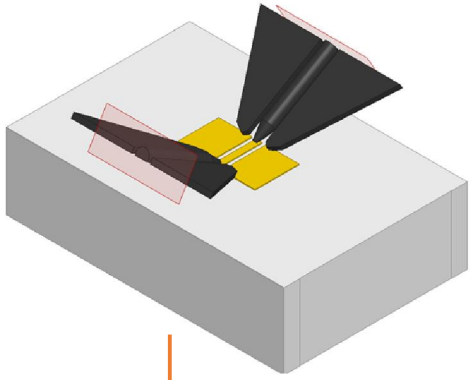


Infineon's B11HFC BEOL



EM simulation vs Measurement up to 500 GHz

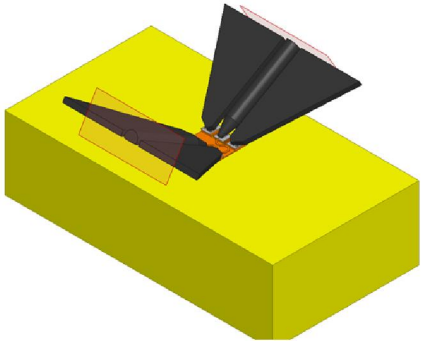
ISS SOLT



Simulation of :
Thru
Reflect (open, Short)
Lines
Load

Extraction of SOLT parameters using ISS TRL

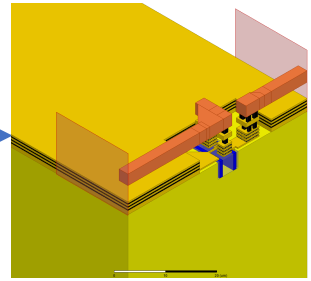
Simulation of :
DUT
Pad open
Pad short



SOLT on ISS

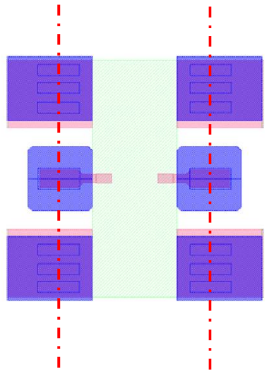
De-embedding

Intrinsic DUT

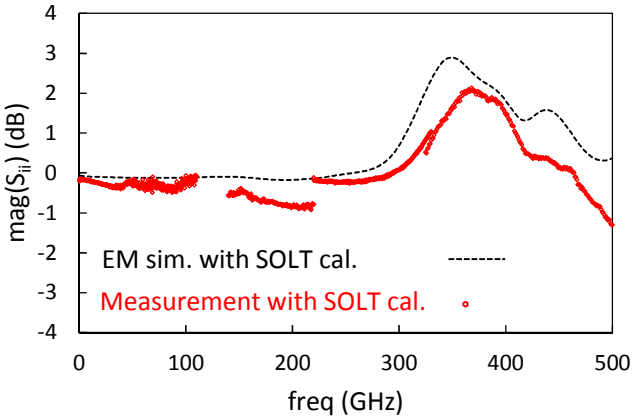


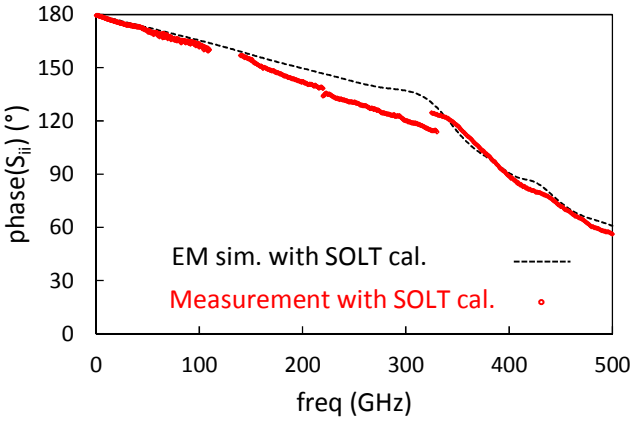
EM simulation vs Measurement up to 500 GHz

- Pad short & Pad open

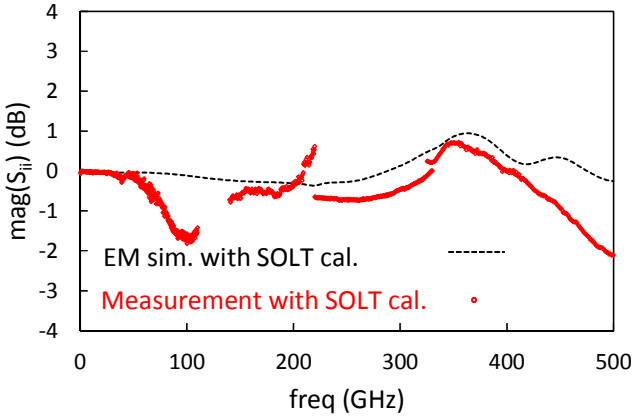


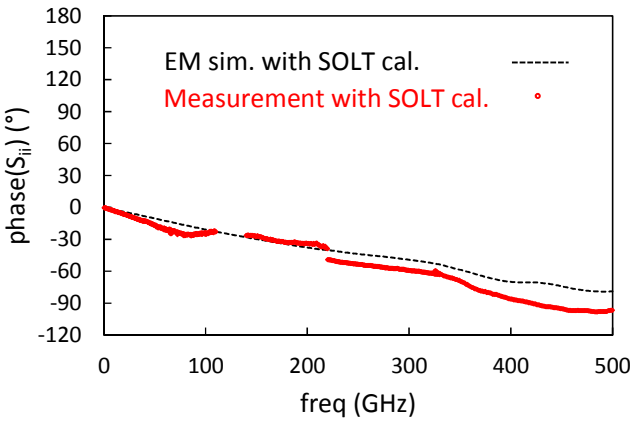
Ref. plane



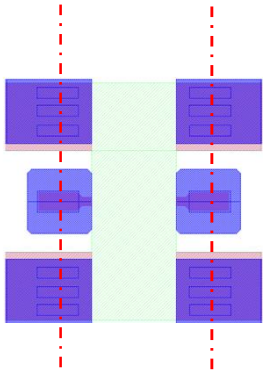


PAD SHORT
after SOLT calibration
Measurement vs Simulation





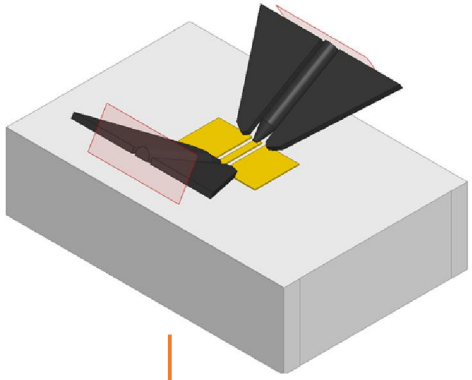
PAD OPEN
after SOLT calibration
Measurement vs Simulation



Ref. plane

EM simulation vs Measurement up to 500 GHz

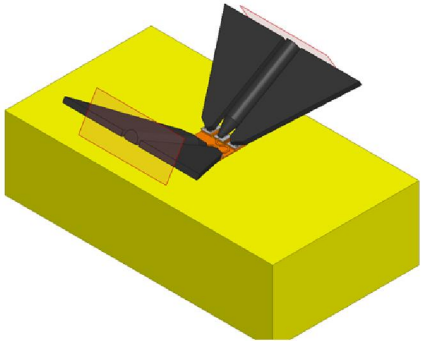
ISS SOLT



Simulation of :
Thru
Reflect (open, Short)
Lines
Load

Extraction of SOLT parameters using ISS TRL

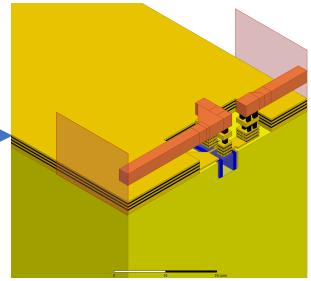
Simulation of :
DUT
Pad open
Pad short



SOLT on ISS

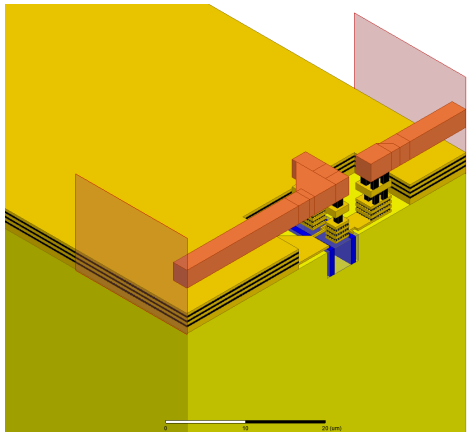
De-embedding

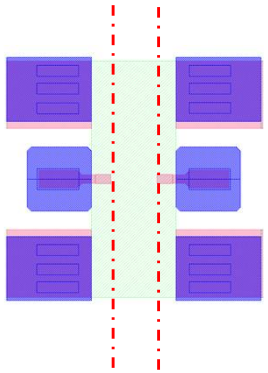
Intrinsic DUT



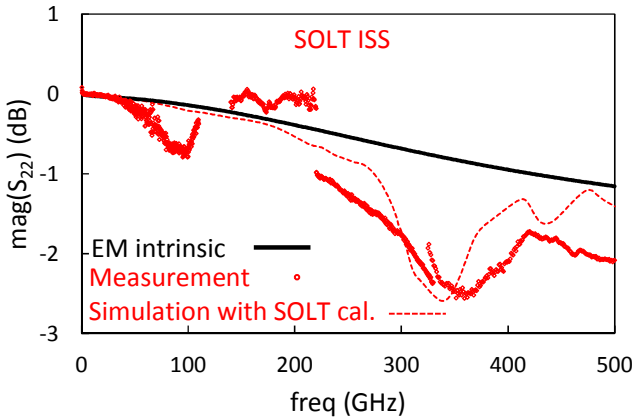
EM simulation vs Measurement up to 500 GHz

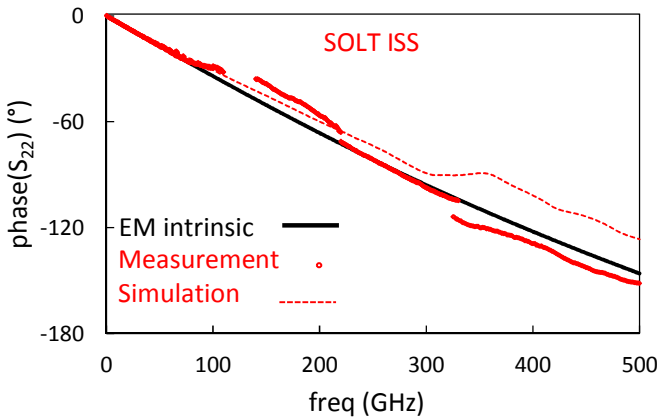
- Calibration and de-embedding : transistor open





Ref. plane

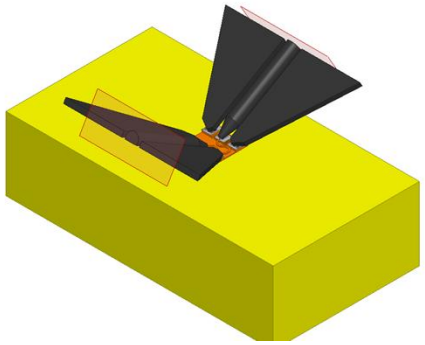




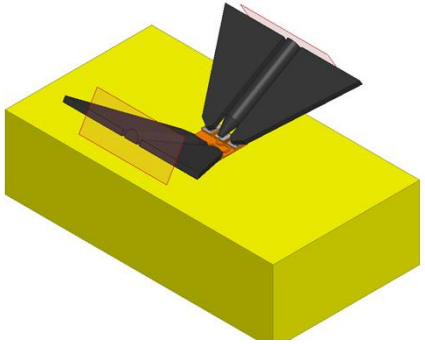
EM simulation vs Measurement up to 500 GHz

On wafer TRL simulation

Simulation of :
Thru
Reflect
Lines
Load

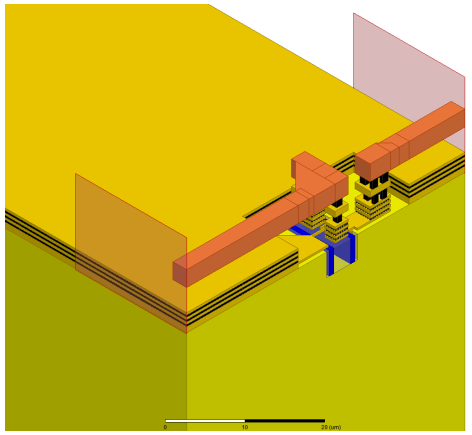


Simulation of :
DUT
Pad open
Pad short



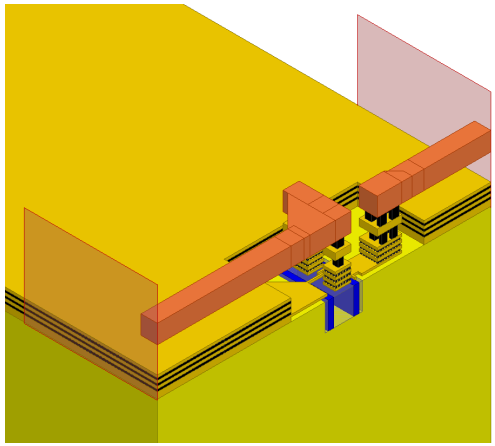
TRL on wafer with Zc correction

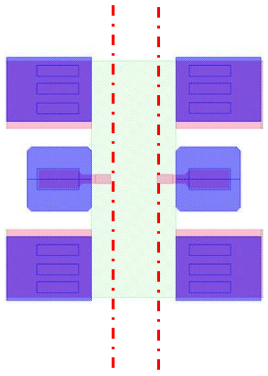
Intrinsic DUT



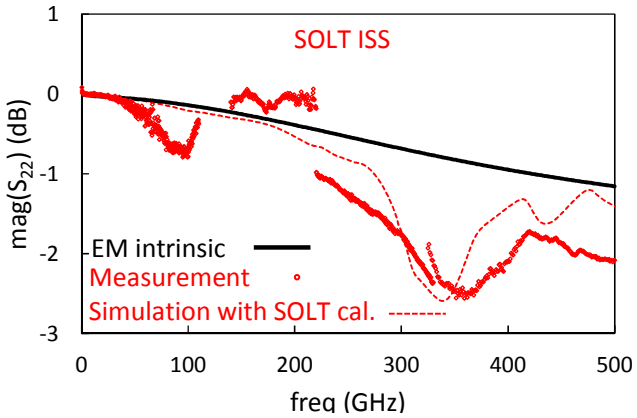
EM simulation vs Measurement up to 500 GHz

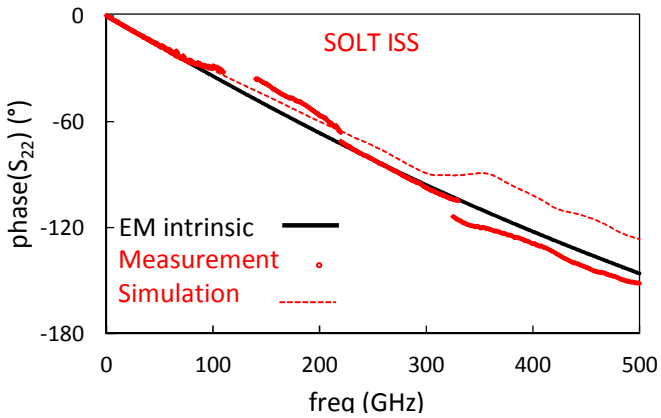
- Calibration and de-embedding : transistor open

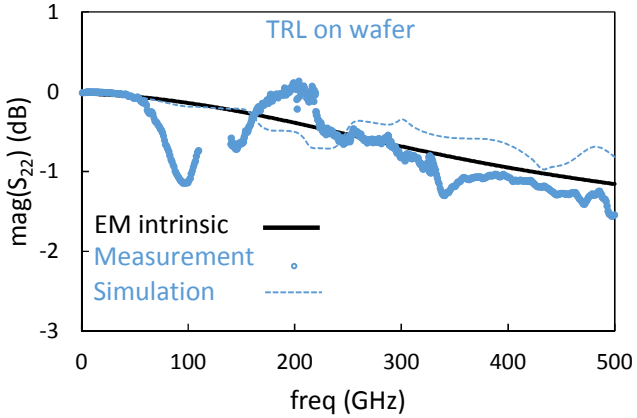


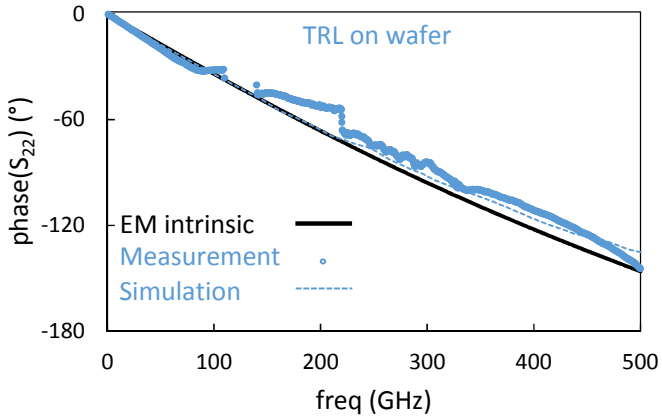


Ref. plane



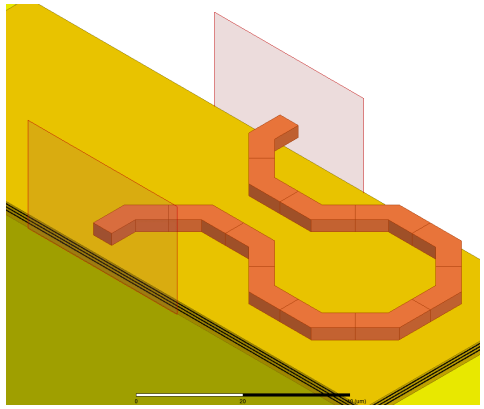


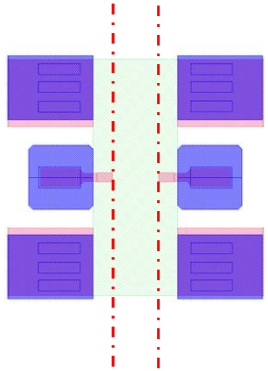




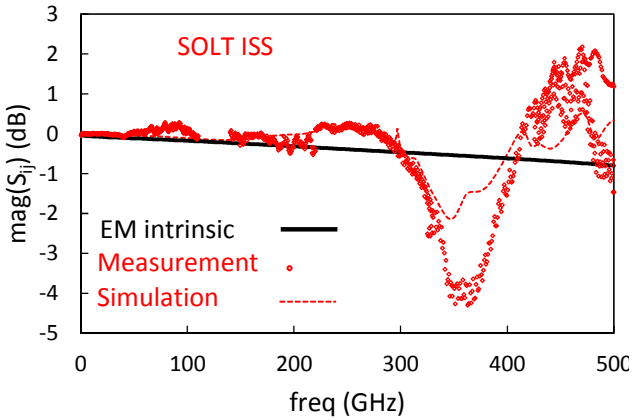
EM simulation vs Measurement up to 500 GHz

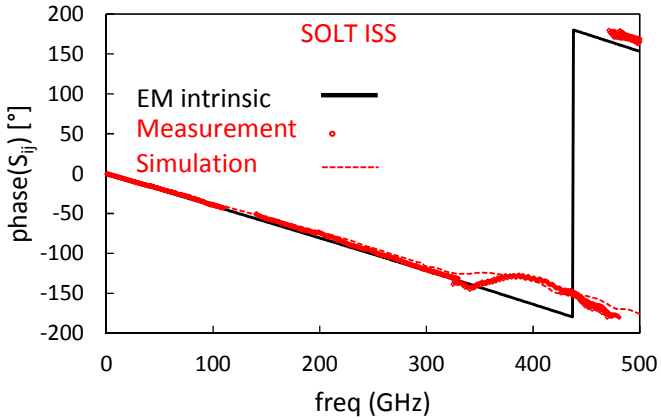
- Calibration and de-embedding : meander line

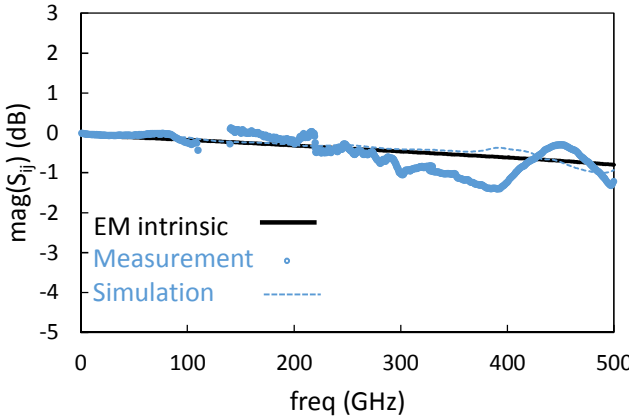


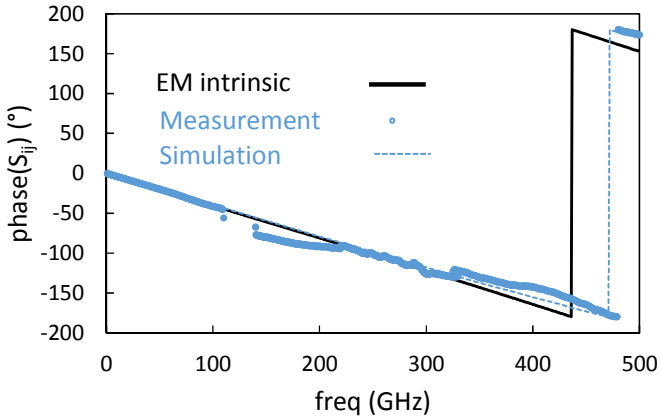


Ref. plane









EM simulation vs Measurement up to 500 GHz

- Limitation of the SOLT ISS parameters:
  - Frequency dependence
  - Probe dependence

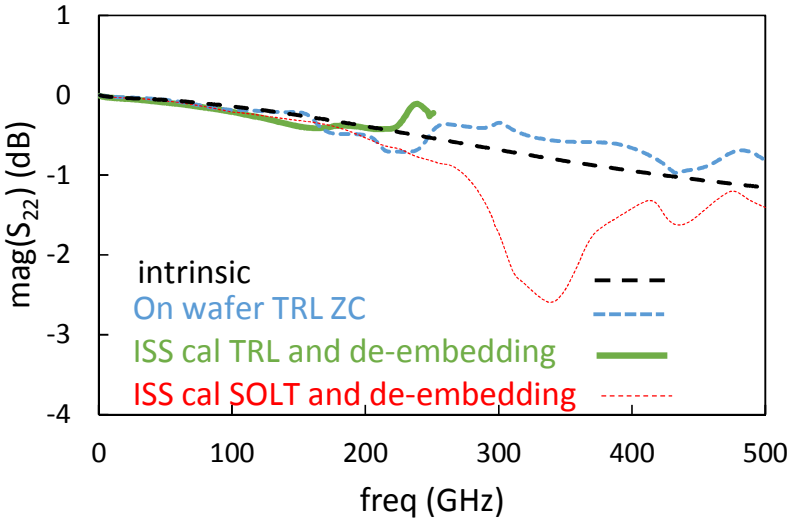
- Substrate to probe coupling
  - Probe dependence
  - Cal-kit material and wafer material

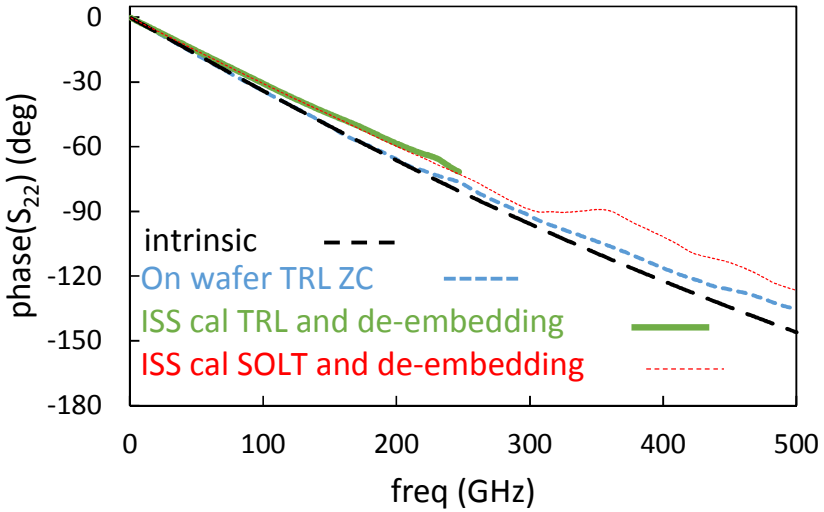
- Limitation of the de-embedding

=> TRL on ISS is used to identify these 3 limitations

EM simulation vs Measurement up to 500 GHz

- SOLT on ISS and TRL ISS with pad-open pad-short de-embedding and on wafer TRL versus intrinsic simulation





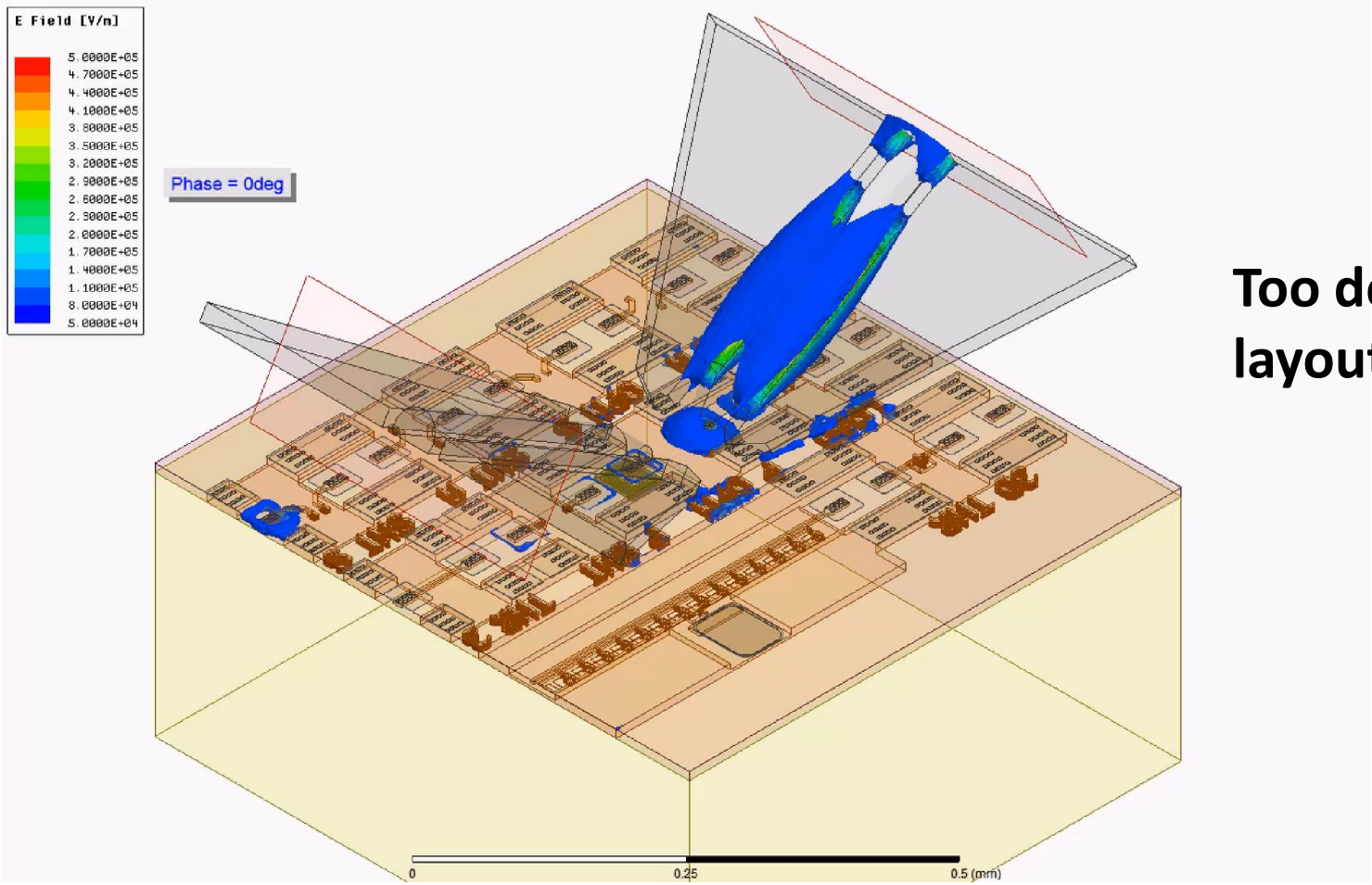
- ISS SOLT and TRL give similar results on the phase but deviate slightly from the intrinsic result from 50 GHz

⇒Deviation is due to electrostatic environment and/or de-embedding procedure

⇒SOLT calibration itself and parameters cannot explain the deviation of the phase

EM simulation vs Measurement up to 500 GHz

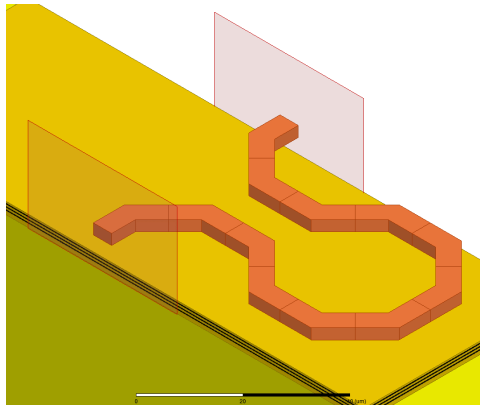
- Impact of adjacent structures: EM simulation @ 500 GHz

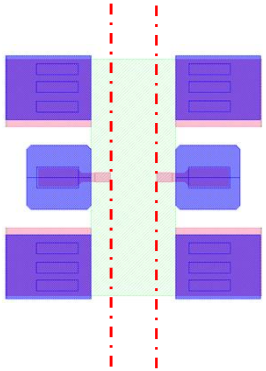


Too dense layout !

EM simulation vs Measurement up to 500 GHz

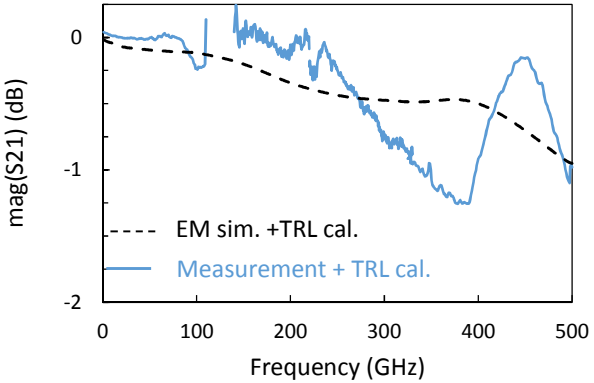
- Impact of adjacent structures:

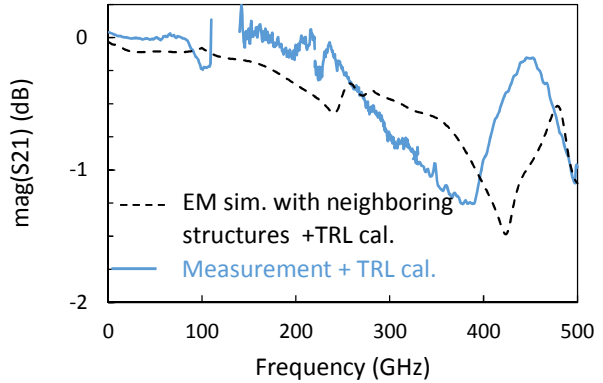




Ref. plane

With adjacent devices in Thru, Refl., Line and DUT



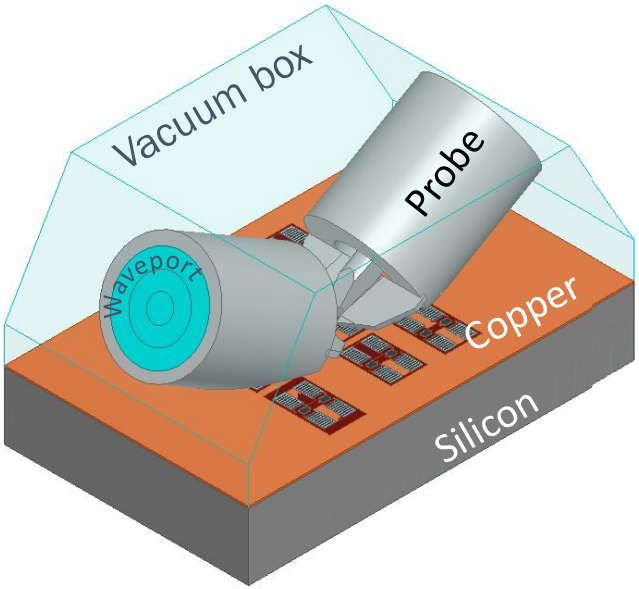


Adjacent structures modifies the result

EM simulation vs Measurement up to 500 GHz

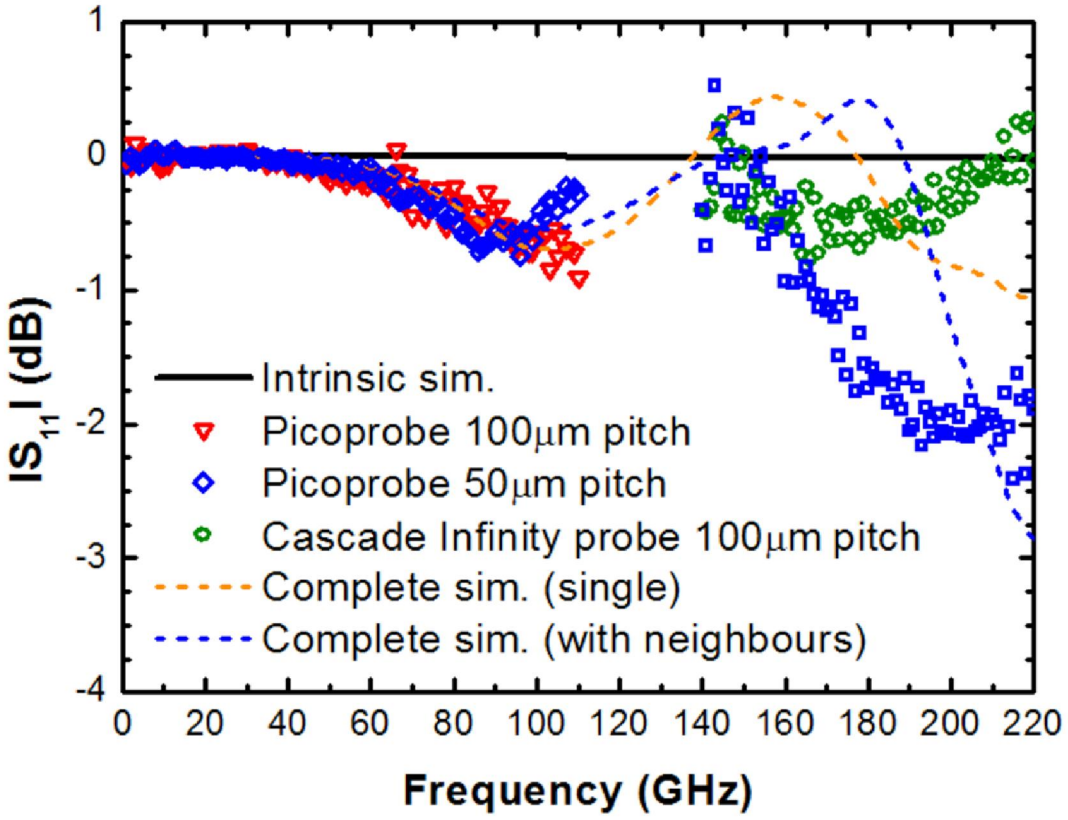
- Impact of probe topology
  - On wafer calibration (STMicroelectronics B55 technology)

IEEE ICMTS 2018



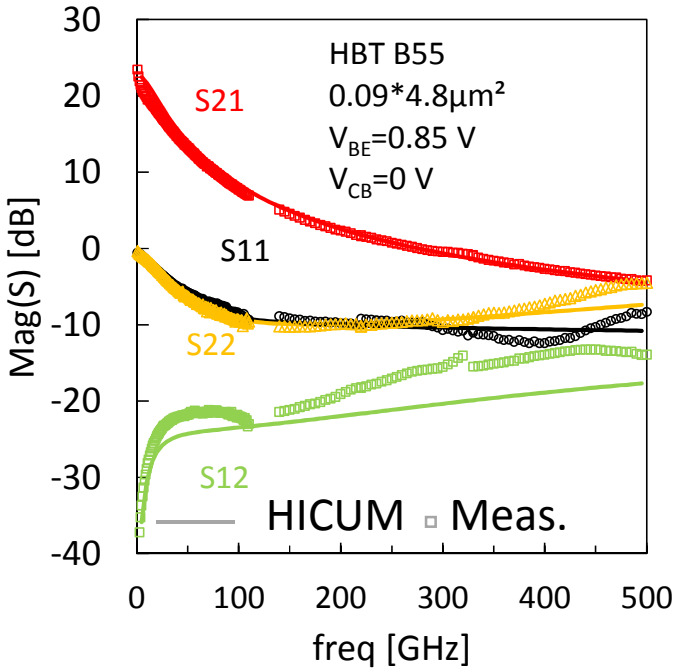
EM sim. setup

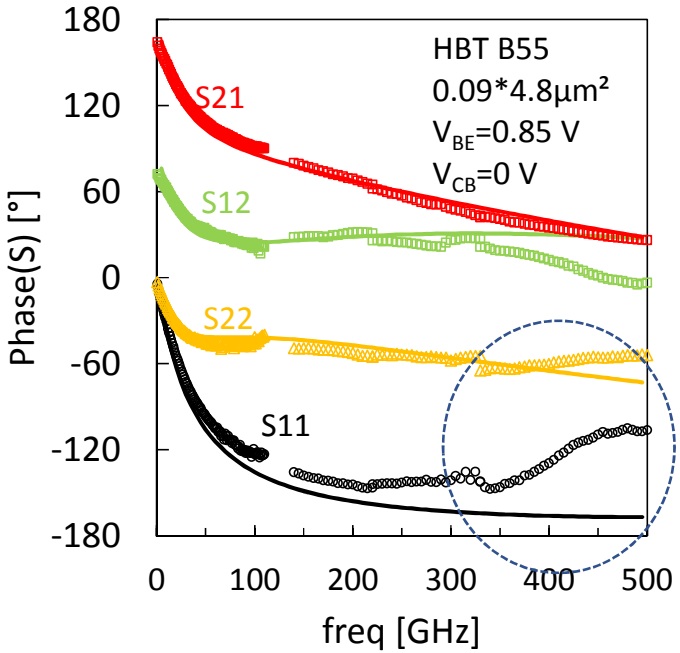
220 GHz Picoprobe model



Application to the HBT

- STMicroelectronics B55 technology
  - On wafer TRL + short-open de-embedding
  - Improved test structures (Pads layout, more space between structures, …)
  - Measurement vs HICUM compact model with substrate extension

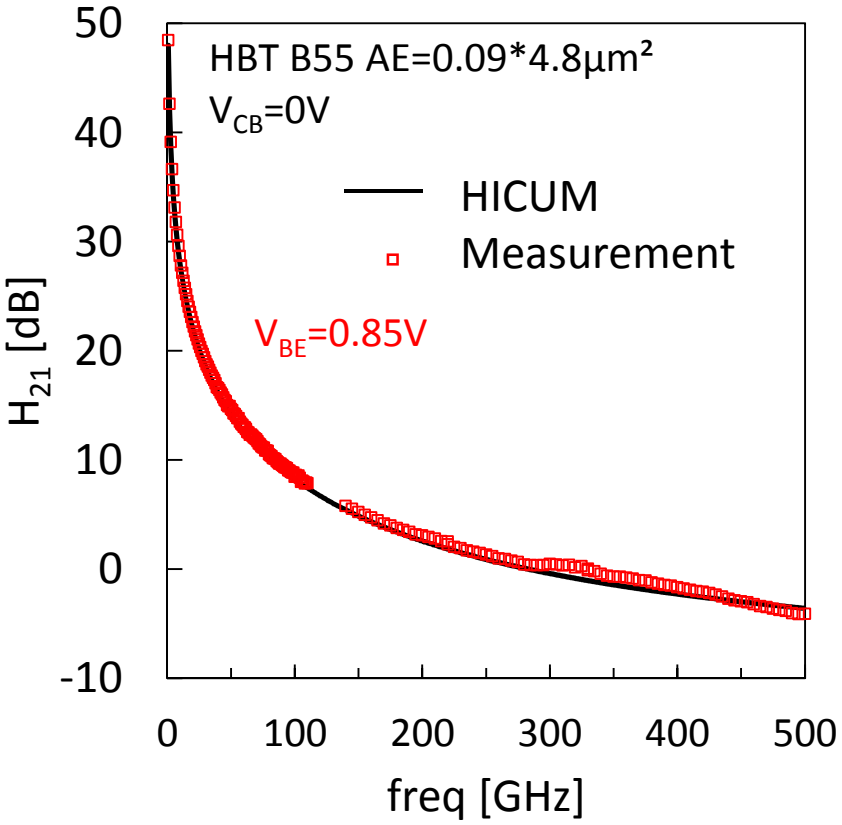


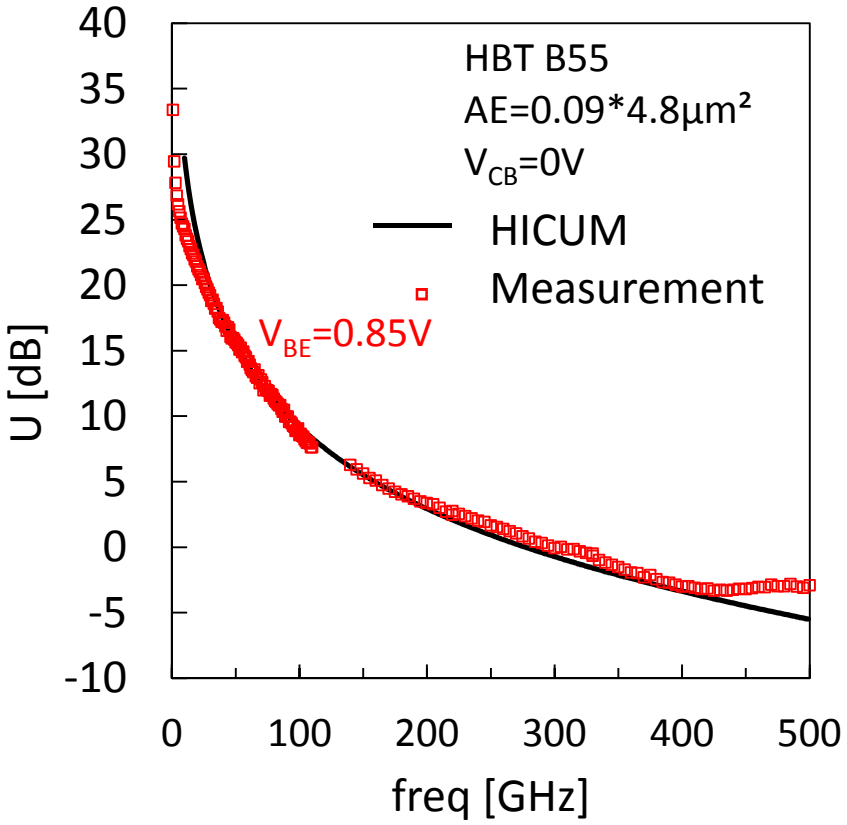


Characterisation & modelling is uncertain above 350 GHz

Application to the HBT

- STMicroelectronics B55 technology

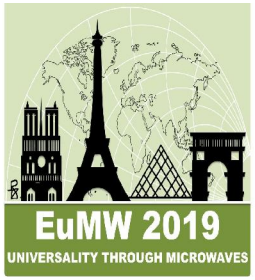




Conclusion

- The simulation methodology has been proven to be able to accurately reproduce the impact of the measurement methodology and set-up
- ISS calibration (SOLT or TRL) with OS de-embedding is not accurate above 200 GHz
- Adjacent structure have an impact on measurement results => requires optimized layout
- HBT: On wafer TRL and especially SO de-embedding => to be verified above 350 GHz

Thank you



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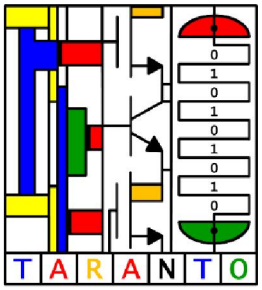

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