Single-stage PFC ac-dc converters

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Abstract *– For single-phase applications, two stage power factor correction (PFC) rectifiers are typical approach used to achieve high power factor and fast output regulation. In low power area this method is to costly. It is possible to construct a converter containing a single transistor which accomplish above mentioned functions. This paper highlights topological and design requirements of single-stage high quality rectifiers. Experimental waveforms confirm the imposed mode of operation.*

Keywords: *Switching power converters, unity power factor correction, single-stage power factor corrector*

I. INTRODUCTION

Power factor correction shapes the input current of off-line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulate a pure resistor, in which case the reactive power drawn is zero. Input current, free of harmonics, is a perfect replica of the input voltage (usually a sine wave) and in phase with it. In this case the current drawn from the mains is a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with the European Norm EN61000-3-2 which specifies the maximum amplitude of line frequency harmonics up to the 39th harmonics.

For single-phase electronic applications, typical active PFC approach (shown in Fig. 1) uses an input current shaping converter in front of a dc-dc converter. The two converters are controlled independently to achieve high quality input current shaping and fast output voltage regulation. This system is known for its superior performance, but the cost may not be justified for lower power applications. It is possible to construct a single converter [1], containing a single transistor, which performs all of the functions accomplished by the system of Fig.1.These are:

1. Input side resistor emulation i.e. the line current is proportional to the line voltage.
2. Internal low frequency energy storage. It is necessary to absorb and supply the difference between the pulsating single-phase AC instantaneous input power and the constant DC output power.
3. Regulation of load voltage is accomplished by a switching converter controlled by a feedback loop with bandwidth much greater then the second harmonic frequency.

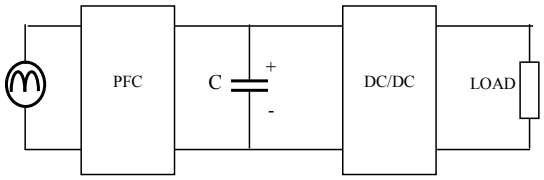


Fig. 1. Single phase power converter using a high quality rectifier, energy storage capacitor and a dc-dc converter

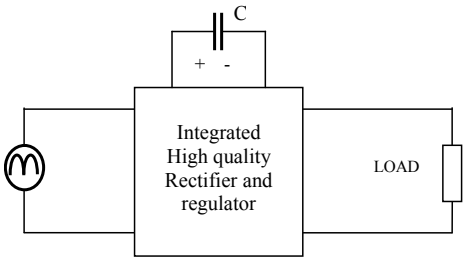


Fig. 2. *Single phase power converter using a single converter which has the integrated functions of high quality rectification, capacitive energy storage and the wide bandwidth output voltage regulation.*

II. TOPOLOGICAL REQUIREMENTS

To develop a PFC AC-DC converter which integrate the three above functions, the low frequency of the input voltage $v_g(t)$, the energy storage capacitor voltage $v_c(t)$, and the load voltage v(t) must all bee independent. To accomplish this, switching elements (high frequency switching transistors and/or diodes) must be placed between v_g, v_c and v which block the difference in the low-frequency components of these voltages.

Once the required independence of v_g, v_c and v is obtained, it is possible to cause the input line current to be proportional to the input line voltage. There are two possible ways. First, feedback can force $i_g(t) = v_g(t)/R_e$, where R_e is the emulated input resistance. Second certain converters are known to naturally emulate a resistor, without active feedback. An exemple is the flyback converter operating in discontinous mode (DCM).

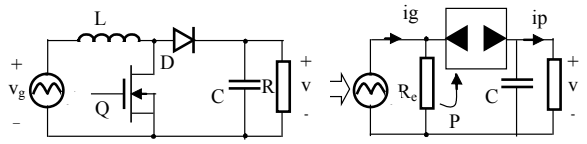


Fig. 3. Boost in DCM modeled with a loss free resistor

Another converter which naturally approximately emulates a resistor is the DCM boost converter (Fig. 3) [3]. This converter can be modeled using the lossless power processing network. The model contains an effective resistence R_e, which apparently consumes instantaneous power equal to $v_g^2(t)/R_e$. This power is transferred to the dependent power source P(t). Since this power source is a nonliniar element, the input line current contains harmonics. Yields

$$i_g(t) = \frac{v_g(t)}{R_e} + \frac{v_g^2(t)}{R_e\left(v(t) - v_g(t)\right)} \qquad (1)$$

with $R_e = 2L/D_1^2\, T_s$, D_1=duty cycle, T_s=switching period. The nonliniar power source leads to the second current term of the equation which is a nonliniar function of v_g and v, but whose zero crossings coincide. By choosing v(t) sufficiently larger then $v_g(t)$, the harmonics due to this term can bee small. Thus, low harmonics rectification is obtainable without active control of the input current.

II. DERIVATION OF TOPOLOGIES

To derivate an integrated topology, a DCM boost converter which functions naturally as a low frequency is connected to the rectified AC line. At the output of this converter is a low frequency energy storage capacitor. A conventional dc-dc topology interfaces the energy storage capacitor to the load. Both cascaded converters switch synchronously. Next, redundant switch and diode functions of the dc-dc converter and the DCM boost rectifier are integrated together in a manner which keep the operating mode DCM boost converter and the independent energy storage function of the capacitor.

A Integration of boost rectifier with a flyback converter

Let us consider integration of a DCM boost converter with a flyback dc-dc converter. To understand how this can be accomplished, let us examine the operation of the two converter system (Fig.4). Each switching period contains three intervals, since the first converter operate in DCM. Assume that switches Q_1 and Q_2 are synchronized and that the flyback converter operate in continuous conduction mode (CCM).

During the first interval, switches $Q_1$and Q_2 conduct. Diodes D_1 and D_2 do not conduct. The inductor L_1 is energized by energy storage capacitor C_1 through Q_2. Loud R receives energy only from capacitor C_2.

During the second interval, switches $Q_1$and Q_2 do not conduct. Diodes D_1 and D_2 conduct. Energy storage capacitor C_1 receives all of energy of inductor L_1 through diode D_1. Inductor L_1 is completely deenergised at the end of this interval. Coupled inductor L_2 transfers some of its energy to the load R and to filter capacitor C_2 through D_2.

The third interval is initiated when diode D_1 becomes reverse biased by the input current reaching zero. Switches Q_1, Q_2 and diode D_1 do not conduct, while D_2 conducts. Inductor L_1 remains at zero energy state. Capacitor C_1 remains at constant positive level of energy. Coupled inductor L_2 continues transfers some of its energy to the load R and to filter capacitor C_2 through diode D_2 as in the second interval.

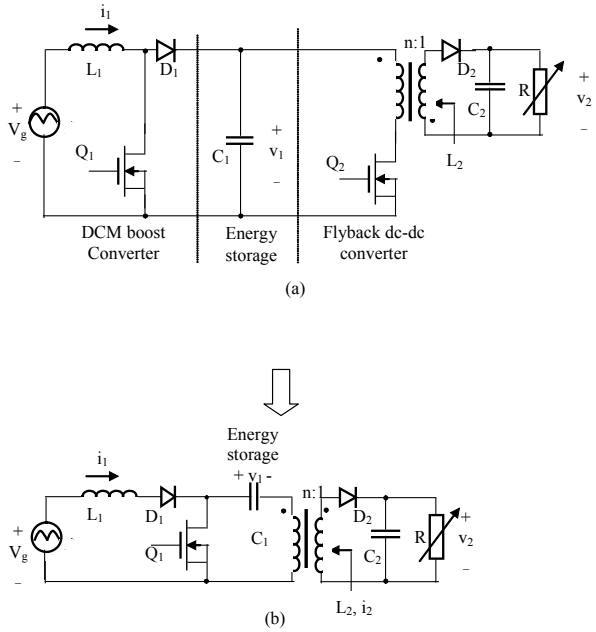


Fig. 4 Integration of boost rectifier with a flyback converter

Now combine the two converters into one converter containing a single switch. Inductor L_1 must be in series with diode D_1 in order to permit the input inductor L_1 to operate in DCM. Diode D_2 cannot be eliminated because the coupled inductor does not necessarily operate in DCM. The switch Q_2 controls the energy flow into the primary of L_2 and it aids in balancing the volt-seconds of L_2. Switch Q_2 can be replaced with a conductor by connecting the energy storage capacitor in series with it and moving switch Q_1 to the other side of diode D_1. The polarity of the primary of coupled inductor L_2 must be reversed to preserve the state of diode D_2 during each interval. The result of combining the two converters in Fig. 4 is the single stage PFC converter which is called a

Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc converter (BIBRED).

B Integration of boost rectifier with a flyback converter

Integration of a DCM boost rectifier with a buck dc-dc converter results in a Boost Integrated with a Buck Rectifier /Energy storage /Dc-dc converter (BIBRED). The synthesis procedure is similar to the procedure for BIFRED.

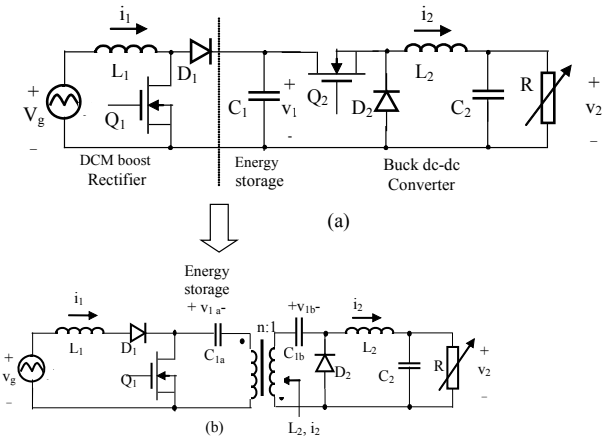
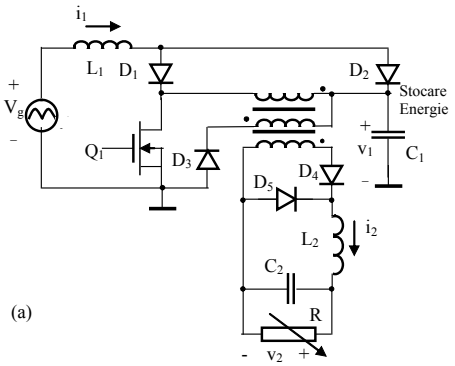


Fig. 5 Integration of a DCM boost rectifier with a buck converter

C Other BIBRED Topologies

Integration of a DCM boost rectifier with other dc-dc converters yields other topologies. Each one require the same number of active switches as in the parent dc–dc converter.

A DCM boost rectifier integrated with a single transistor forward results in a single transistor forward Boost Integrated with Buck Rectifier/Energy storage/Dc-dc (single transistor forward BIBRED Fig. 6.a)converter because the forward converter is a buck derived converter. There is a two transistor variant too. (Fig. 6.b)



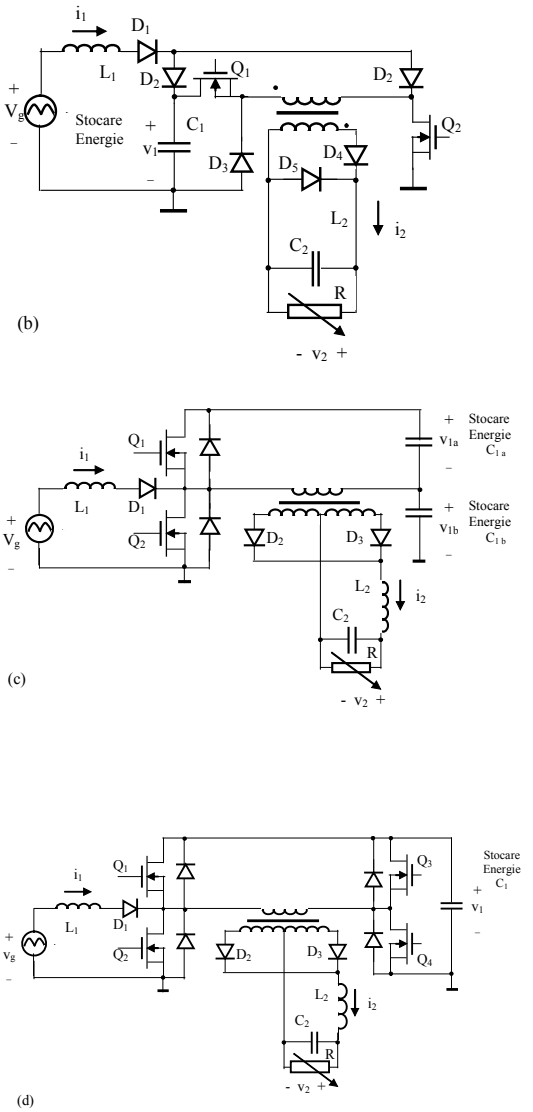


Fig. 6 BIBRED converters: (a) single transistor forward BIBRED, (a) two transistor forward BIBRED, (c) half-bridge BIBRED, (d) full-bridge BIBRED.

A DCM boost rectifier integrated with a half bridge converter results in a half bridge BIBRED. There is also a full-bridge BIBRED.

III. DESIGN REQUIREMENTS

Each topology must have an input inductor which small enough that it always energizes then completely deenergizes during a switch cycle. They must have an energy storage capacitor which is large enough to maintain a sufficient energy level when the instantaneous line voltage is near zero. The capacitor which is in parallel with the load must be large enough to filter switching ripple yet small enough to permit high performance regulation. The line filter elements must be large enough to filter switching ripple to not interfere with the natural commutation of the diode brdge. The line filter sould be placed between the diode bridge rectifier and the integrated converter.

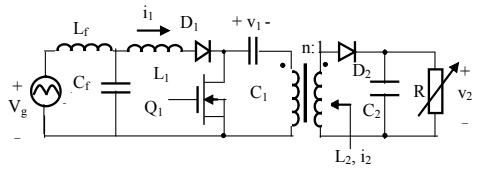


Fig. 7 Schematic of a BIFRED which includes the high frequency EMI filter

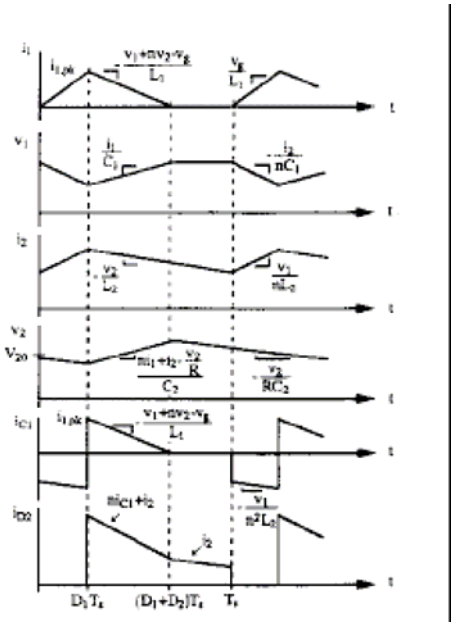


Fig. 8 Switching waveforms of currents and voltages in the BIFRED.

Averaging over one switching cycle yields large signal equations:

$$i_1 = \frac{1}{R_e}\left(v_g + \frac{v_g^2}{v_1 + nv_2 - v_g}\right) \quad (2)$$

$$C_1 v_1 = \frac{1}{R_e}\left(\frac{v_g^2}{v_1 + nv - v_g}\right) - \frac{D_1}{n} i_2 \quad (3)$$

$$L_2 i_2 = \frac{D_1}{n} v_1 - (1 - D_1) v_2 \quad (4)$$

$$C_2 v_2 = \frac{n}{R_e}\left(\frac{v_g^2}{v_1 + nv_2 - v_g}\right) + (1 - D_1) i_2 - \frac{v_2}{R} \quad (5)$$

$$\text{where } R_e = \frac{2L_1}{D_1^2 T_s} \quad (6)$$

These equations can be viewed as the node and loop equations of the non linear large signal equivalent circuit [2].

IV. EXPERIMENTAL RESULTS

Waveforms of a 40 W BIFRED (Fig. 7) with component values given in Table 1are shown in next figures .

Table 1.

parameter	value	parameter	value
L_1	359 µH	R	10 Ω
C_1	220 µF	L_f	262 µH
n	3	C_f	1µF
L_2	204 µH	T_s	20µsec
C_2	47 µF	D_{10}	0.26

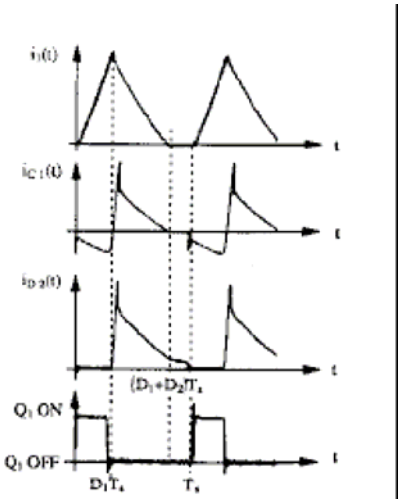


Fig. 9 Experimental switching waveforms which verify the mode of operation.

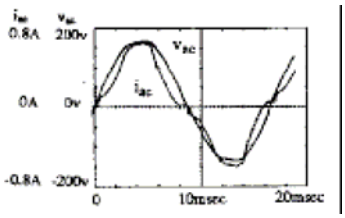


Fig. 10 Line current wave forms

V. CONCLUSIONS

These converters derived by the integration of a DCM boost converter, energy storage capacitor and a cascaded dc-dc converter are capable to perform all functions of system of Fig. 1

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