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Design and realization of a broadband single-side-band mixer with a very short settling time

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Abstract. To achieve high range resolution in synthetic aperture radar imaging a frequency synthesizer with high bandwidth is a possible solution. To operate in the required frequency band an LF-signal usually has to be upconverted. In this paper we describe the design and realization of a broadband Single-Side-Band Mixer with a very short settling time between frequency steps of arbitrary length inside a high bandwidth. Compared to already existing SSB-Mixers, our novel concept has three major advantages: At first, the mixer could be used in combination with an arbitrary signal source. Due to a modular circuit concept it is possible to use the system for different input frequency ranges. Moreover, just by changing single modules, the output frequency-range can be adapted to individual requirements. Thirdly, as a main advantage, the system is able to generate a high frequency output span with a very fast settling time between frequency steps. Even with applied steps up to 400 MHz, the settling time remains below 3 µs, which is more than 5 times faster than the settling time of similar synthesizers.

1 Introduction

A few requirements have been claimed for developing the single side band mixer: A fast frequency sweep, a high output spectrum and a high sideband supression. For synthetic radar imaging with a stepped frequency synthesizer, for example, frequency ramps have to be generated and therefore the system has to be able to switch very fast between discrete frequency steps of up to 400 MHz. Within this time the sideband suppression has to rise as much as possible. Due to a modular concept, the system could be adapted to different signal sources and various RF-frequency-ranges (Haßler, 2009).

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2 System design

There are different concepts how to convert frequency with a high sideband suppression. In Fig. 1 there is shown a fundamental circuit concept of our mixer. The signal is devided into two channels with a relative phase difference of 90°.

The signals amplitude is equalized by an AGC. Due to the requirement of a very fast settling time, the time-constant of the AGC is a fundamental criterion of choice. A broadband AGC unit is necessary to allow a high input spectrum. The output level of the AGC is compared to the setpoint and the difference converted into a current which charges an external capacitor. The voltage at the capacitance adjusts the amplification factor. The smaller the capacitance the lower the settling time but also the higher the probabilty that the system oscillates. With our system we achieve a settling time of 1 µs. The influence of the amplitude differences between the two signal paths on the sideband suppression has been evaluated using a simulation. To show the influence of amplitude differences between the two signal paths on the sideband suppression, the single sideband mixer was simulated. For this simulation, a phase difference of 90° between the I- and Q-signal was assumed. Figure 2 shows the output spectrum of the single sideband mixer during the settling time after a 400 MHz step. Figure 3 shows the output spectrum after the settling time. The different sideband suppression is obvious.

Each signal is mixed with the VCO signal, that is splitted in an inphase and a quadrature component as well. Assuming an equivalent signal level and a phase difference is 90° Fig. 4 shows the spectra of the input signals AI1 and AQ1 together with the output signal.

3 Amplitude and phase error

Referring to Fig. 1, the input signals AI1 and AQ1 can be written as

$$A_{I1}(t) = A_{I1}\cos(w_{\text{in}}t + \Delta\Phi_I) \quad (1)$$

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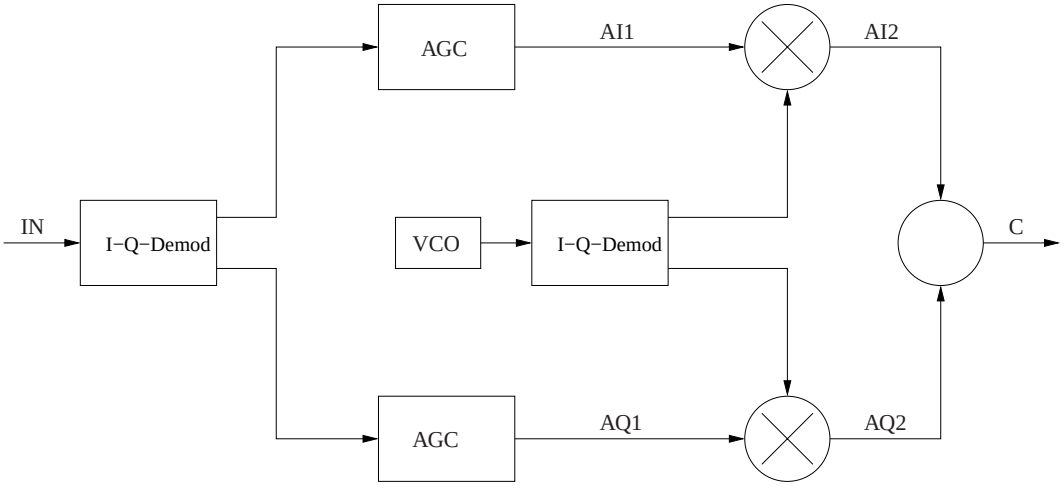

Fig. 1. Systemconcept: single sideband mixer.

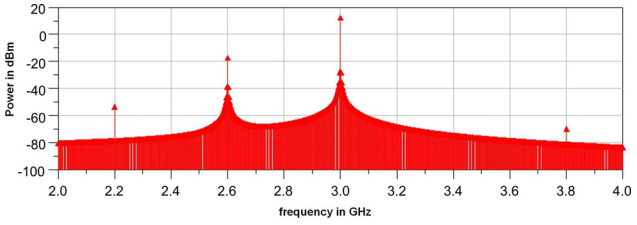

Fig. 2. Output spectrum of FFT during settling time.

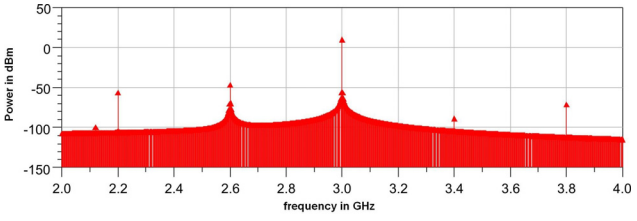

Fig. 3. Output spectrum of FFT after settling time.

and

$$A_{Q1}(t) = A_{Q1}\cos(w_{\text{in}}t + \Delta\Phi_Q). \quad (2)$$

After a few steps, the output signal

$$C(t) = A_{I1}(t) + A_{Q1}(t)$$

can be calculated for the upper and lower sideband

$$|C_{\text{USB}}| = \sqrt{a^2 - b^2} \quad (3)$$

$$|C_{\text{LSB}}| = \sqrt{a^2 + b^2} \quad (4)$$

where

$$a = \frac{A_{Q1}B_Q\sin(\Delta\Phi_Q)}{2}$$

and

$$b = \frac{A_{I1}B_I}{2} + \frac{A_{Q1}B_Q\cos(\Delta\Phi_Q)}{2}.$$

In Fig. 5 the sideband suppression is shown in dependence on the relative phase error and the amplitude deviation in both channels.

Obviously both, an amplitude and a phase deviation have a strong influence on the sideband suppression. A phase error of 3° approximately deteriotrates the signal as much as an amplitude error of about 2 dB.

4 Generation of a broad band I/Q signal

There are a variety of possibilities to generate a broadband I/Q signal. Under consideration of the requirements of a wideband input spectrum and a very fast settling time and regarding previous results of the analysis of phase- and amplitude errors, three concepts have been proven as applicable.

4.1 RC-CR phase shifter

The first possibility to generate a 90° phase difference, is an RC-CR combination. Identical resistors and capacitors assumed, this construction always provides a relative phase difference of 90°. With the transfer functions of the low- and highpass (Eqs. 5, 6) it can be shown, that the relative phase difference between this two filters remains 90° over the whole frequency range.

$$H_{\text{TP}} = \frac{1}{1 + j\omega RC} \quad (5)$$

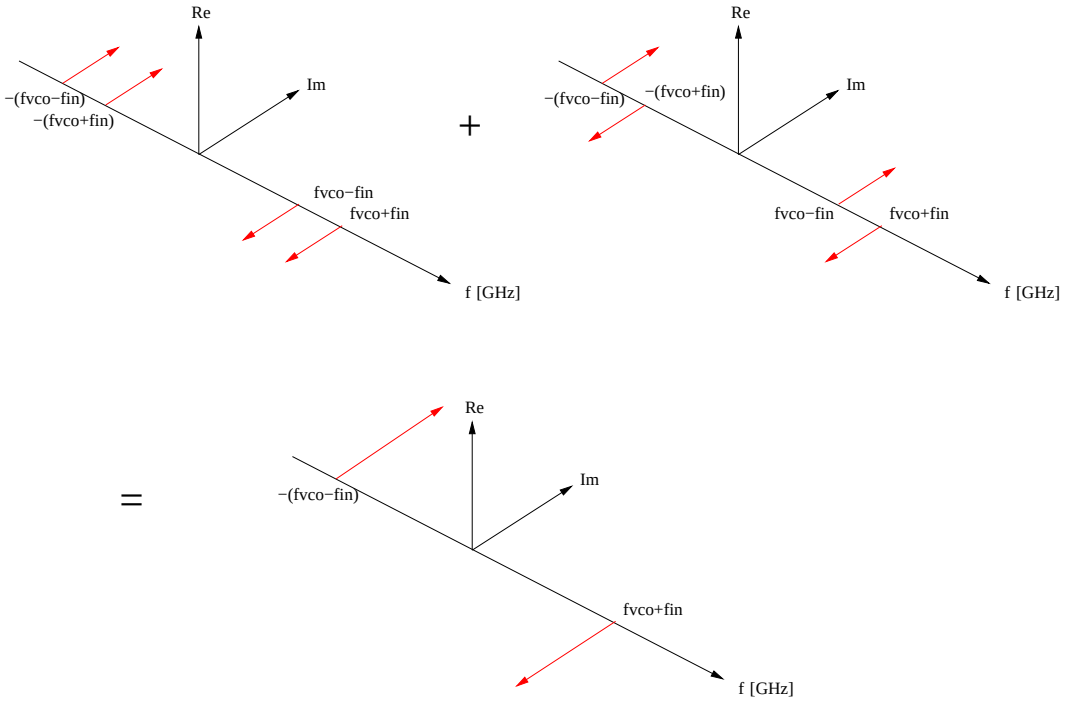

Fig. 4. Spectrum of the inphase and quadrature signals after frequency conversion.

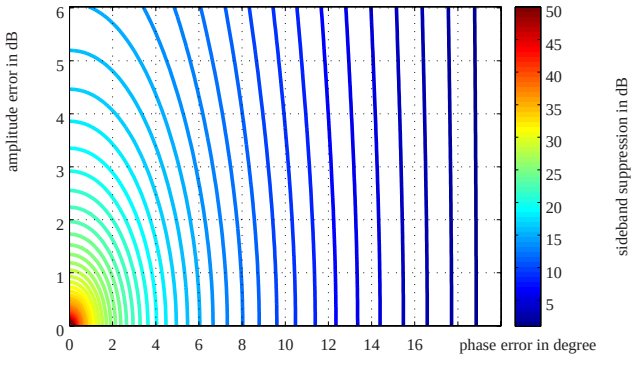

Fig. 5. Influence of phase- and amplitude errors on the side band suppression.

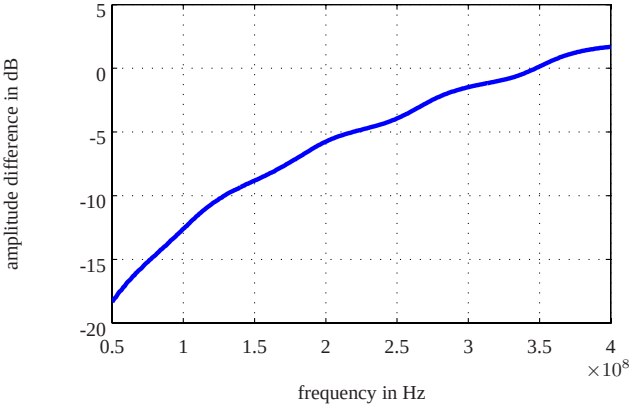

Fig. 6. Amplitude difference of I and Q channel of RC-CR element.

$$H_{\mathrm{HP}} = \frac{j\omega RC}{1 + j\omega RC} \tag{6}$$

$$\text{phase difference} = \angle H_{\mathrm{TP}} - \angle H_{\mathrm{HP}} = -\arctan(\mathrm{wRC}) - \frac{\pi}{2} + \arctan(\mathrm{wRC}) = -90^{\circ} \tag{7}$$

An issue of this type of phase shifter is the antipodal change of the amplitude levels in both signal channels. To achieve good results in sideband suppression the amplitudes of both signals have to be equal. This is done by an automatic-gain-control unit (AGC). In Fig. 6 the difference between the inphase and quadrature channel is depicted. For a frequency step from 400 MHz to 50 MHz the maximum difference is approximately 18 dB.

An increasing difference of the amplitudes causes a higher time constant of the AGC. To minimize the deterioration of the fast settling time, the amplitude influence of the phase shifter should be kept as small as possible. The phase response of this RC-CR component, which is designed for an input frequency range from 50 MHz to 400 MHz, is shown in Fig. 7.

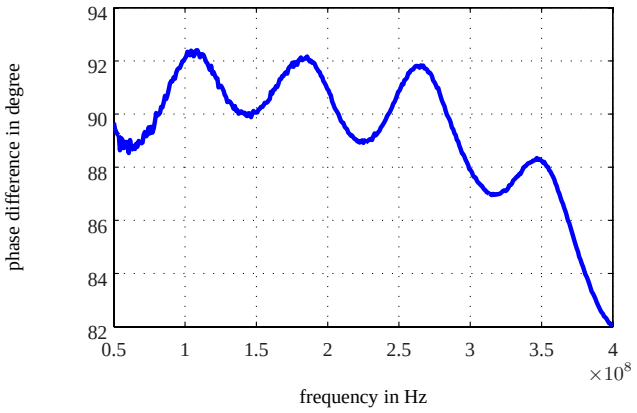

Fig. 7. Phase difference of I and Q channel of RC-CR element.

Up to a frequency of 360 MHz the phase error remains smaller than 2.5°.

4.2 Delay line phase shifter

Another concept for phase shifting is shown in Fig. 8. The generation of a 90° phase difference is realized exclusively with transducers and delay lines. Every transducer is used to split a single-ended signal into a differential signal. For mathematical description, the input signal is written vectorial.

$$\mathbf{IN}(t) = e^{j\omega t}\begin{pmatrix}\cos\varphi\\ \sin\varphi\end{pmatrix} = e^{j\omega t}\begin{pmatrix}1\\ 0\end{pmatrix} \tag{8}$$

The input phase offset can be set to zero without further restrictions and the time dependence can be ignored. Assuming that the upper output of every balun is delayed by 180° B1 and B2 can be written as

$$\mathbf{B1} = \begin{pmatrix}\cos(\varphi_{B1}=180°)\\ \sin(\varphi_{\mathrm{B1}}=180°)\end{pmatrix} = \begin{pmatrix}-1\\ 0\end{pmatrix} \tag{9}$$

$$\boldsymbol{B2} = \begin{pmatrix}\cos(\varphi_{\mathrm{B2}}=0°)\\ \sin 0(\varphi_{\mathrm{B2}}=0°)\end{pmatrix} = \begin{pmatrix}1\\ 0\end{pmatrix}. \tag{10}$$

Each signal is divided by a transducer. The signals C2 and C4 are delayed and compared to C1 and C3. To get a relative phase difference of 90° independent of frequency between the output signals Port2 and Port3, the length of the delay line can be choosen arbitrarily. The amplitude difference of the output signals increases, if the electrical length of the delay line or phase difference between C2 and C1, and as well between C4 and C3, becomes smaller. With $\Delta\Phi_{\mathrm{C2}}$ and $\Delta\Phi_{\mathrm{C4}}$ being the phase differences caused by the delay lines C2 and C4, the output signals at Port2 and Port3 can be written as:

$$|\mathbf{Port2}| = \left|\begin{pmatrix}\cos\Delta\varphi_{\mathrm{C2}}-1\\ \sin\Delta\varphi_{\mathrm{C2}}\end{pmatrix}\right| \tag{11}$$

$$|\mathbf{Port3}| = \left|\begin{pmatrix}\cos\Delta\varphi_{\mathrm{C4}}+1\\ \sin\Delta\varphi_{\mathrm{C4}}\end{pmatrix}\right| \tag{12}$$

Using the dot product (13), it can be shown that the signal vectors at the output ports are perpendicular to each other and therefore the phase difference is 90°, assumed that both delay lines cause the same phase difference.

$$\mathbf{Port2} \bullet \mathbf{Port3} = \cos^2(\Delta\varphi) - 1 + \sin^2(\Delta\varphi) \equiv 0 \tag{13}$$

The attenuation of the delay lines can be neglected and the phase difference of all balun-output-signals accounts for 180°. Due to the frequency dependence of the electrical length of the delay line (Pozar, 1998) the phase difference is

$$\Delta\varphi = \frac{360° \cdot l_{\mathrm{delay}}}{\lambda} = \frac{360° \cdot l_{\mathrm{delay}}\sqrt{\epsilon_r}\, f}{c} \tag{14}$$

Figure 9 shows the variation of the absolute amplitudes at Port2 and Port3, as well as the amplitude difference between the two output signals versus the phase delay caused by the delay lines.

To minimize the amplitude deviation of the output signals at a high frequency step it is necessary to scale the delay line. The phase delay should remain within 50° to 150° inside a frequency range of 50 MHz to 400 MHz. Considering the attenuation of the delay lines Fig.10 visualizes the result.

Measurements of the transfer coefficients S21 are shown in Figs. 11 and 12. Figure 11 shows the absolute value of S21. A frequency step of 350 MHz causes an amplitude deviation of 25 dB.

Regarding Fig. 12 the measured phase deviation is up to 15°. Compared to theory and to the RC-CR module, this component shows a poorer behavior, since a lot of small degradations are accumulated.

4.3 Active allpass as phase shifter

The third possibilty generating an I/Q signal is an active allpass filter. The absolute value of the transfer function is a constant one what in turn makes an AGC dispensable. To maintain equivalent amplitude levels in both signal paths an active allpass filter is used to get a phase difference of 90° at the output. But an allpass with a fixed capacitor generates a phase delay of 90° at merely one frequency point. So the capacitor values of the allpass have to be controlled. In our circuit this is done by a varicap. In addition the allpass in the upper signal path only adds a phase offset to the signal, while the relative phase difference between the two signal paths is generated through the allpass in the lower signal path. The phase response of an allpass is

$$\angle \mathrm{H}(jw) = -2\arctan(w\mathrm{R}C) \tag{15}$$

The required capacitor value of the varicap C_{var} can be calculated in order to get a phase delay of 90° independent of the frequency.

$$C_{\mathrm{var}} = \frac{-\left(\frac{\tan(\frac{\pi}{4})}{2\pi f R}\right) C_{\mathrm{fix}}}{\left(\frac{\tan(\frac{\pi}{4})}{2\pi f R}\right) - C_{\mathrm{fix}}} \tag{16}$$

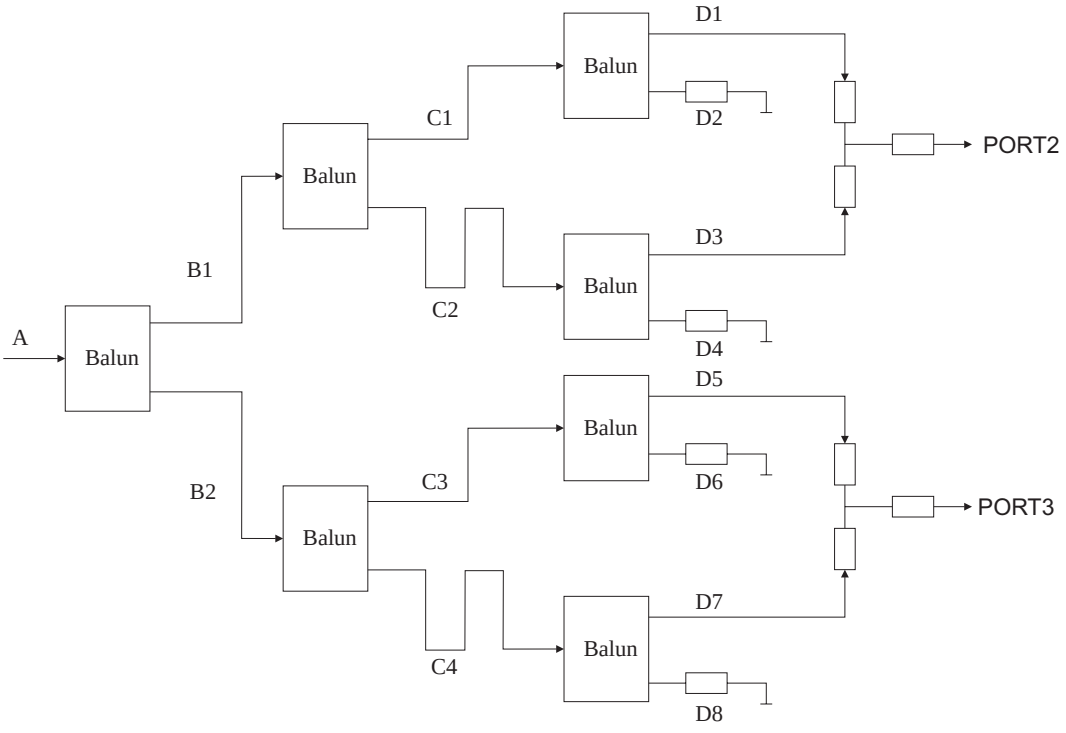

Fig. 8. Phase shifter consisting of transducers and delay lines.

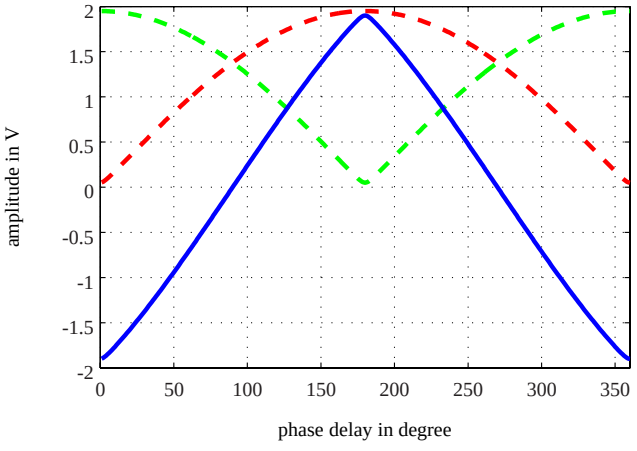

Fig. 9. Simulation of amplitude behaviour at the output of the phase shifter with delay lines, green dashed: PORT2, red dashed: PORT3, blue cont: difference.

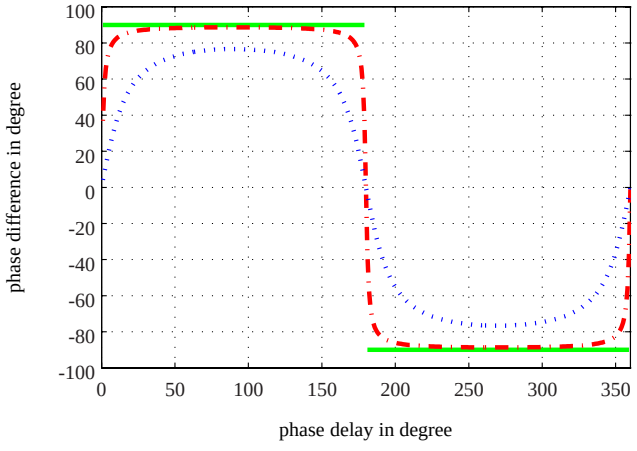

Fig. 10. Influence of attenuation of delay lines on phase difference between output signals, solid line: 0dB, dashed dotted: 0.1 dB, dotted: 1 dB.

To avoid a phase drift a closed loop control is used. The following nonlinear closed loop Eq. (17) adjusts the varicap to get a constant phase shift of 90°.

$$\Delta\varphi(C(\mathrm{U_{var}})) = \Delta\varphi(C(\mathrm{PI}(\mathrm{U_{90^\circ}} - U_{\Delta\varphi}))) \quad (17)$$

where $\mathrm{PI}(\mathrm{U_{90^\circ}} - U_{\Delta\phi})$ and $(C(U_{\mathrm{var}}))$ are the transfer functions of the PI-controller and the active allpass, respectively. The nonlinearity is a reason not to design a stand-alone solution with an allpass. But the transfer function of the allpass could be linearized if the control range of the varicap was smaller. This can be realized by a combination of an RC-CR element and an allpass. In this case the allpass only has to compensate a residual phase shift of about 5°.

Figure 13 shows the large signal schematic of the control loop. The control variable and the output variable is the same one φ_{out1}.

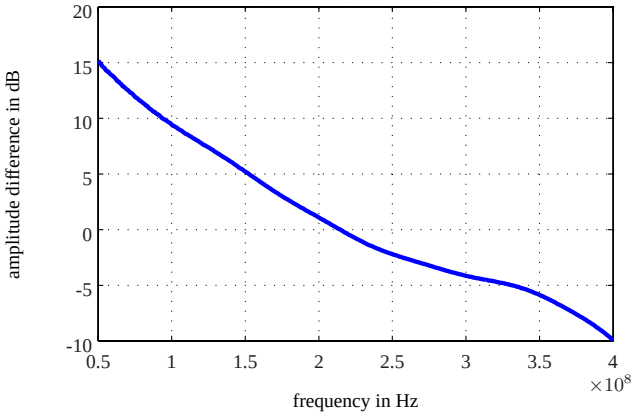

Fig. 11. Measured amplitude difference between the two output signals of the phase shifter with delay lines.

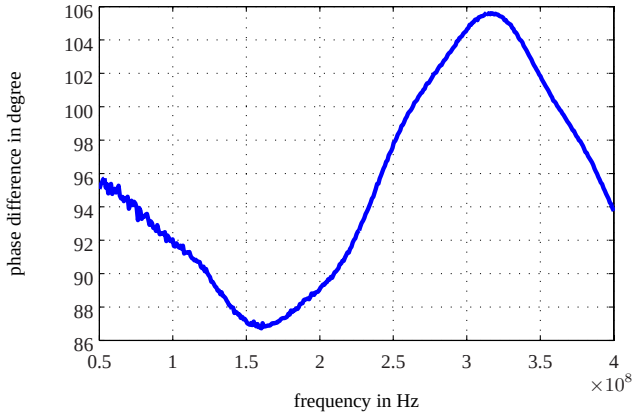

Fig. 12. Measured phase difference between the two output signals of the phase shifter with delay lines.

With an offset voltage U_{off} the operation point is adjusted. The phase delay can be written as

$$\varphi_{out1}(U_{var}, f) = \varphi_{out1}(U_{off} + PI(U_{90^\circ} - U_{\Delta\varphi}, f)). \quad (18)$$

The transfer functions of the allpass and the phase detector have to be linearized. Linearizing the allpass the input signal U_{var} can be written as

$$U_{var} = U_{var_0} + \Delta U_{var}. \quad (19)$$

The allpass transfer function differentiated with respect to ΔU_{var} yields

$$\varphi_{out1}(U_{var}, f) = \varphi_{out1}(U_{var}, f) + \varphi'_{out1}(U_{var}, f) \cdot \Delta U_{var} \quad (20)$$

in the operating point. The phase difference detected by the phase detector is

$$\begin{aligned} \Delta\varphi(U_{var}, f) = \varphi_{out1}(U_{var}, f) - \varphi_{out2}(U_{var}, f) = \\ \varphi_{out1}(U_{offset}, f) + \Delta\varphi_{out1}(\Delta U_{var}, f) \\ -\varphi_{out2}(U_{offset}, f) = \varphi'_{out1}(U_{var}, f) \cdot \Delta U_{var} \end{aligned} \quad (21)$$

Now the input signal of the PI-controller is

$$U_{err}(f) = U_{90} - U_{\Delta\varphi_{off}} - m \cdot \Delta\varphi(f), \quad (22)$$

where $m \cdot \Delta\varphi(f)$ ist the characteristic line of the phase detector. Taking into account the PI-controller the control voltage U_{var} yields

$$U_{var}(f) = \left(K_P + \frac{K_I}{s}\right) \cdot U_{err}(f) + U_{off} \quad (23)$$

where K_I and K_P are the intergrated and the proportional part of the controller, respectively. Finally the transfer function of the control loop.

$$H(s) = \frac{\Delta\varphi(f)}{W(s)} = \frac{-(K_P + \frac{K_I}{s})\varphi'_{out}(U_{off}, f)m}{1 + (K_P + \frac{K_I}{s})\varphi'_{out}(U_{off}, f)m} \quad (24)$$

where $W(s)$ is an interference signal concerning the phase difference. It is used to simulate the change of phase difference between the two channels.

5 Frequency conversion and signal superposition

For upconverting the frequency in both signal paths a mixer (Fig. 1) with a wide output spectrum and a high LO suppression was chosen. The LO consists of a VCO with a PLL. The phase difference of 90° is done by a discrete power splitter and the superposition of the signals at the output by a resistive combiner.

6 Simulation and measurements

6.1 Phase stability

The control loop was simulated in Matlab (Angermann and Beuschel, 2005). A settling time lower than 3 µs can be achieved. Figure 14 shows the control behaviour after an applied phase deviation, that is similar to a frequency step of 350 MHz at the input. The time delay to adjust the manipulated phase to 90° can be seen clearly.

6.2 Measurement of side band suppression

The setup for the measurement is as follows: The input signal is splitted by a resistive divider. For the inphase and quadrature signal generation an RC-CR filter is used followed by an AGC with a settling time below 3 µs. An allpass as described in Sect. 4.3 is resigned but could improve the results. The achievable sideband suppression is shown in Fig. 15.

7 Conclusions

We designed a broadband single side band mixer with a very short settling time. The modular setup allows simple changing. For generating an I/Q signal with high bandwidth three methods have been analyzed. An RC-CR element, a phase shifter with transducers and delay lines and finally an active allpass filter. Each individual method has its advantages but

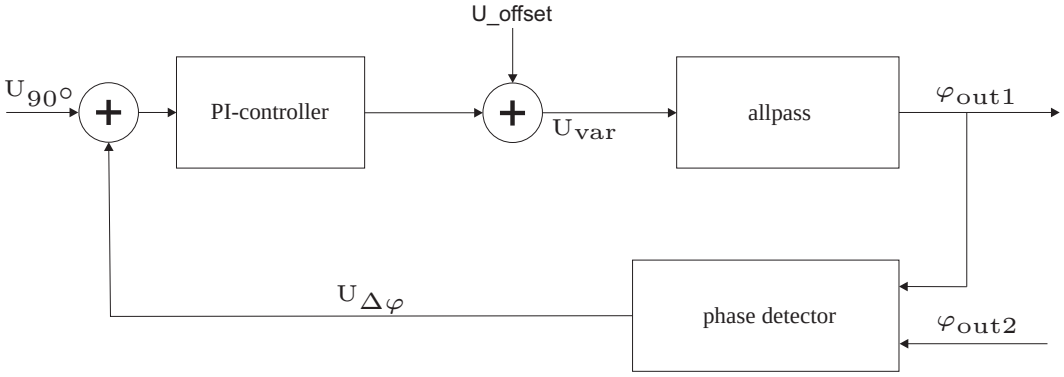

Fig. 13. Control loop of the active phase shifter.

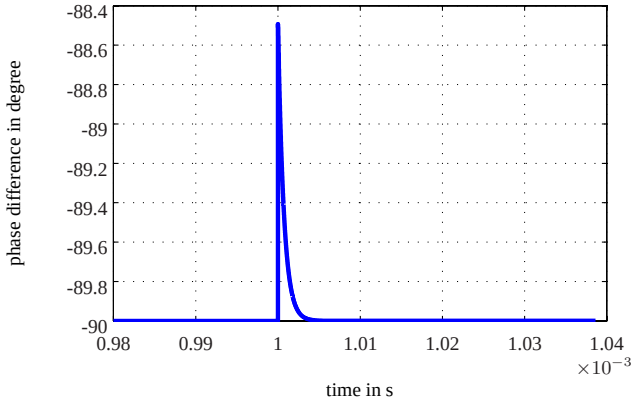

Fig. 14. Matlab/Simulink simulation of the small signal control loop.

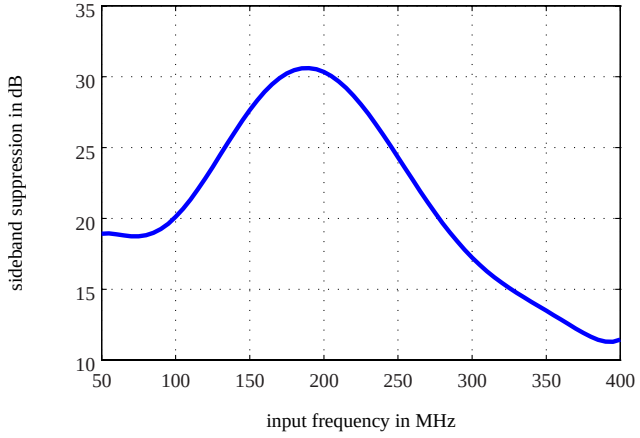

Fig. 15. Sideband suppression with VCO=2.8 GHz.

the RC-CR filter was chosen, since the phase error is best inside the required bandwidth and equalizing the amplitudes up to a difference of 18 dB can be obtained by a fast AGC. In combination with an active allpass filter the phase error could be even improved. The described combination was build up and evaluated. It is shown, that a settling time of less than 3 µs is possible within the bandwidth of 400 MHz. Hence the signal source can be used as synthsizer for stepped frequency radar and could even be used as a hopped frequency signal source.

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