Pile-Up Veto L0 Trigger System for LHCb using large FPGA's

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Abstract

A zero-level trigger system for detecting multiple events in a bunch crossing is in development at NIKHEF. The fraction of multiple events at LHCb is high; a veto on those events frees bandwidth for lowering cuts of zero-level hadronic triggers. The detection is performed by histogramming hit combinations of 2 dedicated Silicon-detector planes and selecting vertex peaks using Mgate Xilinx FPGA's. Details of the logic and implementation are presented.

I. Overview

A. Introduction

The chance of a crossing being accepted by the L0-trigger becomes higher in case of multiple interactions. Such events are more complicated to analyse offline and should therefore be eliminated from the data sample at the lowest trigger level. The fraction of multiple events at the default LHCB luminosity of $2 \cdot 10^{32} cm^{-2} s^{-1}$ and for the nominal LHCb L0 trigger is over 60%. The Pile-Up VETO system will remove events with more than 1 or 2 events per crossing, dependent on other trigger variables as well.

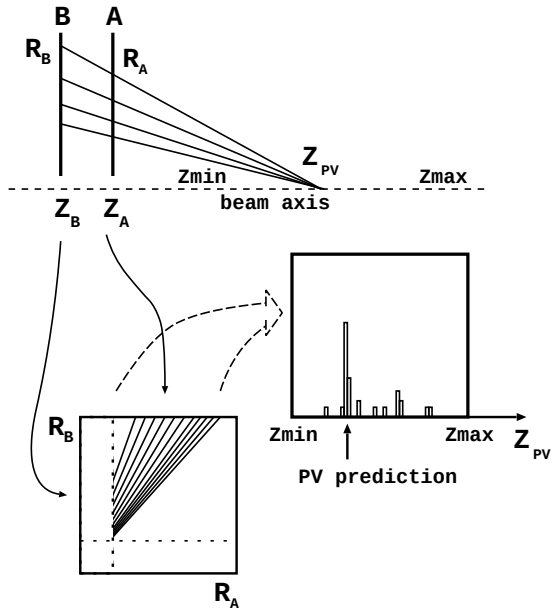

Figure 1: Basic principle of detecting the primary vertex *PV*. The readout hits of plane A and B are combined in a coincidence matrix. The resulting combinations are projected onto a z-histogram. The largest peak corresponds to the primary vertex (PV).

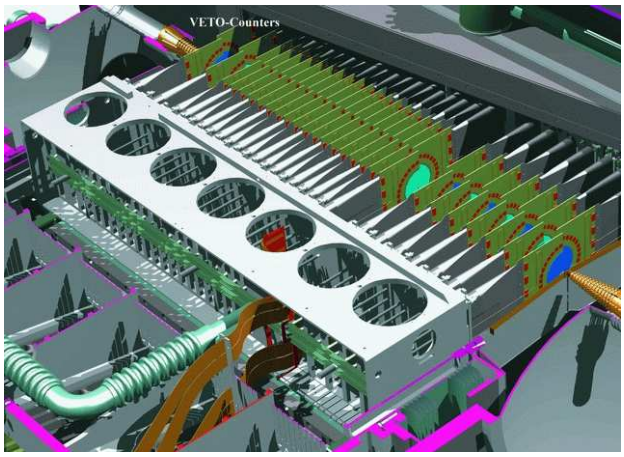

Figure 2: Layout of the Vertex tank with indicated the 2 planes of VETO detectors.

The pile-up detector consists of two planes (*A* and *B*) parallel to each other (fig. 1). Every plane consists of a wheel with 2 180° Silicon strip detectors [1]. In both planes the radii of track hits, R_A and R_B, are recorded. The hits belonging to one track have the following simple relation:

$$\frac{R_B}{R_A} = \frac{Z_B - Z_{PV}}{Z_A - Z_{PV}} = k, \qquad (1)$$

where Z_B , Z_A are the detector positions and Z_{PV} is the position of the (unknown) track origin on the beam axis (*i.e.* the primary vertex). The ratio of the two measurements, k, uniquely relates to a certain z - position along the beam axis. The equation is exact if $x = y = 0$. The resolution of Z_{PV} is limited by multiple scattering and the strip width of the detectors. The latter effect dominates.

In fig. 2 the positions of the VETO Si-detectors are shown. They are located in the backward region of the Vertex Locator (VELO) first-level trigger set-up. General infrastructure is shared by the VELO and Pile-Up VETO systems.

1) Coincidence matrix

The coincidence matrix method makes use of relation (1) in the correlation plot of R_A versus R_B. Vertex information is extracted by summing the entries in a wedge between lines of

Table 1: L0 and L1 parameters for LHCb FE electronics.

L0 Rate	1.1 MHz
L0 Readout latency	4.0 μs
L0 Subdet trigger latency	< 2.2 μs
L0 Consecutive triggers	Max. 16
L0 Derandomiser depth	16 events
L0 Derandomiser readout time	900 ns
L1 Rate	40-100 kHz
L1 buffer depth	1927
L1 Derandomiser depth	15 events

constant *k*-ratio.

The efficiency to find the vertex with the highest track multiplicity (*i.e.* with the highest correspondent peak) is close to 100%. However, there is a possibility that two interactions produce a very different number of tracks. As a consequence, the height of the two peaks in the histogram can differ considerably and the smallest one can be lower than the overall level of combinatorics.

A few additional steps are introduced to cope with this situation. First, after the largest peak is found, the combinations which contributed to this peak are searched for. Then, those hits in both stations are masked. Finally, the hits are correlated in the coincidence matrix again. Some hits from tracks having the second vertex as an origin will also be removed by masking. However, the height of the remaining vertex peak is well above the combinatorics level that is reduced as well.

An extension of the method to recognise even more vertices is under study. A variable bin size over the *z*-scale of -15 cm to +15 cm and the combination of the histograms of left and right detector halves is foreseen.

The gain in the number of *b*-events due to the removal of multiple events has been calculated to be in the order of 30% [2]. However, some events with multiple interactions but with special trigger characteristics are planned be analysed offline anyway. Moreover, the bunch crossing time is prolonged to 75 *ns* for the LHC starting period. The effects will be studied further.

II. TECHNICAL DESIGN

The overall FE L0 and L1 parameters are summarised in Table 1. Fig. 3 shows an overview of the system. The digital signals from the comparators of the 16 Beetle chips on the hybrid are buffered in the Repeater Station on the vertex tank (if necessary) and led to a LVDS to Optical Transmitter Station. Behind the shielding wall the receiver ends of the optical links are located. There the serialised data will be fanned out in parallel again. A single crate will house the Pile-Up VETO System: 2 to 4 Multiplexer Boards, 5 Vertex Finder Boards, an Output Board and a Host Board. The other output paths of the Beetle and SC connections are as described in the VELO-TDR [1]. The decision to locate the processor part behind the shielding wall was taken to avoid radiation induced effects (dose effects,

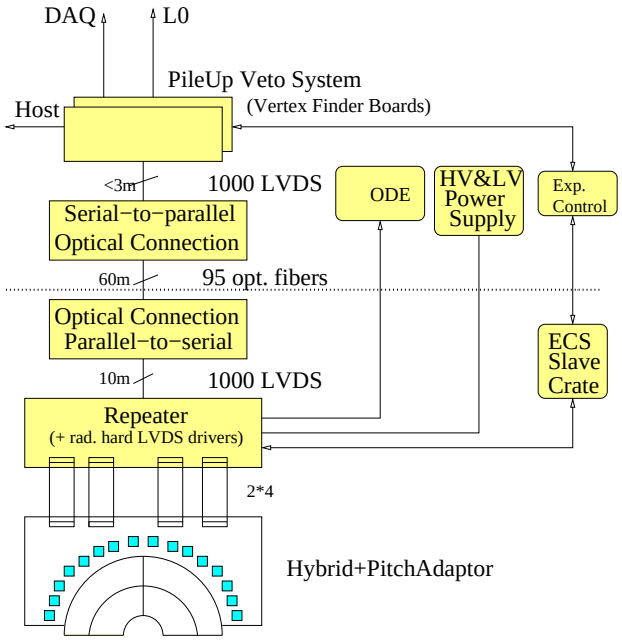

Figure 3: Overview of the Pile-Up VETO system.

Table 2: Radiation levels at several locations of the Pile-Up VETO System electronics.

Hybrid	Repeater Station	10 m off tank
200 kRad/y	20 kRad/y	$<$100 Rad/y

SEU's and SEL's) that could occur when the system would be located near the vertex tank (see Table 2).

A. *Si-detectors*

The detectors used are identical to those to be installed for the VELO system. But only R-detectors and no Phi-detectors will be installed. The strip pitch in the 90° sections of the detectors increases gradually with radius from 40μm pitch to 92 μm at a radius of 42 mm. At radii of $<$ 24.1 mm the strip length is divided in halve, giving an angular coverage of 45°. In case of a dedicated mask for the R-detector for which this division is not made, these strips are combined at detector level for the Pile-Up VETO processing. The number of VETO channels is then much lower (1024→640).

Another option is to use detectors with 45° sectors with increasing strip distances as function of R. If the strips of these sectors can be combined again on the detector into 90° sectors, this will result in a total number of output channels that decreases by a factor 2 from 1024 to 512. The number of readout chips on the hybrid decreases accordingly from 16 to 8.

In the Beetle chip 4 detector input channels are combined at the comparator stage. This implies a vertex accuracy in the order of 3-4 mm from geometrical considerations alone. The sets of detectors of both halves are displaced by 1.5 cm with respect to each other. As a consequence a correction has to be made before combining the results of both halves.

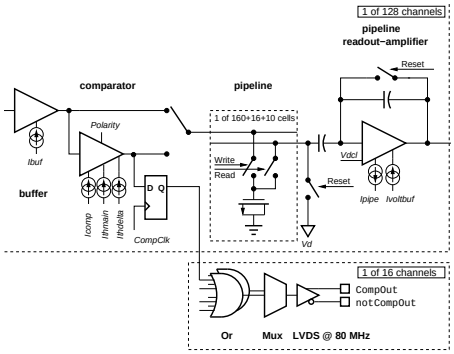

Figure 4: Beetle comparator and pipeline part.

B. *Beetle chip*

The requirements on the readout chip for the Pile-Up VETO system are less strict than for the VELO system: a S/N ratio of 6 is sufficient. The Beetle chip [3] (fig. 4) is selected because of the presence of a fast comparator output per 4 input channels to be used in the Pile-Up VETO processing. The common mode noise contribution to the signal should be small. The strip signals are also stored in the analog pipeline and can either be forwarded to the daq (ODE) in analog or binary mode by the Beetle chip.

The present Beetle chip of generation 1.1 is under test, the next generation 1.2 has an improved preamplifier part. This version has been submitted in Spring 2002. Radiation hardness has been shown for up to 40 Mrad.

C. *Hybrid design*

Compared to the VELO system [1] the number of signal paths is higher by the extra 256 LVDS signal pairs from the comparators. An 8-layer prototype hybrid has been designed (see fig. 5) and is now in production at CERN. Features of the selected kapton based technology for the hybrid are: 50 μm traces and spacing and 300 μm (micro)vias. The combination of version 1.2 Beetle chips, hybrid and R-detector will be extensively tested for crosstalk and noise.

D. *Cabling*

The output lines of the Beetle chip are LVDS conform. A careful analysis has to be made to select the correct conductor width and pitch for the cables to minimise signal loss and crosstalk. The characteristic impedance should be matched to be close to 100 Ohm.

Apart from electronic requirements other constraints for the cable concern vacuum and mechanical properties and radiation hardness. Kapton stripline has been selected as baseline option because of its good electronic properties and the folding endurance of Kapton films. Moreover, Kapton has excellent radiation properties, withstanding MRads of radiation.

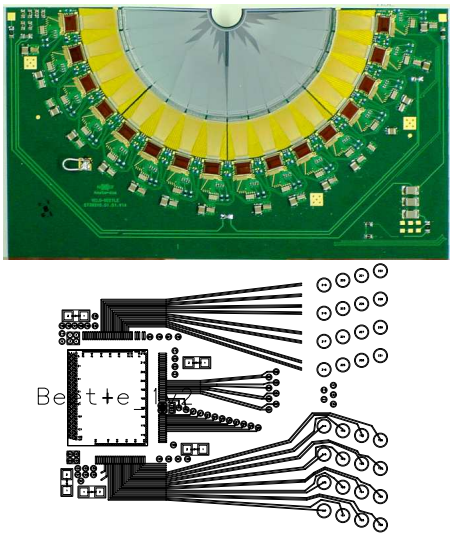

Figure 5: Beetle Velo prototype hybrid (+R-detector) as produced by NIKHEF (above) and Pile-Up VETO hybrid design detail (below).

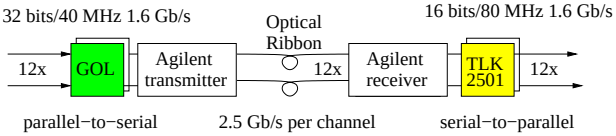

Figure 6: Optical connection.

E. *Repeater station*

If the characteristic impedance of the Kapton cable is close to 100 Ohm, the Beetle chip might be able to drive about 10 m of cable. In that case no Repeater Station modules are needed for transmitting the digital output, provided the optical transmission boards can be placed at that distance in a more or less radiation free environment (estimated rate at 10 m: $<$100 Rad/y). Otherwise the Repeater Station should contain active modules with radiation hard LVDS drivers (estimated rate: $\sim$20 kRad/y) to bridge the additional distance.

LVDS radhard drivers are commercially available [4], devices from other manufacturers will be tested for radiation hardness as well.

F. *Optical link*

As for the LHCb L0-Mu system optical transmission is seen as the baseline solution for transporting the signals to the VETO-system. Using LVDS for distances of about 60 *m* is not feasible at a rate of 80 Mbit/s without applying line equalisers. The VETO system will make use of the same technology as used for the L0-Mu system.

For the L0-Mu trigger prototype tests have been performed using a TLK2501 (16-bit, 80 MHZ) Serializer chip and Method optical transceiver module. The Method transceiver has been replaced in the meantime by an Ribbon Optical

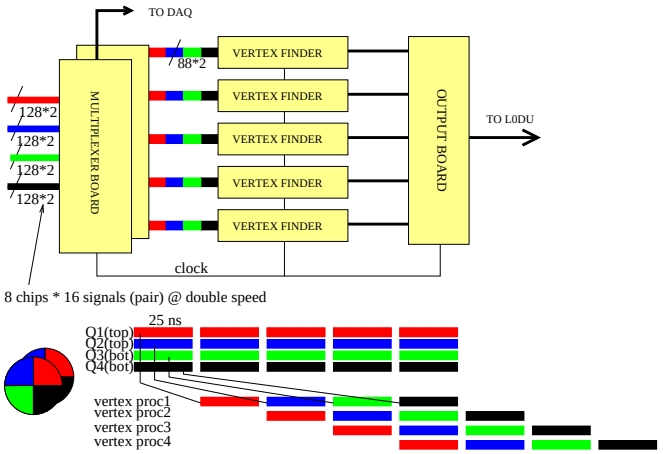

Figure 7: Pile-up veto processing, assuming 512 input signals. The process of multiplexing and serialising of the data is also indicated.

Transceiver from Agilent (see fig. 6). The measure bit error rate is negligible ($< 10^{-14}$ up to 2.5 GB/s). CMS GOL chips are planned to be used at the detector side. The synchronisation with the LHCb clock is foreseen by using a VALID pulse signalling the beginning of a LHC cycle. The effect of SEU on the system should be studied further.

G. *Architecture of the Veto processing system*

The processing of the vertex finding algorithm (fig. 7) is performed in the Vertex Finder Boards. Input data are multiplexed and serialised by the Multiplexer Boards. Processing results are de-multiplexed by the Output Board. Each Vertex Finder Board processes one event as indicated. In case of 1024 input signals the number of Multiplexer Boards will double. The Output Board interfaces the processor system to the central L0 supervisor and to central DAQ. A Host Board serves as general system interface.

Just one 9U/40 cm crate is needed for the processor system. The crate layout and the internal connections are shown in fig. 8. A standard LHCb SC host (i.e. Credit-Card PC) will be used for loading and monitoring of the system.

1) *Multiplexer*

The number of input signals is 1024 if the signals are not combined at the Si-detector level. In case detectors with combined 45° sections will be used, the number of input channels is 512. So either 8 or 4 optical ribbons will be connected to 4 or 2 Multiplexer Boards. The optical to electrical transition will be directly at the Multiplexer Board level. Each Multiplexer Board is connected to all Vertex Finder Boards via PCI-connectors/cables at the backplane. In the Multiplexer Board the data will be round-robin routed to the Vertex Finder Boards. Planned is to copy the input data also directly into memory (L0/L1 buffer) for inclusion in the DAQ chain.

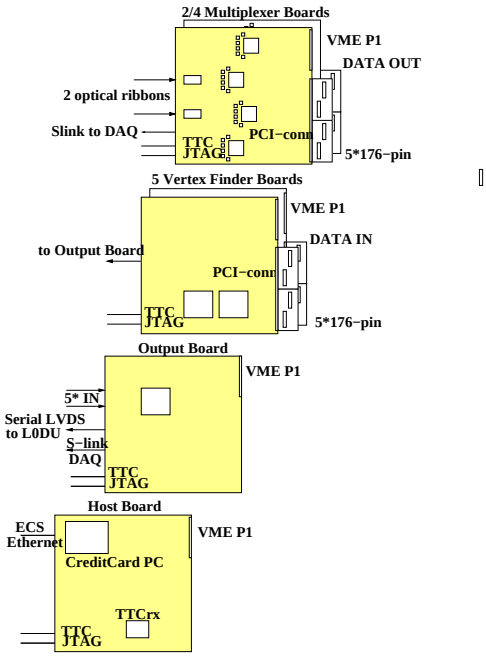

Figure 8: System crate layout and data connections.

2) *Vertex Finder*

In total 5 Vertex Finder Boards are planned to be used. Four of them handle subsequent events. The fifth one is a spare processor board that can be used for checking the results of the others. Minor configuration parameters as threshold levels should easily be adaptable. Algorithms for different beam or geometrical conditions will be pre-programmed and loaded on demand.

For the prototype development the vertex processor algorithm has been described in VHDL and, since the code is too big for just one FPGA, has been partitioned into code for several FPGA's. Xilinx FPGA's have the advantage of having many LVDS inputs and outputs. The XCV3200E is the largest at the moment of the Xilinx Virtex-E 1.8 FPGA family with 4 M system gates. In practice the device utilisation is about 70%. The number of differential input/output pairs is large: 256. Timing analysis shows that the required 40 MHz operation is feasible. The present implementation of the algorithm in the FPGA's takes 48 steps of 25 ns, close to initial predictions. Future FPGA's are expected to be even larger than the XCV3200E, giving the possibility to combine all tasks in just one FPGA.

In fig. 9 and fig. 10 the schematics of the prototype of the Vertex Finder Board (FVB) and of the Test Board are shown. All functionality of the VFB is contained in 2 XCV3200E devices. A third, smaller FPGA on the Test Board houses the logic to supply test patterns to the VFB. The test patterns are loaded via VME into the FPGA on the Test Board, that stores the patterns in memory. The left FPGA on VFB correlates the patterns of the 2 Si-wheels and searches for the highest peak in the histogram. Then the input bits related to the peak are removed from the data stream that is passed on further to the

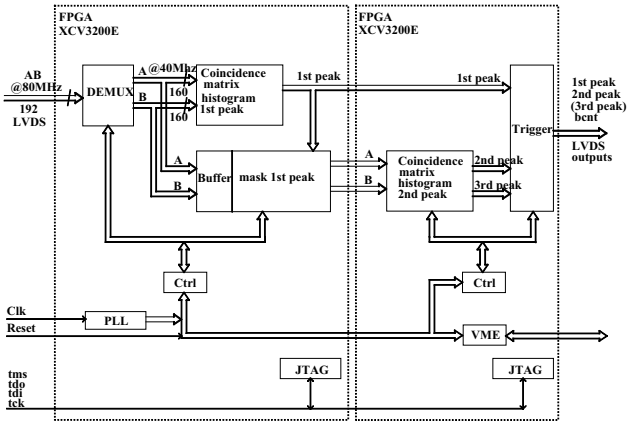

Figure 9: Prototype Vertex Finder Board diagram.

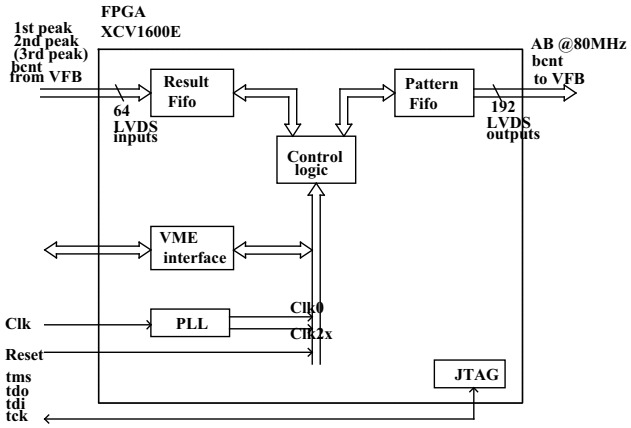

Figure 10: Test Board diagram.

right FPGA. Here second and third highest peaks are searched for. Upon receipt of a software trigger the patterns are sent to the VFB at full speed. To monitor processing in both FPGAs on VFB several registers are added to these FPGAs that capture part of the data stream. The data of those registers are shifted into the FPGA on the Test Board that in turn is read via VME.

The layout of the 12-layer PCB is complicated because of the large number of inputs/outputs. Critical parts of the layout were hand routed, the remainder by dedicated automatic routing software (fig. 11).

III. Luminosity Monitoring

For periods of in the order 5 to 60*s* the output of the Pile-UP VETO system has to be counted for the number of vertices: 0/1/2(/more). This counting is performed in the Output Board. The data will be part of the SC data stream.

IV. Conclusions

The Pile-Up VETO system, still in development, will be able to use Si-detector strip data at the lowest trigger level. The use

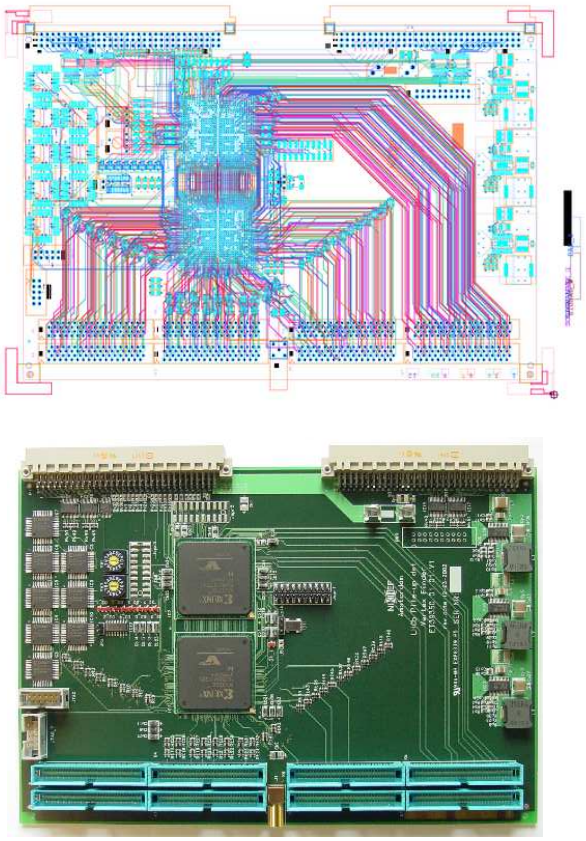

Figure 11: 6U Prototype Vertex Finder Board plus routing (above).

of large FPGA's has the advantage of flexibility in defining the trigger algorithm at the cost of routing and synthesis complexity.

References

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