Functional irradiation tests of the Atlas TileCal Digitizer using FPGA testbenches

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Abstract

The Atlas Tile calorimeter digitizer board was successfully tested on component and system levels with ionizing neutron and proton irradiation. For the functional tests FPGA test benches were developed to provide realistic run time operation during the tests. Using FPGAs on general purpose boards proved very useful when designing test systems for the TileCal Digitizer system. It made it possible to develop the test system iteratively, gradually learning how the test system and the system under test behave.

I. The TileCal Digitizer

The TileCal Digitizer [1] is responsible for digitizing analog data from about 10000 photomultiplier tubes via specially designed preamplifiers. The digitized data are stored locally awaiting validation from the ATLAS trigger. When validated, the data are formatted, buffered and transmitted to the DAQ system via an optical fiber. All the digital electronics of the digitizer boards are located in 3 separate ASICs, one general timing and control circuit (TTCrx [2]) and two specially designed ASICs, called TileDMUs [3]. The former is designed using the radiation hard DMILL process [4] while the latter used a radiation tolerant process from Chip Express [5].

The TileCal has a cylindrical geometry 11.5 m long and a diameter of 8.5 m and is made up of interleaved iron and scintillator tiles. It consists of 256 wedge shaped modules. The Digitizer is located at the base of these modules. The electronics inside the subdetector are subject to radiation. The worst case total dose of ionizing radiation is 10 kRad in 10 years and the total neutron fluence in the same time is $2.8*10^{11}/cm^2$.

II. Test systems

We needed two test systems for testing the Digitizer at full speed operation, performing typical data acquisition tasks. One was needed to test the TileDMU separately, and the second was needed to test the full system.

Two different approaches for design of test systems were considered.

1) Black box test

No knowledge of the tested system is needed.

You provide a well-defined input data stream and record the output data stream into a memory.

Run the system in the test setup, compare the output with the recorded data stream.

No detailed information about the nature of occurring errors will be provided.

2) White box test

Needs knowledge about the protocols and functionality of the system being tested.

Tests are programmed at a high level of abstraction and then successively translated to lower levels in the protocol stack.

Feed physical data to the device under test.

Processed output data in a reverse protocol stack.

Compare high level output primitives with expected output data.

Provides detailed information of errors.

We chose the White box method for the TileCal digitizer radiation tests. This method gives much better diagnostics and during the system tests we wanted as much information as possible about the occurring errors. This method, however, requires a more intelligent test system than the Black box approach. We implemented this using Xilinx FPGAs [6].

III. TILEDMU ASIC TESTS

The TileDMU, which is configured by the TTCrx ASIC, receives data from six ADCs and outputs data along two serial lines. Testing the TileDMU requires that we mimic the configuration commands sent from the TTCrx. We also have to deserialize the output and investigate the output data sequence. The output data consists of three parts; header, data and CRC checksum. The header should be the same for all events except for the event number, making it easy to check. The data are always the same. We realized that if we chose every other bit in the input data to be alternating '0's and '1's this would be a good test of the internal structure of the chip. Both header and data are protected by parity bits. The CRC field can be checked against the CRC algorithm. Eight digitizer boards were modified so that the input and output from the TileDMU could be sent via a flat cable. A small number of previously radiation tested drive and receive circuits were used. The length of the cable was sufficient to place the test bench in a protected position. Since no ADCs were mounted the ADC outputs could be patched to give suitable fixed input data patterns. A board containing a Xilinx 4013 FPGA, originally designed for another purpose, was modified to transfer signals to and from the TileDMU via the flat cable. Each error resulted in a pulse to be counted in a scaler. A user activated test mode produced different rates of false error counts to test the scalers.

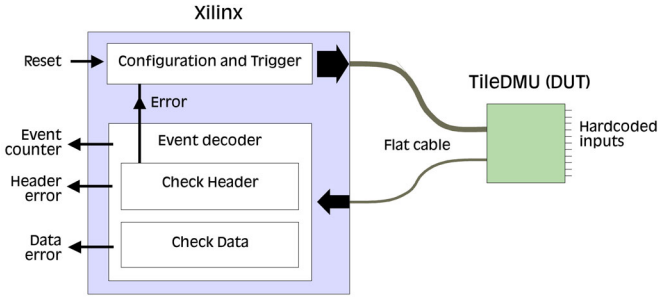

Figure 1: Block diagram of the ASIC test setup.

The Xilinx FPGA sends the necessary configuration and then checks the output for errors. (figure 1) The design gives different error reports depending on whether the error was detected in the header or in the data. If an error was detected in the header a new configuration was sent to reinitialize the TileDMUs and thus avoid multiple logging of the same error.

IV. SYSTEM TESTS

At system level the protocols become more complicated. The configuration now has to be sent serially to the TTCrx chip at 160 MHz along with the trigger commands. The test system has to contain the protocols for the TTC system in addition to the digitizer protocol itself. Since the ADCs were now present the digitizers were configured to read out a bias level in full data read-out mode at full speed (40 MHz), producing 16 samples to be read out for each first level trigger accept. Since the output from the system was identical to the output from the TileDMU itself, we could use the code developed for the TileDMU tests. Triggers were sent at a rate of about 150 kHz. This rate exceeded the maximum readout rate for the specific mode used, (~69 000 events per second) ensuring that all derandomizer buffer memories were always filled.

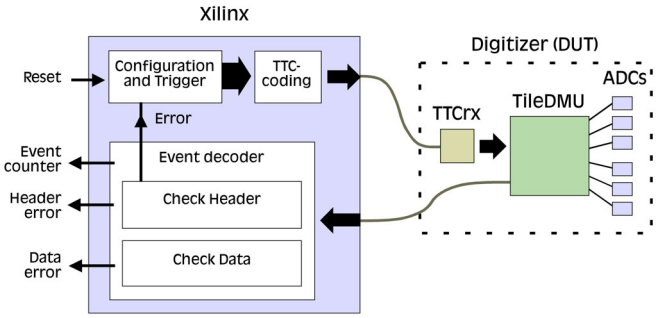

Figure 2: Block diagram of the system test setup. (pictured below)

During startup a configuration is sent to the digitizer. (figure 2) These are coded to mimic TTC-signals. After the configuration, triggers are sent. The FPGA monitors the output, checking for errors, in a similar way as for the TileDMU ASIC tests. The main difference is that the TileDMU reads ADC bias levels and if the bias level deviates more than five counts, out of the 1023 range, a data error is reported.

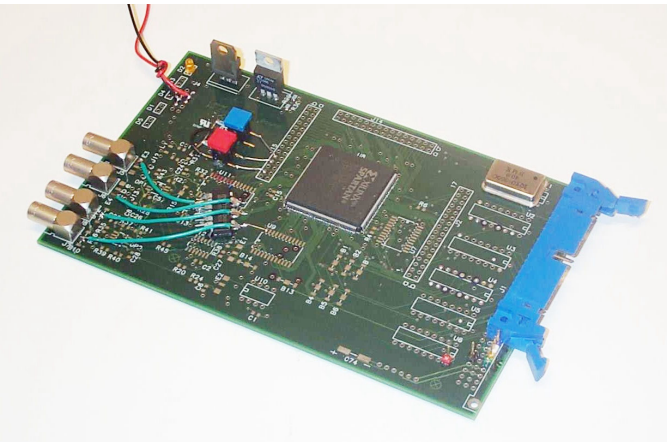

Figure 3: Test system for Digitizer system test.

For the Digitizer system tests a general-purpose circuit board with a Xilinx Spartan2 FPGA was modified to function both as a configuration and readout unit. (figure 3) This unit was attached to the digitizer via a 30 meter long twisted pair flat cable. Most of the complexity was hidden inside the FPGA.

V. RADIATION FACILITIES

ASIC tests were performed at the Karolinska Hospital in Stockholm with ionizing radiation from a cobalt therapy source, providing a dose rate of 90 Rad/min. The total dose was 10 kRad. A neutron test was also performed at the cyclotron in Debrecen, Hungary. Eight ASICs were irradiated with p+Be neutrons (Ep=18MeV). The total fluences were $5*10^{12}$ n/cm^2.

The total dose at the Karolinska Hospital was 10 kRa. Proton tests were performed at the TSL facility in Uppsala to

verify the sensitivity to single event effects. The broad 170 MeV proton beam in the Blue hall had a diameter of 75 mm, which was enough to cover the critical area of the digitizer. The proton flux of the beam was $1.1*10^8$ protons/cm^2/sec at the test position. The total fluence on the boards were 10^{10} protons/cm^2 .

A voltmeter was used to monitor the board current via a resistor to detect latch up. Typically 2 times per run (board) the data error flag started to run continuously, and the beam had to be stopped to allow a reset operation on the readout board (without cycling the power).

VI. TEST RESULTS

During the ASIC tests no errors were found. From the system test results we estimate that the total number of detectable full system digitizer data errors is 2.7±0.1 per ATLAS minute and the number of header errors is 3.9±0.3 per ATLAS hour. These numbers do not take into account the occasional, stepwise increase in the error rate that we observed. These errors were all stopped by a system reset.

We have interpreted the header errors as soft single event upsets (SEU) in the TileDMUs. We estimate that the present test system will record all single event errors in 58% of the memory area and about 95% of those in the logic area. During normal operation the corresponding numbers are 39% and 100%. This means that the test conditions are slightly more severe than those of normal operating conditions (100kHz trigger rate, 6 samples and normal mode readout).

The data errors were interpreted as radiation induced pedestal noise. Arguments for this are that the rate proved sensitive to the bias deviation range allowed. Reducing the bias deviation range from 5 counts to 3 increased the error rate by a factor of two. Furthermore, the data errors were seldom associated with header errors that indicate a TileDMU malfunction. Some of the uncontrolled spells of data errors were attributed to soft single effect events in the DACs that define the analog input levels. This meant that the pedestal setting changed, putting all data outside the limits. Other data error runs could depend on that the test controller, although fairly well shielded, suffered a radiation-induced malfunction. It could also, but less likely, be due to digitizer malfunction. This may in the worst case occur about twice during the ATLAS lifetime for each board. The fact that the operation resumed with normal error rates after a reset supports this interpretation.

The resolution of the current measuring system was about 5mA. No sudden jumps indicating possible latch-ups were observed. However, there was a slow increase in the current consumption up to about 3% (corresponding to about 15 mA) during the entire test period.

VII. CONCLUSIONS

Using FPGAs in test systems gives a good flexibility when developing the tests. It makes it possible to upgrade the tests without much hardware modification, provided that the test board is sufficiently general. With better planning, it would have been possible to produce only one test system for both ASIC and system tests, as the later test system could be adapted for both tasks using a different FPGA configuration.

VIII. ACKNOWLEDGEMENTS

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