Overview of the new CMS electromagnetic calorimeter electronics.

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Abstract

Since the publication of the CMS ECAL Technical Design Report end of 1997 the ECAL electronics has experienced a major revision in 2002. Extensive use of radiation hard technology digital electronics in the front-end allows simplifying the Off-Detector electronics.

The new ECAL electronics system is described with emphasis on the Off-Detector sub-system.

I. THE ECAL ELECTRONICS IN THE TECHNICAL DESIGN REPORT

In the CMS electromagnetic calorimeter Technical Design Report the principle of maximal flexibility for the ECAL electronics system was adopted.

The CMS electromagnetic calorimeter is a very high resolution calorimeter made of 80000 lead tungstate crystals. Each crystal signal generated by an APD is amplified, sampled and digitized with an ADC working at 40 MHz frequency. The adopted solution for the TDR was to process digitally all signals in the Off-Detector electronics sub-system located outside the CMS cavern. This principle translated in a system sub-divided into two distinct sub-systems namely:

- a Very Front-End electronics, mainly analogue, with a multi gain amplifier and an ADC designed in radiation hard technology connected to each crystal equipped with an APD. The digital signal was converted to serial optical signal.

- an Off-Detector electronics mainly developed in digital electronics making use of FPGA circuits located outside the CMS cavern.

The two sub-systems were connected with 80000 serial optical links working at 0.800 Gbits/s.

The Off-Detector electronics was designed to receive this huge amount of digital data and to subsequently store and process them during the L1 latency of 3 microseconds. The designed sub-system had 60 crates with more than 1000 boards.

I. THE NEW ARCHITECTURE

In 2002 the ECAL electronics system was reviewed and a new architecture making use of new radiation hard electronics inside the detector volume was adopted. In this schema, digitized data are locally stored in memories and processed during the L1 latency. Only data corresponding to the L1 accepted events are readout by the Off-Detector system allowing for a substantial reduction in complexity of this sub-system. The interface with the Trigger system is also greatly simplified in this new architecture which is less than 220 boards in total.

A block diagram of this new architecture is shown in Figure 1. The Front-End electronics is presented in chapter III while the components of the Off-Detector electronics are described in chapter IV.

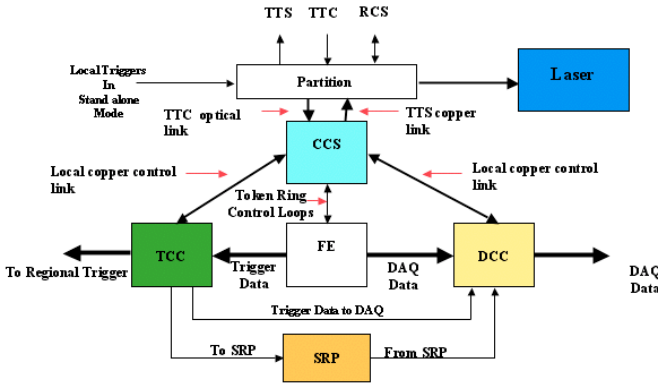

Figure 1: Block diagram of the new ECAL Electronics

I. THE FRONT-END ELECTRONICS

The Front-End electronics performs the following functions:

a) reception of the digital signals from the Very-Front electronics, ie 16 bits delivered at 40 MHz. These 16 bits contain 12 bits from the sampling ADC and 2 bits encoding the gain used by the amplifier stage

a) storage the data during the L1 latency

a) generation of the Trigger Primitive

a) formatting and transmission of the data to the DCC for each L1 accept signal

a) transmission of the Trigger Primitives to the TCC with a 40 MHz clock

The Front-End electronics will mainly sit on Front-End boards serving 25 crystals each. A possible implementation of the Front-End board is shown in Figure 2 in the case of the barrel.

The 25 digital signals generated by the Very-Front-End electronics are distributed to the FE board via connectors labelled VFE.x (with x from 1 to 5). Each signal is transmitted from the VFE at 40 MHz. These input signals are distributed to 5 FENIX circuits (Strip Fenix in the figure). Two additional FENIX chips, TCP Fenix and DAQ Fenix are fed by the output signals (16-bit each) from the 5 Strip FENIX circuits.

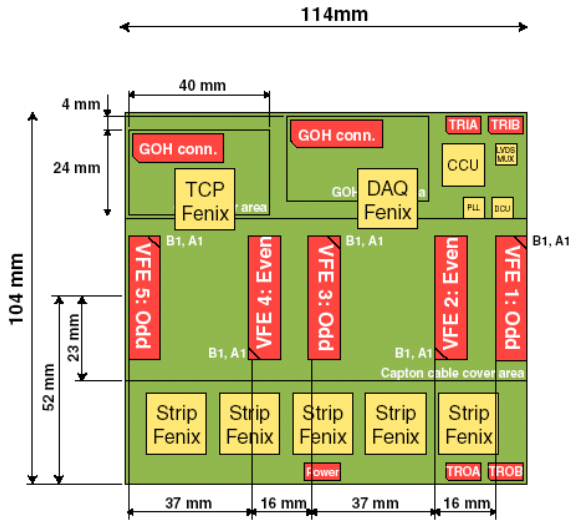

Figure 1: The Front-End Board (barrel implementation)

The DAQ Fenix sends the crystals data to the DCC after reception of a L1 signal accept. A Giga Optical Link circuit (GOL) is responsible for this transmission The TCP Fenix sends the Trigger Primitives to the TCC boards via a second GOL chip.

The FENIX chip[1], sitting on the Front-End board has 5 input 16-bit buses working at 40 MHz and two outputs 16-bit buses.

The FENIX chip has four operation modes:

a) STRIP operation mode whose purpose is to create the strips (5 crystals aligned along the phi direction) signals in the barrel) or the pseudo-strips (groups of 5 crystals with any shape) signals in the endcap.

a) TCP operation mode whose purpose is to compute the Trigger Primitives for a trigger tower (5 strips) in the barrel case

a) DAQ operation mode whose purpose is the storage of the crystals data from a trigger tower in the barrel or a supercrystal (5 pseudo-strips) in the endcap

a) MEM operation mode whose purpose is to perform the readout of the laser monitoring data

The trigger path of the FENIX chip when it is operating in STRIP mode is shown in Figure 3. Figure 4 shows the trigger path in the FENIX running under the TCP operation mode.

Under both operation mode the FENIX performs the computations used in the Trigger Primitives Generation in pipeline mode. The following computational stages are performed in the FENIX STRIP mode:

a) LIN: transforms the non-linear input scale generated by the VFE into a linear transverse energy scale taking into account the calibration factor for each channel

a) ETSTRIP: adds the five inputs

a) AMPLITUDE FILTER and PEAK FINDER: perform together the Bunch Crossing IDentification . The AMPLITUDE FILTER is a 5-tap FIR filter and the PEAK FINDER is a 3-point peak detector.

a) FORMAT: conditions the output of the amplitude filter by the detected peak found in the PEAK FINDER

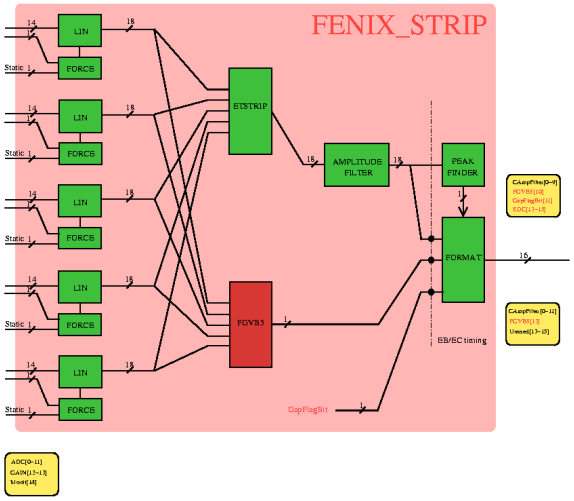

Figure 1:The FENIX chip in STRIP operation mode (only the trigger path is shown)

In the case of the TCP operation mode, only used in the barrel case, the FENIX circuit has the following pipeline stages:

a) ETTOT: computes the total transverse energy of the trigger tower

a) MAXof2 and FGVB(EB): perform together the extraction of the Fine Grain Veto Bit

a) FORMAT: encodes the total transverse energy and the fine grain veto bit in a single word

The FENIX chip will be founded in 0.25 □m CMOS technology in order to resist to the high level of radiation in which the Front-End board is working.

The VHDL description of the FENIX chip has been already downloaded to a field programmable gate array circuit, the XC2V1000 from Xilinx company.

Preliminary simulations, performed in the FPGA version of the FENIX chip, show that the computations of the Trigger Primitives, as done in the pipeline chain formed by the FENIX STRIP and FENIX TCP take 225 ns, i.e 9 cycles of the LHC clock.

In order to fulfil the specifications the ASIC version of the FENIX chip this latency should be decreased to 8 clock cycles.

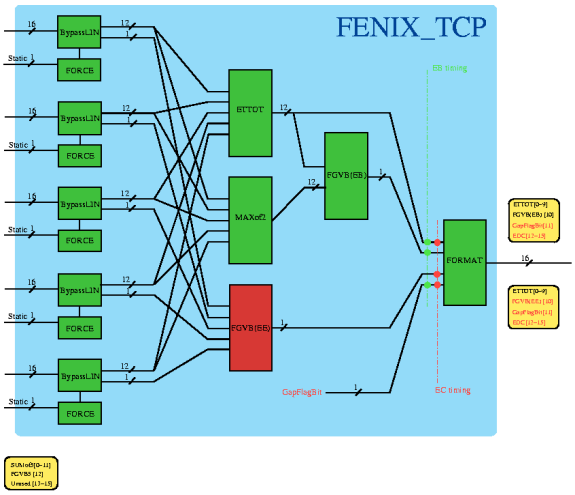

Figure 2: The FENIX chip in TCP operation mode (only the trigger path is shown)

II. The Off-Detector Electronics

The Off-Detector electronics [2] is composed of several types of boards:

a) Clock and Control System

b) Data Concentrator Cards

c) Trigger Concentrator Cards

d) Selective Readout Processor

which are described in the following chapters.

A. *The Clock and Control System*

The CCS is the central body of the 0ff-Detector electronics. It receives the control signals as well as the LHC clock from the Trigger and Time Control (TTC) system and the Trigger Throttling System (TTS) and sends it back to the Trigger Concentrator Cards and to the Data Concentrator Cards.

It also performs the setting-up of the Front-End via optical control loops.

The CCS functions are:

a) optical to electrical conversion of the TTC fibre received from the TTC optical fan-out

b) decoding of the TTC signal for extraction of the LHC clock and the command signals

c) reception of the TTS signals transmitted by the DCC and TCC. After collecting these signals the CCS sends it to the TTS

d) setting-up of the Front-End boards via a network of optical fibres.

B. *The Data Concentrator Card*

The DCC is a common collection point for crystal data transmitted from up to 68 Front-End boards and for trigger data transmitted from up to 5 TCC modules after level 1 accept trigger signal.

The DCC is also responsible for reading data from two monitoring channels.

The DCC functions are:

a) optical to electrical conversion and deserialisation of the serial input streams

b) verification of the integrity of the input event fragments

c) reduction of the data volume using a combination of crystal zero suppression and tower selective readout

d) formatting of DCC events

e) transmission of DCC events to the global DAQ through the standard DAQ link

f) transmission of the monitoring events and spying events to the local DAQ

The DCC accepts several types of events: physics events and monitoring events (laser, monitoring test pulse, leakage current and temperature measurements).

The DCC is designed to accept a total of 38.1 kBytes for input crystal event size and 156 bytes (barrel) and 300 bytes (endcap) for input TCC event.

The average output data rate to the global DAQ is 200 Mbytes/s with a maximum peak output data of 528 Mbytes/s. The DCC is designed to store a maximum of 32 events.

The DCC verifies the integrity of the input data by performing various checks. It implements mechanisms for protecting memories from overflows and signals conditions of overflows to the TTS system via the CCS.

The data reduction can be set up, following two readout modes: Forced Readout or Selective Readout. In Forced Readout mode the DCC selects the readout region of ECAL using a programmable map defined by conditions set without regard to the current event. In the contrary, the Selective Readout mode the readout is determined dynamically by the Selective Readout Processor. Three cases are considered: read all crystals, read crystals above zero suppression threshold, do not read crystal data.

The zero suppression is based on the estimation of the crystal energy performed by a 10-tap FIR filter. The filter coefficients are programmable individually per crystal.

The DCC is implemented in a VME9U board. The DCC diagram is shown in Figure.

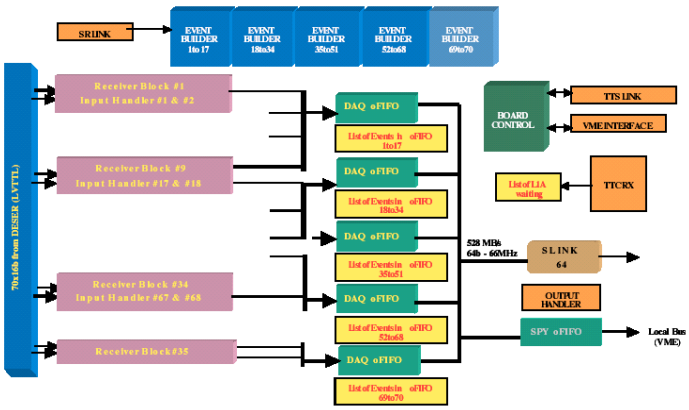

Figure 3: The DCC block diagram

The 68 optical links from the Front-End boards and the 2 additional optical links from the monitoring are shown in this figure.

After optical to electrical conversion and deserialisation into 16-bit words input data enter the Receiver Blocks (one for two channels) The Receiver Block performs link and data integrity checks, data suppression and event storage with input iFIFOs.

The Event Builder Blocks are responsible to move event fragments from the iFIFOs into the output oFIFOs. Data in the oFIFOs is transmitted to DAQ through the S-Link 64 at a maximum rate of 528 Mbytes/s.

C. *The Trigger Concentrator Card and Synchronization and Link Board*

The TCC collects data transmitted from 68 Front-End boards in the barrel and up to 48 Front-End boards in the endcap. This corresponds to 68 trigger towers signals in the barrel and up to 48 pseudo-strips signals in the endcap. The TCC is also responsible to generate the classification of trigger towers for the Selective Readout Processor.

The TCC functions are:

a) optical to electrical conversion and deserialisation of the input data streams

b) geometrical mapping between the pseudo-strips and the trigger towers in the endcap

c) finalization of the trigger primitives generation in the endcap

d) encoding of the trigger primitives using a non-linear scale for the total transverse energy deposited in the trigger tower

e) time alignment and transmission of the encoded trigger primitives to the Regional Trigger system

f) classification of each trigger tower into high, medium or low interest for the Selective Readout

g) storage of the encoded trigger primitives during the L1 latency

h) transmission of the TCC events to the DCC

In the endcap the TCC receives signals from the pseudo-strips. Depending on the endcap region covered by the TCC under consideration the trigger towers signals are build using different groups of pseudo-strips signals.

In order to avoid the design of several types of TCC a single routing has been designed allowing the distribution of the relevant pseudo-strips signals to four processing units. These processing units will be programmed in such a way that they will combine the pseudo-strips signals to form the trigger towers signals.

The TCC is implemented on a VME9U board. The block diagram for the endcap design is shown in Figure 6.

After optical to electrical conversion and deserialisation into 16-bit words the 48 (68 in the barrel case) input data enter 4 Processing Units (6 in the barrel case). These units are responsible for the finalisation of the trigger primitives in the endcap. For both barrel and endcap versions the TCC encodes the total transverse energy in a non-linear scale and classifies the trigger towers in three categories depending on the total transverse energy. The Processing Units stores the encoded trigger primitive during the L1 latency for subsequent reading by the DCC.

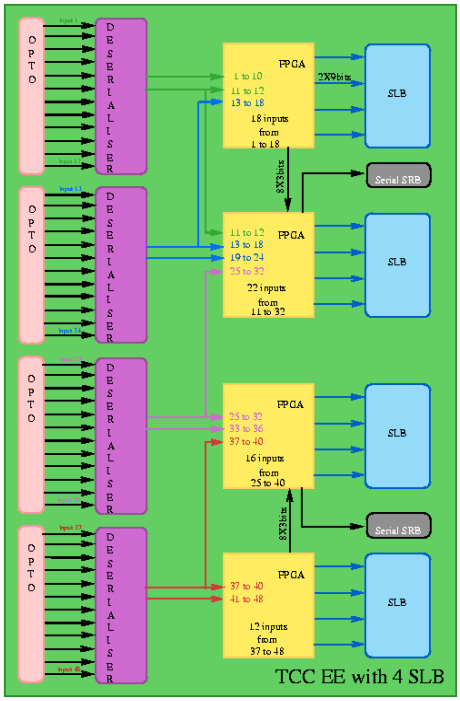

Figure 4: The TCC block diagram (endcap)

The encoded trigger primitives (8 bits for the non-linear representation of the total transverse energy plus 1 bit for the fine grain veto) are time aligned and sent to the Regional Trigger by a dedicated daughter board, the Synchronisation and Link Board (SLB in Figure 6). Each SLB handles a maximum of 8 encoded trigger primitives. It formats the 8 corresponding words in order to be sent via a single Vitesse 7216 chip with a 2 Gbits/s capacity connected to the Regional Trigger system by a copper link.

As one can anticipate, the high number of input and output signals will highly influence the implementation of the TCC either for the endcap or barrel case.

III. SUMMARY

The new ECAL electronics architecture has been presented. This architecture has exactly the same functionality as described in the Technical Design Report of the ECAL but with a substantial reduction (40%) in the estimated cost.

The newly introduced Front-End electronics essentially rely on the design of a new radiation hard circuit, the FENIX chip. The design of this chip in 0.25 μm CMOS technology is already started. Submission of this design is expected to take place end of 2002.

The flexibility principle, which was adopted in the Technical Design Report, has been abandoned. This allows the new architecture to use a reduced number of optical data links for data exchange between the on and off-detector electronics.

This also permits to design a more compact, more simple and less expensive Off-Detector electronics. The design of the Off-Detector electronics has recently started and production of the corresponding electronics modules is foreseen to start beginning of year 2004.

IV. REFERENCES

[1]http://mhansen.home.cern.ch/mhansen/Cms/Cms_ecal/Documentation/Fenix/Fenix.html

[2]http://cmsdoc.cern.ch/~jlfaure/OD_Web_Folder/Page_web.html