ATLAS Tile Calorimeter Interface

K. Anderson, A. Gupta, J. Pilcher, H. Sanders, F. Tang, R. Teuscher, H. Wu
The University of Chicago

ABSTRACT

This paper describes the ATLAS Tile Calorimeter Digitizer-to-Rod Interface card design, performance and radiation hardness tests and production processes.

I. OVERVIEW

The ATLAS Tile Calorimeter (TileCal) [1] [Figure 1] front end electronics consists of four parts, 3-in-1 cards, control motherboards, digitizer boards, and interface card. A block diagram is shown in Figure 2. Up to 48 phototubes and associated 3-in-1 cards can be mounted in each of 256 electronics drawer which are housed inside the backbone girders of the TileCal wedges.

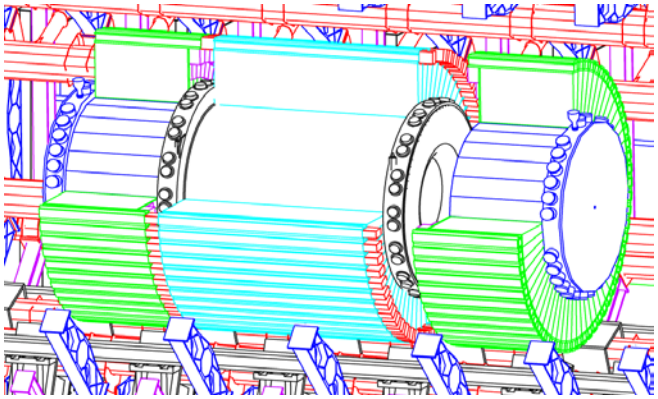

Figure 1: The Tile Calorimeter

The 3-in-1 cards provide a high and low gain shaped output pulses to the digitizer boards, analog trigger output to tower trigger sum boards mounted on the control motherboards, and a slow integrator output used in the Cesium source calibration of the detector. The control motherboard system receives messages via the TTC (Trigger, Timing, and Control) system [2]. The commands configure the 3-in-1 cards, initiate charge injection, set the integrator gain and DAC calibration, and gate the trigger signal. A source calibration ADC card readout via CANBUS is also mounted on the control motherboards. Fast pulse signals from the 3-in-1 cards are digitized in eight digitizer boards and sent down a digital pipeline. On receipt of a level-1 trigger, the digitizer boards capture an event frame consisting of a string of digitizations. The events (data frames) are stored locally and queued for transmission to the interface card.

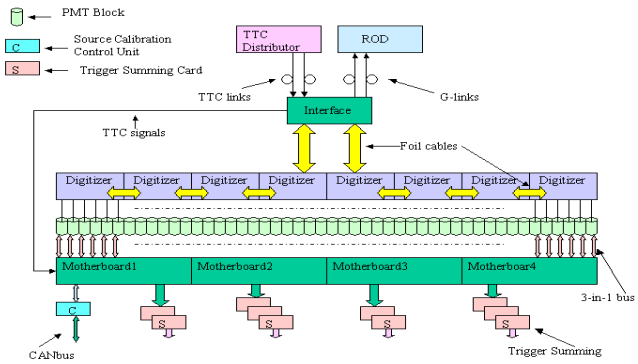

Figure 2: TileCal Readout Electronics Diagram

ATLAS TileCal Interface card carries out four basic functions. First, it receives the TTC optical signal, and distributes it to eight digitizer boards and to the control motherboard system. Second, it collects data from the digitizer cards. Third, the data is aligned and sorted into event frames. Fourth, it transmits data via an optical G-link to the off detector readout drivers crates (ROD) at a data rate of 640 Mbps. Cyclic Redundancy Checks (CRC) are performed on the input and output data streams.

The important considerations for the interface card are resistance to single point failure and appropriate radiation tolerance.

The functional system structure of the interface card is shown in Figure 3.

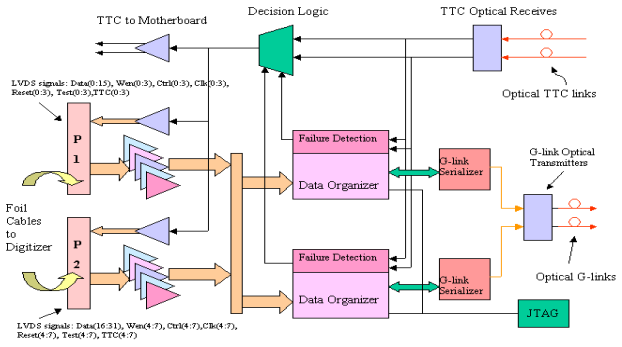

Figure 3: Interface Functional System Structure.

II. TTC RECEIVER AND DISTRIBUTIONS

A low cost fiber optical receiver has been developed for interface card. The schematic is shown in figure 4.

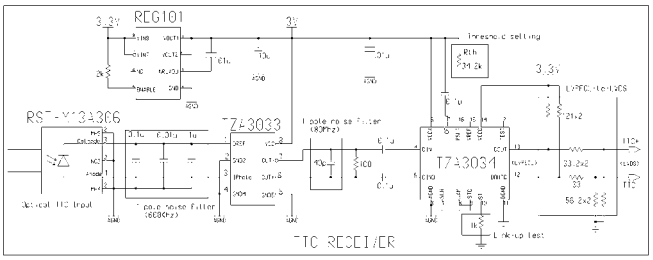

Figure 4: Schematic of TTC receiver.

The Phillips TZA3033 low noise transimpedance amplifier (TIA) with a built-in automatic gain control (AGC) loop amplifies the current that generated by the PIN photodiode when TTC optical signal is applied. The AGC loop of TIA makes it possible to handle a very wide input dynamic range from 0.25uA to 1.6mA. The AGC loop detects the peak of input signals and stored on a hold capacitor, the voltage across the capacitor is then compared to a threshold level that is fixed in an input current of 2.5uA peak to peak. If any input signal amplitude is larger then threshold level, then the AGC become active, otherwise, the AGC is disabled. TZA3033 also has low equivalent input noise of 1pA/√Hz and a moderate bandwidth of 130Mhz. In order to obtain a higher sensitivity, the photodiode output pin and the TIA input pin should be placed very close. Parasitic capacitance that may be cause by the component placement and board layout is required to be minimized. The power planes beneath the pin photodiode output pin and the TIA input pin are also removed for this purpose.

As a post amplifier, the Phillips TZA3034 amplifies the differential signals from TZA3033 TIA and limits the output signals to a differential LVPECL level. A user programmable differential input threshold is set by a single external resistor R_{th}, its value is determined by the formula [3]:

$$V_{th}(\text{diff}) = 830/R_{th} \ [\text{V}].$$

The threshold of TZA3034 post amplifier was set at 24.3mV by a 34.2K resistor for optimization of the noise margin based on TIA output signal amplitude. An 80Mhz, one pole noise filter for the TIA output signals and a 600Khz, one pole noise filter for the PIN photodiode bias voltage pin are also applied to reduce system noise.

Before distributing TTC signal to digitizer boards and motherboard, TTC logic level signals were sent to FPGAs for failure detection. TTC transitions are counted from the two input fiber circuits for a fixed time interval in each of the two FPGAs that independently process data. Each raises or lowers its selection line depending on the choice make. Both selections choose input A (selection line low) if both TTC circuits are deemed operational. An OR circuit selects TTC input B if it is selected but either FPGA.

The selected TTC signal is fanned out to nine pairs of LVDS differential signals. Eight of them are sent to digitizer boards and one to the control motherboards. The TTC signals provide control signals bunch crossing identification, level-1 trigger signals, and locally phased clocks at each TTCrx receiver chip [4].

III. DATA ORGAZIZER

Each 3-in-1 card [5] uses a 7-pole shaper with shaping time of 50ns to shape photo multiplier tube (PMT) output before digitization. In order to achieve a 16-bit dynamic range using 10-bit ADCs, a bi-gain system is used with a 64:1 gain ratio. The high-gain amplifier has a gain of 32 and low-gain amplifier has a gain of 0.5. The low gain output has a sensitivity of 2V/800pC. Eight digitizer boards each receive fast pulse signals from the 3-in-1 cards. High and low gain signals are digitized in 10-bit ADCs and sent to pipeline de-randomizer of Tile-DMU chips. The ADCs digitize at 40.079Mhz using a TTC supplied clock which also is the accelerator bunch structure clock. Each digitizer has two Tile-DMUs which process data from three PMTs. The raw data are sent down a pipeline of programmable length. When level-1 trigger accept is received (via TTC), a programmable number of consecutive samples are moved to a de-randomizer buffer. Normally, the high gain samples are selected unless a programmed level is exceeded, in which the low gain data are retained. An operation mode is also available for retaining both gains for calibration purposes. After data is retrieved from Tile-DMU de-randomizer buffer, it is serialized into two data stream and sent out to the interface card at a rate of 40.079 MBPS. The Tile-DMU sends out data block by block. Consecutive data blocks may contain overlapping samples. The maximum level-1 trigger rate specification for the ATLAS detector is 100Khz at design luminosity.

The four serial signals from each digitizer board (two from each Tile-DMU) plus a clock and various control signals are transmitted down to the interface card mounted at the center of the drawer. Inter-board connections are via 100-pin high-density connectors. Flexible foil cables are used for these connections. In order to reduce signal reflection the impedance of foil cables are designed to match the trace impedance on the boards. All signals transmit between the interface and digitizer boards are in low voltage differential level with point-to-point connections.

The VHDL code block diagram for Altera FPGA Chip EP20K160E is shown in Figure 5.

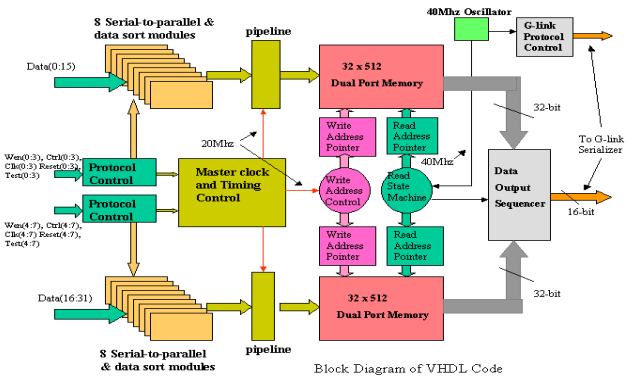

Figure 5: Block Diagram of VHDL Code

The major processing of the serial data sent by the digitizer boards as processed in the interface cards are as follows.

(a) *16 Serial-to-parallel and data resort modules (s2p_sort)* s2p_sort unscrambled and re-aligned 2-bit serial input data to 32-bit words corresponding to header, data and CRC checksum information from each Tile-DMU. The input data protocol controls are also incorporated with these operations.

(b) *Two pipeline modules*
Each pipeline module is asynchronously loaded by eight 32-bit words presented by eight s2p_sort modules every 400ns. Meanwhile, it unloaded every word subsequently through a multiplexer at a rate of 50ns into downstream dual port memory. In order to avoid of timing contention during data load and unload, the last unloaded four words in the pipeline are double buffered.

(c) *Two dual port memories*
Each dual port memory stores 512 32-bit data words from a half drawer. The advantage of using dual port memories is that the Interface card can easily order the data output sequence of channels according to consecutive PMT samples.

(d) *One master clock selection logic unit*
A master clock is used to move data from pipelines to the dual port memory. This clock is selected at power based of a count of clock transitions.

(e) Data Output Sequencer

- A state machine controlled data output sequencer moves data from two 32-bit word dual port memories into a 16-bit word G-link serializer. The data rate is 40M words (16-bit) per second.

- The state machine first sends out a start of event word with the serializer control line high. Next the 16 blocks of data are sent to the serializer corresponding to the data from the 16 Tile-DMU chips. These blocks consist of a header word containing

- Configuration data, sample count number, bunch crossing number, and various parity bits.

- The most significant bit of the header word is always 1. Next the N samples are sent. Each word is of the form 0-p-s1-s2-s2. Where p is the lateral parity, s1, s2, s3 are the 10-bit ADC counts for three phototube channels processed by the Tile-DMU chip. Lastly a word consisting of the two16-bit CRC words associated with two serial data streams from Tile-DMUs is sent. To distinguish from the header word, the CRC-pair word has zero set in the most significant bit.

- After the 16 blocks are sent, a serial CRC ERROR WORD is sent. This word has all bits set to "1" if all of the 32 serial CRC words sent correctly by the digitizer boards check with calculations made in the interface board (see CRC-16 below).

- Next, the state machine sends out a global CRC word. This consists of zeros in the higher order 16-bit and a final 16-bit global CRC calculated from each word sent to the serializer since the start of event control word. This word is transmitted to the serializer with FLAG set to "1" ("0" for all other words).

- Finally, the end of event word is sent with serializer CONTROL line set high.

(f) *CRC checks*
Two type of CRC checks are implemented for transmission error check in both input and output segments. CRC-16 check is applied for the error check in the incoming data to the interface card. Instead of applying 32 calculations to the input data lines, an equivalent parallel calculation is applied as each 32-bit data word is queued for output. This was found to be a much more effective use of resources. The calculation is reset on each header word (high order bit is "1"). As each word is processed, it is compared with the last CRC calculation. If a (15 bits) match is detected, a bit is set to "1" in the CRC ERROR WORD.

The GLOBAL CRC check enables a similar check on the total event to be preformed at the ROD which receives the transmitted data from the interface card.

The principle complexity of the interface cards lies in the different skew of the eight input clocks and in the complex addressing required to accumulate and transmit data at different rate.

IV. G-LINK SERIALIZER AND OPTICAL FIBER TRANSMITTER

A G-link transmitter HPMP-1032 [6] from Agilent Technologies is used to drive a custom designed dual optical transmitter. HPMP-1032 is a 1.4 GBd, 3.3V power supply, and low power dissipation serializer with conditional inversion master transition (CIMT) encoding protocol. The CIMT encodes three types of words: Data words, Control words and Idle words. Idle words are generated internally when serializer is idle. Each parallel input data word (16-bit) is encoded to 20-bit serial output data in a differential LVPECL levels to drive optical transmitter. The 20-bit data consists of a word filed (16-bit) and coding field (4-bit). The coding field indicates the data types. A 40 MHz clock (TXCLK) is used to load 16-bit parallel data from data organizer to serializer and phase locked to makes an 800Mbpsd output transmission rate. The true data rate is 640Mbps after data decoding in G-link destination card [7]. A dual custom designed optical transmitter with 3.3V power supply is driven by serializer to transmit data to ROD over two optical fibers. The wavelength of transmitter is 850nm and the bandwidth is 1.25GBd. Max3288 is used to drive VCSEL laser diode that pre-aligned with ST receptacle. A temperature compensation circuit is incorporated for laser driver to guarantee a stable output power of the laser.

V. PERFROMANCE AND RADIATION RESULTS

The Level-1 trigger specification for ATLAS detector is 100KHz maximum. At this maximum trigger rate and a nominal frame size of seven samples, the interface operates at 75% capacity. The interface can buffer 16 events of this size and the digitizer boards have a similar capacity. Currently available ROD hardware does not allow testing at the full level-1 maximum trigger rate. To test the system, bursts of triggers were sent through the system, for instance, with a burst of 12 level-1 triggers spaced 100ns apart. The system has also been extensively used for the last two years in the test beam calibration of production TileCal modules. The system performs in all tests as expected.

Radiation testing is an important part of the ATLAS detector electronics qualification procedure. The radiation tolerance requirements for the interface card and other components in the electronics are quite modest since it is located behind the calorimeter. TABLE-1 lists the interface testing requirements based on the drawers receiving the greatest exposure. The simulation level is based on 10 years of operation at full design luminosity. Safety factors are applied for uncertainty in the full shower simulation model, component lot variation, low dose rate effects, etc.

Radiation Type	Simulation Level	Safety Factor	Required Level
Total Ionizing Dose (TID)	0.023krad	70	1.6Krad
Non-Ionizing Energy Loss (NIEL)	$1.5\text{x}10^{10}$ n/cm^2	20	$3.0\text{x}10^{11}$ n/cm^2
Hadrons Above 20Mev (SEE)	$6.3\text{x}10^{8}$ h/cm^2	20	$1.3\text{x}10^{10}$ h/cm^2

Table-1 Radiation level for 10 years of 10^7 seconds each, at design luminosity

No increase in current draw was observed in the test and the exposed cards operated normally after irradiation [7].

Total ionizing dose (TID) tests were performed at Argonne National Laboratory in a cobalt-60 hot cell facility. The Interface was placed at three meters from the sources for 15 minutes. The TID rate is 9.57 Krad/hr. The exposed dose on Interface card was 2.4Krad, which is 50% larger than required level for the test. No increase in current draw was observed in the test and the exposed cards operated normal after irradiation [8].

Non-Ionizing Energy Loss (NIEL) test was performed at the CEA / PROSPERO in Dijon, France. A total dose of $5.0\text{x}10^{11}$ neutron/cm^2 is exposed. No effects in the performance of the interface were detected.

Hadrons Above 20Mev (SEE) test is performed at the Indian University Cyclotron. A 200 MeV proton beam with a typical flux at 5.8×10^6 p/cm/s is used for the studies. A total of fluence per run is measured at 1.5×10^{10} p/cm2 with an accuracy of a few percent.

Based on these tests, we would expect one latch up to occur in one of the 256 interface cards in 10 years of ATLAS running which can be reset by cycling At the power. Single event upset is expected at a rate of one event in 10^7 seconds.

All three studies have demonstrated that interface will operate successfully in the anticipated radiation environment.

VI. PRODUCTION QUALITY CONTROL

In order to ensure proper assembly of the cards, a workmanship inspection list [9] is provided to the production vendor. It includes PCB and assembly quality controls, trace impedance control, mechanical dimensions, board flatness tolerance etc. Solder quality inspection and electrical tests that requirements are also specified. The vendor is required to bake chip to remove moisture before soldering and clean of all extraneous debris and flux residue. No excess solder, short circuits, wrong component orient is allowed. A test database is established for

production test at the University of Chicago. Each card is labeled with a bar code serial number. A photo of a pre-production card is shown as Figure 6.

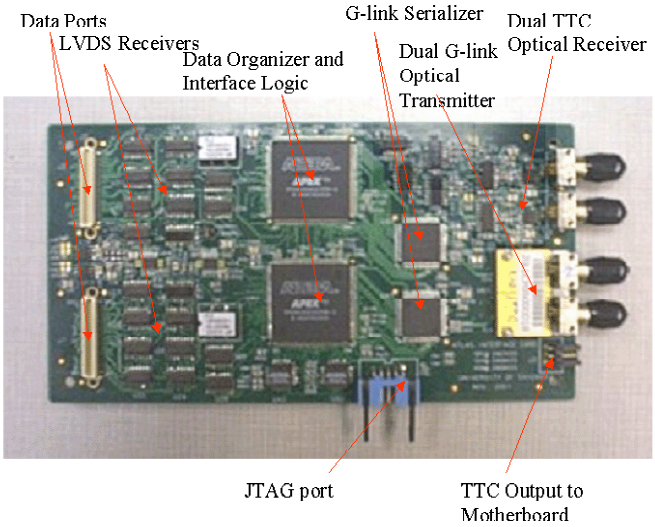

Figure 6: A Photo of Pre-production Interface Card.

A first batch of five cards will be assembly and tested in a completed drawer test stand. All five cards must pass the workmanship requirements and no more than one card can show any source of electrical failure for production to proceed. If the control sample fails to meet these requirements, the vendor will be informed of the nature of the problem and must submit a new control sample that successfully passes the tests before the production begins.

A burn-in at 65C^{o} for five days will be applied to all cards under power-on condition. All cards pass all functional and performance test and be logged into database before delivering to CERN for installation.

VII CONCLUSIONS

The production version of interface cards successfully passed their electronic performance and radiation hardness tests. They are now being installed in production TileCal modules.

VIII. REFERENCES

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