The Design of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger
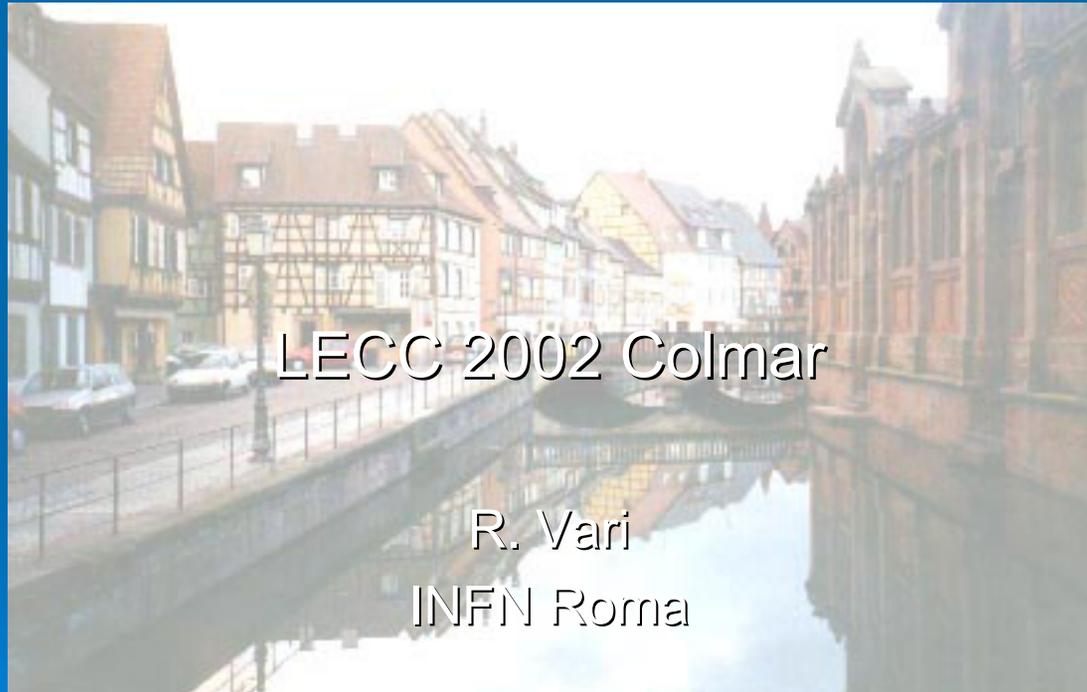
LECC 2002 Colmar

R. Vari

INFN Roma

Level 1 Barrel Muon Trigger Algorithm
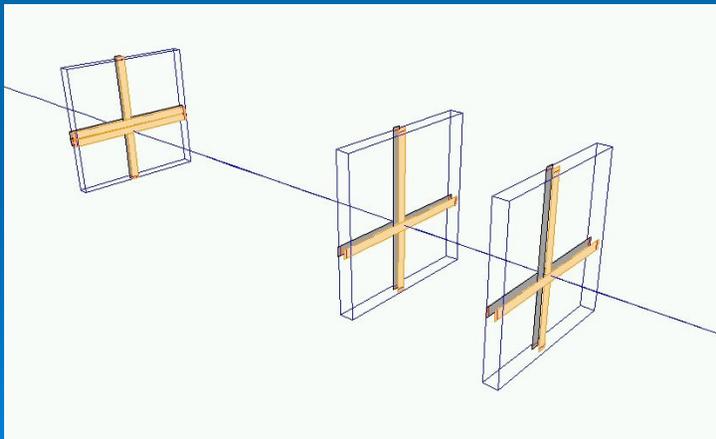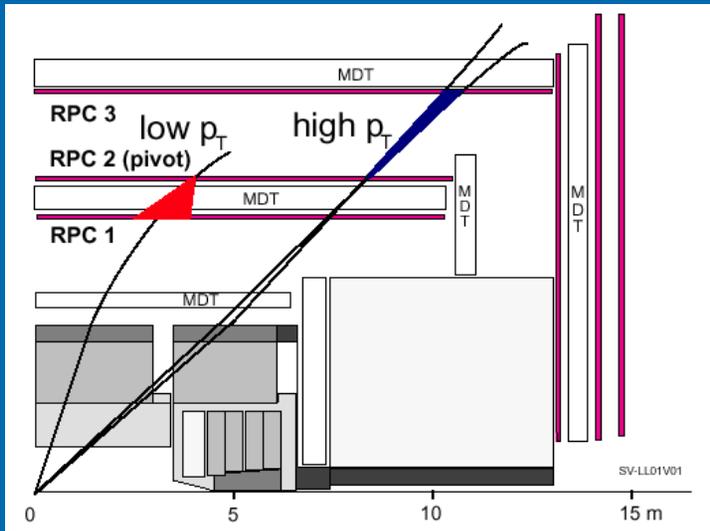
- System based on three Resistive Plate Chamber detector layers

- Each RPC detector is composed by a doublet of η and ϕ strips

- A coincidence of two (low p_T) or three (high p_T) hits in different detector layers is required for a valid trigger

Coincidence Matrix ASIC Functionality

➢ The Coincidence Matrix ASIC performs most of the functions needed for the low-p_T and high-p_T triggers and for the read-out of the ATLAS Barrel Level1 Muon Trigger

➢ Trigger and readout of 192 RPC FE signals

➢ Timing and digital shaping of the signals coming from the RPC doublets

➢ Execution of the trigger algorithm, local muon track candidates identification and p_T classification

➢ ROI overlap flagging

➢ Data storage during Level1 latency

➢ Storage of readout data in derandomizing memory

➢ RPC hit time measurement with 3.125 LSB (1/8 BC)

➢ Readout data serializer

Level 1 Barrel Muon Trigger Scheme
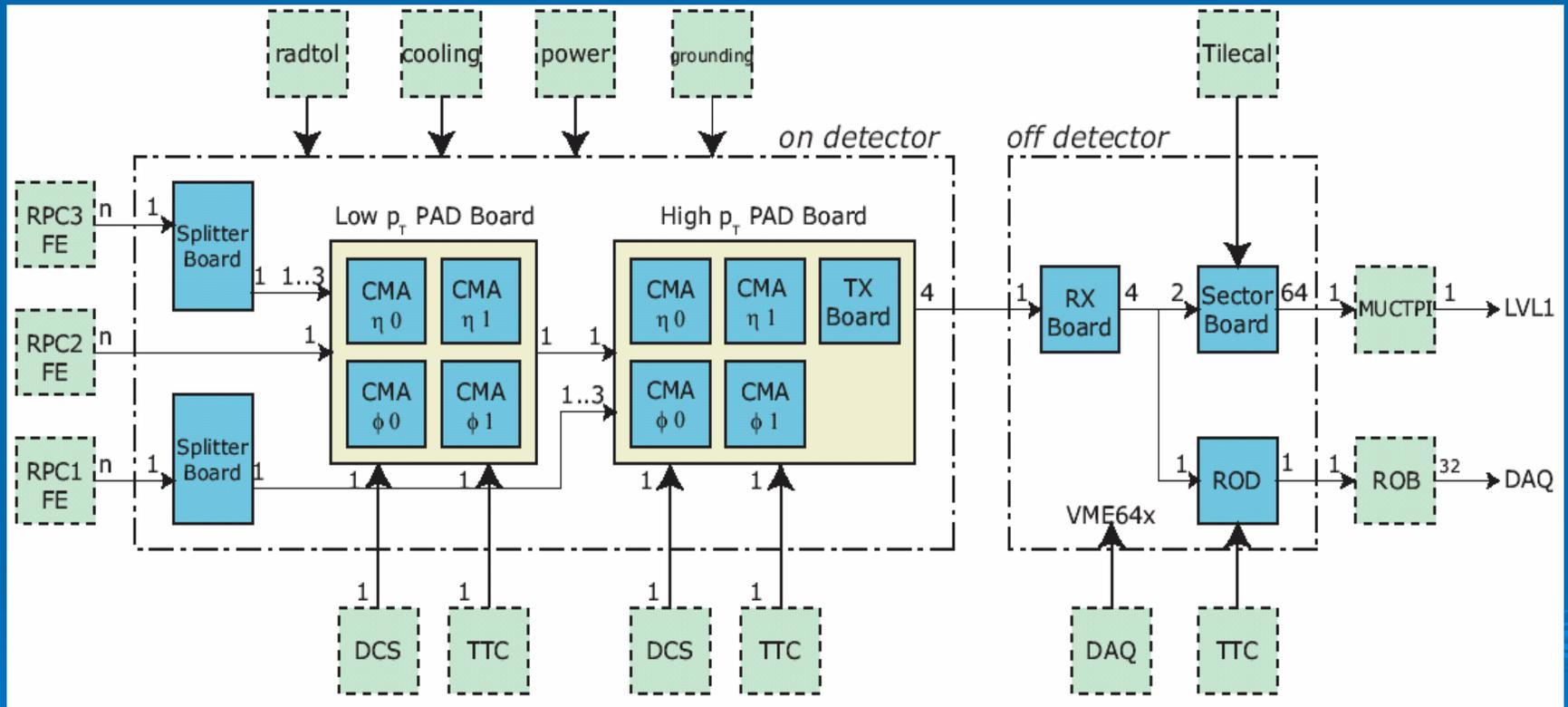
PAD Board
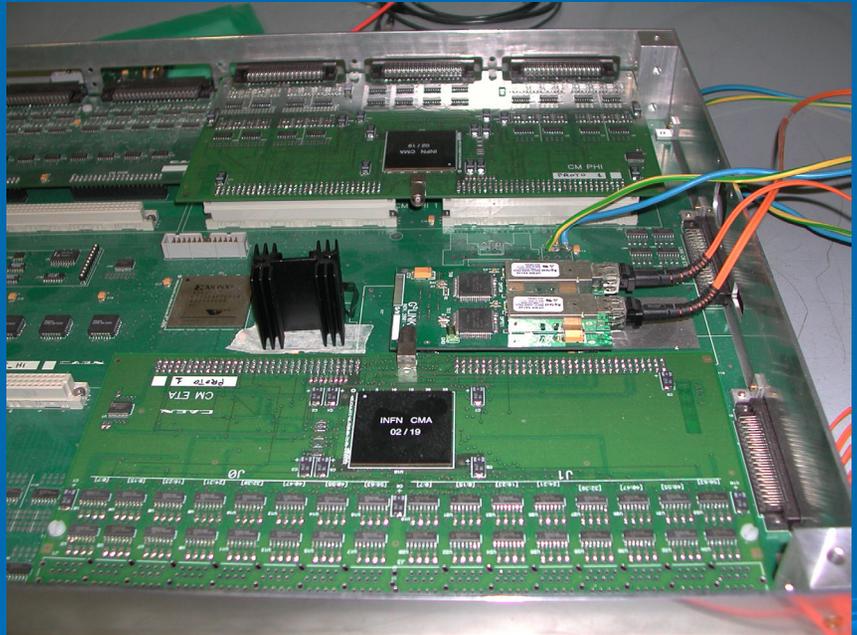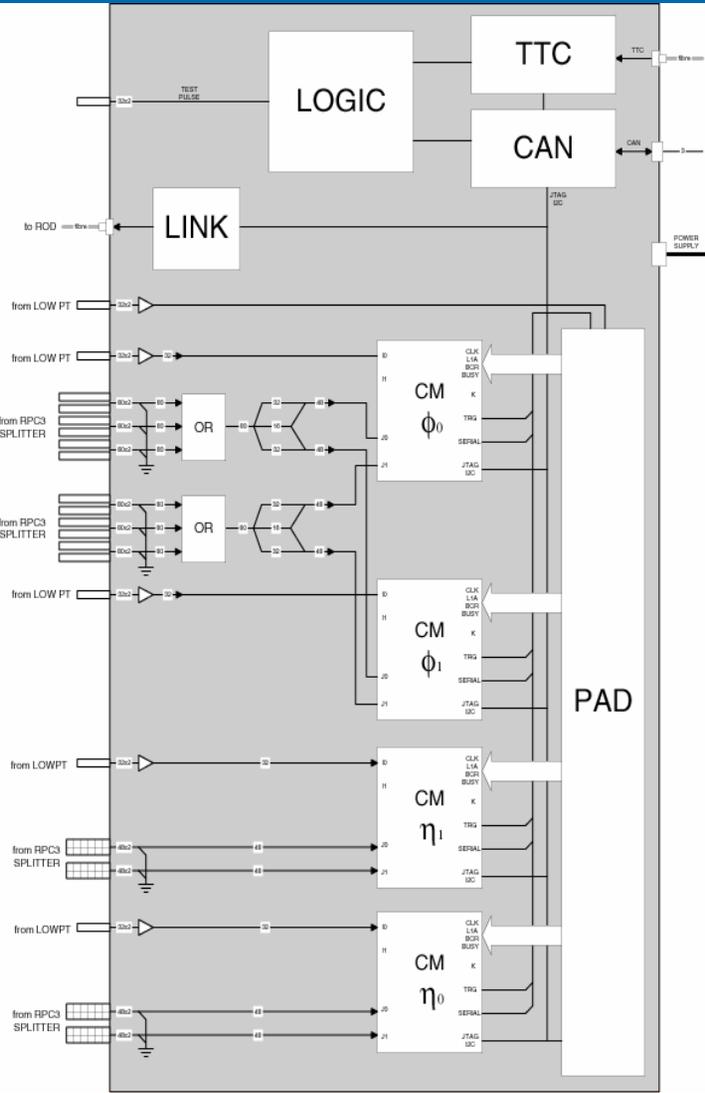
PAD Box

Radiation Environment

Feb 2001 Base (3278) – TotHadrs +N>20MeV /cm**2/Yr (SEE)

Feb 2001 Base (3278) – Ionization Dose, Gy/Yr (TID)
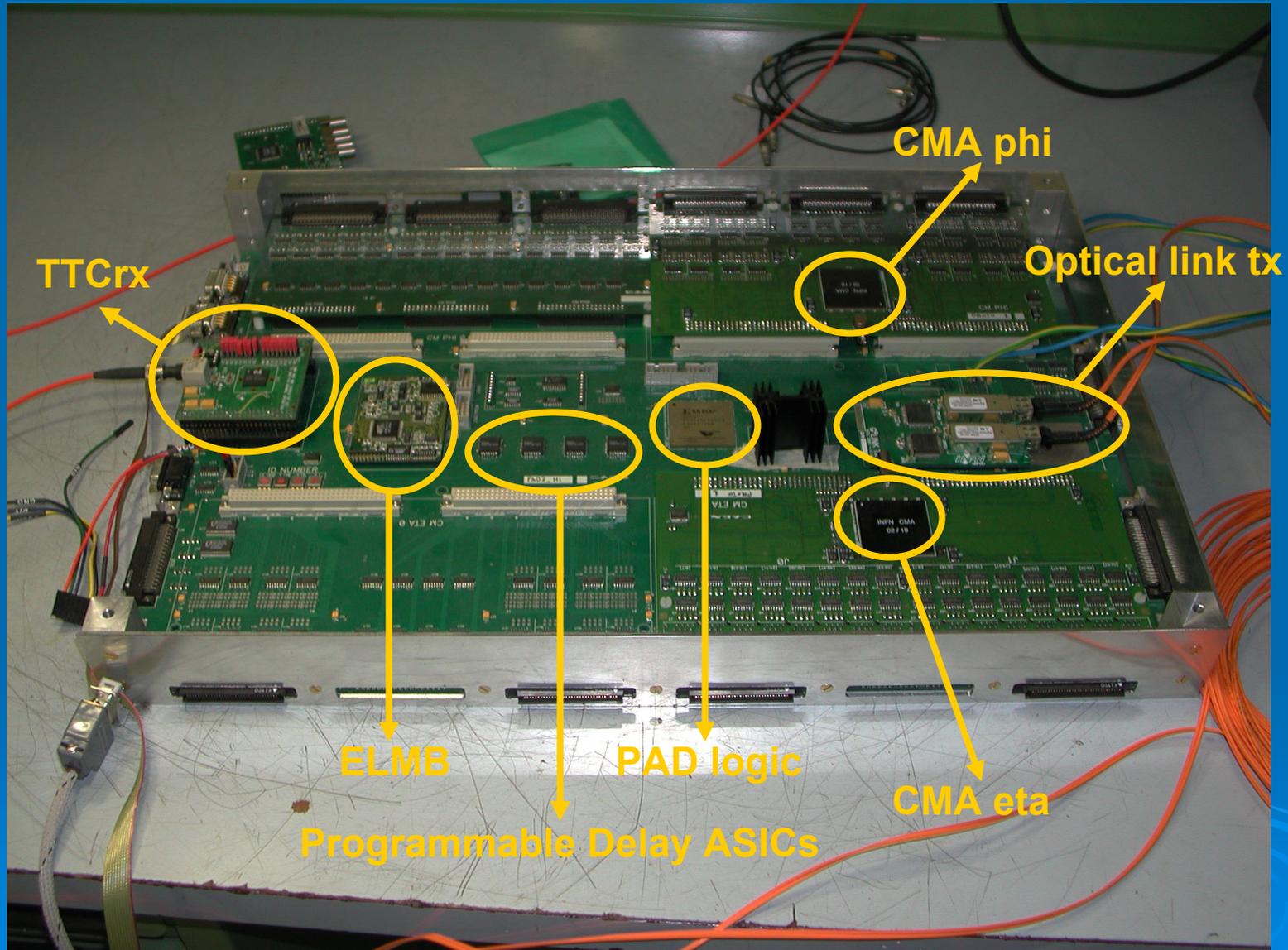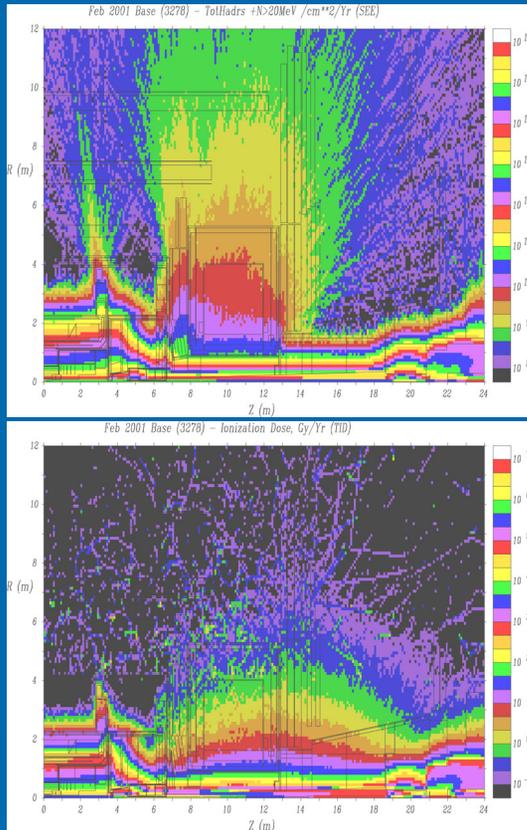
	SIMULATED RADIATION LEVEL		
	SRL_{tid} [Gy·10y^{-1}]	SRL_{niel} [1 MeV n·cm^{-2}·10y^{-1}]	SRL_{see} [> 20 MeV h·cm^{-2}·10y^{-1}]
BMF	3.02	$2.49 \cdot 10^{10}$	$4.69 \cdot 10^{9}$
BML	3.04	$2.82 \cdot 10^{10}$	$5.65 \cdot 10^{9}$
BMS	3.03	$2.50 \cdot 10^{10}$	$4.73 \cdot 10^{9}$
BOF	1.19	$2.14 \cdot 10^{10}$	$4.08 \cdot 10^{9}$
BOL	1.33	$2.20 \cdot 10^{10}$	$4.21 \cdot 10^{9}$
BOS	1.26	$2.10 \cdot 10^{10}$	$4.10 \cdot 10^{9}$

➤ $RTC_{tid} = SRL_{tid} \cdot SF_{sim} \cdot SF_{ldr} \cdot SF_{lot} \cdot 10y \sim 1$ kRad (SF=3.5x1x1)

➤ $SEU_f = ($soft SEU_m / ARL$) \cdot (SRL_{see}$ / 10y$) \cdot Sf_{sim}$ (SF=5)

- SEU_m = the number of measured soft SEU during test.
- ARL = integrated hadrons flux received by the tested component.

CMA Architecture
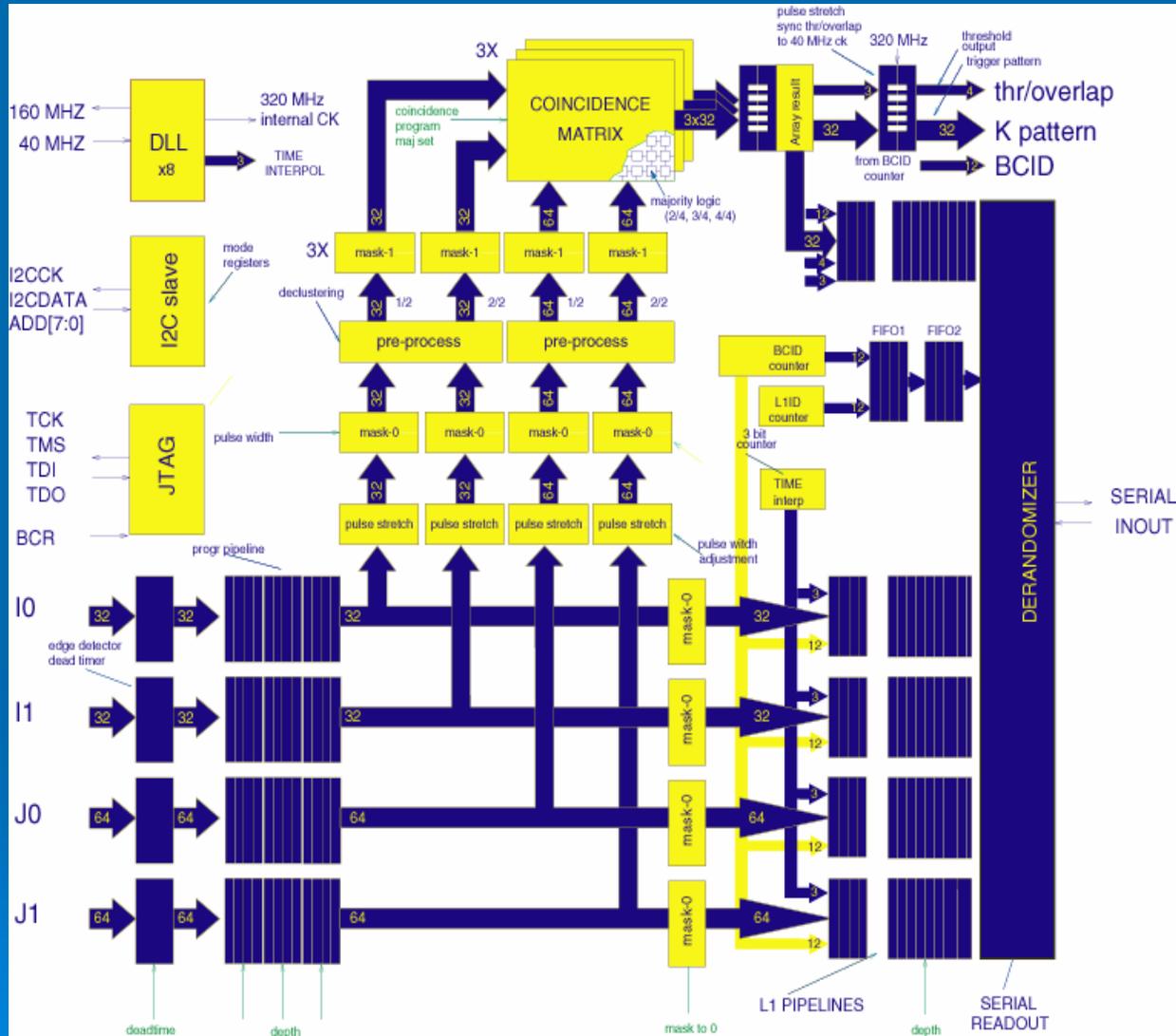
CMA Layout

- UMC 0.18 μm, 6 metal layers, 1.8 V core power supply, 3.3 V I/O pads
- 430 kgates
- Chip area: 4.5×4.5 mm^2
- Virtual Silicon standard cell library
- 320 MHz PLL (x8) macro
- 24 double-port RAMs
- 352 pins BGA package

INFN CMA
02 / 08
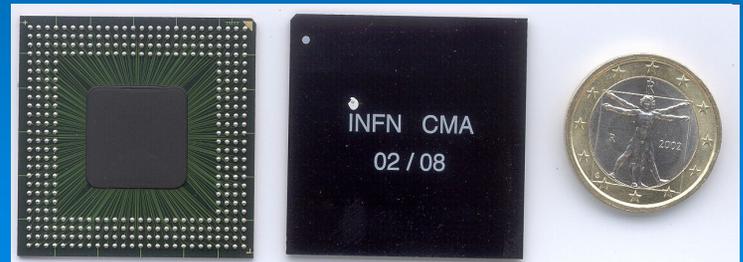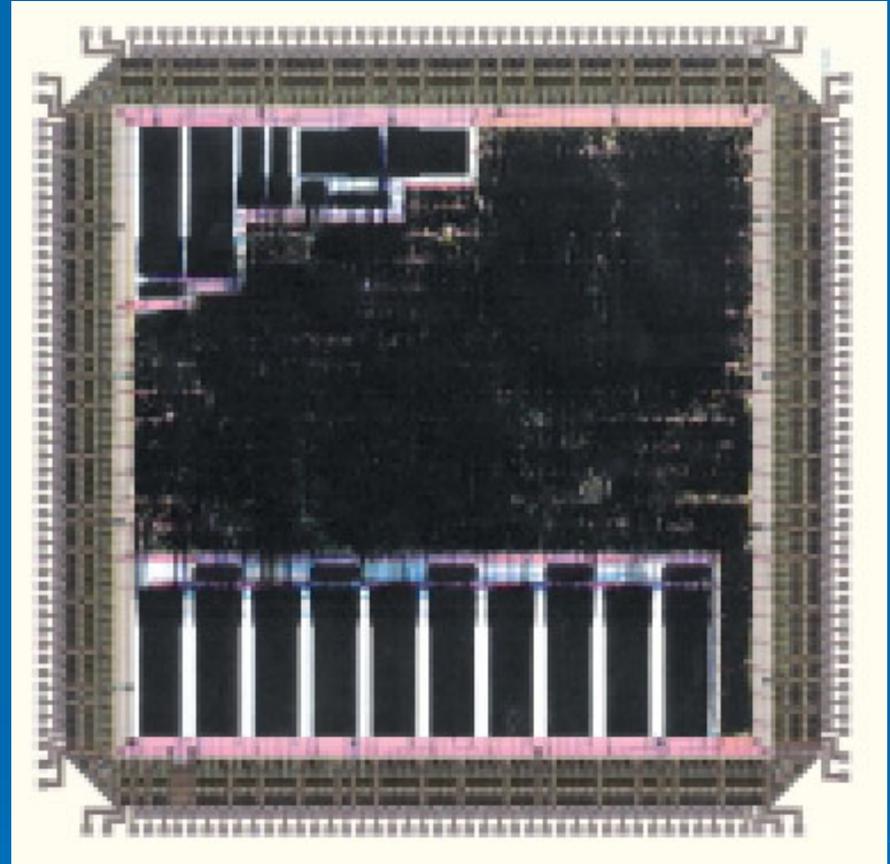
I/O signals

I0[31:0]	positive pivot plane 0 / low pt k-pattern
I1[31:0]	pivot plane 1
J0[63:0]	non-pivot plane 0
J1[63:0]	non-pivot plane 1
L1ACCEPT	L1 Accept signal
L1CNTRES	L1 counter reset
BCNTRES	BCID counter reset
CLK	40 Mhz
TCLK	10 MHz
K[31:0]	k-pattern output
BCID[11:0]	Bunch crossing ID counter
THR[1:0]	Threshold value
OVL[1:0]	Overlap value
SER_D	DS-link Data line
SER_S	DS-link Strobe line

XOFF	Transmit off input
BUSY	ASIC busy signal
SCL	I2C clock line
SDA	I2C data line
DEVID[7:0]	Device identification input
TCK	TAP SCAN clock
TMS	TAP SCAN MODE
TRST	TAP SCAN RESET
TDI	TAP SCAN IN
TDO	Tristate TAP SCAN OUT
SE	Scan enable signal
TST	Test enable signal
CLKOUT	pll_clk tree output
CLK160OUT	clk_160 tree output
CLR_N	Asynchronous clear

Timing Block

- CMA has 3 clock domains, 2 working modes
- Initialization mode:
  - all blocks are driven by the external 40 MHz clock
  - the PLL is bypassed and the 160 MHz clock divider is excluded
  - all registers are accessible as shift registers, driven by the I2C interface.
- Run mode.
  - the PLL is in lock mode, provides the 320 MHz clock, and drives the 160 MHz clock generator.

Input Pipeline Block
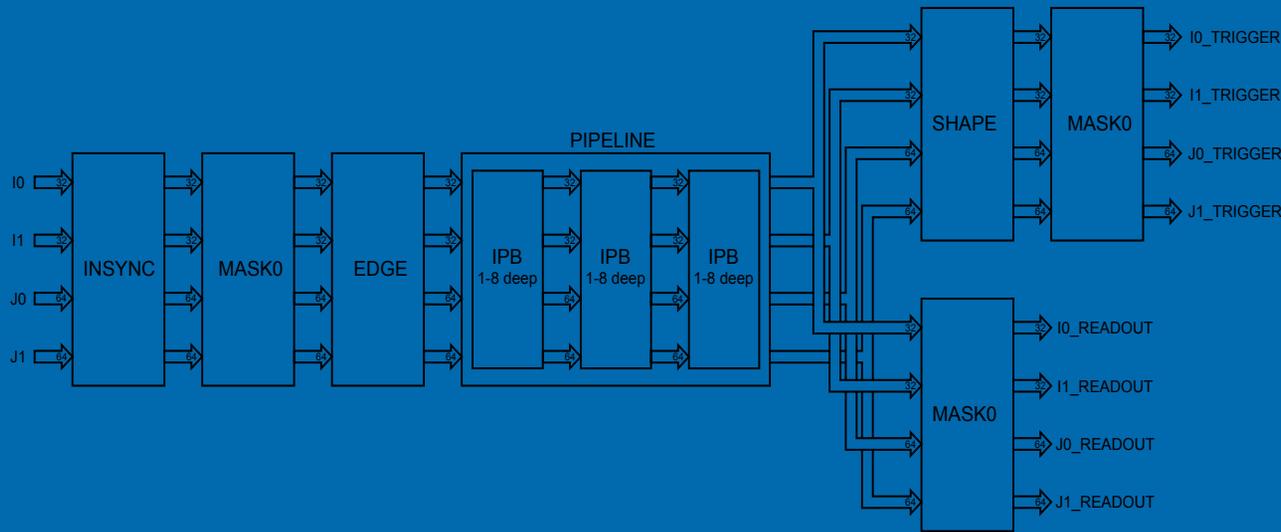
- ➢ Front-end signal digital shaping is programmable in the range 1/8÷1 BC.
- ➢ Pipeline delay is programmable in the range 3/8÷3 BCs
- ➢ FE signal dead time is programmable in the range 0÷4 BCs, in steps of 1/8 BC

Trigger Block
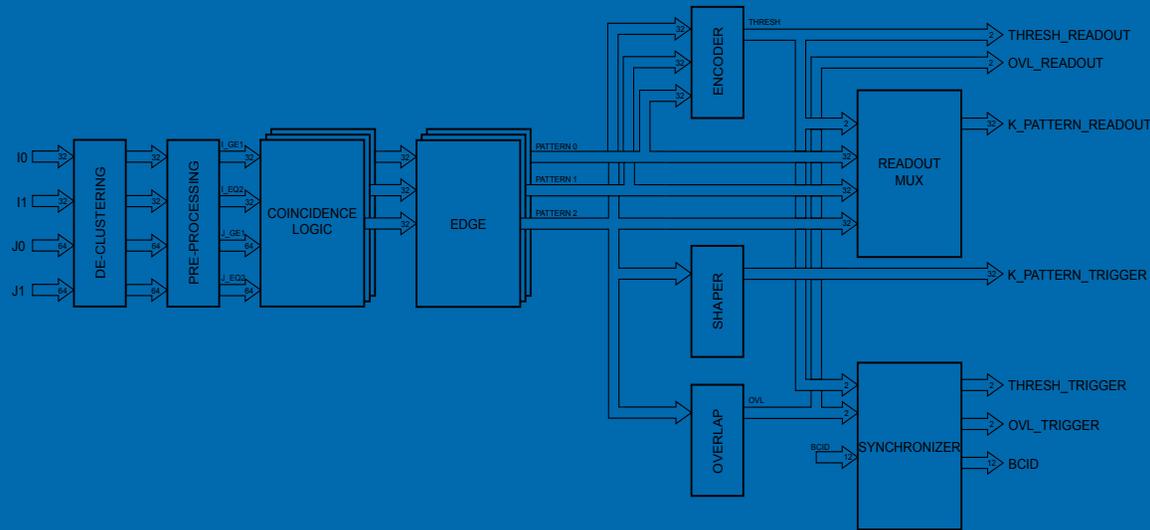
- ➢ Coincidence logic works at 320 MHz
- ➢ Number of matrices/thresholds is 3, logic is repeated three times in parallel, one per threshold setting
- ➢ Majority logic is 1/4, 2/4 (one hit per doublet), 3/4, 4/4
- ➢ The highest threshold k-pattern which has a non-zero trigger information is shaped in time and then sent to the chip output pads

De-clustering + preprocessing
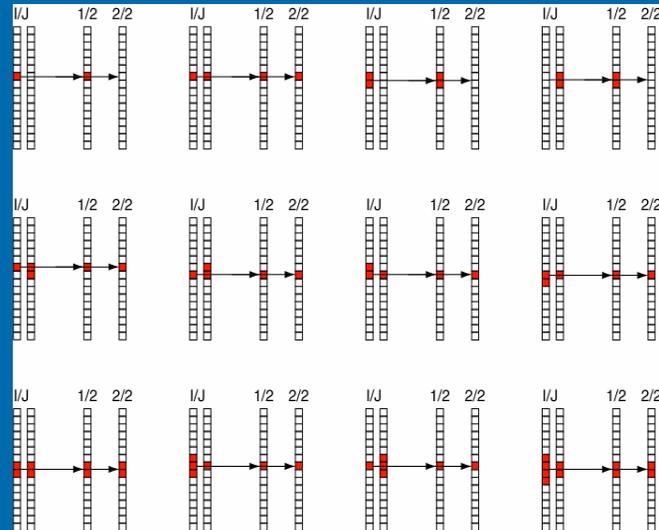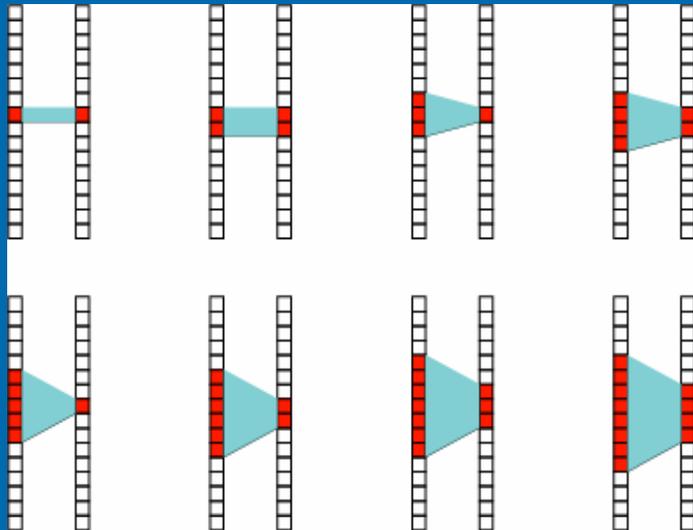
> ➤ RPC average cluster size is ~1.4.
> ➤ De-clustering logic type can be selected at CMA initialization.
> ➤ Max processed cluster size is programmable (up to ±3).

> ➤ Correlates hits from two detector layers
> ➤ 2/2 hits favoured over 1/2.
> ➤ programmable $\eta < 0$, $\eta = 0$, $\eta > 0$ modes can be selected at CMA initialization.

Readout Block
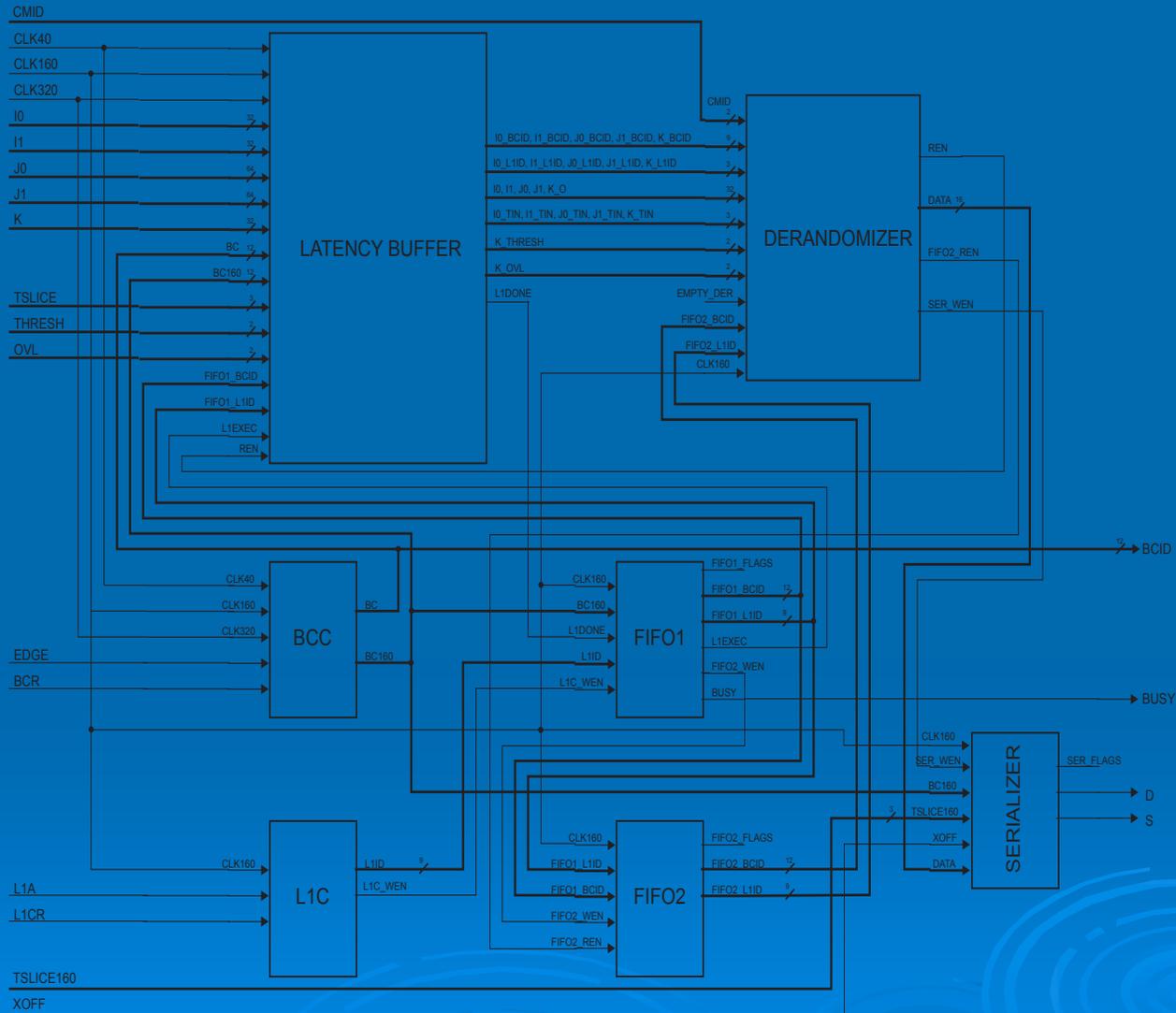
Readout block

- The latency buffer stores hit patterns coming from the input FIFO until they get old

- The input FIFO buffer is written at 320 MHz and contains the hit pattern, BCID and time interpolator value. The readout part of this buffer, together with the rest of the readout logic works at 160 MHz

- In the derandomizer buffer, hits belonging to the same L1ID are assembled in data frame

- All buffer memories are implemented with FIFOs

- FIFO1 and FIFO2 contain a list of L1IDs and relative BCIDs respectively to be processed by the derandomizer and ready to be sent via the serializer

- The serializer block attaches CRC codes to event fragments and ships the data out, following the DS-link protocol, at a programmable frequency of 10-80 MHz

SEU detection

- One parity bit is stored when register is initialized

- Register parity is checked against stored parity every clock cycle

- SEU output signal active when parity check fails

- Single Event Upset detection has been implemented for almost all CMA registers

- For the fundamental chip control registers (Main Control Register, Latency Registers, DSlink Register), triple redundancy, 2/3 majority, has been implemented for error correction.

REGISTER NAME	SEU DETECTION
MAIN CONTROL	yes
MAIN COUNT	no
MAIN STATUS	no
PIPE I0 MASK0 IN	yes
PIPE I0 EDGE	yes
PIPE I0 IPB REGDEPTH 1	yes
PIPE I0 IPB REGDEPTH 2	yes
PIPE I0 IPB REGDEPTH 3	yes
PIPE I0 IPB REGPIPE 1	yes
PIPE I0 IPB REGPIPE 2	yes
PIPE I0 IPB REGPIPE 3	yes
PIPE I0 SHAPE	yes
PIPE I0 MASK0 READOUT	yes
PIPE I0 MASK0 TRIG	yes
PIPE I1 MASK0 IN	yes
PIPE I1 EDGE	yes
PIPE I1 IPB REGDEPTH 1	yes
PIPE I1 IPB REGDEPTH 2	yes
PIPE I1 IPB REGDEPTH 3	yes
PIPE I1 IPB REGPIPE 1	yes
PIPE I1 IPB REGPIPE 2	yes
PIPE I1 IPB REGPIPE 3	yes
PIPE I1 SHAPE	yes
PIPE I1 MASK0 READOUT	yes
PIPE I1 MASK0 TRIG	yes
PIPE J0 MASK0 IN	yes
PIPE J0 EDGE	yes
PIPE J0 IPB REGDEPTH 1	yes
PIPE J0 IPB REGDEPTH 2	yes
PIPE J0 IPB REGDEPTH 3	yes
PIPE J0 IPB REGPIPE 1	yes
PIPE J0 IPB REGPIPE 2	yes
PIPE J0 IPB REGPIPE 3	yes
PIPE J0 SHAPE	yes
PIPE J0 MASK0 READOUT	yes
PIPE J0 MASK0 TRIG	yes
PIPE J1 MASK0 IN	yes
PIPE J1 EDGE	yes
PIPE J1 IPB REGDEPTH 1	yes
PIPE J1 IPB REGDEPTH 2	yes
PIPE J1 IPB REGDEPTH 3	yes
PIPE J1 IPB REGPIPE 1	yes
PIPE J1 IPB REGPIPE 2	yes
PIPE J1 IPB REGPIPE 3	yes
PIPE J1 SHAPE	yes
PIPE J1 MASK0 READOUT	yes
PIPE J1 MASK0 TRIG	yes

REGISTER NAME	SEU DETECTION
TRIG THR0 THR REG (0 .. 31)	yes
TRIG THR0 MAJ REG	yes
TRIG THR0 MASK 1 I GE1 REG	yes
TRIG THR0 MASK 1 I EQ2 REG	yes
TRIG THR0 MASK 1 J GE1 REG	yes
TRIG THR0 MASK 1 J EQ2 REG	yes
TRIG THR1 THR REG (0 .. 31)	yes
TRIG THR1 MAJ REG	yes
TRIG THR1 MASK 1 I GE1 REG	yes
TRIG THR1 MASK 1 I EQ2 REG	yes
TRIG THR1 MASK 1 J GE1 REG	yes
TRIG THR1 MASK 1 J EQ2 REG	yes
TRIG THR2 THR REG (0 .. 31)	yes
TRIG THR2 MAJ REG	yes
TRIG THR2 MASK 1 I GE1 REG	yes
TRIG THR2 MASK 1 I EQ2 REG	yes
TRIG THR2 MASK 1 J GE1 REG	yes
TRIG THR2 MASK 1 J EQ2 REG	yes
TRIG DECLU I0 CLSIZE	yes
TRIG DECLU I0 PIPE	no
TRIG DECLU I1 CLSIZE	yes
TRIG DECLU I1 PIPE	no
TRIG DECLU J0 CLSIZE	yes
TRIG DECLU J0 PIPE	no
TRIG DECLU J1 CLSIZE	yes
TRIG DECLU J1 PIPE	no
TRIG PRP I GE1 REG	no
TRIG PRP I EQ2 REG	no
TRIG PRP I ETA REG	yes
TRIG PRP J GE1 REG	no
TRIG PRP J EQ2 REG	no
TRIG PRP J ETA REG	yes
TRIG SHAPE K REG	yes
TRIG OVL SX REG	yes
TRIG OVL DX REG	yes
TRIG EDGE REG	yes
READOUT BUFFER EMPTY	yes
READOUT BUFFER ALMOST EMPTY	yes
READOUT BUFFER HALF FULL	yes
READOUT BUFFER ALMOST FULL	yes
READOUT BUFFER FULL	yes
READOUT BUFFER LATREG	yes
READOUT BUFFER LOWREG	yes
READOUT BUFFER HIREG	yes
READOUT SERIALIZER DSLINK	yes
READOUT BCC PRE	yes
READOUT BCC CTR	yes
READOUT L1C PRE	yes
READOUT L1C CTR	yes

Testability

- 32+5 serial scan chains, JTAG boundary scan, I2C register access
- Scan chains (including RAM chains) used during ASIC acceptance tests:
  - All core registers and all RAMs are accessible via scan chains
  - Dedicated scan chains have been designed for RAM data, addresses and control signals, in order to be able to test the RAM cores
- JTAG for tests during board assembly test
- I2C is used for register accessibility and test pattern generation during trigger operation
- Input pipelines can be preloaded with hit patterns and chip can be run for a fixed programmed number of cycles

Design flow

- VHDL RTL code
- VHDL testbenches for all blocks and full chip
- Design exploration synthesis
- Top-down compile core and timing blocks
- Scan chains, JTAG and IO pads insertion
- Place & routing
- Clock tree
- Parasitic capacitance extraction
- Final layout

CMA LAB Test

- ➢ Loadboard developed for industry Teradyne tester

- ➢ The board has been designed with additional connectors for PLL test and lab tests in Rome
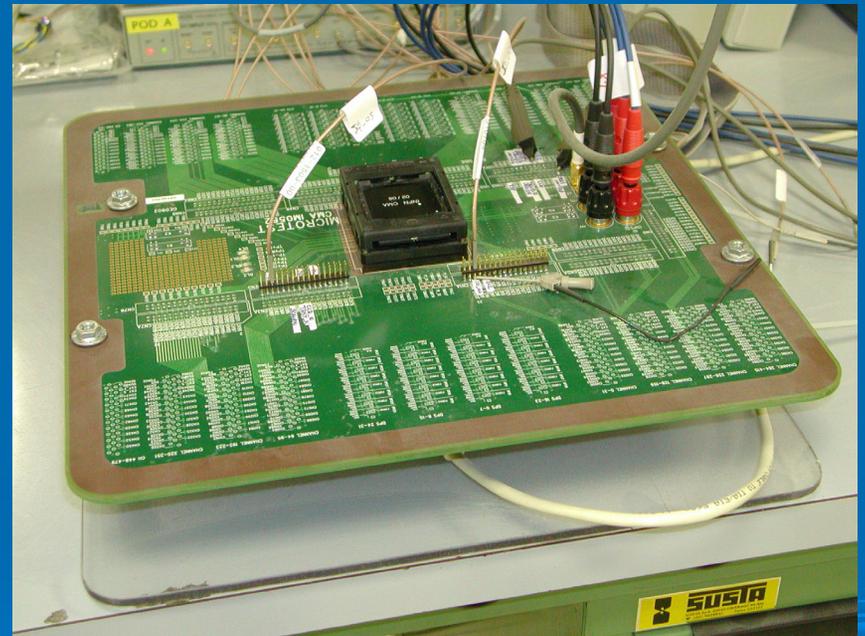
Test Patterns

- Scan and functional tests were performed on Teradyne machine at 1 Mhz, 40 MHz, at room and at 125°C temperatures. PLL lock was also tested.
  - SCAN test: 32 scan chains, maximum of 900 cells (generated with Synopsys Test Compiler)
  - RAM test: using single dedicated scan chain (23,743,440 cycles), generated from RTL model
  - Functional test: 105576 vectors, to test I2C interface and start PLL, generated from full netlist+timing simulation
- 86 packages tested by industry:
  - 7 GND fails
  - 5 RAM fails
  - 4 SCAN fails
  - 70 good (~81%)
  - No logic fail on functional test!

LAB setup

36x64K T=6.125ns
Pattern generator

Clock jitter

Waveform
Analyser T=10ns
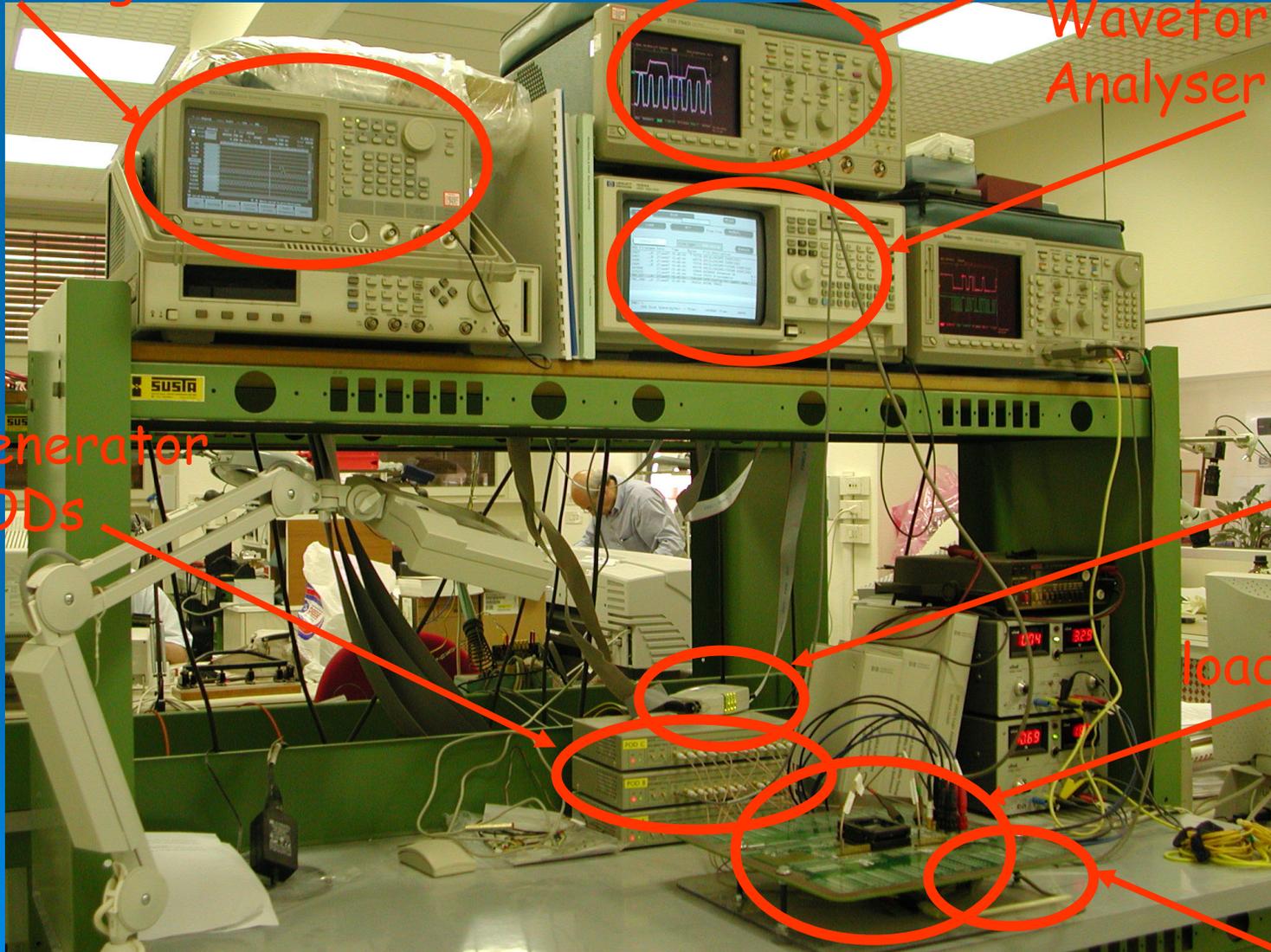
Generator
PODs

GPIB
LAN

loadboard

I2C on RJ45

PLL Test

➢ 160 MHz derived clock output has been used to check PLL stability (320 MHz)

➢ PLL has been characterized vs V and vs input frequency

➢ Measured jitter: 25 ps rms, 150 ps pk-pk

➢ PLL works according to specifications
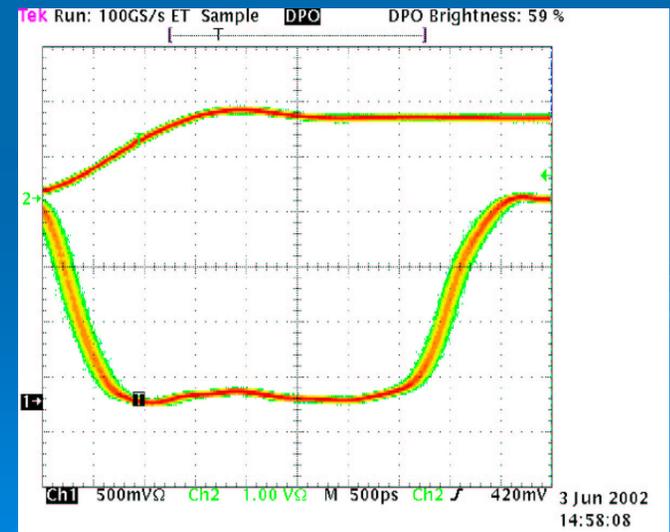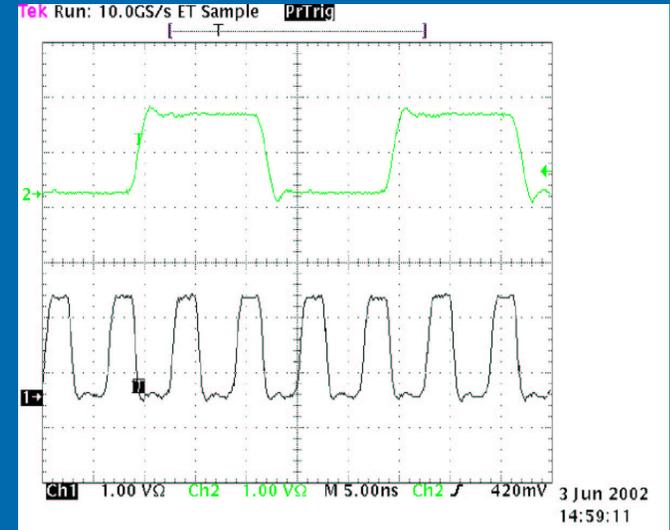
Trigger test

- Trigger test on a limited number of input channels, due to limitations on the laboratory setup

- Minimum pulse width measurement:
  - $T_{wmin} > 6.126$ ns (12 ns in specs)
  - Dead timer, pulse shaping and pipeline delay working according to specs.

Trigger output latency:

- Input to K-pattern delay
  - $T_{latkpat} = (59 \pm 1)$ ns
- Input to THR/OVL delay
  - $T_{latthr} = (63\div88 \pm 1)$ ns
- Skew between THR and OVL signals
  - $T_{outskew} = (2 \pm 0.5)$ ns

Readout test
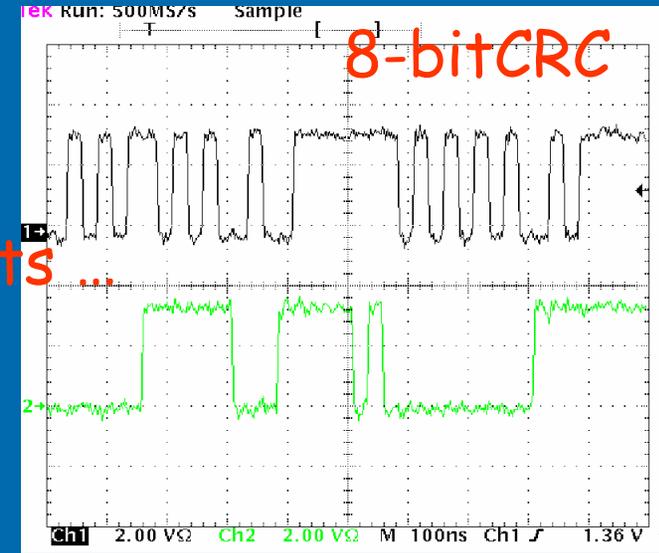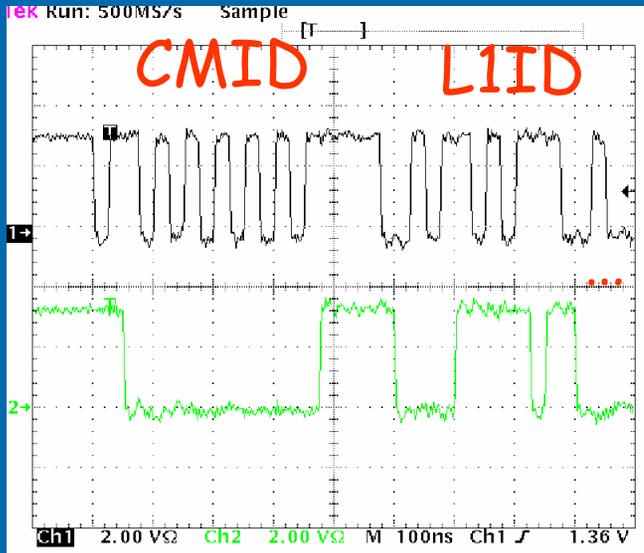
> ➢ **Readout tests done at 40 Mbit/s using:**
>   - 10ns period sampling with waveform analyser
>   - GPIB LAN box connected to waveform analyser
>
> ➢ **VISA-GPIB library (linux) in deserializer program has been used to convert waveform vectors to readout data fragments**

Readout latency

1% RPC occupancy
1-BC window
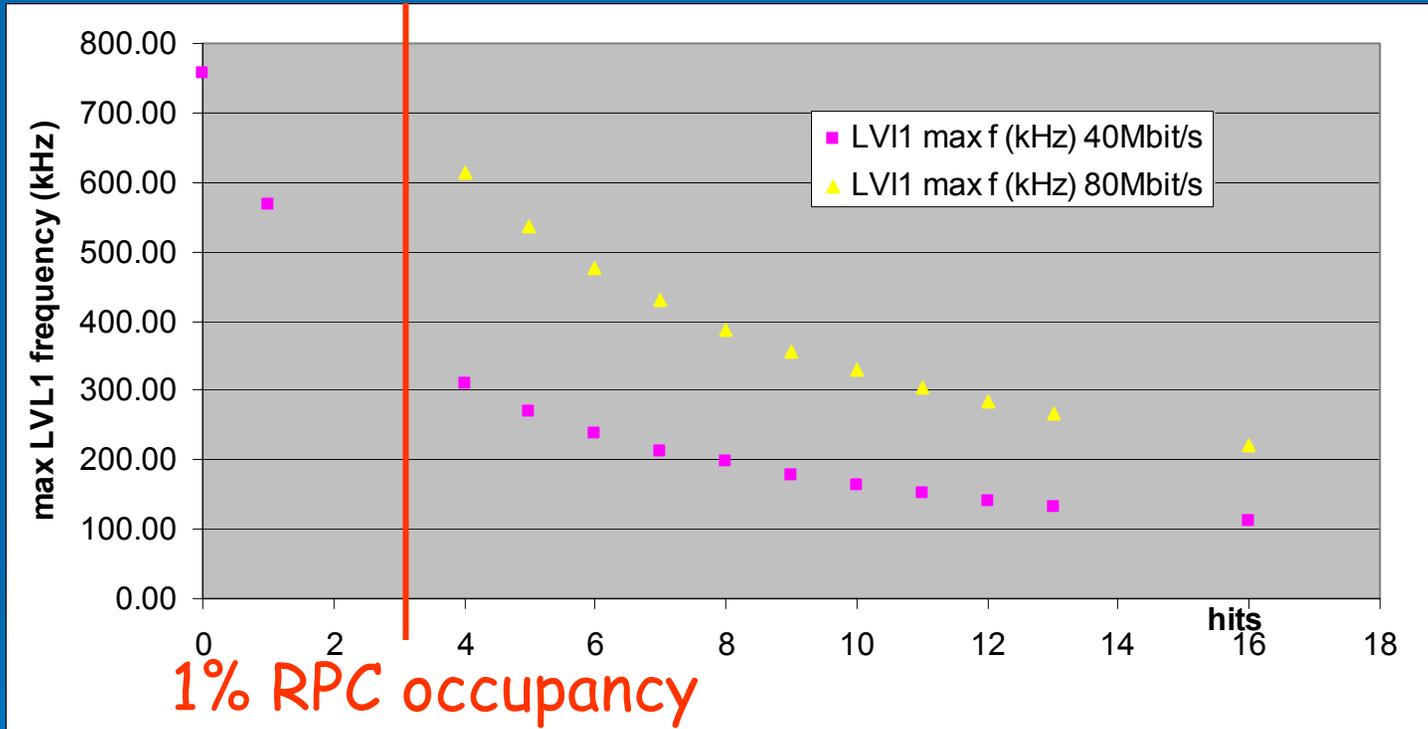
Power consumption

➤ **Nominal power consumption during normal run mode operation is ~1.2 W**

Power consumption vs. voltage

Power consumption vs. clock frequency
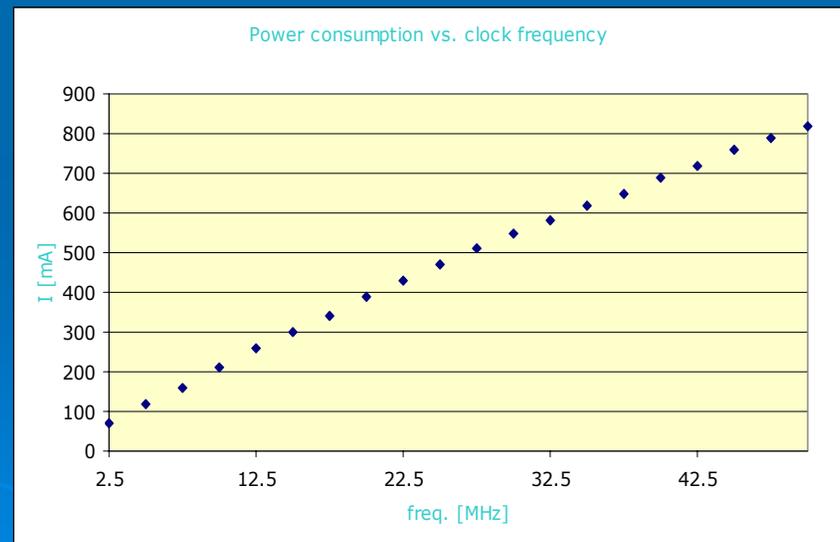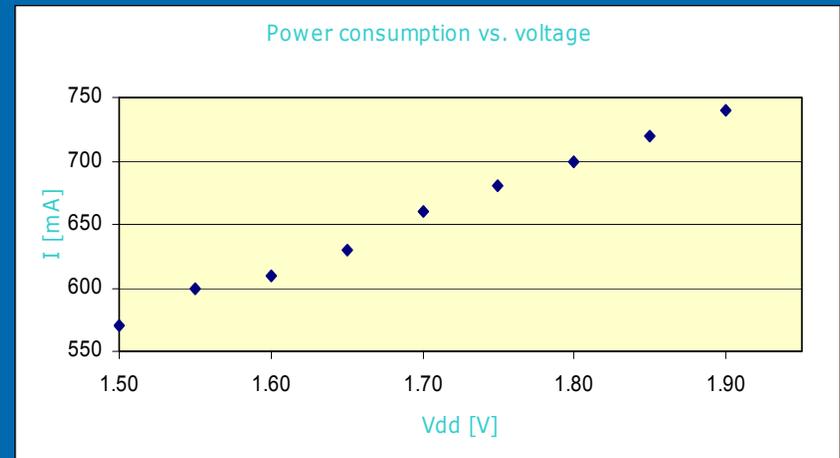
Plans & Conclusions

- Radiation Test:
  - 60 MeV proton SEE test
  - Gamma TID test
- Slice Test:
  - all slice components are now available
- Test Beam with RPC detector
  - muon beam with background photon source
- No problems or bugs founded up to now
- No second ASIC version previewed!