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The Alice Silicon Pixel Detector Readout System – Moving towards system integration

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Abstract

A number of key components have been designed, produced and tested for the readout system of the Alice Silicon Pixel Detector (SPD). This paper gives an overview of the system, describes the results obtained from the individual components as well as the software and hardware of the Data Acquisition System.

I. INTRODUCTION

The ALICE SPD is composed of two concentric barrel layers of pixel detectors, with radii of 3.9 and 7.6 cm [1]. The basic building block of the ALICE SPD system is the ladder, a high resistivity p^+ on n silicon detector of around 13 x 71 mm^2 that is bump-bonded to five Alice1LHCb pixel readout chips. Two ladders are connected together and then to a Multi Chip Module (MCM) by means of a special Pixel Bus to form a half stave (figure 1).

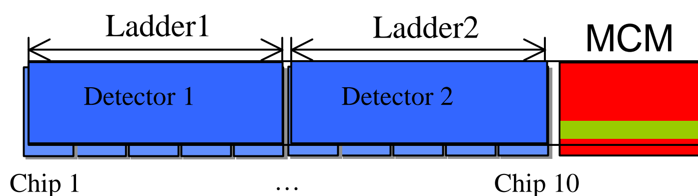

Figure 1: Two ladders connected to an MCM by means of a Pixel Bus forming a half stave

The MCM hosts three different ASICs: one for the biasing of the Alice1LHCb chip and for temperature and DC bias monitoring, one for digital read-out and one for data transmission. Two half staves form a stave, and six staves are mounted on a carbon fibre support to make a sector, with two inner staves and four outer staves. Ten sectors assembled together, as depicted if figure 2, form the SPD detector.

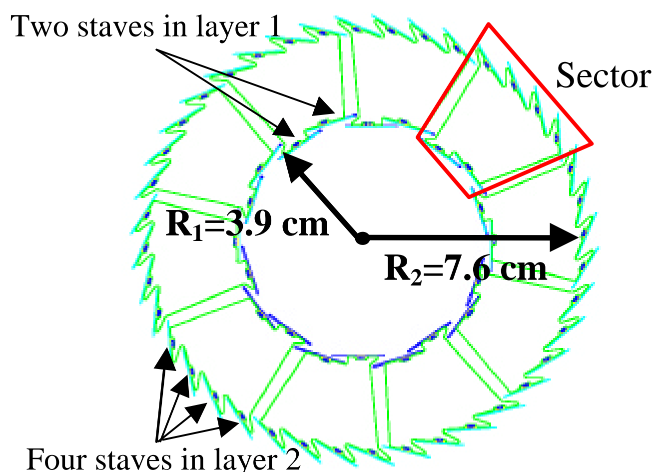

Figure 2: Cross section of the SPD detector, showing the ten sectors assembled together

II. TECHNOLOGY AND RADIATION TOLERANCE

The SPD is expected to receive a total ionising radiation dose of up to 5 kGy and a neutron flux (1 MeV equivalent) of $2x10^{12}n/cm^2$ in its ten years lifetime. For this reason, all of the ASICs in the SPD system were developed in a commercial 0.25µm CMOS using radiation tolerant layout techniques thus offering a high component density and an intrinsic radiation tolerance due to the thin gate oxide (t_{ox} ~5.5 nm) [2, 3, 4]. Measurements on transistors and chips implemented in the chosen technology and using the radiation tolerant layout rules confirm the almost negligible changes in transistor parameters up to very high doses [3]. Moreover some special digital design techniques were used to reduce the risk of Single Event Upsets (SEU) in the digital control logic [5]. The critical storage elements are triplicated and all outputs are the result of majority voting.

III. THE FRONT-END CHIP

A. The architecture of the chip

The pixel detector readout chip (Pixel Chip) was developed to serve two experiments, ALICE and LHCb [6]. The chip is a matrix of 32 columns each containing 256 readout cells, measuring 13.5x15.8 mm^2 (fig. 3).

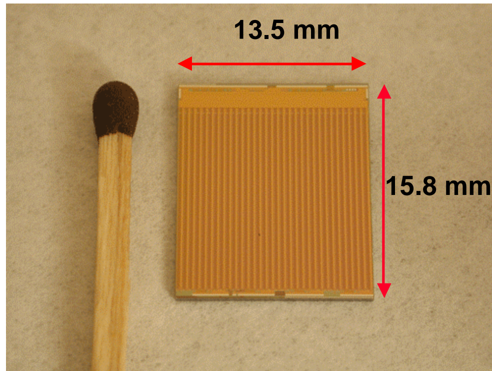

Figure 3: Picture of the front-end Pixel Chip

The analogue front-end of the pixel cell is composed of four main blocks: a charge preamplifier, a first shaping stage, a current feedback stage and a second shaping stage, which feeds a low time-walk discriminator. The first three stages constitute a system with two complex conjugate poles and a real pole. This solution was chosen instead of a standard charge integration and pole-zero cancellation scheme to achieve low noise and fast return to zero of the amplifier, avoiding pile-up effects in high rate environments. As a consequence the next hit on the same pixel can be processed after less than 200 ns. A low-frequency feedback is also present, to compensate for detector leakage current and correct for offset at the second shaping stage output.

The discriminator output is connected to some logic which stores a time stamp for the length of a trigger latency. When a stored event coincides with a trigger the event is stored in a FIFO. Up to 4 triggered events can be stored before readout is initiated. The cell also contains 3 bits to finely adjust the threshold on a pixel-by-pixel basis. An on-chip pulser allows electrical tests to be performed on the chip without a detector being attached. Measurements done with this pulser indicate a minimum operating threshold of ~1000 e-, with a dispersion of ~200 e- rms (unadjusted), and a noise of ~120 e- rms.

B. Radiation Tolerance

The radiation tolerance of the pixel chip has been extensively evaluated.

The effects of Total Ionising Dose (TID) were assessed by exposing the chip to 10 keV X-rays at a rate of 6 kGy/hour. As the beam spot was smaller that the chip two different positions of the chip were used, for a TID of 120 kGy in some zones of the chip, and 240 kGy in some others. After the irradiation the minimum threshold at which the chip can operate is unchanged (~1000 e- rms) and the pixel noise is still below 120 e- rms. The power consumption of the chip is unaffected by the irradiation [7].

The cross section for a Single Event Upsets (SEU) in the memory cells of the chip was measured in two different ways, with heavy ions with a Linear Energy Transfer between 6 and 120 $MeVmg^{-1}cm^2$ and with a 60 MeV Proton beam and a total fluence of $6.4x10^{12}cm^{-2}$. In the first case we extrapolated a SEU cross-section of $9x10^{-16}$ cm^2 for protons with energy of 60 MeV, in the second case we measured a cross section of $3x10^{-16}$ cm^2. No Single Event Gate Ruptures or Single Event Latch-ups were observed.

C. Wafer probing

A Karl-Suss PA200 probe station equipped with an 8" chuck was used to probe several wafers. A standard testing procedure has been established for the selection of Known Good Die (KGD) for bump bonding. The tests include: measurement of the power supply currents, JTAG functionality, DAC scans, configuration registers functionality, minimum threshold measurement and a full threshold scan. The chips are then sorted into three different classes, the first one containing the good chips for bump bonding. The yield of Class 1 chips changes from wafer to wafer and lot to lot from 35% to 75%, with an average yield of about 50%. Production testing is going to start in the coming months.

IV. BUMP BONDING AND ASSEMBLY TESTS

A critical process step for hybrid detectors is bump-bonding. The bumps have to provide electrical contact and mechanical stiffness, and have to withstand a certain amount

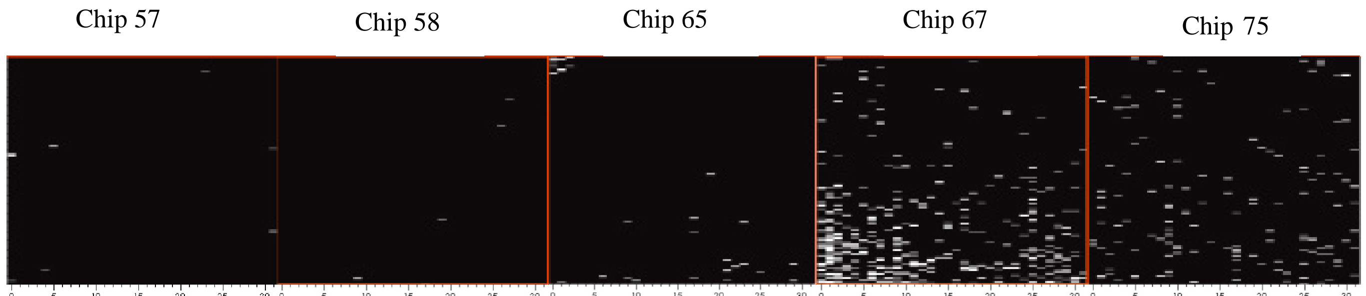

Figure 3b:Hit map of a test ladder with a Cadmium source. All chips have efficiency >98%, chip67 has an efficiency of 94%

of thermal cycling. Two different vendors, each with full 8" processing capability are being assessed. One of the vendors provides solder bump-bonding and the other uses Indium.

We recently received the first 5-chip ladders. The bump-bonding quality has been assessed using both Sr and Cd radioactive sources. The response of one ladder to Cd is shown in figure 3b.Note that the hit map has been normalised to 1. The 5 chips have 99.5%, 99.5%, 99.2%, 94.2% and 97.9% of working pixels, respectively. Efforts are now being concentrated on reduction of the thickness of the readout chips. The native wafer thickness is ~750 µm. Our target thickness for Alice is ~150 µm.

V. THE READOUT SYSTEM

A block diagram of the complete SPD readout scheme is presented in figure 4b. The block on the left is the Pixel Bus with the two half staves (10 pixel chips) and the temperature sensors added to monitor online the temperature variations. The centre block is the Pilot MCM. The third block shows a schematic view of the Control Room section, which will not be discussed in this paper. For more information, see [8].

A. *The Multi Chip Module (MCM)*

The MCM consists of four metal layers, two dedicated to power supplies and two for signal routing. It hosts three different chips (the Analog Pilot Chip, the Digital Pilot Chip and the Gigabit Optical Link), various passive Surface Mount Devices (SMDs) for biasing and decoupling, and laser and pin diodes for optical data transmission. The main components are described below. At present we have received the first prototype version of the MCM.

B. *The Analog Pilot Chip (APC)*

The Pixel Chip requires six external bias voltages; two are for reference for the GTL input/output logic, two provide reference voltages to the DACs and two are used for electrical testing of the chip. These biases are provided, for all the ten chips mounted on the same half stave, by the Analog Pilot Chip (APC), shown in figure 4. The APC is a mixed-mode IC containing the following blocks:

–Six 8-bit DACs, providing reference voltages to the Pixel Chip. The design is a modified version of the DACs used for the Pixel Chip itself. However, the reference voltages for these DACs are derived from an on-chip band-gap reference circuit[10].

–Four current sources designed to be independent of temperature and power supply variations. These provide currents which can be used by PT1000 devices for monitoring of the temperature of the stave.

–A 16-input analogue multiplexer followed by a 10-bit ADC, running at 10 MHz (designed by A.Rivetti [9]). These inputs are used to enable in-situ scanning and monitoring of the Pixel Chip and APC DACs. They can also be connected to the PT1000 outputs for temperature monitoring.

–A JTAG-controlled digital block, providing all the necessary control signals to the other blocks.

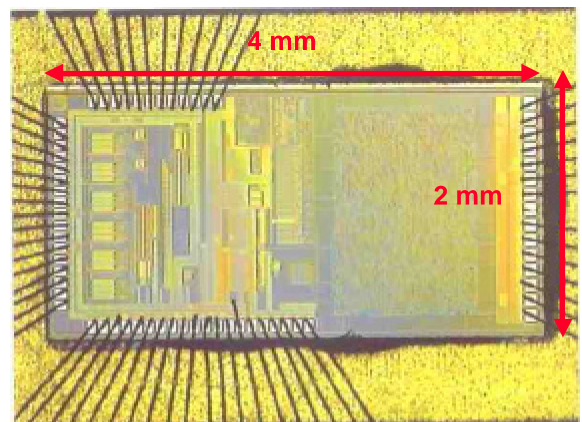

Figure 4: Picture of the Analog Pilot Chip

Until now only very preliminary tests have been performed. All of the DACs perform correctly but one of the six has an offset which is not yet understood. In any case it provides a sufficiently large dynamic range to be usable in its present form. The current sources for temperature monitoring are within the specifications. The JTAG interface is fully functional. The multiplexer and the ADC are currently under test, but first results show that they are functional. A final prototype will be submitted in 2003. At present, the inclusion of a fast ADC to digitise the analogue fast multiplicity signal generated by the Pixel Chips for trigger generation purposes is still under discussion.

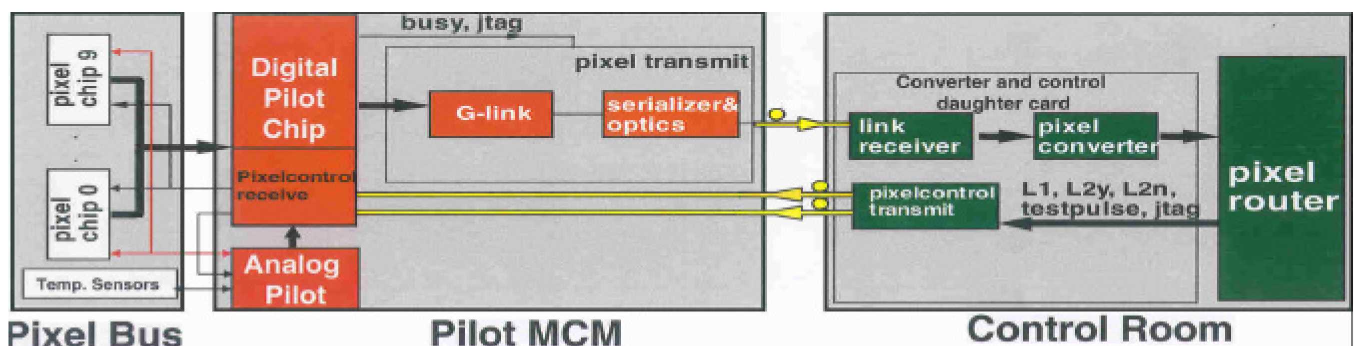

Figure 4b: Block diagram of the complete readout scheme

C. The Digital Pilot Chip (DPC)

The core of the MCM is the DPC (figure 5), as it controls all of the chips on the half stave, and readout of data from the Pixel Chips [8].

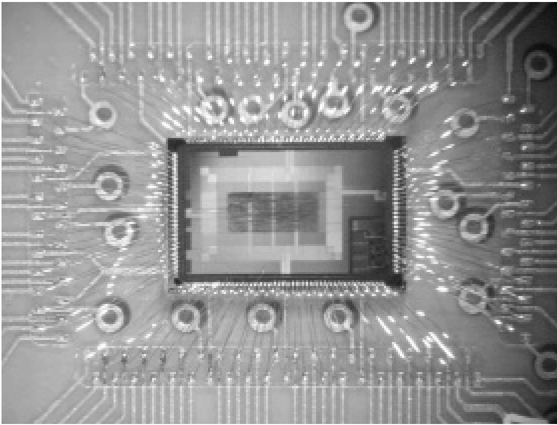

Figure 5: Picture of the Digital Pilot Chip

The link from the control room to the MCM is done via two fibers, one for data and the other for the clock. The use of this second fiber avoids the need for clock reconstruction on the MCM. On the data fiber the control room sends both configuration and test signals for all of the chips (mainly JTAG) and trigger information for the Pixel Chips. When the ALICE data acquisition issues a Level 1 trigger signal, the pixel router forwards the signal to the DPC, which asserts a strobe signal to all Pixel Chips. They store the delayed hit information into a multievent buffer, waiting for Level 2 (L2) trigger. If the pixel router sends an L2n, hit data are discarded from the Pixel Chips. If an L2y is asserted, the DPC starts the readout procedure of the 10 Pixel Chips one after the other. The 256 rows of 32 pixels of a pixel chip are presented on a 32-bit bus. The Pixel Chip data is then sent to the Gigabit Optical Link for encoding, serialization and transmission to the control room.

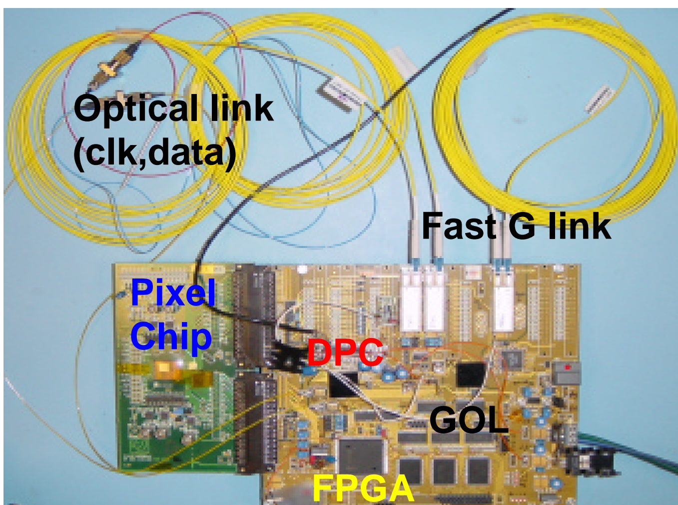

Figure 6: Picture of the Readout Test System Board

No data compression is performed by the DPC. Data processing units are located in the control room, allowing physical access and reprogrammability during the experiment.

A dedicated board was designed and produced to test the DPC (figure 6). The core of the test system is an FPGA that emulates the control room, all the other components of the half stave (but for the APC) are hosted on the test board. The FPGA can send/read control/hit data, and check data integrity at the end of the full test chain. Tests performed on the complete chain show that the system is fully functional.

D. The Gigabit Optical Link (GOL)

The connection between the MCM and the control room is done via a fast optical link. Hit and control data are generated by the DPC chip, which sends them to the GOL chip. The GOL chip multiplexes the data into a Glink compatible 800Mbit/s stream of data on an optical link to the control room. This chip was already developed and tested at CERN, and is fully functional [11].

VI. THE PIXEL BUS

The two ladders and the MCM are connected together by means of the pixel bus. A special kapton bus has been designed which uses Aluminium metal layers to reduce the material budget. The flexible bus has a total of seven layers of aluminium and a total thickness of about 240 m. The bus is glued on top of the detector, and the electrical connection with the Pixel Chips is done with wire bonds. SMDs will be placed on the bus for decoupling of power supplies. The bus is a complex technical development in the EST-DEM workshop at CERN.

Up to now we have successfully tested the first prototype version of the pixel bus with 10 chips mounted on it in the laboratory (it is shown in figure 7, glued on a dedicated test board). Moreover, a ladder was mounted on an identical bus and this was used in the test beam in 2002. At present, we are waiting the second prototype version of the bus.

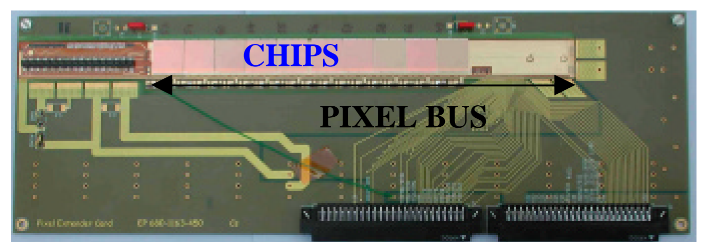

Figure 7: Picture of the test board with the first prototype Pixel Bus with ten chips glued and wire bonded.

VII. THE PIXEL TEST SYSTEM (PTS)

The test system [12] has been designed around a PC connected with a MXI connection to a VME crate. A Readout Controller (PILOT Module) has been developed in the VME

standard to control the readout of the Pixel Chip. As the Pixel Chip is configured and controlled by JTAG, JTAG is also used to control a DAQ Adapter board that is situated close to the Pixel Chip under test. Differential connections between the modules installed in the VME crate and the DAQ Adapter board allow the use of long interconnecting cables making the system suitable for use where the readout/test system must be sited far from the Pixel Chip or chips.

The test software architecture (based mainly on Windows and LabView) reflects the flexibility of the hardware. Its modularity and architectural structure guaranties that the system can be used with different hardware configurations without the need of rewriting the software core. The test beam DAQ and monitoring program is the most powerful part of the PTS. A single application enables the acquisition of data in a variety of conditions, and some plug-ins are loaded on demand to perform specialised tasks (e.g. checking of trigger efficiencies). The test system proved to be extremely robust and flexible, and was used with great advantage in a number of tests: single chip electrical tests, single chip assembly tests with radioactive source, ladder testing, wafer probing, pixel bus studies and test beams.

VIII. TEST BEAMS

Several single assemblies and ladders were tested during three test beams at the CERN SPS, the first two in July and September 2001, with a beam of 150 GeV pions, and the third one in September 2002 in a beam of 350 GeV protons. In all tests four scintillators were used to select a beam spot of about 2x2 mm^2. During the first two test beams we used three detector planes with single chip assemblies [7,13], and tested mainly chip efficiency, timing and threshold scans. In 2002 five planes of pixel chips were used: two groups of closely spaced single chip assemblies plus (in the middle) the device under test (DUT).

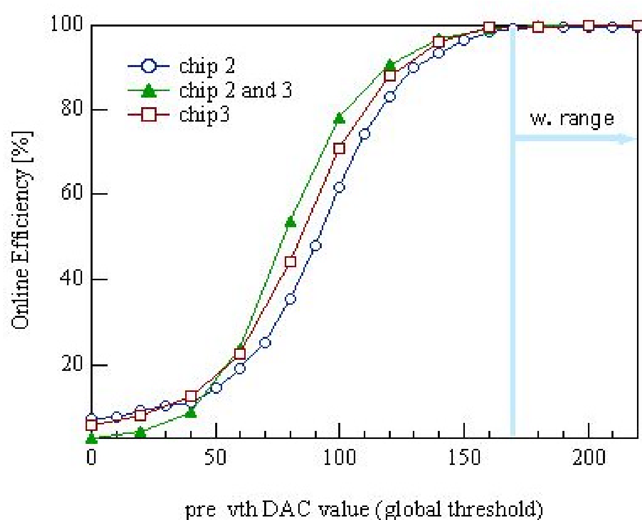

Figure 8: Online efficiency of two chips in a ladder.

The DUT was placed on an X-Y table, to expose different zones of the chip to the beam. It was also possible to rotate it, to study the efficiency and cluster size as a function of the incident angle of the particles. During the latest test beam we tested successfully a thick assembly (with a detector 300 m thick), a thin assembly (200 m) and a thick ladder.

As an example, in fig. 8 is shown the online efficiency of two chips of a ladder as a function of the pre_vth DAC value. This is the DAC that sets the global threshold in the chip; the region on the right of the picture is the region within which the chip will be operated. Similar measurements were obtained with thin detectors. In all cases full detection efficiency was achieved over a long plateau in threshold.

IX. CONCLUSIONS

All the components of the SPD half stave have been produced, even if they are still in prototype version. All the tests performed up to now are very promising, and confirm their functionality. The first steps towards system integration are underway, and we were able to operate 10 chips together on a dedicated Pixel Bus, and a ladder on the bus during a test beam. The test system proved to be extremely robust and flexible, and was used with great advantage in a number of tests both in the laboratory and in the test beam.

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