The CMS Microstrip Silicon Tracker System Tests

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Abstract

The CMS Microstrip Silicon Tracker is approaching the production and construction phase. The first sub-units of the Tracker are being built in their final configuration in order to undertake a series of tests intended to qualify the entire system. The functionality of the whole system, (read-out, control, data acquisition) is being tested carefully both from the hardware and software point of view, the hardware architecture being in its final version and the software architecture very close to the final one.

A review is given in this paper of the status of the activity. Some of the relevant tests and results obtained so far are shown.

I. INTRODUCTION

The CMS Microstrip Silicon Tracker is divided into three main distinct units, the Inner Barrel, the Outer Barrel and the two End-Caps, each of them having its own geometry. The Inner Barrel (TIB) is composed of four cylindrical layers built with shell mechanics and it is divided in two at z=0. Each half contains 6 detectors in z (300µm sensors). The Outer Barrel (TOB) is composed of six layers built from multi-module units ("rods") each layer being made of two rods in z, each rod containing 6 detectors (500 µm sensors). The End-Caps (TEC) are made of nine wheels each composed of eight petals. The sensors are arranged on the petals to form rings (a maximum of 7 in the biggest wheels next to the barrel, a minimum of 4 in the smallest wheels). The three outermost rings are equipped with 500 µm sensors. A detailed description of the Tracker design and expected performance can be found in [1].

While the tracker is geometrically divided into three parts, it has a uniform read-out and control scheme as well as powering. The read-out and control system for the CMS Tracker is a relatively complex design to cope with the new and extremely hostile LHC conditions. A sketch of its architecture is shown in Fig. 1. It is a huge system of about 20,000 detectors corresponding to about 10M read-out channels. The read-out of the system is based on about 80,000 front-end chips, 50,000 analogue optical links and about 440 Front End Drivers. The control of the system is based on about 50 Front End Controllers, 2000 digital optical links and about 2000 CCUs.

The electronic challenges for the system are principally to ensure low noise during the entire operational lifetime, along with adequate bunch crossing identification, which is ultimately limited by the speed and amplitude of signals coming from the detectors as well as by electronics.

The detector modules are equipped with front-end hybrids housing APV25 chips [2] for analogue read-out. The analogue outputs from two chips are multiplexed on a single line to the opto-hybrid [3] where the signal is converted from electrical to optical and distributed via fibre [4] to the DAQ interface card (FED) [5] in the control room. At the FED input optical receivers provide the optical to electrical conversion. Signals are then digitised, zero-suppressed and sent to the DAQ.

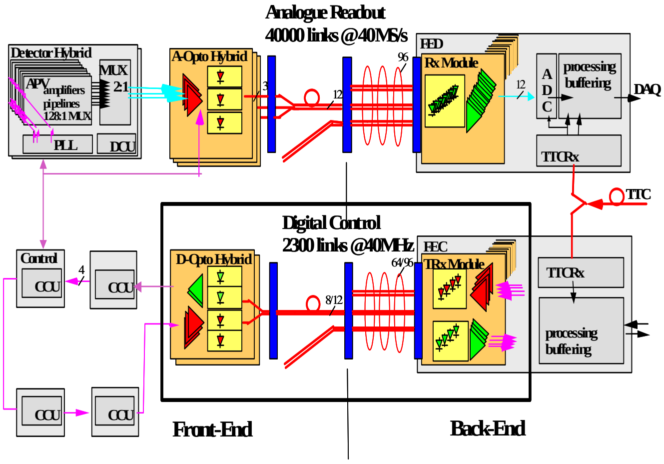

Figure 1: Schematic view of read-out and control architecture for the CMS Tracker.

The timing and control path is separated from the readout path in order to ensure that control and monitoring are totally independent from the DAQ system. The Front End Controller module (FEC PCI card) [6] takes care of: -

a) interfacing with the Timing, Trigger and Control system [7] and distributing the encoded clock and trigger signals to the front-end, and

b) setting and monitoring via I^{2}C protocols all the parameters (e.g. bias voltages on APV25s, delays on PLLs, etc.) needed to operate the system.

The communication architecture in the slow control system is based on a 'token-ring' protocol, which connects the FEC to the Communication and Control Units (CCUs) and a 'channel' protocol, which connects each CCU with the front-end chips. The digital control and timing signals are distributed from the FEC to the front-end via digital optical links [8].

The overall status of the Tracker electronics is well advanced; the design of all ASICs is definitive and pre-production orders have been placed for them and optical links, both digital and analogue. The design and definitive choice of the front-end hybrids is still on-going [9]. On the DAQ side, the first prototypes of the final production version of the Front End Driver, (96 ADC channel, 9U VME64x form factor card), are about to be manufactured while the final version of the Front End Controller has been defined and the final radiation-hard version of the Communication and Control Unit (CCU25) has been built in deep sub-micron technology [10]. Finally, prototypes for power supplies are under evaluation.

Software development is recognised to be a large task but is progressing well.

A. Definition of System Test

All components of the Tracker system have been individually tested and qualified. However, during the pre-production phase, testing the whole system is mandatory to verify the overall design and correct possible faults, if they exist, before launching production. The goal is to build a complete sub-unit for each of the three components of the Tracker (TIB, TOB and TEC) i.e.

a) Integrate the sensors with front-end electronics and the necessary interconnecting boards and buses in the final mechanical supports ;

b) Integrate the full optical link distribution of the signals, for both control and read-out;

c) Integrate power supplies, both for High and Low Voltages, in conjunction with the use of long cables;

d) Set-up the cooling facilities.

In order to fully validate the system a long series of checks must be performed. From the mechanical point of view, the compatibility of the various components has to be verified, including effects on modules due to mechanical stress. Since the Tracker is meant to work at –10°C, possible deformations due to cooling also have to be measured.

After integrating modules, interconnect cards and buses in the mechanical supports, the next step is to perform electrical tests to verify the integrity of signals during transmission between cards, in particular timing and control signals around the control loop, these being critical for correct functioning of the system. A very delicate point is also uniformity in the LV power supply distribution, whose requirements are variations less than ±5% for the ASIC LV 2.5V and 1.25V supplies. On the read-out path there are many issues to be taken into account. Tuning of the analogue-optical link is the first essential step; this involves adjustment of the phase of the clock on the FED with respect to the incoming data in order to choose the best sampling point on the signals, to allow for sufficient settling of the analogue output. In Fig.2 the synchronization pulses of the APV are shown, as reconstructed after digitisation, by sweeping the available delays in steps of 1 ns. Since two APVs are multiplexed onto a single line and the outputs of the two chips are interleaved, the synchronization pulse is 50 ns wide. The optimal sampling point sits on the plateau a few ns before the falling edge.

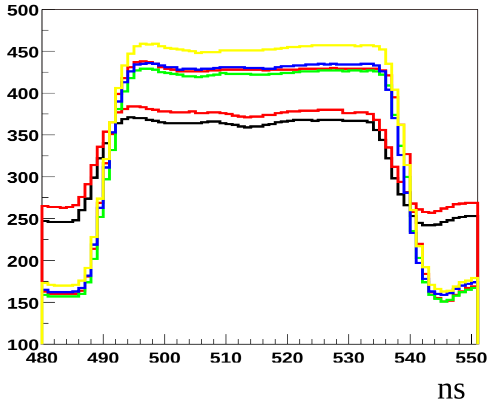

Figure 2: APV25 synchronization pulses seen from the DAQ by sweeping the delays in 1 ns steps.

Bias and gain of the links also need to be optimised taking into account the dynamic range at the input of the FED[5]. Only then can contributions to noise and common mode effects be studied.

One of the setting-up operations necessary in order to make reliable tests, is the relative synchronization of the APVs and hence of the modules. APVs on the same hybrid are synchronous by construction since they share a common local clock. APVs belonging to different modules within a ring or in different rings reside at different places in the timing and trigger distribution path. In order to acquire data from the same event the delay (PLL units) have to be tuned in order to ensure the signals are correctly synchronized with the clock and trigger.

Finally tuning the front-end chips to optimise the signal pulse shaping is required. A pair of internal bias parameters, which are temperature dependent, have to be set so that the output from the shaper stage on the chip provides the correct rise and decay time.

Only after the setting up is complete and checked, can analysis of data from the sensors be carried out in a reliable way. All the measurements, especially the signal to noise ratio, have to be performed in a controlled environment where temperature and humidity are monitored and stable and, in a second step, at the working Tracker temperature of –10°C.

II. GENERAL INTEGRATION ACTIVITY AT CERN

The integration of the CMS Tracker electronics has been under way for the last couple of years, mainly at CERN, causing some modifications to the design of a few components. Since not all components were available in their final form at the start, iterative progress has been necessary to build systems with increasing levels of complexity. Nevertheless this has allowed to qualify the components and to design and build software necessary to control, read-out and commission the system, as well as to start implementing calibration and synchronization procedures. The objective is that most of them should eventually be fully automatic. An example is shown in Fig.2. The APV synchronization pulses can not only be used, as previously explained, to find the best sampling point on the analogue output; the difference in their arrival time at the FED input gives a measure of the delays between modules. This procedure is automated, although it needs to be scaled to larger systems where analogue fibres have different lengths and more than one FEC is included.

In the most recent beam-test, actually under way while this paper is being written, a system fully equipped with digital and optical links has been tested. It is composed of six TOB modules connected in a control ring as shown in Fig.1. Six final prototype analogue opto-hybrids with final laser drivers and lasers transmitters, with miniature connectors, have been used. A prototype (single-fibre to 12 way ribbon) optical fan-out is used in conjunction with the final prototype Multi-Ribbon Cable (12-way ribbon) to deliver the analogue signals to a prototype Analogue 12-channel receiver module. Since the FED used is a prototype temporary PCI Mezzanine card (8 ADC channels)[11] the receiver has been mounted on a single-ended to differential converter board to interface to the PMC FED.

Controls and DAQ are performed housing the FEC and two FEDs in two separate PCs.

High quality data have been taken. In Fig.3 Landau distributions are shown for all modules. The signal over noise measured is very satisfactory, the average value being 30 and 18 with APVs operated in peak and deconvolution mode respectively [2]. It is in agreement with that expected from the APV noise dependence on input capacitance and the total effective coupling for the sensors under test. The result obtained agrees with that previously measured using electrical connection to the FED.

III. OUTER BARREL SYSTEM TEST STATUS

One complete rod of the Outer Barrel has been built and is under test. Preliminary checks on mechanics and on interconnections have been successful. The design of the rod has been validated and is final. The whole system is now being tested with a β-source in a controlled environment.

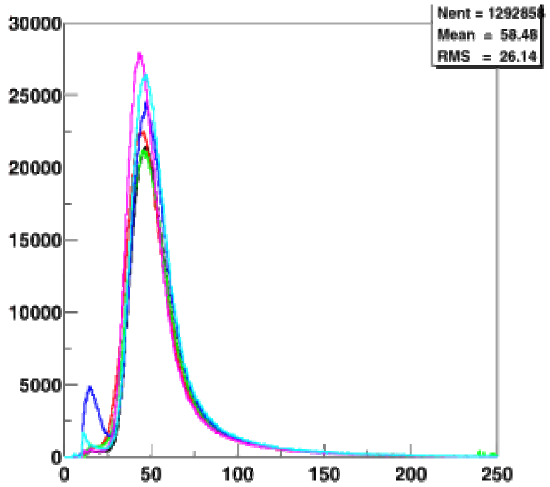

Figure 3: Landau distributions for the recently built six TOB modules qualified on the beam.

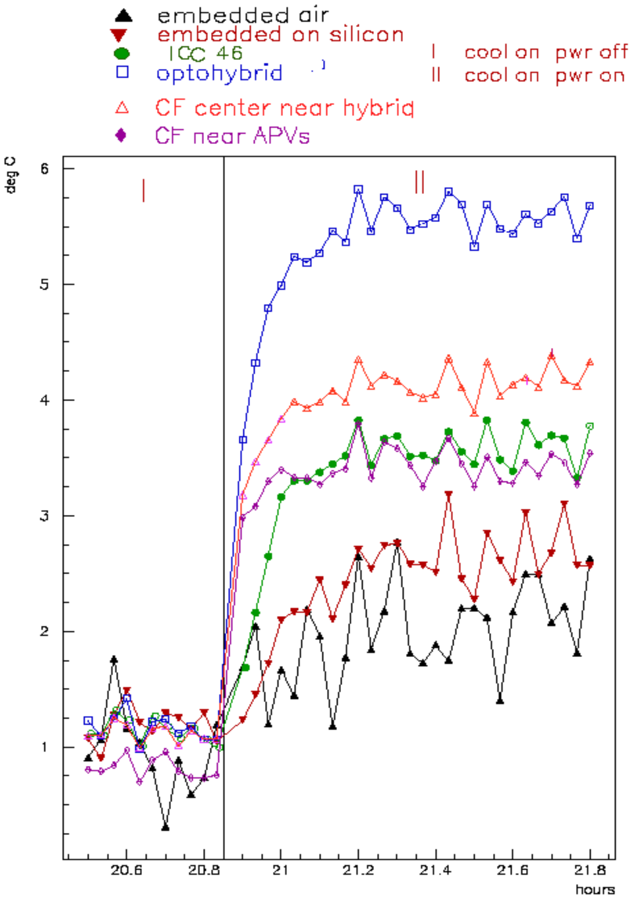

Figure 4: Temperatures of the various components along the rod in function of time. The temperature of the cooling pipe (about 19°C) is subtracted.

A cooling system has been setup to keep the temperature constant at about 24°C. The result of the temperature monitoring (Fig.4) shows that the opto-hybrid is the hottest element in the chain.

A grounding scheme resembling the final one has been adopted in order to perform reliable measurements.

Preliminary measurements of noise and signal over noise are encouraging as shown in Fig. 5 and 6, which display data for one of the six modules in the rod.

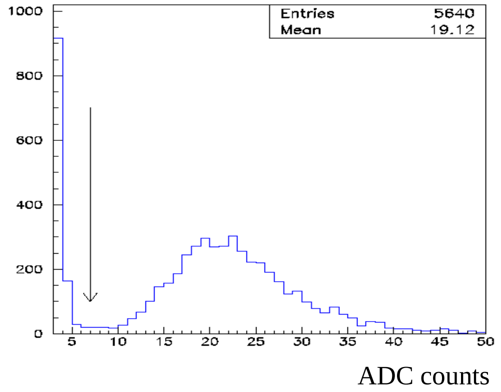

Figure 5: Signal over noise ratio measured with the largest reconstructed cluster. The APVs are operated in peak mode.

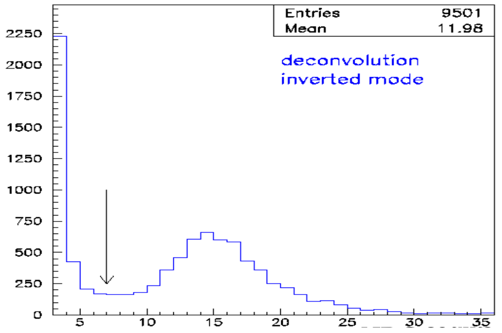

Figure 6: Signal over noise ratio measured with the largest reconstructed cluster. The APVs are operated in deconvolution mode.

In Fig.7 and Fig.8 the noise and the profile of the signals along the same detector are shown.

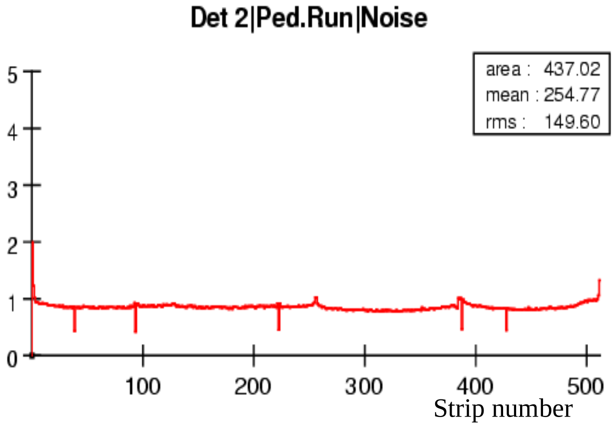

Figure 7: Noise of the same module referred to in Fig.5, 6.

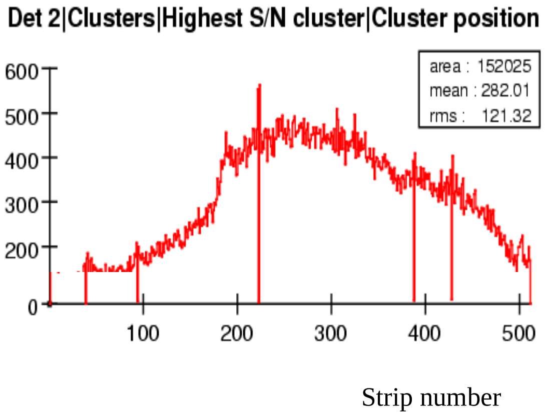

Figure 8: Profile of the cluster position along the module (512 strips).

IV. INNER BARREL AND END-CAPS SYSTEM TEST STATUS

The tests of the Inner Barrel and the End-Caps are at a slightly less advanced stage but in progress. A few TIB modules with optical read-out, have been tested individually. The TIB also confirms no substantial difference in the final signal to noise ratio compared with previous tests carried out with electrical read-out. The design of the mechanics (cylinders) is frozen and a prototype is under construction. The first electrical and mechanical integration is planned in the next couple of months.

The design of the TEC mechanics (petals) has been verified and the basic electrical checks on the interconnecting boards and buses as well as on the control links have already been successfully performed. Over-voltage measurements (which could occur due to the inductance of long cables and the slow reaction time of the power supplies) have been carried out, using a commercial power supply and a 100m long cable. Fig. 9 shows that the over-voltage can be controlled with suitably chosen value of a damping capacitance on the interconnect boards. The over-voltage excursion measured with the largest damping capacitance and switching on four front-end hybrids, is larger than required (Fig.10) and represents a potential problem. However, it appears that the response time of the power supplies can be shortened and a radiation hard protection circuit based on regulators developed for LHC can be installed to provide extra protection.

TEC detectors have different geometrical configurations depending on which ring of the wheel they belong. A series of system tests for each of them is expected to take place and give results by the end of 2002.

V. CONCLUSIONS

System tests for the CMS Microstrip Silicon Tracker are in progress for each of the three components, Inner

Barrel, Outer Barrel and End-Caps. The results obtained so far from close to final modules are encouraging even though further work is needed especially in implementing grounding and shielding schemes. A grounding plan has been devised which will be fully evaluated when the final power supplies are available.

Final results from all kind of detectors are expected by Spring 2003.

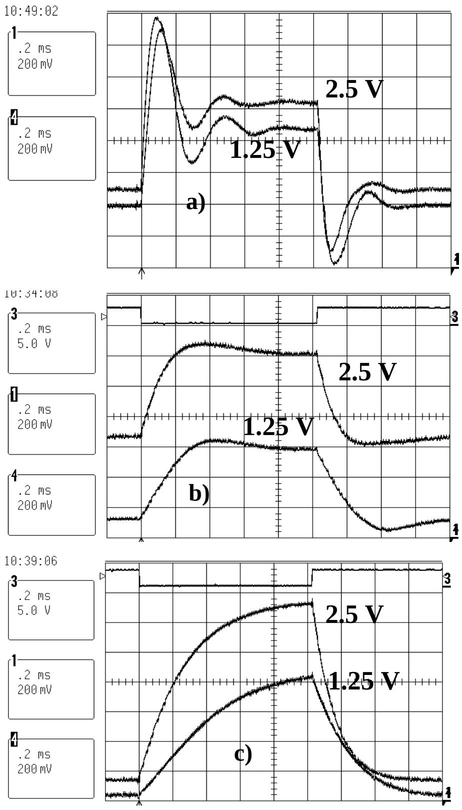

Figure 9: Over-voltage swing measured on the TEC petal interconnecting bus. a) C250 = 60 µF, C125 = 40 µF, b) C250= 330 µF, C125 = 330 µF and c) C250 = 740 µF, C125 = 740 µF.

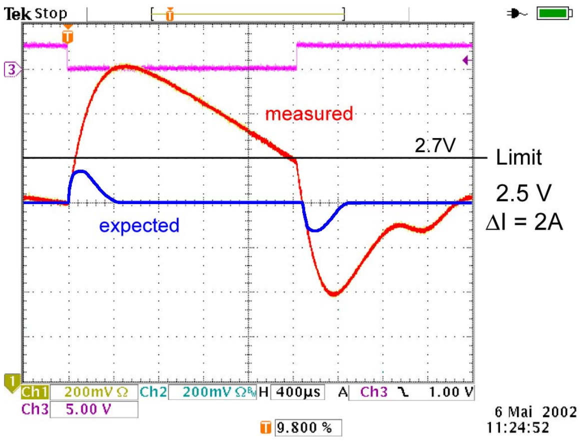

Figure 10: Over-voltage gradient measured with TEC hybrids.

VI. ACKNOWLEDGMENTS

The author would like to thank all members of the CMS Tracker Collaboration involved in this work and acknowledge the financial support from the UK Particle Physics and Astronomy Research Council.

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