OTIS – A Radiation Hard TDC For LHCb

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Abstract

For the outer tracker of the LHCb experiment the OTIS chip is developed at the University of Heidelberg. A first full-scale radiation hard prototype of the chip has been submitted in April 2002. The OTIS chip is a 32 channel TDC (Time to Digital Converter) manufactured in a standard 0,25µm CMOS process.

Within the clock driven architecture of the chip a delay locked loop (DLL) provides the reference for the drift time measurement. The drift time data of every channel is stored in the pipeline memory until a trigger decission arrives. A control unit provides memory and trigger management and handles data transmission to the subsequent DAQ stage.

This paper introduces the design of the OTIS chip and presents first measurement results with the prototype chip OTIS 1.0.

I. INTRODUCTION

In the LHCb experiment the signals from the straw tubes of the outer tracker are digitised with discriminator chips of the ASD [1] family. The OTIS TDC measures the arrival time of those signals with respect to the LHC clock. The drift time data of 4 chips is then combined and serialised with the GOL chip [2] and optically transmitted to the off detector electronics at 1.2 Gbit/s net data rate (see figure 1).

The architecture of the OTIS chip is clock driven: the chip operates synchronous to the 40MHz LHC clock. Thus the chip's performance can not be degraded by increasing occupancies. Main components of the OTIS chip are the TDC core - consisting of DLL, hit register and decoder - the pipeline plus derandomizing buffer and the control circuit. The memory cells are dual ported SRAM to cover the L0 trigger latency [3] and to cope with trigger rate fluctuations. A control algorithm provides memory and trigger management and

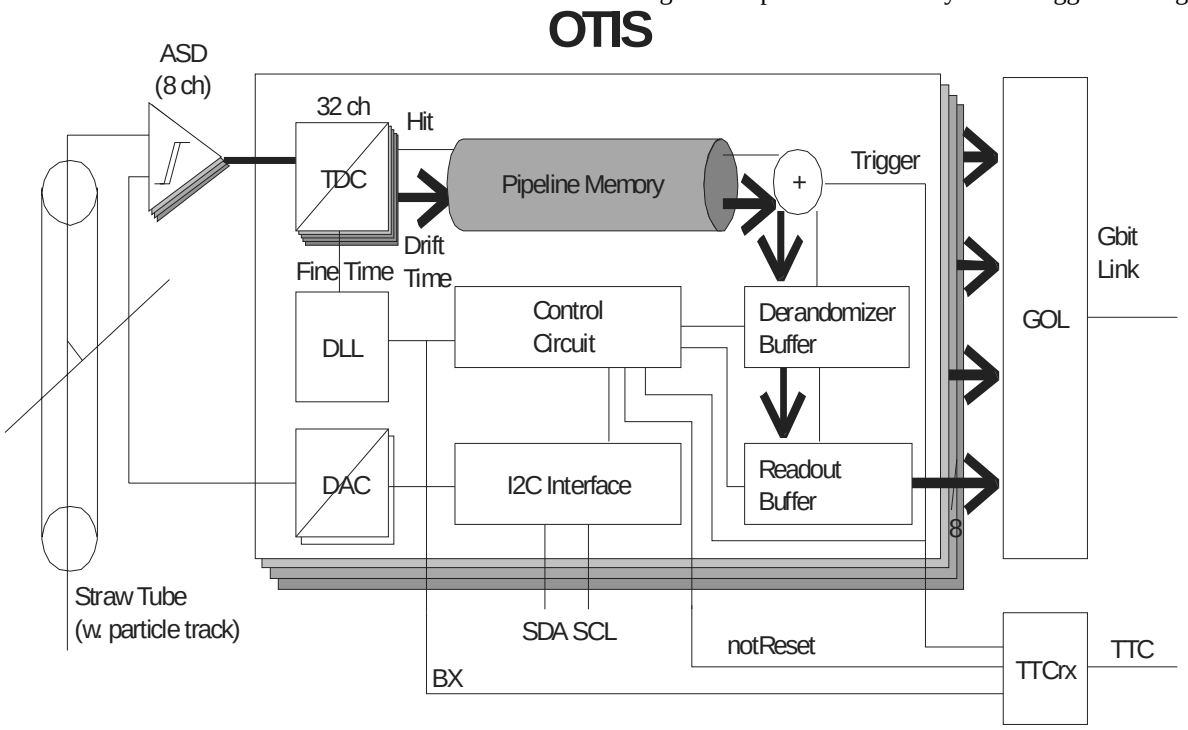

Figure 1: Outer tracker front end electronics

handles the output data stream. In addition the chip integrates several DACs (digital to analog converter) providing the threshold voltages of the ASD discriminator chips and a standard I^2C [4] interface for setup and slow control.

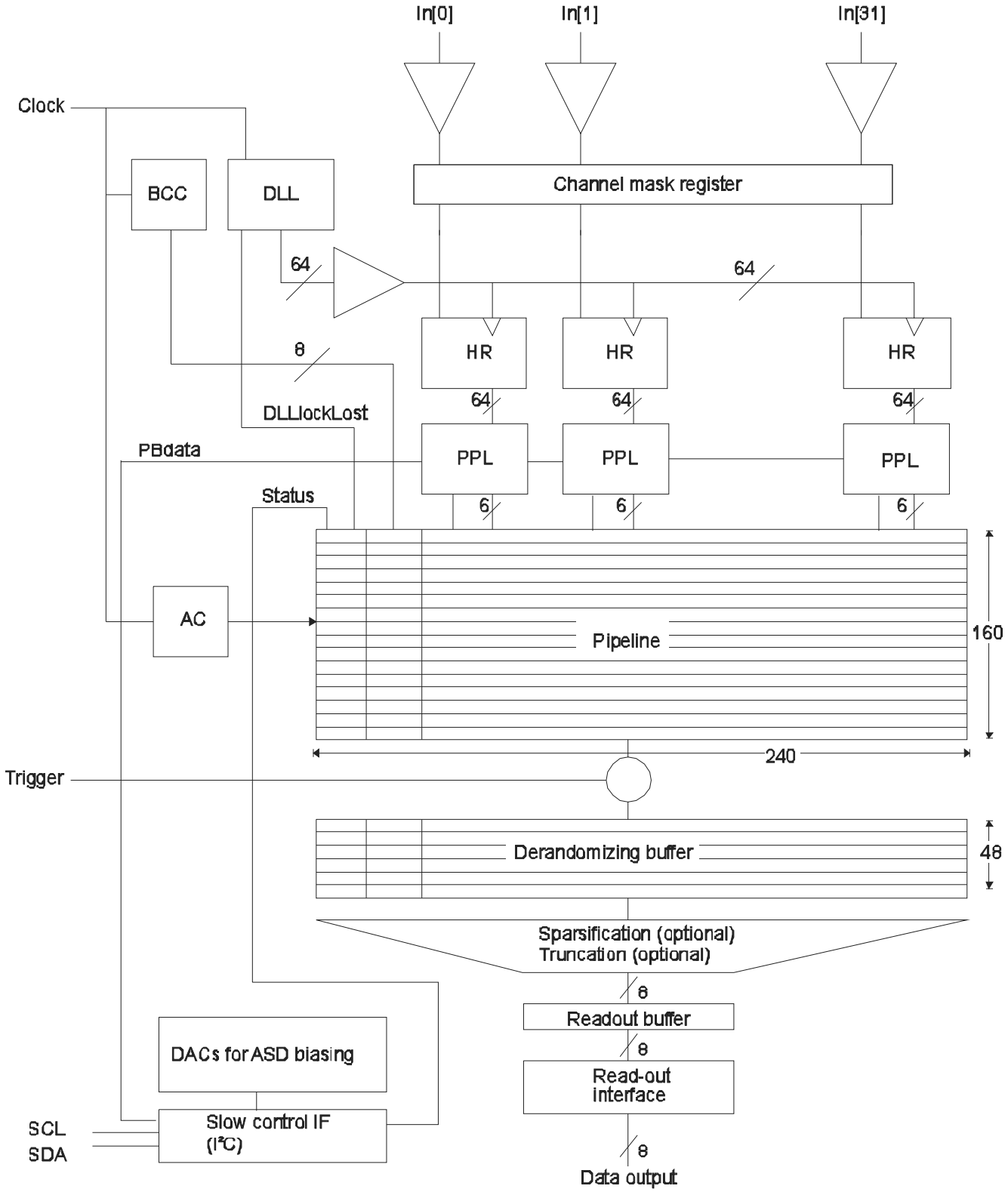

Figure 2: OTIS1.0 block diagram

II. Chip Architecture

A. The TDC Core

The TDC core, consisting of DLL, hit register and decoder, performs the drift time measurement. Therefore the DLL consists of a chain of voltage controlled delay elements through which the LHC bunch crossing clock propagates. The phase detector of the DLL then compares original (undelayed) clock and propagated clock. Depending on the phase between these two clock signals, a charge pump adjusts the delay elements until LHC clock and propagated clock are in-phase. In this state, called lock state, the reference signals for the drift time measurement can be obtained from the 64 delay elements providing a nominal resolution of 390ps. These reference signals are then used to latch the discriminated detector signals into the corresponding hit registers. The hit register holds a picture of the detector signal from which the 6 bit drift time is encoded.

A test chip containing the DLL and hit register was produced in advance. This test chip was fully functional and a differential nonlinearity of 0,51 ± 0,03 LSB was obtained.

B. Pipeline and Derandomizing Buffer

Pipeline and derandomizing buffer are realised as arrays of dual ported SRAM cells. Their dimensions are 164x240 bit and 48x240 bit respectively. Every clock cycle a new data set, consisting of drift time data, bunch crossing number and status information is stored into the pipeline. The pipeline is able to hold 164 data sets to cover the 4µs L0 trigger latency. Upon a trigger the corresponding data sets are copied to the derandomizing buffer, which is able to hold data sets representing 16 triggers.

Also for memory and derandomizing buffer a test chip was produced in advance. It was fully functional and the memory cells were found operatable up to 2,5 times the design frequency of 40 MHz.

C. Control Algorithm

The control algorithm provides trigger and memory management as well as the control of the data output stream. The hardware description language *Verilog* was used to code the algorithm, and apart from extensive simulations the most important parts of the code were tested on an FPGA.

Caused by the long drift times, which are up to 50ns, the control algorithm can search detector signals within 3 data sets for each trigger, representing 3 bunch crossings. But for each channel, only the first hit found within the 3 data sets will be transmitted. This way the OTIS chip acts as a single hit TDC. Two additional bits are used to indicate the bunch crossing the detector signal was found in.

Upon a trigger data transmission starts with 4 header bytes followed by 32 bytes representing the drift times for each channel. The header bytes contain chip ID, status information and the actual bunch crossing number. Table 1 shows how data is organised within a read out sequence. Table 2 indicates how the extended 8 bit wide drift time is composed of the signal's drift time (6 bit) plus its position within the search window of up to 3 bunch crossings (2 bit).

Table 1: Data output sequence

Bit	0 .. 31	32 .. 39	…	28 .. 287
Data	Header	Drift Time 0	…	Drift Time 31

Table 2: Extended drift time

Hit Position	Data
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	1100000000

In addition to the normal operation mode, the control algorithm provides the possibility to bypass the drift time measurement unit and to insert arbitrary drift time data into the pipeline. This play back mode is usefull to test the data path independent from the detector or the TDC core.

III. Measurements

The following sections summarize some of the measurements with the OTIS1.0 prototype. Since the chip is under test for only 6 weeks, these are preliminary results.

A. Power Consumption

After powering the chip, it performs a power up reset. In this state power consumption is 465mW. The power consumption increases to 550mW when operating at the nominal clock frequency of 40MHz.

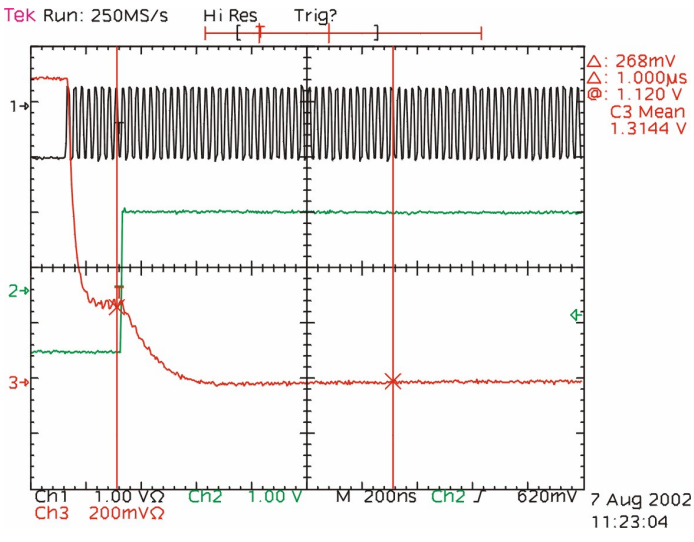

Figure 3: DLL lock time

B. DLL Lock Time

While the chip is resetted, the charge pump which adjusts the control voltage of the delay elements gets precharged. Figure 3 shows that after the reset signal (channel 2 in the diagram) is released the control voltage (channel 3) reaches a stable value within less than 1µs. In this state the DLL is locked.

C. Control Algorithm

First functionality tests with the control algorithm of the OTIS1.0 prototype chip show no unexpected behaviour. The control algorithm performs correct memory and trigger management and all triggered read out sequences show the correct timing, i.e the length of the read out sequences is 900ns.

All debug signals that are included in the prototype chip, such as the zero crossing of the memory pointer or the derandomizing buffer full and empty signals show the expected behaviour.

With the play back mode, which is also fully functional, it was possible to verify the correct encoding of header data and drift times.

D. Fine Time Measurement

The measured fine times are expected to follow the detector signals position within a bunch crossing linearly. But first measurements show an unexpected behaviour of the measured fine times. Figure 4 shows the measured fine times of a single channel as a function of the signal's position within the bunch crossing.

A simple workaround which can be used to procede with the measurements is to send two consecutive hit signals with exactly the same relative timing with respect to the 40 MHz clock. Figure 5 depicts the fine time measurement of such a double hit. The measurement shows the expected linear relation between hit position and fine time.

Since the problem of the fine time measurements is not yet completely understood all the results presented in this section are considered preliminary.

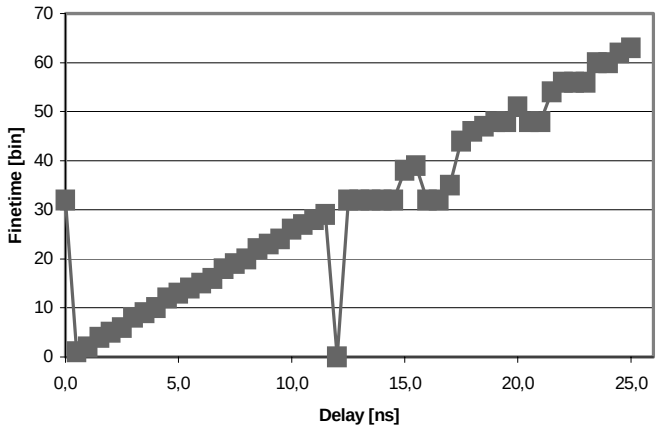

Figure 4: Fine time vs. hit position (single hit)

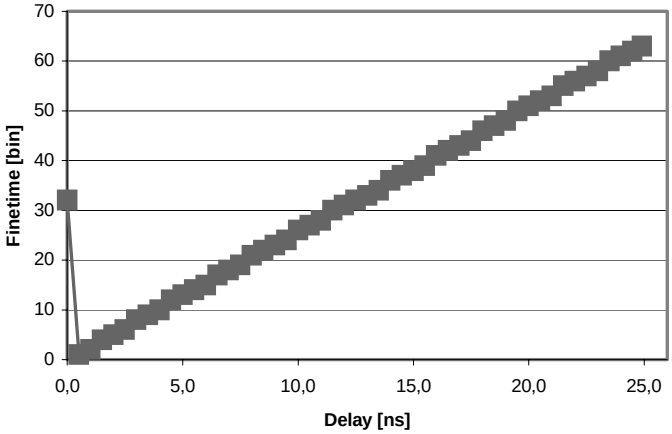

Figure 5: Fine time vs. hit position (double hit)

IV. Conclusions

A first full scale prototype chip OTIS1.0 for the outer tracker of the LHCb experiment was submitted in April 2002. It complies with the LHCb specifications and provides basic functionality.

First measurements show correct behaviour of the DLL, pipeline and derandomizing buffer and control algorithm. The TDC shows an unexpected behaviour within the drift time measurement unit, which is not yet fully understood.

V. References

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