Fast CMOS Transimpedance Amplifier and Comparator circuit for readout of silicon strip detectors at LHC experiments.

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Abstract

We present a 64-channel front-end amplifier/comparator test chip optimised for readout of silicon strip detectors at LHC experiments. The chip has been implemented in radiation tolerant 0.25 µm CMOS technology. Optimisation of the front-end amplifier and critical design issues are discussed. The performance of the chip has been evaluated in detail before and after X-ray irradiation. The basic electrical parameters of the front-end chip like shaping time, noise and comparator matching meet the requirements for fast binary readout of long silicon strips in the LHC experiments.

I. INTRODUCTION

Development of front-end electronics for readout of silicon strip detectors in the experiments at the LHC has reached a mature state. Complete front-end readout ASICs have been developed for silicon trackers in both large experiments, ATLAS and CMS. Progress in scaling down CMOS technologies opens, however, new possibilities for front-end electronics for silicon detectors. In particular, CMOS devices can be now used in the areas where in the past bipolar devices were definitely preferable. These technologies offer possibility to obtain very good radiation hardness of circuits by taking advantages of physics phenomena in basic devices and implementing special radiation tolerant design and layout techniques [1].

In this paper we present a test chip, ABCDS-FE, which has been designed and prototyped to study performance of the deep submicron process in application for the fast binary front-end as used in the ATLAS Semiconductor Tracker [2]. The chip comprises 64 channels of front-end amplifiers and comparators and an output shift register. The design has been implemented in a 0.25 µm IBM technology following the radiation hardening rules.

II. ARCHITECTURE OF THE SINGLE CHANNEL

The schematic diagram of one channel of the ABCDS-FE chip is shown in Figure 1. Single channel comprises three basic blocks: fast transimpedance preamplifier with 14 ns peaking time, shaper delivering additional amplification and integration of the signal and a differential discriminator stage. The preamplifier stage is designed as a fast transimpedance amplifier employing an active feedback circuit. The choice of the architecture was driven by the possibility to obtain much higher bandwidth of the preamplifier stage than in the case of simple resistive feedback using low-resistivity polysilicon resistors available in the process used.

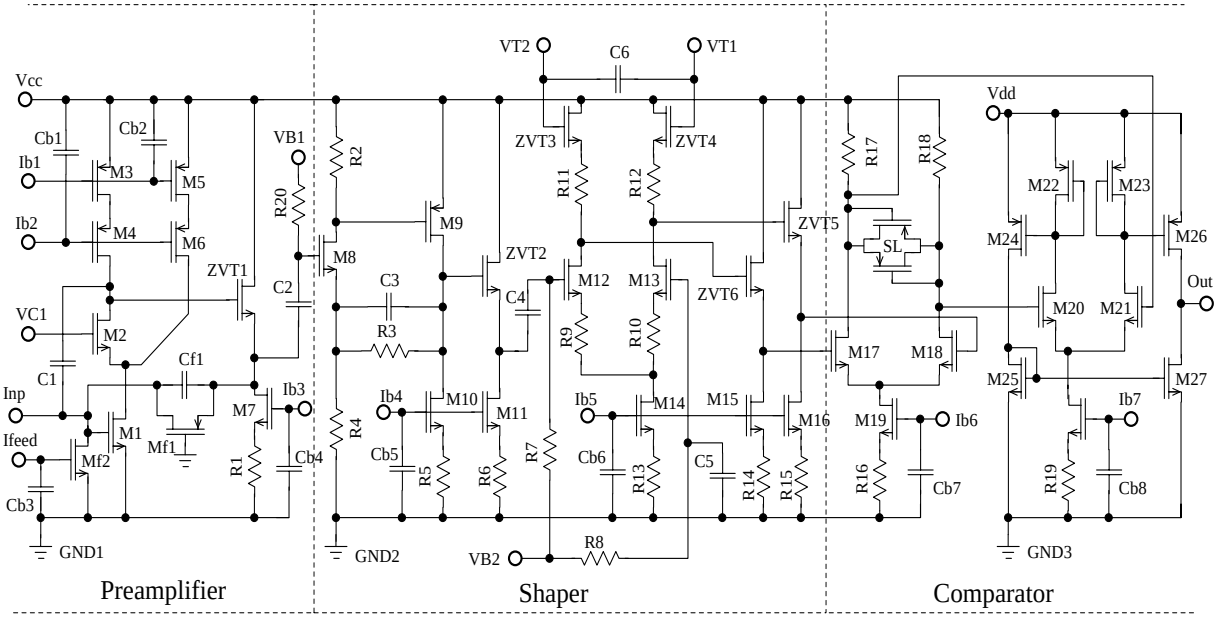

Figure 1: Schematic diagram of one channel of the ABCDS-FE chip.

A. Preamplifier stage

The cascode amplifier employed in the preamplifier stage is a classical structure with an NMOS input device M1 of dimensions 3000µm/0.5µm and PMOS cascode current source load. The dimensions of the input transistor allow for operating the device close to weak inversion, which is necessary to obtain a low value of the excess noise factor Γ, of about 1.3 [3]. The total gate capacitance of the input transistor including intrinsic as well as Gate-to-Source and Gate-to-Drain overlap capacitances, is in the range of 6 pF.

An additional branch of the current source (transistors M5 and M6) connected directly to the input transistor provides the desired bias current without degradation of the cascode output impedance and it improves the open loop gain. In addition, the decrease of the nominal current in the main branch of the cascode allowed us for decrease of the sizes of the transistors used in the current sources, which limits the parasitic capacitances and increases the bandwidth of that stage. The configuration provides open loop gain of about 83 dB and the bandwidth in the range of 600 MHz for wide range of the input transistor bias. The dimensions of the PMOS transistors used in current sources allow biasing the input transistor up to 800 µA, at the worst case technology corner (highest Vt) and limited voltage supply (-10% with respect to the nominal of 2.5 V). The bias current ranging from 400 to 700 µA provides roughly 9 to 16 mS transconductance of the input transistor, which is sufficiently high to obtain desired noise performance for high input capacitance. High gain together with wide bandwidth of the amplifier helps to keep the input resistance low over wide frequency range as shown in Figure 2.

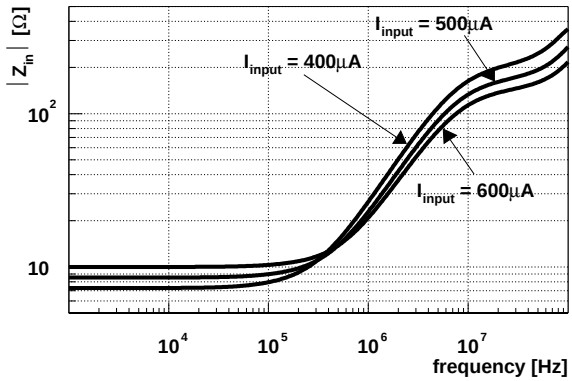

Figure 2: The input resistance of the preamplifier for various bias of the input transistor as a function of frequency.

For the bias of the input transistor with current between 400 µA and 600 µA the input resistance is in the range of 100 to 150 Ω at 10 MHz, which is the centre frequency of the shaper band. This ensures small cross talk and relatively small loss of input charge due to the detector interstrip capacitance. The phase compensation of the preamplifier stage is provided by two metal-to-metal capacitors Cf1 and C1 with a total capacitance of 190 fF, which also decreases the input impedance for high frequencies. A large phase margin, above 80 degree, is obtained for wide range of bias condition of the preamplifier and the feedback circuit. The phase margin can be still improved if needed, by controlling the feedback current i.e. decreasing the transconductance of the feedback transistor with the penalty of slight increase the width of the response pulse. The phase margin and preamplifier response for different bias condition and nominal input capacitance of 20 pF are shown in Figure 3 and Figure 4.

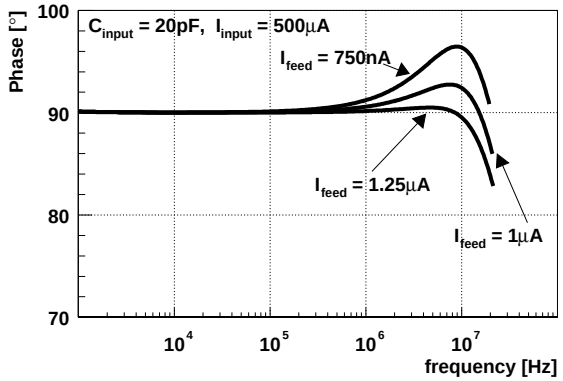

Figure 3: Simulation of preamplifier phase margin for 500 µA bias current of the input transistor, 20 pF input capacitance and various feedback currents.

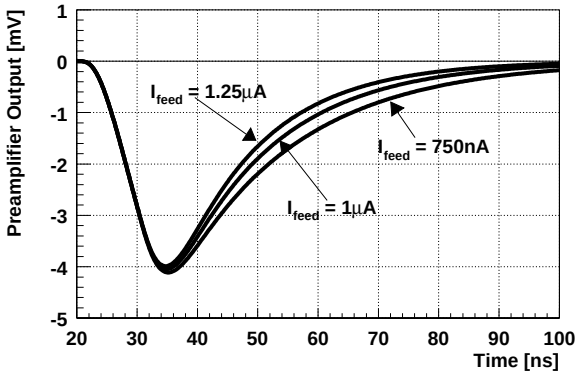

Figure 4: Preamplifier responses to 1 fC signal charge for various feedback currents, nominal input transistor bias (550 µA) and 20 pF input load capacitance.

The principle of the Active Feedback Preamplifier (AFP) is described in [4]. Transistor Mf1 is placed in the feedback path of the cascode stage instead of conventional feedback resistor in a classical transresistance amplifier. Transistor Mf1 works in saturation and is biased in moderate inversion by a current source built of transistor Mf2. Therefore, Mf1 acts as a cascode stage across the feedback path. The trans-conductance g_m of that transistor determines the effect of the feedback resistor (in classical design) and together with feedback capacitance Cf1 the gain. For the nominal bias current of 1 µA, the transconductance of Mf1 is about 10 µS, which is equivalent to 100 kΩ feedback resistor in a classical design. The chosen value of the feedback current provides high linearity in wide range of input signals, and fast response time (14 ns peaking time for 20 pF of input capacitance and nominal bias condition). The gain of that stage for a nominal bias condition (550 µA in the input transistor, 1 µA in the feedback transistor) and input capacitance of 20 pF is of about 4 mV/fC (see Figure 4).

B. Shaper stage

The shaper stage consists of two AC-coupled amplifiers. First amplifier is built in single ended configuration of two cascaded common source stages (transistors M8 and M9). The closed loop DC gain is set by the ratio of resistors R3 and R4. The stage integrates the signal up to about 20 ns. The pulse gain is defined by resistive feedback and by the compensation capacitor C3 of 130 fF. The closed loop pulse gain of that stage is of about 6 V/V. The open loop gain of the stage is in the range of 50 dB, which provides excellent linearity up to 40 fC of the signal. Taking into account the low power consumption of the stage (175 μW without the buffer) this solution is very attractive for many applications.

A second stage of the shaper built as a differential amplifier (transistors M12 and M13) serves for two purposes. First, it amplifies and converts the single ended signal to a differential one. The differential gain of that stage is 2.5 V/V. In addition it interfaces the threshold voltage VT1-VT2 for the comparator, which is applied differentially through the gates of the transistors ZVT3 and ZVT4 connected as source followers. The same voltage appears on the R11 and R12 load resistors (the NMOS devices are "zero Vt" type) and produces a differential voltage at the outputs of the differential pair.

The total gain of the analogue chain of the FE preamplifier and shaper is about 60 mV/fC. The response pulse is semigaussian, with 20 ns peaking time. The simulated response to 3.5 fC signal with the threshold set at 1 fC (nominal operating condition of the binary electronics for ATLS SCT) is shown in Figure 5.

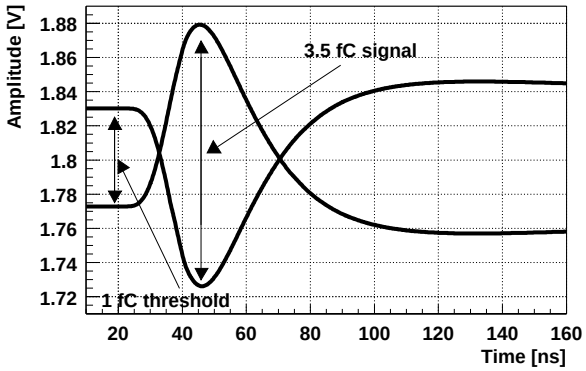

Figure 5: Response of the preamplifier/shaper chain to 3.5fC signal for nominal bias and load conditions and the threshold set at 1fC The differential signal at the comparator input is shown.

C. Comparator

The differential signal from the output of the shaper is buffered by two NMOS source followers and transferred to the first differential pair (M17 and M18). The differential gain of the comparator input stage is 28 dB. A high gain in combination with threshold input voltage ranging from 0 to 800 mV might lead to the saturation of the stage. To prevent the saturation a swing limiter (SL) based on PMOS devices has been employed. The second section of the comparator is a classical two-stage amplifier with very high DC gain (~72 dB). The current switched during the transitions is limited by the current source, which biases that stage. The last stage is supplied from the digital power supply. It has been found that this configuration of the power supply provides a very high rejection of the pick-up (up to 56dB) from digital power supply to the analogue part of the circuit.

Several components will contribute to final spread of the comparator offset:

- Offset of the M12 and M13 differential pair amplified by the gain of that stage (~2.5)
- Offsets of the transistors used in the threshold circuit (ZVT3&ZVT4), NMOS source followers and comparator stage
- Voltage mismatch due to the mismatch of the R11 and R12 resistors (14.7kΩ). For the used dimensions the matching of the resistors is estimated to be 0.5%.

Assuming a value of 1mV rms for the threshold voltage spread in used transistor pairs and nominal bias of 2x30 μA for transistors M12 and M13, one can estimate the value of the comparator offset spread to be around 4.5mV rms.

An important parameter is the minimum overdrive of the comparator for fast pulses delivered from the shaper. For the nominal bias condition, the comparator requires at least 3 mV overdrive in order to produce a full swing pulse at the output (width of the input signal is in that case around 5 ns).

Another critical parameter of the discriminator is the time walk. In our case this parameter is defined for the comparator connected to the Front-End amplifier. Thus, we combine all timing effects, peaking time of the amplifier and response delay of the comparator itself into one number. Time walk is defined as the delay of the comparator response to input charges of 1.2 fC with respect to the response to 10 fC while the comparator threshold is set at 1 fC. For a nominal input load and bias of the Front-End the total time walk has been simulated to be 12 ns.

III. TEST RESULTS

The basic analogue parameters of the amplifier like speed, gain, linearity and the noise performance were evaluated in details for different bias and input capacitance loads using eight analogue test channels available on the chip. The gain, offset and noise of the full chain has been evaluated by scanning the discriminator threshold for a given input charge. For each threshold value a series of pulses has been applied. The threshold scan for a given input charge (called "S-curve") gives the counting rate at the discriminator output as a function of the threshold. Provided the noise has a Gaussian distribution the S-curve is described by the complementary error function. The 50 % point of the S-curve corresponds to a threshold equal to the signal amplitude while the width of the S-curve contains information about the rms value of noise. By performing these measurements for several values of calibration signals one can extract the gain, offset and noise of the full signal chain.

A. Analogue measurements

Figure 6 shows the measured response of the amplifier channel as seen by the input of the comparator for input charges from –4 to 16 fC.

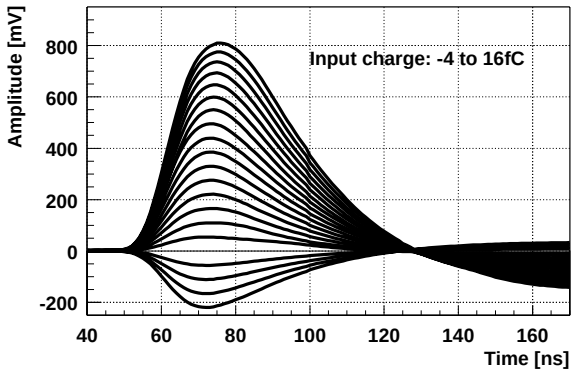

Figure 6: Response of the amplifier biased with nominal currents to the input charges from –4 to 16 fC.

The dynamic range and linearity of the analogue chain for nominal as well as for corner process parameters and limited power supply is shown in Figure 7. As one can see, the good linearity is kept up to 12 fC range in all measured FE amplifiers. One can observe a few percent change in gain for the chips from the corner runs and almost no difference for lowered power supply compared to the nominal one.

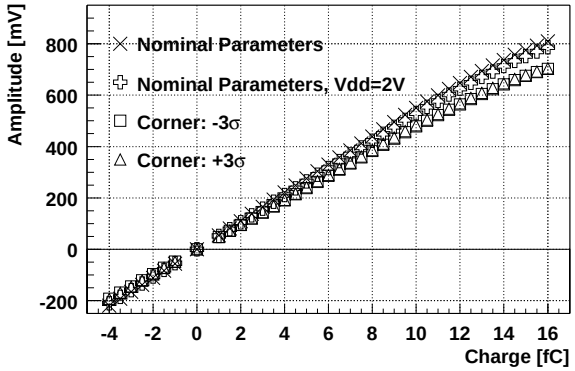

Figure 7: Linearity of the FE amplifier for various corner of the process parameters as well as for nominal and limited power supply.

The gain, speed and the noise of the amplifier are the function of bias, especially the feedback current, which defines the transconductance of the feedback loop. The performance of the amplifier has been tested in wide range of the biases of the input transistor (between 400 and 700 μA) as well as feedback current (0.4 and 1.6 μA). The plots of the peaking time and gain for open channels are shown in Figures 8 and 9. Depending on the input bias current and feedback bias current the gain seen on the comparator input is between 50 and 65 mV/fC. The peaking time might vary between 18 and 22 ns depending mostly from the value of the feedback current.

The noise performance of the Front-End for various biases and loaded with different capacitances is shown in Figure 10. The dependence of the peaking time on the input capacitance is shown in Figure 11. Small variation of the peaking time with respect to the load capacitance confirms low value of the input resistance of the preamplifier.

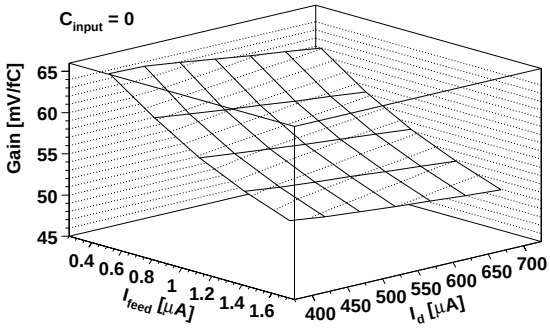

Figure 8: Gain as a function of bias conditions.

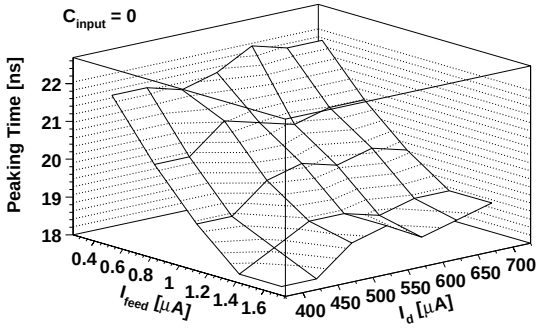

Figure 9: Peaking time as a function of bias conditions.

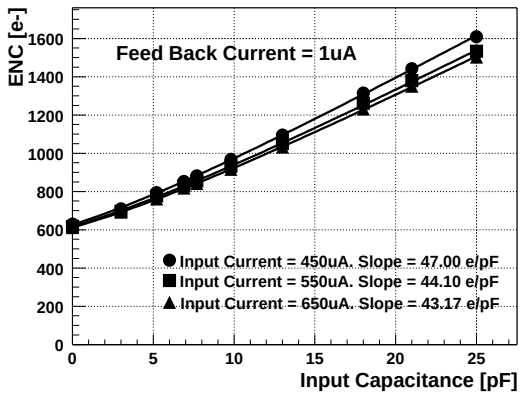

Figure10: The noise slope measured for various input transistor bias.

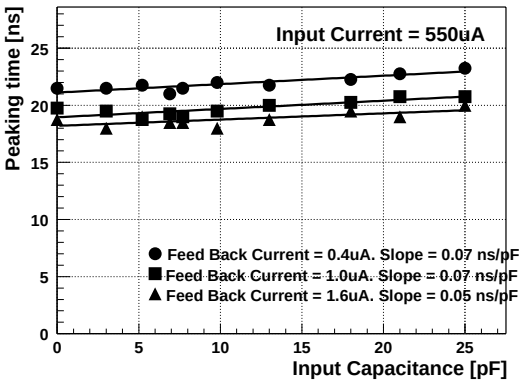

Figure 11: Peaking time as a function of input capacitance.

B. *Full chain measurements*

The measurements of the full chain of the FE amplifier were focused on evaluation of matching of the parameters like gain and comparator offsets, as well as on the timing performance of the comparator. The measurements of gain and ENC for the nominal bias conditions agree well with the analogue measurements of a single channel. The distribution of channel gains in one typical ABCDS/FE chip is shown in Figure 12. The gain was extracted from the threshold scans done for 1, 2, 3 and 4 fC input charge, in linear region of the amplifier. The mean value of the gain is 60 mV/fC and the spread of gain is well below 1 % rms.

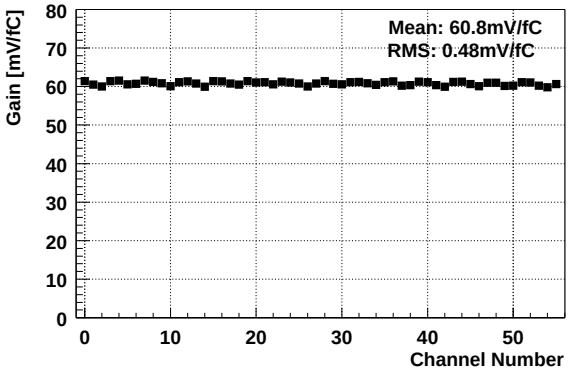

Figure 12: Distribution of channel gain across ABCDS-FE chip biased with nominal currents.

The distribution of comparator offsets is shown in Figure 13. The rms value of the offset spread is around 3 mV for all chips measured, which is about 5 % of the amplitude response to 1 fC charge.

Figure 14 shows the distribution of time walks in one typical ABCDS-FE chip. The threshold voltage equivalent to 1 fC charge has been applied commonly for all channels, thus we may expect the variation of the measured time walks due to the variation of effective thresholds for each channel. The average value of 12.5 ns agrees well with the simulation.

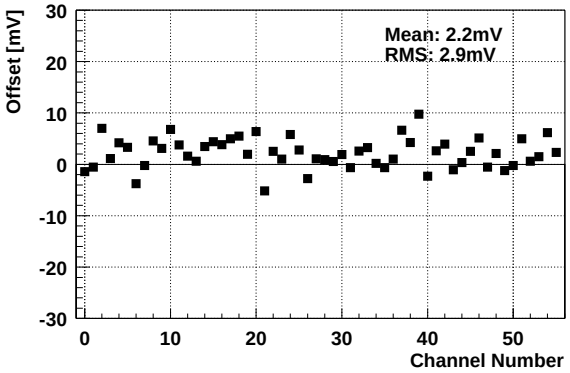

Figure 13: Distribution of comparator offset across ABCDS-FE chip for nominal bias conditions.

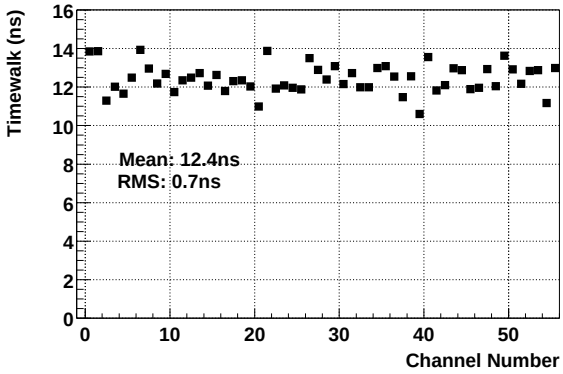

Figure 14: Distribution of time walk across one ABCDS-FE chip working with nominal bias conditions.

IV. CONCLUSIONS

The functionality of the ABCDS-FE chip has been tested for wide range of the bias currents and power supply voltages. The performance of the chips processed with nominal and corner technology parameters are very stable with respect to process variation. Very good uniformity of parameters across the channels has been obtained. No noticeable degradation of analogue parameters was observed after X-ray irradiation up to a dose of 10 MRad.

The design demonstrates that using a submicron CMOS process one can meet the basic requirements of the front-end electronics for long silicon strips at operational conditions represented by the LHC experiments. With respect to noise and power consumption the performance of the fast preamplifier realised in the deep submicron CMOS process is comparable with the performance achievable using a fast bipolar input transistor.

V. REFERENCES

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