A Radiation Tolerant Gigabit Serializer for LHC Data Transmission*

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Abstract

In the future LHC experiments, some data acquisition and trigger links will be based on Gbit/s optical fiber networks. In this paper, a configurable radiation tolerant Gbit/s serializer (GOL) is presented that addresses the high-energy physics experiments requirements. The device can operate in four different modes that are a combination of two transmission protocols and two data rates (0.8 Gbit/s and 1.6 Gbit/s). The ASIC may be used as the transmitter in optical links that, otherwise, use only commercial components. The data encoding schemes supported are the CIMT (G-Link) and the 8B/10B (Gbit-Ethernet & Fiber Channel). To guarantee robustness against total dose irradiation effects over the lifetime of the experiments, the IC was fabricated in a standard 0.25 µm CMOS technology employing radiation tolerant layout practices.

The device was exposed to different irradiation sources to test its sensitivity to total dose effects and to single effects upsets. For this tests, a comparison is established with a commercial serializer.

I. INTRODUCTION

The high bunch crossing rate (40MHz) of particles together with the large number of channels in the LHC detectors will generate massive amounts of data that will be transmitted out of the different sub-detectors for storage and off-line data analysis. Trigger links will also be transmitting large amounts of data to the trigger processors. The last type requires low data latency and operation synchronous to the LHC master clock. Low latency reduces the required amount of storage memory needed inside the detectors while, synchronous operation avoids complex synchronization procedures of the data arriving to the trigger processors from the different locations in the detectors. Economic considerations as well as power budget, material budget and physical space impose the use of high-speed links for data transmission. Consequently, optical links operating in the Gbit/s range were chosen for these applications.

Modern day commercial components meet (or exceed) the needs existing in the High Energy Physics (HEP) environment. However, for the applications mentioned above, the transmitters will be located inside de particle detectors and will be subject to high doses of ionizing irradiation during the lifetime of the experiments. In general, Commercial-Off-The-Shelf (COTS) devices are not designed to withstand irradiation. If the large number (~ 100K) of links planned for LHC is taken into account, the few radiation-hardened devices that exist on the market have prohibitively high prices. It was thus considered necessary to develop a dedicated solution that would meet the very special HEP requirements. Since only the transmitters will be subject to irradiation, only they need to be developed and qualified for radiation tolerance. Adopting commercial components for all the other parts in the chain reduces the development and maintenance costs. Following this line of reasoning, a transmitter ASIC was developed that is capable of operating with two of the most common data transmission protocols. Several features of the device are configurable so that different user requirements can be accommodated. It was designed using radiation tolerant layout practices that, when applied to CMOS sub-µm circuits, guarantee tolerance to irradiation effects to the levels necessary for the LHC experiments [1] and [2].

In this work, emphasis will be put on the radiation effects on the circuit operation. A COTS serializer has also been irradiated. The results of these tests will be discussed.

II. THE GOL ASIC ARCHITECTURE

The basic principles of the serializer operation have already been discussed in previous publications [3] and [4] and consequently will not be repeated here. Only a brief discussion of the IC architecture will be made since it is relevant for the understanding of the irradiation tests.

As shown in Figure 1 the ASIC "Data Interface" is composed of a 32-bit bus and two data flow control lines

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("dav" and "cav"). Depending on the transmission mode the data bus operates either as a 16 (least significant bits only) or as a 32-bit bus. Since the operation is synchronous with the LHC clock (running at 40 MHz), these two modes result in data bandwidths of 640 Mbit/s and 1.28 Gbit/s respectively. Before serialization, data undergo encoding using either the 8B/10B [5] or the "Conditional-Invert Master Transition" (CIMT) [6] line coding schemes. The encoding procedures introduce two additional bits for each eight bits of data transmitted resulting in serial data rates of 800 Mbit/s or 1.6 Gbit/s. Any combination of line coding and data rate can be used. If CIMT encoding is employed, a G-Link receiver [7] is required while if, 8B/10B coding is performed then either a Gbit Ethernet [8] or a Fiber Channel receiver can be used provided they are compatible with the data rates being generated.

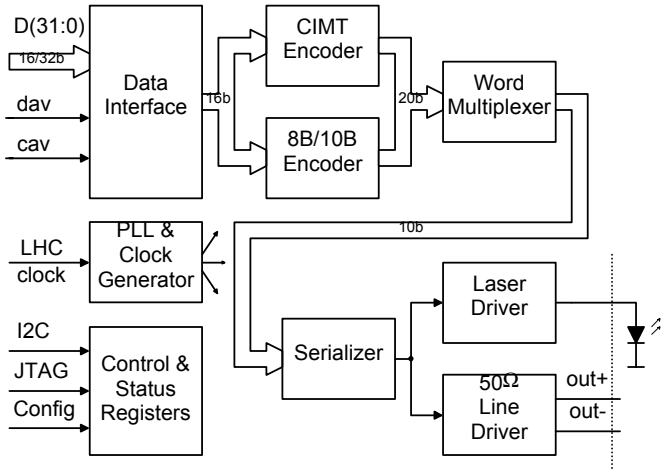

Figure 1: IC architecture

For operation in the 32-bit mode, the "Data Interface" performs time division multiplexing of the 32-bit input words into two 16-bit words at a rate of 80 Mwords/s. No multiplexing is done at this stage if the 16-bit mode is used. During encoding, the 16-bit data words are transformed into 20-bit words that are further time-division multiplexed into two 10-bit words by the "Word Multiplexer" before they are fed to the "Serializer". The "Serializer" converts them into the final serial data stream and drives both the "Laser Driver" and the "50Ω Line Driver". The use of the output drivers is mutually exclusive.

The several clock frequencies necessary to run the different circuits of the serializer are internally generated by a clock multiplying PLL that uses as a reference the LHC master clock signal (40.08 MHz).

Due to radiation effects, it is expected that the threshold current of the laser diodes will increase with time over the lifetime of the experiments [9]. To compensate for this, the laser-driver contains an internal bias current generator that can be programmed to sink currents between 0 and 55 mA. Programming the ASIC can be done using either an I2C [10] or a JTAG [11] interface. External hardwired pins set the main operation modes of the receiver. Although these two interfaces are present in the ASIC they are not essential for its operation. They have been added to allow additional flexibility in the use of the serializer. The main modes of operation are configurable by external hard-wired pins allowing the ASIC to work standalone.

III. Experimental Results

The ASIC was tested using the test setup shown in Figure 2. The transmitter card is composed of a reference clock generator (40MHz), an FPGA that generates the test data to be fed to the GOL serializer, an optical transmitter, and a laser-diode. The same card, equipped differently, was used to test both the CIMT and the 8B/10B modes of operation. The optical transmitter used was the Infineon V23818-K305-V15 for 800 Mbit/s operation in the G-Link mode and the Stratos MLC-25-8X-TL for 1.6 Gbit/s operation using 8B/10B encoding.

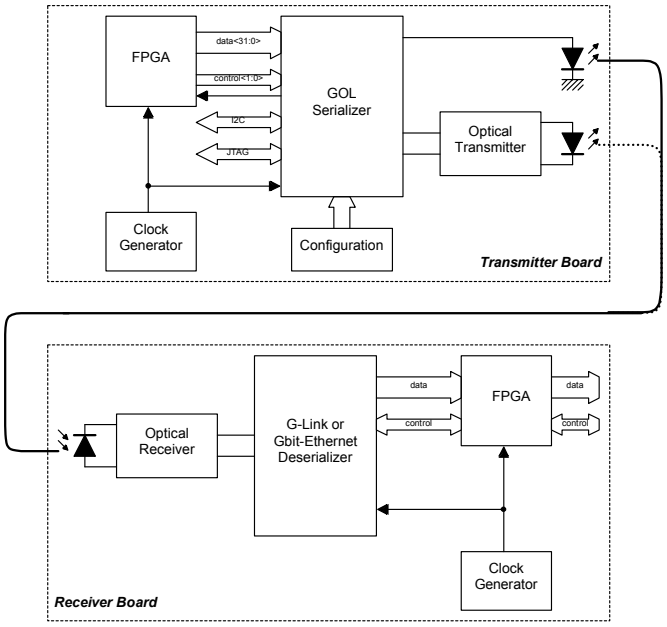

Figure 2 : Test setup block diagram

The receiver board contains a reference clock generator, an optical receiver, a de-serializer and an FPGA whose function is the detection and counting of errors present in the input data stream. The 8B/10B and the G-Link modes of operation required the use of two different receiver boards but their operation principle is the same. The two boards are equipped with parallel ports that allow them to be connected to either a computer or a logic analyzer for monitoring and analysis of errors. One of the boards was setup as a G-Link receiver operating at 800 Mbit/s and it is based on the Agilent HPMD-1024 de-serializer. The other was setup as an 8B/10B receiver operating at 1.6Gbit/s and the de-serializer used was the Texas Instruments TLK2501.

This test setup was used both to perform the evaluation tests and the irradiation tests (total dose and single event effects).

A. Evaluation Tests

All the ASIC functions proved functional. However, the ASIC laser driver displays levels of jitter incompatible with the data rates being transmitted (mainly at 1.6 Gbit/s). Because of that, all the Bit Error Rate (BER) tests reported here refer to data transmission using an external laser driver driven by the ASIC 50Ω line driver outputs.

An error free four days long BER test was done in the G-Link mode at 800 Mbit/s. In addition, a 13-hour error free data transmission test was made in the 8B/10B mode at 1.6 Gbit/s. The chip displays a power consumption of 300 mW and 400 mW at 800M Bit/s and 1.6 Gbit/s, respectively (the power consumption includes a laser-diode bias current of 26 mA). Both the JTAG and the I2C interfaces proved fully functional.

B. Total Dose Irradiation Tests

The ASIC was irradiated with X-rays (10 KeV peak) in a single step to a total dose of 10 Mrad (SiO_2) at a dose rate of 10.06 Krad (SiO_2)/min. A BER test was performed after irradiation for 72 hours and no errors were observed. The data transmission test was done using the G-Link mode at 800 Mbit/s. The power consumption remained the same after irradiation.

C. Single Event Effects Tests

The ASIC was irradiated using heavy ions and protons at the cyclotron Research Center (CRC) of UCL Louvain-la-Neuve, to test its sensitivity to single event effects. The irradiation tests consisted in irradiating the IC during normal operation while at the same time monitoring the transmitted data for errors (BER test). The tests were performed in all cases at room temperature.

1) Proton Test

Two BER tests were made while irradiating the ASIC with 60 MeV protons. The tests were done for the G-Link and the 8B/10B modes of operation at 800 Mbit/s and 1.6 Gbit/s data rates, respectively. Table 1 summarizes the experimental conditions and results. No data transmission errors or PLL losses of lock were observed during the experiment leading to the limit cross sections of $<3.2\ 10^{-13}$ cm2 (8B/10B) and $<4.5\ 10^{-13}$ cm2 G-Link). The evolution of the power consumption was also monitored during the tests with no changes being observed.

Table 1 : Proton test results

Mode	**Flux** *p/(cm² s)*	**Fluence** *p/cm²*	**SEU** *events*	**Limit cross-section** *cm²*
G-Link 800 Mbit/s	$3\ 10^{8}$	$2.20\ 10^{12}$	0	$4.5\ 10^{-13}$
8B/10B 1.6 Gbit/s	$3\ 10^{8}$	$3.14\ 10^{12}$	0	$<3.2\ 10^{-13}$

2) Heavy Ion Test

BER tests were also performed using heavy ions. For this experiment, the dominant cause of errors was the loss of synchronization of the PLL. Loss-of-lock is reflected as a few consecutive words in error, if only a small phase deviation is in cause, or by large groups of erroneous words, if frequency lock is lost or if large phase jumps are present. In the graph shown in Figure 3 the cross section for the loss of synchronization event is plotted as function of the Linear Energy Transfer (LET) of the ions. To plot these curves, frequency loss-of-lock was not distinguished from phase loss-of-lock. The loss of lock event was considered present every time there were more than two consecutive wrong words detected. Single errors were only a small fraction of the total number of errors observed, mainly for the higher LETs. In Figure 3 three curves are plotted. The points marked as "♦" represent previously made measurements [4] using the first version of the GOL serializer operating at 1.2 Gbit/s and implementing only the PLL and the high-speed part of the serializer. The points represented by "□" correspond to 8B/10B operation at 1.6 Gbit/s, while points marked as "▲" correspond to the G-Link mode at 800 Mbit/s. From these curves, it is clearly seen that, for the same chip, the behaviour under radiation depends on the operation speed. Although it is not possible to make a direct comparison between the present version of the IC and the simple serializer, the curves seem to indicate that changes made to the circuit, aimed at obtaining a more SEU robust operation, were effective. It is also worth noting that, while the ASIC active area has increased by a factor of five (due to the presence of additional logic circuits) the total measured cross-section has not increased in that proportion. The measured values of LET threshold are 6.5 MeV cm^2/mg for 1.6 Gbit/s operation and 14 MeV cm^2/mg for 800 Mbit/s operation. The value measured previously for the serializer was 7 MeV cm2/mg at 1.2 Gbit/s. Based on these results and using the extrapolation method proposed in [12] the error rates for several CMS environments were estimated. The results of such calculations are given in Table 2.

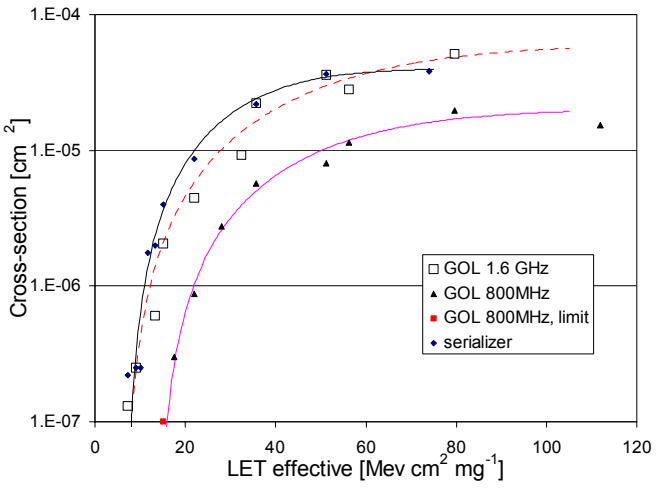

Figure 3 : Experimental cross-section

3) Commercial Serializer

Using a transmitter board similar in functionality to the one described above for the GOL transmitter, two samples of the TLK2501 Texas Instruments transceivers were subject to 60 MeV protons irradiation.

For this test, the proton flux was fixed at 3.5 10^8 p/(cm^2.s). At a total proton fluence of 1.0 10^{12} p/cm^2, 8 events were observed for the first device tested and 11 upsets for the second device. Among those 19 events, 11 were found corresponding to single word upsets and 8 to PLL losses of synchronization. These result in cross-sections of 8 10^{-12} cm^2 for the loss of lock event and 1.1 10^{-11} cm^2 for single errors.

The transmitter board current consumption was monitored during irradiation. The test was interrupted when the power consumption reached a value 2.5 times higher than the pre-irradiated value, at a fluence of 9.4 10^{11} cm^2. This increase is surely due to total dose effects. The accumulated fluence corresponds to a radiation dose of about 130 Krad.

Table 2 : Estimated error rates for four different CMS environments

Environment	**Pixel** *R = 4 - 20 cm*	**Endcap ECAL** *R = 50 - 130 cm*	**Outer Tracker** *R = 65 - 120 cm*	**Exp. Cavern** *R = 700 - 1200 cm*
Serializer [4] *Errors/(Chip Hour)*	1.4 10^{-2}	1.9 10^{-4}	8.4 10^{-5}	3.1 10^{-8}
GOL 800 Mbit/s *Errors/(Chip Hour)*	0	0	0	0
GOL 1.6 Gbit/s *Errors/(Chip Hour)*	9.4 10^{-3}	1.3 10^{-4}	5.8 10^{-5}	2.2 10^{-8}

IV. ASIC UPGRADE

As discussed before, the jitter levels on the laser driver output exceed the values reasonable for error free transmission. The causes for this problem were traced down and a new version of the ASIC with modifications aimed at solving this problem was submitted for fabrication. Besides this, a few more modifications were introduced that were requested by the CMS collaboration. A list of new features and modifications follows:

- I/O input cells were redesigned to be TTL and 5V CMOS compatible;
- An optional differential clock input was added. It is compatible with LVDS and PECL voltage swings;
- An open fiber control safety logic circuit was introduced;
- The ESD protection circuits were improved;
- The input buffers of the I2C interface were replaced by Schmitt trigger cells;
- The pinout was redefined.

V. SUMMARY

A configurable Gbit/s serializer (GOL) has been developed and manufactured to address the HEP experiments requirements. The device was experimentally validated to comply with the levels of radiation tolerance required by the LHC experiments. Both total dose and SEU irradiation tests were realized. The SEU tests were made using 60MeV protons and Heavy Ions. Using the SEU test results, an estimate of the error rates for such a device in different CMS environments was made. SEU results for a commercial serializer were also presented for 60 MeV proton irradiation tests. When compared to the commercial device, the GOL ASIC displays higher tolerance in what concern tolerance to total dose irradiation and single event upsets..

VI. REFERENCES

[1] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects", IEEE Trans. Nucl. Sci. Vol. 46 No.6, p.1690, 1999.

[2] K. Kloukinas, F. Faccio, A. Marchioro and P. Moreira, "Development of a radiation tolerant 2.0V standard cell library using a commercial deep submicron CMOS technology for the LHC experiments" *Proc. of the fourth workshop on electronics for LHC experiments*, pp. 574-580, Rome, 1998

[3] P. Moreira, J. Christiansen, A. Marchioro, E. van der Bij, K. Kloukinas, M. Campbell and G. Cervelli, "A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links", *Proceedings of the Fifth Workshop on Electronics for LHC Experiments*, Snowmass, Colorado, USA, 20-24 September 1999, pp. 194-198

[4] P. Moreira 1, T. Toifl, A. Kluge, G. Cervelli, F. Faccio, A. Marchioro and J. Christiansen, "G-Link and Gigabit Ethernet Compliant Serializer for LHC Data Transmission," 2000 IEEE Nuclear Science Symposium Conference Record, October 15 - 20, 2000, Lyon, France, pp. 9.6 – 9.9

[5] IEEE Std 802.3, 1998 Edition

[6] C. Yen, R. Walker, P. Petruno, C. Stout, B. Lai and W. McFarland, "G-Link: "A chipset for Gigabit-Rate Data Communication," Hewlett-Packard Journal, Oct. 92.

[7] See for example the Agilent HDMP-1034 receiver chip data sheet: http://www.agilent.com

[8] See for example the Texas Instruments TLK2501 transceiver chip data sheet: http://www.texasinstruments.com

[9] F. Vasey, C. Azevedo, G. Cervelli, K. Gill, R. Grabit and F. Jensen, "Optical links for the CMS Tracker," *Proc. of the*

fifth workshop on electronics for LHC experiments, pp. 175-179, Snowmass, 1999

[10] "The I2C-BUS specification", Philips Semiconductors, Version 2.1, January 2000

[11] C. M. Maunder and R. E. Tulloss, "The Test Access Port and Boundary-Scan Architecture," IEEE Computer Society Press, 1990

[12] M. Huhtinen and F. Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", *Nuclear Instruments and Methods A*, vol. 450, pp. 155-170, 2000