

Development of a DMILL radhard multiplexer for the ATLAS Glink optical link and radiation test with a custom Bit Error Tester.

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Abstract

A high speed digital optical data link has been developed for the front-end readout of the ATLAS electromagnetic calorimeter. It is based on a commercial serialiser commonly known as Glink, and a vertical cavity surface emitting laser. To be compatible with the data interface requirements, the Glink must be coupled to a radhard multiplexer that has been designed in DMILL technology to reduce the impact of neutron and gamma radiation on the link performance. This multiplexer features a very severe timing constraints related both to the Front-End Board output data and the Glink control and input signals. The full link has been successfully neutron and proton radiation tested by means of a custom Bit Error Tester.

I) INTRODUCTION

The Liquid Argon Calorimeter of the ATLAS experiment at the LHC is a highly segmented particle detector with approximately 200 000 channels. The signals are digitized on the front-end board and then transmitted to data acquisition electronics located 100m to 200m away. The front-end electronics has a high degree of multiplexing allowing the calorimeter to be read out over 1600 links each transmitting 32 bits of data at the bunch crossing frequency of 40.08 Mhz. The radiation hardness is a major consideration in the design of the link, since the emitter side will be exposed to an integrated fluence of $3 \cdot 10^{13}$ n (1 MeV Si) over 10 years of the LHC running.

II) OPTICAL LINK DESCRIPTION

The demonstrator link is based on an Agilent Technologies HDMP1022/1024 serialiser/deserialiser. This Glink is used in a double frame mode: the incoming digitized data of 32 bit at 40.08 Mhz are multiplexed and sent as two separate 16 bit frame segments at 80.16Mhz with the use of an external multiplexer. The Glink chip set adds a 4 bit control field to each 16 bit data segment which results in a total data transfer rate of 1.6 Gb/s (see figure 1).

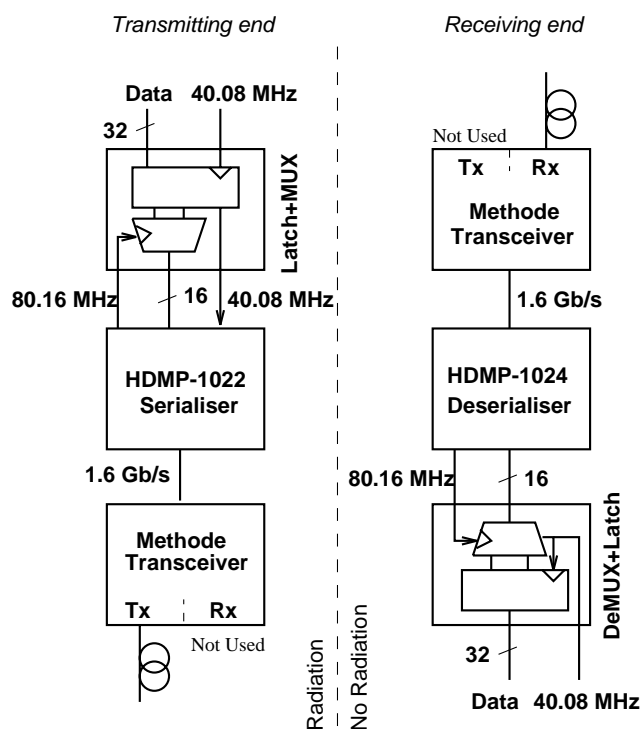


Figure 1: A 1.6Gb/s optical link based on the G-link chipset.

The Glink serialiser outputs drive a VCSEL that transforms the electrical signal into light pulses transmitted over a Graded Index (GRIN) 50/125 mm multimode fibre to a PIN diode located on the receiver board. For the link described in this document the VCSEL and the PIN diode are packaged together with driving and discriminating circuits as transceiver modules manufactured by Methode. The PIN diode output signals are deserialised by the GLINK receiver chip (HDMP1024), then a Programmable Logic Array (ALTERA EMP7128) is used for demultiplexing the 16 bits data into the basic 32 bits format.

III) MULTIPLEXER CHIP

The Glink is used in a double frame mode so that the full link has the capability to transfer the 32 bit format data (figure 2).

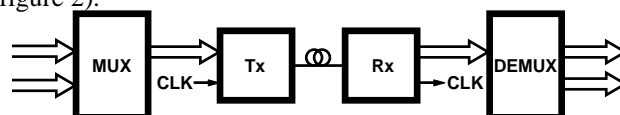


Figure 2: The Glink chipset in a double frame mode.

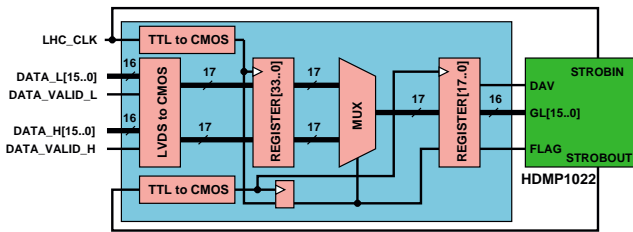


Figure 3 The multiplexer block diagram.

This configuration requires an external multiplexer. One can see in figure 3, the block diagram of the multiplexer ASIC (MUX). Since this chip must be located on the FEB board, it must be radiation hard, thus the design was done in the radhard DMILL technology.

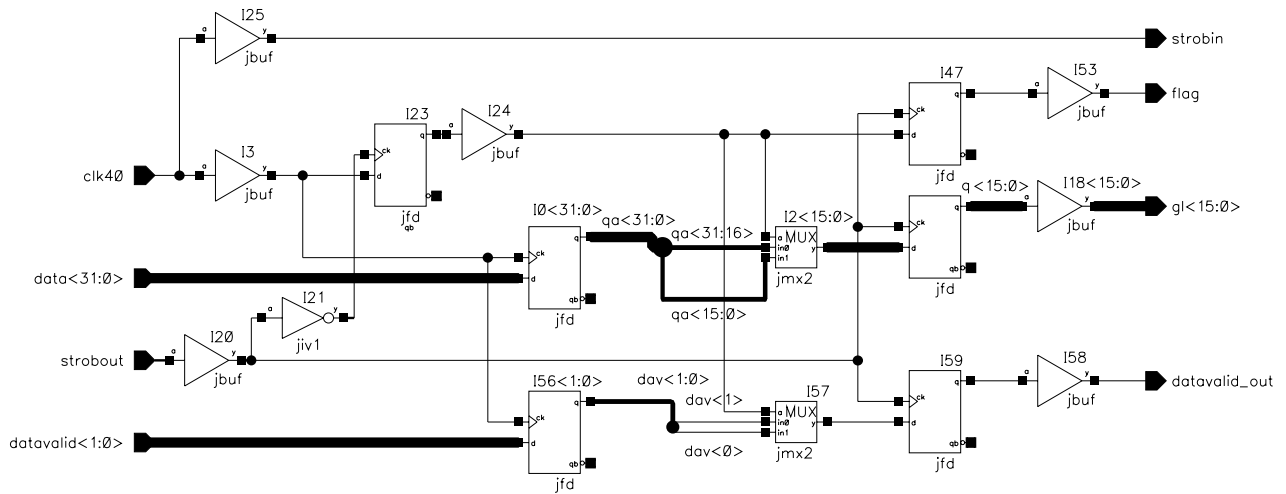


Figure 4: Schematic of the multiplexer

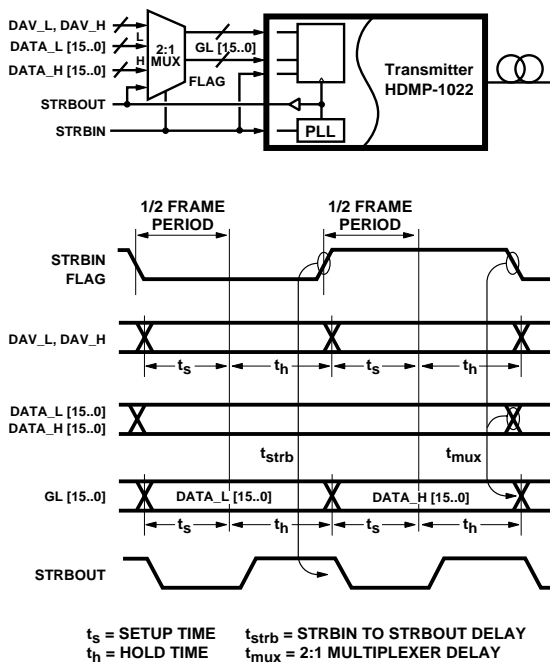


Figure 5: Transmitter data interface and timing constraints.

The data signals sent to the multiplexer have a LVDS logic standard, therefore the first stage of the MUX chip is a LVDS to CMOS level translator; then at the second stage the data are registered, and finally multiplexed. In addition to the data signals, the FEB sends two validation signals (one for each 16 bit segment) which go through the MUX chip via the same logic flow. Hence in the output register there are 16 bits (for data)+ 1 bit (for validation), and 1 extra FLAG bit. In the double frame mode, this FLAG bit is used by the transmitter and receiver to distinguish the first or second frame segment. The schematic of the multiplexer chip is shown in figure 4. One could notice that the output registers are synchronized with Strobout which is a 80.16Mhz latch clock generated by a PLL inside the serialiser. This clock features 50% of duty cycle which is the best configuration

for the Glink in a double frame mode. Figure 5 shows the transmitter data interface that the multiplexer must fit in with. The Tstrb delay is defined from the falling edge of STRBOUT to the corresponding rising or falling edge of STRBIN. The typical value for this delay is 4ns.

The data (at the MUX output) must be valid for a set-up time (T_s) before it is sampled and remain valid for a hold time (T_h) after it is sampled. The minimum value required in the data sheets [1] for both T_s and T_h is 2ns.

A double channel version of the multiplexer has been designed and tested successfully with the full optical link [2]. For the main 40.08Mhz clock the link has shown a tolerance of the duty cycle from 32% to 65%. The limits found for the general delays between the main clock edge and the incoming data sampling time are 1.2ns and 13.2ns. The total power dissipation is 0.6W, leading into 0.3W/channel.

IV) A CUSTOM BIT ERROR TESTER

The Glink chip set provides a link-down and a single error monitoring through a 4 bit control field which is appended to each 16 bit data field. The control field has a master transition (which the receiver uses for frequency locking) and includes information regarding the data type (control, data, fill frame). The control bits are analyzed by the deserialiser to provide two output flags: a 'link-down flag' occurs when the receiver can not identify a frame to

lock onto, and a 'single error flag' indicates an illegal control field in the transmitted frame.

Initially the error detection was done mainly by monitoring the Glink's inbuilt error flags, as reported in [3], but later a custom Bit Error Tester (BERT) has been developed [4]. It helps to refine the testing and in particular to discriminate between different types of errors in the link. Besides it permits several links to be tested simultaneously. The basic idea was to develop a system capable to send a flow of ATLAS like data in parallel through two different paths. One path is the reference one and the other follows the full optical link to be tested as described in figure 1. The BERT must also be able to synchronise, read and compare the out-coming data from both paths.

The BERT system includes EPLD-based boards plugged in a VME crate. It is coupled to a pseudo-random pattern generator based on the CompuGen3250 board from Gage[5], and provide an interface to a computer for on-line monitoring. One can see the details on this BERT system in figure 6.

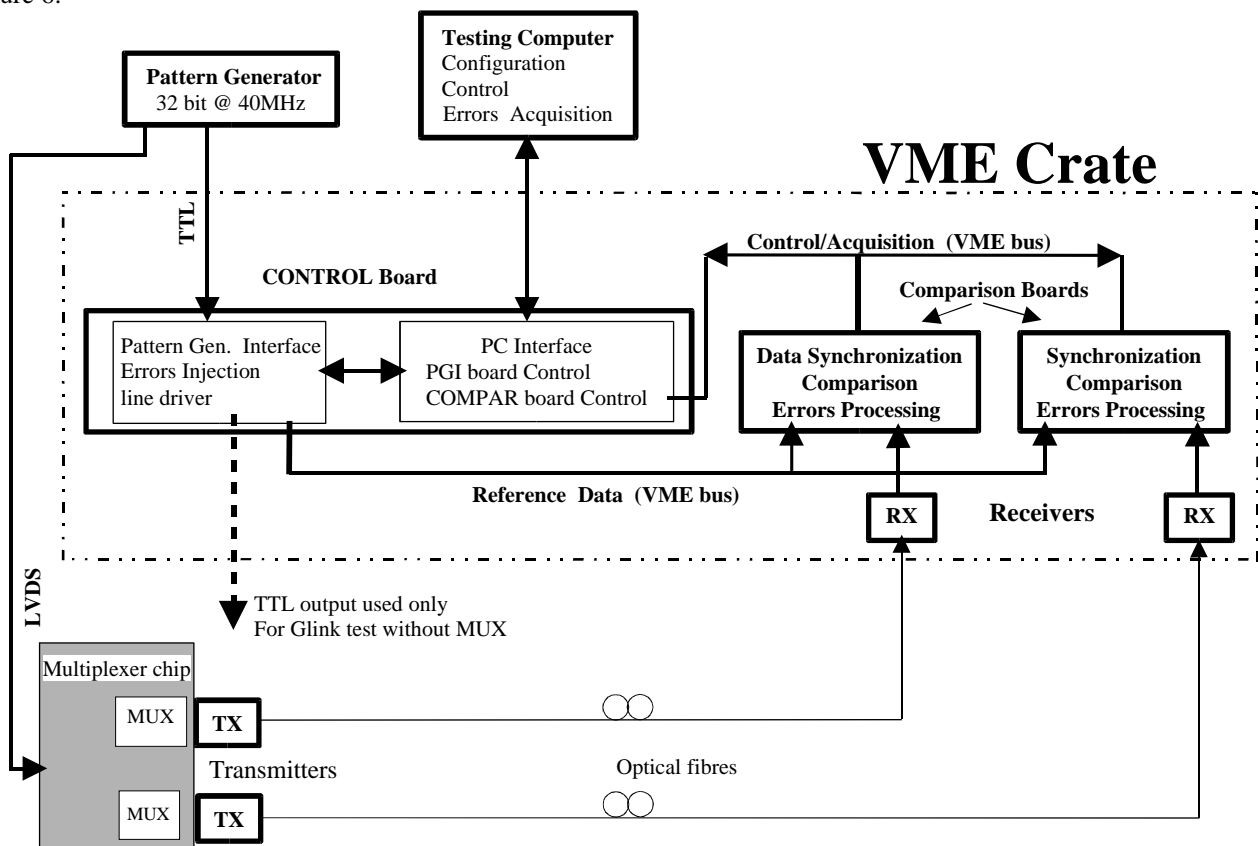


Figure 6: Details of the custom BERT set-up.

The CONTROL board:

It provides interfaces both to the pattern generator and to the acquisition and configuration computer. It sends data simultaneously via the VME bus (reference data) and through a set of optical links (including the multiplexer) to be tested in parallel.

The COMPARISON board:

It reads the reference data sent on the VME bus and performs a bit to bit comparison with the data transmitted

through an optical link. This comparison result is sent to the CONTROL board via the VME bus.

The slow control of any step, from the data generation to the comparison result acquisition, is done by a computer.

By means of this BERT system, we have successfully tested the Glink in our laboratory for many weeks, and also during the irradiations tests:

V) RADIATION TEST WITH THE BIT ERROR TESTER

Several link sender boards were exposed to neutron flux to assess the radiation tolerance of the DMILL MUX, the Glink serialiser and the Methode transceiver. During the radiation tests, the behaviour of the link was monitored on-line by means of the BERT coupled to a pseudo-random pattern generator [5].

The radiation tolerance of a G-link serialiser coupled to a Methode transceiver has been proved under neutron

integrated dose up to $5 \cdot 10^{13}$ (1 Mev Si) neutrons/cm². However, transient data transmission errors were observed and identified as Single Event Upsets (SEU).

The interaction of neutrons with silicon produces secondary charged particles, which could be located on the active devices of the electronics chip. A fraction of the released charge along the ionizing particle paths is collected at one of the circuit nodes. If it is high enough the resulting transient current might produce a SEU. In order to estimate the SEU rate, the main parameters that need to be taken into account are the sensitive volume of the chip within which

the ionization takes place, and the critical energy to be exceeded before triggering an upset.

Initially the link error detection was performed by monitoring the G-link's inbuilt error flags as reported in [3], and later by means of the a Bit Error Rate Tester (BERT) coupled to a pseudo-random pattern generator.[4]

Four different types of errors were identified:

- single bit flip (relative rate 72%)
- n bit flips (relative rate 9%)
- clock corruption in the transmitted frame for a few 40.08 MHz clock counts (relative rate 9%)
- link-down error, in addition to a loss of data this error leads to a loss of clock information (relative rate 10%)

The experimental data were then interpreted using two different methods that are described in [3] and [6]. These methods lead to a predicted ATLAS error rate as high as 0.65 +/- 0.30 error/link/hour.

A test was carried out with a 60 MeV proton beam at the CRC in Louvain-La-Neuve (Belgium) in June 2001. In this experiment, the method used to analyse the data recorded with the BERT system was the one described in Ref [7]. A nice agreement with the results obtained at CERI was found. In addition, it confirms that the proton flux (as well as neutron flux) has very little influence on the DMILL multiplexer performance, and it induces less than 0.1% of the total SEU error rate.

VI) CONCLUSION

The radiation tolerance of the sender part of the link has been demonstrated under neutron radiation up to 10^{14} n cm⁻².

Transient data transmission errors (Single Event Upset) were observed by means of the BERT set-up but it has been shown that the contribution of the DMILL MUX to this error rate is very negligible.

VII) REFERENCES

[1] Manufactured by Hewlett Packard, Agilent Technologies, P.O. Box 10395, Palo Alto, CA 94303, <http://www.semiconductor.agilent.com>.

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[3] M-L Andrieux et al., Nuclear Instr. And Meth A 456 (2001), p342.

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[7] Ph Fartouat et al. 'ATLAS policy on radiation tolerant electronics' ATLAS document No ATC-TE-QA-0001, 21 July 00.