Controlling Front-End Electronics Boards Using Commercial Solutions

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***Abstract*—LHCb is a dedicated B-physics experiment under construction at CERN's large hadron collider (LHC) accelerator. This paper will describe the novel approach LHCb is taking toward controlling and monitoring of electronics boards. Instead of using the bus in a crate to exercise control over the boards, we use credit-card sized personal computers (CCPCs) connected via Ethernet to cheap control PCs. The CCPCs will provide a simple parallel, I2C, and JTAG buses toward the electronics board. Each board will be equipped with a CCPC and, hence, will be completely independently controlled. The advantages of this scheme versus the traditional bus-based scheme will be described. Also, the integration of the controls of the electronics boards into a commercial supervisory control and data acquisition (SCADA) system will be shown.**

***Index Terms*—Controls, credit-card personal computer (PC), experiment, front-end electronics.**

I. Introduction

This document is intended as an overview of one concept, the LHCb (cf. Fig. 1) [1] controls system will use. A novel approach to control front-end electronics boards is the use of individual control central processing units (CPUs) on each electronics board in contrast to using one per crate which communicates via a high-performance bus system that is part of the crate with the modules inside. This traditional approach is not very cost effective when the crate bus is exclusively used for controls, which it would be in LHC experiments as commercial crate bus systems are too slow for the transfer of physics data.

II. Basic Controls System Architecture

LHCbs controls system will span over four layers, a supervisory layer, a partition layer or system layer, a subsystem layer, and a device layer. A sketch of the involved systems and devices is show in Fig. 2.

As one can easily see, LHCb will have one experiment controls system (ECS), which takes care of all the controls functions needed for the full experiment, including communications with the accelerator (LHC), handling of detector safety system (DSS) states and exceptions, controlling the detector itself (DCS), and the data acquisition (DAQ). All these high-level systems contain systems that correspond to hardware systems and/or partitions of the experiment, which in turn may contain subsystems that need controls (e.g., configuration, flow-control, etc.). These subsystems control devices that may be hard and/or software. Some examples of possible connections are shown in Fig. 2. Clearly, there is a substantial need for communication between the individual systems, which could be reduced by relocating, e.g., configuration data to a more dispersed system of controls CPUs. The shown abstract system translates into a hardware architecture that is shown in Fig. 3, where different approaches for the controls system are also illustrated. These are especially the conventional approaches, i.e., a controls node directly communicating with devices, communicating via a fieldbus (e.g., WorldFIP), or communicating with a controls crate that, in turn, communicates with the devices via a fieldbus. Furthermore, one has to take into account that not only detector parts are controlled with the ECS, but also PC-farms for higher level triggers, online data-analysis, and data storage to name just the most prominent tasks.

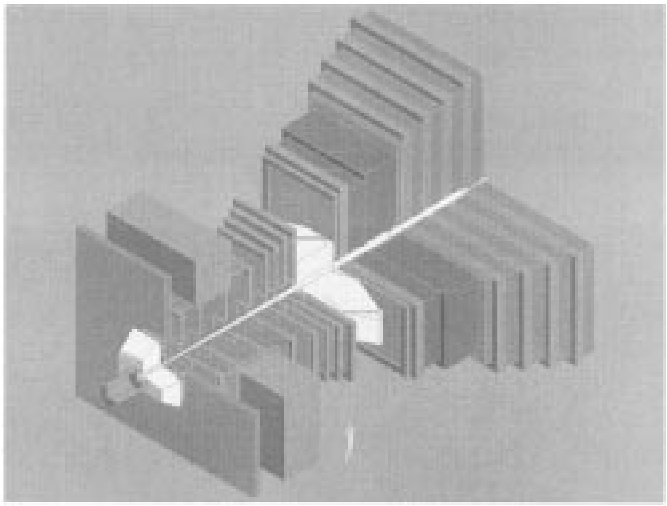

Fig. 1. Sketch of the LHCb detector, one of the four physics detectors planned at CERN's large hadron collider (LHC).

On the right-hand side, the novel LHCb approach is shown, where a controls PC communicates via ethernet with a number of CCPCs, which each control a single front-end electronics board on which they are located. These CCPCs may have sizeable storage capacity, e.g., for configuration data for FPGAs and alike. Furthermore, local actions can be handled directly on the CCPC without bothering the supervising control PC and without network load. At the same time, the control PC is informed about all actions and, thus, can keep track of the status of its complete subsystem.

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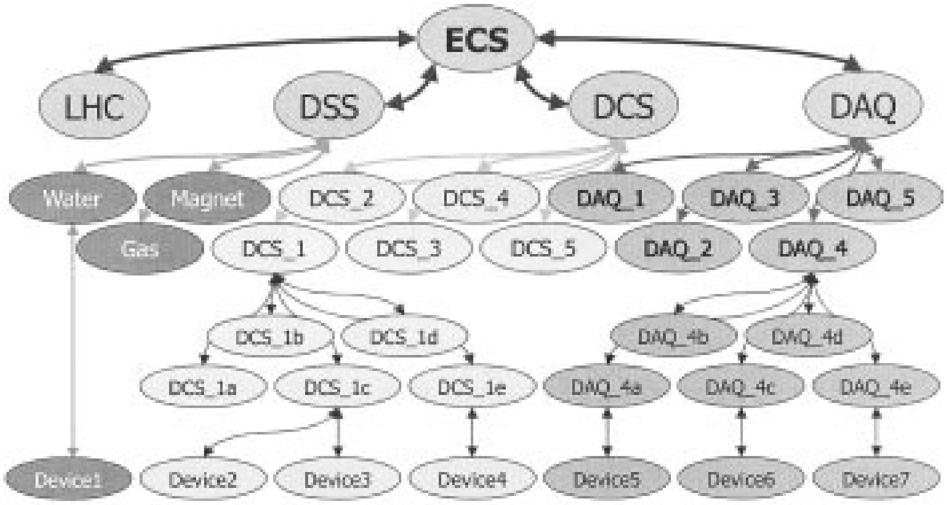


Fig. 2. Systems and devices in the LHCb controls system.

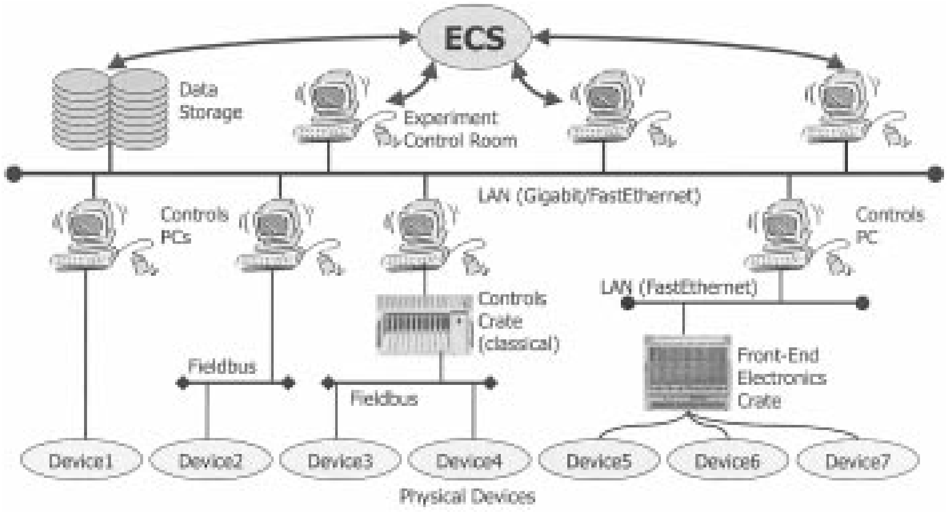


Fig. 3. Basic hardware architecture of the LHCb controls system.

III. Commercial Hardware

The most attractive commercial solution turned out to be the so-called "smartModule" produced by Digital-Logic in Luterbach/CH. These more-or-less credit-card sized PCs are manufactured with several configurations. LHCbs test module has a 586 CPU, 32-MB RAM, and a 2-MB flashdisk (see Table I). What is nice about these modules are their size, the relatively low power consumption, as well as the price of less than 300 CHF (Swiss francs).

Together with the module itself, we used the evaluation board from Digital-Logic, which consists of a power supply, floppy disk drive, and a board to mount the CCPC, which has all necessary connectors (i.e., IDE, keyboard, mouse, VGA, etc.) on it. On the available module, a DOS-like operating system is installed on the flashdisk. We were able to boot the CCPC with Linux from a floppy. A possible approach is to leave the shipped operating system (DOS) and start Linux with the LoadLin-utility from the flashdisk.

TABLE I
Technical Specifications for the Envisaged SmartModule [2]

smartModule SM586PCX	
CPU	ZF586
Storage	2-8 MB flashdisk 16-128 MB RAM
Interfaces (initially available on a proprietary bus system)	ISA, PCI, memory bus VGA, LCD display RS232, USB, LPT, FastEthernet I2C, JTAG
Dimensions	66 × 85 × 12 mm3

IV. Adaptation of the CCPC for LHCb

In order to use the CCPC on front-end electronics boards, a special connection scheme including a glue logic has been developed at CERN. Main issues have been the availability of all needed ports on "standardized" lines—independent of future changes of the CCPC connectors and the so-called reset immu-

TABLE II
AVAILABLE PORTS ON THE LHCB-SPECIFIC ADAPTATION OF THE CCPC

separate reset- and interrupt-lines
power and ground connections
parallel bus: 32 multiplexed address-/data-lines 11 control lines
4× I2C
2× JTAG
parallel port (LPT), RS232
Ethernet 10/100baseT

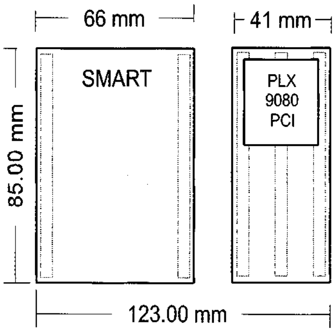


Fig. 4. Block-layout of the adaptation for LHCb with glue logic.

nity of all output ports. This is meant to separate the CCPC outputs from the board in order to have the possibility to reset the CPU without interfering with the front-end electronics board.

In the end, the LHCb adaptation provides the interfaces listed below to the front-end electronics board (see Table II and Fig. 4). The described scheme has been realized on an evaluation board where different reset schemes can be tested together with the interfaces. The evaluation board consists of an embedded PC mounted on a VME module.

So far, the CCPC is integrated on the timing and fast control (TFC) switch [3] and integral to the network-processor-based readout unit [4].

The LHCb ECS Group will provide to all possible users the results and experience with the CCPC hardware and the adaptation, but it is the task for the users to integrate the CCPC on their front-end electronics boards.

V. SOFTWARE

A. Operating System

As already mentioned, the CCPC comes with a customized DOS, which fills about 10% of the standard 2-MB flashdisk. In addition to that, we verified that the standard CERN Linux system (at present RedHat 6.1) runs on the CCPC. In the final system, Linux will be started making use of the LoadLin-utility. This allows keeping at least two versions of the operating system on the flashdisk and choose the version to be run without loading the network with the full kernel image.

Linux has been chosen due to a number of reasons such as high modularity, which would even allow booting from the network with a moderate load when most modules are held on NFS repositories on the controls network, and availability to all developers who can program their control software and interfaces to the ECS on their desktop PCs.

TABLE III
ENVISAGED ROUTINES PROVIDED BY THE LHCB ONLINE GROUP

from controls PC

ccWriteI2C(ipCCPC,I2Caddress,data,size)
ccReadJTAG(ipCCPC,JTAGaddress,data,size)

on the CCPC

ReadI2C(I2Caddress,data,size)
WriteJTAG(JTAGaddress,data,size)

B. Programmer's Interfaces

The online group of LHCb will provide an API for developers from the subdetectors who want to integrate CCPCs into their front-end electronics. These application programmer's interfaces (APIs) will include routines to communicate via the different interfaces as well as basic diagnostic tools, e.g., boundary scan programs. Following the Joint Controls Project (JCoP) naming convention [5] these routines will be named as shown in Table III. Software running on the CCPC will be stored on the network and downloaded at initialization time.

C. Interface to the Controls System

Using CCPCs as universal interfaces to front-end electronics allows for quick exchange of faulty modules, but needs complex configuration of the respective setup. This can be done using PVSS[1] in a very transparent and modular way.

The idea is to define certain board types (cf. Fig. 5) in which the contents of the front-end electronics board and the possible actions and action sequences are defined. This approach provides in the end the possibility to exchange CCPCs only by defining the new hardware address of the physical device placed on the respective board, an operator action that takes only seconds.

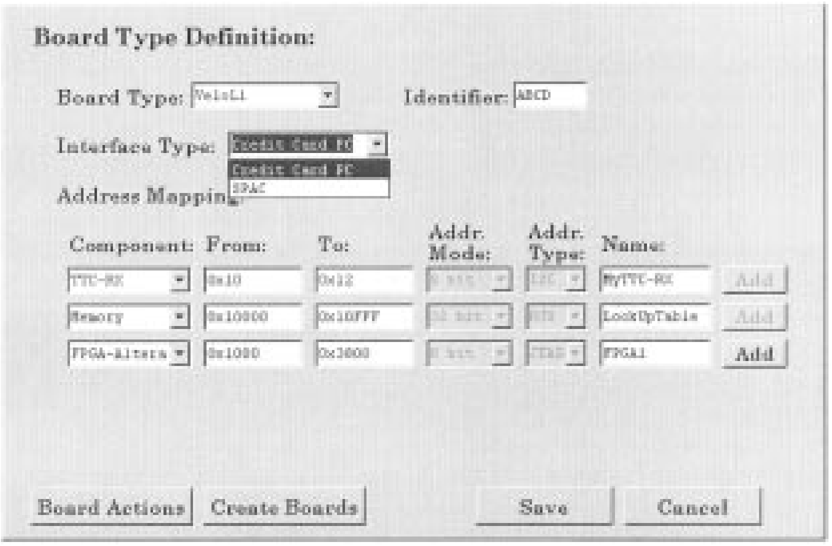
VI. CONCLUSION AND OUTLOOK

The credit-card-sized PC as made by Digital Logic has been preliminarily tested as solution for the controlling of front-end electronics boards. It can straightforwardly be integrated in any controls environment and its various interfaces can be addressed and made available easily to a SCADA system. Tests on the developed evaluation board will be performed as soon as the new version of the CCPC will be available.

Taking this into account, as well as the moderate price, it is one of the three presently supported controls interfaces to front-end electronics for the LHCb experiment.

In the near future, first front-end electronics boards like the TFC switch are available and will be tested with the CCPC. The end of the year at the latest, quasi-final APIs will be provided to

[1] The *Process Visualization and Control System* (PVSS) made by ETM has been chosen as the supervisory controls and data acquisition (SCADA) system for LHC experiments at CERN and will be used in the framework of the CERN JCoP for the four LHC experiments and others.



Board Type Definition:

Board Type: VeloL1 Identifier: ABCD

Interface Type: Credit Card PC

Address Mapping:

Component:	From:	To:	Addr. Mode:	Addr. Type:	Name:
TTC-RX	0x10	0x12	8 bit	I2C	MyTTC-RX
Memory	0x10000	0x10FFF	32 bit	BUS	LookUpTable
FPGA-Altera	0x1000	0x3000	8 bit	JTAG	FPGA1

Fig. 5. PVSS panel for the definition of front-end electronics board types.

developers of front-end electronics boards and the integration in the ECS will evolve.

Acknowledgment

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[2] *Solution Guide 2001*, Digital-Logic, Luterbach, Switzerland, 2001.

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[5] "Guidelines and conventions," JCOP Framework Team, Geneva, Switzerland, 2001.