A test bench
for the Front End Chip
of the AMS RICH

Ludovic ERAUD
Laurent GALLIN-MARTEL

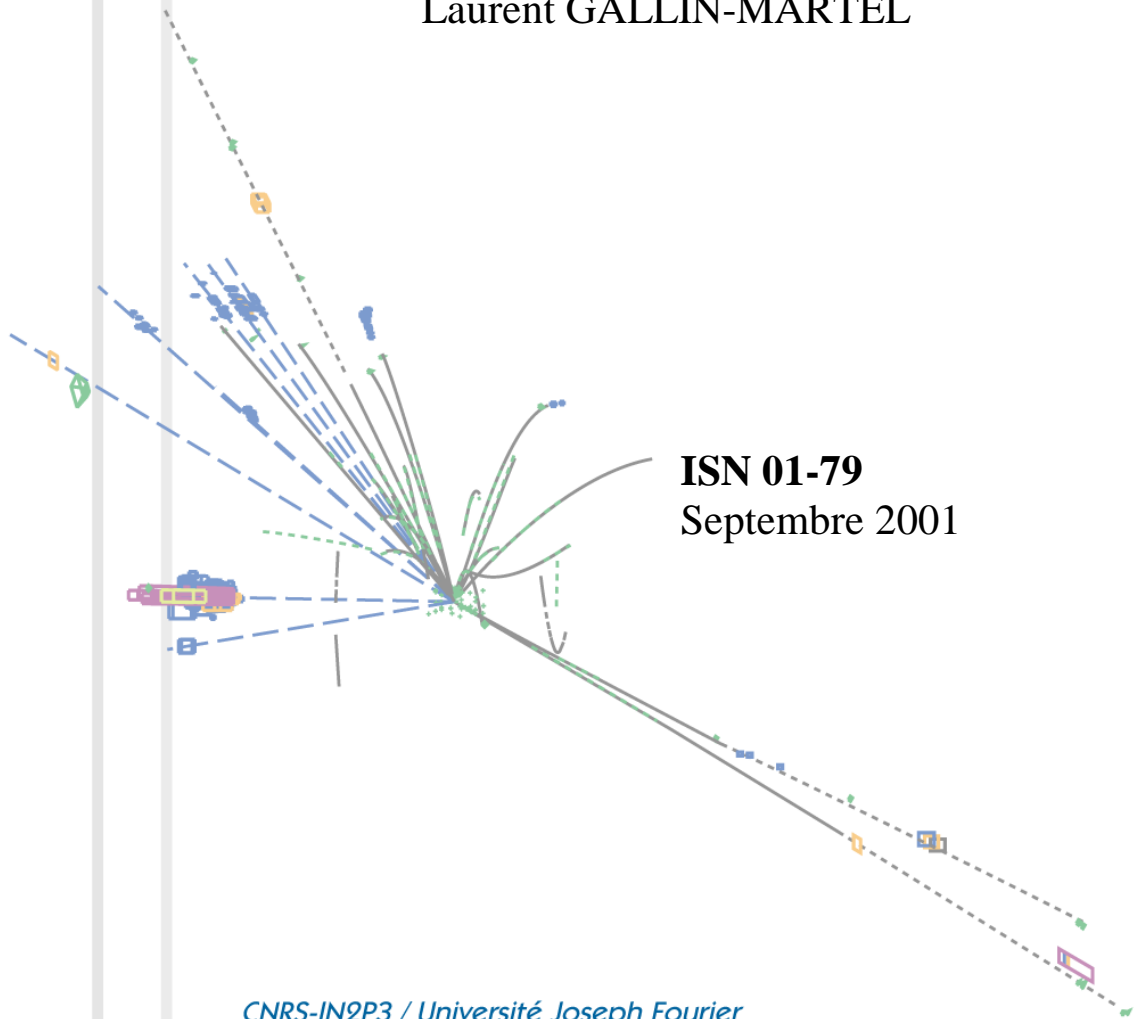Institut des Sciences Nucléaires de Grenoble

Table of contents

1. Introduction

ISN is involved in the development of a Ring Imaging Cherenkov (RICH) counter for the AMS detector [1]. A first integrated circuit was designed in year 1998 to process the signals from the PMTs that equip the RICH detector [2]. A complete prototype, including trigger and tracker detectors as well as a DAQ system, was designed and assembled at ISN [3]. This prototype was tested in laboratory with cosmic rays and a beam test was carried out at GSI (Gesellschaft für Schwerionenforschung mbH, Darmstadt, Germany) in year 1999 with ions [4]. In this early design, the PMTs were single anode ones and the 3 channel front end chip processed 3 PMTs. In order to improve the 2D resolution of the detector (by reducing the pixel size), multi-anodes (16 anodes) PMTs (R5900-M16 PMT manufactured by Hamamatsu [5]) were choosen to equip the upgrade version of the RICH prototype. A new 16 channel chip was designed using the AMS 0.6 μm CMOS technology (Austria Mikro Systeme) and was submitted in year 2000 [6]. The chips of the prototyping run were successfully tested in laboratory and a 250 piece engineering run was ordered in 2001. A set of parameters has to be measured to insure a complete test of the chip (250 chips x 16 channels x 2 gains = 8000 channels). In order to perform these measurements, the design of a computer based test bench was decided. This test bench is described in details in this document, it permits to measure :

- the power consumption,
- the mean value and the width of the pedestal for each channel,
- the integral non linearity for each channel,
- the gain 5 to gain 1 ratio for each channel,
- the peak position of the shaper pulse for each channel,
- the track & hold drop,
- the tagging channel functionality for each chip.

An EXCEL format data sheet is recorded for each chip under test. Then a module written with EXCEL Visual Basic (from Microsoft) makes a selection among these files according to a set of parameters fixed by the RICH functionality requirements. Finally, the result of this analysis can be histogrammed.
The test bench is monitored by a PC running a programme written with LABVIEW (from National Instruments). It includes a GPIB module dedicated to the measurement of the power consumption and a high speed digital I/O board coupled to a custom designed testing board. This allows the complete test of a chip in 1 minute.

2. Front end chip architecture

1. Block diagram

This low power chip is designed using the CMOS 0.6 μm from AMS. It processes signals from a 16 channel PMT (R5900-M16). The chip comprises 16 identical channels coupled to a multiplexing system. Each channel performs the pulse height measurement of the corresponding anode signal. Furthermore a 17th channel is dedicated to the dynode signal processing (Figure 1).
The anode signal amplification is performed by :

- a charge preamplifier,
- a first order differentiation stage with pole-zero cancellation,
- a first order integrator,
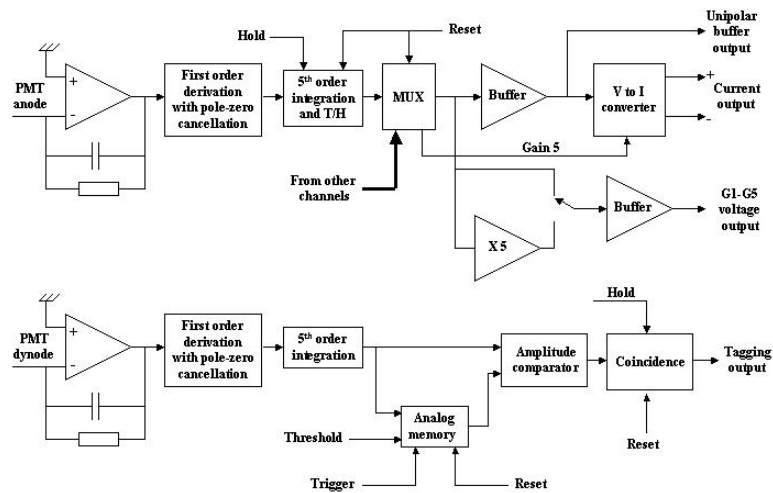- two second order integrators

<u>Figure 1</u>

A gain stage between the two second order integrators allows the compensation of the gain losses in the integration stages. The pulse height is then memorised using a "track & hold" circuit (see **Hold** signal in Figure 1).
This scheme is repeated 16 times this corresponds to the 16 anode signals treatment.

The 16 signals are loaded at the input of a multiplexer. A gain 5 (G5) amplifier associated with the multiplexing system allows two ranges of amplification. Then three output signals are available :

- the **unipolar buffer output** which is a voltage output with no gain,
- the **current output** which is a differential current output with two gains (G1 and G5),
- the **G1-G5 voltage output** which is a unipolar voltage output with two gains.

The dynode signal of the PMT which is the sum of the anode signals can be used to perform an on line data reduction. This channel is also based on a spectro amplifier chain that processes the dynode signal. When a **Trigger** signal occurs the DC level at the output of the last integrator is memorised and added to an external **Threshold** by the **Analog Memory** module. The **Amplitude comparator** circuit compares the next shaper pulse to this memorized value. Then the result of this comparison is latched using the **Hold** signal.
The different analog and digital memories are cleared by the **Reset** signal at the end of the digitalization. The 16 anode and dynode channels are controlled by a clock signal that carries the **Trigger** and the **Hold** signals.

2. Readout chronograms of anode channels

The figure 2 shows a readout sequence of the 16 anode channels. The input signal labelled **CLK** comprises :

- a **Trigger** pulse to initiate the sequence in the logic module,
- a **Hold** pulse to memorize the peak of the shaper pulse,
- 32 pulses to control the mutiplexer (16 pulses for G1 and 16 pulses for G5),
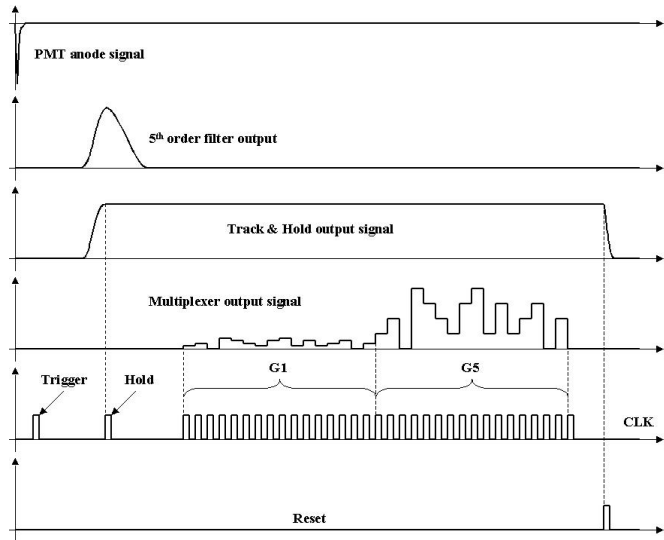- a 33rd to turn the output of the chip into high impedance state.

Figure 2

In figure 2 the **Reset** signal occurs once the readout of the 32 values is completed. However a **Reset** can be sent sooner : just after the first 16 pulses bunch (which corresponds to G1data) in the case there is no use to record the G5 data. The multipexing frequency is limited to 1.5 MHz.

3. Dynode channel synchronization

The tagging channel that processes the dynode signal is implemented to perform on line data reduction. The 5th order integrator used in the spectro amplifier induces a delay in the output signal. This delay (600 ns in the present scheme) is equal to 2.5 times the filtering time constant of the integrator. It is used to sample (on a **Trigger** occurrence) the DC level of the signal. This DC level is added to an external **Threshold** and the particle signal is compared to this value. The **Hold** signal is used to latch the comparator output to generate the output signal **Tagging**. This signal is cleared by the **Reset** signal at the end of the digitization.
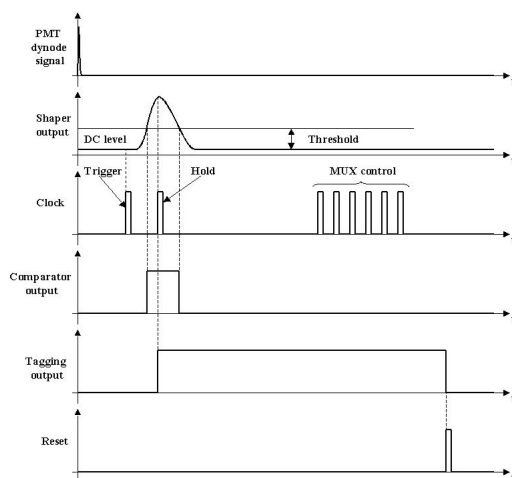

Figure 3

The **Trigger** pulse that also initiates the logic sequence has to be sent even if the tagging facility is not used. Otherwise, the **Trigger** pulse has to be generated less than 600 ns after the particle occurrence. If the tagging is not used the **Trigger** pulse can be generated just before the **Hold** signal (100 ns).

4. Typical features of the chip

- 17 analog inputs : 16 anode and 1 dynode inputs
- 1 analog output : 32 multiplexed channels
- 1 tagging output
- 1 input clock carrying the trigger, the hold and the multiplexing signals
- 1 threshold input
- 1reset input
- maximum frequency for multiplexing : 1.5 MHz
- integrating capacitance : 12 pF
- integral non linearity : $< \pm 0.3\%$
- low gain dynamic range : 250
- high gain dynamic range : 50
- high gain/low gain ratio : $5 \pm 1\%$
- T&H drop : < 1 mV / ms
- Noise : < 0.02 photoelectrons rms
- power supplies : +3 V -2 V
- input and output logic level : 0 to 3V
- analog output amplitude : 0 to 2.8 V
- power consumption : < 13 mW

5. Layout

The chip was designed using the AMS 0.6μm CMOS technology. The area of the layout (shown in figure 4) is 2.9 x 2.2 mm^2.

Figure 4

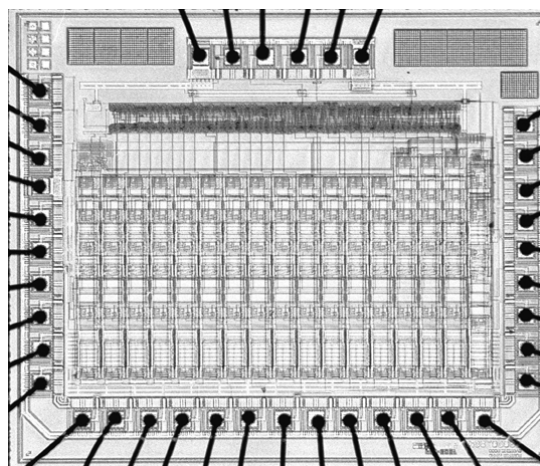Laurent Gallin-Martel (gallin-martel@isn.in2p3.fr), ISN Grenoble

3. Test bench

1. *Test bench block diagram*

The test bench was designed to perform the test of the RICH front end chip in short time and to generate a data sheet containing the test results for each chip. The measured features are :

- the power consumption,
- the mean value and the width of the pedestals,
- the integral non linearity,
- the gain 5 to gain 1 ratio,
- the peak position of the shaper pulse,
- the track & hold drop,
- the tagging channel functionality.

The test bench comprises a PC equipped with a GPIB interface and a high speed digital I/O board. The GPIB module, which is coupled to a power supply (**FEC POWER SUPPLY** in figure 4) and a multimeter, performs the measurement and the recording of the chip current consumption. The digital I/O board (PCI-DIO-32HS manufactured by National Instruments) is connected to a custom design board (**FEC TESTING BOARD**). A second power supply is used to power the testing board. The chip under test is plugged on a socket on the testing board (red area in figure 5).
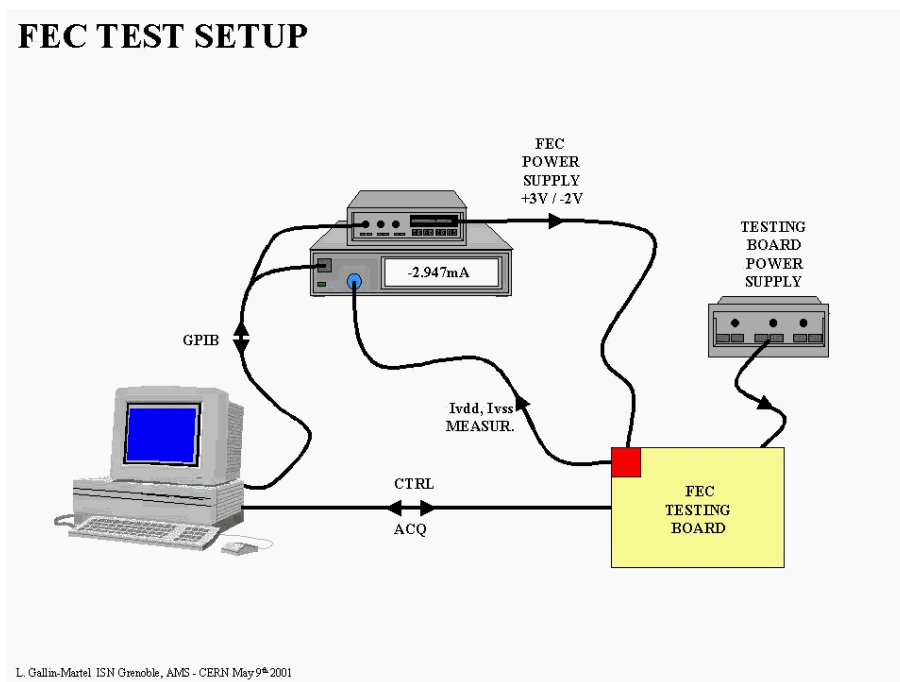

Figure 5

The program that monitors the test bench is written with LABVIEW (from National Instruments). It allows the recording of the chip number and performs the GPIB modules and testing board control.

2. Testing board

The testing board is monitored by the PC, it performs the front end chip control and transfers the measured values to the digital I/O board. It is based on EPLDs (7000s and FLEX10k families from ALTERA) that control a set of integrated functions required for the different parts of the test. The chip under test is symbolized by a red square in figure 6. The other modules on the testing board are :

- a programmable **DELAY LINE** used to delay the **Hold** pulse (shaper pulse reconstruction),
- a 8 bit digital to analog converter (**DAC**) coupled to 4 anode charge injectors (**CI**) (non linearity measurement),
- a dynode charge injector associated to a **Threshold** 8 bit DAC (test of the tagging channel),
- a current to voltage converter (**CVC**) that processes the **FE chip** output current,
- a 12 bit analog to digital converter (**ADC**),
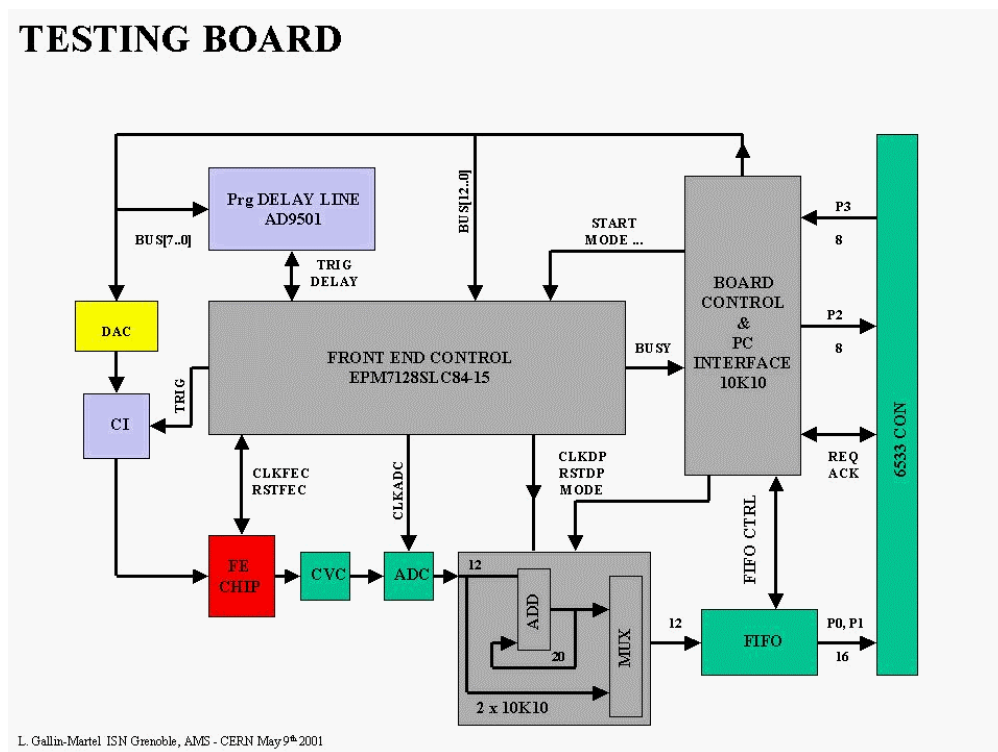- a buffer memory (**FIFO**) to store data before acquisition.

Figure 6

The EPLD chip labelled **BOARD CONTROL & PC INTERFACE** (**BC&PCI**) decodes the orders generated by the PC, configures the different functions of the board and performs the data acquisition. The **FRONT END CONTROL** module is triggered by the **BC&PCI** module and generates the signals required by the chip under test, the **DELAY LINE**, the **ADC**, and … Another EPLD is implemented in the data path. It allows the ADC data to be either directly written in FIFO or averaged using a pipelined adder.

3. BC & PCI module

The relays, the delay line, the **DAC**s, the **FECTRL** and the **DP** module have to be set before the testing board performs a measurement. The acquisition software provides a set of parameters which are registered in the **BC&PCI** module using a 8 bit bus (port 3 of the DIO-32HS board). These parameters are composed of :

- FECTRL[15..8]
- FECTRL[7..0]
- DAC[7..0] : to set the **Charge injectors** or the **Threshold**
- MONO[7..0] : to set the **Hold** pulse delay

FECTRL[15..0] is a 16 bit word transmitted in two times by the acquisition software. The 13 lower bits FECTRL[12..0] are registered in the **FECTRL** module and are used to set a counter that fixes the delay between the **Hold** pulse and the first pulse of the multiplexing sequence (Figure 2). This allows the measurement of the hold drop by increasing the hold duration. The 4 upper bits codes the instruction to be executed by the board. Relays have to be switched to measure the current consumed by Vdd and Vss. The **FECTRL** module triggers either the anode charge injectors (**ACI**) or the dynode one (**DCI**). Concerning the pedestal acquisition none charge injector is triggered.
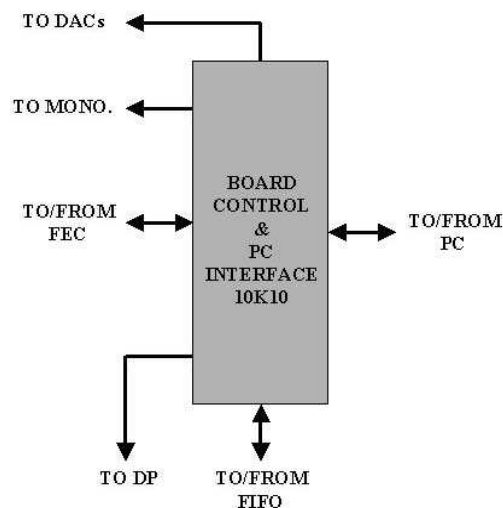

Figure 7

The **DP** is also set by the **BC&PCI** module to average **ADC** data in order to save acquisition time. The possible values of FECTRL[15..13] are :

- 0 : average mode, **ACI** triggered, **DCI** not triggered (pulse acq. and non linearity),
- 1 : Vss current measurement,
- 2 : Vdd currenr measurement,
- 3 : average mode, **ACI** not triggered, **DCI** not triggered (pedestal mean value),
- 4 : transparent mode, **ACI** triggered, **DCI** not triggered (signal to noise ratio),
- 5 : transparent mode, **ACI** not triggered, **DCI** not triggered (pedestal distribution),
- 6 : transparent mode, **ACI** not triggered, **DCI** triggered (tagging channel).

Once the parameters are set, the acquisition software generates a **START** signal to initiate the test sequence. The **BC&PCI** module checks that the **FECTRL** is not busy and triggers it on. The second function of the **BC&PCI** module is the acquisition managing. Data from the **DP** module are written in a FIFO memory controlled by the **BC&PCI**. Two 8 bit ports are dedicated to the acquisition (port 0 and port 1 of the DIO-32HS board) and the signals **REQ1** and **ACK1** perform the data transfer synchronization.

The table below summarizes the DIO-32HS signals involved in the slow control and the data transfer :

Port 0 and port 1	Data acquisition
REQ1 and ACK1	Data acquisition handshake
Port 3	Testing board setting
ACK2 (bit 3 of port 4)	Testing board setting write signal
PLCK1 (bit 0 of port 4)	Relays setting write signal
PLCK2 (bit 1 of port 4)	START signal

4. FECTRL module

The FECTRL module is triggered by the **BC&PCI** module. It consists in a state machine performing the :

- chip under test control (CLK and Reset),
- **ADC** control (CLK),
- **DP** module control (WRITE and RESET),
- **ACI** and **DCI** triggering,
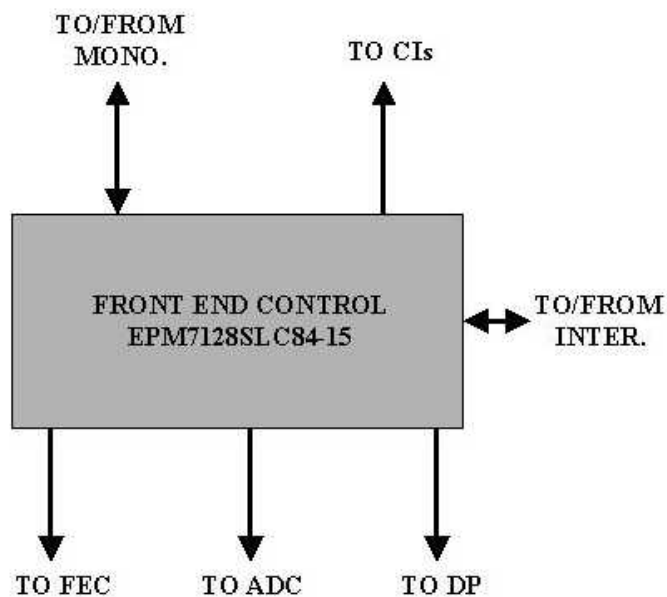- progamable delay line triggering.

Figure 8

Each trigger generated by the **BC&PCI** module induces 256 tests of the front end chip with the same set of parameters.

5. DP module

The DP module allows the data from ADC to be either directly written in FIFO or averaged before writing. In this case the data of each anode channel is added to itself using a 32 in depth pipelined adder.
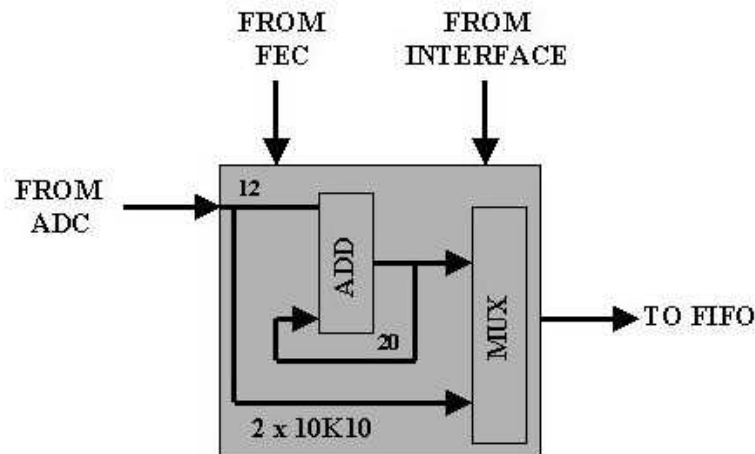
Figure 9

6. Charge injectors (ACI & DCI)

The figure 10 shows the block diagram of the anodes charge injection module (**ACI**). Four **ACIs** are coupled to a **DAC** which provides a DC level controlled by the **BC&PCI** module. On a trigger occurence (trigger sent by **FECTRL**) the four **ACI** modules generate an edge with an amplitude calibrated by the **DAC** output voltage.
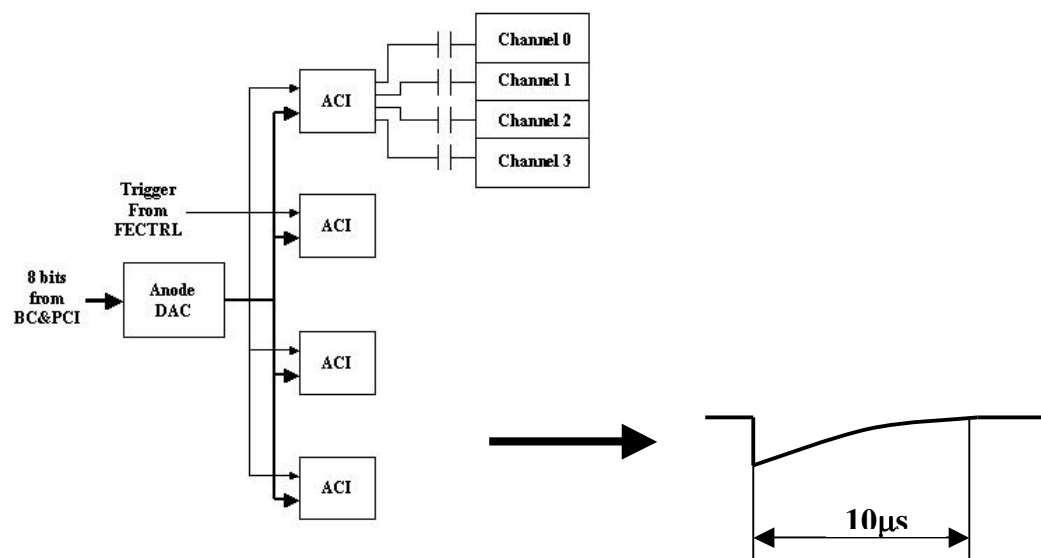
Figure 10

Charges are injected trough a capacitor in the charge preamplifier of each anode channel. An **ACI** module drives 4 anode channels. The same principle is used to test the dynode channel. However, in this case, another **DAC** (also controlled by the **BC&PCI** module) sets the DC level on the **Threshold** input of the chip under test.and the **DCI** provides an edge with a fixed amplitude. The **CIs** consist in 5 daughter boards plugged on the testing board.

7. User Interface

The test bench is monitored by a PC running a program written with LABVIEW. It includes a GPIB module which is dedicated to the measurement of the power consumption and a high speed digital I/O board (coupled to the testing board) that performs the data acquisition. Once the identification number of the chip under test is recorded, the LABVIEW software sets and controls the testing board in order to carry out the complet test of the chip. This programme allows the display of different features of the chip in order to check on line its global functionality :
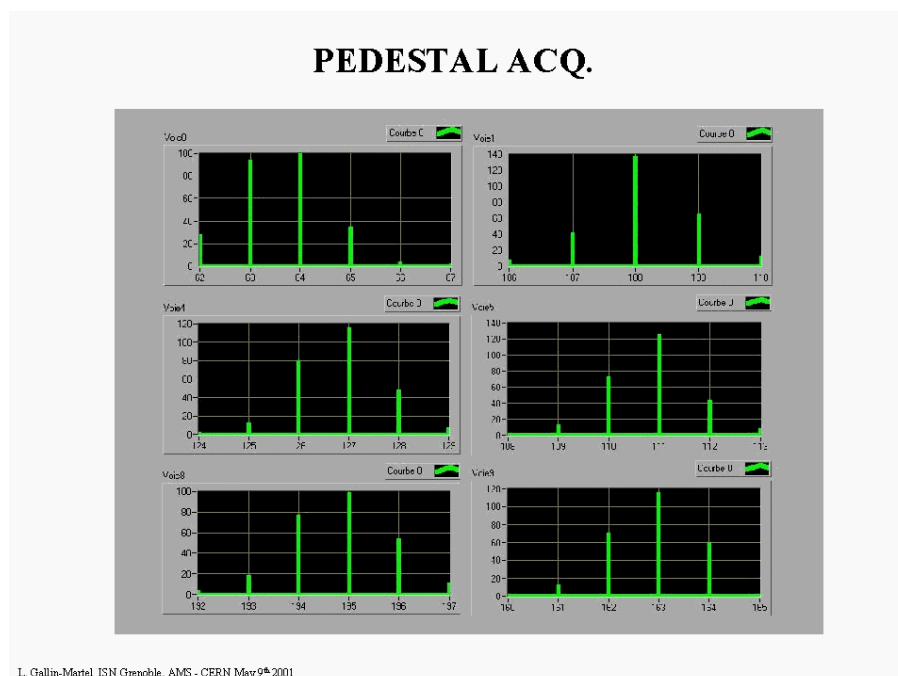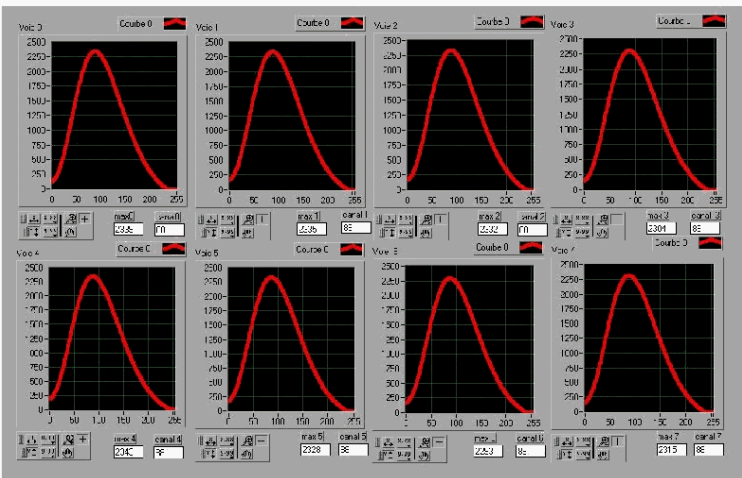

Figure 11

In figure 11 the chip pedestal distributions are displayed. To make the present document more readable only 6 out of 32 channels are plotted in figure 11 and in the following ones. The DP module is used in the transparent mode.

SHAPER PULSE ACQ.

L. Gallin-Martel ISN Grenoble, AMS - CERN May 9th 2001

Figure 12

In Figure 12, the reconstructed shaper pulses are plotted. The programmable delay line is used to delay the **Hold** pulse in order to sample the shaper output signal at different times. Each plot is made of 256 points. Each of these 256 points is the mean value of 256 measurements performed with the same delay line setting. The DP module is used in the average mode.

NON LINERARITY ACQ.
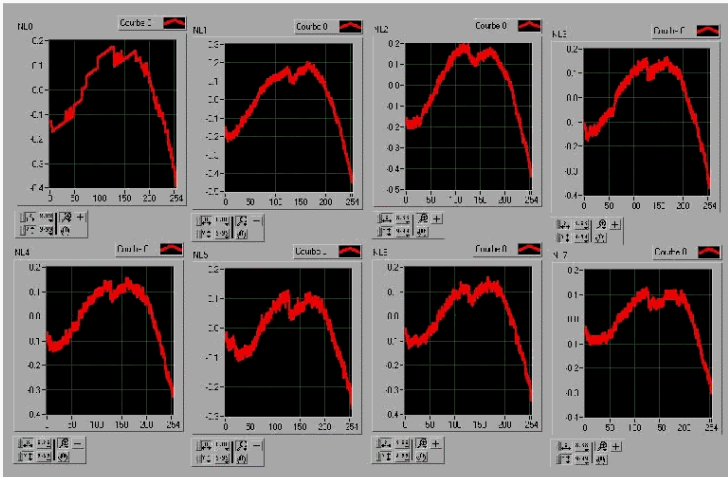
L. Gallin-Martel ISN Grenoble, AMS - CERN May 9th 2001

Figure 13

The plots in figure 13 illustrate the integral linearity of the chip under test. This data acquisition is performed using the digital to analog converter that sets the 4 anode charge injectors. As in figure 12, each plot is made of 256 points and each of these 256 points is the mean value of 256 measurements performed with the same DAC setting. The DP module is used in the average mode.

Moreover the data acquisition sofware generates one file for each measured feature. These files are then processed off line by a Visual Basic module written with EXCEL (from Microsoft). This module generates a data sheet for each chip and performs a selection among these data sheets according to a set of constraints fixed by the RICH functionality requirements.

4. Conclusion

A test bench was developed at ISN to permit a complete test of the 16 channel chip designed to equip the RICH detector of the AMS experiment. This test bench performs in 1 minute the measurement of :
- the power consumption,
- the mean value and the width of the pedestal for each channel,
- the integral non linearity for each channel,
- the gain 5 to gain 1 ratio for each channel,
- the peak position of the shaper pulse for each channel,
- the track & hold drop,
- the tagging channel functionality for each chip.

The test bench is monitored by a PC running a programme written with LABVIEW. It includes a GPIB module dedicated to the measurement of the power consumption and a high speed digital I/O board coupled to a custom designed testing board. An EXCEL format data sheet is recorded for each chip under test. Then a module written with EXCEL Visual Basic makes a selection among these files according to a set of parameters fixed by the RICH functionality requirements. Finally, the result of this analysis can be histogrammed that allows an easy data quality checking.

5. References

[1] : B. Alpat et al, *"Alpha Magnetic Spectrometer experiment for antimatter, dark matter search on International Space Station"*, Nuclear Physics B (Proc. Supl.) 54B 1997, pp 335-343.

[2] : L. Gallin-Martel, J. Pouxe, O. Rossetto, *"A BiCMOS integrated charge to amplitude converter"*, IEEE 1996 Nuclear Science Symposium and Medical Imaging Conference, Anaheim, 3rd-10th November 1996.

[3] : L. Gallin-Martel, J. Pouxe, O. Rossetto, P. Stassi , *"Data read out and formating for PMT based RICH detectors"*, Nucl. Inst. and Meth. A 433, 1999, pp 444-449.

[4] : T. Thuillier, F. Malek, G. Boudoul, J. Ballon, A. Barrau, J. Berger, M. Buenerd, L. Gallin-Martel, A. Menchaca-Rocha, J. Pouxe, *"Experimental study of a proximity Cherenkov counter prototype for the AMS experiment"*, ISN report 01-89, January 2002.

[5] :More details can be found at the following address : http://www.hamamatsu.fr/

[6] : L. Gallin-Martel, J. Pouxe, O. Rossetto, M. Yamouni, *"A 16 channel analog integrated circuit for PMT pulses processing"*, ISN report 01-49, 2001.