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DESIGN AND PERFORMANCE OF A 500 V PULSE AMPLIFIER FOR THE CHOPPER OF THE CERN SUPERCONDUCTING H^- LINAC (SPL)

M. Paoluzzi, CERN - Geneva - Switzerland

Abstract

The Superconducting H^- Linac under study at CERN requires a high performance 3 MeV chopper. The pulse amplifier driving the chopper structure has to provide 500 V on 50 Ω, with rise and fall times below 2 ns at a repetition rate as high as 45 MHz. After analysis of the limiting parameters, potential solutions are described. The detailed design of the selected solution is presented, together with the actual performance of the prototype.

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The Superconducting H^- Linac under study at CERN requires a high performance 3 MeV chopper. The pulse amplifier driving the chopper structure has to provide 500 V on 50 Ω, with rise and fall times below 2 ns at a repetition rate as high as 45 MHz. After analysis of the limiting parameters, potential solutions are described. The detailed design of the selected solution is presented, together with the actual performance of the prototype.

1 INTRODUCTION

In the CERN Superconducting H^- Linac (SPL) the required beam time-structure is created in the chopper line. This line transports the beam through the travelling-wave deflectors where an electric field deviates part of it towards a beam dump. The chopper deflecting structures are essentially two 50 Ω, micro-strip, meander type transmission lines facing each other and driven with opposite polarity signals [1,2,3]. The main characteristics of the required driving pulse are:

Pulse amplitude	0 to 500 V or 0 to –500 V (depending on the chopper plate)
Rise and Fall Time (10%- 90%)	2 ns
Pulse Length	8 ns to 1700 ns
Max Repetition Frequency	45 MHz
Burst Length	2.8 ms
Burst Repetition Frequency	50 Hz

Table 1-Main Characteristics of the Driving Pulse.

2 DESIGN CONSIDERATIONS

Generation of single polarity pulses with transition times of ~2 ns implies a frequency response extending from DC to above 200 MHz. Making use of the pulse burst pattern, the low frequency limit could possibly be shifted above DC but should still be much lower than that imposed by the burst length (i.e. a few Hz). To limit the bandwidth required from each amplification stage, the pulse amplifier should use the minimum number of cascaded stages and be optimized for transition speed rather than gain linearity. The high output voltage, peak-power (5 kW) and repetition-rate limit the choice of usable devices to vacuum tubes. Although attractive at first sight, the distributed amplifier configuration is not recommended: the need of loading the anode line at both ends doubles the required power, increases the number of tubes and thus the amplifier's rise-time. Since tubes with high enough gain-bandwidth product exist, a standard configuration is preferable. To generate positive and negative pulses with vacuum tubes, some kind of polarity inverter is required. Since we also need to match the 50 Ω characteristic impedance of the chopper deflecting structure to the required plate load, RF transformers must be used for signal inversion and matching. This brings along the extra complication of the transformer low frequency cut-off. A transformer with a bandwidth extending from a few Hz to >100 MHz does not seem to be feasible and a DC and low frequency restore scheme has to be implemented. To overcome these difficulties, the design is based on the idea of generating the low and high frequency part of the spectrum with two separate amplifiers. Their output signals are then merged at the beam. Since beam dynamics require minimization of the chopper line length, the deflecting structures will be inserted in the chopper-line quadrupoles. Their ground planes, instead of being grounded, will be used as deflectors to provide the low frequency part of the field.

3 DESIGN PRINCIPLE

The basic component of the pulse amplifier is the wide-band, delay-compensated, transmission-line transformer. It consists of transmission lines threaded through ferrite in order to increase the common mode impedance and extend the bandwidth towards the low frequencies. Since the high frequency response is theoretically independent of the transmission line physical length, the ferrite cross-section and volume can be adjusted to obtain the desired low frequency cut-off and to stay below ferrite saturation. Ideally, when connected as an inverting transformer and used as a three port device it behaves as a diplexer: a port will exhibit a low-pass response, a second one a high-pass response and the third an all-pass response. If the low-pass and high-pass cut-off frequencies are set at the same value, perfect signal separation (or recombination) in the frequency domain can be obtained. Figure 1 shows the principle on which the positive output amplifier is based.

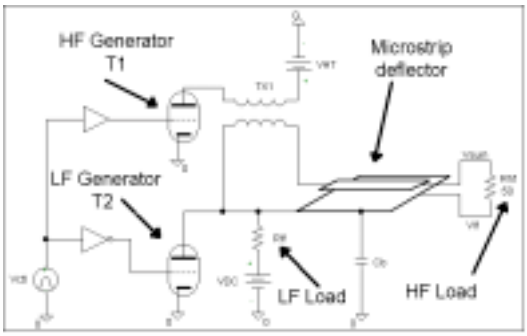

Figure 1- Basic Scheme for Positive Output Amplifier

Two current generators (i.e. vacuum tubes) amplify the same input signal. T1 takes care of the high frequency part of the spectrum while T2 generates the low frequencies. The HT supply to T1 is inserted at the

grounding point of TX1 primary winding. The grounding point of the secondary winding is used for introducing the low frequencies. The power supply for T2 comes through the low frequency load R_{lf} so that the frequency response extends to DC. The high-pass cut-off frequency is set by the transformer's common mode inductance and by R_{hf} while C_b and R_{lf} set the low-pass cut-off. Figure 2 plots the simulated response (SPICE).

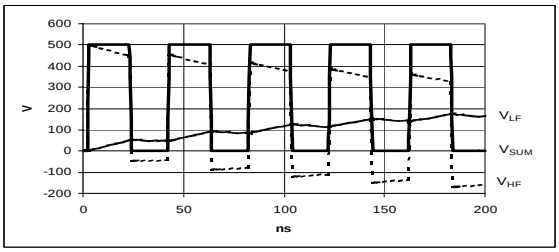

Figure 2- Simulated Response (Positive Output)

To produce a negative pulse, an inverting transformer and a slightly different connection of the low frequency tube is required.

4 HIGH FREQUENCY AMPLIFIER

The tube used in the output stage is the YL1056 tetrode whose main characteristics are listed in Table 2.

Anode DC Voltage	3.5 kV	C_{gk}	42 pF
Anode Dissipation	2 kW	C_{gs}	60 pF
Screen Voltage	500 V	C_{ag}	0.05 pF
Screen Dissipation	30 W	C_as	8.4 pF
Grid Dissipation	5 W	I_a@V_{gk}=0 V_a>1kV	5.5 A
I_s @ V_{gk}=0V, V_a=1.2kV	0.3 A	I_a @V_{gk}=-40 V_a>1kV	0.2 A

Table 2 YL1056 Main Characteristics

Since the stray capacitance of the tube plate radiator cannot be compensated in a distributed line, the total tube output capacitance becomes ~15 pF. Four paralleled tubes loaded with 12.5 Ω are therefore used to achieve the required high frequency cut-off. The anode circuit (Fig.3) is basically composed of a 4 to 1 inverting transformer. It provides DC to RF decoupling for connection to the anode power supply, as well as the input for low frequency restoration (positive output).

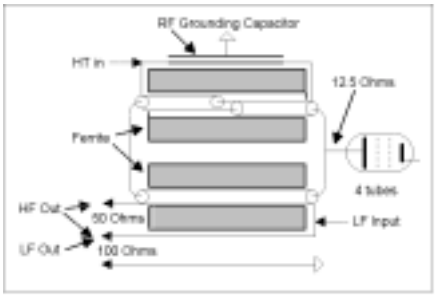

Figure 3- Anode Circuit Simplified Schematic

The common mode inductance seen on the 50 Ω output is 8 µH and saturation of the ferrite due to DC current flowing from the DC supply only changes this value by ~4%. The –3 dB bandwidth limits are then

$$f_1 = \frac{50}{2\cdot\pi\cdot 8\cdot 10^{-6}} \approx 995 \quad \text{kHz}$$

$$f_2 = \frac{1}{2\cdot\pi\cdot 60\cdot 10^{-12}\cdot 12.5} \approx 212 \quad \text{MHz}$$

A low inductance (<5 nH) inserted between the anodes and the transformer can improve the high frequency limit at the price of some overshoot. With 5% overshoot, the –3 dB bandwidth can reach 300 MHz and the transient time be as low as 1.2 ns. Maximum induction is limited to 25 mT at f_1 (B_{sat}~200 mT). With 15% duty-cycle, 5.5 A drawn by each tube and an anode DC voltage V_{HT}=1.55 kV, the anode dissipation will be P_a~1.3 kW. Corresponding screen grid dissipation is P_s~23 W. The high tube gain permits to drive the grid with LD-Mosfets* that can typically work with drain voltage of ~60 V and up to frequencies in excess of 1 GHz. The use of these devices, driven by a strongly non-linear gate driver, limits the number of cascaded stages, thus optimizing the amplifier transient time. To avoid distortion of the recombined pulse, both amplitude and phase relations among the different harmonic components of the signal must be preserved. Therefore this recombination scheme only works if the low-pass and high-pass responses are of first order. The tube input circuit must thus have a low frequency response that extends well below the crossover point (f_1). The four parallel tubes, connected in common cathode configuration, have independently driven grids (Fig.4). The input capacitance of each tube (~100 pF) is charged through R_{grid} and discharged by the MRF182 Mosfet. This device has a maximum drain-source voltage of 65 V, draws more than 10 A, dissipates about 60 W and works up to 1 GHz. L_a, L_b and L_c are leakage inductances due to the circuit layout; they give some desired overshoot to the grid voltage. Fast, high current, strongly non-linear gate drivers are used to control the MRF182 gate. They provide the charge required to switch the device from an open state to saturation and vice versa. To limit the power dissipated in R_{grid} and in the MRF182, the 63 V supply is only applied when required, and control is provided via the Bias CTL input. The tubes are biased well below I_a=0 A by the dedicated supply. A prototype has been constructed and measured performances are described in section 6.

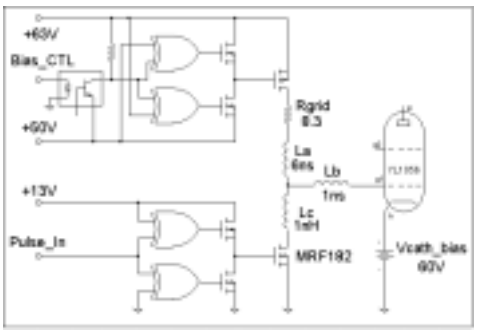

Figure 4-Input Circuit Simplified Schematic

* Lateral D-Mosfet

5 LOW FREQUENCY AMPLIFIER

To avoid pulse length limitations or distortion around the transients, the active devices used in the low frequency amplifier must provide current transients with about the same speed as those of the high frequency amplifier. For these reasons, unless a linear amplifier is used, power Mosfets cannot be employed and the low frequency amplifier will also use a YL1056. The total capacitance of the micro-strip deflecting structure reference plane to ground, the connections between the amplifier and the deflector, the active device output capacitance, etc. have been estimated to be well below C_b=800 pF. For a 1 MHz cut-off frequency, the load can be 100 Ω and the maximum required current amounts to 5 A. A single tube, with the same grid driver, will thus be used. To obtain a positive output pulse, the tube reference level will be shifted to –1 kV and the low frequency load supplied with +500 V. For the negative output pulse, the tube reference level will be shifted to –1.5 kV and the low frequency load simply grounded. Level shifting of the control signals will not be a major problem as no linearity is required, only proper positioning of the transition fronts.

6 HIGH FREQUENCY AMPLIFIER TESTS

Measurements of the output circuit give a –3 dB response from 1 MHz to 220 MHz with a transient time of ~1.4 ns. As expected, the grid driver provides a 57 V pulse with fronts of ~2.5 ns (Fig. 5). The amplifier output signal is shown in Fig. 6, 7 and 8.

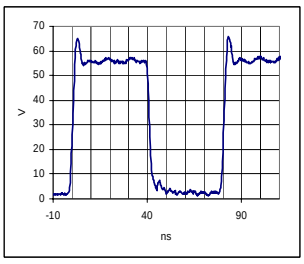

Figure 5-Grid Voltage Pulse

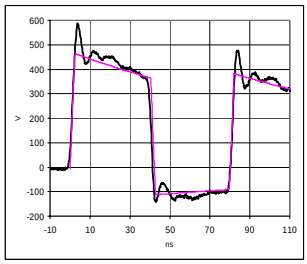

Figure 6-Output Pulse

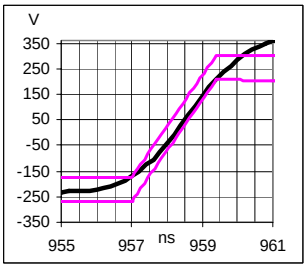

Figure 7-Rising Front

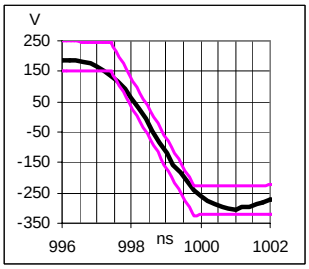

Figure 8-Falling Front

The amplitude is lower (475 V) than expected and transition times are longer (2.5 ns). This is partly due to a 'hidden' resistance in the cathode circuit. It limits V_{gk} by ~17% thus reducing amplitude and transition times by a similar amount. As plotted in fig. 6, the droop follows the superimposed simulated response. This confirms the low frequency cut-off. The minimum pulse length the pulse amplifier can provide is 7.5 ns, and the maximum repetition frequency is 45 MHz. Unfortunately saturation effects in the grid driver do not allow to obtain both at the same time.

7 FUTURE DEVELOPMENTS

To meet the switching time and output voltage specifications, the 'hidden' resistance existing in the cathode circuit must be drastically reduced. Additional switching speed improvements might come from the use of Mesfets working with higher drain-source voltage. Tests with a new device family of SiC semiconductors working at 100 V are foreseen. Saturation problems in the driver have also to be solved to reach at the same time the minimum pulse length and maximum repetition rate specifications. To simplify the overall circuit, a single HT supply will be used for the anode and screen voltages. A cathode self-bias circuit will be introduced to avoid the cathode bias supply.

8 CONCLUSIONS

A technically viable solution for the generation of the CERN SPL chopper driving voltage has been identified. It is based on the idea of generating the low and high frequency components of the required spectrum with two different generators. The sum of the two signals is obtained using the deflecting structures virtual ground planes as low frequency deflectors. To limit the chopper line length, the deflecting structures are inserted in the quadrupoles. A prototype of the high frequency generator, which is the most critical component, has been produced and tested. Although the measured characteristics do not comply with specifications yet, they still demonstrate the effectiveness of the chosen layout and show where substantial improvements can be obtained. A complete prototype will be produced by the end of the year.

ACKNOWLEDGEMENTS

I would like to thank Mr. F. Caspers for all the ideas he gave and suggestions he made concerning this pulse amplifier. Thanks also to Mr. M. Haase for his helpful collaboration in the prototype construction.

REFERENCES

1 M.Vretenar (editor), Conceptual Design of the SPL, a High Power Superconducting H^- Linac at CERN, CERN 2000-012

2 M.Vretenar (editor), Proposal for a 3 MeV Test Facility in the PS South Hall, CERN PS/RF Note 2001-017

3 F.Caspers et al., Fast Chopper Structure for the CERN Superconducting Proton Linac, in this conference.