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ANTIPROTON BEAM PARAMETERS MEASUREMENT BY A NEW DIGITAL-RECEIVER-BASED SYSTEM

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Abstract

The Antiproton Decelerator (AD) provides the users with very low intensity beams, in the 10^7 particles range, hence prompting the development of an innovative measuring system, which was completed in early 2000. This system measures antiproton beam intensity for bunched and debunched beams, together with momentum spread and mean momentum for debunched beams. It uses a state-of-the-art Digital Receiver board, which processes data obtained from two ultra-low-noise, wide-band AC beam transformers. These have a combined bandwidth in the range 0.02 MHz - 30 MHz and are used to measure AC beam current modulation. For bunched beams, the intensity is obtained by measuring the amplitude of the fundamental and second RF Fourier components. On the magnetic plateaus the beam is debunched for stochastic or electron cooling and longitudinal beam properties (intensity, momentum spread and mean momentum) are measured by FFT-based spectral analysis of Schottky signals. The system provides real-time information characterising the machine performance; it has been used for troubleshooting and to fine-tune the AD, thus allowing further improved performance. This system has been operating since May 2000 and providing beam intensity data to the users on a routine basis since late 2000. A dedicated software package was expressly developed to take care of the control, data acquisition and processing phases. It consists of three main codes, namely a GUI, a Real Time Task and a Low Level Code. This report gives an overview of both the hardware and software developed.

Geneva, Switzerland
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1. INTRODUCTION

A new CERN machine for low energy antiprotons production, named the Antiproton Decelerator AD [1], has completed its commissioning phase, becoming operational in 2000. The intensity of its antiproton beam varies from some $5x10^7$ particles at 3.5 GeV/c to some $2.5x10^7$ at 100 MeV/c. Traditional DC beam transformers do not work at these low intensities, hence two ultra-low-noise pick-ups are used [2].

The new digital-receiver-based AD beam-diagnostic system acquires and processes the data generated by these pick-ups. The system measures beam current intensity, momentum spread and mean momentum throughout the AD cycle. It therefore enables a real-time evaluation of cooling and deceleration performance during the AD cycle. In addition, the intensity thus measured is also made available to and used by the experimental teams.

2. SYSTEM OVERVIEW

Figure 1 gives an overview of the system.

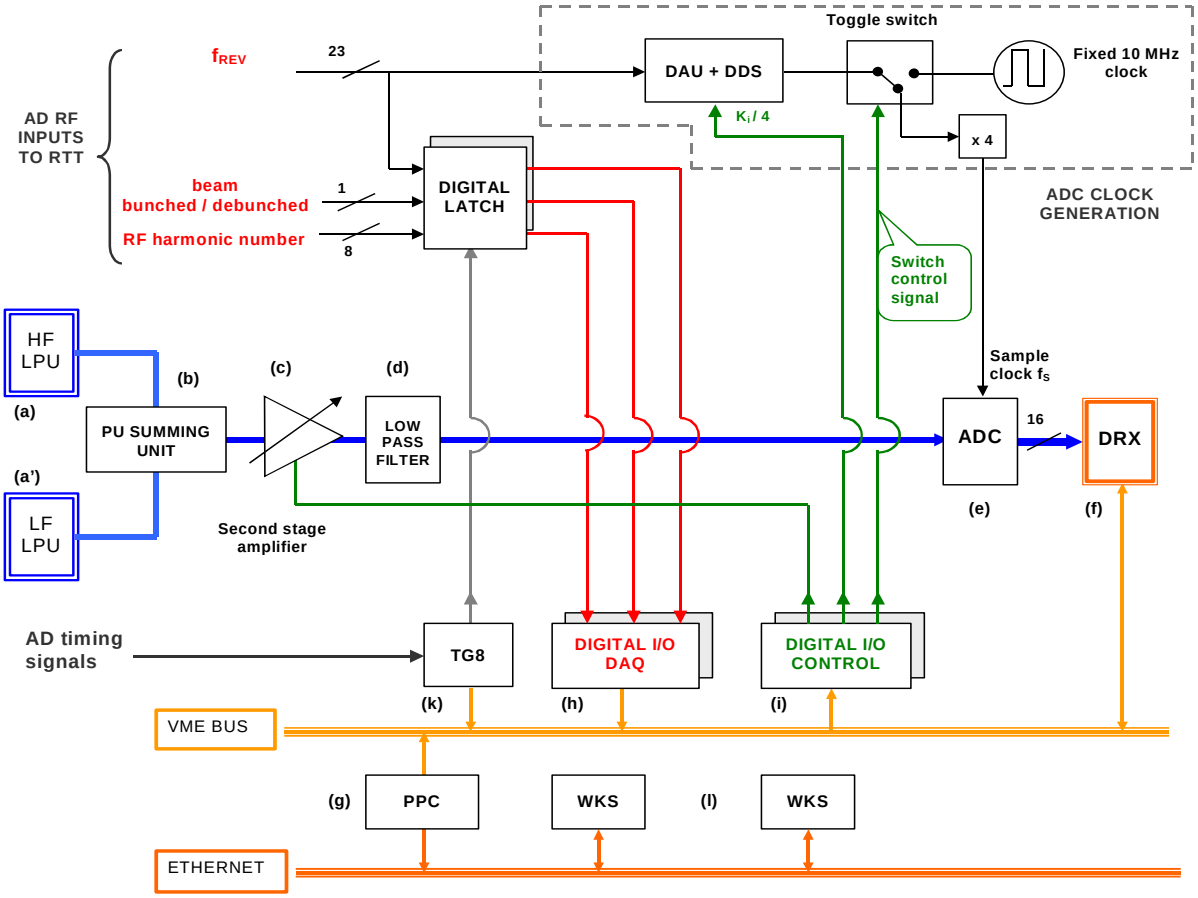

Figure 1: *Schematic view of the new digital-receiver-based system for the measurement of antiproton beam parameters.*

The inputs from the two longitudinal pick-ups (LPUs) **(a)** and **(a')**, optimised respectively for high (HF LPU) and low frequency (LF LPU) [2], are filtered and added together by a summing unit **(b)** to give the total input over the whole frequency range. The resulting signal is amplified by a variable-gain, remotely-controlled second-stage amplifier **(c)**. After a 16 MHz low-pass filter stage **(d)**, the signal is digitised by a Pentek 6441 fast ADC **(e)**. The data are digitally down-converted and processed by a Pentek 6510 Digital Receiver (DRX) board **(f)**, which is set up before each measurement. Finally the Real-Time Task (RTT), running in the PowerPC (PPC) VME board **(g),** collects, post-processes and stores the data for later display. The RTT uses the Digital I/O DAQ unit **(h)** to acquire, from the AD RF system, the information needed to optimise the choice among various user settings. The RTT controls several hardware subsystems through the Digital I/O Control **(i)** and is synchronised to machine events by a timing reception and generation module (TG8) **(k)**. Users access the system, to evaluate data and to set various parameters, through the local Ethernet via an application program running on any workstation **(l)**. The system has been providing beam intensity, momentum spread, revolution frequency and debunched beam power spectral density *PSD* since May 2000.

3. HARDWARE

3.1 Longitudinal pick-up

Two LPUs [2], located in a straight section of the AD ring, provide the frequency bandwidth 0.1 MHz to 16 MHz required for the measurement of Schottky signals and beam intensity. They also improve the S/N ratio by lowering the overall noise floor. The noise power spectral densities of the two LPUs are given in Figure 2 and Figure 3 as functions of frequency and are summarised in Table 1.

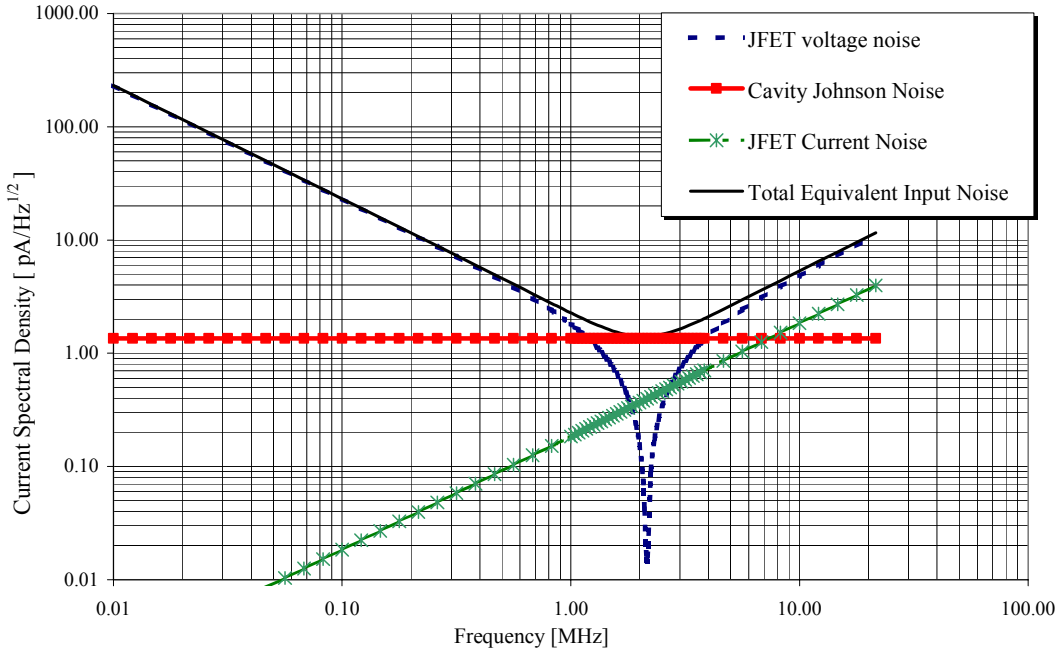

***Figure 2**: Equivalent input current noise for the HF LPU.*

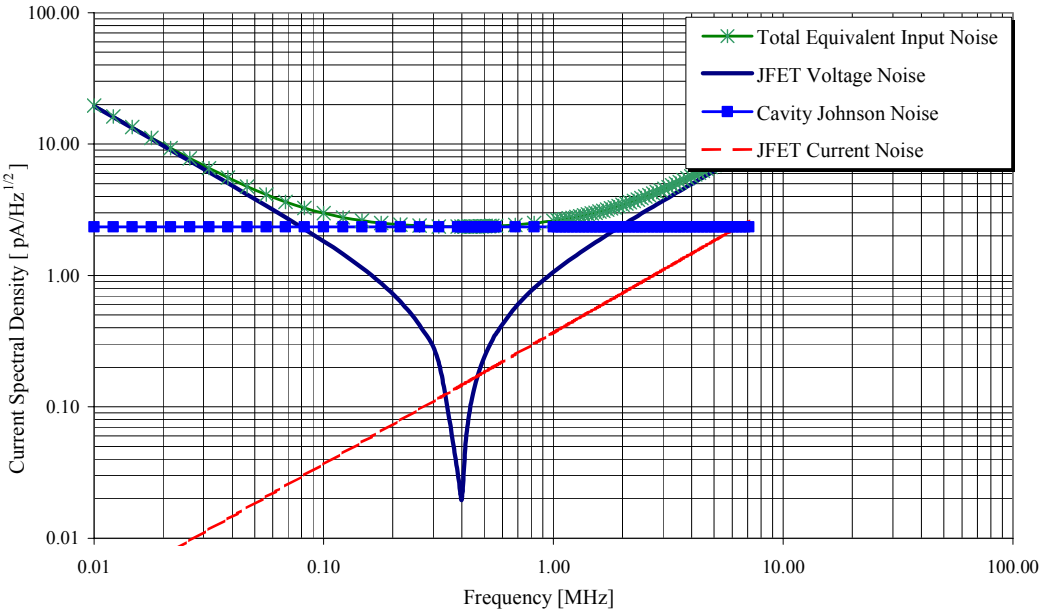

***Figure 3**: Equivalent input current noise for the LF LPU.*

	Total response bandwidth/MHz	**Low noise bandwidth/MHz**	**Low noise value / pA/Hz^½**
HF LPU	0.25 – 30	[1 - 3]	1.5
LF LPU	0.02 - 3	[0.1 – 1]	2

***Table 1:** Nominal characteristics of the HF and LF LPUs.*

The LPUs are high-Q resonant devices, hence with a minimised Johnson noise. They are broad-banded by an active feedback, around the head amplifier, which simulates a "noise-free" resistor in parallel with the resonant circuit, as shown in Figure 4. The design of the LPUs and the corresponding head amplifiers ensures that the total equivalent input noise, in a part of the bandwidth, is dominated by the cavity Johnson noise. This can be seen in Figure 2 and Figure 3. Such bandwidth is indicated as the low-noise bandwidth in Table 1.

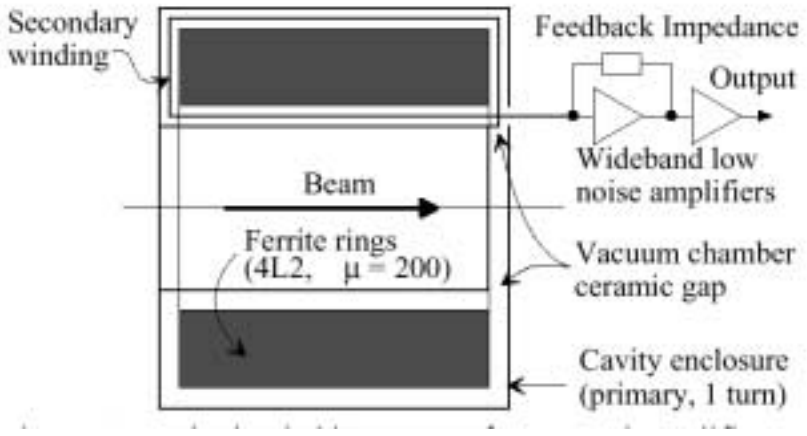

***Figure 4**: The HF LPU ferrite-loaded beam transformer and amplifier.*

3.2 PU Summing Unit

The outputs of the two LPUs are filtered and added together by the PU Summing Unit, to give a flat frequency response over the 0.02-30 MHz bandwidth. The low frequency pick-up signal is low-pass-filtered, the high frequency pick-up signal high-pass-filtered, giving the required bandwidth when the two are summed.

3.3 Second-stage amplifier and filter

The dynamic range of the LPU output signals is very broad. It varies from a minimum corresponding to Schottky signals to a maximum given by a bunched-beam signal measured at a frequency equal to a harmonic of the revolution frequency f_{REV}. A second-stage amplifier, located between the head amplifier and the ADC, adapts these signals to the ADC input voltage range, which is 0.5 V to –0.5 V. The maximum gain of the second-stage amplifier is such that the LPU noise level is lifted by 12 dB over the ADC quantization noise. In this way, the system total noise is dominated by the cavity's Johnson noise. The minimum gain is specified so that the head-amplifier's maximum output voltage is lowered to the ADC maximum voltage.

Two software-selectable, elliptic low-pass filters with a passband of 7 MHz and 16 MHz are included on the board hosting the second-stage amplifier. In fact, the same type of hardware was conceived to treat signals coming from both transversal and longitudinal PUs, needing a 7 MHz and a 16 MHz filtering action, respectively.

A software-selectable dithering action, carried out by a means of low-pass-filtered noise, is implemented on the same board to reduce spurious contents when the measured signal and the ADC clock are not harmonically related.

The second-stage amplifier and filter board characteristics are summarised in Table 2.

Amplifier gain	16 steps	-1 dB to 51 dB
Output power	1dB compression	23 dBm
7 MHz filter	Total pass band flatness	< ± 0.1 dB
	Stop band > 14 MHz	Attenuation > 60 dB
16 MHz filter	Total pass band flatness	< ± 0.2 dB up to 7 MHz
		< ± 0.4 dB up to 16 MHz
	Stop band > 24 MHz	Attenuation > 60dB
Z_{IN} and Z_{OUT}	(S_{11}, S_{22} at 10 MHz)	50 Ω (-40 dB, -40 dB)
Input channel	Multiplexer	2 : 1 (+ monitor output)
	Separation	< 100 dB at 1 MHz, < 80 dB at 10 MHz
	Switch time	< 1 ms
Dither noise	< 400 kHz	-100 dBm
	> 600 kHz	Under noise level

Table 2*. Second stage amplifier and filter board characteristics.*

3.4 External ADC clock generator

One of the measurement requirements is to take samples at the highest possible frequency, so as to minimise the quantization noise spectral density. The maximum allowed ADC sampling frequency f_S is 40 MHz. For the debunched beam case, a fixed f_S of 40 MHz is therefore acceptable. For the bunched beam case, f_S must be made to vary following the varying revolution frequency f_{REV} on the deceleration ramps, as explained under 5.2. Hence f_S must be a multiple K_i of f_{REV}. The choice of K_i is such that the product $K_i f_{REV}$ is the maximum value smaller than or equal to 40 MHz.
The DAU+DDS unit (see Figure 1) can provide a signal with a maximum frequency of 10 MHz. A frequency multiplier equal to 4 is therefore needed in order to achieve the maximum f_S. For this, a Phase Locked Loop (PLL) is used. Its output frequency ranges between 20 MHz and 40 MHz, its lock-in time is approximately 100 µs and its phase noise at 30 kHz from the central frequency is greater than 125 dBC. For a debunched beam, the PLL is fed with a fixed-frequency signal from a commercial 10 MHz atomic clock, thus generating the fixed f_S equal to 40 MHz.

3.5 Pentek 6441 ADC board

The ADC is a customised version of the Pentek 6441 model, a dual channel, 12-bit, VMEbus board that operates at sampling rates of up to 41 MHz. A block diagram of the as-received board is shown in Figure 5. Two analogue input signals are first amplified and then low-pass filtered prior to being fed to the Analog Devices 12-bit A/D chip. The digital signal is multiplexed so that both signals are made available on two different flat cables (Upper and Lower).

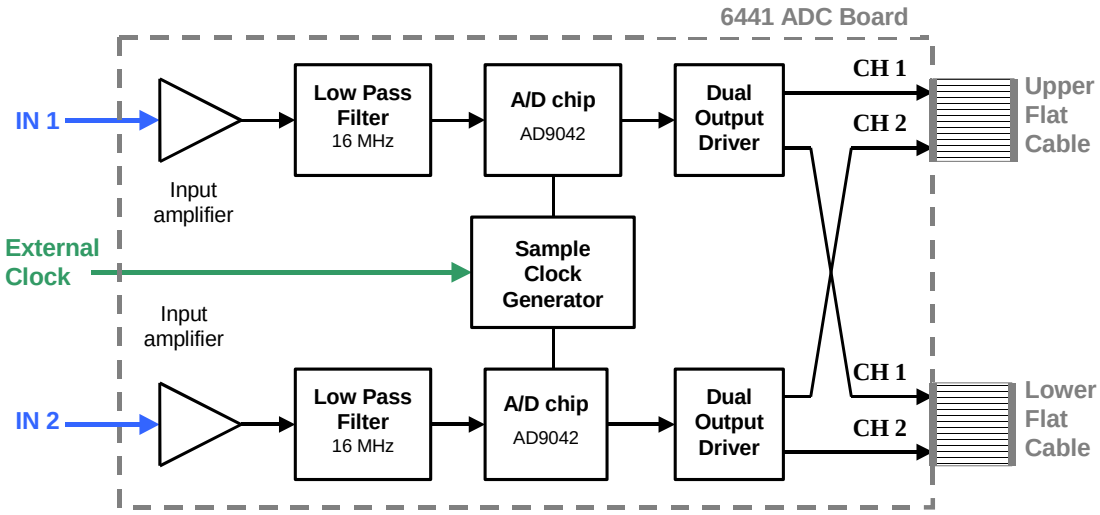

***Figure 5**: Schematics of the as - received Pentek 6441 ADC. We improved the S/N ratio by 12 dB, by means of an in-house modified analogue input front-end.*

Figure 5 shows that the ADC board may function with an Internal (Sample Clock Generator) as well as with an External Clock. In this system, an external clock controls the board: this is necessary because f_S changes according to the beam state. The ADC output is 12 bits, while the DRX input is 16 bits. As a consequence, the output data lines have been arranged at the

data connector such that the 12 MSB of the DRX are driven by the outputs of the ADC [3, 4]. The main ADC features are noted in Table 3.

Analogue Inputs	Number Type Signal range	2 Single-ended, SMA connector, AC-coupling, 50 Ω input impedance. -0.5 V to +0.5 V (- 1 V to + 1 V in the as-received board)
Input filters	Number Passband Stopband	2, can be bypassed (jumper-selectable). [1 kHz - 16 MHz] 26 MHz
A/D conversion	Converters number Model Resolution Sampling frequency Signal to Noise ratio SINAD Spur-free dynamic range	2 Analog Devices AD9042 12 bits Up to 41 MHz ≥ 50 dB (originally specified as ≥ 65 dB) ≥ 60 dB ≥ 70 dB (originally specified as > 75 dB)
Internal sample clock	Sampling frequency	40 MHz, user-replaceable crystal. 256 different sample clock rates allowed through internal divider DIP-switch.
External sample clock	Connector Bandwidth Signal types	Front panel SMA, 5 kΩ input impedance, DC coupling. DC to 41 MHz Single-ended or differential (jumper-selectable).

Table 3*: Pentek 6441 ADC board specifications.*

Initial off-line testing of the 6441 ADC showed that the measured S/N ratio was over 15 dB worse than what was listed in the original manufacturer specifications. It was found that the additional noise came from the board analogue input front-end. This major drawback was overcome by developing an in-house front-end which bypassed the input amplifier and the low-pass filter. The trade-off was the need to add an external filter on the analogue signal path before its digitisation. In this way, the S/N ratio was improved by 13 dB on average. Based on this solution, the ADC board manufacturer later developed a "low-noise" version of the board analogue front-end, which is now commercially available.

3.6 Pentek 6510 digital receiver board

The Pentek 6510 digital receiver is a commercial off-the-shelf VME board [4,5]. It hosts 8 Harris HSP50016 Digital Down Converters (DDC) and one TI TMS320C40 Digital Signal Processor (DSP). This board is in charge of parallel data acquisition, independent digital down conversion and processing of up to 4 digitiser inputs. Figure 6 gives a schematic version of the board. The digitised inputs are pre-processed by the DDC chips, by digitally translating (*downmixing*) the input signal to DC, then zooming (*decimation*) on the frequency window of interest. Both the bandwidth and the centre f_{LO} of the frequency window are user-selectable. Each DDC is connected to a FIFO memory where data are stored. From the FIFOs

the data are then retrieved and processed by the DSP. The board is equipped with several memory banks, of which the Global Memory is visible from the VMEbus and is used to retrieve processed data.

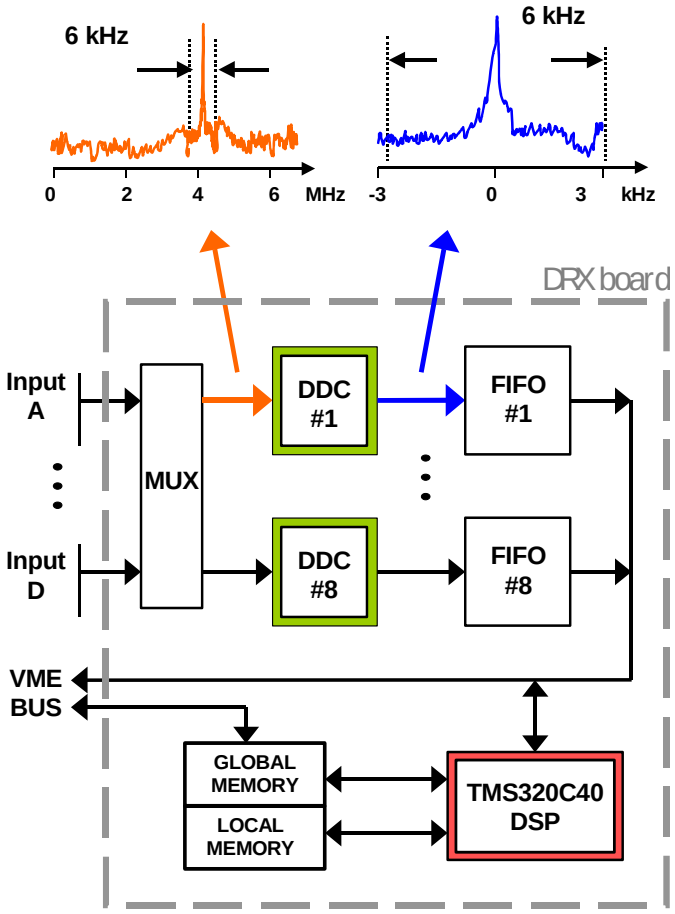

***Figure 6**: Schematics of Pentek's 6510 DRX board. Shown at the top is an example of digital zoom on the window of interest and DDC sample decimation.*

A DDC chip, also known as "digital receiver", is the evolution of the classical analogue superheterodyne receiver. Digital down-mixing, filtering and decimation have several advantages over the analogue implementation. First, aliased signals are strongly rejected, thanks to the accuracy of the sinusoidal waves generated by the local oscillator and by the mathematical precision of the mixer. Such rejection is a difficult task if performed by analogue electronics. Second, the DDC filters the input data and significantly cuts down the number of data samples, therefore making it possible to carry out a DSP real-time data processing. Third, the system flexibility is increased, thanks to the DSP and the DDC chips' re-programmability. As a consequence, implementing new functions only requires a software upgrade and no hardware changes. Finally, the characteristics of the components vary negligibly with temperature or component age. This guarantees a great level of stability and diminishes the need for re-calibrations.

4. SOFTWARE

Three separate codes have been implemented: the Low Level Code (LLC) [5] running on the DSP, the RTT and the Top Level software (TLS) running on the workstation. The LLC performs the core data acquisition and real-time processing, while the RTT sets-up the system hardware and drives the DRX board as an actual instrument. Finally, the TLS provides a plot of the data and functionalities such as the possibility to compare data sets taken during different AD cycles. These features are particularly useful during troubleshooting attempts, for example to determine whether and when beam losses have occurred.

Communication and data exchange between RTT and LLC are implemented in the DRX global memory, since it is the only on-board memory that can be accessed from the VMEbus. The LLC is only outlined here and a thorough description is given in [5].

Data exchange between RTT and TLS is implemented using properties of a dedicated Equipment Module (EM), which provides a structured data buffer in a shared memory segment of the PPC and data access methods from both sides.

4.1 Low Level Code

The LLC is the code running on the DSP. It executes the measurements from digitised pickup signals and manages the DRX board; it sets up the required DDCs after receiving a VME-bus interrupt (as fast as one every 20 ms); it acquires data from each DDC, processes them and makes results available to the RTT. The LLC also supplies the RTT with full diagnostic information and provides the DRX-to-RTT interface.

The LLC turns the DRX into a real instrument, completely driven via the interface and that can be used without any knowledge of its inner workings.

The LLC source is written in C and assembler; the executable is obtained by cross-compiling the source code on a PC under Code Composer as development environment. The output of the compilation is then uploaded to the UNIX environment and it is loaded into the DSP memory every time the DRX-hosting VME crate is powered up.

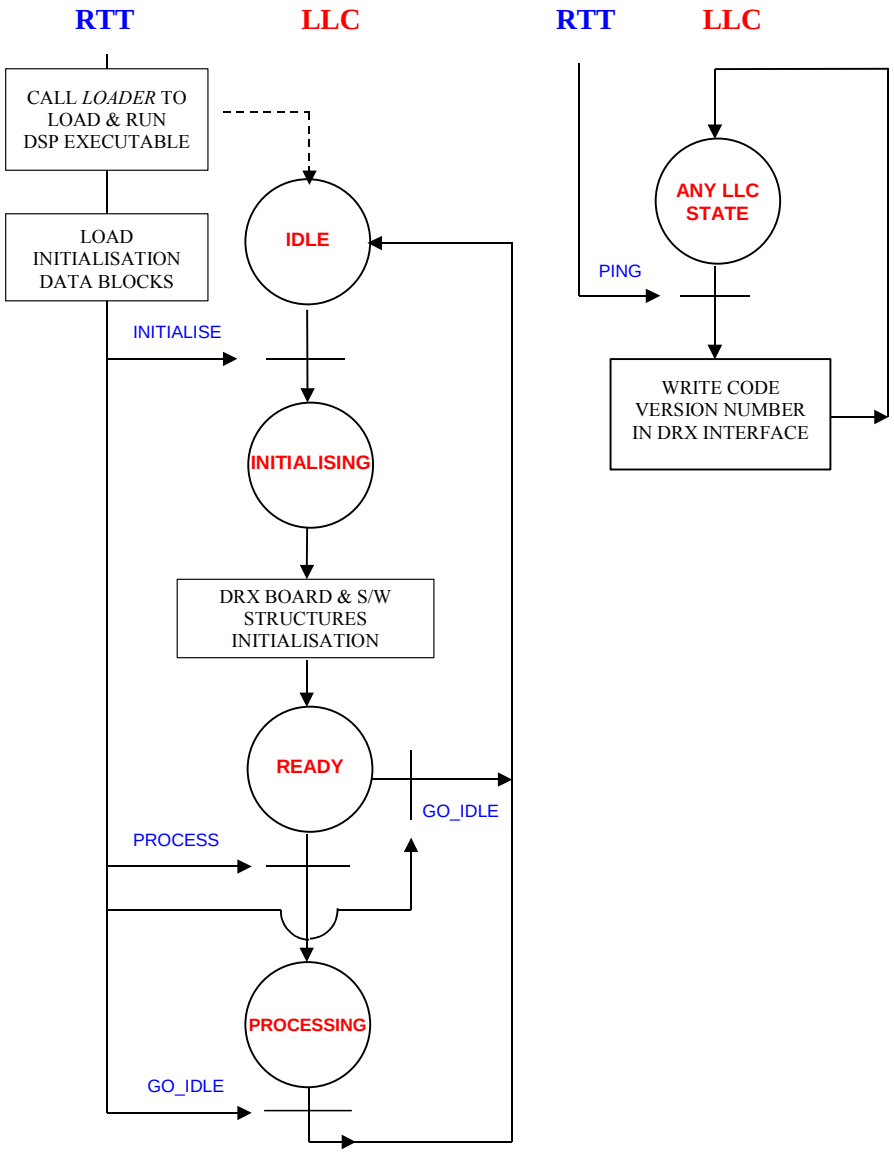

Fig. 7: *LLC state machine schematics following an RTT-issued command.*

The operation of the LLC is illustrated in Figure 7, which shows the LLC state machine and its interaction with the RTT. After loading the executable, a joint RTT-LLC initialisation and setup phase takes place. In this phase the LLC goes from *IDLE* to *PROCESSING* by passing through the *INITIALISING* and *READY* states. In addition, at any time the RTT can *PING* the LLC, which replies by writing its version number into a dedicated global memory location. Depending on the reply from the LLC, DRX status information can be gathered.

The *PROCESSING* phase is described in Figure 8, for one single measurement. In this phase, the RTT downloads a set of control parameters to the DRX global memory, thus specifying hardware and data processing set ups for every receiver used in the current measurement. Then the RTT sends a VMEbus-to-C40 interrupt to the LLC, thus requesting the LLC to start a measurement.

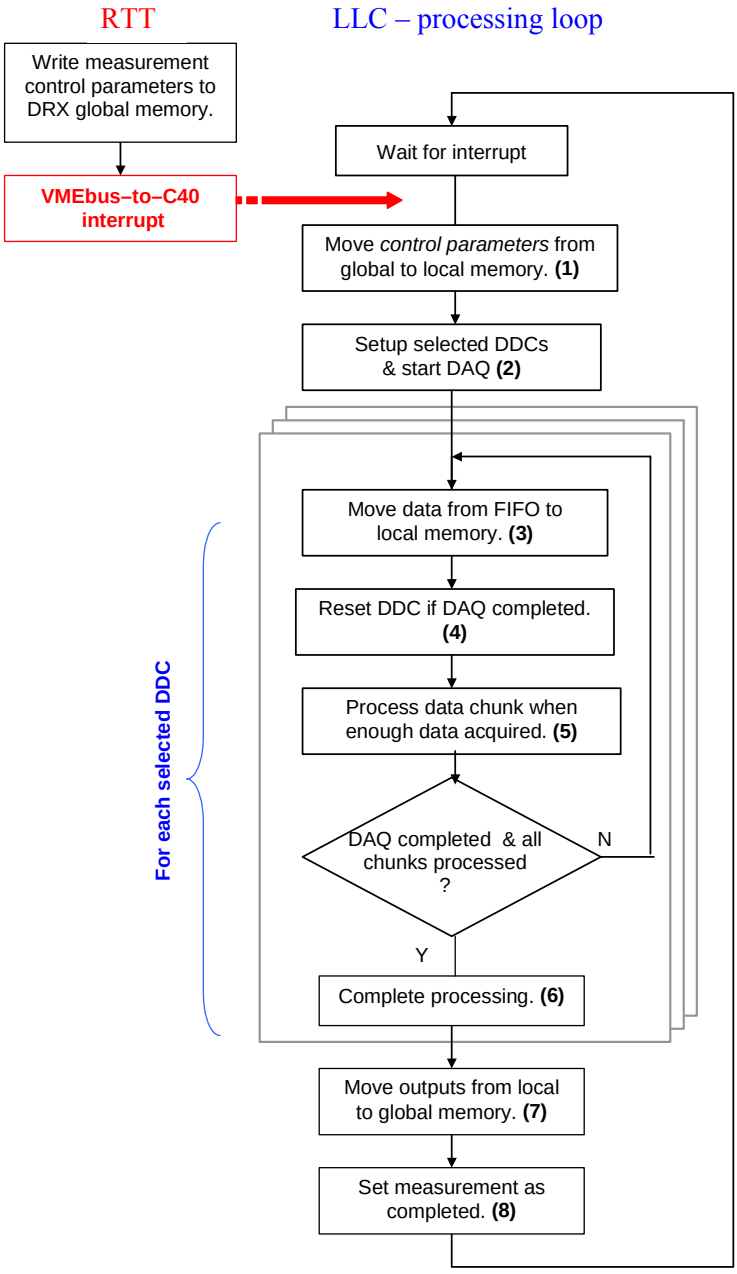

Fig. 8: *LLC actions following an RTT-issued VMEbus interrupt.*

The LLC minimises global bus use by moving all control parameters to local memory **(1)**. Then all requested DDCs are setup and released **(2)** and begin filling the corresponding FIFOs. When a FIFO is half full, the DSP is notified by an interrupt and is requested to empty the FIFO. The LLC then moves half the FIFO total storage capability to the local memory **(3)**. Each DDC is reset **(4)** when enough data have been acquired. A partial processing **(5)** is carried out as soon as enough data are stored in the local memory for one processing chunk, therefore speeding up the whole measurement and freeing local memory space. After all chunks have been processed, the LLC moves on to step **(6)** where the processed chunks are subjected to a final joint processing phase. With reference to the longitudinal de-bunched processing type, step **(5)** corresponds to the FFT calculation of a data chunk, while step **(6)** refers to the calculation of the cumulative spectral density and the beam parameter extraction.

In phase **(7)** all processed outputs from all DDCs are copied to the global memory, ready for retrieval by the RTT. Finally the measurement is marked as completed **(8)**.
The flow described in Figure 8 is actually more complicated than it appears, since while some actions occur in normal execution mode, most are totally interrupt-driven and executed by five different Interrupt Service Routines.

4.2 Real Time Task

The RTT runs on a PowerPC VMEbus board under LynxOS. It controls several hardware modules according to user requirements, to various constraints associated to the type of measurement carried out and to selected machine parameters. Some of these parameters are revolution frequency f_{REV} and the beam state (bunched vs. debunched), both acquired in real-time. The RTT also converts the DRX outputs to physics quantities by applying appropriate calibration factors. Finally, it stores a 3 minutes-wide sliding history window for beam intensity, momentum spread $\Delta p/p$ and f_{REV}, which is then made available to the TLS.

The RTT is synchronised to the AD machine via a constant-frequency clock which ticks every T_x = 20 ms and through two specific machine timings for start-of-cycle and beam injection. The RTT-to-machine interface is implemented with TG8 [6] and Digital I/O units [7] only, all of them being PS standard modules.

The RTT reads and interprets the slowly-varying configuration as well as user requests coming from the TLS. This input data may change at the fastest each 1200 ms. At each T_x the RTT acquires current machine status and beam conditions, controls the system set-up parameters and adjusts them as necessary. Depending on these conditions, the RTT decides which action to undertake, for example setting up the DRX for a new measurement, setting up the ADC clock or changing the second-stage amplifier gain.

The DRX is set up by writing a set of control parameters to the DRX global memory. This set of parameters defines processing and hardware setup for every used DDC. Some of these control parameters are taken directly from a set of user-selected process parameters (PPA), which was previously loaded as part of the configuration, depending on f_{REV} and beam state. These control parameters are process type, number of averages, FFT bins number, width of sliding–FFT overlap window, FFT region-of-interest (FFT ROI) and noise parameters used to determine the correction to be subtracted from the acquired data. Other control parameters, such as the DDC phase increment, indicated as *K factor*, the optimum observation harmonic and the decimation rate, depend on f_{REV} and must be determined in real-time within the current T_x. The calculation of these control parameters takes into account various constraints associated with the type of measurement carried out and uses appropriate look-up tables included in the configuration.

Table 4 lists the DRX control parameters and their dependencies for the longitudinal bunched (LB) and debunched (LD) cases: parameters in a row depend only on parameters present in higher rows. Since the RF system is unable to provide the RTT with a value of f_{REV} on the plateaus for a debunched beam, a lookup strategy is used to determine the nominal f_{REV} based on that actually measured by the DRX. In addition, when the beam is bunched the RTT must calculate the value of the harmonic clock number K_i. The second stage amplifier is also set up at run-time by means of a lookup table located in the configuration file, depending on the acquired value of f_{REV}.

Parameters	Depend on	Come from	Acquired	Calculated
Beam state (bunched/debunched)	Machine state	Digital I/O	Always	N.A.
f_{REV}, RF harmonic number h	Machine and beam states	Digital I/O	For bunched beams.	N.A.
Process type	f_{REV}, beam state	PPA	N.A.	Always
Number of averages	f_{REV}, beam state	PPA	N.A.	Always
FFT bins number	f_{REV}, beam state	PPA	N.A.	Always
Sliding-FFT overlap window	f_{REV}, beam state	PPA	N.A.	Always
FFT ROI	f_{REV}, beam state	PPA	N.A.	Always
Noise correction	f_{REV}, beam state	PPA	N.A.	Always
ADC K_i	f_{REV}, beam state	RT calculation	N.A.	For bunched beams.
K factor	Process type, h, ADC K_i	RT calculation	N.A.	For any DDC running LB measurements.
Beam observation harmonic n	LPU low-noise bandwidth, f_{REV}	RT calculation	N.A.	For any DDC running LB measurements.
Decimation rate	ADC K_i , f_{REV}	RT calculation	N.A.	For any DDC running LB / LD measurements.
f_{REV}	Machine and beam states	Last DRX-measured f_{REV}	N.A.	For debunched beams.
K factor	Process type, n, f_{REV}	RT calculation	N.A.	For any DDC running LD measurements.

***Table 4**: Process parameters needed to set up the DRX for LB and LD processing. Parameters in a row depend only on higher-rows parameters, for the corresponding beam state.*

The structured data buffer used for communication with the TLS provides time contingency, real-time de-coupling and history buffering. Time contingency is assured by time-stamping each data point, so that data with identical time-stamps describe the same physical beam.

Data are buffered prior to publishing them to the TLS. In fact, each of the eight receivers may produce a large amount of data within a short time, with a different rhythm and format with respect to any other receiver, and frequent "append" accesses to the data history are technically very inefficient. Any spectral-type data (256 or 512 values) is buffered separately in a PPC shared memory segment and can be retrieved individually using an asynchronous request-reply mechanism through a PS controls standard server program. The RTT reports some 70 different specific errors and warnings, some of which can occur as often as every $T_{x.}$

4.3 Top Level Software

An easy-to-use graphical user interface has been developed in Java language in order to give the user a fast access to the data. Equipment access is achieved using the standard ASC Java access libraries [8], a high level interface built on CDEV [9].

The TLS reads data from EMs every AD cycle and stores them; recent data are kept in memory while older-than-10-AD-cycles-data are stored in disk files. The user can select the data and the time of interest.

The TLS plots the selected data against time and groups them in AD cycle units, thus providing the user with a flexible data handling tool. The user may carry out the following actions: compare different cycles, zoom in a specific part to see more details, roll back in time to see previous cycles stored in memory, open archive files in order to compare the current situation to previous ones, select a specific data point and find the corresponding numerical values, examine longitudinal spectra at a given time and display several spectra in a 3D graph to follow the evolution of stochastic or electron cooling.

5. LONGITUDINAL SIGNALS PROCESSING

The processing of longitudinal signals is carried out at DRX level, first by the DDCs and then by the LLC. The output is then passed on to the RTT for post-processing and to derive the appropriate physical quantities. The actual processing depends on the beam state: in particular, Schottky signals [10] are processed only with a debunched beam, thus producing Power Spectral Density (*PSD)* plots. With a bunched beam, only the amplitudes at the fundamental (f_{RF}) and second RF Fourier components are considered. The various data processing stages are detailed in [5].

5.1 Debunched beam

The longitudinal PSD of a coasting beam composed of N particles, randomly distributed in azimuth along the ring circumference, is made of bands having width Δf, centred around the harmonics $n \cdot f_{REV}$ as can be seen in Figure 9. Here the *PSD* is expressed in A^2/Hz.

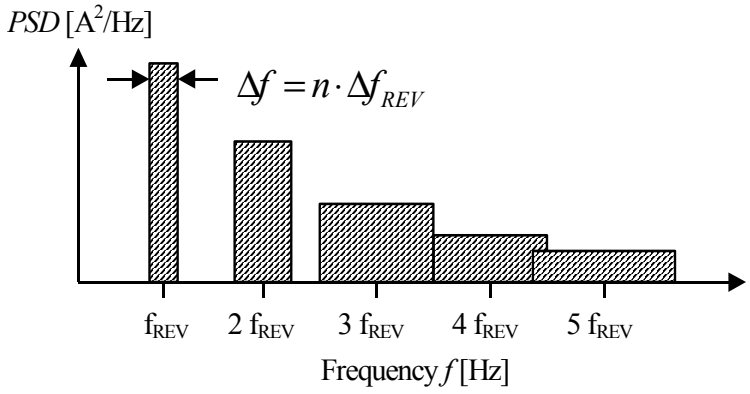

Figure 9*: PSD of a coasting beam as a function of the f_{REV} harmonic number n.*

The area $<I_n^2>$ of each band is constant and directly proportional to the number of particles N

$$<I_n^2>= 2 \cdot N \cdot e^2 \cdot f_{REV}^2 \qquad (1)$$

where e is the elementary charge. Defining $I_{n,rms} = \sqrt{<I_n^2>}$ it follows that the rms n-th current component $I_{n,rms}$ is proportional to $\sqrt{N}$. The width Δf of each band increases with the harmonic number n,

$$\Delta f = n \cdot \Delta f_{REV} = n \cdot f_{REV} \cdot \eta \cdot \frac{\Delta p}{p} \qquad (2)$$

where Δf_{REV} is the revolution frequency spread of N particles, $\Delta p/p$ is the momentum spread, $\eta = (\gamma_{TR}^2 - \gamma^2)/(\gamma_{TR}\,\gamma)^2$, $\gamma = E/E_0$, and $\gamma_{TR} = 4.75$.

The LLC sets up the DDC so that the frequency window to zoom onto is centred on the *n-th* harmonic of f_{REV}. Both the harmonic number n and the observation window bandwidth are user-selected. At high S/N ratios, such as at high momentum, signal processing is performed on high harmonics, thus speeding data acquisition; at low S/N ratios, low frequency harmonics must be used.

Figure 10 shows the *PSD* measured by the DRX, in arbitrary units, as a function of frequency f. Each *PSD* is the average of 60 complex FFTs, and is calculated every 1400 ms. The ADC f_S is fixed at 40 MHz and n equals 4. The peak centred on f_{REV} represents the n-th band and its area is proportional to the number of particles N. The beam cooling is evident from the progressive narrowing of this peak by going from the curve labelled PSD 1, taken before cooling, to the curve labelled PSD 4. Thus the beam progress can be followed by examining a similar sequence of spectra.

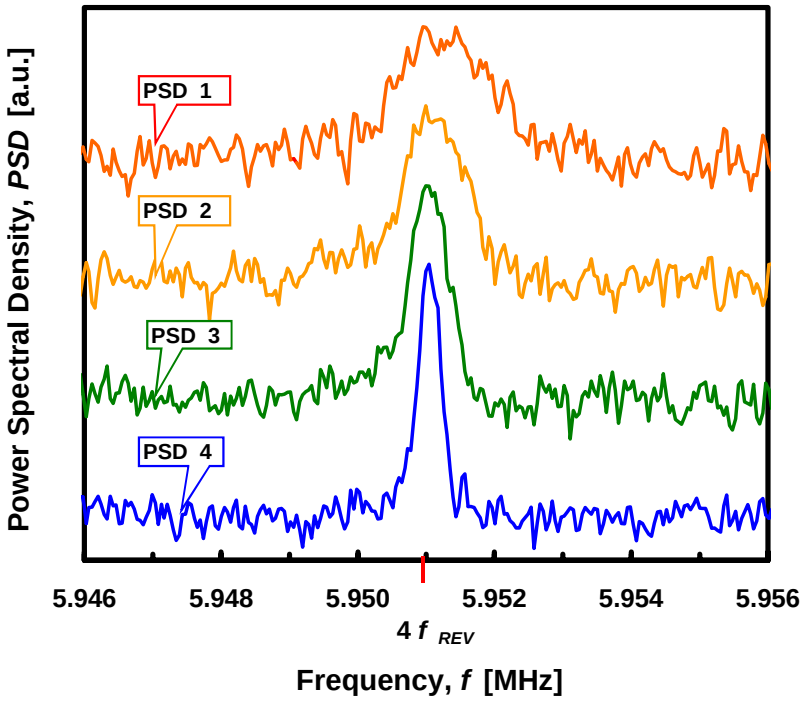

***Figure 10**: Effect of stochastic cooling on PSD, for a debunched beam, before (PSD 1) and after cooling (PSD 4).*

The DRX calculates the area A_{PSD} under the peak of the *PSD* vs. f curve. This value is then passed on to the RTT, where the number of coasting particles N is found from f_{REV} and A_{PSD}:

$$N = \frac{\alpha_U}{G_U^{\,2}} \cdot \frac{A_{PSD}}{f_{REV}^{\,2}} \tag{3}$$

where α_U is a calibration constant and G_U is the global system gain.

The DRX calculates the width Δf of the *PSD* curve at a 2σ height, and passes it on to the RTT, where $\Delta p/p$ is determined from (2) as:

$$\frac{\Delta p}{p} = \frac{1}{n \cdot f_{REV} \cdot \eta} \cdot \Delta f \tag{4}$$

Figure 11 shows the momentum spread measured by the system in case of a multibunch injection. Three bunches were injected into the AD at three different times. The cumulative effect of these bunches are shown as 3 peaks at approximately 0 s, 40 s and 70 s, respectively, on the first plateau. While the first peak is made up of just the first bunch, the second includes particles from the first two bunches, which have been debunched. The third peak on the first plateau includes particles from all three bunches, now all debunched. After each bunch is injected, the beam is cooled, hence the momentum-spread decreases. This is shown in Figure 11 by the three following smaller peaks in the three different plateaus.

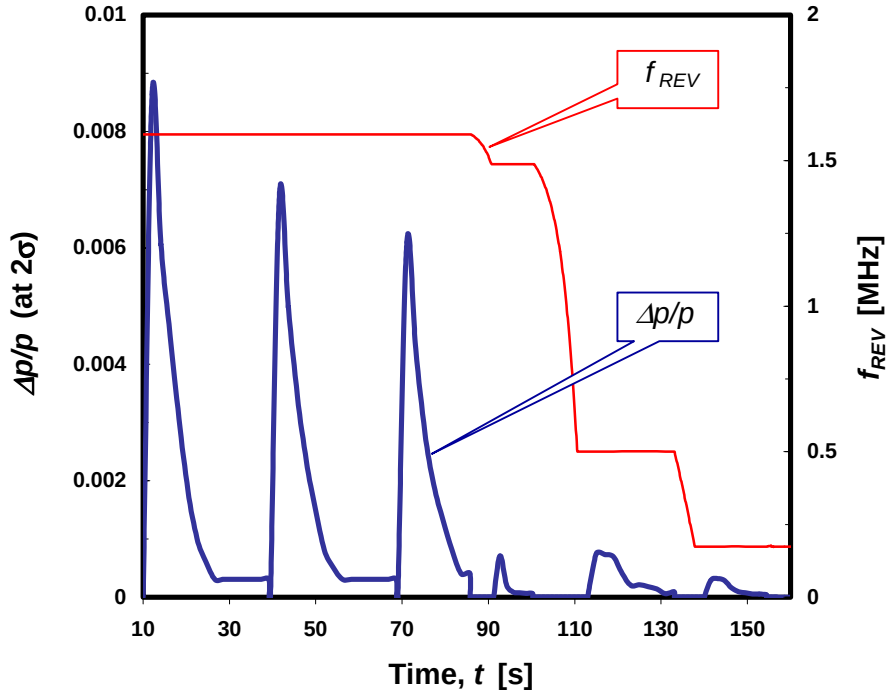

***Figure 11**: Momentum spread Δp/p measured by the system in a multibunch injection scenario. The revolution frequency is also shown.*

5.2 Bunched beam

For a bunched beam, the ADC sampling frequency f_S is proportional to f_{REV} via the clock harmonic number K_i, whose usage is illustrated in Figure 1. This allows tracking of the beam when its revolution frequency changes. In fact, the DDC setup parameter is $K = f_{LO}/f_S$, where f_{LO} is the local oscillator frequency [5], corresponding to the centre of the observation window. The K factor is constant if K_i remains constant. The measurements described here have been carried out using only the HF LPU.

At each turn m = 0,1,2 .. in the AD, ring the intensity time profile $I(t)$ of a single bunch is approximated, in the interval $[(m\text{-}½)/f_{REV}$; $(m\text{+}½)/f_{REV}]$, by a parabola:

$$I(t) = \frac{3}{4\sqrt{2}} \frac{I_0}{\tau \cdot f_{REV}} \cdot \left(1 - \frac{t^2}{2\tau^2}\right) \tag{5}$$

where I_0 is the DC current intensity per bunch and 2τ is the bunch FWHM.

In the AD Schottky system, two DDCs are used to measure the signal amplitude at the fundamental (f_{RF}) and second RF harmonic, respectively [5]. The experimental Fourier coefficients J_k (k=1, 2, ...) are calculated and then fitted with a truncated series of f/f_{RF}

$$J_k = I_0 \cdot h \cdot \left[2 - \Delta \cdot \left(f / f_{RF}\right)^2\right] \tag{6}$$

where $h = f_{RF}/f_{REV}$ is the RF harmonic number. Hence I_0 and Δ, and thus the bunch size τ, are obtained**:**

$$\tau = \frac{1}{f_{RF}} \cdot \sqrt{\frac{5\Delta}{4\pi}} \tag{7}$$

Integration of the beam profile over time gives the total number N of particles circulating in the machine:

$$N = \frac{h \cdot I_0}{e \cdot f_{REV}} \tag{8}$$

where e is the elementary charge. Hence the DC current intensity I_0 is directly proportional to N. Recalling that for the bunched beam case, according to equation (1), the rms n-th current component $I_{n,rms}$ is proportional to √N it can be seen that debunched beam measurements are more influenced by noise than bunched beam ones.

Figure 12 shows f_{REV} and the progress of the antiproton beam intensity in terms of N, for three AD cycles. It has to be noted that at the end of each ramp there is a drop in the measured number of particles. In the first ramp, the drop represents an actual particle loss, owing to the Common Mode Rejection of the RF voltage program not working properly. This problem was eliminated in July 2001. The other drops do not correspond to particle losses and are

generated by the low-frequency cut-off of the HF LPU. In fact, until the end of the 2001 operational period, both LPUs were installed but data were taken only from the HF LPU. This drawback has been overcome by means of the PU summing unit described in 3.2.

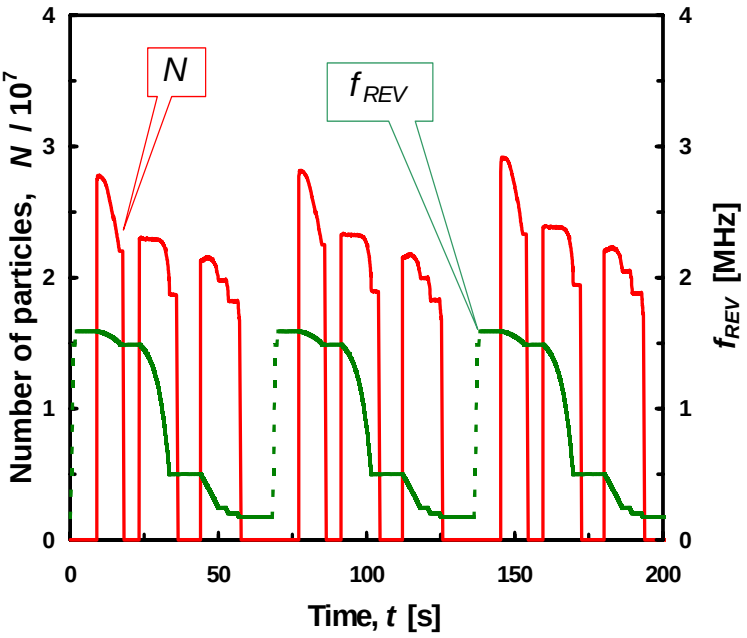

***Figure 12**: Number of particles N in the beam vs. time, computed from beam current amplitudes at f_{RF} and 2 f_{RF}. Bunched-beam data for 3 AD cycles.*

6. CONCLUSION AND FUTURE WORK

The system described has been reliably operating since May 2000. It was very useful during the various phases of the AD commissioning effort. The data produced by the system, and particularly the beam intensity, have become essential both for smooth AD operation and for the users. An upgrade to the system is under way, to measure tunes from transverse signals using the Beam Transfer Function (BTF). In addition, PU-to-amplifier cables will be replaced with EMC shielded cables for the 2002 running period, to reduce environment noise pick-up.

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