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**Digital Signal Processing:  
State-of-the-Art at CERN and Recommendations**

**Final report of the  
PS Division DSP Working Group**

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**Abstract**

Dramatic hardware performance improvements over the last decades have paved the way to the ascent of digital techniques for processing signals, with a concurrent and parallel interest in Digital Signal Processing (DSPing) and in the use of Digital Signal Processors (DSPs). Recent discussions within PS showed that there are needs for DSP-qualified manpower in new projects that cannot be fully satisfied internally. In order to determine how PS can best profit from the growing importance and efficiency of DSP technologies, with an effort compatible with the available divisional resources, a DSP working group was created. Its mandate is to advise PS management on the best way to proceed in the DSPs and DSPing domains. In particular, the issues targeted are wide-ranging, from evaluating the state-of-the-art at CERN to hardware standardisation and required training. This report gives the findings of the working group and presents its closing recommendations.

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## **1. Introduction**

The dramatic hardware performance improvement of the last decade has made it possible for functions once exclusively accomplished by analogue methods, to be improved by the application of an alternative digital approach. This is true to a point that the conversion to digital processing has become inevitable. Some factors to consider when deciding whether to cross the border towards digital implementations are speed as well as precision, signal-to-noise ratio and dynamic range. In addition, aspects that favour the digital approach are the possibility of implementing more sophisticated processing algorithms together with re-configuration flexibility, better control of accuracy requirements, components stability and often a lower cost.

The meaning of the acronym “DSP” has become so broad now that it includes both Digital Signal Processors (DSPs), i.e. the actual hardware, and Digital Signal Processing, DSPing in short. The latter deals with the theory and practice of processing all digital signals, hence including for example signal sampling, digital filtering, FFTs and wavelets, to name just a few aspects. This dichotomy i.e. DSPs vs. DSPing is used throughout this report. It is apparent that DSPing is a rather broad discipline, covering a widespread area, and that it generates a lot of interest. In fact DSPing may be applied even to non-DSP-based applications, such as those using Programmable Logic Devices (PLDs); in particular, to applications using High Capacity PLDs (HCPLDs) which are the most performant devices. The HCPLD class is composed of Complex PLDs (CPLDs) and Field Programmable Gate Arrays (FPGAs).

The DSP Working Group was created in October 2001, following discussions within the PS Division revealing the need for DSP-trained staff in view of possible DSP-based upcoming projects.

## **2. Mandate of the DSP working group**

The mandate of the DSP Working Group (WG) [1] is to advise the PS Division management on how to best proceed in the domain of DSP technology and digital processing of signals.

In particular, the following issues have to be addressed by the DSP WG:

1. what is happening elsewhere in CERN,
2. the interest and practicability of standardisation,
3. the need for and suggestions on training,
4. general recommendations to the Division that might help improve the Division’s efficiency on working methods in this domain.

It has to be mentioned that in this context, standardisation is meant as the choice of a common and “standard” DSP/PLD platform (consisting of hardware and software) throughout the whole PS Division. Here the emphasis is on the enforcement of a “normal” or default type of DSP/PLD with its associated software development tools.

### **3. DSP and PLD basics**

DSPs and PLDs are the main ingredients of modern digital processing projects. This paragraph details the basic characteristics of DSPs and PLDs and ends with a functional comparison of DSPs to FPGAs, the latter being one of the most performant device subclasses in the PLDs category.

#### **3.1 PLDs**

A PLD chip is an integrated circuit composed of an array of logic cells that can be interconnected by programming to achieve different designs. Programming actually needs two steps: a design entry and a design implementation.

Design entry can be carried out by means of a schematic entry package, provided by the chip manufacturer, or a high-level hardware description language. There are two such languages, namely VHDL and Verilog, the former being the supported choice at CERN and generally in Europe.

Design implementation on the chip uses the tools provided by the manufacturer. Therefore, the design is converted to the format supported by such tools. Then the logic is partitioned into logic blocks that are optimally placed in a map of the chip. Finally, the software creates the binary programming file used to configure the device.

The internal architecture of PLDs varies from one manufacturer to another, as well as among different families, but a common point is the presence of matrices of logic blocks and internal routing resources that allow the designer to implement blocks of combinational and sequential logic, in one single chip. Of particular interest are FPGAs, characterized by very high capacity (currently in the  $10^6$  gate range) and flexibility. They are leading the way to the system-on-a-programmable-chip (SOPC) technology, which combines in a chip a large quantity of programmable logic with memory, a processing engine and possibly additional Intellectual Property (IP) core.

The main PLD producers are Xilinx, Altera and Lattice. They also provide the tools to optimise the function allocation in the PLD chip.

#### **3.2 DSPs**

DSPs are microprocessors particularly tailored to fast processing of huge amounts of data and to math-intensive tasks. DSPs became commercially available in the early eighties and the first was the Texas Instruments TMS320C10.

Their whole architecture is shaped by digital signal processing algorithms. Most of these algorithms can be easily implemented using a special DSP that has that special feature.

The main characteristics of a typical DSP are:

- a) Dedicated hardware to perform multiply-accumulate functions, which are among the most often required operations in DSPing algorithms.
- b) Separate data and address buses for data and instructions (a modified version of the Harvard architecture) to maximise memory access efficiency.
- c) Instruction sets tailored for

- 1] increased efficiency through maximised hardware use and
  - 2] minimised amount of memory space for DSP programs storage.
- d) Specialised hardware to maintain numeric fidelity, such as extended-precision registers that are wider than other registers.

The DSP software development phase is carried out on a different platform, typically a PC or a workstation, connected to the DSP via a special interface. The resulting executable code is downloaded to the DSP, again through the same interface. Modern development environments provide several debugging utilities and allow real-time code debugging.

The DSP market is currently dominated by three brands, namely Texas Instruments (TI), Analog Devices (AD) and Motorola. The most performant DSPs are produced by TI and AD and are based on two different architectures: Very Long Instruction Word (VLIW) by TI and Single Input Multiple Data (SIMD) by AD. In fact, DSPs themselves are now moving away from their original internal architecture homogeneity to accommodate new application needs and improved performance.

### **3.3 Functional comparison of DSPs and FPGAs**

The most important factors to consider during a system development phase in order to choose between DSPs and FPGAs are:

- a) System input data rate.
- b) Number of channels to be acquired and processed.
- c) Type of tasks to be carried out.
- d) Required flexibility.

The main difference between the way DSPs and FPGAs carry out the signal processing is that DSPs treat input data serially, while FPGAs use a parallel approach. This allows FPGAs to be much faster when performing tasks such as digital filtering or FFTs. A problem with this parallel approach is the case of a large number of inputs, since each input must be provided with its own dedicated hardware processing chain, possibly resulting in a very large or expensive chip. On the other hand, DSPs themselves may suffer from inadequacy difficulties, particularly with very large system input data rates.

Control tasks requiring action-branching according to some events can be easily implemented in a DSP, but not always with FPGAs. In fact, an FPGA needs to build dedicated resources for each configuration; therefore several very large configurations may not fit in the FPGA at the same time. In addition, very complex mathematical algorithms can be implemented, changed and updated more easily in software (as for DSPs) than in hardware (as for FPGAs).

It is also possible to mix the advantages of both DSPs and FPGAs, using for instance the FPGAs as DSP front-ends or buffers. Alternatively, hybrid chips combining a dedicated processor core with an area of programmable logic are already commercially available. Finally, several processor cores can be found, ready to be embedded within an FPGA.

The market trend is to produce FPGAs with an ever-increasing number of gates. This allows to implement many more functions and capabilities. In addition, libraries of ready-to-use IP cores are becoming increasingly available, easing and speeding up function implementation. Finally, Altera has very recently launched a new device family, called Stratix, which includes DSPing-dedicated blocks.

On the other hand, DSPs are getting faster and faster, hence they may become a valid alternative to FPGAs for some particular applications. The consequence of this simultaneous software and hardware evolution is that DSP and FPGA typical applications will increasingly overlap.

## **4. Current situation at CERN**

Both DSPs and PLDs are used at CERN, although in different quantities. PLDs are widely used since they can find application in tasks ranging from simple to very complex. On the contrary, DSPs are mostly used within complex applications, hence their smaller number. This also causes a difference in the way development is carried out. While for PLDs there is a CERN-wide central support, although mostly for development tools, the DSP developer is basically left on his own.

### **4.1 PLDs**

Mainly three divisions at CERN use PLDs, namely PS, SL and EP. While PLD design is a marginal activity in PS and SL, it is the core competence of some groups in the EP Division. In addition, there is a quite large degree of expertise in Experiments but wholly belonging to external bodies such as universities and research institutes.

At the PS Division, in the diagnostics group for example, PLDs have been extensively used for quite a long time: in simple designs, with Programmable Array Logic (PAL), or complex designs, with HCPLDs. Recent developments of general purpose piggyback boards, based on Altera PLDs, allow the designer to implement completely different functions using the same hardware [2,3].

The vast majority of designers at CERN use Xilinx and Altera. Some of them have installed a local copy of the design and implementation software in their computers to avoid depending on IT's Sun station cluster, but the design flows are the same. The trend is to use VHDL Hardware Description Languages for complicated designs. These allow a text-based approach to hardware design and therefore profit from all the developments the software world has introduced to deal with complexity. For schematics-based design, Maxplus is the tool of choice at CERN and therefore Altera chips are used most of the time. In general, easy designs are mostly done with Altera, while complicated designs are done either with Altera or Xilinx. The number of designers using Lattice is very small.

### **4.2 DSPs**

Similarly to the situation with PLDs, there are mainly three divisions at CERN that make use of DSPs, namely PS, SL and EP. Within the EP Division, the expertise is located mostly in the Experiments, hence wholly belonging to external institutions.

DSP software development tool are usually bought on a per-project basis, i.e. no CERN-wide supply policy is implemented. As a result there is no central-support for tools and the few DSP developers have to work pretty much on their own.

All three major DSP brands are present at CERN, although Motorola is not on a par with the other two, as far as new developments are concerned. Hence this leaves, de-facto, only TI and AD. There are different reasons why a given manufacturer is chosen for a particular project.

Some are due to cost and resource-saving aspects, in the sense that the same DSP make had already been used for similar developments. Hence the expertise and/or the software (or part of it) or the development environment may be re-utilised. In other cases, the DSP is acquired in a package with a chosen Commercial-Off-The-Shelf (COTS) board. Finally, other DSPs are chosen because of specific characteristics and are mounted on in-house designed and built custom boards.

There are two main categories of typical DSP uses at CERN:

1. Custom DSP boards, developed in-house. This allows cost cutting when a large number of identical modules have to be produced. In addition, specific needs such as a particular type of interface can be more easily accommodated. Typical examples of groups falling within this category are Power Supplies (PS [4] and LHC [5]) and Experiments. For the latter, another factor resides in the possibility of foreseeing DSP's evolution trends over time, a fact that seems very difficult for COTS boards.
2. COTS boards. One obvious advantage is that less time has to pass between purchasing and actually installing the board in the system. The higher hardware cost associated with COTS boards is easily compensated by lower board design and assembly costs. Furthermore, this category implies the need for a much smaller number of modules, thus offsetting the possible savings associated with large numbers. Typical examples of applications falling within this category are control, feedback and diagnostics [6] systems.

The following pages contain a list of applications that make use of DSPs at CERN, grouped by division. The list is probably not exhaustive, owing to the difficulty in gathering information on the subject about DSP uses in Experiments. This list may be useful to give a flavour of the type of DSP expertise available at CERN, as well as to pinpoint the divisions where a given expertise may be found.

The work required to assemble these tables permitted us to gather useful ideas and to identify at least two development systems, currently operational. These are:

1. *D.Modules*, developed and manufactured by the German company D.SignT ([www.dsignt.de](http://www.dsignt.de)). These modules are DSP-based processing modules, to be used as a stand-alone platform or as part of an embedded DSP application. Each module includes a DSP chip, a fast memory data block, serial and parallel interfaces, a BIOS and a user-configurable I/O based on a CPLD. Several DSP types and brands are available, as well as peripheral daughter modules that can be mounted on top of the DSP modules. The *D.Modules* have been used for LEP in the past [7] and are currently operational in still undocumented SL Division applications. They provide a very flexible and "LEGO"-like development.
2. *VC Series cameras*, manufactured by Vision Components ([www.vision-components.de](http://www.vision-components.de)). They are image processing systems that integrate a high-resolution CCD camera with a DSP. A system based on these products is the "LHC Mole dipoles testing", used in LHC-MTA for magnet testing [8].

## PS Division

Group	Application	DSP type	Board	Notes
<b>BD</b>	AD beam parameters measurement [9].	TI TMS320C40	COTS (Pentek Digital Receiver 6510 model).	System in use – upgrade under way to measure tunes with BTF method.
	PSB tune measurements [10, 11].	Motorola 96002	COTS DataBeta DBV96	System in use. Board out of production. We use 1 board for operation and we have 7 spares.
	PS tune measurements [12].	TI TMS320C25 + 4xZoran ZR34161 vector processors.	COTS VASP-16	System in use. Board out of production. We use 1 board for operation and we have 1 spare.
<b>RF</b>	CLIC active alignment system for CTF2 [13, 14, 15].	TI TMS320C31	In-house built.	Prototype built. System not currently in use.
<b>PO</b>	Digital Regulation for Thyristor-based power supplies.	Motorola 56001	In-house built.	70 units. DSP out of production.
	Digital Regulation for Tekelec power supplies: 12 phases Thyristor bridge with Transistor Bank Active filter [4].	Motorola 56001	In-house built.	50 units. DSP out of production.
	Power supplies digital regulation for Septum Magnets (SMH 57, 61).	Motorola 56302	In-house built.	20 units. DSP out of production.
	a) Thyristor Gate control for Main power supply of PS complex. b) Power supplies digital regulation for Pole Face Windings (PFW).	Motorola 56303	In-house built.	Prototype.
	Prototype	TI TMS320C542		Abandoned.
	Prototype	TI TMS320C32		Abandoned.

## SL Division

Group	Application	DSP type	Board	Notes
<b>BI</b>	SPS Large oscillation interlock.	TI TMS320C6701	COTS (Transtech DM11)	Already tested, will become operational in 2002.
<b>HRF</b>	SPS RF frequency program to generate the RF frequency settings during ramps.	AD ADSP21065L	COTS (D.SignT 21065L) on in-house made board.	
	Tuning of LHC 400 MHz cavities.	AD ADSP21065L	COTS (D.SignT 21065L) on in-house made board.	One card for each cavity. Currently 4 cards in place, up to 60 foreseen.
	Helium level measurements of 400 MHz cavities.	AD ADSP21065L	COTS (D.SignT 21065L) on in-house made board.	
<b>PO</b>	LHC Power Converter Function Generator and Controller [16, 17].	TI TMS320C32	Custom made board.	About 2000 boards are needed. Each board includes one Motorola MC68HC16Z1 CPU as main processor and one TI DSP as coprocessor.

## LHC Division

Group	Application	DSP type	Board	Notes
<b>MTA</b>	Mole-based system for warm magnetic and optical LHC dipoles testing [8].	AD ADSP2181	Commercial system {CCD camera + DSP + memory + PC interface} from Vision Components GmbH, Germany. Image-processing algorithms developed by Fraunhofer Institut, Germany.	The system is operational and will be extensively used during the next 4 years for testing purposes. No software upgrade is foreseen, but calibration tables will have to be periodically re-loaded via a serial link.



## Experiments

Experiment	Application	DSP type	Board	Notes
<b>LHCb</b>	Vertex Off detector electronics: DAQ interface	TI TMS320C6211 or TI TMS320C6202	In-house built, 100 units, 16 DSP each.	Prototyping in progress.
	Vertex Off detector electronics: inner tracker	TI TMS320C6211 or TI TMS320C6202	In-house built, 100 units, 16 DSP each.	Prototyping in progress.
<b>ATLAS</b>	Liquid argon calorimeter Read Out Driver	Under evaluation both AD ADSP21160 and TI TMS320C6202	In-house built, 200 units, each carrying 8 DSPs.	The final prototype should be ready by end 2002.
	Muon precision chamber Read Out Driver.	AD ADSP21160	In-house built. About 200 units, each carrying 5 DSPs.	The final prototype should be ready by end 2002.
	Muon Cathode strip chambers (CSC) Read Out Driver	TI TMS320C6202 or TI TMS320C6203.	In-house built. Each board carries 13 DSP chips. There are 16 boards so far foreseen.	

## **5. Standardisation: interest and practicability**

The main topic here is DSP standardisation as explained in section 2 above. In fact, it turns out that for PLDs, a de-facto standardisation is already in place, although in a rather loose fashion. As for DSPs, there is no standardisation in place at the moment. The WG feels a standardisation would not be efficient because the drawbacks would far exceed the benefits.

### **5.1 PLDs**

Standardisation has already been effectively enforced at CERN by the support group in the IT Division. This group chose to install and support software from three manufacturers: Altera, Xilinx and Lattice. Support for Altera is provided through the Maxplus and Quartus software packages, both very easy to use. Xilinx design is supported by the Alliance series, which is a little harder to work with. Further restriction to only one manufacturer is impractical and should be avoided.

### **5.2 DSPs**

As mentioned in § 4.2, for most new projects, DSPs from only two manufacturers, namely TI and AD, are present at CERN. The WG feels that there should be no further restriction to one manufacturer or one family. There are several reasons for this suggestion.

First, the choice of a particular DSP, hence of a brand, is application-driven. Since in some cases different DSPs (brands) do not cover the same application, there is no competition among the three brands; one is compelled to choose one brand, for a given application. In other words, in some cases, different DSPs are suited to different applications and there is no overlapping.

Second, DSP software is increasingly moving away from assembler towards high-level languages. Hence, development and support is bound to become easier and more easily portable to other platforms in the future.

Third, for several applications, one may be satisfied with buying a COTS board rather than a DSP, with significant savings on the cost associated with the development of a customised board. So, to keep some degree of flexibility, one should avoid standardisation.

It cannot be denied that, in a few cases, standardisation would entail some degree of saving and, perhaps, of improved efficiency. However, the WG feels that the savings would be minor if compared to the associated drawbacks, such as loss of flexibility, or being obliged to resort to in-house customised boards, or even to be constrained to non-optimal design owing to lack of suitable components in the “standard” brand.

As far as estimating the cost-savings associated with standardisation, it has to be stated that it is very difficult to make meaningful predictions on cost related to projects that either do not exist yet, or are preliminary. Hence the WG feels that this issue, which was not strictly speaking in the mandate, cannot be dealt with satisfactorily at this time.

However, standardisation could be worthwhile for mass production. This is difficult in the PS Division where, except in the Power Supply Group, there are different small projects with different needs.

After long and thorough discussion within the WG as well as with DSP developers from several CERN divisions, the WG feels that standardisation would not be the most efficient choice. Instead, the WG feels that a more efficient solution would be to identify a number of “DSP advisors”, i.e. experts working on DSPs in various PS groups, who would be consulted by a Project Leader on a need-only basis to get help on the selection of the best DSP or COTS board for a given project. The Project Leader should point out specifications, available budget and “constraints” and then rely on the experts. The advisors would have to remain up to date on all DSPs topics, from market evolution to digital signal processing algorithms, down to software availability, applicability and portability.

## **6. Training needs and suggestions**

### **6.1 PLDs**

Several PLD-related training courses are already available at CERN, such as ‘VHDL for synthesis’ or ‘Tool usage’. The ELEC-2002 refresher course devoted one whole lecture to PLD basics, development tools and support. The other skills necessary for PLD design are mostly related to general digital design, a topic already covered in all electronics engineering university courses. The ELEC-2002 lectures are a good example of some of the topics/skills that would be used in PLD design, although no theoretical course can replace actual practice in a real world environment. Hence, one could think of a hands-on practical training course whereby a very limited number of participating technicians would spend a finite time in an already established CERN PLD laboratory, working under strict supervision to design and develop the necessary hardware required for the tasks/projects of that laboratory. The same type of hands-on training could be devised for hardware and software design engineers.

### **6.2 DSPs**

In the case of DSPs, the situation is different in that there is no established CERN-wide course on DSP basics. Even the ELEC-2002 did not cover any DSP-related aspects. Outside the PS Division, a few training actions have been organised in the past by the SL Division, on an almost personal basis and by particularly interested groups. This happened to respond to a particular need, i.e. in order to bring their own staff up to speed in view of an imminent project requiring DSP-related work. For example, the SL Division organised a four-day DSP/DSPing course in 1995, and a three-day training on AD’s SHARC family in 1999.

To these occasional training actions, one should add the obvious CERN-wide periodic presentations by most DSP manufacturers, which are to be classified as “information dissemination” for marketing purposes rather than as part of a proper training action. Similar presentations are useful and should be maintained. They are, however, obviously product-driven and therefore not tailored to particular CERN needs. As well as providing a little general information, these seminars are definitely of advanced level and assume previous knowledge or experience of DSPs.

DSP experts will have to keep abreast by attending manufacturer seminars/exhibits. On the other hand, a general training for experts is difficult to organise. These people rather need more specialised courses, possibly including a relevant part with hands-on sessions on custom board hardware design and/or on software/development tools. Such training could be provided by manufacturers, obviously on a family of their own products.

It is very important to keep PS staff correctly informed on DSP platform capabilities and recent development improvements. This is to avoid prejudice leading to automatic rejection of DSPs in the project-definition phase. This need could be satisfied by short seminars on given aspects of the DSP field. There could be, for example, an initial seminar covering the basics, followed by other lectures focused on recent improvements, as they happen. An additional action could be the creation of an introductory-level CERN-wide DSP website, covering the basics of DSPs and digital signal processing, as well as giving information on hardware and manufacturers. A further action would be the creation of a CERN-wide, open-to-all-levels DSP mailing list, provided with detailed topics.

### **6.3 DSPing**

DSPing is a topic which generates a lot of interest mainly because of its applicability also to digital systems based on hardware other than DSPs. Hence the strong need for training to remain abreast and to profit from progress in this field. Furthermore, the need for a more detailed training is apparent, because often the DSPing developer has to find his own way due to inaccurate or blurred specifications for his project. Technicians and/or technical engineers needing to work on DSPing, who have not received formal training on this topic, would benefit from such courses.

Concerning DSPing training, as for DSPs, there has been no CERN-wide activity. Only a few sporadic courses have taken place, on a group basis. Examples are the one organised by SL in 1999 for their technical staff and the previously-mentioned 1995 course on DSP/DSPing. Consequently, this is an untouched area, which seems ready for and suited to a series of training actions, possibly as a combination of formal courses and hands-on sessions. A caveat exists when considering external courses, since they will hardly be tailored to CERN-relevant needs. Rather, they tend to include industry hot-topics, such as GSM, audio and video DSPing applications. Hence the need for a carefully tailored, in-house course, perhaps with the help of external lecturers.

Finally, most of the training needs mentioned in this paragraph exist on a CERN-wide basis, therefore some degree of saving could be obtained by extending all training actions to the whole of CERN, thus sharing the associated costs with other divisions. The CERN Training Service is currently evaluating possible DSP training courses.

## **7. General recommendations to improve efficiency**

The DSP WG feels that creating and maintaining a “PS DSP experts group” would only be justified in case of a large number of DSP-based projects within the Division. In that case, it could be cost-effective. Nevertheless, given the current lack of DSP-based projects within PS, it is not practicable for now. It should be considered, however, as a CERN-wide effort, but only after the proper actions have been undertaken within PS.

The WG feels that the creation of a DSP user-support-only Divisional group is also to be avoided as inefficient, impractical, due to the current lack of DSP projects, and conducive to reduced productivity.

The DSP WG therefore puts forward the following recommendations for application within the PS Division:

- a) To keep experts in different groups, and consult them when the need arises.
- b) To keep these experts knowledgeable by means of regular and appropriate training (specialised seminars, hands-on sessions etc)
- c) To build temporary inter-group teams including, but not limited to, DSPs/DSPing experts, on a project basis, as the need arises. This structure may turn out to be more difficult to manage, but it should be effective.

## **8. Closing recommendations**

This report has covered many topics, gathered a large amount of information and provided several suggestions and recommendations on the aspects of the mandate.

To make the DSP WG recommendations appear more clearly to the reader, they are broken down according to the mandate items and concisely summarised as follows.

### 1. Standardisation (see § 5):

The WG feels a standardisation (already partially enforced for PLD) would not be efficient because the drawbacks would far exceed the benefits. As an alternative, the WG feels the Division should identify a number of “DSP Advisors” within PS, to be consulted, on a need-only basis, by Project Leaders seeking help on selecting DSP/COTS boards for a given project. The “DSP Advisors” would have to remain up to date on all DSPs topics through appropriate training. This alternative would fit well with recommendations on efficiency further down in this paragraph.

### 2. Training on DSPs (see § 6.2):

The WG feels the PS Division should

- a. Maintain presentations by manufacturers.
- b. Allow DSP experts to attend manufacturer seminars/exhibits and receive hands-on, specialised training.
- c. Run short general/introductory seminars, on a regular basis, to keep PS staff correctly informed on DSP and DSPing platform capabilities. Follow-up on them by means of “update modules”, either in the form of internal seminars or lectures by external experts, to keep up with progress in the field.
- d. Set up and maintain an introductory level DSP website as an information vehicle.
- e. Activate and maintain a CERN-wide, open-to-all-levels DSP and DSPing mailing list.

3. Training on DSPing: (see § 6.3):

The WG feels the PS Division should

- a. Organise an internal, open-to-all, carefully tailored training, as a combination of formal courses and hands-on sessions.
- b. Extend training actions to the whole of CERN for cost cutting.

4. Efficiency: (see § 7):

The WG feels the PS Division should

- a. Keep experts in different groups, and consult them as needs arise.
- b. Allow these experts to remain knowledgeable by means of regular and appropriate training (specialised seminars, hands-on sessions etc).
- c. Build temporary inter-group teams including, but not limited to, DSPs/DSPing experts, on a project basis, as the need arises. This structure may turn out to be more difficult to manage, but it should be effective.
- d. Actively support CERN-wide training actions, currently under consideration by the Training Service, and take an active participation in them. This would be with the aim of steering the preparation and organisation of the training effort.

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