
CMS Conference Report

7 March 2001

Recent Results for the CMS Tracker Silicon Detectors

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Abstract

The paper reports on a detailed study of the radiation resistance of p^+ on n silicon microstrip detectors for the CMS tracking system.

From this study it is seen that the use of low resistivity substrates with $\langle 100 \rangle$ crystal lattice orientation promises excellent performance of the Inner Tracker after heavy irradiation in the LHC environment. Furthermore, the advantage of using detectors thicker than $300 \mu\text{m}$ in the Outer Tracker is discussed together with experimental measurements on prototypes.

Presented at *IEEE Nuclear Science Symposium and Medical Imaging Conference*,
Lyon, France, 15-20 October 2000

Submitted to *IEEE Trans. on Nucl. Sci.*

1 Introduction

At full LHC luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$, the CMS Tracker [1] will be subjected to unprecedented levels of irradiation. The highest dose will be accumulated by the innermost layers of the system, that must survive fluences up to $1.6 \times 10^{14} \text{ 1 MeV-equivalent neutrons cm}^{-2}$ [2]. For this reason, over the last few years, considerable effort has been concentrated on better understanding the operation of silicon microstrip detectors after heavy irradiation. The most recent results concern the use of relatively low resistivity substrates and the use of crystals with a $\langle 100 \rangle$ lattice orientation.

In december 1999 the CMS collaboration decided to replace the gaseous detectors of the Outer Tracker with silicon sensors [3]. In order to maintain the same number of readout channels it is planned to use large detector modules based on sensors manufactured in 6" industrial production lines. The possibility of using 400 and 500 μm thick detectors in this context has been investigated.

2 Low resistivity

To study the effect of substrate resistivity, several sets of prototypes have been produced by different manufacturers (CSEM, Hamamatsu, Micron). The depletion voltage before and after irradiation has been measured using the standard C-V characterization of small diodes and full size devices.

The depletion voltage V_{dep} of a $p^+ - n$ junction silicon device depends strictly on the effective doping concentration N_{eff} of the n -type substrate. For a simple diode it is given by

$$V_{dep} = \frac{ed^2}{2\epsilon_0\epsilon_{Si}} N_{eff} \quad (1)$$

where d is the thickness of the substrate, e the electron charge, ϵ_0 the free space permittivity and ϵ_{Si} the dielectric constant of silicon. On the other hand N_{eff} is inversely proportional to the substrate resistivity.

As a consequence of radiation damage N_{eff} changes with fluence and, after an initial decrease until type inversion occurs, shows a linear increase. This implies a rise of the operating voltage needed to ensure good detector performances, and results in a higher risk of breakdown.

Low resistivity ($1 \div 2 \text{ k}\Omega \cdot \text{cm}$) substrates are interesting because they are known to reach type inversion at a higher neutron dose with respect to the "traditional" high resistivity ($4 \div 10 \text{ k}\Omega \cdot \text{cm}$) detectors [4]-[8]. This reflects on lower depletion voltages for the same integrated dose (after type inversion) and consequently additional safety factors in the operating voltage.

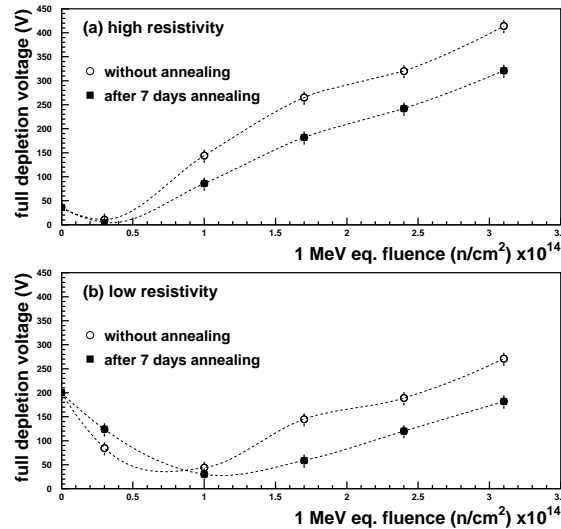


Figure 1: Depletion voltage of (a) high resistivity ($>5 \text{ k}\Omega \cdot \text{cm}$) and (b) low resistivity ($1.5 \text{ k}\Omega \cdot \text{cm}$) detectors at different values of 1 MeV equivalent neutron fluence. Measurements have been done on diodes both immediately after irradiation and after a 7 days annealing period.

Fig.1 compares the depletion voltage, as a function of neutron fluence, of low resistivity detectors to high resistivity ones for the same fluence. The measurements have been done immediately after irradiation and repeated after an annealing period of one week at room temperature. It can be noted that, after type inversion, low resistivity detectors can be operated at a voltage that is at least 100 V lower with respect to high resistivity ones.

The lower limit on resistivity is set by the depletion voltage before irradiation, which is specified to be lower than 300 V. To maintain reasonable safety factors in depletion voltage both before and after irradiation, the sensors for CMS will be selected by severe acceptance criteria in terms of breakdown performance ($V_{break} > 500$ V and current stability at 500 V better than 15% over 24 h).

The inter-strip resistance is another parameter that benefits from the lower depletion voltage of low resistivity detectors. Fig.2 shows the inter-strip resistance as a function of the bias voltage measured on irradiated detectors. Using low resistivity detectors it is possible to reach the optimal value of inter-strip resistance at a voltage ~ 100 V lower with respect to high resistivity detectors. It is worth noticing that in both cases the inter-strip resistance decreases from a few tens of $G\Omega$ before irradiation to a few tens of $M\Omega$, a value still acceptable to guarantee the isolation from neighbouring strips.

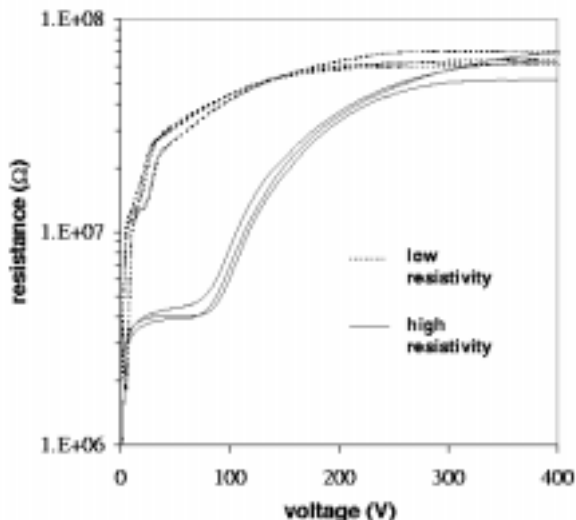


Figure 2: Inter-strip resistance as a function of bias voltage for low resistivity ($1.5 \text{ k}\Omega \cdot \text{cm}$) and high resistivity ($>5 \text{ k}\Omega \cdot \text{cm}$) detectors irradiated at $10^{14} \text{ 1 MeV equivalent n cm}^{-2}$. All measurements have been performed in DC. The substrates have $\langle 111 \rangle$ crystal orientation.

No drawbacks concerning leakage current and breakdown performance have been found using low resistivity substrates [9].

Modules equipped with low resistivity detectors and read out by APV6 fast shaping electronics have been successfully operated up to 500 V of bias voltage in beam tests. A detailed study of signal-to-noise ratio and detection efficiencies has also proved that their performance is very similar to that of high resistivity detectors [10].

3 $\langle 100 \rangle$ Crystal orientation

The use of substrates with $\langle 100 \rangle$ crystal lattice orientation has been extensively studied on prototypes (Hamamatsu, CSEM) produced from 4" and 6" wafers. The crystal orientation is an important parameter for the inter-strip capacitance, which is the dominant source of noise in our application.

Devices based on $\langle 111 \rangle$ crystal orientation show a significant increase of inter-strip capacitance after irradiation. The effect can be explained by the increase of oxide charge, due to radiation damage, in the interface region between the silicon substrate and the oxide layer used to passivate the detector [11], [12]. The positive oxide charge induces an accumulation layer of electrons in the surface region between two neighbouring strips, thus resulting in a higher inter-strip coupling.

In $\langle 100 \rangle$ crystal orientation the number of dangling bonds at the surface, and therefore the interface trap density, is one order of magnitude smaller than in $\langle 111 \rangle$ orientation. This makes $\langle 100 \rangle$ substrates less sensitive to surface radiation damage [13], [14] and therefore better suited to be used for silicon detectors in high radiation

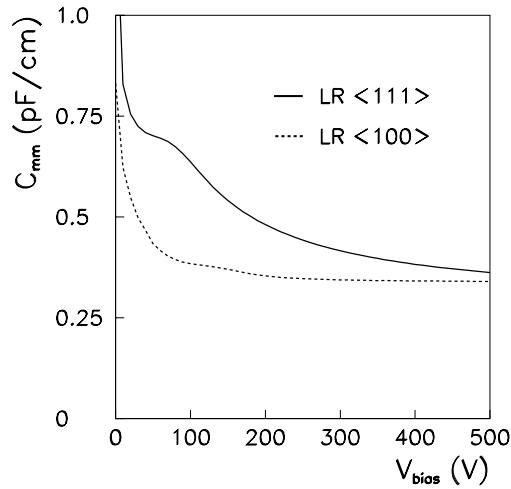


Figure 3: Inter-strip capacitance measured at 100 KHz between two neighbouring metal strips, on low resistivity detectors with different crystal lattice orientation, after irradiation at 10^{14} 1 MeV equivalent $n\text{ cm}^{-2}$. The strip pitch is $61\ \mu\text{m}$ and the strip width is $14\ \mu\text{m}$.

Fig.3 shows the inter-strip capacitance after neutron irradiation as a function of bias voltage for devices with different crystal orientation and similar initial resistivity. For $\langle 111 \rangle$ devices the pre-irradiation value can be recovered only by applying a large bias voltage, corresponding to an over-depletion by 200 V. On the other hand the $\langle 100 \rangle$ detectors reach the same plateau value at a considerably lower voltage.

4 “Thick” detectors

Large area modules ($\sim 180\text{ cm}^2$) will be used to equip the huge volume of the CMS Outer Tracker. Longer strips ($\sim 19\text{ cm}$) will minimize the number of readout channels. At the same time the position resolution required in these layers is less demanding thus allowing a large readout pitch ($122\div 205\ \mu\text{m}$). Longer strips and larger readout pitch can affect the total strip capacitance and therefore the noise performance when connecting the detector to fast shaping electronics.

In order to understand the effect of the strip pitch on the capacitance, an extensive set of measurements has been carried out on special R&D detector layouts with different geometries [15]. The results of this study show that, at a given thickness, the increase of backplane capacitance¹⁾ with the strip pitch is compensated by the decrease of inter-strip capacitance, as long as the strip width over pitch ratio is kept constant. As a first approximation the total strip capacitance per unit length depends linearly on the dimensionless ratio w/p , and can be parametrized as

$$C_{tot} = 0.8 + 1.7 \frac{w}{p} \text{ pF/cm.} \quad (4)$$

The 19 cm long strips foreseen for the outer region of the Tracker (to be compared with the 12 cm length of the inner region) imply a higher total capacitance. To avoid any deterioration of the signal-to-noise ratio, the

¹⁾ The backplane capacitance per unit length calculated with a semi-analytical solution of the Poisson equation [16] is given by

$$C_{bck} = \varepsilon_0 \varepsilon_S \frac{p}{d + pf(\frac{w}{p})} \quad (2)$$

where $f(x)$ is a function numerically approximated by

$$f(x) = -0.00111x^{-2} + 0.0586x^{-1} + 0.240 - 0.651x + 0.355x^2. \quad (3)$$

corresponding higher noise can be compensated using a substrate thicker than $300\ \mu\text{m}$, the standard value used in microstrip silicon detectors up to now.²⁾

We expect that in thicker detectors more charge is produced per incident track, but it is not obvious that this charge can be fully collected in heavily irradiated devices read out with fast shaping electronics. To verify the charge collection efficiency in thick devices a detailed program of measurements has been performed on prototypes with different thicknesses up to $500\ \mu\text{m}$.

Sets of prototypes have been produced by Hamamatsu ($320\div 410\ \mu\text{m}$) and ST Microelectronics ($500\ \mu\text{m}$) on $6''$ processing lines. Laboratory measurements have been performed on these devices to study how inter-strip and backplane capacitances scale with thickness.

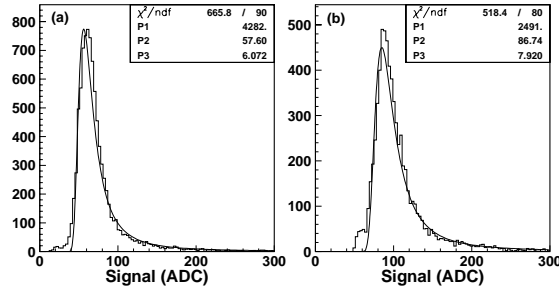


Figure 4: Signal measured with minimum ionizing particles on non-irradiated detectors with (a) $300\ \mu\text{m}$ and (b) $500\ \mu\text{m}$ thickness.

A few detectors were then irradiated above the fluence expected in the first layer of the Outer Tracker ($3.5 \times 10^{13}\ \text{n/cm}^2$). Some detector modules were assembled and read out with APV6 electronics. The behaviour of 400 and $500\ \mu\text{m}$ thick modules has been compared with a standard $300\ \mu\text{m}$ thick detector used as a reference.

Fig.4 shows a comparison of the signals produced by a $100\ \text{GeV}/c$ pion beam, measured on non-irradiated 300 and $500\ \mu\text{m}$ thick detectors. The most probable value of the Landau fit to the signal distribution is 58 counts for $300\ \mu\text{m}$ thick detector and 87 counts for $500\ \mu\text{m}$ thick detector, showing that the collected signal scales with the thickness. Similar results have been obtained with irradiated detectors using a β source, confirming that the charge collection efficiency is independent from the thickness even in irradiated devices [17], [18].

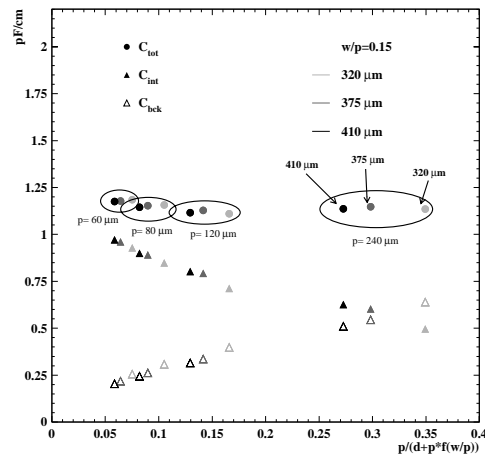


Figure 5: Inter-strip, backplane and total capacitance measured in non-irradiated devices of different thicknesses and strip width over pitch of 0.15 . The x coordinate represents the p/d ratio corrected for finite strip width (see footnote 1).

Both source and test beam data show that the noise is in first approximation independent from the detector thick-

²⁾ In order to maintain the depletion voltage below $300\ \text{V}$ before irradiation with thicknesses in the range $400\div 500\ \mu\text{m}$ it is foreseen to use $3.5\div 6\ \text{k}\Omega\cdot\text{cm}$ resistivity for the detectors of the Outer Tracker.

ness, providing that the strip pitch is kept smaller than the substrate thickness ($p/d < 0.8$). This noise behaviour can be explained if one assumes that the lower backplane capacitance in thicker detectors compensates the higher inter-strip capacitance due to a stronger coupling between neighbouring strips. This assumption has been confirmed by laboratory measurements. Fig.5 reports the measurements of backplane, inter-strip and total capacitance in 6" devices of different thicknesses but with the same value of the width over pitch ratio.

These measurements confirm the total strip capacitance parameterization given in (4), and in special mode its independence from the wafer thickness.

5 Conclusions

After a detailed investigation of detector properties in several series of prototypes the CMS collaboration has decided to adopt $\langle 100 \rangle$ crystal orientation for all sensors of the Tracker.

The detectors of the inner part will be based on sensors 300 μm thick and with a resistivity in the range $1.5 \div 3 \text{ k}\Omega \cdot \text{cm}$, while the Outer Tracker will be equipped with 500 μm thick sensors produced in standard production lines and having substrate resistivity between 3.5 and 6 $\text{k}\Omega \cdot \text{cm}$.

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