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The All-digital Approach to LHC

Power Converter Current Control

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Abstract

The design of the LHC machine imposes severe demands upon the control of current in the 1800 magnet circuits. This has required the use of novel methods for the control of individual power converters [1, 2] and of the magnet current control system as a whole. This paper will review the chosen hardware and software methods and architectures. The digital regulation techniques used to achieve the overall targets for short-term stability (< 3 ppm) and reproducibility (< 5 ppm) of the 24 principal LHC circuits will be discussed. While the proposed system architecture will follow the canonical three-layer design, so successfully exploited in LEP, the software will be far from traditional. This software must be more reliable and maintainable than ever before, and will need to integrate with advanced object-oriented applications via commercial middleware. These challenges will be faced by applying object-oriented techniques throughout the system and by harnessing the power of XML for system definition.

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1 HARDWARE

Powering a magnet circuit requires a voltage source combined with a system for control and regulation. At CERN, the combined unit is known as a Power Converter. In this paper we examine the new controller for LHC power converters, which will have two principal tasks:

- Management of the voltage source state.
- Regulation of the circuit current.

The same controller hardware will be used with all the different families of LHC voltage sources [3].

1.1 Computing platform

The control system for each voltage source will be a dedicated twin processor computer developed by our group. It features a 16-bit micro-controller[1] and a 32-bit floating-point digital signal processor[2]. The micro-controller manages all the system peripherals, including the field-bus interface, while the DSP performs the math intensive tasks of reference function generation and current regulation. The DSP is able to access the micro-controller's 256 KB SRAM memory, while having an independent 512 KB SRAM memory of its own.

A major effort has been made to make the controller radiation tolerant, using error detection and correction (EDAC) logic[3] with all the SRAM memories. Code for both processors will run out of flash memory, which is inherently tolerant. This will allow the LHC orbit corrector power converters to be placed in the tunnel underneath the accelerator, where radiation levels of 1-2 Gray per year are expected.

With so many circuits, the reliability of the controllers will have to be very high if operation is not to be continually interrupted. Great care is being taken in the choice of connectors and components to maximize reliability.

1.2 Analogue Interface

By implementing the current regulation feedback loop in software, the analogue performance of the system depends only upon the quality of the measurement of the current, which requires a transducer and an analogue to digital converter (ADC). The transducer will be a Direct Current Current Transformer (DCCT) that will produce a signal in the range ±10 V. The ADC will digitize this signal at 1 kHz. For the main LHC circuits, the ADC will use an ultra high precision temperature controlled 1 MHz Sigma Delta modulator, developed within the group [4]. For the rest of the circuits, a less expensive commercial 500 kHz Sigma Delta modulator[4] will be used. In all cases, the complete current measurement system will be duplicated for redundancy.

The absolute performance of the digital to analogue converter (DAC) is not critical, but it must provide monotonicity and good resolution. For the moment, we have achieved good results with a 20 bit audio DAC[5].

1.3 Network Interface

The network chosen for LHC power converter control is WorldFIP. This is a robust industrial field-bus, especially well suited to distributed real-time control systems. We will deploy the 2.5 Mbps version,

[1] Motorola MC68HC16Z1 (16 MHz)
[2] Texas Instruments TMS320 (32 MHz)
[3] Integrated Device Technology IDT49C465
[4] Burr Brown ADS 1201U
[5] Analog Devices AD1862N

which supports up to 32 stations and up to 500 m of cable without repeaters.

The network adapter has been designed in house using standard WorldFIP components. It provides a very cost effective network solution with low demands upon the micro-controller.

There will be around 100 field-buses for LHC power converter control with each one linked to the LHC real-time controls LAN by a gateway system.

1.4 Diagnostic Interfaces

The controller has three diagnostic interfaces:

1. RS232 9.6 kbaud: This can support a dumb terminal for a human operator, or a local control program such as Labview running on a workstation.
2. Parallel 192 kbaud: This links to a 1 kHz diagnostic data acquisition system based on a standard PC running a program written for Matlab.
3. Serial 500 kbaud: This links to as many as 30 small diagnostic data input cards that can be distributed inside the voltage source. Each card can collect 4 analogue signals (12-bit resolution) and 24 digital signals at 100 Hz.

Interfaces 1 and 2 will normally only be used for local diagnosis of a problem with a controller or circuit. Given the size of LHC, remote diagnosis of voltage source problems will be very important so interface 3 will always be connected to data input cards permanently installed in the voltage source.

The controller also has a debug interface for each processor: BDI for the micro-controller and MPSD for the DSP.

2 SOFTWARE

There are three main elements to the *real-time* software:

- Code for the micro-controller, based on a real-time operating system (RTOS).
- Code for the DSP, based on interrupts.
- Code for the gateway system, based on the LynxOS RTOS.

There is also a large component of offline software written in PERL that processes the system definition files, and non-real-time code written in C++ and JAVA that integrates the communications middleware.

2.1 Micro-controller code

The MC68HC16Z1 is a low cost 16-bit integer micro-controller with powerful on-chip interface components, including a general purpose timer (GPT) and queued serial module (QSM). The software has been written in C and assembler using Metrowerks tools, and is built on a tiny real-time kernel called NanOS. This has been written in house, based on MicroC/OS-II [5].

The code supports two sources of commands simultaneously: (i) the RS232 serial interface, and (ii) the WorldFIP field-bus interface. The field-bus interface also receives synchronized time-of-day packets that trigger a software phase locked loop to discipline the local 1 kHz real-time clock. Millisecond events such as *start-ramp* are also received in the time-of-day packets. These allow all the power converters to ramp synchronously.

The micro-controller is responsible for managing the DSP and the state of the voltage source. The state machine is formulated as a Petri net[6] run at 200 Hz.

2.2 DSP code

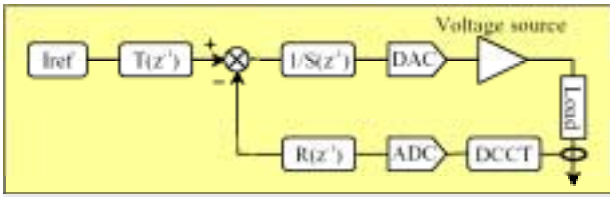
The TMS320C32 is a low cost 32 bit DSP, which provides fast floating point multiply and add. The DSP code is almost entirely written in C using T.I. tools. It is not built on a RTOS, but instead uses four prioritized interrupt levels to perform up to four "tasks" concurrently. This is possible because the DSP tasks are all slaves of micro-controller tasks and do not intercommunicate.

The primary duty of the DSP is the regulation of the current. This uses a control algorithm based on the RST tri-polynomial form in which the performance of the regulation (R, S) and tracking (T) can be independently optimized [6]. This is illustrated in figure 1. The polynomials have been chosen to match an inductive load and support two integrators. As a result, $R(z^{-1})$ has three coefficients, $S(z^{-1})$ has four and $T(z^{-1})$ five.

The small signal closed loop bandwidth for LHC circuits will be in the range 0.1 Hz to 5 Hz. The RST algorithm is typically run 20 times faster than this. The ADC is always sampled at 1 kHz so that the measurement can be filtered digitally to remove 50 Hz noise and to compensate for the measurement delays.

2.3 Gateway code

The gateway has demanding real-time constraints and the code is mostly written in C under LynxOS. There will be a small component



[6] http://www.daimi.au.dk/PetriNets

Figure 1: Current Regulation Loop

of C++ for the interface with the middleware, but this will not be real-time. The gateway has the function of passing commands from application programs to the power converter controllers via the WorldFIP field-bus. Command responses are returned in the other direction. It also acts as a real-time conduit for current reference corrections from beam feedback applications (e.g. orbit and tune), and for power converter status data from the controllers. Both corrections and status will be sent at 100 Hz over the field-bus. The status data for all the controllers belonging to the gateway will be sent using UDP to a central data server. Real-time applications will be able to subscribe to status data for the whole system via this server. The server will also publish the status data via the middleware for applications that require data rates of less than 1 Hz.

2.4 Middleware

Communication between LHC control applications and the gateways will be via commercial middleware. The middleware chosen for LHC is CORBA[7], which is an open standard and supports many different platforms and languages. LHC applications will be written in JAVA, while the server side will be C++ and C. CORBA provides asynchronous command-response and publish-subscribe communication.

All the 1800 LHC power converter controllers and the 100 gateways will be visible through the middleware as named *devices.* A device is a logical grouping of typed data items known as *properties*. The middleware enables an application to set and get/subscribe to device properties without needing to know physically where they are.

For JAVA applications, the complete device property model will be encapsulated into a JAVA class that will hide the middleware interface from the application writer.

2.5 PERL and XML

All the properties for the different classes of devices are defined along with documentation in XML files. The files are parsed by PERL scripts that generate C header files, HTML pages and code for the JAVA class, including appropriate JavaDoc. This approach is fundamental to the reliable management of the system, and makes extending the functionality relatively simple and secure.

3 CONCLUSION

More than 20 prototype systems have been successfully deployed during the past 12 months, and our confidence in a digital regulation solution has been justified. The final design for the LHC controller is now in development with pre-series production scheduled for the end of 2002, and series production during 2003.

The complete system software should be operational in 2003 when it will be tried out with the LHC magnet test facility.

4 ACKNOWLEDGEMENTS

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