IMPLEMENTATION OF FAST HISTORY MECHANISM IN THE NSLS MICRO SYSTEMS[1]

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Abstract

In the NSLS control system, slow and fast history programs for data collection and retrieval run at the high level computers. The fast history collects data from the front-end control computers (micro subsystems) at 5 to 30Hz rates in a ring buffer and dumps it to a disk file on request. This is a very useful diagnostic tool for machine operations. The software for the micros has been upgraded to implement fast history in the front-end computers. This paper discusses the procedures for the specifications of parameter list, rates for data collection and the advantages of this approach.

1 INTRODUCTION

The National Synchrotron Light Source Facility at Brookhaven National Laboratory consists of two storage rings, one for VUV operating at 750 Mev and one for Xray at 2.5 Gev and a common injection system (a linac and a booster). The control system has a two-level distributed architecture [1]. High performance HP700 series workstations constitute the high-level (operator level). They communicate via high-speed Ethernet with VME-based micro subsystems (Motorola 68k series and power PC's) at the equipment level. As in any accelerator or storage ring control system, tools for data archiving (history), data retrieval and display have been developed at workstation level and they are widely used for diagnostics and other purposes. This paper discusses the implementation of history in the micro systems for fast varying signals and its advantages.

2 LIMITATIONS OF HIGH-LEVEL FAST HISTORY PROGRAMS

In the present control system, the history programs run at the operator level. Any authorized user can create a directory in a dedicated history disk and specify in a file the parameters of interest, the rates for data collection, etc. and then start the history process. There are two types of history programs [2].

2.1 Slow History

The program collects data from the micro subsystems as per specifications and writes it to the designated directory. One file is generated for each day with the date as the file name (ex. Sep298). Even though, in theory, the rate can be as fast as the network can handle, slow history is used only at 1Hz or lower rates to avoid huge sets of data on the hard disk and network congestion. The present slow history is more than adequate for slowly varying data (such as beam current, vacuum, lifetime, energy, radiation doses from detectors located at different areas, beam line status etc.).

2.2 Fast History

The program polls the micro subsystems responsible for the specified parameters and writes the data to a ring buffer in the program memory. The data is dumped to a disk on demand. The maximum rate is 30 Hz. Usually the fast history is used to provide 2 to 120 minutes worth of data prior to the time at which the dump request is made. The user specifies the duration for which the data is required. The program allocates memory large enough to hold the data for the requested duration and rate. The present fast history is very useful for detecting equipment problems, and for determining the causes for unexpected beam motion or dump.

2.3 Limitations

However at NSLS, some power supplies are ramped at rates 1 to 10 kHz and analog signals from the supplies are digitized at the same rate. In some micros (X-ray and UV orbit systems), the data is acquired at rates higher than 100 Hz. Archiving of analog signals digitized at rates higher than 50 Hz using fast history is very challenging. It puts a heavy burden on the network. When a critical event occurs, the data is saved on the disk by a manual dump request. With fast varying signals, one can miss the data that led to the critical event. Also time correlation of data from multiple stations is difficult. These limitations can be overcome by implementing fast history in the micros.

3 FAST HISTORY IN MICRO SUBSYSTEMS

The software that runs in the VME micros consists of a real-time kernel and real-time tasks and is referred to as NSLS control monitor [3]. The core software is standard for all micros and it manages communication, command-decoding etc. The software views the input and output signals as logical devices or as a set of logical devices. High level programs access these devices by meaningful names. A standard device format is used to store the various information about the device. It supports

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calibration arrays and four data arrays. The format is upgraded to support fast history data buffer. The software treats the micro system itself as a logical device. The system device is similar to any device and is used for sending global commands and storing system data in memory.

History data can be saved as one block in the system history buffer or in the history buffer of individual devices. The block-saving is used when the CPU time is intensively used for high-speed data acquisition. The data collected for all signals in one scan are packed as one block with time-stamp and stored sequentially in the ring buffer. Both system and device history buffers start with a header. It contains the size of the header, a function code to indicate the data format of each item (e.g. every data with time-stamp or one time-stamp at the start of acquisition), time interval between successive data or scans (wherever applicable), pointer to the last updated data in the buffer, etc. The header supplies all the information necessary for data analysis and display. The system device has two arrays for configuration purposes. One array is used when history is saved as block. The array is initialized with the number of devices in one block and the order in which they are scanned. The second array is dynamically configurable. The operator loads the array with a list of devices (for which the history is required), collection rate and duration of the history data. When a configuration array is received, the micro stops the current history collection and evaluates the memory requirement. If enough memory is available, the software allocates history buffers to the specified devices, reinitializes the headers and starts the data collection. Otherwise, an error message is sent to the operator. When a micro receives a global *Halt history* command, it will stop further update of history. The history can also be stopped by an interrupt triggered by a critical event.

A general purpose light source (GPLS) board is an integral part of every micro subsystem [4] and it provides timers, ASCII video, bus interrupter and a Time-code reader/generator. The time-of-day information can be read with a micro-second resolution. This is used to time stamp the data.

In the following sections, three examples with different sampling rates are described.

3.1 Sampling Rates (1 kHz to 100 kHz)

For such high-speed digitization of analog signals, commercial or custom boards with sufficient on-board memory and preferably with block transfer capability across the VME-bus, are used. Depending on the requirements, the input signals can be continuously digitized and stored in the board's buffer. By monitoring the flags for half-buffer and full-buffer, the first and second halves of the buffer can be alternatively emptied into the CPU memory and saved in history buffers. When a *halt history* request or an interrupt initiated by a critical event is received, the system will copy the last segment of digitized data to the ring buffer and stop the history update. The workstation can retrieve the data for analysis. Instead of continuous sampling, digitization can be started and stopped by giving an arm and a halt signal (interrupt) and the data can be moved to the history buffer with time stamp information.

In the NSLS facility, during injection the booster power supplies (dipole, quadrupole etc.) are ramped at the start of every booster cycle (830 millisec. period). The ramping rate is 10 kHz. To achieve good injection or to diagnose problems, if any, the current, voltage read-backs and error signals from the supplies have to be monitored at the same ramping frequency. For this a commercial fast ADC board from VME Microsystems International Corporation (VMIC) is used. The board has 16-bit digitizing resolution on 16-channels, simultaneous sample/hold and a data buffer up to 8 Mbytes. Maximum sampling rate is 100 kHz. The board can use either an internal sampling clock or an external clock. In transient capture mode, the board samples the input signals and stores the data sequentially in its memory buffer. When the capture trigger is given, the board completes the circular buffer and returns to idle mode. The address of the buffer at the trigger point (location of the first sample) is saved in its address register. For the booster application, the board is used in transient capture mode. The buffer is set up to hold samples for 800 milli-sec. from the start of the booster cycle. The booster start cycle is used for triggering the capture. The sampling clock is 10 kHz (the same one used for ramping). When the buffer is full, the data is quickly moved before the start of the next cycle. Since the CPU is relieved of data acquisition, the system has time to save the data in the history buffer of each device and update its data array. The arrays are double buffered and can be accessed at any time from a workstation. Figure 1 shows the history data for three signals of the booster dipole for one booster cycle.

Figure 1:Booster Dipole Signals for one Booster Cycle.

The history buffer size is set up to save data for 10 booster cycles. The memory required for 16 channels for 10 booster cycles is 2 to 3 megabytes. When a command or interrupt is received for halting, the history update stops.

3.2 Sampling Rates (100 to 500 Hz))

For these rates, inexpensive, multiplexed ADC boards (Acromag 9330) are used. The board has 16 channels and a 14-bit resolution. When a channel is selected, the time required for conversion is ~64 micro-sec. (settling time is 33, acquisition time is 14 and conversion time is 17 micro-sec.). The board allows selection of the next channel after the conversion is started for the current one. By overlapping, all 16 channels can be read in less than 1 milli-sec. Using proper software strategy, data acquisition rates as high as 500 Hz have been realized in systems with 200 signals. For measuring X-ray beam orbit, the ring has 48 pick-up electrodes, each generating 4 signals (a total of 192). The micro has 12 Acromag ADC boards. The system generates a pulse every 100 micro-sec., which is used to trigger the boards externally. The same pulse invokes an interrupt handler in which the CPU switches the multiplexor to the next channel for all boards. A delay circuit generates another interrupt after 20 micro-sec, during which the conversion is complete for the current channels. The data is read for the converted channels from all boards in the interrupt routine. It takes 1.6 milli-sec. to read 192 channels (with a settling time of the order of 100 micro-sec). The next 2 interrupt slots are used to move the data to another buffer before it is overwritten by the next data acquisition cycle. A background task uses the buffer to update the individual devices as well as the system history buffer. The data for each cycle is stored sequentially in the history buffer of the system device with time-stamp. The header section of the buffer provides all the necessary information (number of devices, interrupt rate, data size, a pointer to the last cycle, etc.). The mapping information between the device names and the ADC channels can be obtained from the system block configuration array. For 192 signals with 2 bytes of data and a data acquisition rate of 500 Hz, approximately 12 megabytes of memory are needed for 2 minutes of fast history. Since the CPU time is heavily used in data acquisition, the history data is saved as a block for this micro.

3.3 Sampling Rates (100Hz or lower)

The data acquisition rates used in transport power supplies and RF systems are 40 to 100 Hz. A scan task can read the data within 1 milli-sec. for all boards (by reading channel 0 of all boards, then channel 1 and so on). The task needs to wait only for ~50 micro-sec. for settling and conversion irrespective of the number of ADC boards in the system. Since the CPU is not heavily time-bound, the data can be saved in the history buffer of the requested devices with time-stamp. The time-stamp needs to have only a milli-sec. resolution. For each data with time stamp, 6 bytes are needed. This can be reduced if 3 bytes are used except when there is a roll-over to the most significant byte. At 100 Hz rate, with full time stamp, one requires 72 kbytes for 2 minutes of history for one device.

4 CONCLUSIONS

The fast history mechanism in the front-end micro systems allows one to archive data, as fast as it is acquired and there is no load on the network. The fast history can be stopped by a critical event simultaneously for all the systems relevant to that event. As an example, a micro monitoring the beam current can initiate a trigger to all the relevant micros when a beam dump is recognized. The workstation can retrieve the fast history collected prior to the event and can do time correlation and post-mortem analysis. The trade off are: (1) every micro requires more memory and (2) the CPU needs to move lots of data in memory. With the availability of high-speed CPU boards with large on-board memory and inexpensive memory boards, these are not big issues.

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REFERENCES

[1] J.D.Smith, S.Ramamoorthy, Y.Tang, “NSLS Control System Upgrade”,Nucl.Inst. and Methods in Phys. Res, A32, p114, 1994.

[2] Y.Tang , J.D.Smith, “History Data Collection in NSLS Control System”, PAC, Dallas, p2253,May1995.

[3] S.Ramamoorthy, J.D.Smith, “NSLS Control Monitor and its Upgrade”, PAC, Washington D.C., p1849, May 1993.

[4] S.Ramamoorthy, J.D.Smith, “GPLS VME Module: A Diagnostic and Display Tool for NSLS Micro Systems”, PAC, New York, p690, Mar 1999.