HIGH-SPEED MULTICHANNEL ICs FOR FRONT-END ELECTRONIC SYSTEMS

A.Goldsher, Yu.Dokuchaev*, E.Atkin**, Yu.Volkov***

**-- State unitary enterprise "Science and Technology Enterprise "Pulsar", Russia, 105187, Moscow, Okruzhnoy proezd, 27.*

*** -- Moscow State Engineering Physics Institute (Technical University), Russia, 115409, Moscow, Kashirskoe shosse, 31.*

Abstracts

The basic set of high-speed multichannel analog ICs for front-end electronic systems, designed and put into production in Russia, is considered. It is implemented as a number of application specific ICs (ASIC) and ICs, based on an application specific semicustom array (ASSA), containing eight channels of analog signal collection and preliminary processing.

By their electrical parameters the created ICs are on a par with foreign functional analogs.

The prospects of the further development of analog front-end ICs in Russia are expounded.

Introduction

Contemporary front-end electronic systems, intended, particularly, to carry out research in high-energy and elementary particle physics, show a demand for an increase in the number of data collecting and processing channels, reaching nowadays some hundreds thousand and expected to reach several millions during the nearest 5…7 years.

In its turn that demands a radical change in the approach to the creation of front-end electronics, which should simultaneously provide a high speed, wide dynamic range, relatively low power consumption, high sensitivity, as well as an increased radiation hardness, since the electronics is placed either directly on the radiation detectors or in the vicinity of them. Besides that, especial importance is acquired by such factors, as dimensions, cost, durations of design and manufacture of printed circuit units.

The multichannel equipments of physical experiment, of environment monitoring, of nuclear reactor safety and fissionable material supervision are united by common algorithms of analog signal processing. That allowed the specialists of certain Russian enterprises to create in short terms a basic set of analog ICs for front-end electronic systems. It was implemented within the framework of a project, financed by the International Science and Technology Center, in the forms both of application specific ICs (ASIC) and an application specific semicustom array (ASSA).

The generalized structural diagram of a front-end electronic channel, considered in [1], is shown in fig.

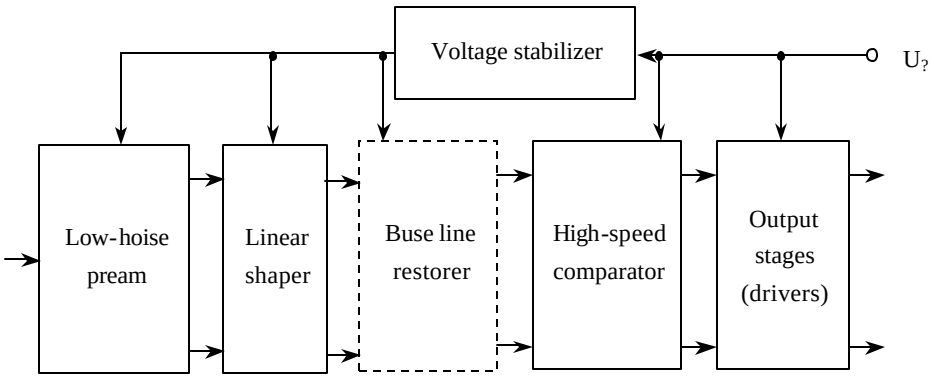

Fig. Generalized structural diagram of a channel of front-end electronic

Types of ICs and basic peculiarities of their design and technology.

At present the basic set of ICs includes:

- an ASIC containing a high-speed comparator and D-trigger, intended for application in fast timing (fractions of nanosecond) circuits – A1181;
- a 4-channel ASIC of an amplifier-shaper with differential input and output, intended for amplitude data processing (amplification, filtration) – A1182;

- a 4-channel ASIC of a differential low power comparator of the nanosecond range, intended for analog signal discrimination – A1183A;
- a 4-channel ASIC of a differential comparator of the nanosecond range, having an output stage with open collector and implementing the OR-function with four inputs – A1183?;
- the LSIC A1184, implemented with the analog ASSA.

The use of ASSA allows by means of changing only the plating layers the creation of ASICs, which circuitry takes into consideration the peculiarities of specific physical experiments, and that is done within exceptionally short terms and at low costs.

The circuitry of ICs, the contents of ASSA functional modules have been elaborated by the specialists of the Electronics Department of the Moscow State Engineering Physics Institute (Technical University), namely E.Atkin, Yu.Volkov, I.Ilyushchenko, S.Kondratenko, Yu.Mishin and A.Pleshko.

The lay-outs of all ICs are protected by copyright documents, what witnesses on their novelty and originality.

The set of active devices of ICs contains NPN transistor structures, including those with Shottky diodes, and PNP vertical transistors with collectors in substrate [2]. The set of passive devices contains high- and low-resistance resistors and capacitors based on MOS structures. The range of working currents of standard (library) elements extends from fractions of mA to (3…5)mA, the values of resistors – from tens of Ohm to tens of kOhm.

The employment of such an element basis provides simultaneously high electrical parameters of IC, resistance to external disturbing factors, easiness of the processes of IC manufacture, high yield and, hence, a low cost.

The technological process of IC manufacture is based on the planar-epitax technology with element insulation by a reverse-biased p-n junction. The insulating boron diffusion is then conducted by using highly doped p^+-layers with a retention of boron-silicon glass before the second stage of diffusion. Comparing with usually applied modes, that allowed to reduce the stray capacitances of insulating layers by 1.5 times [3].

One should also regard as basic ones the following technological peculiarities of ICs:

- small depths of p-n junction embedding, equaling fractions of um (base width h_B~0.1um), what ensures (at appropriate element lay-outs and manufacturing processes) a unity-gain frequency about 7GHz for n-p-n transistor structures;
- the use of antimony, boron and arsenic ion doping, what ensures high reproducibility of layer electrophysical parameters in a wide range of dopant concentrations;
- small sizes of elements, that influence the IC speed to the greatest extent, particularly, the use of the so-called full emitter; the minimal emitter size is restricted, in its turn, by the requirements to the collector bulk resistance r_C of transistor structures;
- the use of molybdenum as a barrier metal in Shottky diodes; molybdenum, comparing with aluminum or platinum silicide, has a considerably lower potential barrier f_B, what allowed to provide simultaneously the specified direct voltage drops U_D and a low value of stray capacitances C;
- the use of a double-level plating, based on aluminum, doped with silicon (about 1%); as an interlayer dielectric there was used the silicon dioxide film, partially doped with phosphorus.

Parameters of ICs

IC A1181

Functional destination: the IC is intended for use in arrangements of nanosecond pulse processing.

The basic parameters of functional modules:

Parameters of comparator

Name of parameter, literal designation, unit of measurement	Range of parameter values	
	? min	Xmax
Input offset voltage, U_{OF}, mV	-3.0	+3.0
Input bias current, I_{BI}, uA		25.0
Difference of input bias currents, I_{DBI}, uA		5.0
Range of input voltages, ΔU_{IN}, V	-2.5	+2.5
Current consumption from first supply source, $I_{CON.1}$, mA		21.0
Current consumption from second supply source, $I_{CON.2}$, mA		30.0
At ECL output		
Output voltage high, U^1_{OUT}, V	-1.00	-0.73
Output voltage low, U^0_{OUT}, V	-1.00	-1.60
Switching time, t_{SW}, ns		2.0
Transition time at switch-on (switch-off), $t^{1,0}$ ($t^{0,1}$), ns		2.0 (2.0)
At TTL output		
Output voltage high, U^1_{OUT}, V	2.4	4.0
Output voltage low, U^0_{OUT}, V	0.2	0.6
Output current, I_{OUT}, mA	4	10
Switching time, t_{SW}, ns		15
Transition time at switch-on (switch-off), $t^{1,0}$ ($t^{0,1}$), ns		15 (15)

Parameters of ECL D-trigger

Name of parameter, literal designation, unit of measurement	Range of parameter values	
	? min	Xmax
Input current low at the D, C, R inputs, I^0_{IN}, uA		0.5
Input current high at the D, C, R inputs, I^1_{IN}, uA		0.8
Input voltage low, U^0_{IN}, V	-2.0	-1.5
Input voltage high, U^1_{IN}, V	-1.1	-0.73
Output voltage high, U^1_{OUT}, V	-1.0	-0.73
Output voltage low, U^0_{OUT}, V	-1.95	-1.60
Output current from output Q, I^Q_{OUT}, mA		50
Propagation delay of signal at inputs C and R, $t_{PR.D}$, ns	0.8	1.5
Transition time at switch-on (switch-off), $t^{1,0}$ ($t^{0,1}$), ns	0.6 (0.6)	1.3 (1.3)
Current consumption, I_{CON}, mA		60

Parameters of ECL-NIM converter

Name of parameter, literal designation, unit of measurement	Range of parameter values	
	? min	Xmax
Input current low (in statics), I^0_{IN}, uA		10
Input current high (in statics), I^1_{IN}, uA	7	10
Propagation delay of signal, $t_{PR.D}$, ns		0.8
Transition time at switch-on (switch-off), $t^{1,0}$ ($t^{0,1}$), ns		2.0 (2.0)

The IC has two supply sources, the voltages of which are, correspondingly, U_{SS1}=3V, U_{SS2}=-3V.The permissible spread of supply voltages is ±5%.

The IC is placed in the case H06-24-2b. It is available also in a caseless version (modification 4).

IC A1182

Functional destination: the IC is intended to amplify and shape signals, coming from high-resistance radiation detectors.

Basic parameters of the four-channel amplifier-shaper IC

Name of parameter, literal designation, unit of measurement	Typical value of parameter
Transimpedance, R_T, kOhm	10
Input impedance, R_{IN}, Ohm	160
Output rise-time, t_R, ns	5
Output pulse duration at base level, t_P, ns	40
Output signal full swing, U, V	0.8
Range of input currents, I_{IN}, uA	1÷100
Crosstalks of neighboring channels, %	≤1
Power consumption per channel, P_{CON}, mW	15

The IC has two supply sources, the voltages of which are, correspondingly, U_{SS1}=3V, U_{SS2}=-3V.The permissible spread of supply voltages is ±5%.

The IC is placed in the case H09-28-1b. It is available also in a caseless version (modification 4).

IC A1183

Functional destination: the IC is intended for analog-to-digital signal conversion.

Basic parameters of the four-channel comparator IC

Name of parameter, literal designation, unit of measurement	Value of parameter
Input currents, I_{IN}, uA	8
Input offset voltage, U_{OF}, mV	5
Comparator threshold, U_{TH}, mV	10÷180*
Dynamic range, D_R, V	3.0
Rise-time t_R, ns	3
Fall-time t_F, ns	3
Propagation delay of signal, $t_{PR.D}$, ns	6
Maximal common-mode voltage, U_{CM}, V	±1.1
Power consumption per channel, P_{CON}, mW	18
Output signal logic	GTL (TTL)

Remarks:

*- the threshold voltage is given for the case of using the comparator together with amplifier-shaper A-1182;

**- GTL – low-level CMOS logic (logic unity -- +1.2V, logic zero -- +0.4V).

The IC has two supply sources, the voltages of which are, correspondingly, U_{SS1}=3V, U_{SS2}=-3V. The permissible spread of supply voltages is ±5%.

The IC is placed in the case H06-24-2b. It is available also in a caseless version (modification 4).

LSIC A1184

The LSIC contains 8 channels, collecting and processing preliminary the analog signals from tracking detectors. Each channel contains: a low-noise preamp, linear shaper, comparator and output driver. The LSIC contains also one OR-circuit, common for the 8 channels. It is implemented on the basis of an ASSA, containing 7000 elements, including approximately 1400 n-p-n transistor structures with a unity-gain frequency of 7GHz [3].

The printed circuit units (PCU), created in the Research Institute of Pulse Technology (Moscow) on the basis of the above described ASICs and LSIC, by their electrical characteristics are on a par with the PCUs, implemented with the LSIC ASD/BLR, designed in the Pennsylvania University (USA) and widely used by research centers in the advanced countries of the world [4].

As it was marked earlier, the active devices of the ICs A1181…A1184 are n-p-n transistor

structures. One should acknowledge, that the absence of complementary high-frequency transistor structures entails a complication of circuitry, deterioration of performance of ICs and in some cases practically excludes the possibility to implement some important units in a differential version. Therefore the further improvement of the ICs for front-end electronics depends on the creation of LSICs, containing n-p-n and p-n-p high-frequency transistor structures with unity-gain frequencies not less than (2…3)GHz, sufficiently close values of their basic electrical parameters and using dielectric insulation. That will, particularly, allow to:

- increase considerably the ratio of speed to power consumption – the major quality index of multichannel ICs; that is especially important for amplifiers and comparators, driving a large capacitive load;
- increase essentially (1.5 - 2 times) the integration scale at the expense of using p-n-p transistor structures as current setting elements instead of resistors with high nominal value;
- exclude practically the mutual coupling of IC channels through supply sources at the expense of introducing internal voltage stabilizers, built with complementary transistors; those stabilizers should meet stringent requirements on the voltage drop (not exceeding 100 – 300mV) and efficiency (not less than 90%), whereas practice shows, that a voltage stabilizer, built with n-p-n transistors only, can not have a voltage drop less than (1…1.5)V and an efficiency greater than (60…70)%.

The elaboration of an ASSA, based on n-p-n and p-n-p high-frequency transistor structures, is conducted at present by the specialists of a number of Russian enterprises.

The created set of high-speed analog ICs has successfully passed probation in the equipment of the leading Russian and international research centers. It can find application not only in front-end electronic systems, but also in those of ecological and radiational environment monitoring, spectrometric material analysis, in space and medical research.

Conclusion

1. At present in Russia the following ASICs and LSIC for front-end electronic systems have been designed and put into production:

- an ASIC containing a high-speed comparator and D-trigger, intended for application in fast timing (fractions of nanosecond) circuits;
- a 4-channel ASIC of an amplifier-shaper with differential input and output, intended for amplitude data processing (amplification, filtration);
- a 4-channel ASIC of a differential low power comparator of the nanosecond range, intended for analog signal discrimination;
- a 4-channel ASIC of a differential comparator of the nanosecond range, having an output stage with open collector and implementing the OR-function with four inputs;
- the LSIC, implemented with the analog ASSA.

- 2. The process of IC manufacture is based on the planar-epitax technology with insulation of elements by a reverse biased p-n junction. Among the design and technology peculiarities the following ones should be regarded as basic:
- the use of highly doped p+-layers (NS ~ $4*10^{20}$ cm^{-3}) for element insulation, what in combination with the retention of boron-silicon glass before the second stage of diffusion allowed to reduce 1.5-fold the stray capacitances of insulating junctions, comparing with the commonly used modes (NS ~ $4*10^{18}$ cm^{-3}).
- small depths of p-n junction embedding, equaling fractions of um (base width h_B~0.1um), what ensures (at appropriate element lay-outs and manufacturing processes) a unity-gain frequency about 7GHz for n-p-n transistor structures;
- the use of antimony, boron and arsenic ion doping, what ensures high reproducibility of layer electrophysical parameters in a wide range of dopant concentrations;
- small sizes of elements, that influence the IC speed to the greatest extent, particularly, the use of the so-called full emitter; the minimal emitter size is restricted, in its turn, by the requirements to the collector bulk resistance r_C of transistor structures;
- the use of molybdenum as a barrier metal in Shottky diodes; molybdenum, comparing with aluminum or platinum silicide, has a considerably lower potential barrier f_B, what allowed to provide simultaneously the specified direct voltage drops U_D and a low value of stray capacitances C;
- the use of a double-level plating, based on aluminum, doped with silicon (about 1%); as an interlayer dielectric there was used the silicon dioxide film, partially doped with phosphorus.

3. On the basis of the designed ASICs and LSIC there have been implemented PCUs, by their electrical parameters being on a par with those implemented with the LSIC ASD/BLR, created in the Pennsylvania University (USA) and widely used by research centers in the advanced countries of the world.

References

1. E.Atkin, Yu.Volkov, S.Kondratenko, Yu.Mishin, A.Pleshko. “Analog signal preliminary processing ICs, based on bipolar semicustom arrays” – Scientific Instruments, 1999, #5, pp.54-57.
2. A.Goldsher, V.Kucherskiy, V.Mashkova. “Components of Fast Analog Integrated Microcircuits for Front-end Electronic Systems” – Fourth Workshop on Electronics for LHC Experiments. Rome, September 21-25, 1998, pp.545 – 549.
3. A.Goldsher, V.Kucherskiy, V.Mashkova. “A Semicustom Array Chip for Creating High-speed Front-end LSICs” – Third Workshop on Electronics for LHC Experiments. London, September 22-26, 1997, pp.257 – 259.
4. E.Atkin, Yu.Volkov, Yu.Mishin, V.Subbotin, V.Chernikov. “Electronic units for the collection and preliminary processing of multiwire chamber signals” – Scientific Instruments, 1999, #5, pp.58-62.