Printed Circuit Board Signal Integrity Analysis at CERN.

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Abstract

Printed circuit board (PCB) design layout for digital circuits has become a critical issue due to increasing clock frequencies and faster signal switching times. The Cadence® SPECCTRAQuest™ package allows the detailed signal-integrity (SI) analysis of designs from the schematic-entry phase to the board level. It is fully integrated into the Cadence® PCB design flow and can be used to reduce prototype iterations and improve production robustness. Examples are given on how the tool can help engineers to make design choices and how to optimise board layout for electrical performance. Case studies of work done for LHC detectors are presented.

I. INTRODUCTION

A. High-speed digital design

Electronic Design Automation tools are becoming essential in the design and manufacture of compact, high-speed electronics and have been extensively used at CERN to solve a wide range of problems [1], [2].

A typical fast digital system poses many high-speed signal integrity questions (Figure 1).

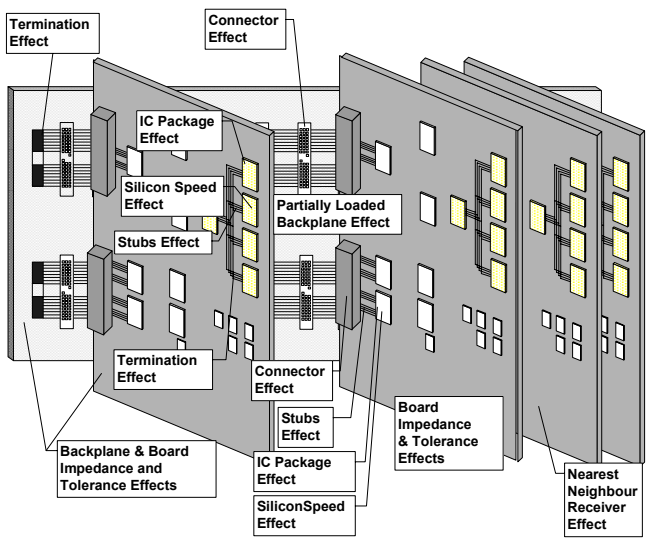

Figure 1: Typical backplane and onboard bus systems

Some rules of thumb can be applied to try and achieve a working design. These include:

- A track should be considered as a transmission line when:
  $2tpd \geq tr$
  where tpd is the propagation delay for an interconnect length and tr is the signal switching time.
- For a digital signal with switching time tr, the equivalent bandwidth is given by:
  $$F = \frac{1}{\Pi tr} \Rightarrow \frac{0.32}{tr}$$
  Note that this expression is dependent only on switching speed and not clock frequency.
- For a backplane, the effective loaded transmission-line characteristic-impedance (Zeff) can be estimated as [3]:
  $$Zeff \cong Zo \frac{1}{\sqrt{1+\frac{Cl_{oad}}{C}}}$$
  Zo = unloaded transmission-line characteristic-impedance
  C = Total unloaded transmission-line capacitance
  Cload = Total load capacitance along the backplane line.

The above guidelines are very useful but insufficient to ensure a working design. Other rules of thumb exist to estimate crosstalk and reflections but it becomes impractical to apply them all to a large design with many nets.

The Cadence SPECCTRAQuest SI Expert suite was developed to try and overcome these problems. It has three main components (Figure 2).

SigXplorer has been primarily used at CERN during the pre-layout stage. It can be used to perform "what if" analyses and to determine the effects of different design and layout strategies on signal integrity. While fully integrated into the Cadence flow, it is simple enough to be used as a standalone tool.

The program represents a circuit as a number of drivers and receivers that are linked via interconnects (Figure 3). The user can explore different placement and routing strategies and is free to experiment with parameters such as track impedances and terminations and choice of IC technology.

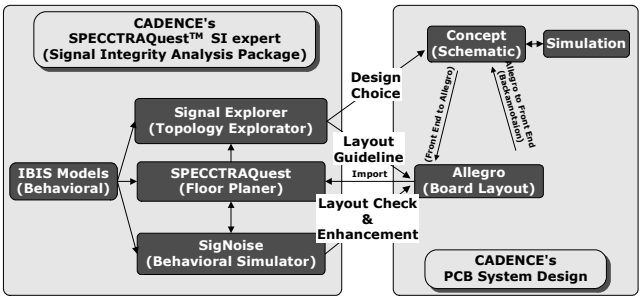

Figure 2: Signal Integrity Design Flow

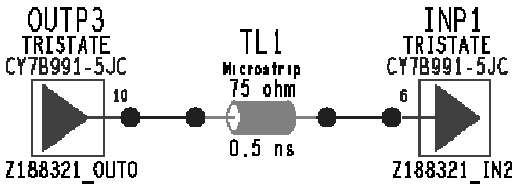

Figure 3: Typical SigXplorer pre-layout analysis

Typical design choices to be considered would be:

- Architecture evaluation (bus, clock tree…)
- Topology exploration
- Standard ICs technologies comparison
- Termination type and value characterization
- Package type selection
- ASICs I/O cells characterization

These preferences are then transferred to the Schematic Editor before producing an Allegro PCB netlist (Figure 2).

SigXplorer (via the SPECCTRAQuest Floorplanner /Editor) can verify that simulation results from the routed PCB correspond to those obtained from the pre-layout analysis. While using the same simulator in both cases, there is an important difference between the models used. During pre-layout analysis, the user specified all relevant parameters such as line delays and impedances to allow SPECCTRAQuest to estimate the high-speed signal phenomena. For post-layout analysis, the program calculates these values directly from the board layout and stackup using a built-in 2-D electromagnetic field solver.

For each interconnect type of interest, the simulator searches its libraries for a corresponding electrical model. If no appropriate model exists, SPECCTRAQuest automatically derives one using the field-solver. This is then stored in the interconnect model library so the calculation is only necessary once for each specific cross-section.

While not providing the precision of other more specialised tools e.g. Ansoft's Maxwell, the solver aims to provide a good compromise between accuracy and computation time.

The SPECCTRAQuest SI Expert Simulation environment is called *SigNoise*. It embraces tools for entering and editing device models, simulating the circuit and displaying results. It uses a SPICE-type simulation engine that incorporates a lossy, coupled, frequency-dependent transmission line model valid to the tens of GHz region.

Traditionally, an important shortcoming in the PCB flow was that there was no formal means of passing design rules between different stages. The latest SPECCTRAQuest SI Expert release has seen an extension of the *Constraint Manager* application. This tool can manage high-speed electrical constraints across all stages of the design flow. These rules can be defined, viewed and validated at any step from schematic capture to floor planning and to PCB realization in Allegro. For example, an electrical constraint can be formally applied in Concept and carried through to the PCB layout stage. If the layout designer violates this constraint, it will be automatically flagged as an error. These new features are currently being evaluated at CERN.

B. IBIS models

SPECCTRAQuest is delivered with a built-in library of commercial driver and receiver models. However, the user sometimes needs to define a new device. A SPICE model could be used to describe fully a driver or receiver at transistor level but this approach has some serious disadvantages. One is the impractically long simulation times that could arise for a large circuit. Another is that IC manufacturers usually do not wish to disclose proprietary information regarding their processes.

An alternative approach is to describe devices according to the Input/Output Buffer Information Specification (IBIS) modelling standard [4]. Here, only the input and output stages are modelled and no attempt is made to represent the internal circuit structure. Two basic models have been defined for the standard (Figures 4, 5).

Contrary to the SPICE approach, the buffers are described using behavioural modelling only. A set of tables is used to represent various characteristics such as output stages pull-up or pull-down capabilities (using I-V relationships) and the output switching speed (using a V-t table).

This largely overcomes the disadvantages of the SPICE approach:

- The system simulates quickly as there is no circuit detail involved.
- The voltage/current/time relationships are defined only for the external nodes of the gates. This conceals both process and circuit intellectual property.

There are also programs available that can translate a SPICE netlist to an equivalent IBIS model. These have been used at CERN to characterise ASICS' output buffers [5].

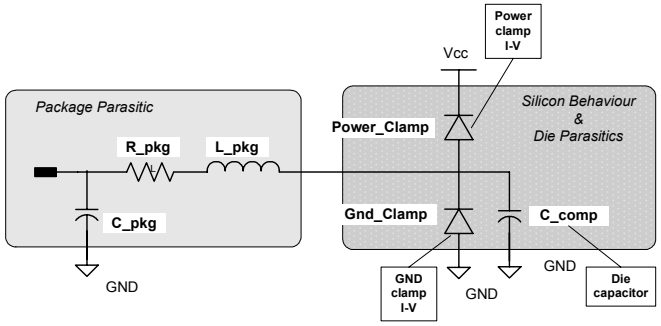

Figure 4: IBIS Buffer input stage definition

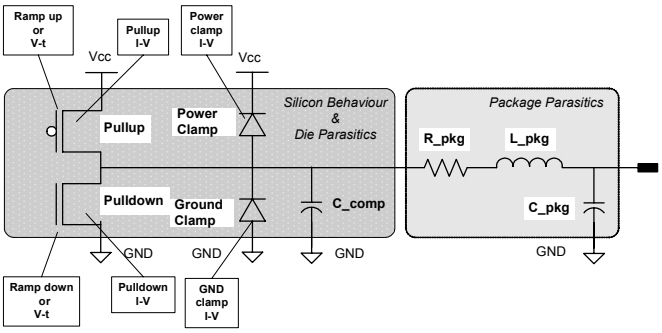

Figure 5: IBIS Buffer output stage definition

II. LHC Detectors Case Studies

We shall now give examples of how these tools have been applied during the development of LHC detector electronics.

A. FPGA Bus Design application for ATLAS LARG ROD Injector module

1) Project Overview

The Read Out Driver Injector module has been designed to debug the ATLAS Liquid Argon Calorimeter ROD system [6]. The module emulates the Front End Buffers output data and generates typical Timing, Trigger and Control signals.

2) Module description

During normal operation, a Front End Buffer module receives analogue signals from calorimeter cells. After amplification and shaping, these signals are digitised at 40 MHz sampling frequency and the resulting data sent to the ROD.

The injector module emulates 4 half-FEBs and the TTC signals (Figure 6). Each function is implemented in an ALTERA Flex 10K30E FPGA with data for each function stored in an associated 32Kwords SRAM memory. The module is built as a 9U VME64x card with a 16 bits data VME interface.

There are 3 separate data busses with the following characteristics:

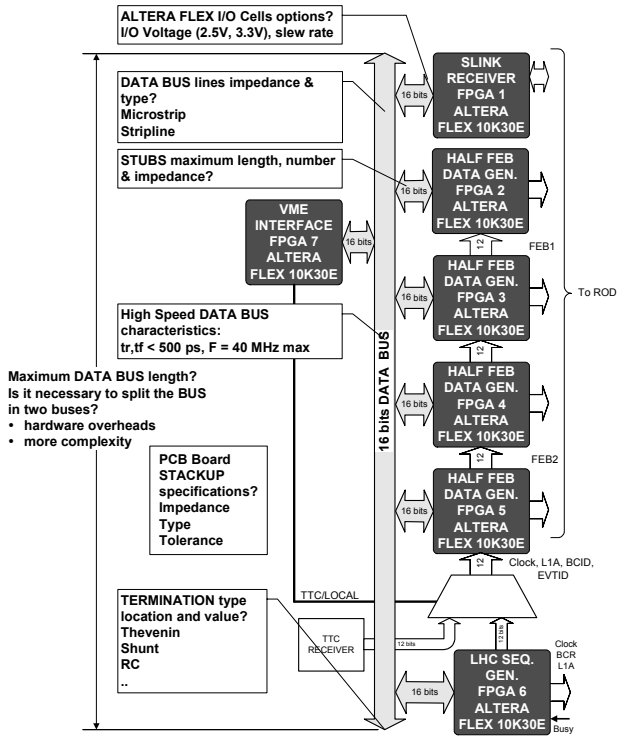

Figure 6: LARG ROD Injector Module

- A 12 bit unidirectional data bus links the Timing generator to the 4 half-FEB generators. Data on this bus is transferred at 40 MHz.
- A 16-bit bi-directional data bus and a 15-bit unidirectional address bus (this bus is not explicitly shown on Figure 7) link these functions to the VME interface. The busses are sampled at 40 MHz but data is transferred at VME bus rates.

3) Design choices and layout recommendations

An extensive pre-layout analysis was undertaken on the system busses and the clock distribution system. This allowed some significant decisions to be made already at this early stage.

The analysis was based on a multipoint bus using ALTERA FLEX 10K30E devices with tf < 500pS. Using the recommended design choices and layout rules ensures that signals switch on the first incident wave with at least 500mV positive noise margin at sampling time. The important conclusions include:

- It is possible to use a single 300mm long DATA BUS with these devices if proper termination is used (see below). This avoids the complication of splitting the bus into two or more segments.
- Only one termination scheme was found to provide consistently good results. This was a combination of an AC termination (R= 100 Ohm, C=1nF) at both DATA_BUS ends complemented by 4.7 Ohms STUBS SERIES terminations added near the DATA BUS. The latter was needed to lower stubs and

package impedance effects. DC termination could not be used as it overloaded the driver fan out capabilities.

- DATA BUS lines impedance and type were confirmed to be capable of being manufactured as a class 5, 8-layer PCB. Calculations were made for a line impedance of 70Ω with a +/- 20 % tolerance – this was evaluated using SigXplorer's sweep parameters functionality.
- Simulations showed that stub lengths could be at least 10 mm.
- Simulation showed that design was robust enough to allow working with worst-case driver/receiver combinations as regards switching speeds and IC location.

4) Post-layout check before board manufacture

The guidelines were implemented in the PCB layout phase. Prior to board manufacture, all critical parameters (time propagation delay, skew, first incident wave, noise margin) were verified and found to be satisfactory.

5) Module state and future development

A prototype is fully functional and integrated with the ROD in the current DAQ environment.

B. GTL Bus Design case study for ALICE pixel chip carrier

1) Project overview

The ALICE Silicon Pixel Detector (SPD) is located within the Inner Tracking System (ITS) and is the detector with the highest active channel density. The Pixel Carriers have been designed to physically support the detector ladders, power them and to carry signals between the pilot and the readout chips.

2) Module description

Figures 7 and 8 show different views of the ALICE pixel chip carrier [7]. 10 Readout chips are connected to the data bus by bonding wires. The data is then fed to the I/O Cells Pilot chip via a series of "vertical" and "horizontal" lines.

3) Design choices and layout considerations

Due to its position in the active area, the board has to be as transparent as possible to physics particles. This physical constraint eventually led to a choice of a 200µm thick, 6-layer aluminium/polymide PCB. This has important implications for the electrical characteristics. Due to the small PCB thickness and the need for fine lines, the track impedances become uncomfortably low compared to the driver impedance and to its current capabilities. There is also another mismatch problem as the horizontal and vertical lines have different characteristic impedances. Detailed analyses were performed to confirm that the system would still work acceptably under these sub-optimum conditions. Important design points are:

- The horizontal data-bus microstrip-lines signals were estimated to have an impedance of 19Ω. The vertical lines were calculated to be nominally 9Ω.
- For these lines and I/O cells, the optimum pull-up termination was found to be 22Ω on one end only of the PCB.
- The PIXEL chip was designed with GTL-like I/O technology with output-cells switching speeds selectable from 4 to 30ns. Simulations were made at 4, 7 and 20ns with virtual silicon using IBIS models created at CERN from the HSPICE netlist.

The complete assembly was fully analysed before delivery of the Carrier PCB or chips with a full load of 10 pixel chips for all three switching times. The crosstalk was estimated as being less than 120mV Root Sum Square.

This figure has not yet been measured on hardware.

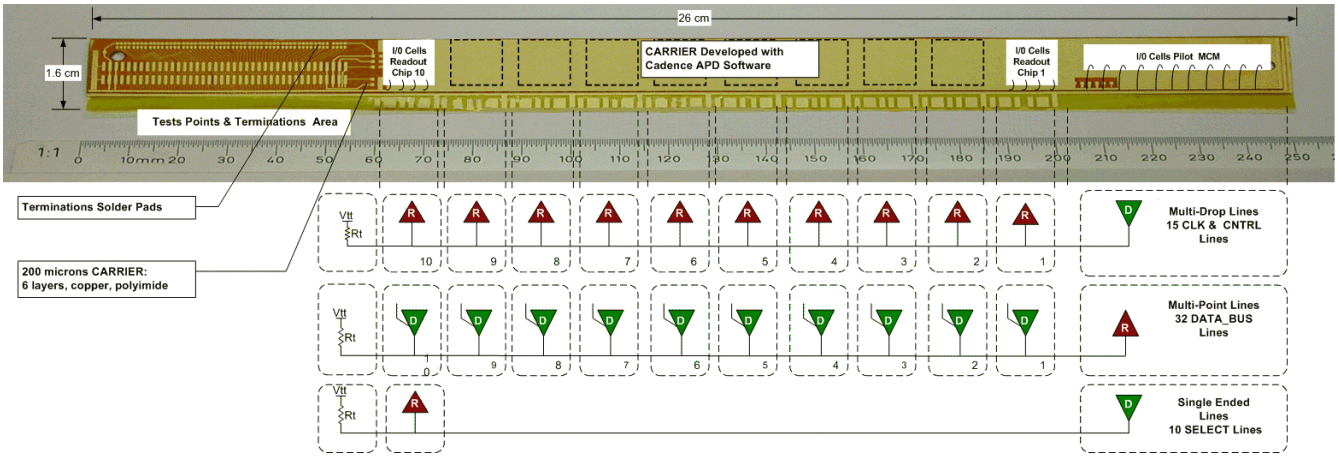

Figure 7: ALICE Pixel Chip Carrier

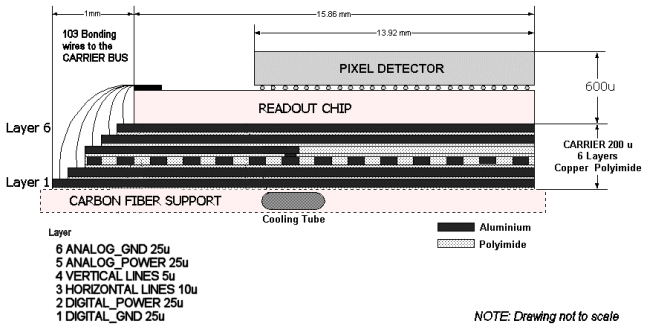

Figure 8: ALICE Pixel System Detector

III. CONCLUSIONS

Signal integrity analysis is essential for designing reliable sub-nanosecond switching-time circuits. We have described SPECCTRAQuest and shown how it can help with all aspects of the design flow from circuit design choices to PCB layout. We have given examples of how it has been used to help in validating IC technology choice and in developing placement and routing guidelines for the layout designers.

Future developments will include the deployment of the "Constraint Manager" to automatically manage high-speed electrical constraints across all design-flow stages. We also hope to evaluate the SUN/Cadence "Power Integrity" module to address the issues of correct power-plane design.

The SPECCTRAQuest SI Expert tools are presently available at CERN and fully supported by IT/CE-AE [9].

IV. ACKNOWLEDGEMENTS

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