Power Supply and Power Distribution System for the ATLAS Silicon Strip Detectors

J.Bohm[A], V.Cindro[D], L.Eklund[E], S.Gadomski[C&E], E.Gornicki[C], A.A.Grillo[I], J.Grosse−Knetter[E], S.Koperny[B], G.Kramberger[D], A.Macpherson[E], P.Malecki[C], I.Mandic[D], M.Mikuz[D], M.Morrissey[H], H.Pernegger[E], P.W.Philips[H], I.Polak[A], N.A.Smith[F], E.Spencer[I], J.Stastny[A], M.Turala[C], A.Weidberg[G]

ATLAS SCT Collaboration

[A] Academy of Sciences of the Czech Republic, Prague, Czech Republic

[B] Faculty of Physics and Nuclear Techniques of the UMM, Cracow, Poland

[C] Institute of Nuclear Physics, Cracow, Poland

[D] Josef Stefan Institute and Department of Physics, University of Ljubljana, Ljubljana, Slovenia

[E] CERN, Geneva, Switzerland

[F] Department of Physics, Oliver Lodge Laboratory, University of Liverpool, Liverpool, UK

[G] Department of Physics, Oxford University, Oxford, UK

[H] Rutherford Appleton Laboratory, Chilton, Didcot, UK

[I] Institute of Particle Physics, University of California, Santa Cruz, CA, USA

Piotr.Malecki@ifj.edu.pl

Abstract

The Semi−Conductor Tracker of the ATLAS experiment has modular structure. The granularity of its power supply system follows the granularity of the detector. This system of 4088 multi−voltage channels providing power and control signals for the readout electronics as well as bias voltage for silicon detectors is described.

Problems and constraints concerning power distribution lines are also presented. In particular, optimal choice between concurrent requirements on material, maximum voltage drop, space available for services, assembly sequence etc. is discussed.

I. Power Supply System for the ATLAS SCT

The ATLAS SCT detector[1] consists of 4088 modules of which 2112 form four barrel cylinder layers and 1976 are mounted on end cap wheels. Single−sided micro−strip detectors are glued back−to−back to form one double−sided module with 1536 strips. The module is equipped with a hybrids, a small boards carrying 12 ABCD3T readout chips and electronics to transfer digital data from and to SCT modules. Present barrel and end cap hybrids are substantially different in many aspects but identical from the point of view of power supplies.

A. Basic design principles

The ATLAS SCT readout chips and electronics for the optical transmission of digital data to the off−detector stations (as well as timing, trigger and control data to SCT modules) require several low voltage supplies. In addition silicon micro−strip detectors operating in the LHC high radiation environment require the bias voltage which can be regulated in 0 − 500 V range.

SCT power supply and power distribution system has been designed according to following basic requirements:

- modularity of the power supply system follows the modularity of the detector,
- power supply modules are fully isolated and voltages in modules are "floating",
- every detector module is powered by separate, multiwire line (tape or cable).

In the context of this article it seems appropriate to underline that among other consequences for the detector performance the above mentioned design rules allow for the maximum flexibility in selection of optimal shielding and grounding scheme

B. Requirements for Low Voltage power supplies

Present requirements[2] for low voltage power supplies result from several iterations of readout chip design and from many beam and radiation tests of module prototypes. Main objects of concern are Vcc, "analog" voltage supplying analog circuits of the readout chip, and Vdd, "digital" voltage supplying digital part of the ABCD3T chip, as well as electronics for the optical links (DORIC4 and VDC ASICs). These two voltages should provide relatively high currents of the order of 1A. Their load may, in addition, vary over a wide range.

Low voltage power supply channel should also provide several low power voltages and control signals: bias voltage for the photodiode, control voltage for VDC ASIC, voltage (two current sources) for the temperature monitoring, module reset and clock select signals. Nominal values for voltages and signal levels with typical and maximal loads are listed in Table 1. The inclusion of these extra power and control signals, as well as the temperature readout mentioned in section G below, in the low voltage supply channel is to insure a common reference potential for all electrical signals on the detector module. This minimises the possibility for electrical pick−up or extraneous noise.

Table 1: LV Power Requirements

Name	Nominal value [V]	Current [mA]	Max. Current [mA]
Vcc	3.5	900	1300
Vdd	4.0	570	1300
VCSEL	1.6 − 6.6	6	8
PIN bias	10.0	0.5	1.1
Current source 0	Max. 8.0	0.08	
Current Source 1	Max. 8.0	0.08	
RESET	Vdd/−0.7	0.4	
SELECT	Vdd/−0.7	1.3	

These main requirements, together with others referring to voltage setting resolutions, voltage and current monitoring accuracy, over voltage and over current trip limits and maximum output ripple, lead to specifications for LV power supplies which have recently been fixed [2].

C. HV requirements

Bias voltage power supplies should provide stable, digitally controlled voltage in 0 − 500 V range and precise measurement of the output current in 40 nA −5 mA range. One should be able to set the current trip limit individually for each channel in range from hundreds nA to 5 mA as well as select one of the predefined voltage ramping rates: 50, 20, 10, 5 V/s. It is also required that the maximum allowable noise level is not higher than 40 mV peak to peak[3].

D. Basic block characteristics

Several low voltage modules are grouped onto one board equipped with the board micro−controller. The low multi−voltage power module[4] consists of separate floating supplies for analog and digital voltages. Each module is controlled and monitored by its own micro−controller which receives commands and receives or transmits data to/from the board micro−controller.

The HV power module has very similar structure and similar basic components: rectifier, filter, regulator, error amplifier, DAC and ADC.

Two voltages of a relatively high current, Vcc and Vdd, differ from others by using sense wires. This is necessary for the considerable resistance of each transmission line and hence the considerable voltage variation at the module side in response to variations of the current draw. Analog data from sense wires is converted to digital and processed by the channel micro−controller for the appropriate output voltage adjustment.

LV and HV channels are powered from the 48V, 48 kHz square wave generators. An isolation of individual channels and individual voltages is realised by HF transformers on the power path and by optical couplers on communication lines.

More details concerning design and performance of prototypes of the LV power supply modules are in ref. [4]. HV power supply module design has been presented in the Proceedings of the previous, 6−th Workshop on Electronics for the LHC Experiments [5].

E. LV/HV integration

Low and high voltage power supplies form together one system. Multi−channel LV and HV 6U cards are integrated in common 19'' EURO crate equipped with the custom back plane, the crate controller, the interlock card, and a common power pack. One crate will house 48 SCT power supply multi−voltage channels mounted on 12 LV cards, 4 channels each, and on 6 HV cards, each containing 8 channels.

All cards in one crate are supplied from the crate 1.6 kW power pack which provides 48V, 48 kHz square wave

for HF transformers and DC supply for the commercial crate controller as well as for all card controllers.

All SCT LV power supply cards are identical. Similarly, there is full interchangeability between HV power supply cards. The card address and consequently the channel address is determined from the card position in the crate. The custom back plane design predefines positions for LV and HV cards. The mechanical construction prevents card misplacement.

It has been decided to use commercial crate controller which communicates within the crate with the eighteen card controllers via parallel 8−bit bus. This communication is serviced by a simple and efficient custom made protocol.

The crate controller is equipped with the CAN bus interface for communication with the higher levels of the Detector Control System.

Custom back plane bears on the back side special 48 connectors for the multi−wire cables which connect power supply modules with the first patch panel (PP3) on the way to detector modules. These connectors (CONEC 17W5) have five thick pins allowing for connection of four high cross section wires and another wire with hv insulation. Twelve thin pins serve the rest of low current lines (of which one is reserved for the drain wire of the cable).

F. Location of power supplies

The choice of the power supplies location has important implications on the power distribution system, discussed in the next section, as well as on the power supply design and specifications. For example, the maximum power path length determines the maximum voltage drop and hence the maximum output voltage which power supply must provide to reach the nominal value at the detector side. Anticipating some results of the following discussion it is worth to mention here that the Vcc supply should be designed for the maximum output voltage of 8.75 V and Vdd for 9.33 V to be able to provide the nominal values on the detector module side in the case of the maximum voltage drop (with 1 V margin included)[2].

The standard location for the off−detector electronics is in the cavern (named USA15) next to the detector hall. For such location the length of the power path will be in range of 100 − 130 m. SCT plans to locate 50% of its power supply crates in another cavern, on the other side of ATLAS detector (named US15). This will shorten the path length by 30 − 40 m for that part of modules, making the longest path about 100m.

II. Power Distribution for the ATLAS SCT

About 23 kW are needed for the normal operation of the ATLAS SCT. The delivery of that power to the inner part of the Inner Detector can not be done without extra material, more power dissipation, space for services, cost etc. In the following short review we will concentrate on a group of requirements which mostly concern high current lines for Vcc and Vdd voltages. Grounding and shielding problems, which are very important for the system of thousands of wires distributed over large surfaces, are discussed elsewhere [6].

G. List of lines

In the following list the first four lines, out of all seventeen, should have considerably larger cross section to conduct high current, 1.3 A maximum. All other lines can practically use as thin conductor as technologically possible.

1. Vdd − digital voltage
2. DGND − digital ground
3. Vcc − analog voltage
4. AGND − analog ground
5. HV − bias voltage
6. Hvgnd − bias ground
7. Vddsense
8. DGNDsense
9. Vccsense
10. AGNDsense
11. VCSEL − driver
12. SELECT − clock redundancy
13. RESET − clock
14. PIN − diode bias
15. TEMP1 − sensor
16. TEMP2 − sensor
17. drain wire

Several voltages (VCSEL, SELECT, RESET, PIN.TEMP1, TEMP2) use the digital ground, DGND, as the common return. In all present tests of SCT module prototypes analog and digital grounds are directly connected. AGNDsense and DGNDsense wires sense then the same point but it has been agreed to keep both lines as the present laboratory practice may not be continued in the final installation.

H. Conflicting requirements

The design of the power delivery system for the detector located in the innermost part of the ATLAS experimental setup should satisfy several conflicting requirements. One should minimise material, voltage drop, power dissipation and costs. One should observe rules concerning the radiation hardness of and flame resistance of materials used. The design is also strongly influenced by the limited space for services as well as by the foreseen assembly sequence.

An optimisation process has different priorities in different regions of the detector. Consequently, it has been decided to divide the power path between the SCT modules and power supplies into four parts.

I. 4−fold way

Final design of the power distribution system for the ATLAS SCT is in progress and is closely related to the process of integration of all services.

1) Low mass tapes

In the innermost part material introduced by cables seems to be the most critical parameter. This first part, from detector modules to the first patch panel (PPB1 for the barrel, PPF1 for end cap modules) located at the cryostat wall, is served by low mass tapes [7]. These tapes are made from 25 micron thick Kapton and 25 micron glue substrate with 50 micron aluminium conductors covered by another Kapton and glue layer of 25 micron. The width of conductor lines as well as the space between conductors can −for technological reasons −be made in steps of 0.5 mm. Our four critical lines (for Vcc and Vdd) are chosen to be 4.5 mm wide while all other lines have the minimal allowable width of 0.5 mm. The length of these tapes is in range 0.7 − 1.6 m for barrel modules and reaches about 3 m for some of end cap modules. A contribution to the material budget is often characterised by calculating a cumulative amount of material in certain region of the detector and "dilute" it over some characteristic surface. An example for 6 tapes serving one barrel half stave averaged over the surface of one module shows the material contribution of about 0.24% of Xo.

Total maximum power dissipated by low mass tapes is estimated on about 3 kW. Maximum voltage drop for some barrel tapes reaches 0.6V and for end cap tapes 1 V.

2) "Very thin" cables

It is estimated[8] that the distance from the PPB1 (barrel) to the next patch panel PP2 should not exceed 9 m and the corresponding one for the end cap (PPF1 − PP2) 5 m. Final numbers depend on the PP2 location and details of routing, subject of the decision of the ID coordination.

We have originally planed to use Al on Kapton tapes also for this part, but with the conductor thickness increased to 100 micron. As the maximum allowable voltage drop become the most critical parameter it has been decided to use the copper conductors.

Maximum allowable voltage drop requires special attention because if it exceeds certain limit then, in case of a sudden loss of load, the safe limit of 5.5 V for the readout chip is exceeded.

It is planned to use the multi−wire round cable of 6 mm outer diameter, with a thin Kapton insulation and with the four high current lines of 0.6 mm^2. With such choice the maximum voltage drop will not exceed 1.6 V for Vcc or 1.4 for Vdd what is safe providing that the some voltage limiters are installed on the PP2. These limiters seem to be unavoidable since another 2V drop has still to be considered for the rest of the power path.

3) Thin conventional cables

For the part which extends from patch panels PP2 and PP3 of length of about 20 m it is planned to use multi−wire "conventional" cable[8] with somewhat complicated geometry taking into an account the requirement of twisting wires in groups belonging to the same voltage (e.g. Vcc, AGND, Vccsense and AGNDsense). With such requirement the cable outer diameter is about 12 mm with the cross section of our four critical lines equal 1 mm^2. Maximum voltage drop for that part is estimated on 1.3 V.

4) Thick conventional cables

The distance from PP3 to power supply crates depends on the final location of PS racks. ATLAS SCT considers use of two locations in caverns on both sides of the detector hall. That will considerably shorten the path for thick conventional cables, and hence reduce power dissipation, cost etc. The multi−wire cable[8] with the geometry similar to the thin conventional cable will have the four critical lines with the 4 mm^2 cross section and the outer diameter of about 20 mm. The estimated maximum voltage drop equals about 1V.

J. Final remarks

The power distribution system for the ATLAS SCT is in the development state. Several elements require final design and tests. In particular:

- final construction and location of patch panels as well as final details of routing of cables. This depends strongly on the overall process of integration with other subsystem and involves some coordination on the level of the Inner Detector
- full power dissipation by cables in all four regions is estimated on 10 kW (for nominal currents and maximal cable lengths)[8]. To satisfy the "rule of thermal neutrality" of each subdetector one has to find solution for the cable cooling in some regions
- total voltage drop along power lines considerably exceeds the safety limit for the readout ASICs and some voltage limiters have to be installed in the region of PP2. An appropriate voltage limiter circuit has been designed for PP2 and is now undergoing system and radiation testing
- PP3 is being designed with common−mode inductors to filter unwanted pick−up from the long cable runs from the power supplies. Prototypes have been tested in the system test and have been shown to be quite beneficial.

III. References

1. ATLAS Inner Detector TDR Volume 2 CERN/LHCC/97−17 p 385

2. J.Bohm, SCT Week Prague 25 − 29 June 2001 http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/SCT/sct_meetings.html
3. http://www.ifj.edu.pl/ATLAS/sct/scthv/
4. http://www−hep.fzu.cz/Atlas/WorkingGroups/ Projects/MSGC.html
5. P.Malecki. Multichannel System of Fully Isolated HV Power Supplies or Silicon Strip Detectors, 6−th Workshop on Electronics for LHC Experiments. CERN/LHCC/2000−041. p.376
6. Ned Spencer. ATLAS SCT/Pixel Grounding and Shielding Note. Nov 22. 1999. UCSC. EDMS Id:108383, Number ATL−IC−EN−0004 v.1
7. http://merlot.ijs.si/~cindro/low_mass.html
   http://www−f9.ijs.si/atlas/
8. H.Pernegger.Services in:
   http://perneg.home.cern.ch/perneg/